



# MS-96A9 Ver:0A

## CPU:

Intel Penryn

## System Chipset:

Intel CANTIGA

Intel ICH9M-E

## On Board Chipset:

WINBOND Super I/O -- W83627DHG

LAN1 -- Intel 82573LM

LAN2 -- 82567LM Boazman

HD Codec --ALC888

BIOS -- SPI ROM 4MBit

## Main Memory:

DDR \* 2 (Max 8GB)

## Expansion Slots:

PCI-EX16\*1

PCI-EX4\*1

PCI 2.2 Slot X 2

## PWM:

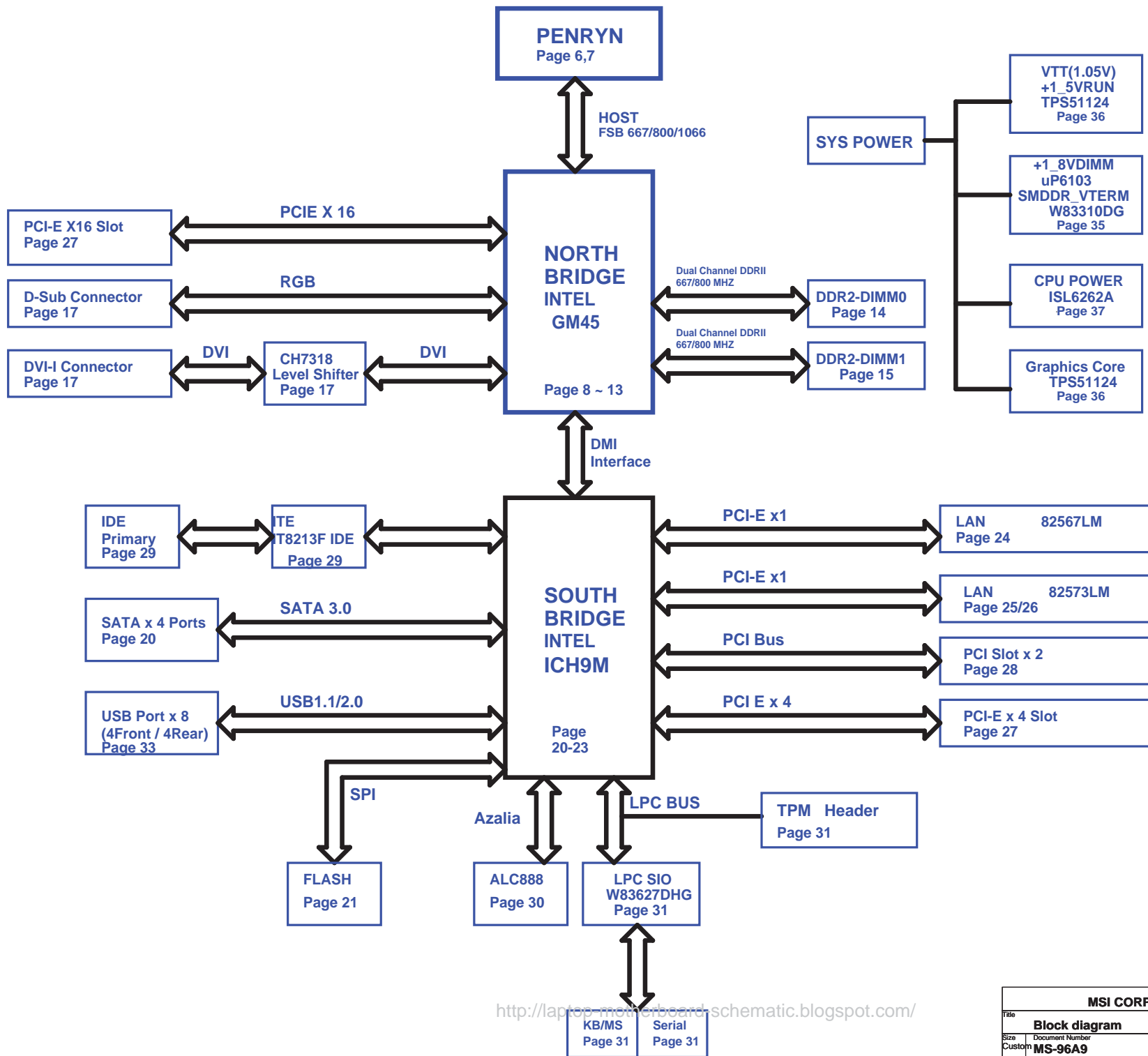
Controller--Intersil ISL6262A 2 Phase

## Clock Generator:

Controller--ICS9LPRS113

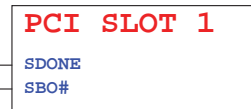
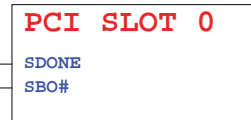
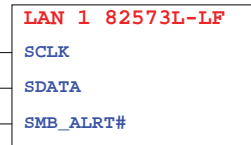
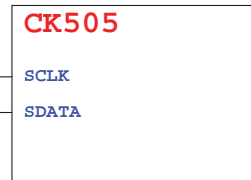
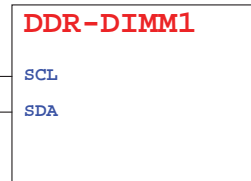
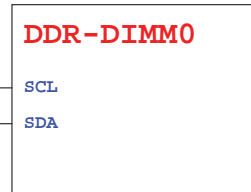
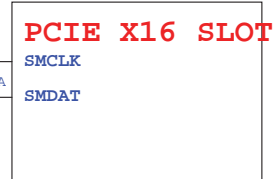
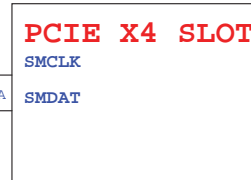
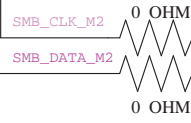
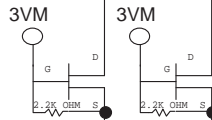
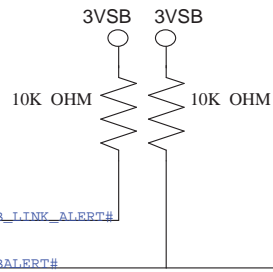
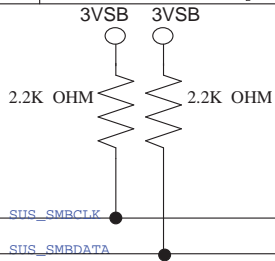
Title	Page
Cover Sheet	1
Block diagram	2
System SMBus Block	3
System Reset and Power on MAP	4
System Clock	5
Penryn (HOST BUS)	6
Penryn (POWER/GND)	7
CANTIGA-1 (HOST BUS)	8
CANTIGA-2 (DMI/VGA)	9
CANTIGA-3 (DDR)	10
CANTIGA-4 (POWER-1)	11
CANTIGA-5 (POWER-2)	12
CANTIGA-6 (VSS)	13
DDR2 DIMM 0	14
DDR2 DIMM 1	15
DDR2 TREMINATION	16
CH7318 VGA, DVI	17
D-Sub 15Pin Video Connector	18
CLOCK GEN	19
ICH9M-1 (CPU/IDE/Azalia)	20
ICH9M-2 (PCI/USB/PCIE/DMI)	21
ICH9M-3 (SM BUS/GPIO)	22
ICH9M-4 (POWER/GND)	23
LAN(82567)	24
LAN1_82573L Signal	25
LAN1_82573L Power&Connect	26
PCI -Express X 16/4 Port	27
PCI 0,1	28
ITE/IT8213F IDE	29
AZALIA CODEC(ALC888)	30
SIO W83627DHG(KBC/EC/uP )	31

Title	Page
FAN,ATX	32
Front Panel	33
USB	34
POWER 5VDIMM/3VSB/+1.5V	35
POWER VTT_DDR/+3VM/+3VM_WOL/+1.8VDIMM	36
M_Graphics Core +1.05VM/VTT	37
M_CPU power V_CORE	38
Screw/EMI	39
GPIO BUFFER	40
POWER MAP	41



<http://laptop-motherboard-schematic.blogspot.com/>

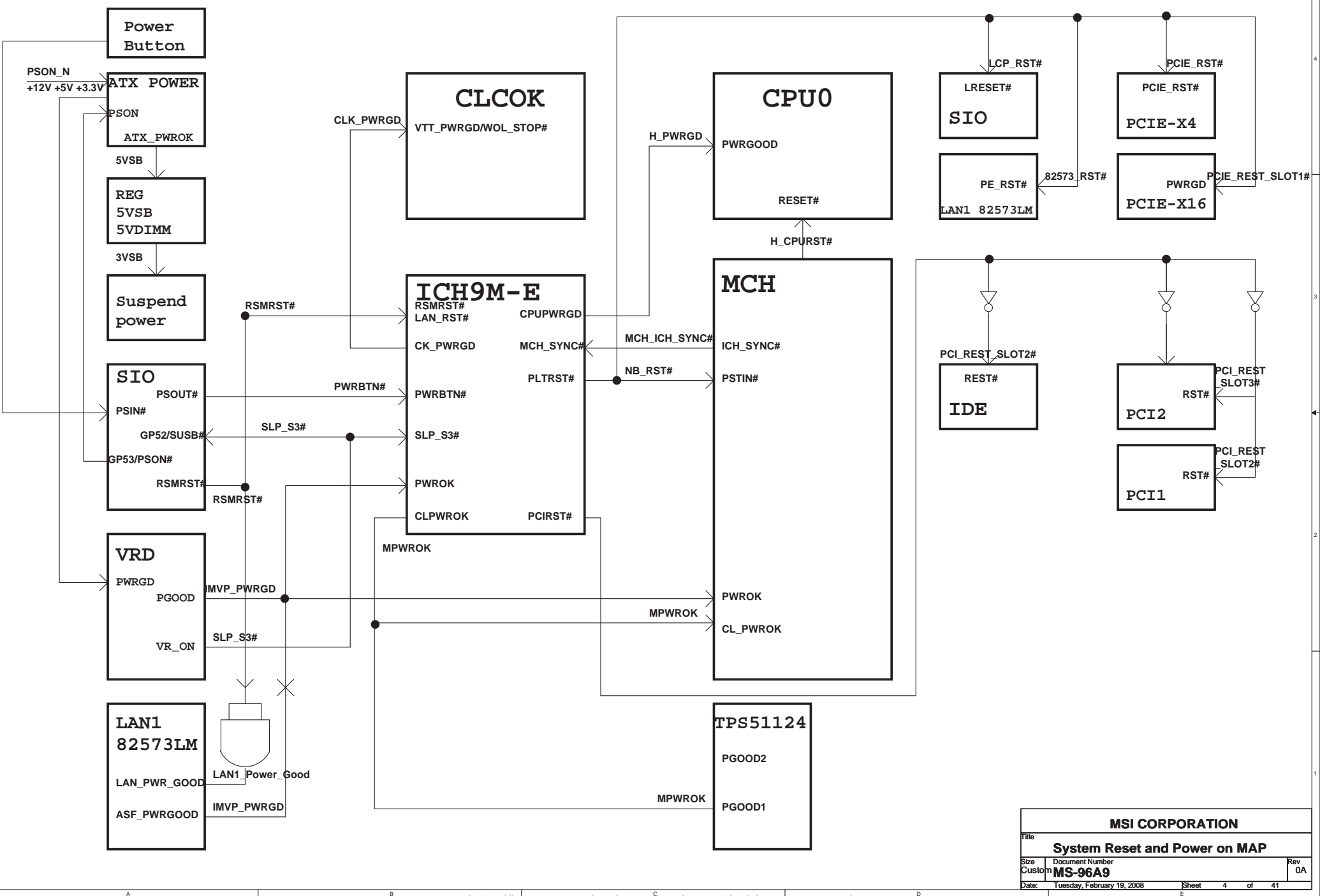
<b>MSI CORPORATION</b>			
Title <b>Block diagram</b>			
Size	Document Number	Rev	
Custom	<b>MS-96A9</b>	0A	
Date:	Tuesday, February 19, 2008	Sheet	2 of 41



<http://laptop-motherboard-schematic.blogspot.com/>

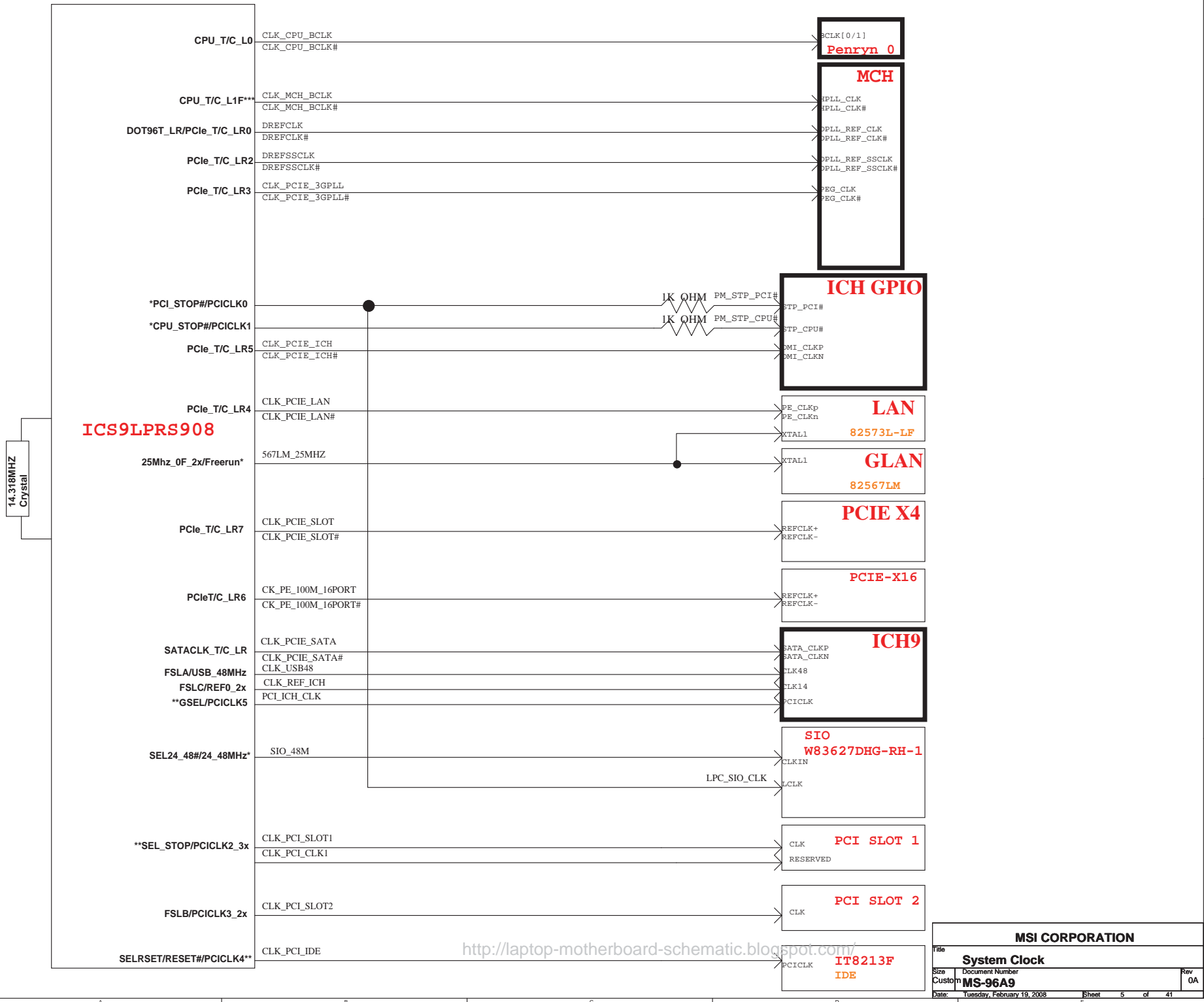
<b>MSI CORPORATION</b>			
File	<b>System SMBus Block</b>		
Size	Document Number		Rev
Custom	<b>MS-96A9</b>		0A
Date:	Tuesday, February 19, 2008	Sheet	3 of 41

# MS-96A9 SYSTEM RESET & POWER ON SEQUENCING BLOCK DIAGRAM



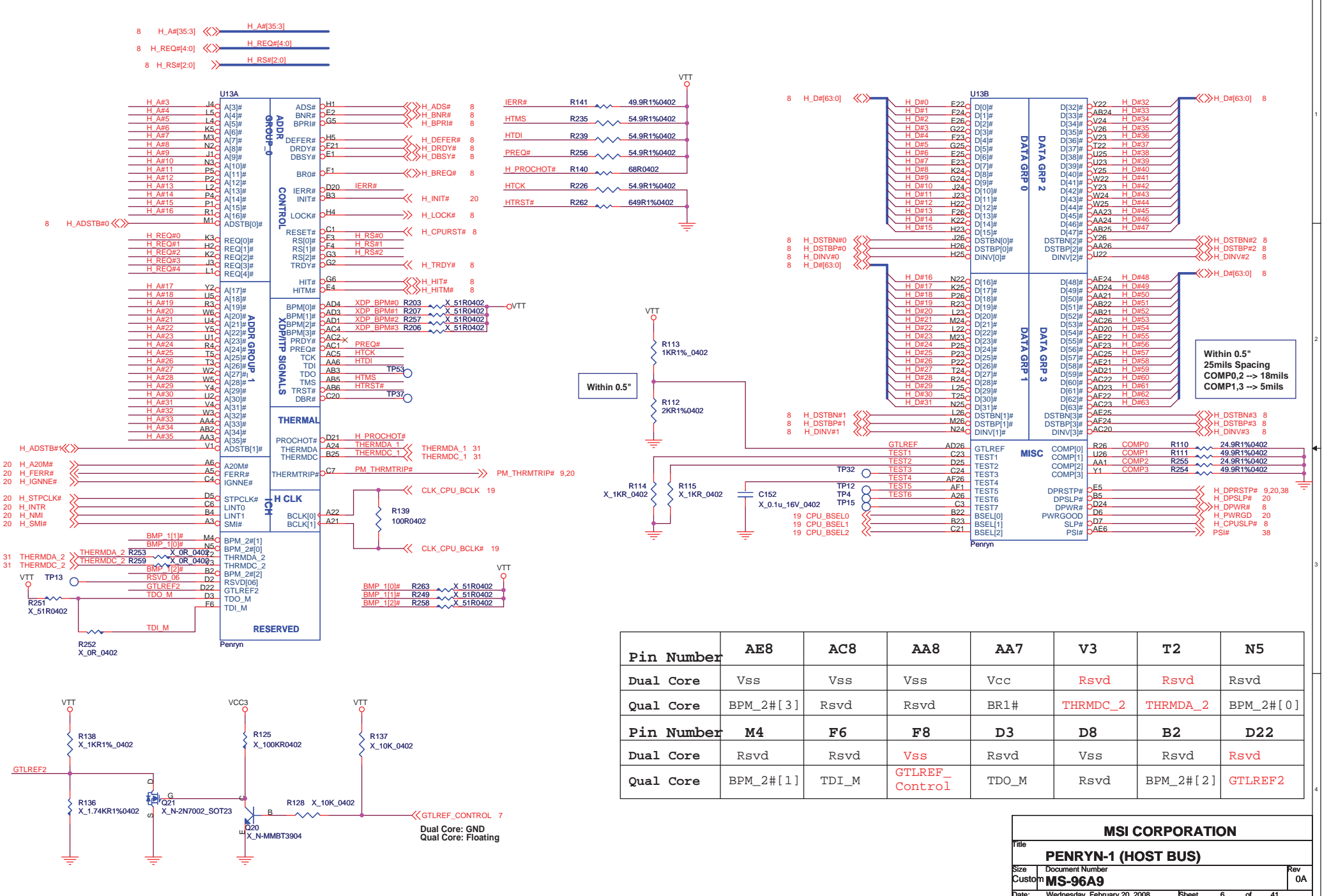
<b>MSI CORPORATION</b>			
File: <b>System Reset and Power on MAP</b>			
Size	Document Number	Rev	
Custom	<b>MS-96A9</b>	0A	
Date:	Tuesday, February 19, 2008	Sheet	4 of 41

# MS-96A9 CLOCK BLOCK DIAGRAM



<http://laptop-motherboard-schematic.blogspot.com/>

<b>MSI CORPORATION</b>		
Title	<b>System Clock</b>	
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	<b>0A</b>
Date:	Tuesday, February 19, 2008	Sheet 5 of 41



Within 0.5"

Within 0.5"  
25mils Spacing  
COMP0,2 --> 18mils  
COMP1,3 --> 5mils

Pin Number	AE8	AC8	AA8	AA7	V3	T2	N5
Dual Core	Vss	Vss	Vss	Vcc	Rsvd	Rsvd	Rsvd
Qual Core	BPM_2#[3]	Rsvd	Rsvd	BR1#	THRMD_2	THRMDA_2	BPM_2#[0]
Pin Number	M4	F6	F8	D3	D8	B2	D22
Dual Core	Rsvd	Rsvd	Vss	Rsvd	Vss	Rsvd	Rsvd
Qual Core	BPM_2#[1]	TDI_M	GTLREF_Control	TDO_M	Rsvd	BPM_2#[2]	GTLREF2

**MSI CORPORATION**

**PENRYN-1 (HOST BUS)**

File: **MS-96A9**

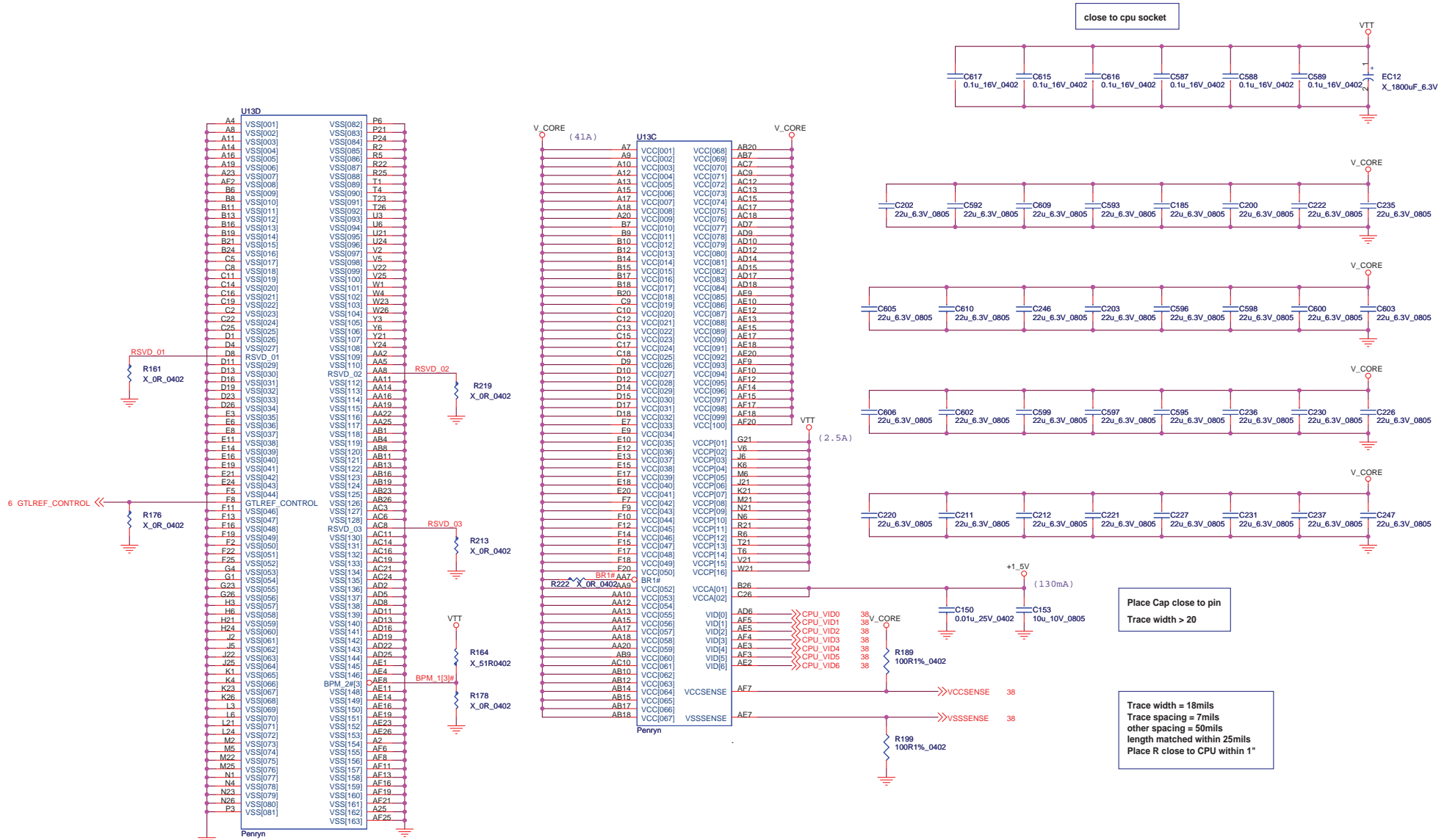
Size: **MS-96A9**

Customer: **MS-96A9**

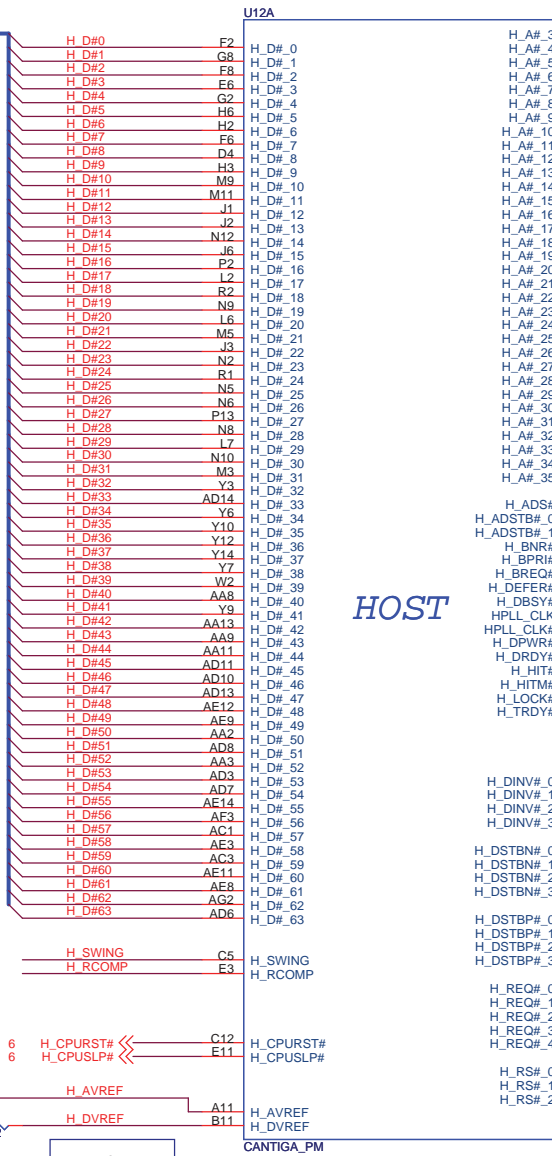
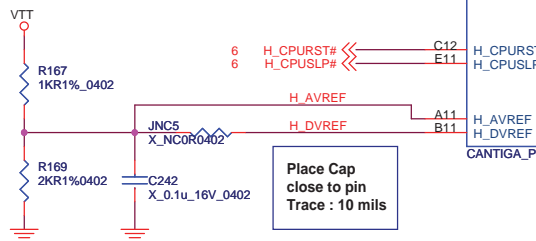
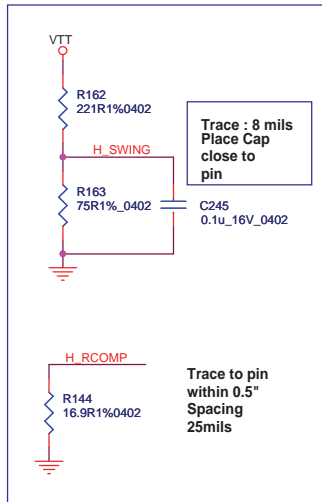
Date: **Wednesday, February 20, 2008**

Sheet: **6** of **41**

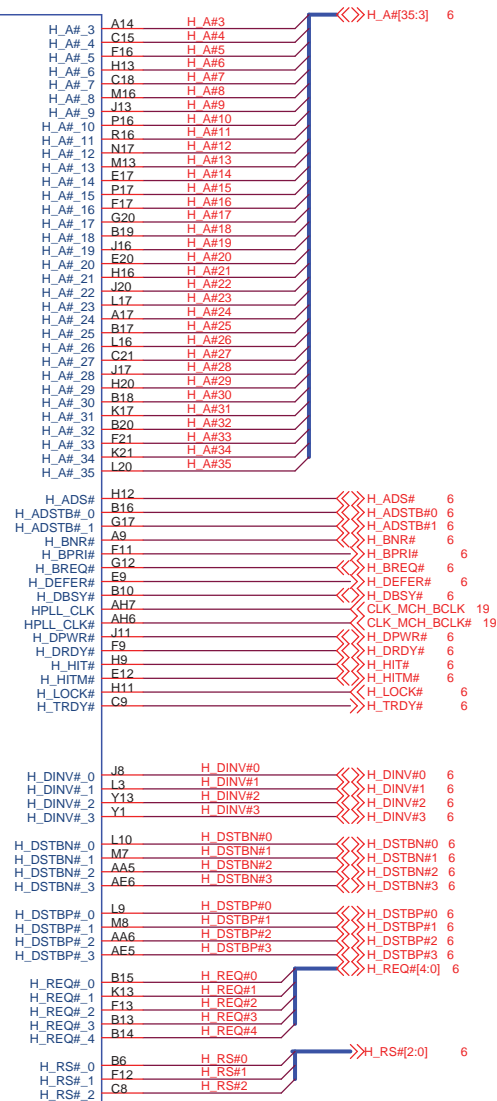
Rev: **0A**



MSI CORPORATION			
Title	PENRYN-2 (POWER/GND)		
Size	Document Number		Rev
Custom	MS-96A9		0A
Date:	Wednesday, February 20, 2008	Sheet	7 of 41

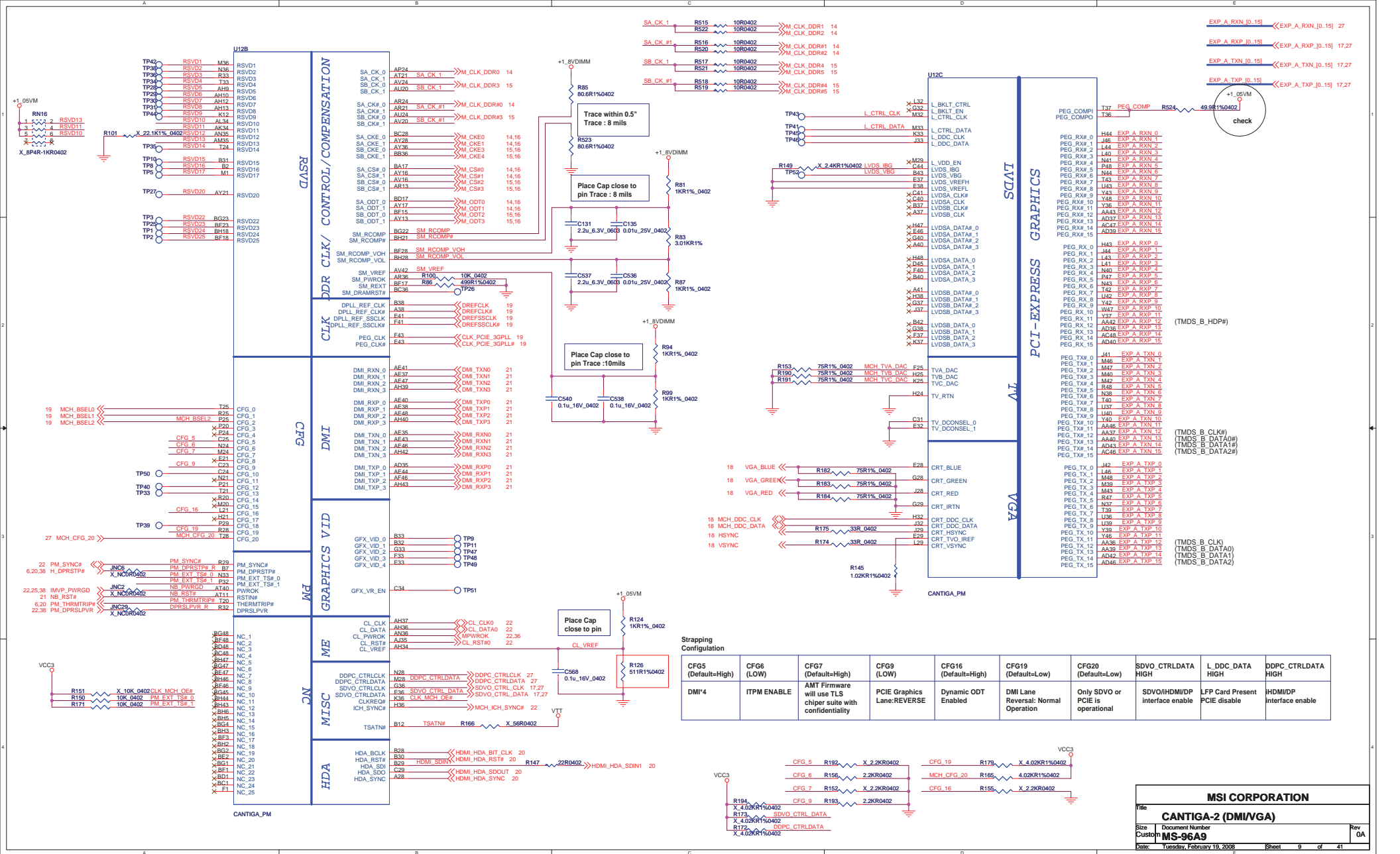


HOST



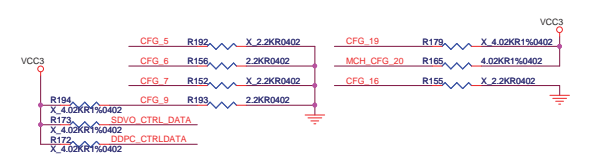
<b>MSI CORPORATION</b>		
Title		
<b>CANTIGA-1 (HOST BUS)</b>		
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	0A
Date:	Tuesday, February 19, 2008	Sheet 8 of 41





Strapping Configuration

CFG5 (Default=High)	CFG6 (LOW)	CFG7 (Default=High)	CFG9 (LOW)	CFG16 (Default=High)	CFG19 (Default=Low)	CFG20 (Default=Low)	SDVO_CTRLDATA HIGH	L_DDC_DATA HIGH	DDPC_CTRLDATA HIGH
DM14	ITPM ENABLE	AMT Firmware will use TLS chip set with confidentiality	PCIe Graphics Lane: REVERSE	Dynamic ODT Enabled	DMI Lane Reversal: Normal Operation	Only SDVO or PCIe is operational	SDVO/HDMI/DP interface enable	LFP Card Present PCIe disable	HDMI/DP interface enable



**MSI CORPORATION**

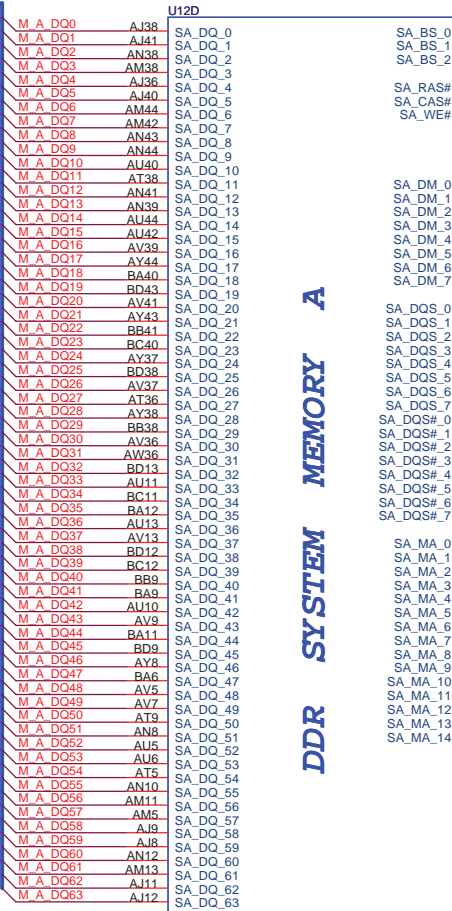
Part Number: **CANTIGA-2 (DMI/VGA)**

Rev: **0A**

Date: Tuesday, February 19, 2008

Sheet 9 of 41

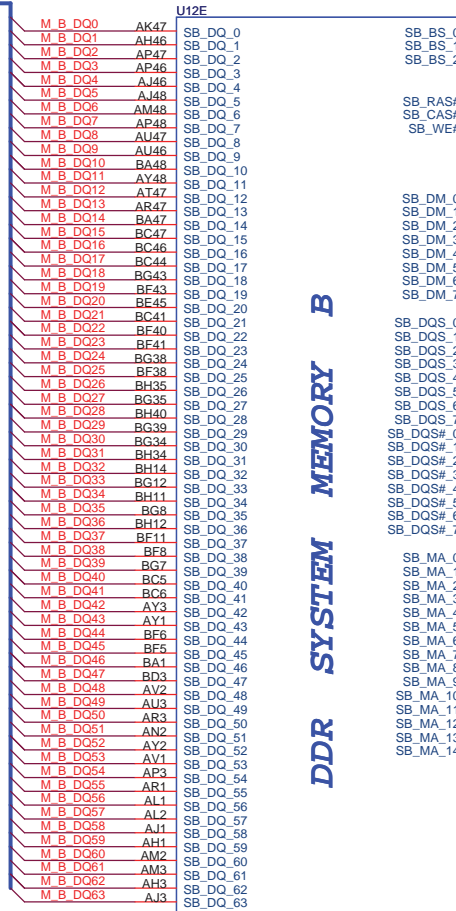
14 M\_A\_DQ[63:0] <<<



DDR SYSTEM MEMORY A

CANTIGA\_PM

15 M\_B\_DQ[63:0] <<<



DDR SYSTEM MEMORY B

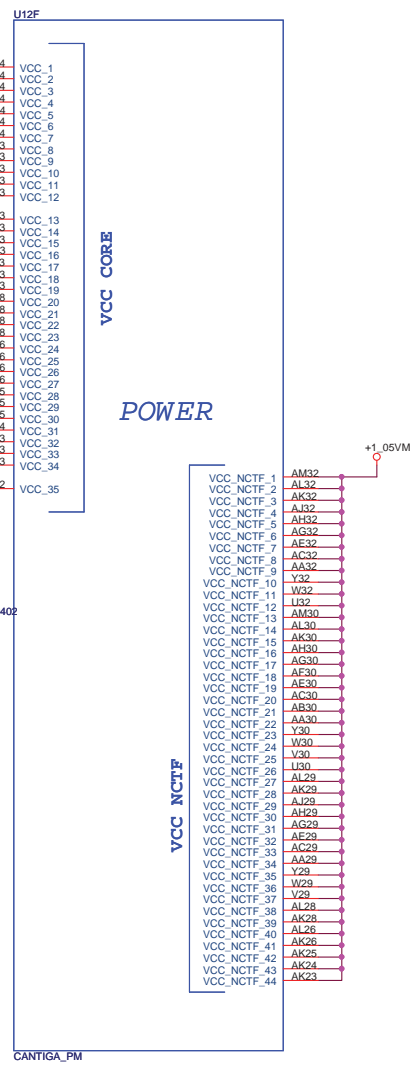
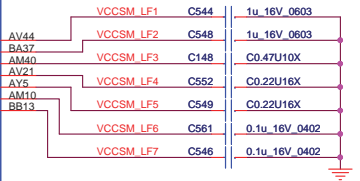
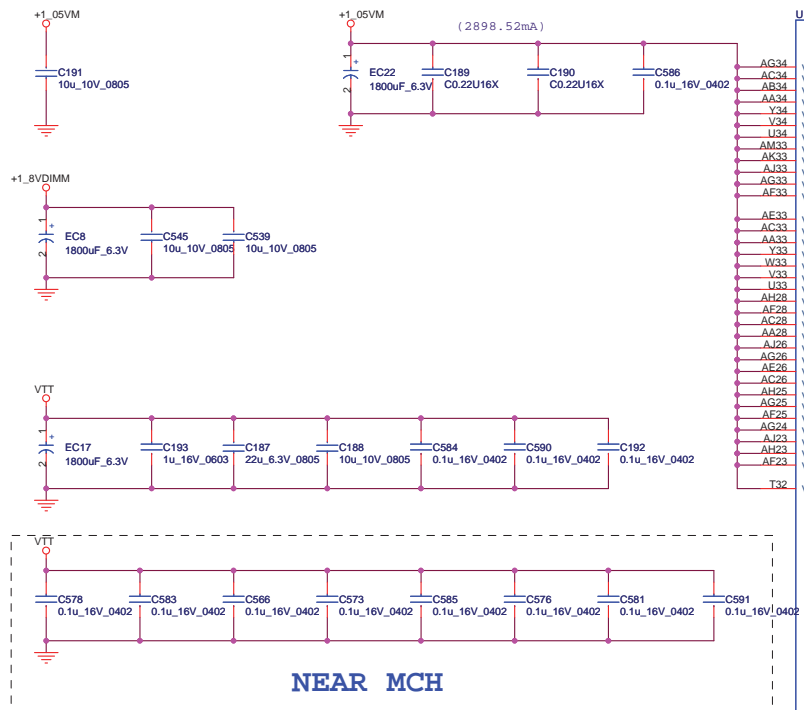
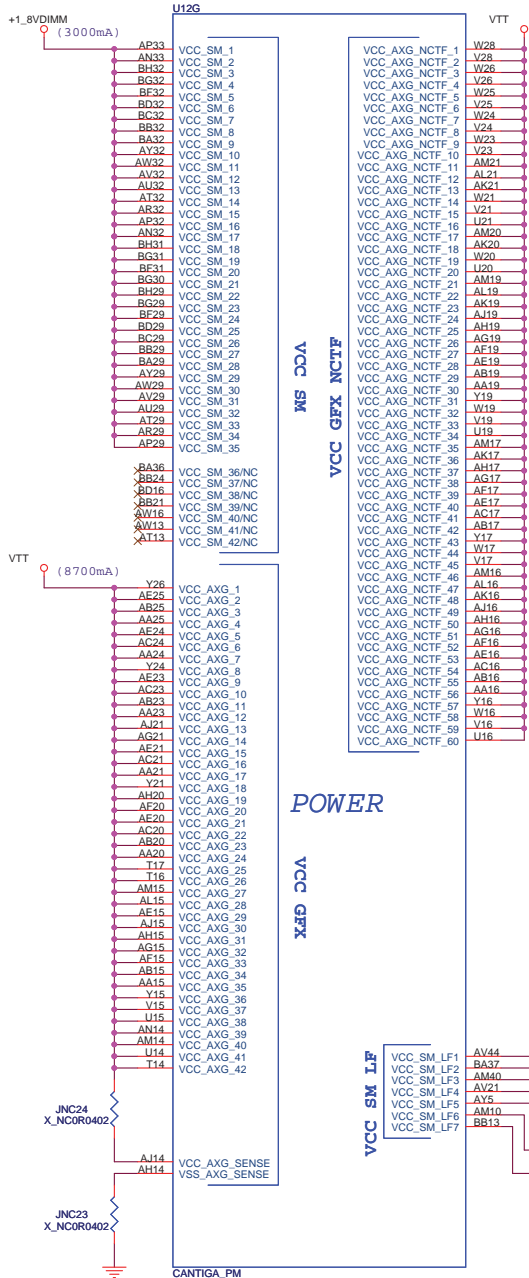
CANTIGA\_PM

**MSI CORPORATION**

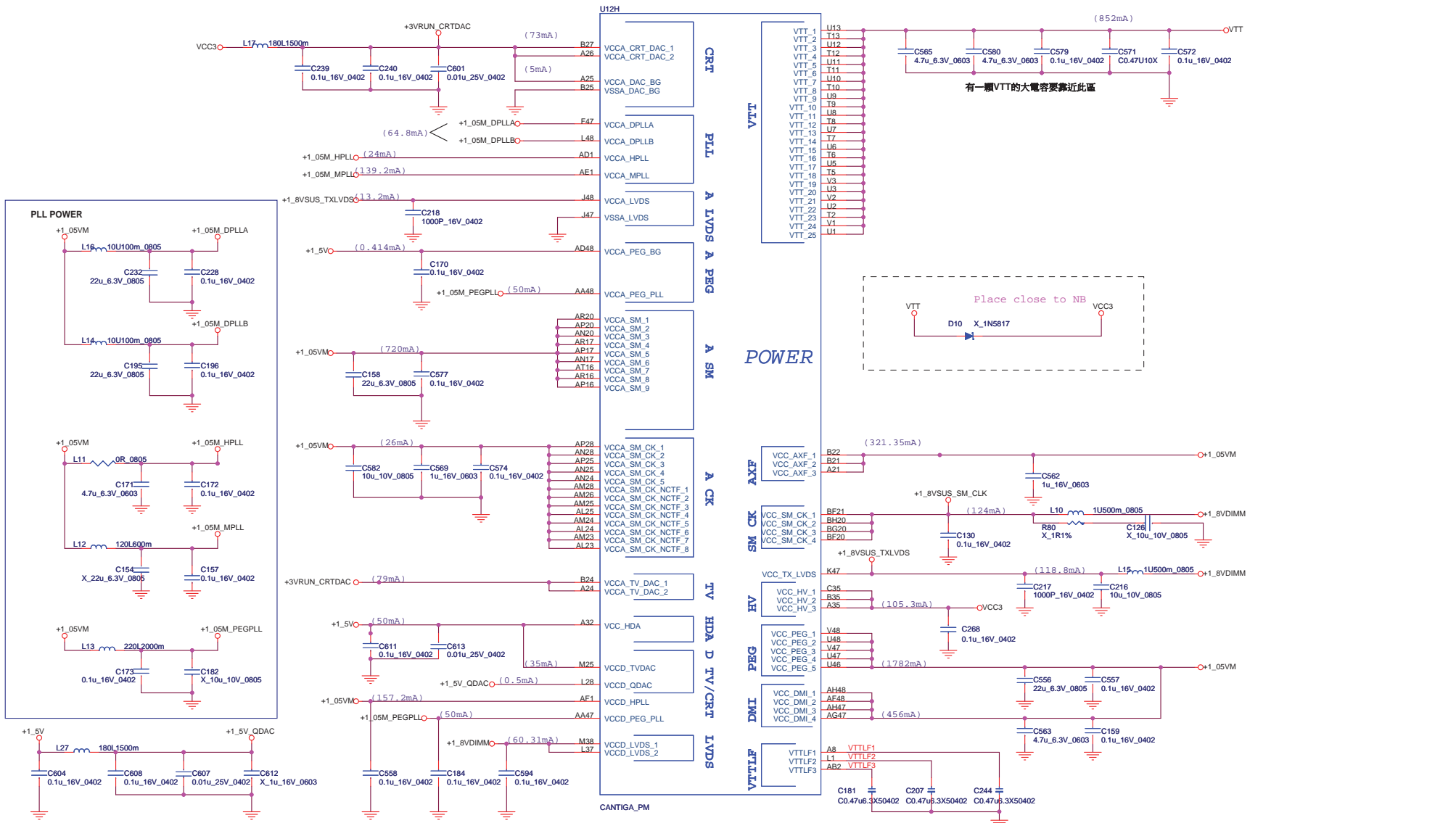
Title: **CANTIGA-3 (DDR)**

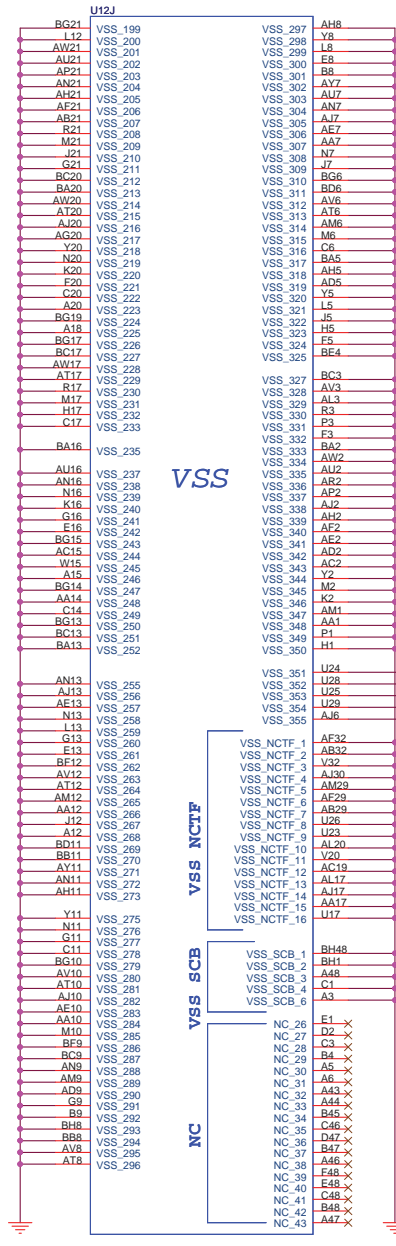
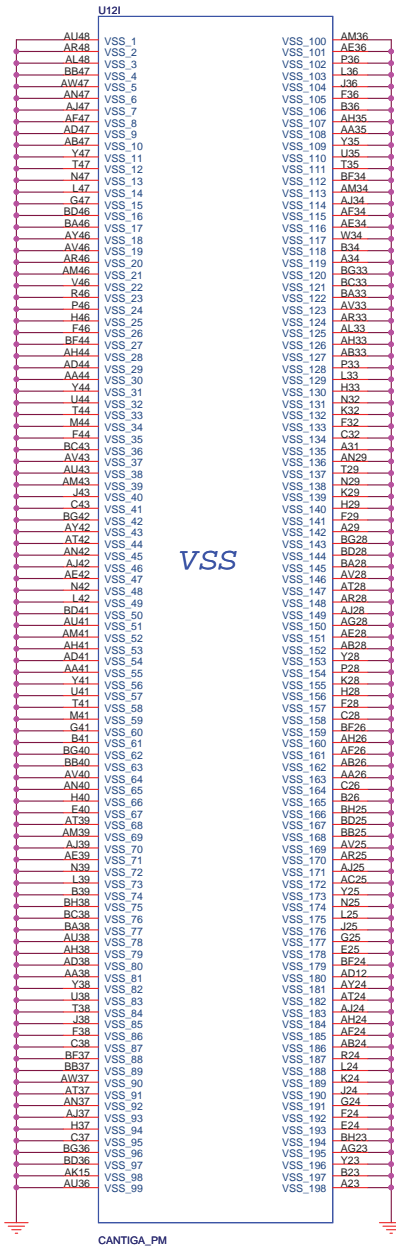
Size: Custom Document Number: **MS-96A9** Rev: 0A

Date: Tuesday, February 19, 2008 Sheet 10 of 41



<b>MSI CORPORATION</b>			
<b>CANTIGA-4 (POWER-1)</b>			
Title	Document Number		Rev
Size	MS-96A9		0A
Customer			
Date:	Tuesday, February 19, 2008	Sheet	11 of 41



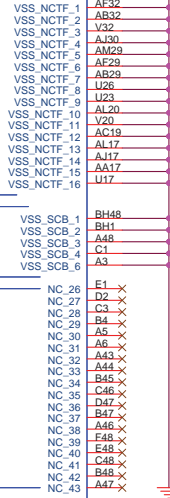


VSS

VSS\_NCTF

VSS\_SCB

NC

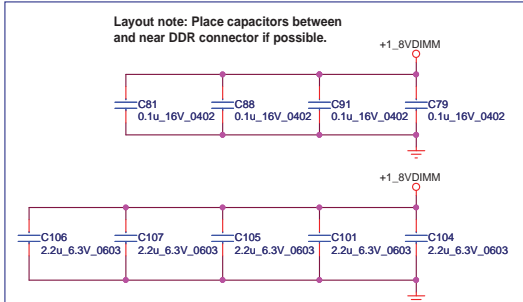
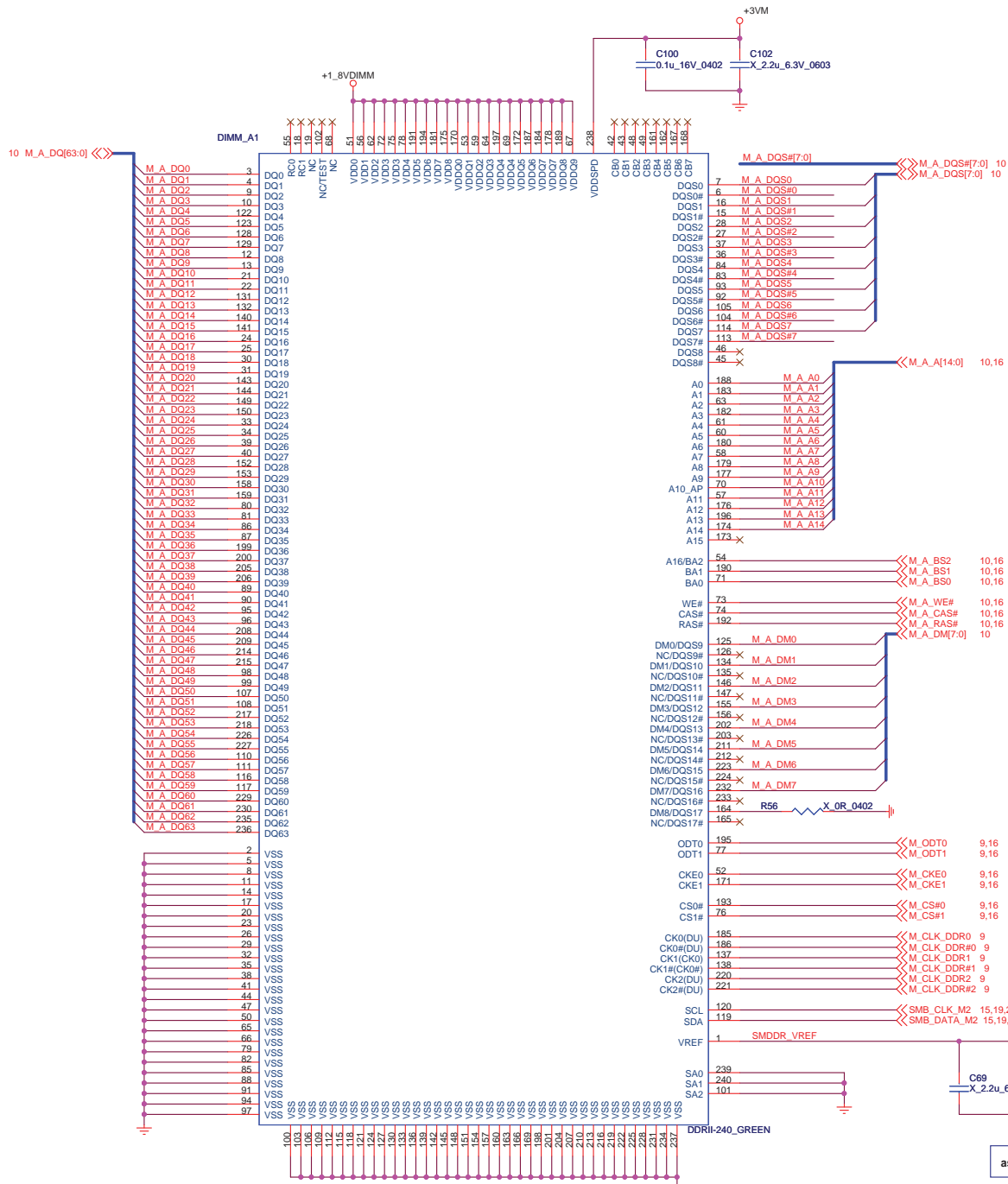


**MSI CORPORATION**

Title: **CANTIGA-6 (VSS)**

Size: Document Number  
 Custom: **MS-96A9** Rev: 0A

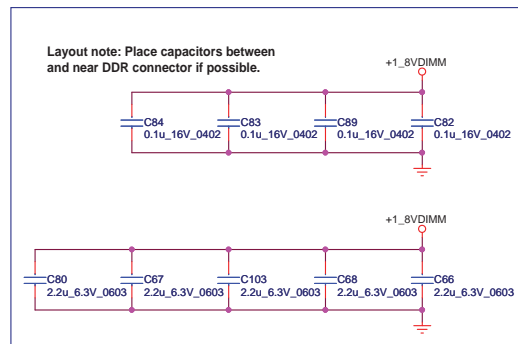
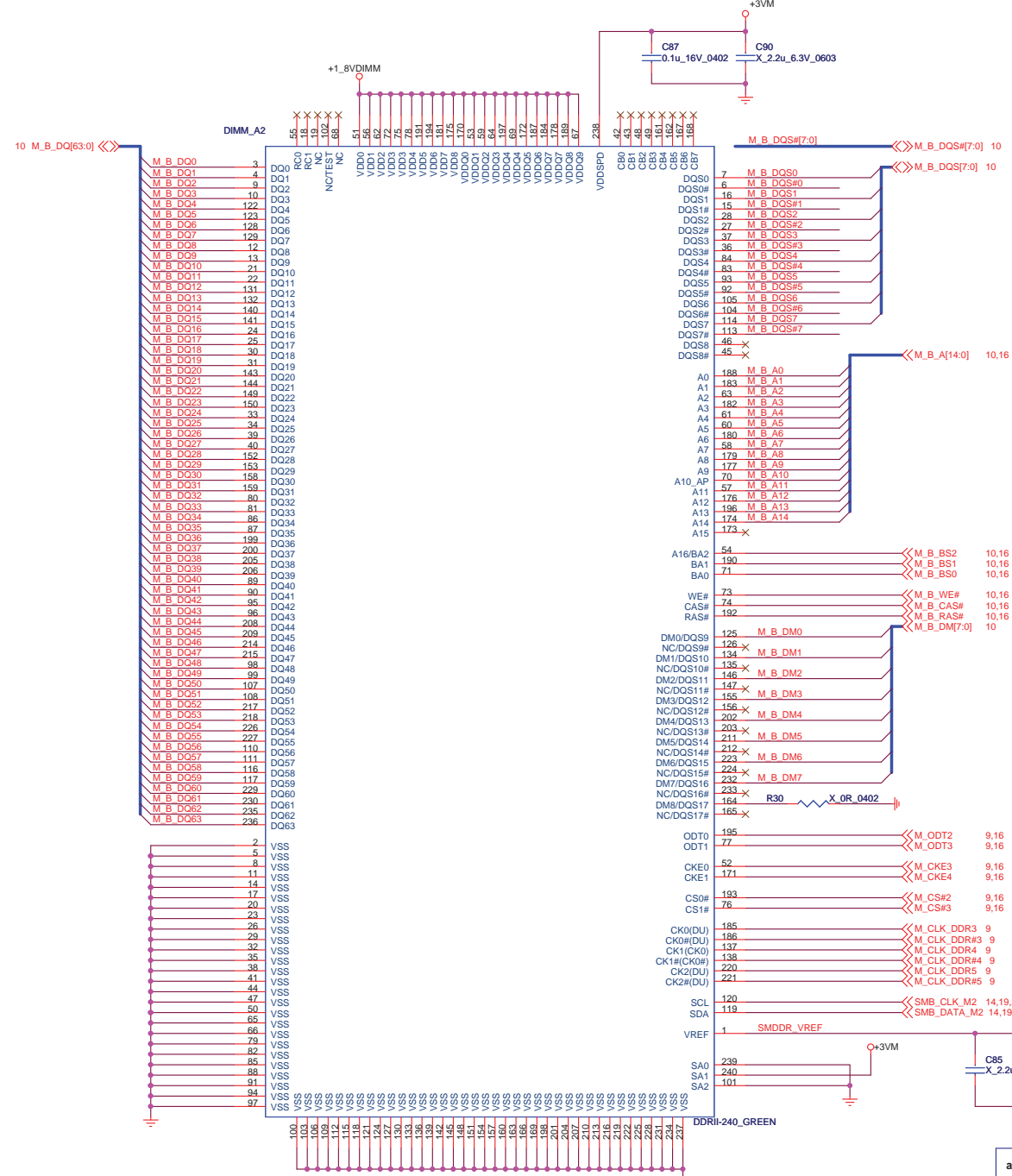
Date: Tuesday, February 19, 2008 Sheet: 13 of 41



as close as SO-DIMM Trace : 10 mils

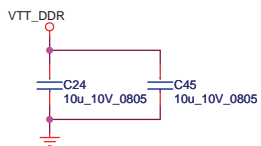
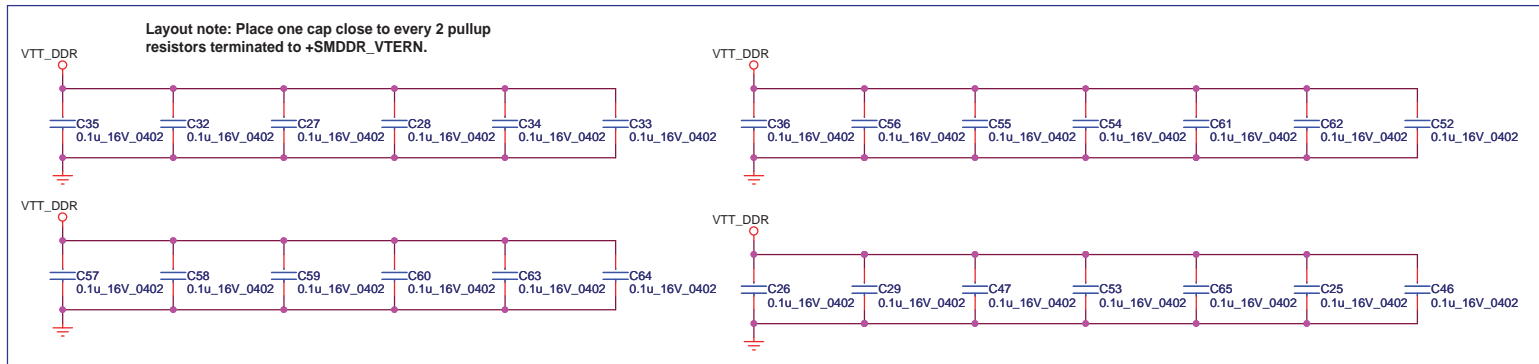
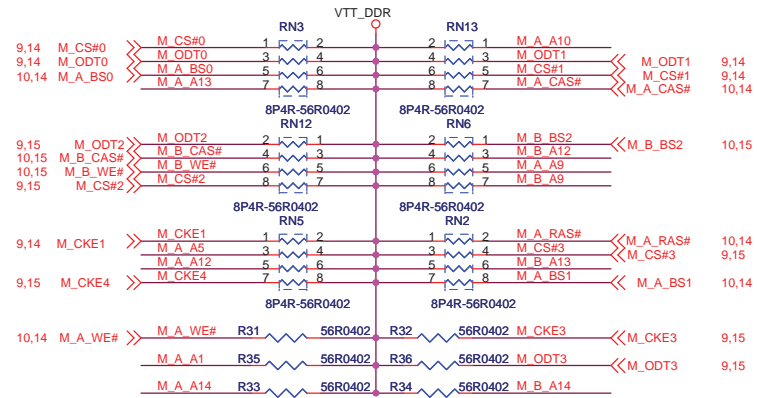
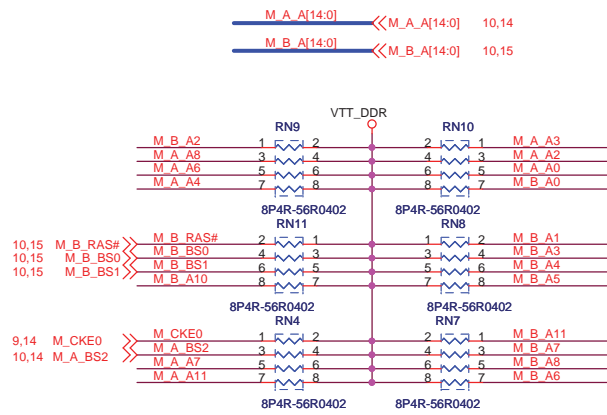
## DDR2 DIMM\_1\_CHA

<b>MSI CORPORATION</b>		
<b>DDR2 DDRDIMM_A0</b>		
Title	Document Number	Rev
MS-96A9		0A
Date:	Tuesday, February 19, 2008	Sheet 14 of 41



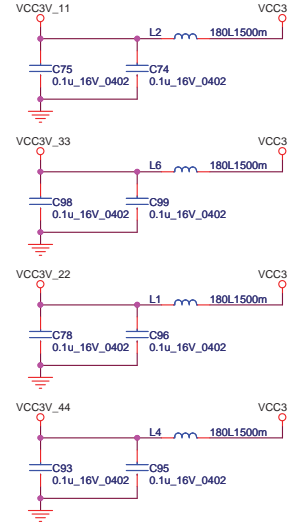
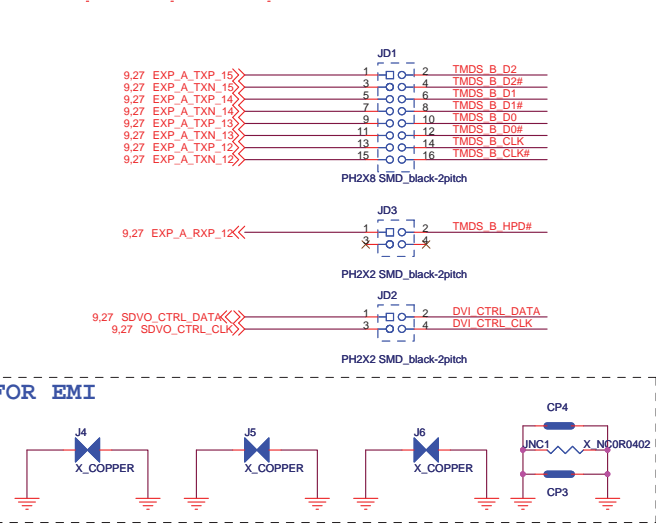
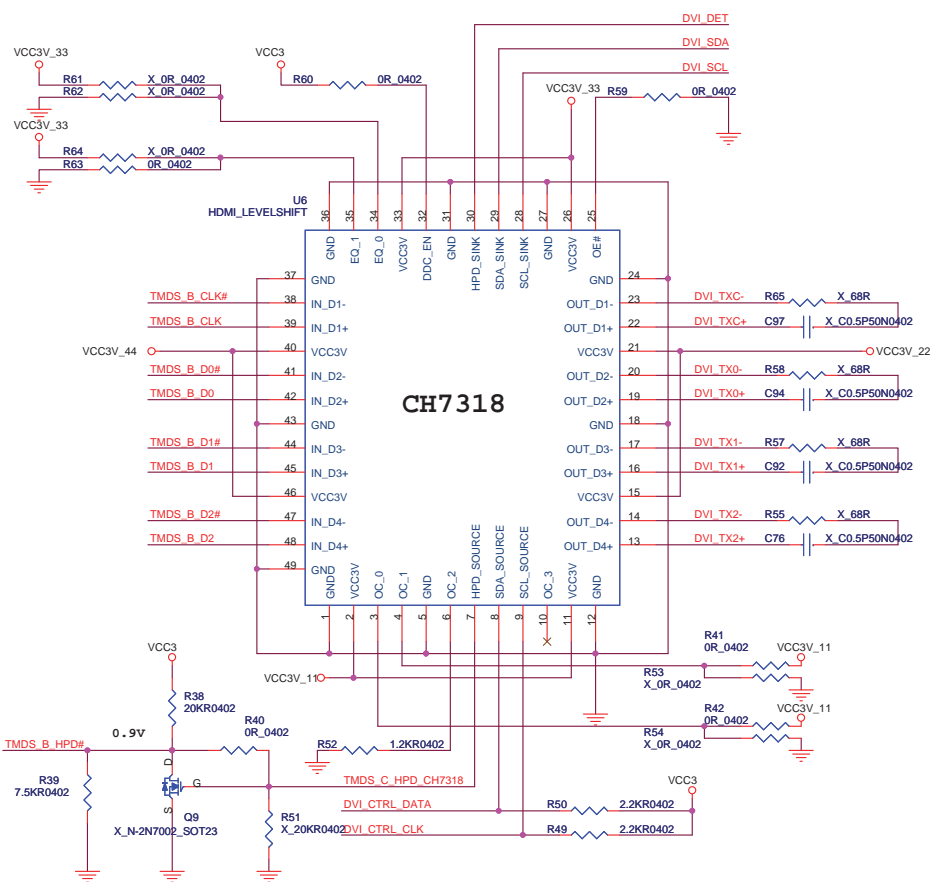
# DDR2 DIMM\_2\_CHB

MSI CORPORATION		
Title	DDR2 DDRDIMM_B0	
Size	Document Number	Rev
Custom	MS-96A9	0A
Date:	Tuesday, February 19, 2008	Sheet 15 of 41

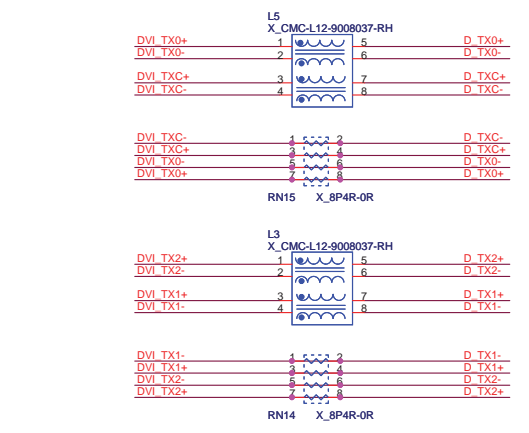
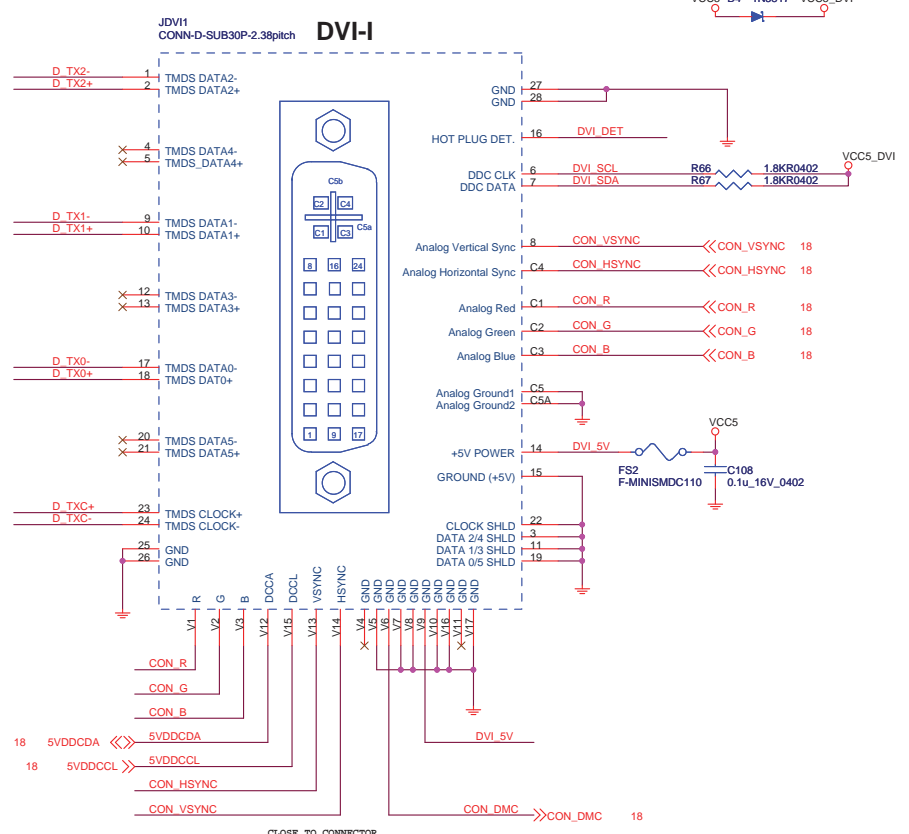


<b>MSI CORPORATION</b>		
Title		
<b>DDR2 TREMINATION</b>		
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	0A
Date:	Tuesday, February 19, 2008	Sheet 16 of 41



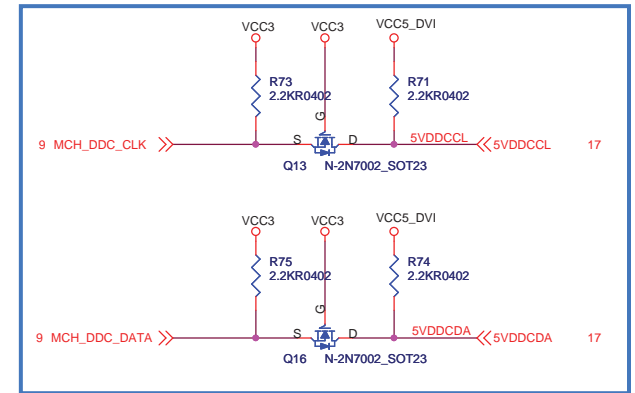
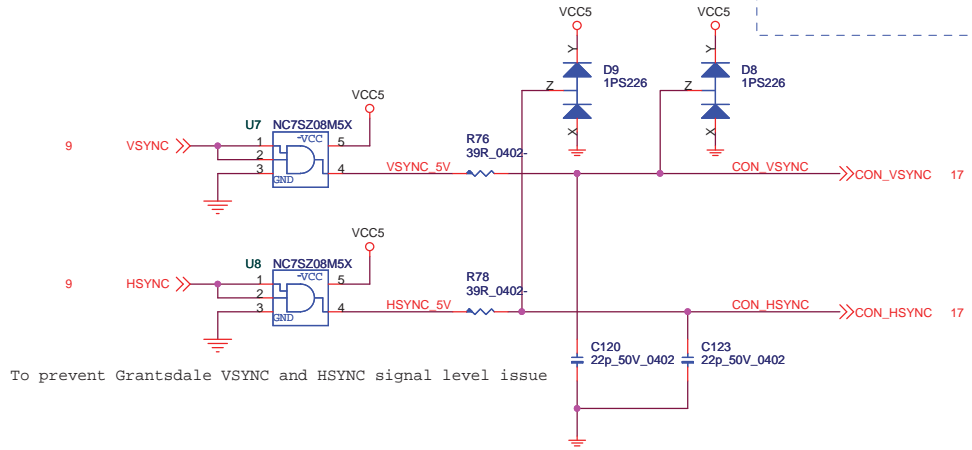
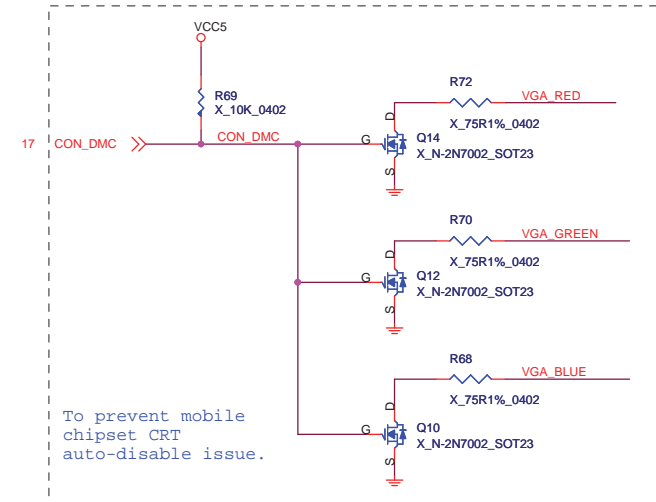
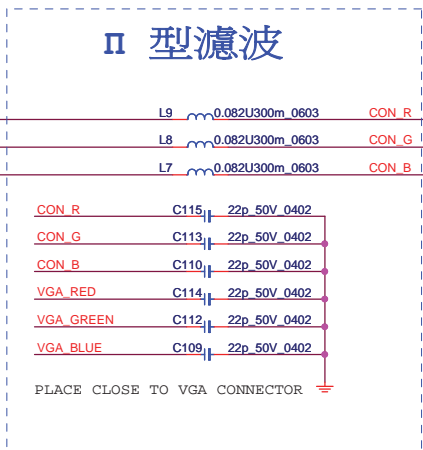
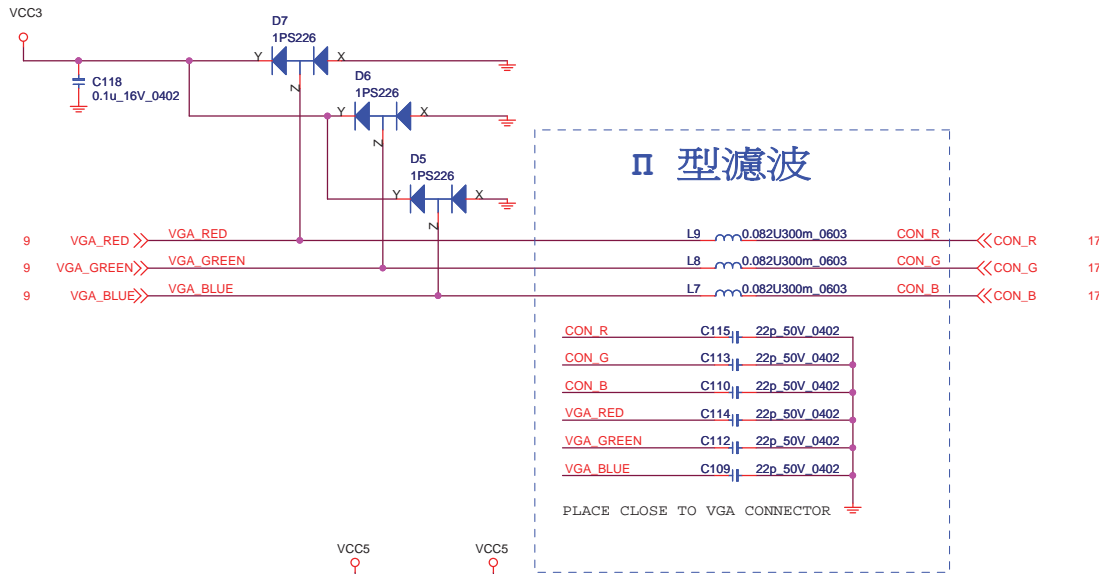


Combined Analog and Digital DVI-I Connector

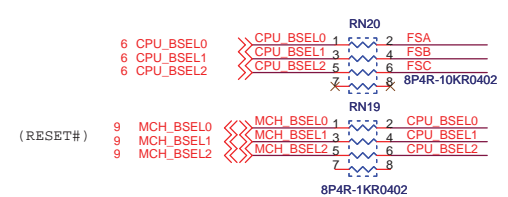
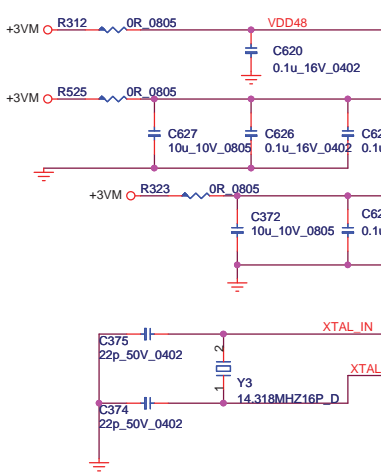
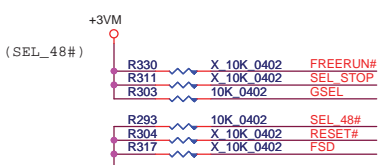
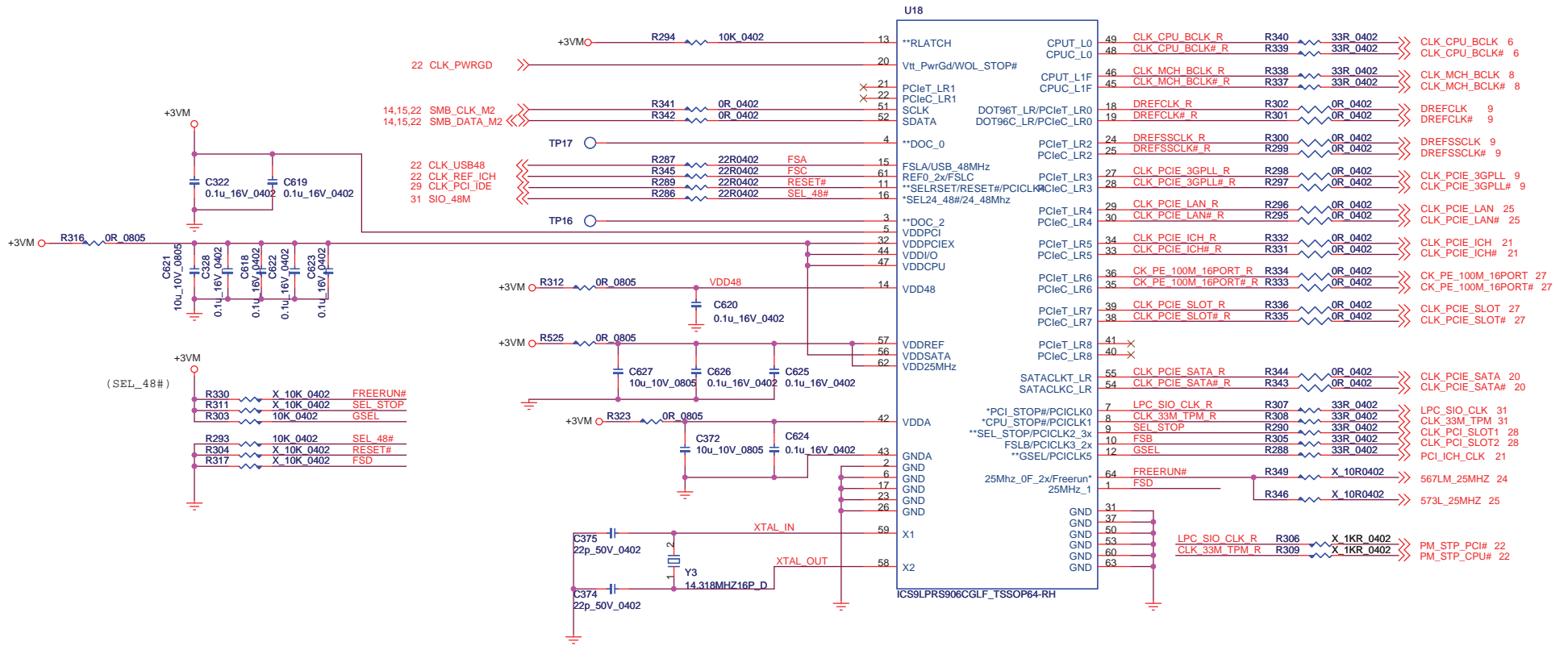


<b>MSI CORPORATION</b>			
Title	<b>CH7318 VGA, DVI</b>		
Size	Document Number	Rev	
Custom	<b>MS-96A9</b>	0A	
Date:	Thursday, February 21, 2008	Sheet	17 of 41

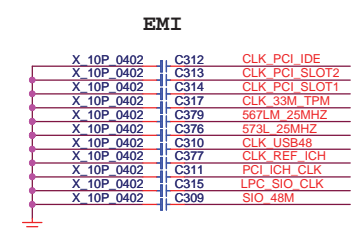
# Video Connector



<b>MSI CORPORATION</b>		
Title		
<b>D-Sub 15Pin Video Connector</b>		
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	0A
Date:	Tuesday, February 19, 2008	Sheet 18 of 41



CPU Table			FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]	
L	H	H	667 MHz
L	H	L	800 MHz

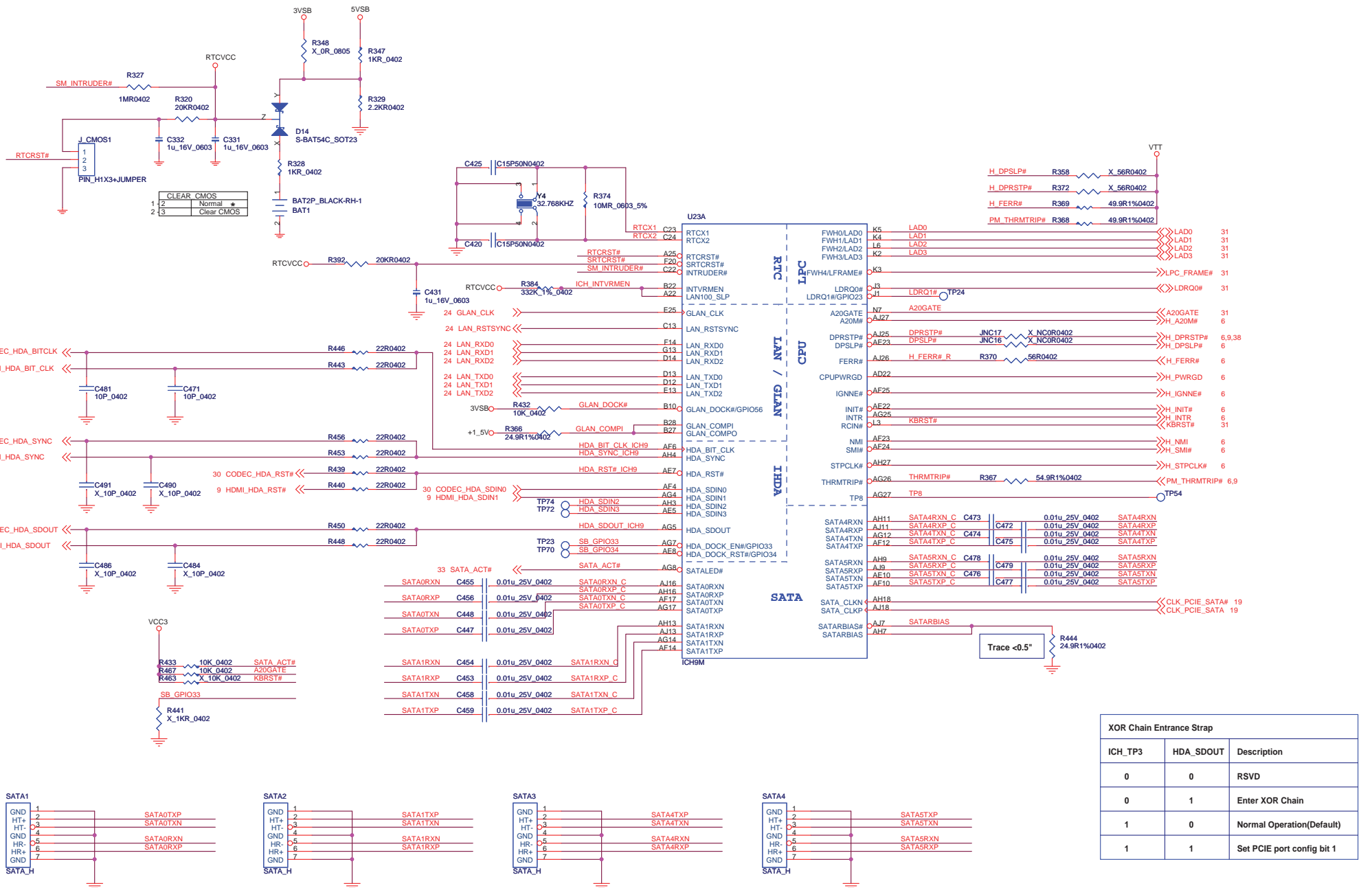


**MSI CORPORATION**

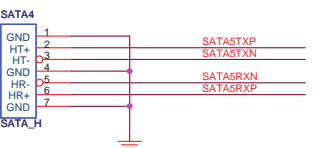
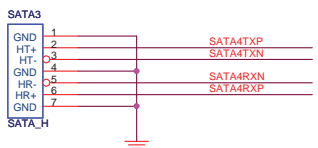
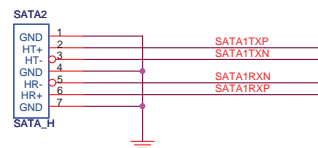
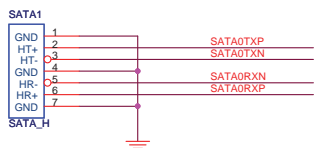
**CLOCK Generator (ICS9LPR906)**

Size: Custom    Document Number: **MS-96A9**    Rev: 0A

Date: Tuesday, February 19, 2008    Sheet: 19 of 41



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(Default)
1	1	Set PCIe port config bit 1

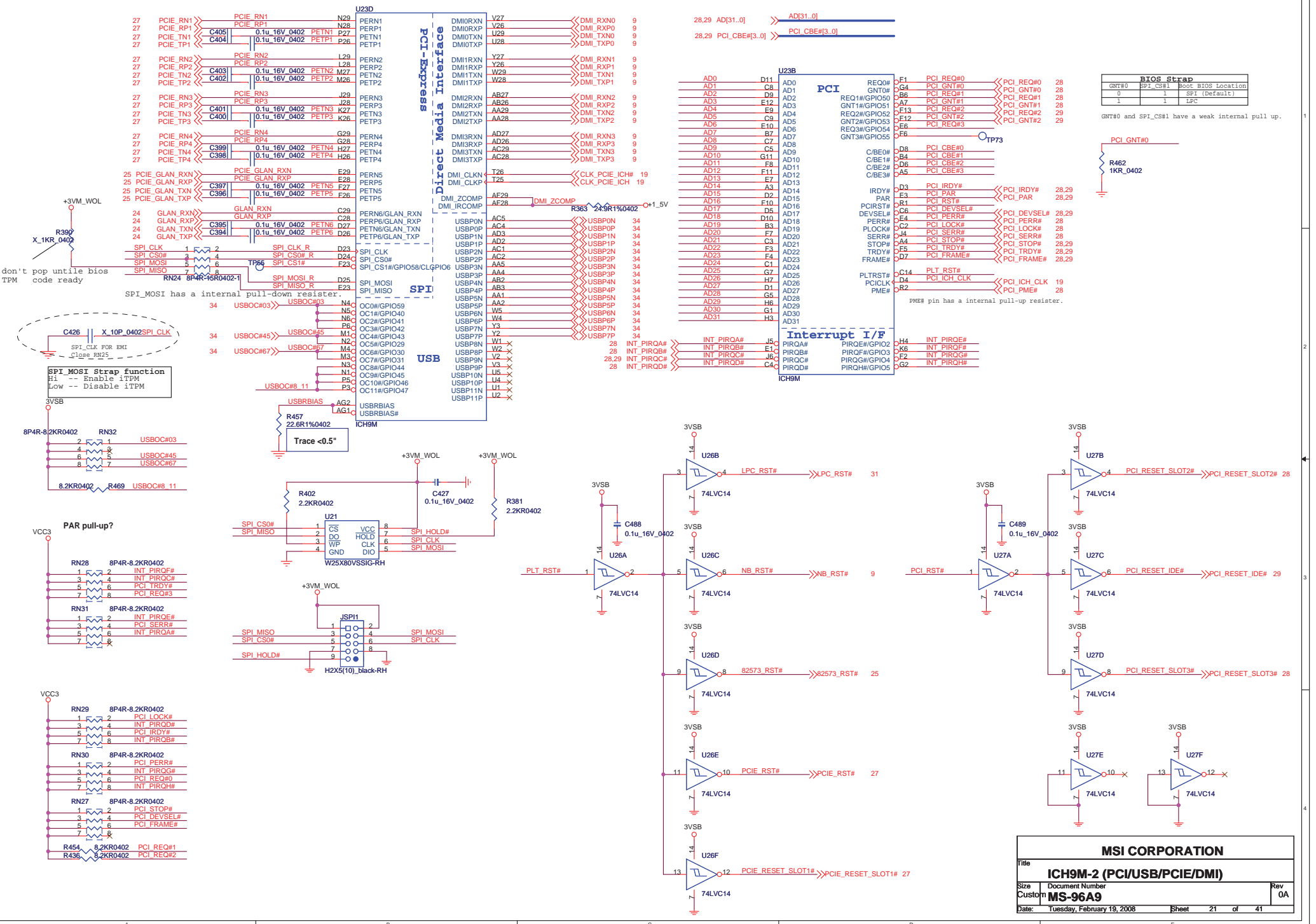


**MSI CORPORATION**

Title: **ICH9M-1 (CPU/IDE/Azalia)**

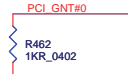
Size: **MS-96A9**      Document Number: **MS-96A9**      Rev: **0A**

Date: **Tuesday, February 19, 2008**      Sheet: **20** of **41**



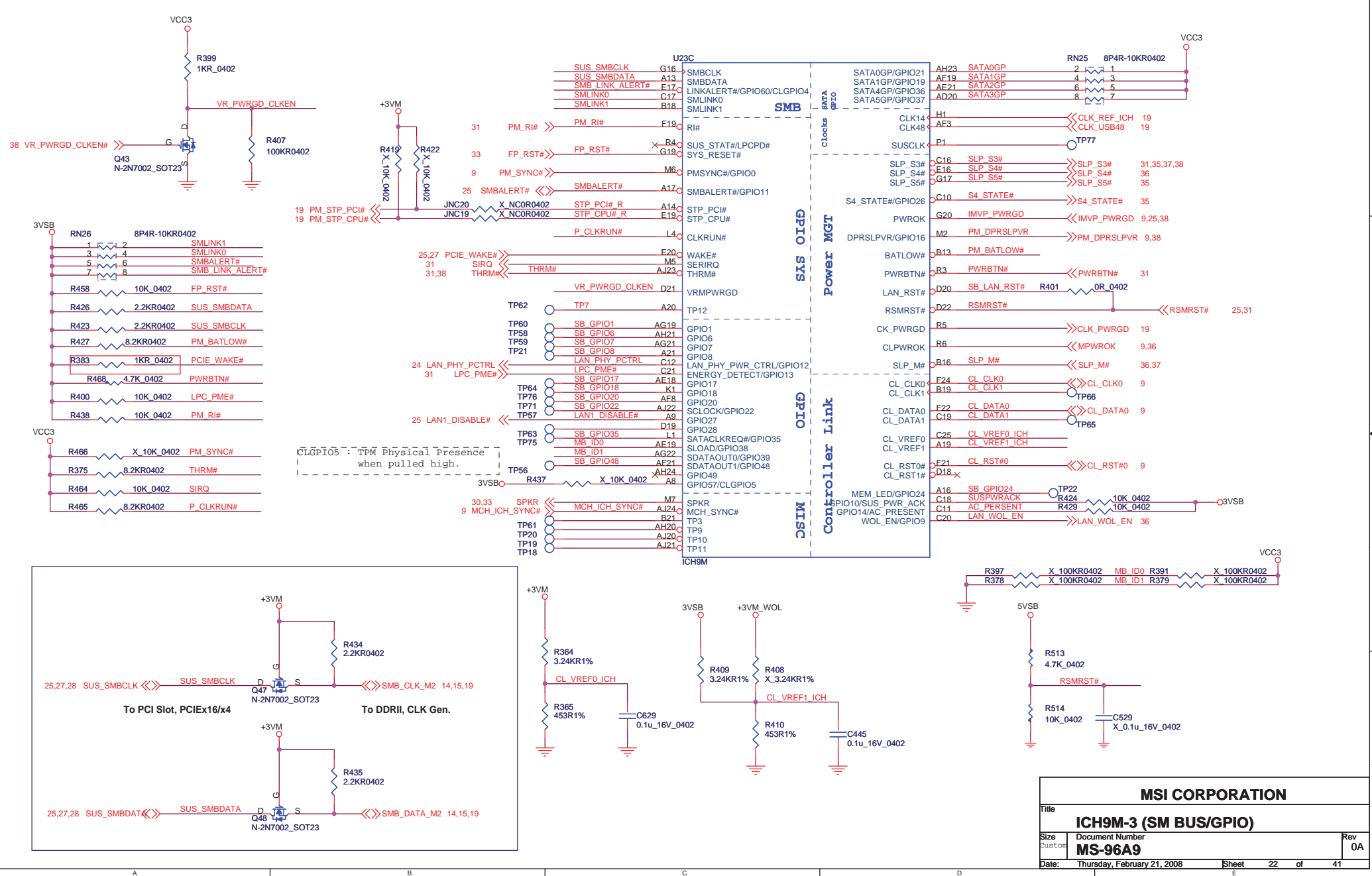
BIOS Strap		
GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI (Default)
1	1	LPC

GNT#0 and SPI\_CS#1 have a weak internal pull up.

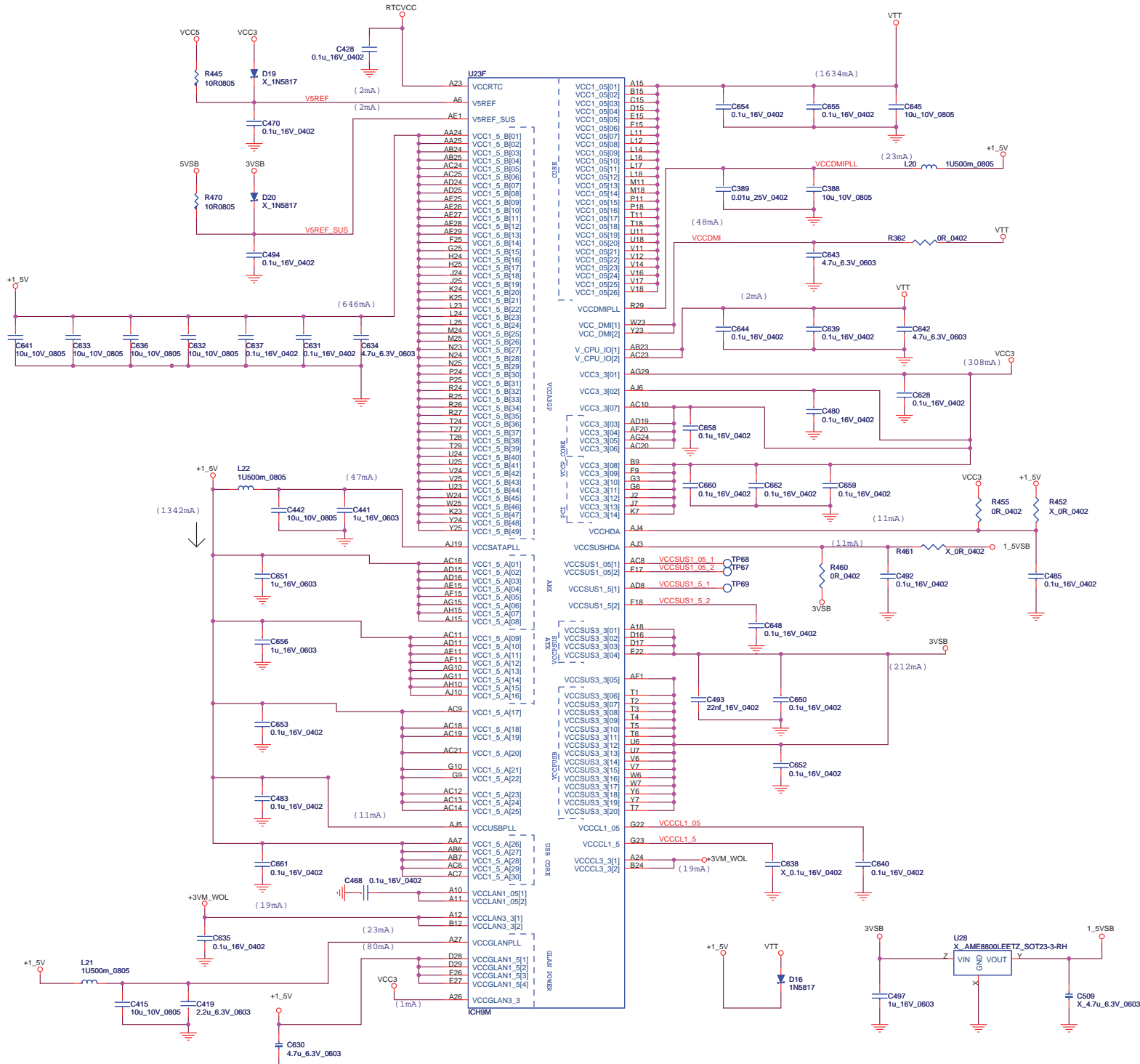


PME# pin has a internal pull-up resistor.

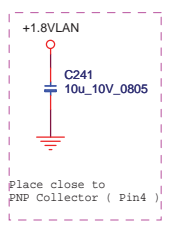
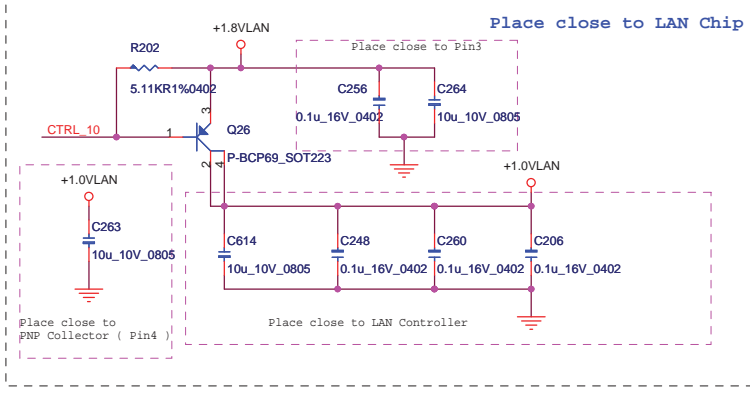
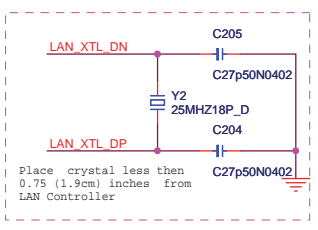
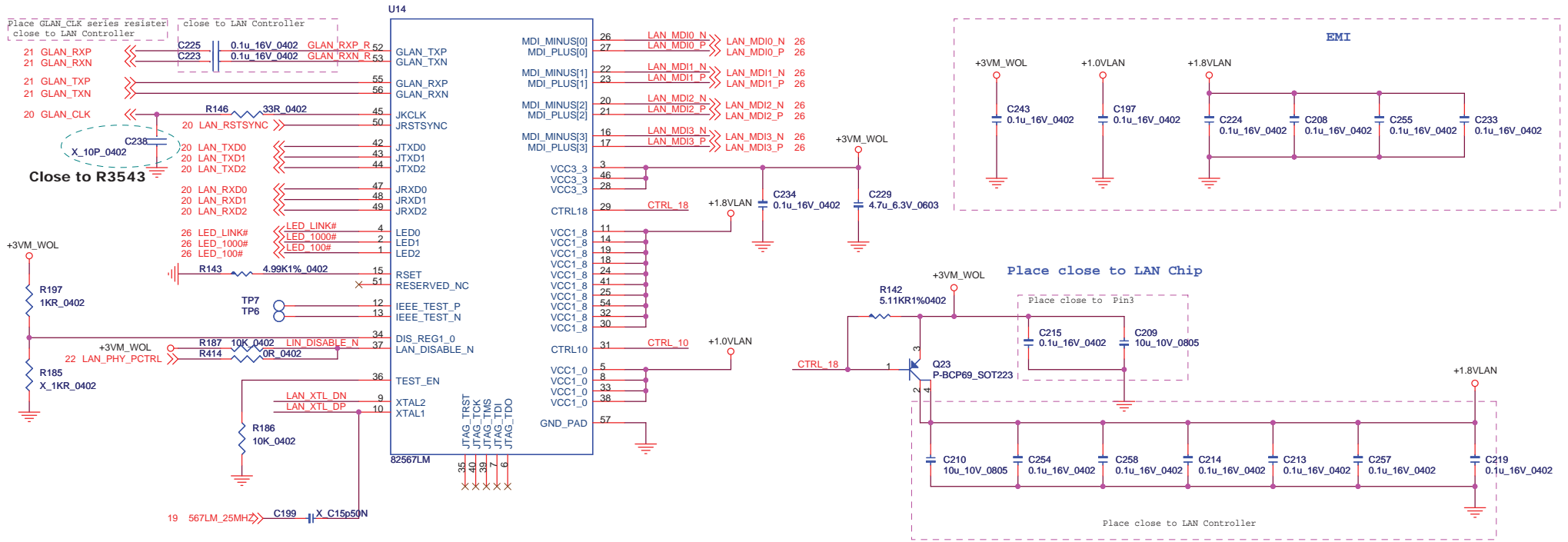
<b>MSI CORPORATION</b>		
<b>ICH9M-2 (PCI/USB/PCIE/DMI)</b>		
Title	Document Number	Rev
Size	MS-96A9	0A
Customer		
Date: Tuesday, February 19, 2008	Sheet 21	of 41



<b>MSI CORPORATION</b>		
Title		
<b>ICH9M-3 (SM BUS/GPIO)</b>		
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	0A
Date:	Thursday, February 21, 2008	Sheet 22 of 41

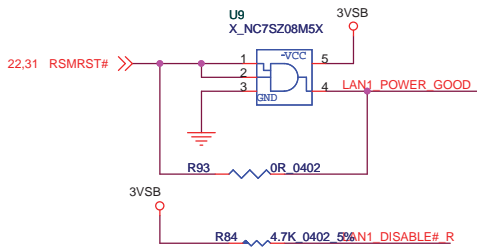


U23F			
AA26	VSS[001]	VSS[107]	H5
AA27	VSS[002]	VSS[108]	J23
AA3	VSS[003]	VSS[109]	J26
AA6	VSS[004]	VSS[110]	G7
AB1	VSS[005]	VSS[111]	AC22
AA23	VSS[006]	VSS[112]	K28
AB28	VSS[007]	VSS[113]	K23
AB29	VSS[008]	VSS[114]	L13
AB4	VSS[009]	VSS[115]	L15
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L7
AC27	VSS[013]	VSS[119]	L5
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M28
AD18	VSS[021]	VSS[127]	M23
AD21	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	N11
AD29	VSS[024]	VSS[130]	N12
AD4	VSS[025]	VSS[131]	N13
AD6	VSS[026]	VSS[132]	N14
AD7	VSS[027]	VSS[133]	N15
AD9	VSS[028]	VSS[134]	N16
AD11	VSS[029]	VSS[135]	N17
AE12	VSS[030]	VSS[136]	N18
AE13	VSS[031]	VSS[137]	N26
AE14	VSS[032]	VSS[138]	N27
AE16	VSS[033]	VSS[139]	P12
AE17	VSS[034]	VSS[140]	P13
AE20	VSS[035]	VSS[141]	P14
AE24	VSS[036]	VSS[142]	P15
AE3	VSS[037]	VSS[143]	P16
AE4	VSS[038]	VSS[144]	P17
AE6	VSS[039]	VSS[145]	P2
AE9	VSS[040]	VSS[146]	P23
AE10	VSS[041]	VSS[147]	P28
AE11	VSS[042]	VSS[148]	P29
AE18	VSS[043]	VSS[149]	P7
AE19	VSS[044]	VSS[150]	P7
AE22	VSS[045]	VSS[151]	R11
AE26	VSS[046]	VSS[152]	R12
AE27	VSS[047]	VSS[153]	R13
AE28	VSS[048]	VSS[154]	R14
AE3	VSS[049]	VSS[155]	R15
AE7	VSS[050]	VSS[156]	R16
AE9	VSS[051]	VSS[157]	R17
AG13	VSS[052]	VSS[158]	R18
AG16	VSS[053]	VSS[159]	R28
AG18	VSS[054]	VSS[160]	R28
AG20	VSS[055]	VSS[161]	T13
AG23	VSS[056]	VSS[162]	T14
AG3	VSS[057]	VSS[163]	T15
AG6	VSS[058]	VSS[164]	T16
AG9	VSS[059]	VSS[165]	T17
AH12	VSS[060]	VSS[166]	T23
AH14	VSS[061]	VSS[167]	B26
AH17	VSS[062]	VSS[168]	U12
AH19	VSS[063]	VSS[169]	U13
AH2	VSS[064]	VSS[170]	U14
AH22	VSS[065]	VSS[171]	U15
AH26	VSS[066]	VSS[172]	U16
AH28	VSS[067]	VSS[173]	U17
AH5	VSS[068]	VSS[174]	AD23
AH8	VSS[069]	VSS[175]	U26
AH12	VSS[070]	VSS[176]	U27
AH14	VSS[071]	VSS[177]	U27
AH17	VSS[072]	VSS[178]	V1
AH18	VSS[073]	VSS[179]	V13
B11	VSS[074]	VSS[180]	V15
B17	VSS[075]	VSS[181]	V23
B2	VSS[076]	VSS[182]	V28
B20	VSS[077]	VSS[183]	V4
B23	VSS[078]	VSS[184]	V29
B5	VSS[079]	VSS[185]	V5
B6	VSS[080]	VSS[186]	W26
BB	VSS[081]	VSS[187]	W27
C26	VSS[082]	VSS[188]	Y1
C27	VSS[083]	VSS[189]	Y1
C28	VSS[084]	VSS[190]	Y29
E14	VSS[085]	VSS[191]	Y28
E18	VSS[086]	VSS[192]	Y4
E2	VSS[087]	VSS[193]	Y5
E21	VSS[088]	VSS[194]	Y6
E24	VSS[089]	VSS[195]	AG28
E5	VSS[090]	VSS[196]	AH6
E8	VSS[091]	VSS[197]	AF2
F16	VSS[092]	VSS[198]	B25
F28	VSS[093]	VSS[199]	
F29	VSS[094]	VSS NCTF[01]	A1
G12	VSS[095]	VSS NCTF[02]	A2
G15	VSS[096]	VSS NCTF[03]	A28
G18	VSS[097]	VSS NCTF[04]	A29
G21	VSS[098]	VSS NCTF[05]	AH1
G24	VSS[099]	VSS NCTF[06]	AH29
G26	VSS[100]	VSS NCTF[07]	AJ2
GB	VSS[101]	VSS NCTF[08]	AJ28
H2	VSS[102]	VSS NCTF[09]	AJ29
H3	VSS[103]	VSS NCTF[10]	B1
H23	VSS[104]	VSS NCTF[11]	B29
H28	VSS[105]	VSS NCTF[12]	
H29	VSS[106]	VSS NCTF[12]	

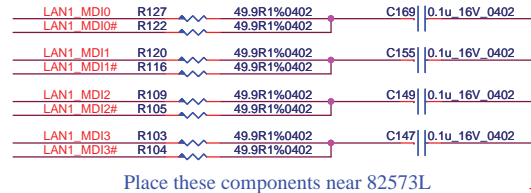
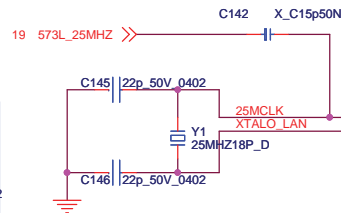
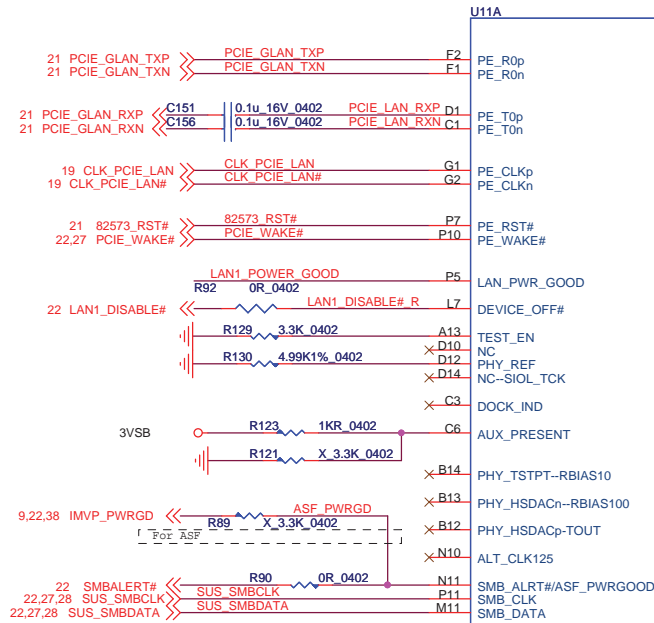
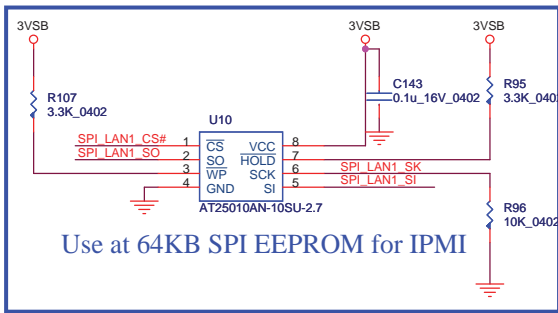


<b>MSI CORPORATION</b>		
Title <b>LAN(82567)</b>		
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	<b>0A</b>
Date: Tuesday, February 19, 2008	Sheet 24	of 41

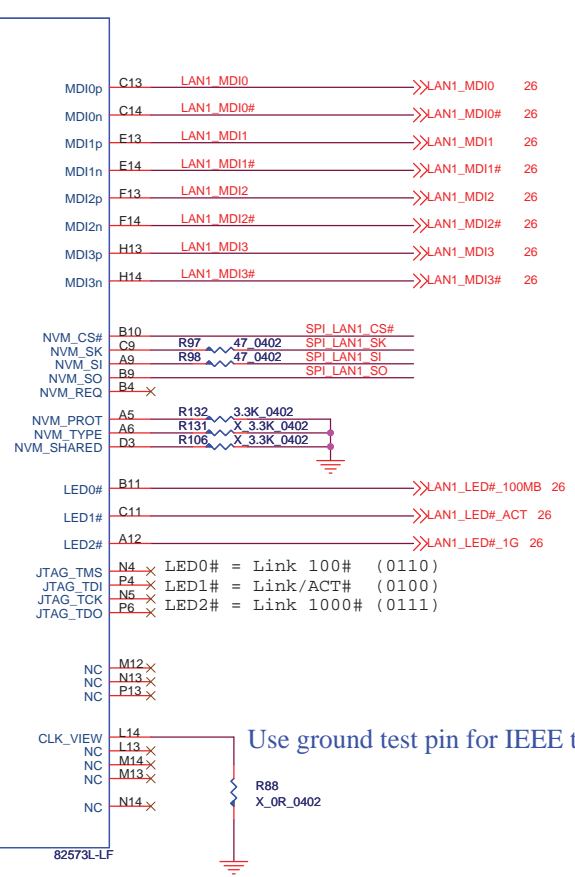




NVM_PROT	empty	stuff
NVM protection	Enable	Disable
NVM_TYPE	empty	stuff
NVM Device Type	EEPROM	Flash
NVM_SHARED	empty	stuff
NVM Shared with ICH9	Disable	Enable



Place these components near 82573L

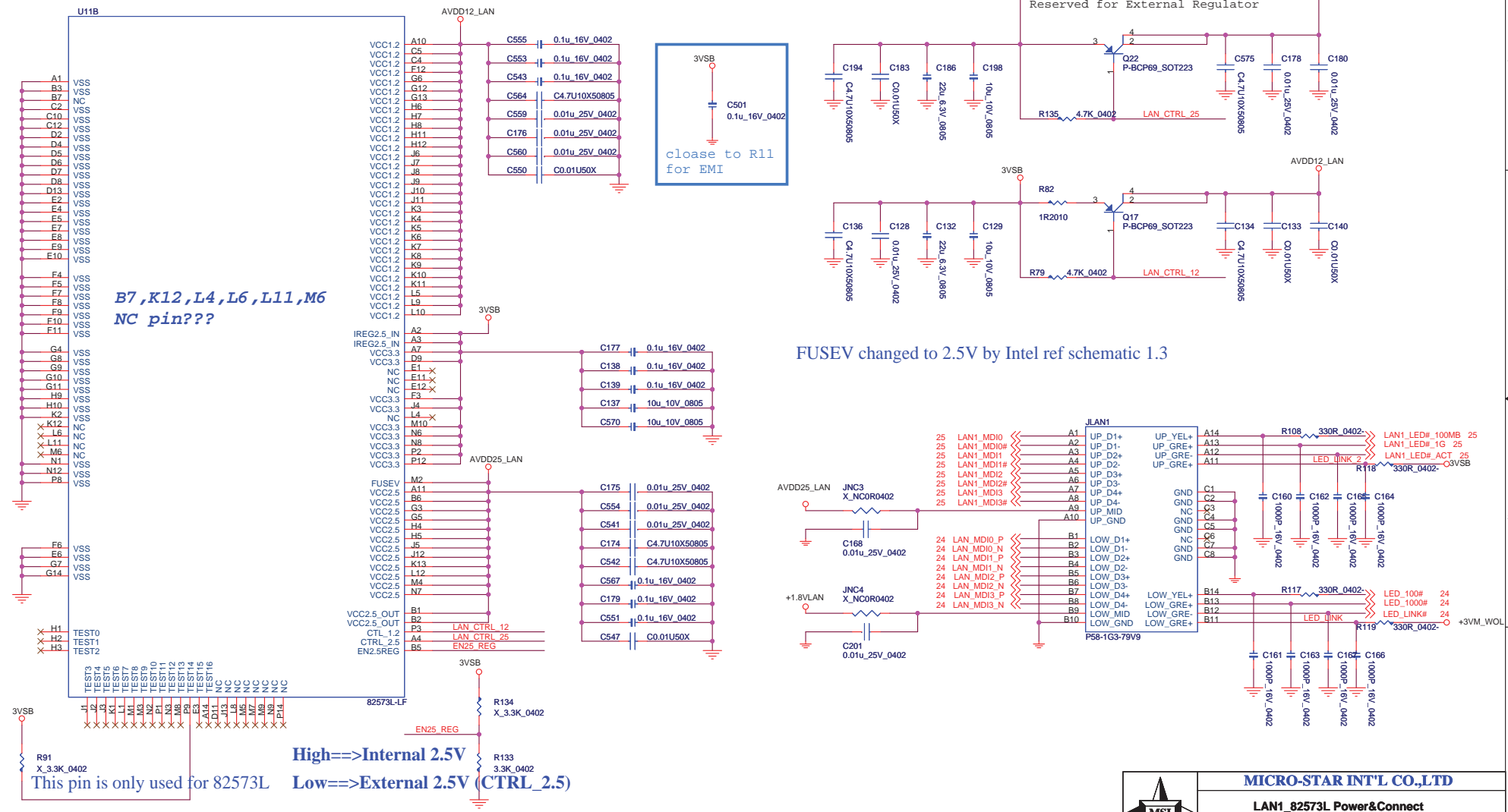


Use ground blue pin for IEEE test

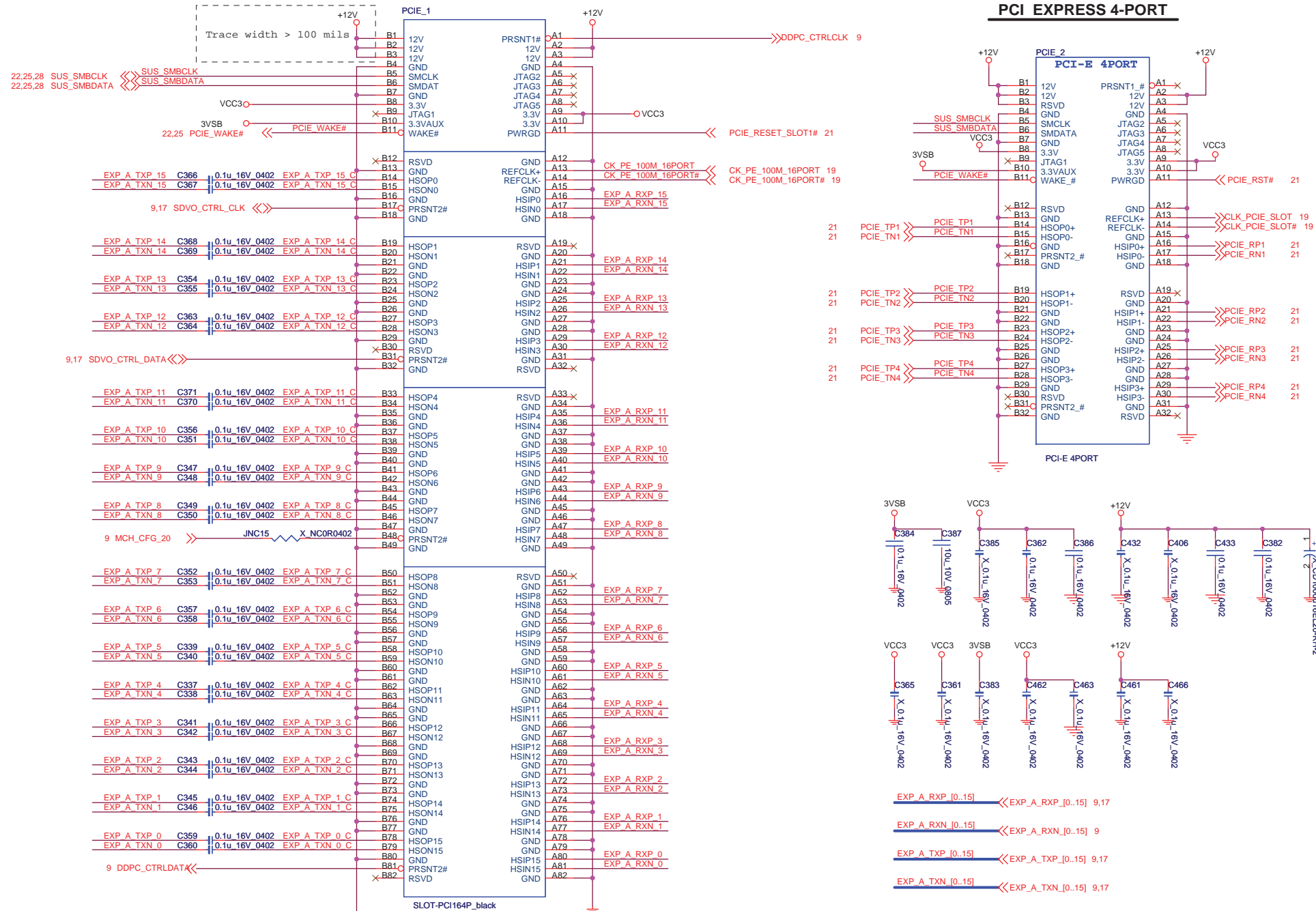
**MSI**  
Link to the Future  
**MICRO-START INT'L CO.,LTD.**


Title: **LAN1\_82573 Signal**

Size Custom	Document Number <b>MS96A9</b>	Rev <b>0A</b>
Date: Tuesday, February 19, 2008	Sheet 25 of 41	

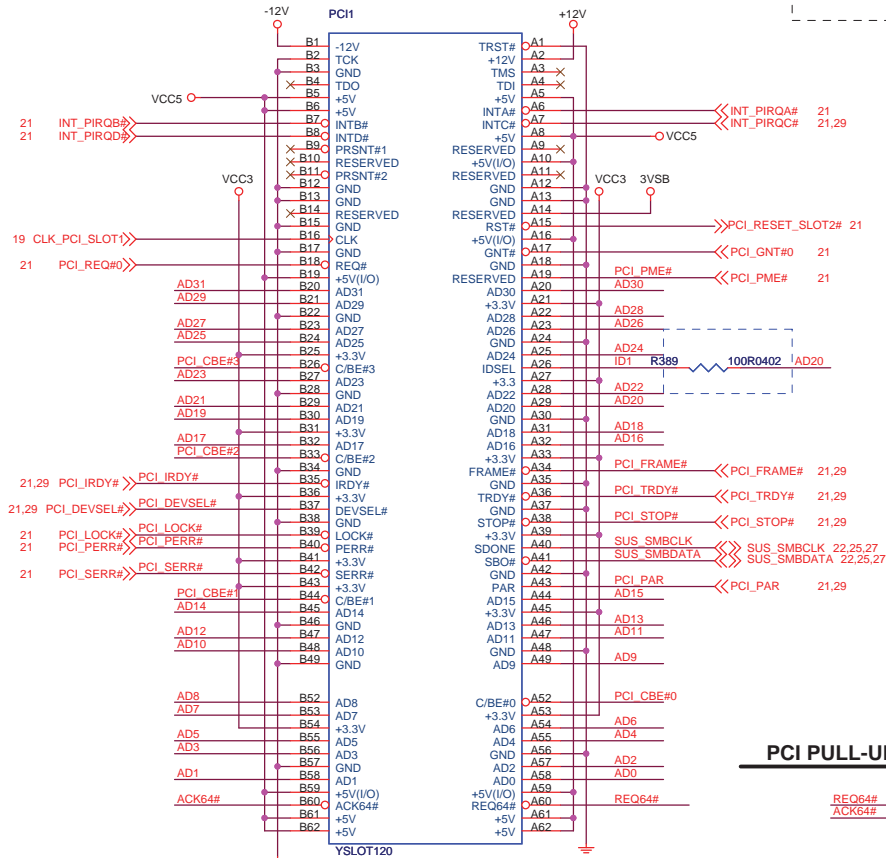


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>LAN1_82573L Power&amp;Connect</b>		
Size Custom	Document Description MS-96A9	Rev 0A
Date: Tuesday, February 19, 2008	Sheet 26	of 41



		<b>MICRO-STAR INT'L CO.,LTD</b>	
		<b>PCI -Express X 16/4 Port</b>	
Size Custom	Document Description <b>MS-96A9</b>		Rev 0A
Date: Tuesday, February 19, 2008		Sheet 27	of 41

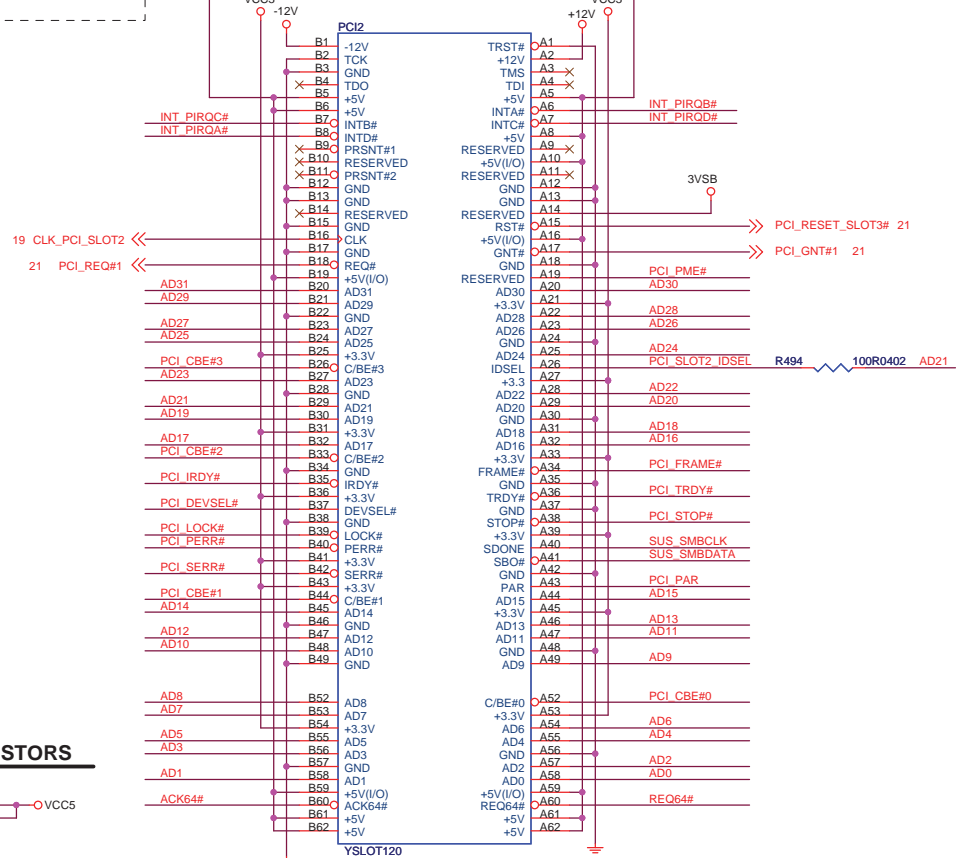
**PCI SLOT 1 (PCI VER: 2.2 COMPLY)**



**IDSEL = AD20**  
**MASTER = PCI\_REQ#0**  
**PCI\_GNT#0**

21,29 AD[31..0] >> AD[31..0]  
 21,29 PCI\_CBE#[3..0] >> PCI\_CBE#[3..0]

**PCI SLOT 2 (PCI VER: 2.2 COMPLY)**

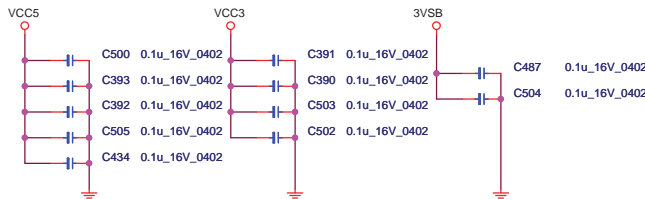


**IDSEL = AD21**  
**MASTER = PCI\_REQ#1**  
**PCI\_GNT#1**

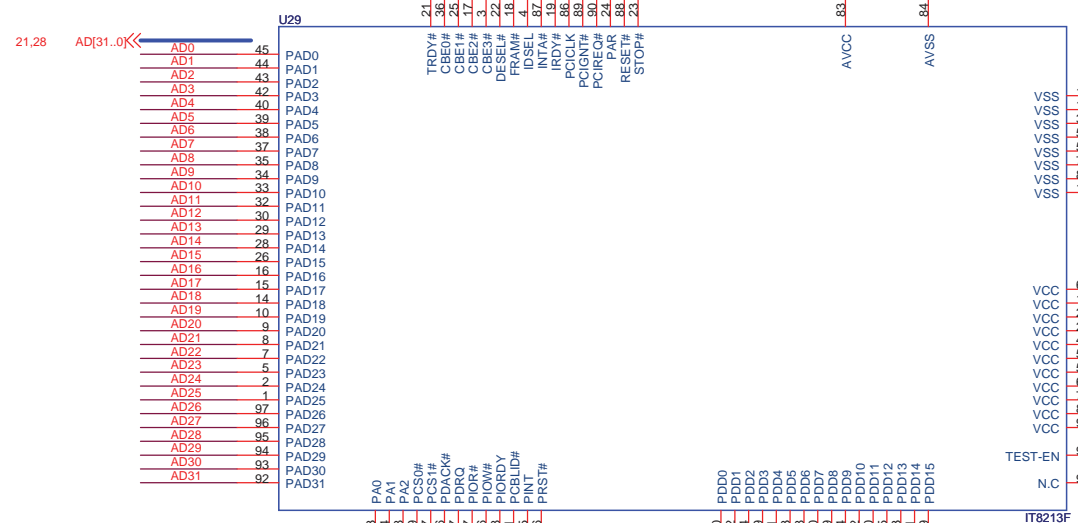
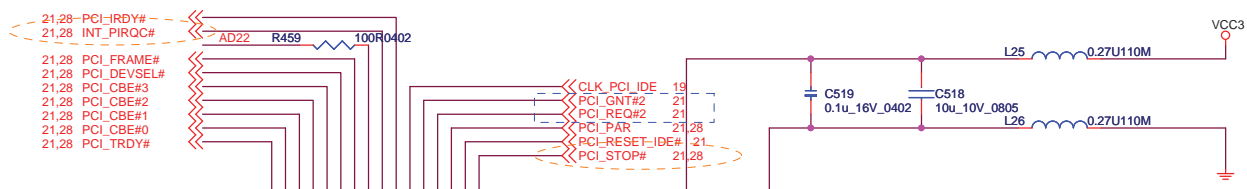
**PCI PULL-UP / DOWN RESISTORS**



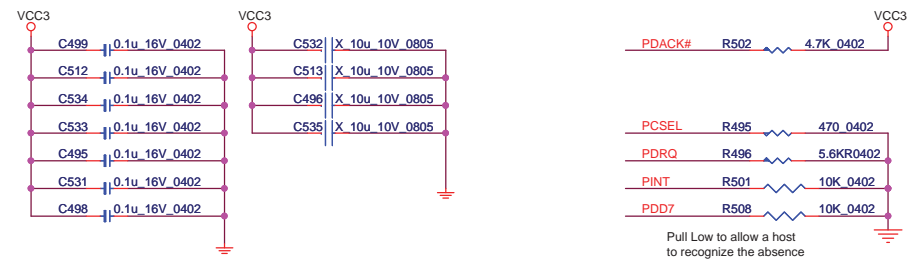
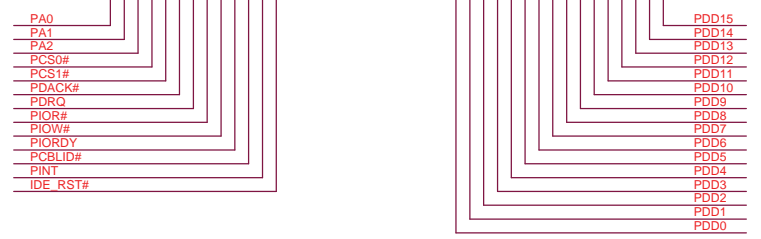
**PCI SLOT DECOUPLING CAPACITORS**



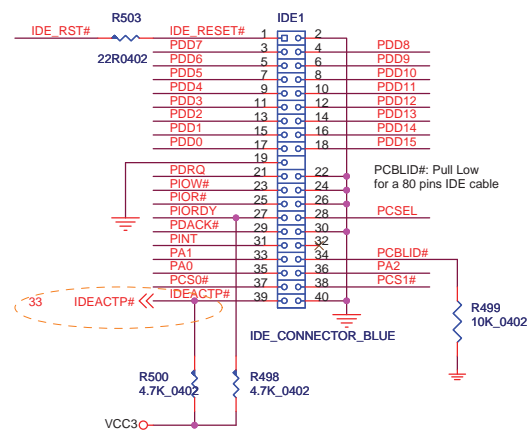
MSI CORPORATION			
Title	<b>PCI 0,1 SLOT</b>		
Size	Document Number		Rev
Custom	<b>MS-96A9</b>		<b>0A</b>
Date:	Tuesday, February 19, 2008	Sheet	28 of 41



IDSEL ==>PCI\_AD22  
 REQ ==>PCI\_REQ#2  
 GNT ==>PCI\_GNT#2  
 IRQ ==>INT\_PIRQC#

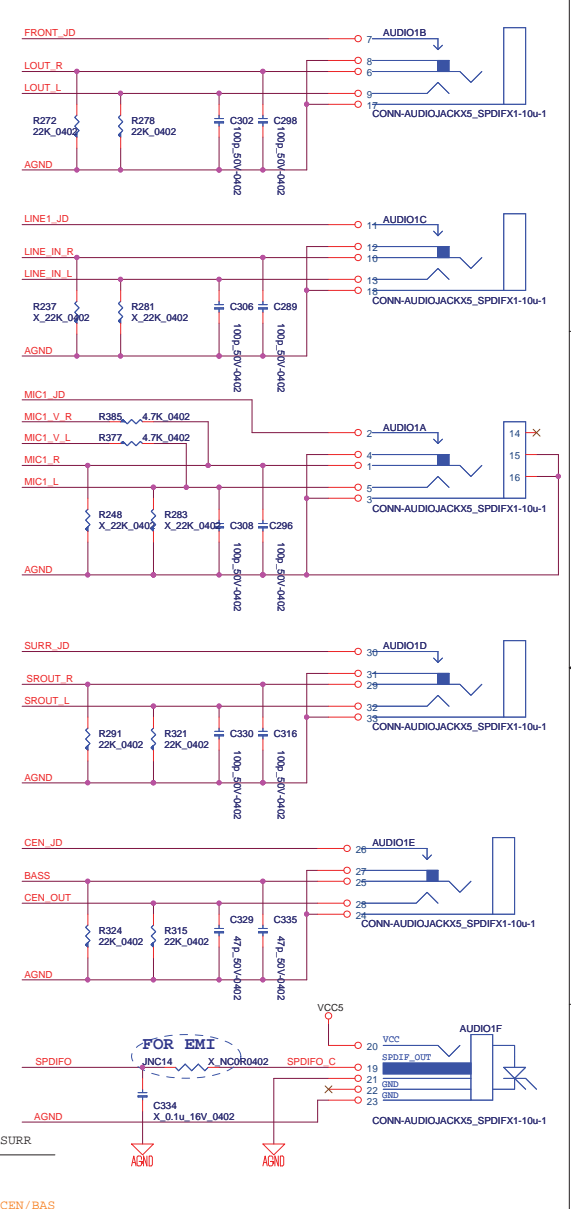
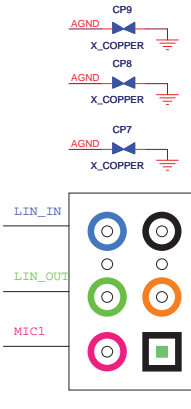
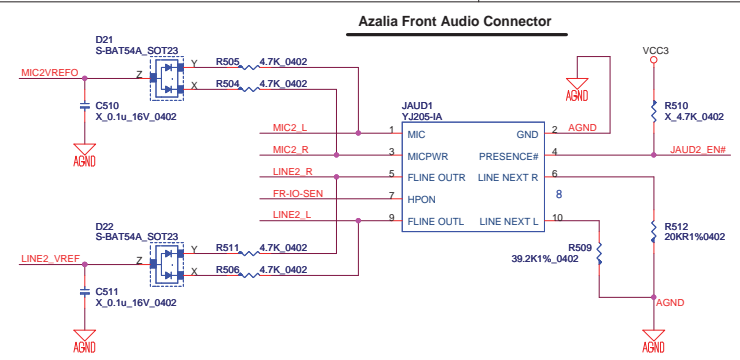
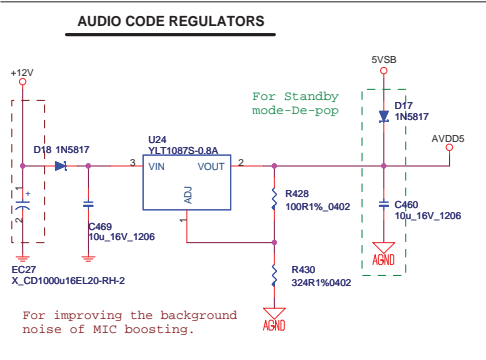
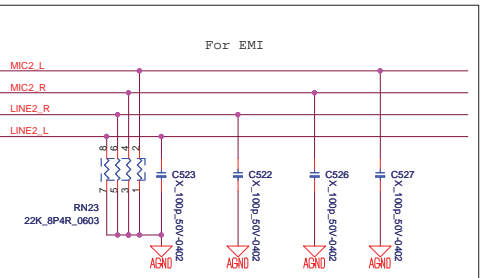
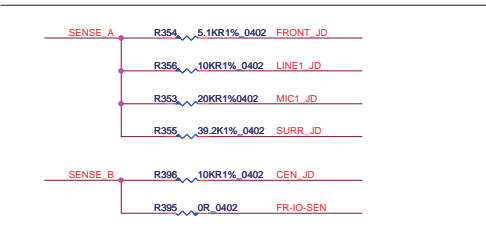
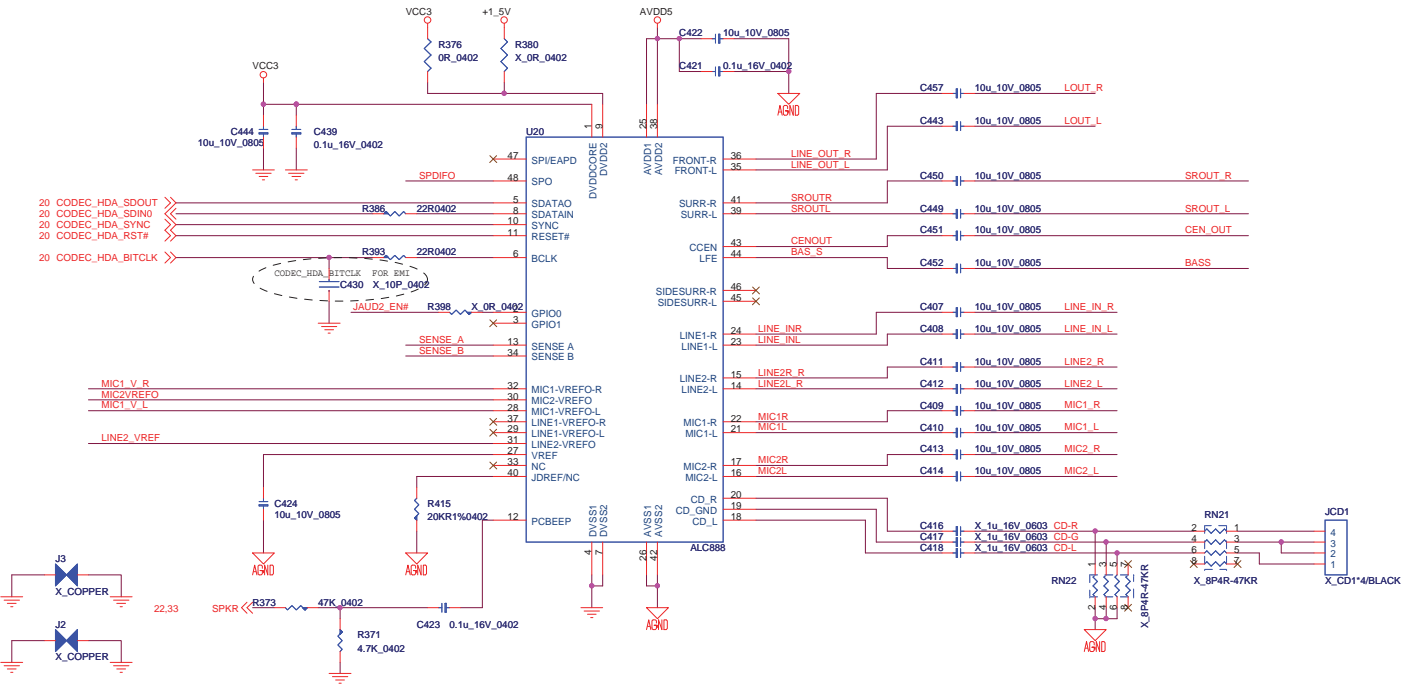


### IDE Connector



<b>MSI CORPORATION</b>		
Title		
<b>ITE/IT8213F IDE</b>		
Size	Document Number	Rev
4.1x8.1cm	<b>MS-96A9</b>	0A
Date:	Tuesday, February 19, 2008	Sheet 29 of 41

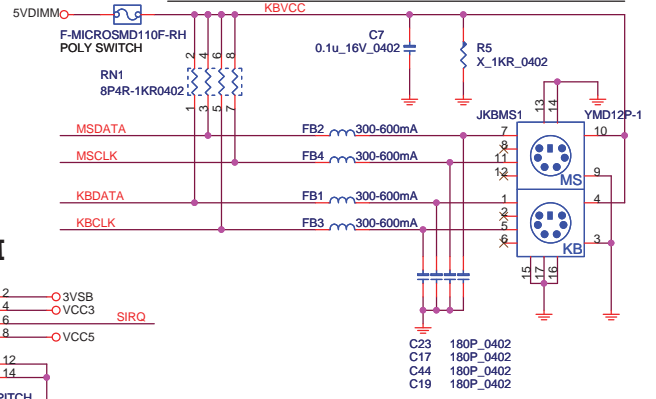
Pull Low to allow a host to recognize the absence of a device at Power-Up



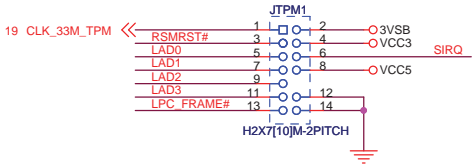
<b>MSI CORPORATION</b>		
Title	AZALIA CODEC(ALC888)	
Size	Document Number	Rev
Custom	MS-96A9	0A
Date:	Tuesday, February 19, 2008	Sheet 30 of 41

INDEX# must be pulled up to 5V only for A version chip

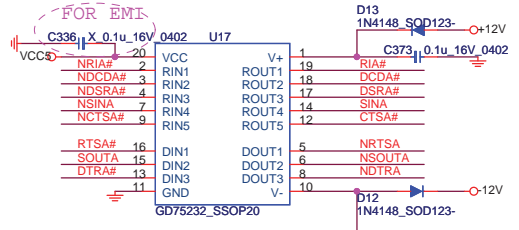
PS2 KEYBOARD & MOUSE CONNECTOR



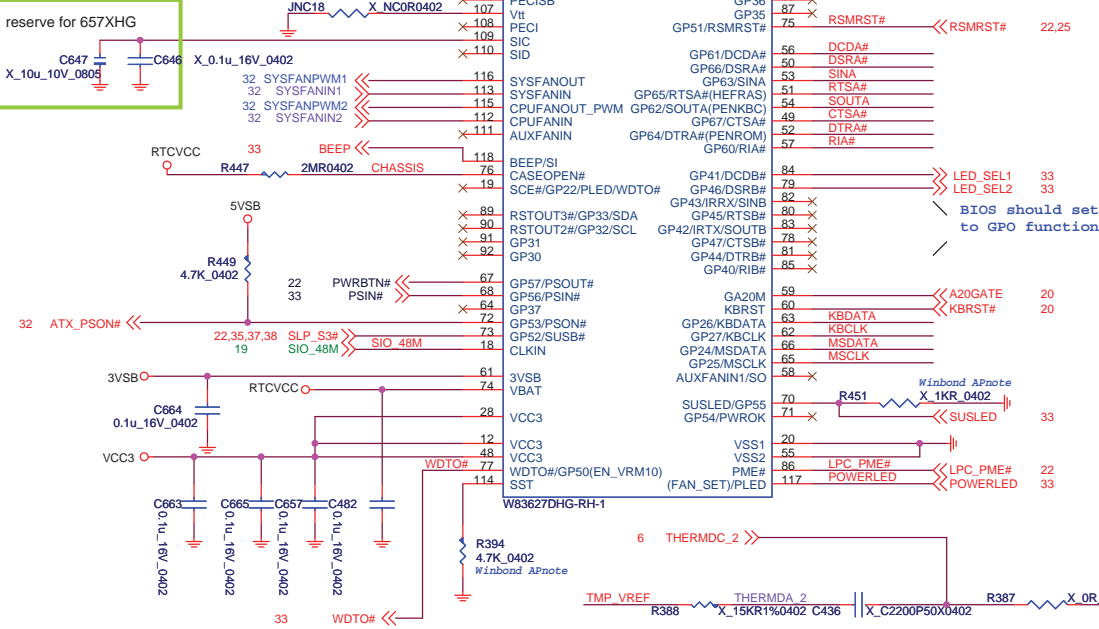
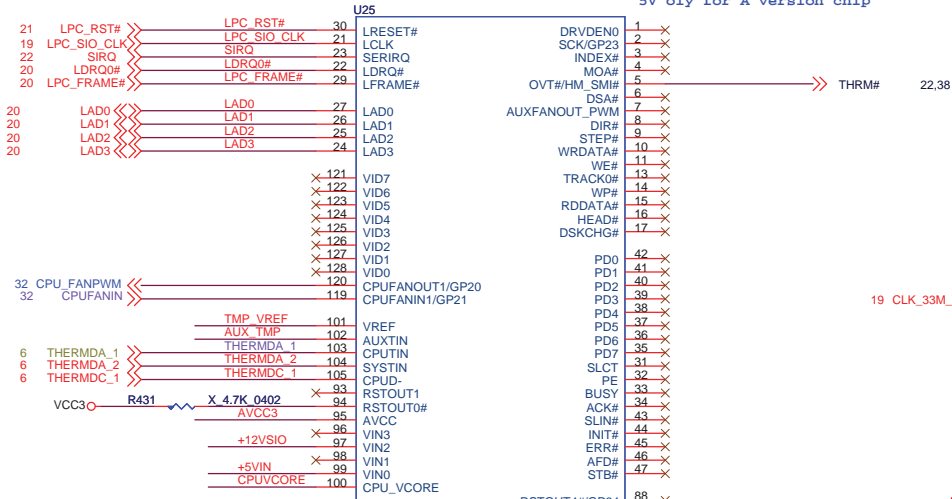
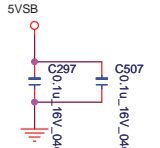
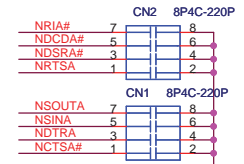
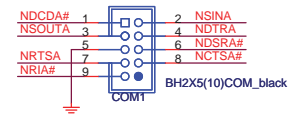
TPM



FOR EMI



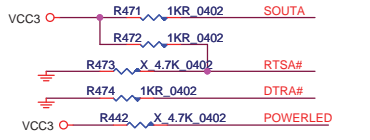
COM1



BIOS should set to GPO function

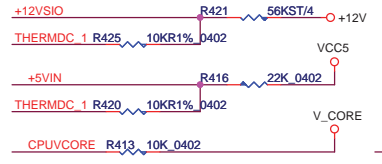
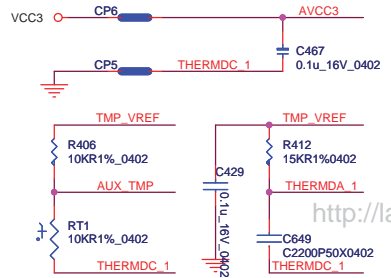
Winbond A>Note

LPC I/O STRAPPING RESISTOR



RTSA#	L: CFAD=2E	H: CFAD=4E
GP50	L: TTL LEVEL	H: GTL LEVEL
SOUTA	L: KBC DISABLE	H: KBC ENABLE
DTRA#	L: DISABLE SPI	H: ENABLE SPI
FAN SET1	L: CPU1 PWM50%	H: CPU1 PWM100%

Hardware Monitor



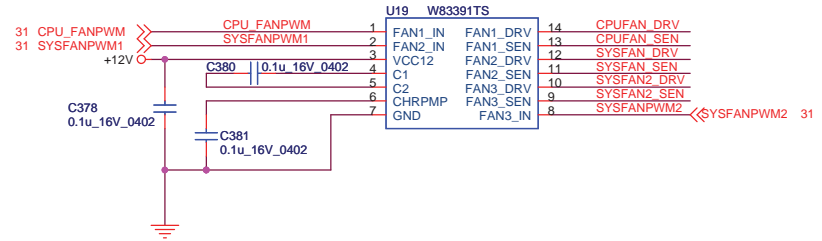
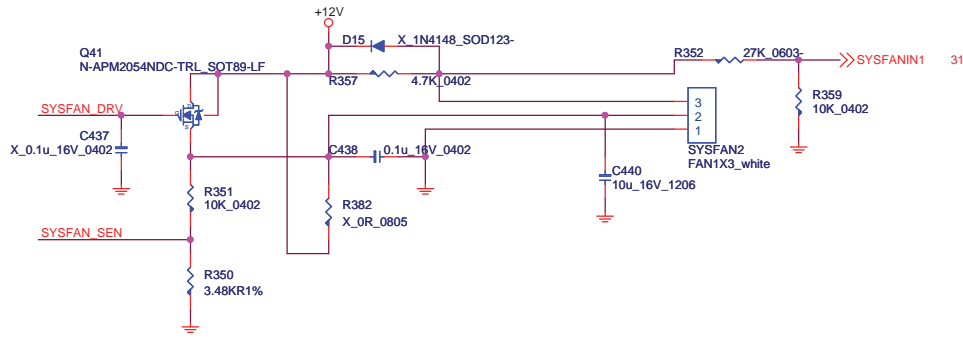
<http://laptop-motherboard-schematic.blogspot.com/>

MSI CORPORATION

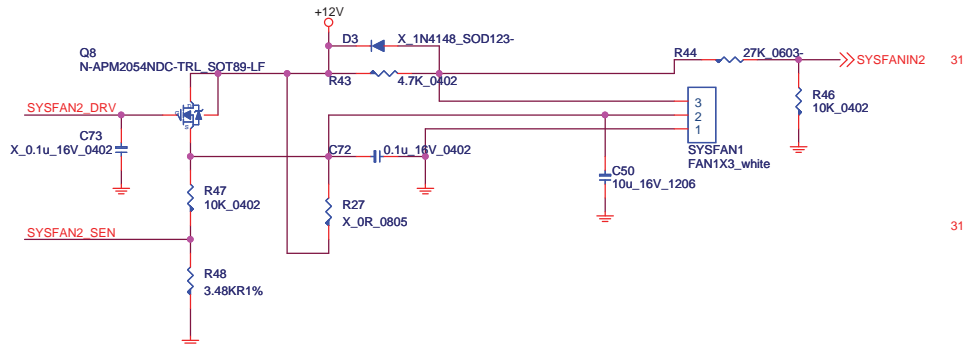
Title	<b>SIO W83627DHG</b>		Rev	0A
Size	Document Number			
Customer	<b>MS-96A9</b>			
Date:	Thursday, February 21, 2008	Sheet	31	of 41

# FAN CONTROL

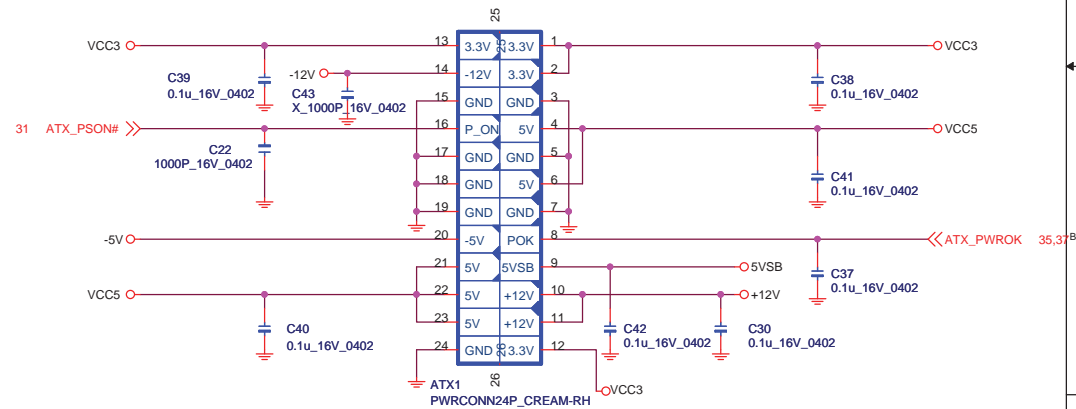
## SYSTEM FAN 1



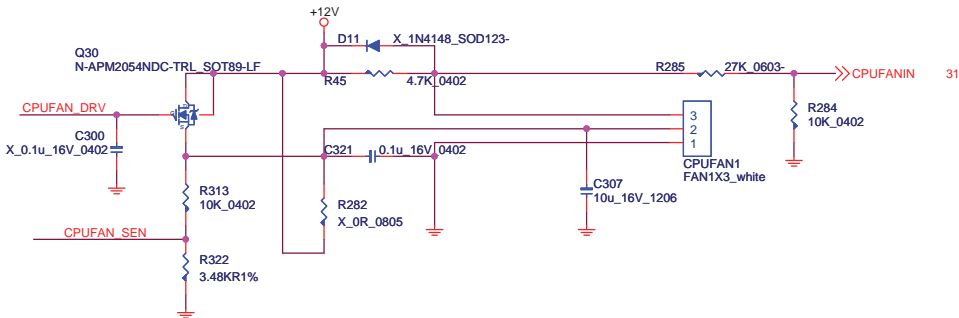
## SYSTEM FAN 2



## ATX Connector



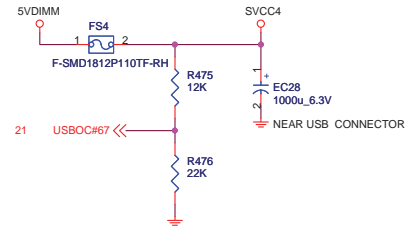
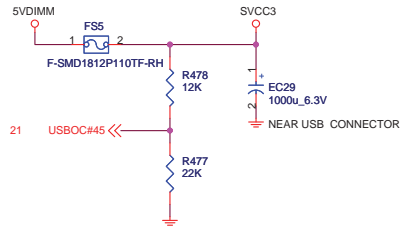
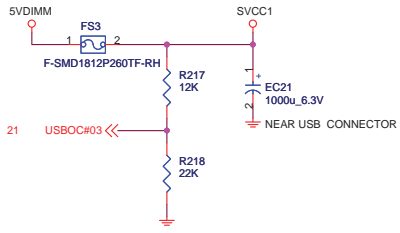
## CPU FAN



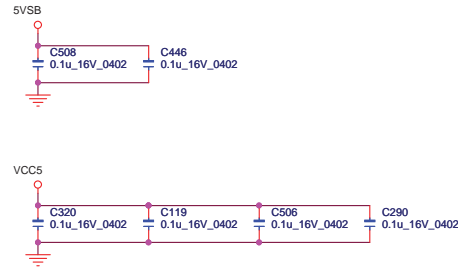
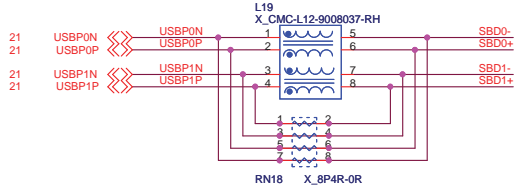
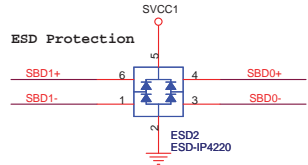
<b>MSI CORPORATION</b>		
Title		
<b>FAN,ATX</b>		
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	0A
Date:	Tuesday, February 19, 2008	Sheet 32 of 41



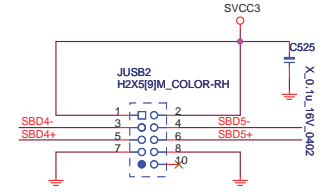
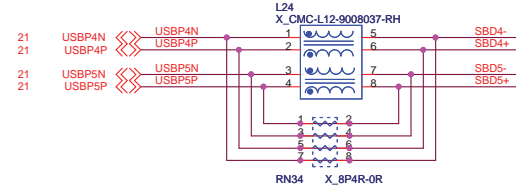
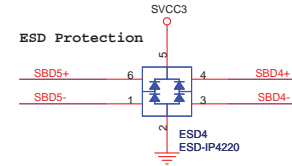




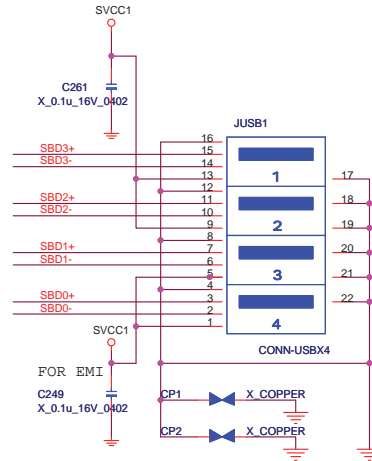
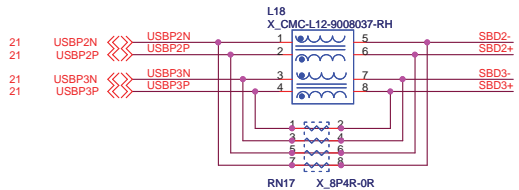
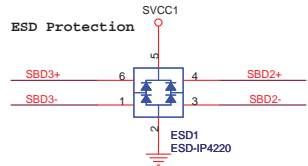
**REAR PANEL USB CONNECTOR FOR USB PORT 0,1**



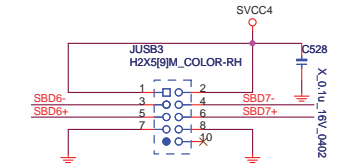
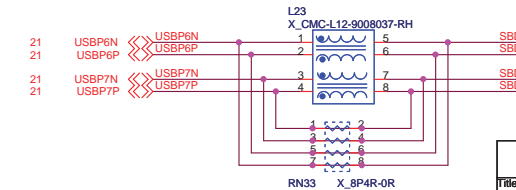
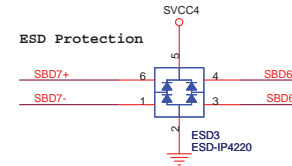
**FRONT PANEL USB CONNECTOR FOR USB PORT 4,5**



**REAR PANEL USB CONNECTOR FOR USB PORT 2,3**

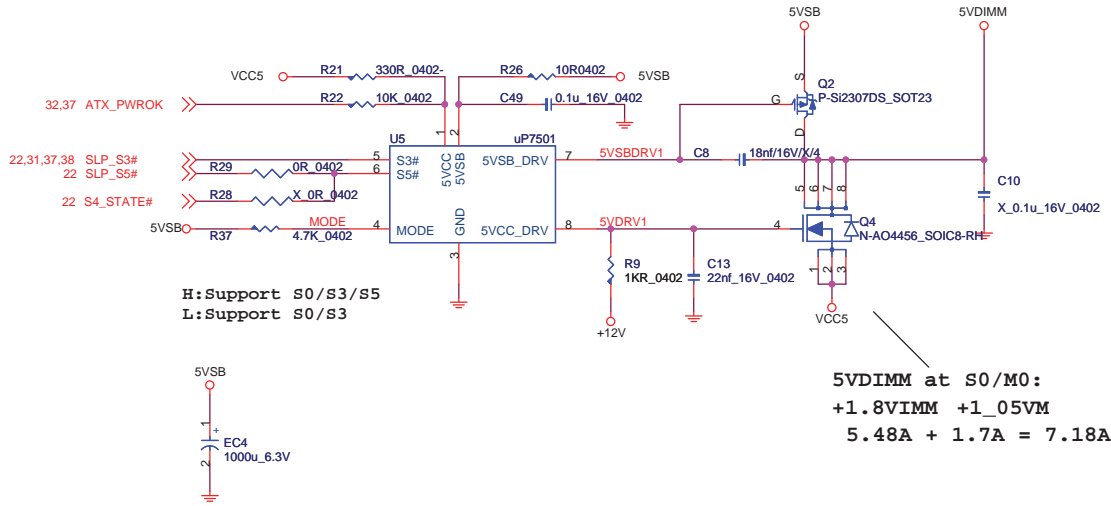


**FRONT PANEL USB CONNECTOR FOR USB PORT 6,7**

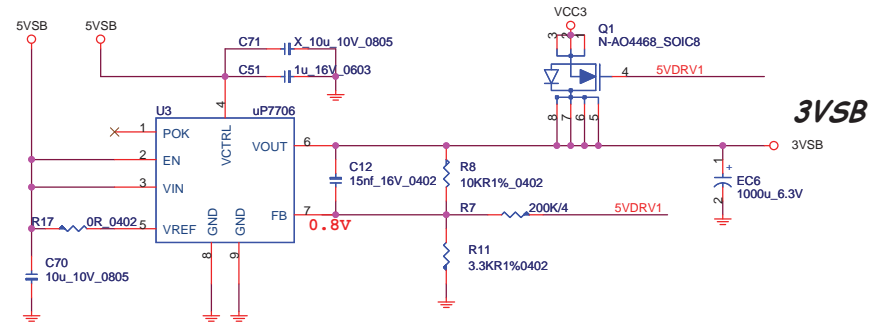


<b>MSI CORPORATION</b>		
<b>USB</b>		
Title	Document Number	Rev
Size	MS-96A9	0A
Customer		
Date: Tuesday, February 19, 2008	Sheet 34 of 41	

# 5VDIMM FOR DDR/AMT



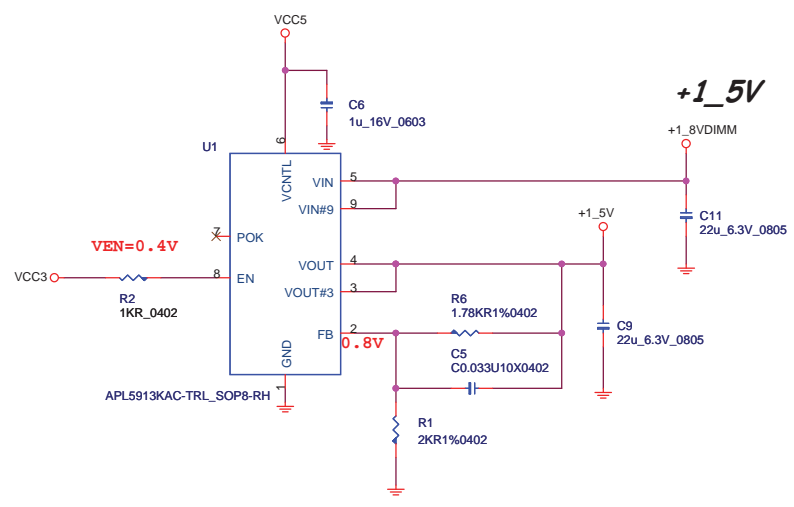
# 5VDIMM



**5VDIMM at S0/M0:**  
**+1.8VIMM +1\_05VM**  
**5.48A + 1.7A = 7.18A**

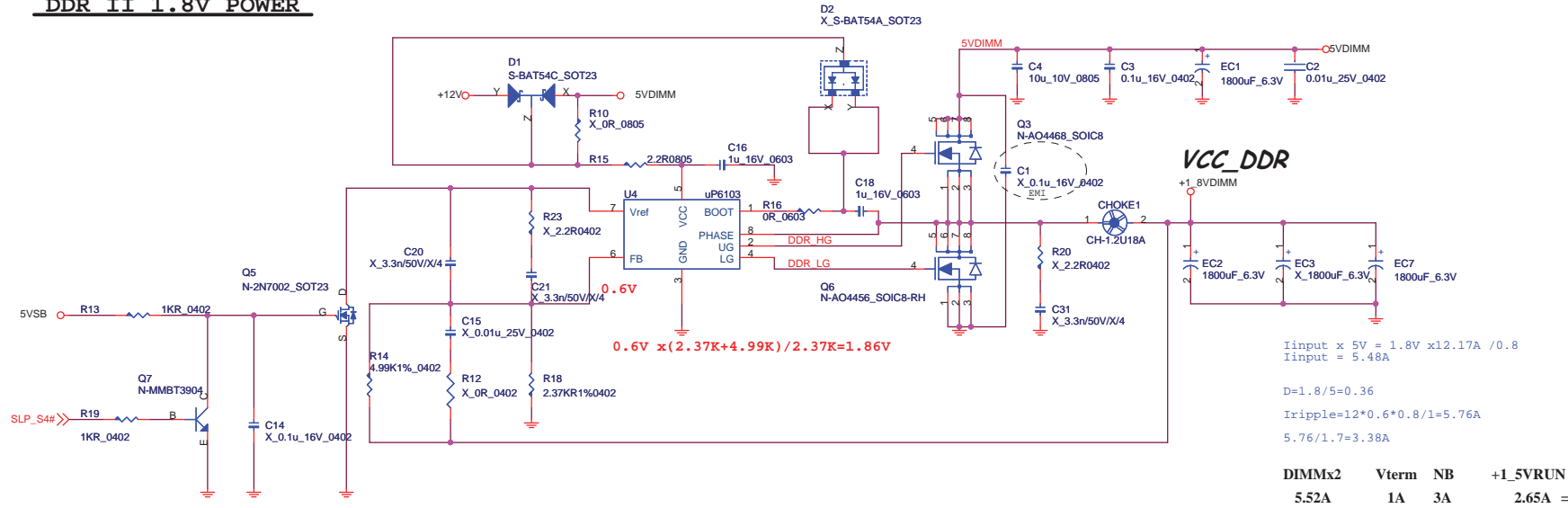
# +1\_5V

**SB**  
**2A**  
**CPU**  
**0.5A = 2.5A**



<b>MSI CORPORATION</b>		
Title		
<b>POWER 5VDIMM/3VSB/+1.5V</b>		
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	0A
Date:	Tuesday, February 19, 2008	Sheet 35 of 41

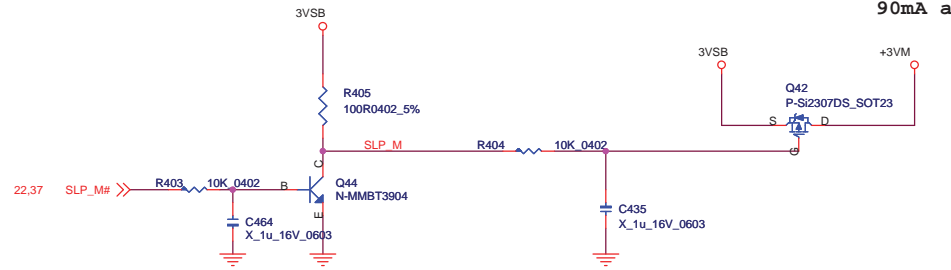
**DDR II 1.8V POWER**



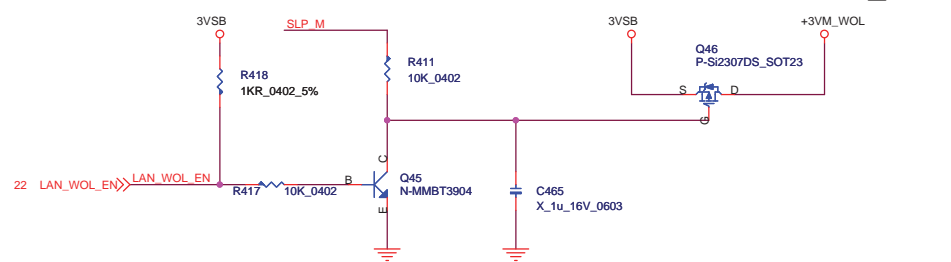
$I_{input} \times 5V = 1.8V \times I_{2.17A} / 0.8$   
 $I_{input} = 5.48A$   
 $D = 1.8 / 5 = 0.36$   
 $I_{ripple} = 12 \times 0.6 \times 0.8 / 1 = 5.76A$   
 $5.76 / 1.7 = 3.38A$   
**DIMMx2**    **Vterm**    **NB**    **+1.5VRUN**  
 5.52A    1A    3A    2.65A =

12.17A

**+3VM**  
90mA at AMT mode



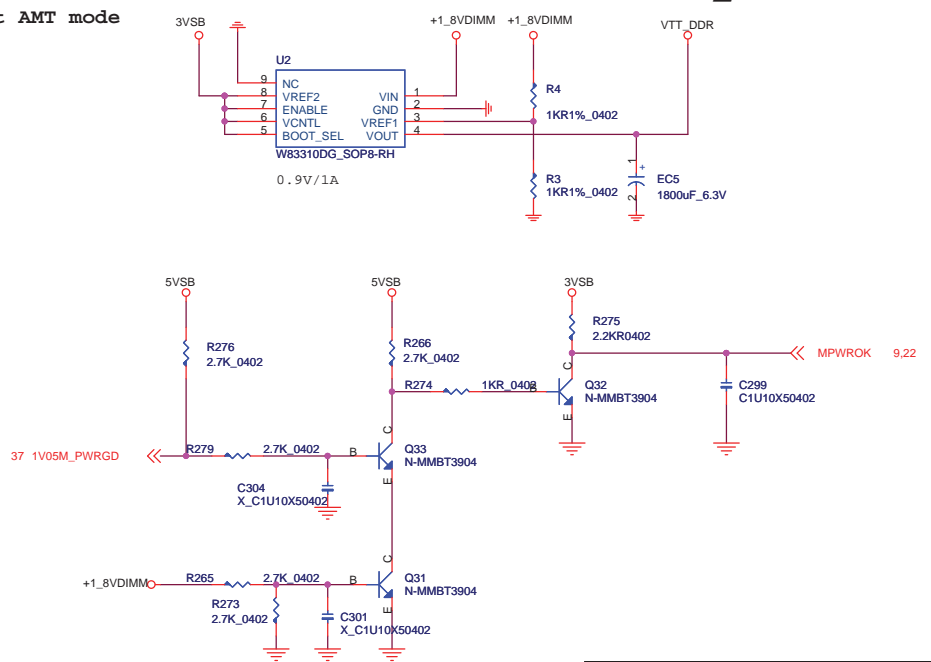
**+3VM\_WOL for ICH9**  
150mA at S3/S4/S5



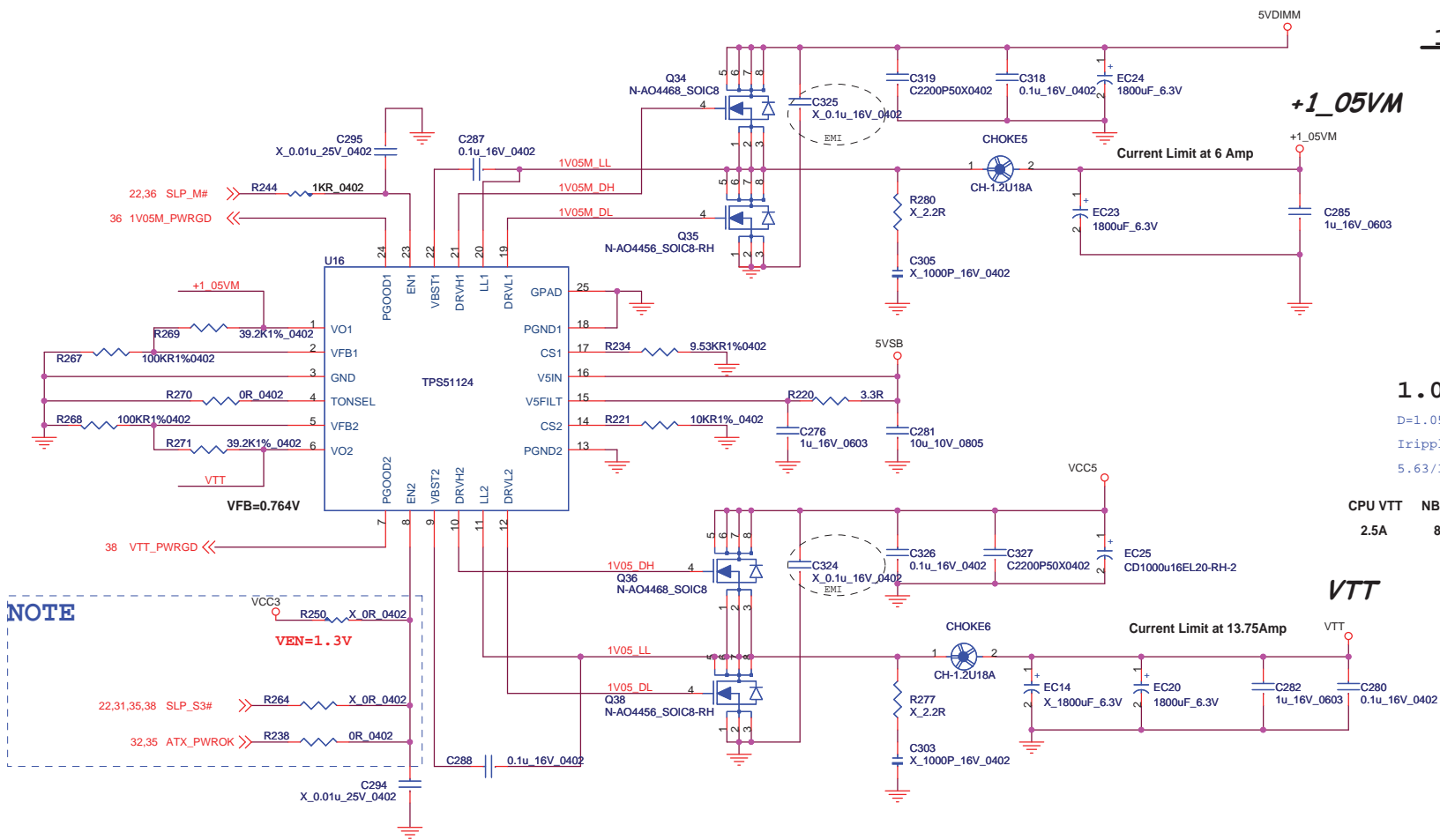
Default Tri-State from ICH9  
pull-up for default WOL after G3

**DDR VTT Power**

**VTT\_DDR**



<b>MSI CORPORATION</b>		
Title	<b>POWER VTT_DDR/+3VM/+3VM_WOL/+1.8VDIMM</b>	
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	0A
Date:	Tuesday, February 19, 2008	Sheet 36 of 41



**1.05VM for AMT**

$I_{input} \times 5V = 1.05V \times 6.5A / 0.8$   
 $I_{input} = 1.7A$   
 $D = 1.05/5 = 0.21$   
 $r_{ripple} = 6.5 \times 0.46 \times 0.89 / 1 = 2.66A$   
 $2.66 / 1.7 = 1.56A$   
**TOTAL 6.5A**

**1.05VM for VTT & VGFX**

$D = 1.05/5 = 0.21$   
 $r_{ripple} = 13.75 \times 0.46 \times 0.89 / 1 = 5.63A$   
 $5.63 / 1.7 = 3.31A$

CPU VTT	NB Graphic Core	NB VTT	SB
2.5A	8.7A	0.85A	1.7A = 13.75A

**NOTE**

VCC3

VEN=1.3V

22,31,35,38 SLP\_S3#

32,35 ATX\_PWROK

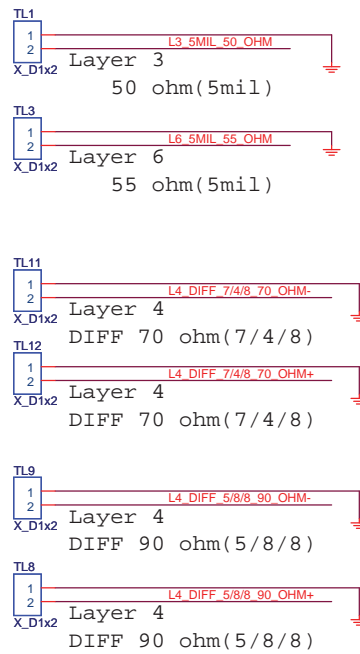
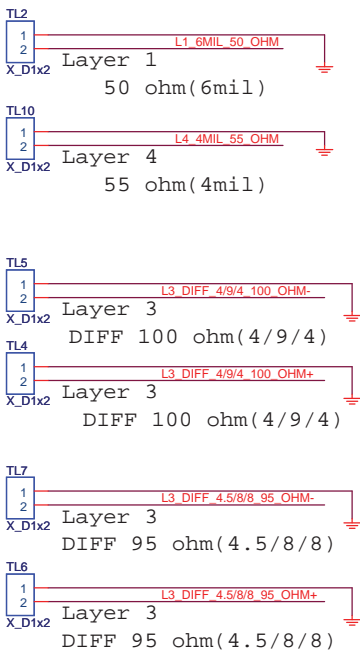
**VTT**

Current Limit at 13.75Amp

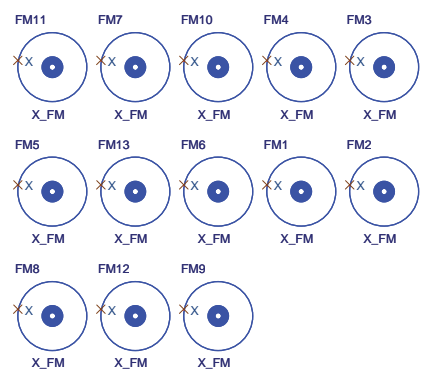
<b>MSI CORPORATION</b>			
Title			
<b>M_Graphics Core +1.05VM/VTT</b>			
Size	Document Number	Rev	
Custom	<b>MS-96A9</b>	0A	
Date:	Tuesday, February 19, 2008	Sheet	37 of 41



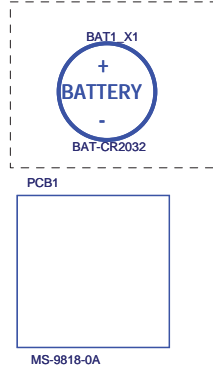
**IMPEDANCE TRACE**



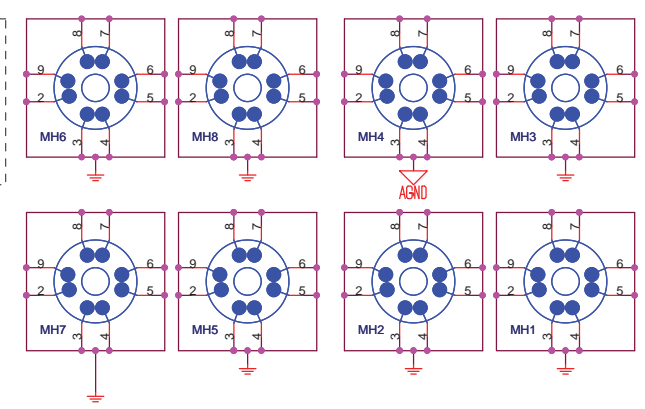
**Optics Orientation Holes**



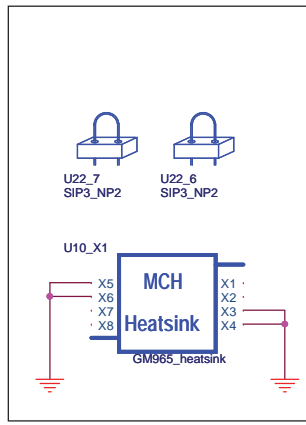
**RTC Battery**



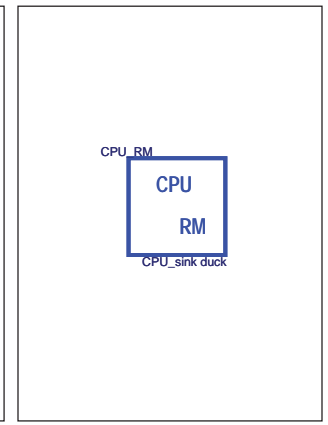
**Mounting Holes**



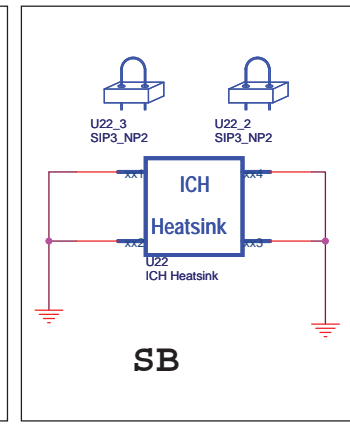
**NB**



**CPU**



**SB**



<b>MSI CORPORATION</b>		
Title		
<b>Screw &amp; EMI</b>		
Size	Document Number	Rev
Custom	<b>MS-96A9</b>	0A
Date:	Tuesday, February 19, 2008	Sheet 39 of 41

## ICH9 GPIO setting

GPIO	Alt Func	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	PMSYNC#	I/O	Core	3.3V	GPI	PM_SYNC#
GPIO[1]	GPIO1	I/O	Core	3.3V	GPI	SB_GPIO1
GPIO[2]	PIRQE#	I/OD	Core	5V	GPI	INT_PIRQE#
GPIO[3]	PIRQF#	I/OD	Core	5V	GPI	INT_PIRQF#
GPIO[4]	PIRQG#	I/OD	Core	5V	GPI	INT_PIRQG#
GPIO[5]	PIRQH#	I/OD	Core	5V	GPI	INT_PIRQH#
GPIO[6]	GPIO6	I/O	Core	3.3V	GPI	SB_GPIO6
GPIO[7]	GPIO7	I/O	Core	3.3V	GPI	SB_GPIO7
GPIO[8]	GPIO8	I/O	Resume	3.3V	GPI	SB_GPIO8
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	LAN_WOL_EN
GPIO[10]	SUS_PWR_ACK	I/O	Resume	3.3V	GPI	SUSPWRACK
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	SMBALERT#
GPIO[12]	LAN_PHY_PWR_CTRL	I/O	Resume	3.3V	GPO	LAN_PHY_PCTRL
GPIO[13]	ENERGY_DETECT	I/O	Resume	3.3V	GPI	LPC_PME#
GPIO[14]	AC_PRESENT	I/O	Resume	3.3V	GPI	AC_PERSENT
GPIO[15]	UNUSED (DP)	I/O	Resume	3.3V	Native	UNUSED (DP)
GPIO[16]	DPRSLPVR	I/O	Core	3.3V	GPO	PM_DPRSLPVR
GPIO[17]	GPIO17	I/O	Core	3.3V	GPI	SB_GPIO17
GPIO[18]	GPIO18	I/O	Core	3.3V	GPO	SB_GPIO18
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	SATA1GP
GPIO[20]	GPIO20	I/O	Core	3.3V	GPO	SB_GPIO20
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	SATA0GP
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	SB_GPIO22
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	LDRQ1#
GPIO[24]	MEM_LED	I/O	Resume	3.3V	GPO	SB_GPIO24
GPIO[25]	UNUSED (DP)	I/O	Resume	3.3V	Native	UNUSED (DP)
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	S4_STATE#
GPIO[27]	GPIO27	I/O	Resume	3.3V	GPO	LAN1_DISABLE#
GPIO[28]	GPIO28	I/O	Resume	3.3V	GPO	SB_GPIO28
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	USBOC#45
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	USBOC#67
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	USBOC#67
GPIO[32]	UNUSED (DP)	I/O	Core	3.3V	GPO	UNUSED (DP)
GPIO[33]	HDA_DOCK_EN#	I/O	Core	3.3V	GPO	SB_GPIO33
GPIO[34]	HDA_DOCK_RST#	I/O	Core	3.3V	GPO	SB_GPIO34
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	SB_GPIO35
GPIO[36]	SATA4GP	I/O	Core	3.3V	GPI	SATA2GP
GPIO[37]	SATA5GP	I/O	Core	3.3V	GPI	SATA3GP
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	MB_ID0
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	MB_ID1
GPIO[40]	OC1#	I/O	Resume	3.3V	Native	USBOC#03
GPIO[41]	OC2#	I/O	Resume	3.3V	Native	USBOC#03
GPIO[42]	OC3#	I/O	Resume	3.3V	Native	USBOC#03
GPIO[43]	OC4#	I/O	Resume	3.3V	Native	USBOC#45
GPIO[44]	OC8#	I/O	Resume	3.3V	Native	USBOC#8_11
GPIO[45]	OC9#	I/O	Resume	3.3V	Native	USBOC#8_11
GPIO[46]	OC10#	I/O	Resume	3.3V	Native	USBOC#8_11
GPIO[47]	OC11#	I/O	Resume	3.3V	Native	USBOC#8_11
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	SB_GPIO48
GPIO[49]	GPIO49	I/O	Core	3.3V	GPO	UNUSED
GPIO[50]	REQ1#	I/O	Core	5V	Native	PCI_REQ#1
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PCI_GNT#1
GPIO[52]	REQ2#	I/O	Core	5V	Native	PCI_REQ#2
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PCI_GNT#2
GPIO[54]	REQ3#	I/O	Core	5V	Native	PCI_REQ#3
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	TP73
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	GLAN_DOCK#
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	3VSB
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC0#	I/O	Resume	3.3V	Native	USBOC#03
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	SMB_LINK_ALERT#

## Super IO GPIO setting

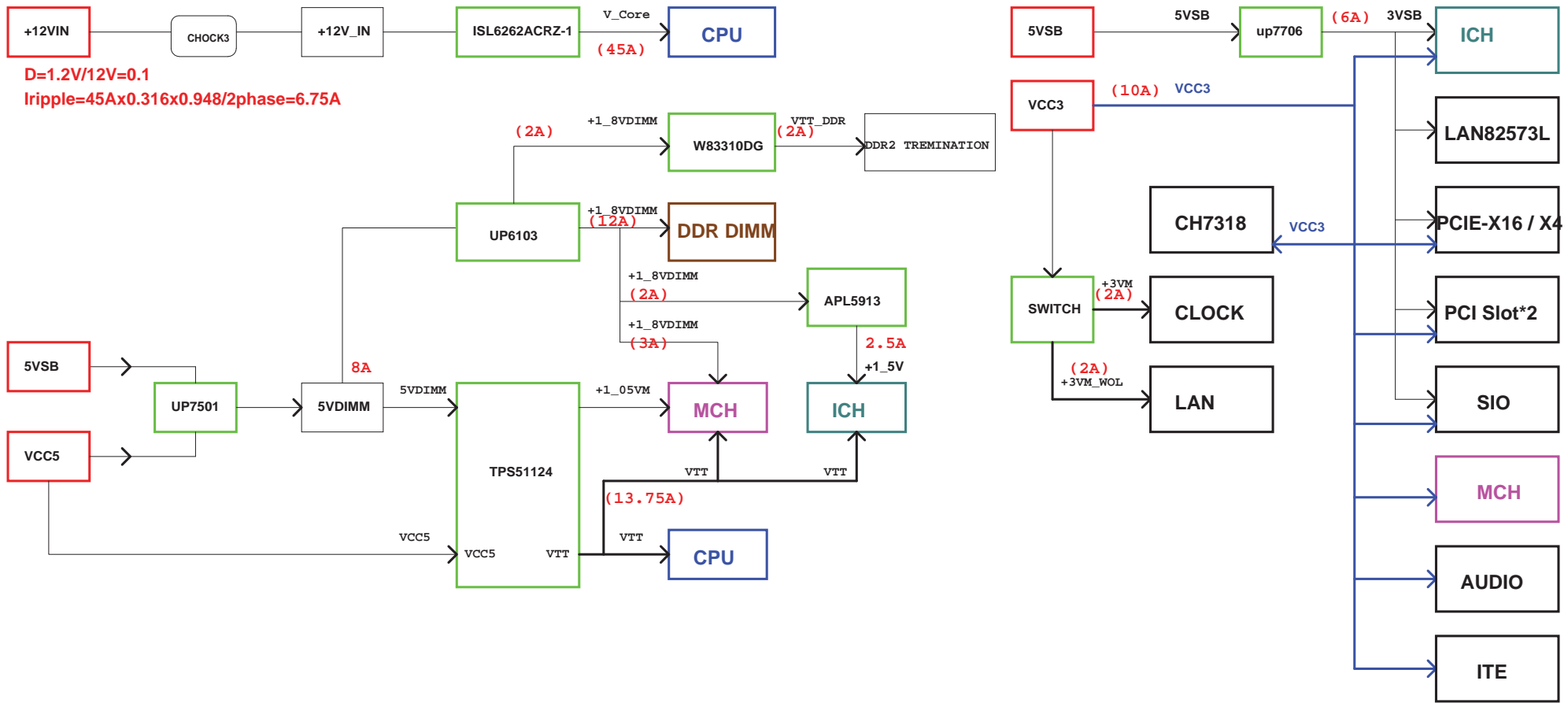
GPIO	Alt Func	Power	Signal Name	I/O
GPIO[20]	CPUFANIN1	Core	CPU_FANPWM	Output
GPIO[21]	CPUFANOUT1	Core	CPUFANIN	Input
GPIO[22]	SCE#/PLED/WDTO#	Core	unused	
GPIO[23]	SCK	Core	unused	
GPIO[24]	MSDATA	Resume	MSDATA	
GPIO[25]	MSCLK	Resume	MSCLK	
GPIO[26]	KBDATA	Resume	KBDATA	
GPIO[27]	KBCLK	Resume	KBCLK	
GPIO[30]	GP30	Resume	unused	Output
GPIO[31]	GP31	Resume	unused	Output
GPIO[32]	RSTOUT2#/SCL	Resume	unused	
GPIO[33]	RSTOUT3#/SDA	Resume	unused	
GPIO[34]	RSTOUT4#	Resume	unused	Output
GPIO[35]	GP35	Resume	unused	Output
GPIO[36]	GP36	Resume	unused	Output
GPIO[37]	GP37	Resume	unused	Output
GPIO[40]	RIB#	Resume	unused	
GPIO[41]	DCDB#	Resume	LED_SEL1	
GPIO[42]	RTX/SOUTB	Resume	unused	
GPIO[43]	RRX/SINB	Resume	unused	
GPIO[44]	DTRB#	Resume	unused	
GPIO[45]	RTSB#	Resume	unused	
GPIO[46]	DSRB#	Resume	LED_SEL2	
GPIO[47]	CTSB#	Resume	unused	
GPIO[50]	EN_VRM10/WDTO#	Resume	WDTO#	Output
GPIO[51]	RSMRST#	Resume	RSMRST#	Output
GPIO[52]	SUSB#	Resume	SLP_S3#	Input
GPIO[53]	PSON#	Resume	ATX_PSON#	Output
GPIO[54]	PWROK	Resume	unused	Output
GPIO[55]	SUSLED	Resume	SUSLED	Output
GPIO[56]	PSIN#	Resume	PSIN#	Input
GPIO[57]	PSOUT#	Resume	PWRBTN#	Output
GPIO[60]	RIA#	Core	RIA#	
GPIO[61]	DCDA#	Core	DCDA#	
GPIO[62]	SOUTA/PENKBC	Core	SOUTA	
GPIO[63]	SINA	Core	SINA	
GPIO[64]	DTRA#/PENROM	Core	DTRA#	
GPIO[65]	RTSA#/HEFRAS	Core	RTSA#	
GPIO[66]	DSRA#	Core	DSRA#	
GPIO[67]	CTSA#	Core	CTSA#	

## PCI routing

Device	Interrupt	ID select	REQ&GNT
PCI slot 1	INT_PIRQ#A INT_PIRQ#B INT_PIRQ#C INT_PIRQ#D	AD20	PCI_REQ#0 PCI_GNT#0
PCI slot 2	INT_PIRQ#B INT_PIRQ#C INT_PIRQ#D INT_PIRQ#A	AD21	PCI_REQ#1 PCI_GNT#1
ITE IT8213F	INT_PIRQ#C#	AD22	PCI_REQ#2 PCI_GNT#2

MSI CORPORATION			
Title <b>GPIO BUFFER</b>			
Size	Document Number	Rev	
Custom	<b>MS-96A9</b>	0A	
Date:	Thursday, February 21, 2008	Sheet	40 of 41





MICRO-STAR INT'L CO.,LTD.			
<b>POWER MAP</b>			
Size	Document Number	Rev	
Custom	MS-96A9	GA	
Date:	Tuesday, February 19, 2008	Sheet	41 of 41