MS-96B9 Ver:1.1

CPU:

Intel Penryn
1066-MTs Source-Synchronous (FSB)

System Chipset:

Intel CANTIGA
Intel ICH9ME

On Board Chipset:

WINBOND Super I/O -- W83627DHG
LAN1 -- 82567LM Boazman
LAN2 -- Intel 82573LM
LAN3 -- Intel 82551QM(10/100M)
BIOS -- SPI ROM 4MBit

Main Memory:

DDRII * 2 DIMM (Max 4GB)

Expansion Slots:

PCI-EX16*1
PCI-EX4*1
PCI 2.2 Slot X 2

PWM:

Controller
Intersil ISL6262ACRZ-T 2 Phase

Clock Generator:

Controller--ICS9LPRS113

MSI CORPORATION

Title: Cover Sheet

Size: Coustom | Document Number: MS-96B9 | Rev: 1.1

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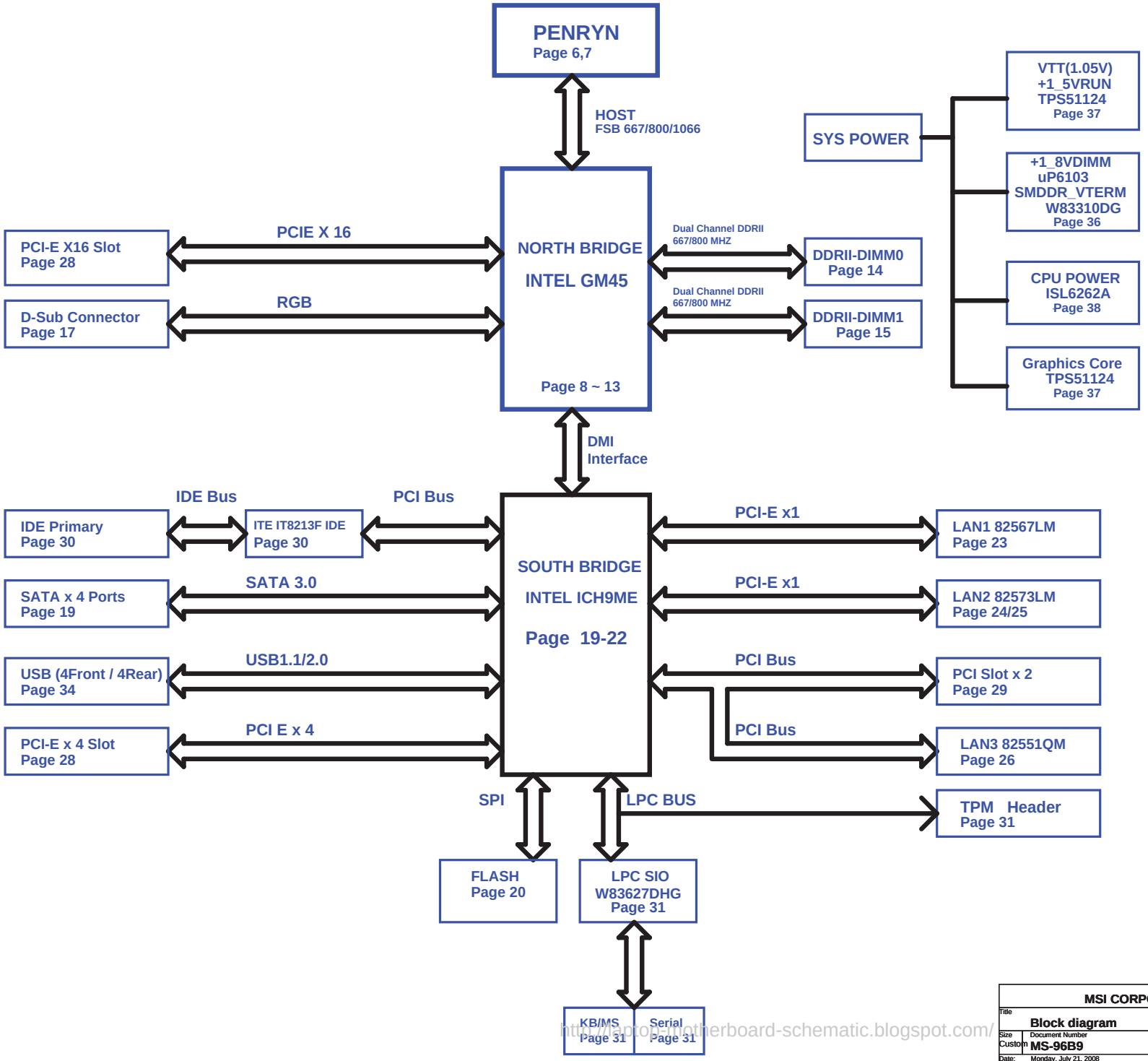

MSI CORPORATION		
Title: Block diagram		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
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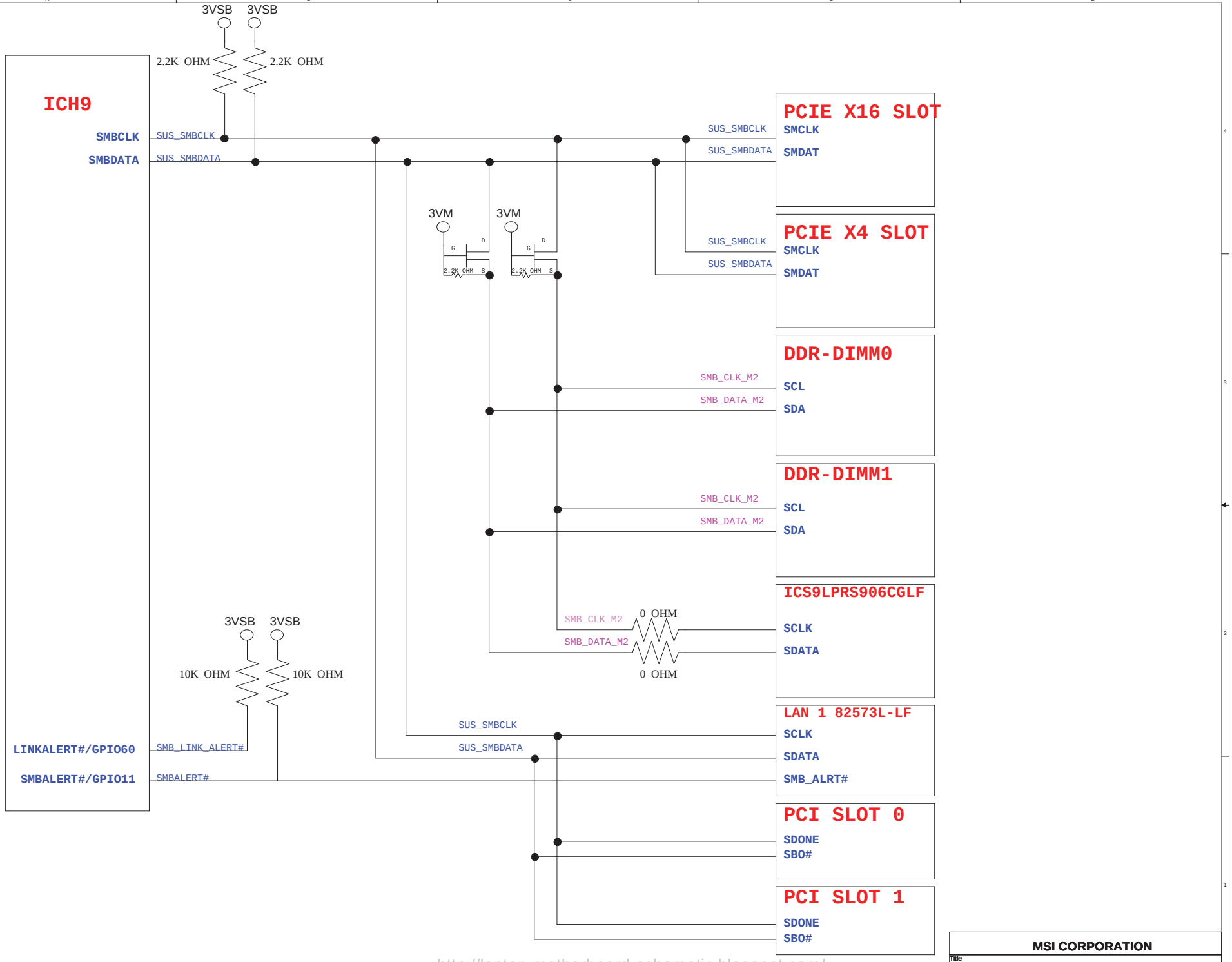

MSI CORPORATION

Title: System SMBus Block

Size: Custom | Document Number: MS-96B9 | Rev: 1.1

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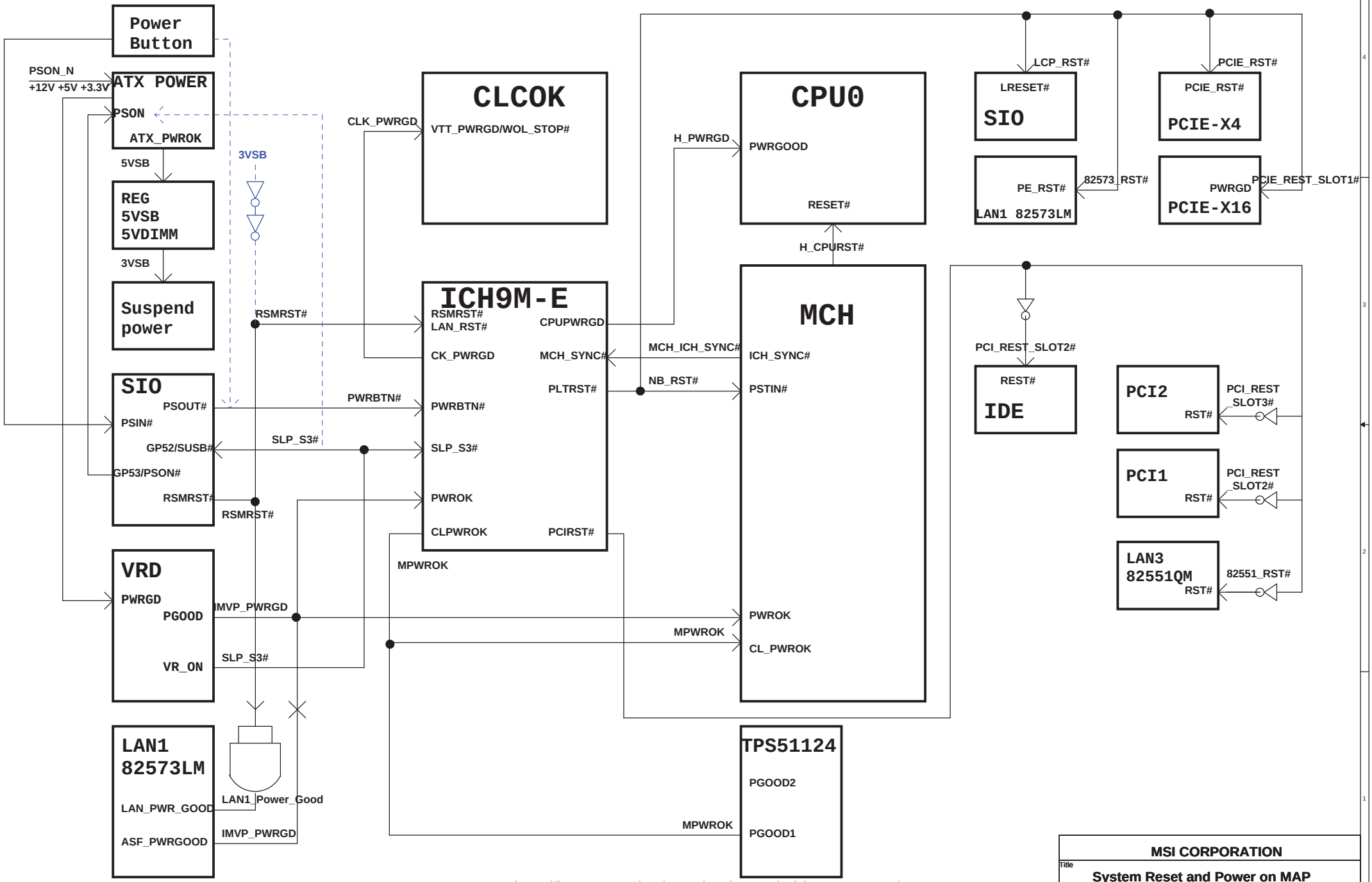
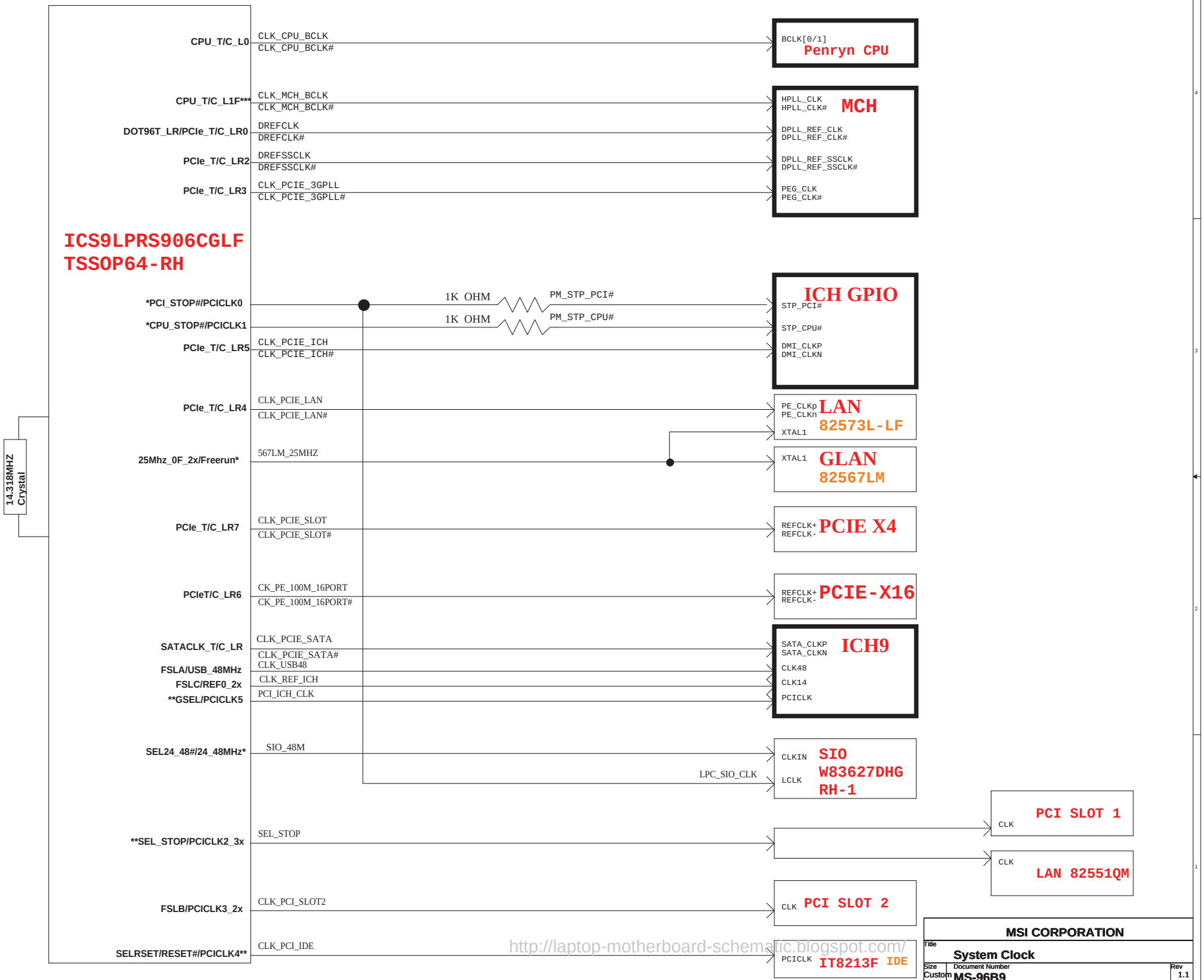
MS-96B4 SYSTEM RESET & POWER ON SEQUENCINGBLOCK DIAGRAM

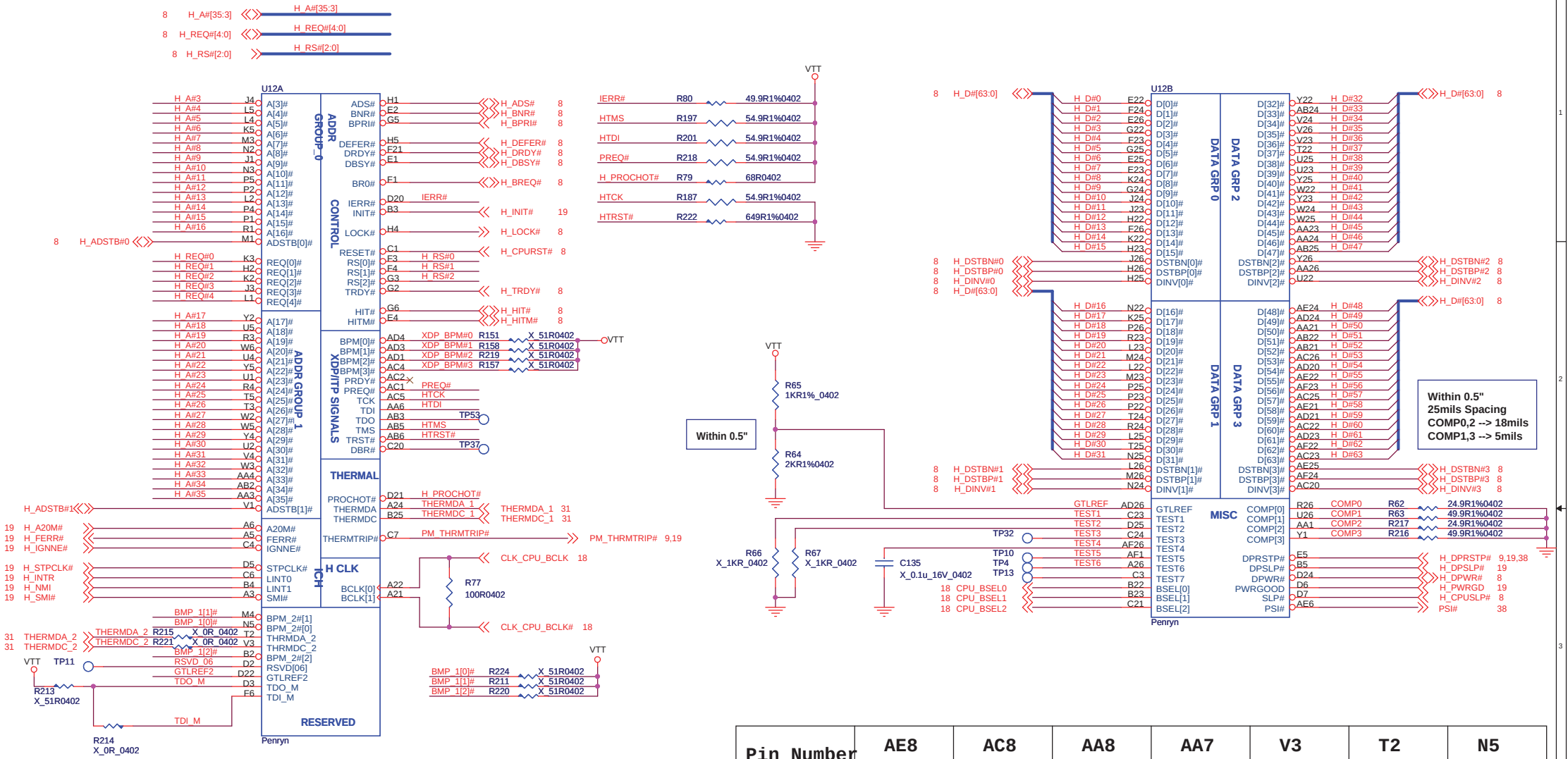


MSI CORPORATION		
Title: System Reset and Power on MAP		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
Date: Monday, July 21, 2008	Sheet 4 of 41	

MS-96B4 CLOCK BLOCK DIAGRAM

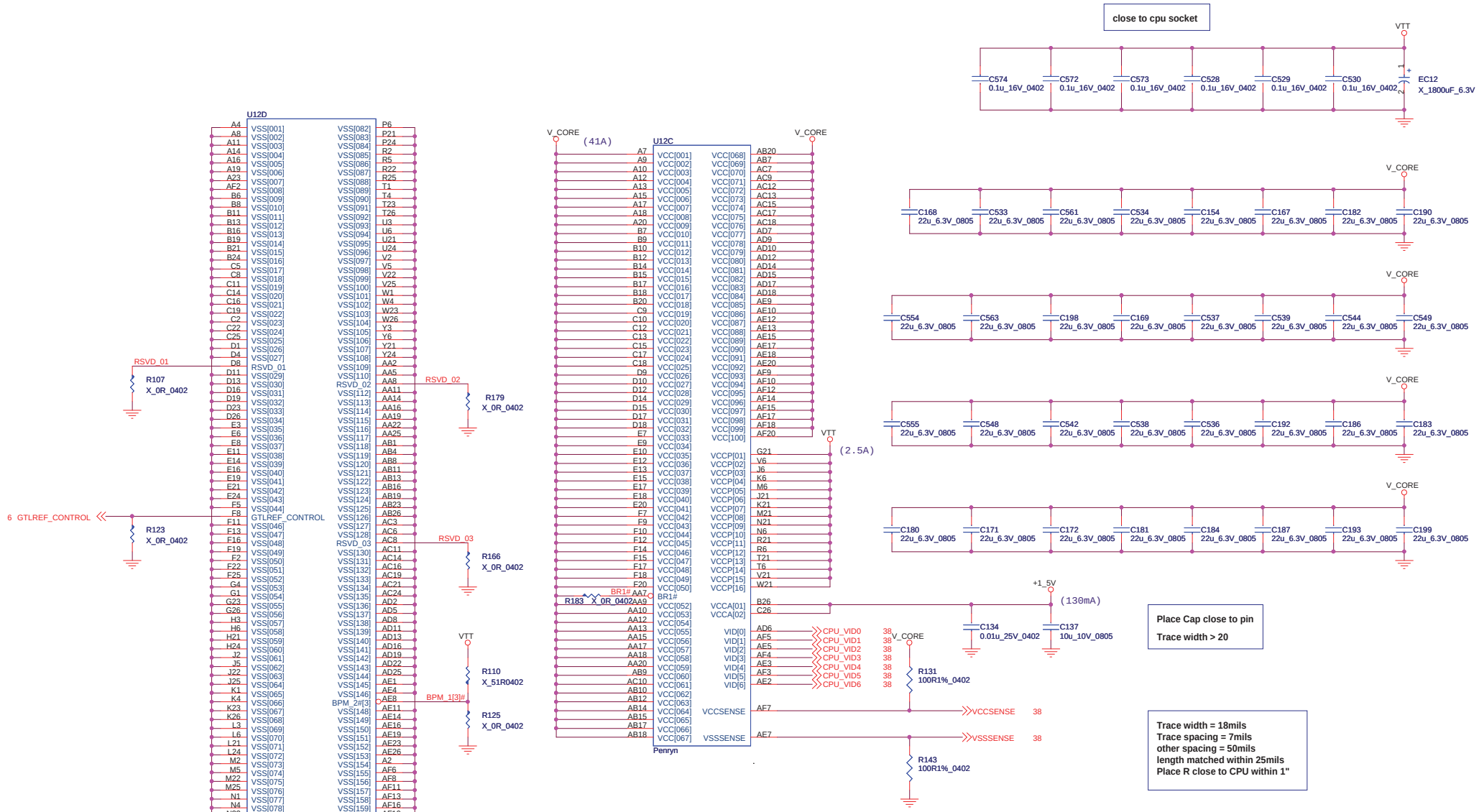


MSI CORPORATION		
Title: System Clock		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
Date: Monday, July 21, 2008	Sheet 5 of 41	



Pin Number	AE8	AC8	AA8	AA7	V3	T2	N5
Dual Core	Vss	Vss	Vss	Vcc	Rsvd	Rsvd	Rsvd
Qual Core	BPM_2#[3]	Rsvd	Rsvd	BR1#	THRMDC_2	THRMDA_2	BPM_2#[0]
Pin Number	**M4**	**F6**	**F8**	**D3**	**D8**	**B2**	**D22**
Dual Core	Rsvd	Rsvd	Vss	Rsvd	Vss	Rsvd	Rsvd
Qual Core	BPM_2#[1]	TDI_M	GTLREF_Control	TDO_M	Rsvd	BPM_2#[2]	GTLREF2

MSI CORPORATION			
Title: PENRYN-1 (HOST BUS)			
Size: Custom	Document Number: MS-96B9		Rev: 1.1
Date: Monday, July 21, 2008	Sheet 6 of 41		



MSI CORPORATION	
Title	PENRYN-2 (POWER/GND)
Size: Custom	Document Number: MS-96B9
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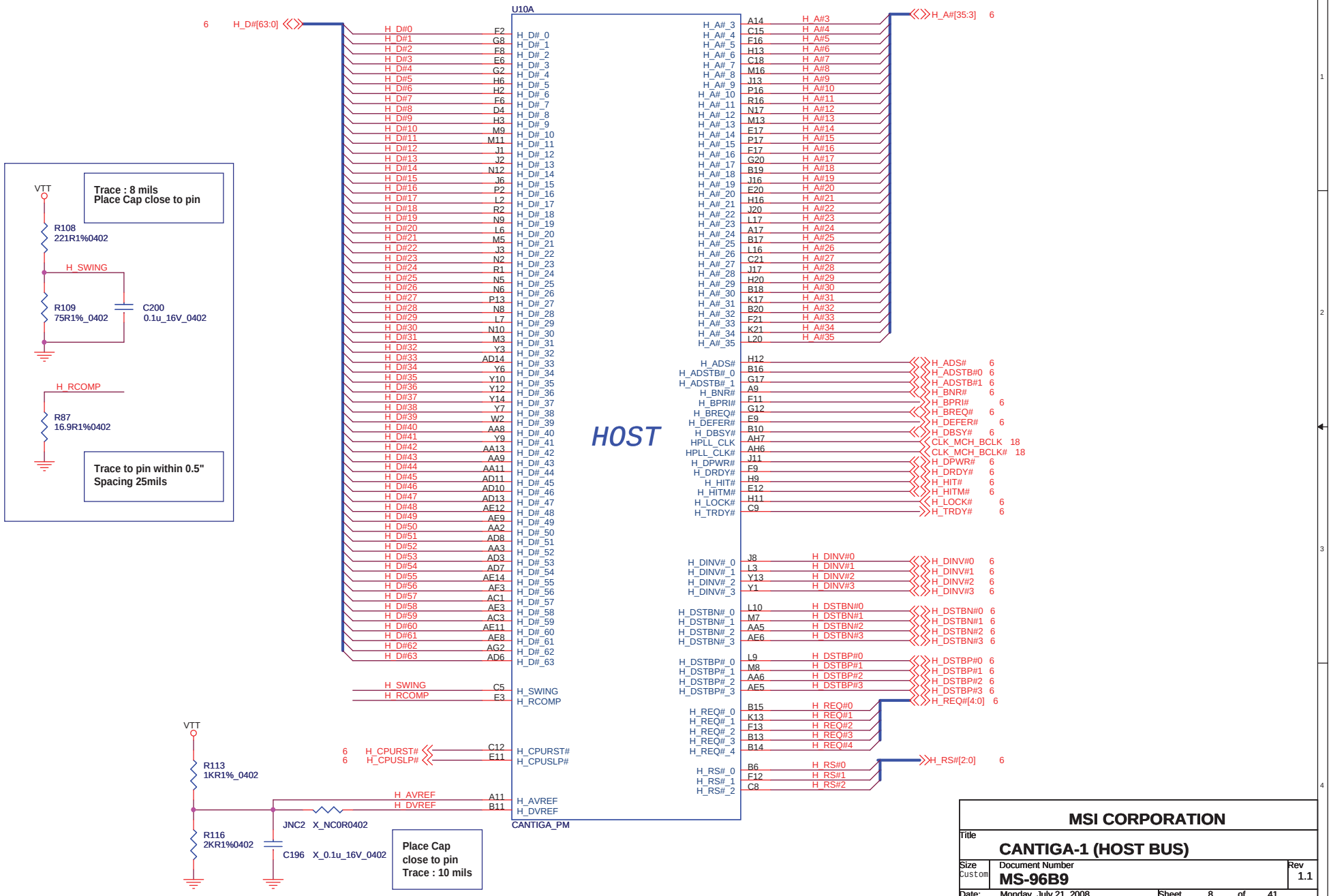
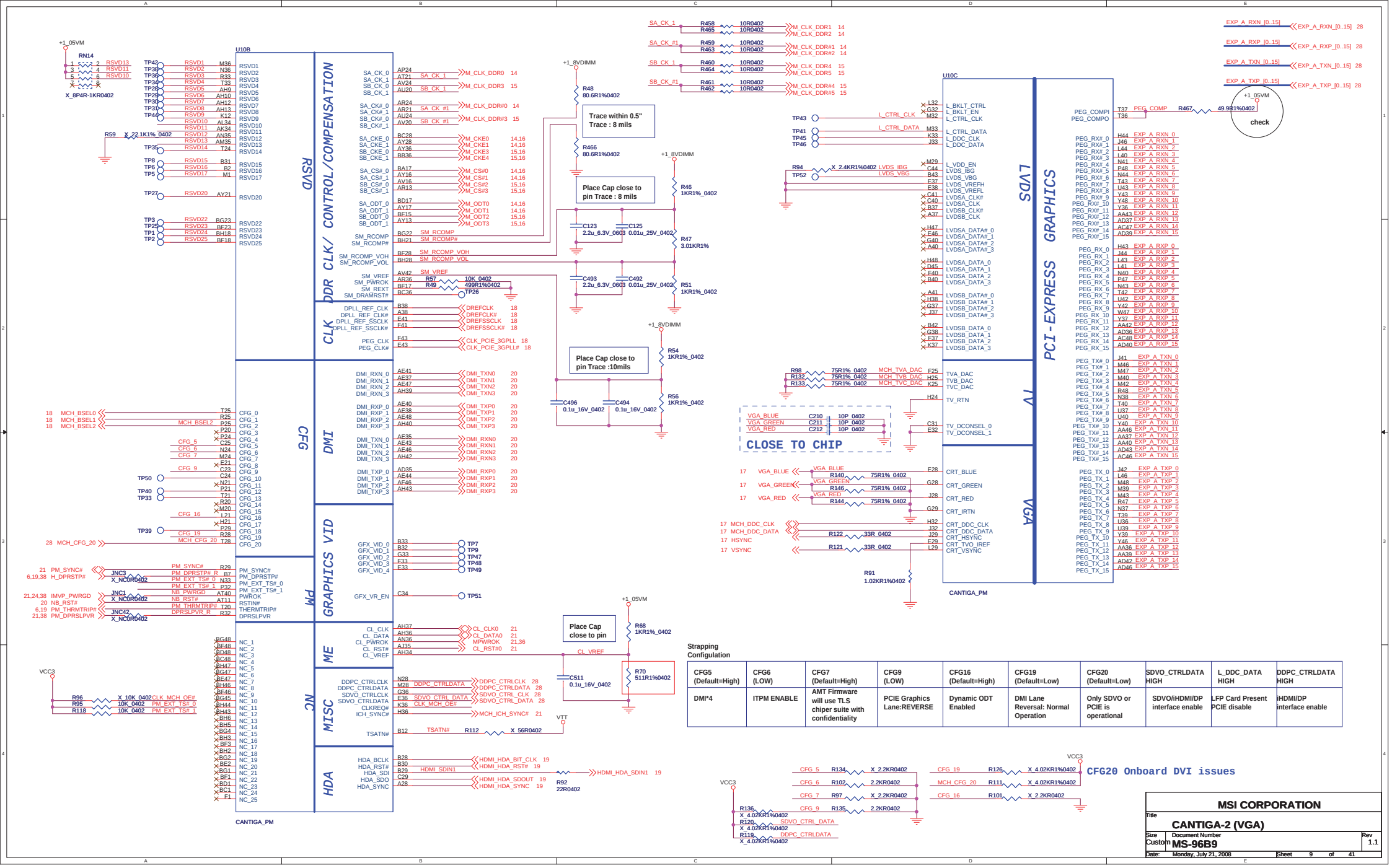
Date: Monday, July 21, 2008	Sheet 7 of 41





CFG5 (Default=High)	CFG6 (LOW)	CFG7 (Default=High)	CFG9 (LOW)	CFG16 (Default=High)	CFG19 (Default=Low)	CFG20 (Default=Low)	SDVO_CTRLDATA HIGH	L_DDC_DATA HIGH	DDPC_CTRLDATA HIGH
DMI*4	ITPM ENABLE	AMT Firmware will use TLS chiper suite with confidentiality	PCIE Graphics Lane:REVERSE	Dynamic ODT Enabled	DMI Lane Reversal: Normal Operation	Only SDVO or PCIE is operational	SDVO/iHDMI/DP interface enable	LFP Card Present PCIE disable	iHDMI/DP interface enable

MSI CORPORATION

Title: CANTIGA-2 (VGA)

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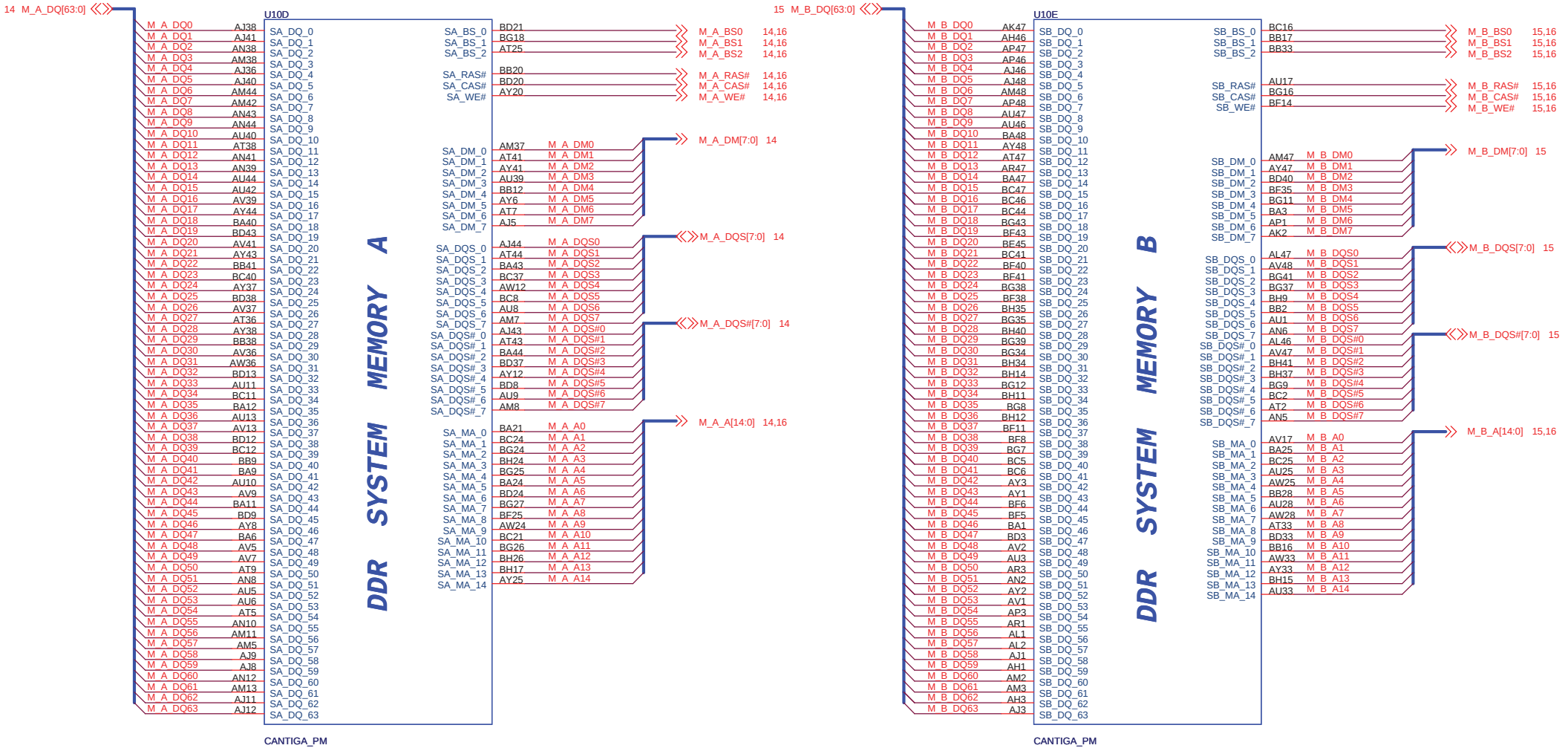
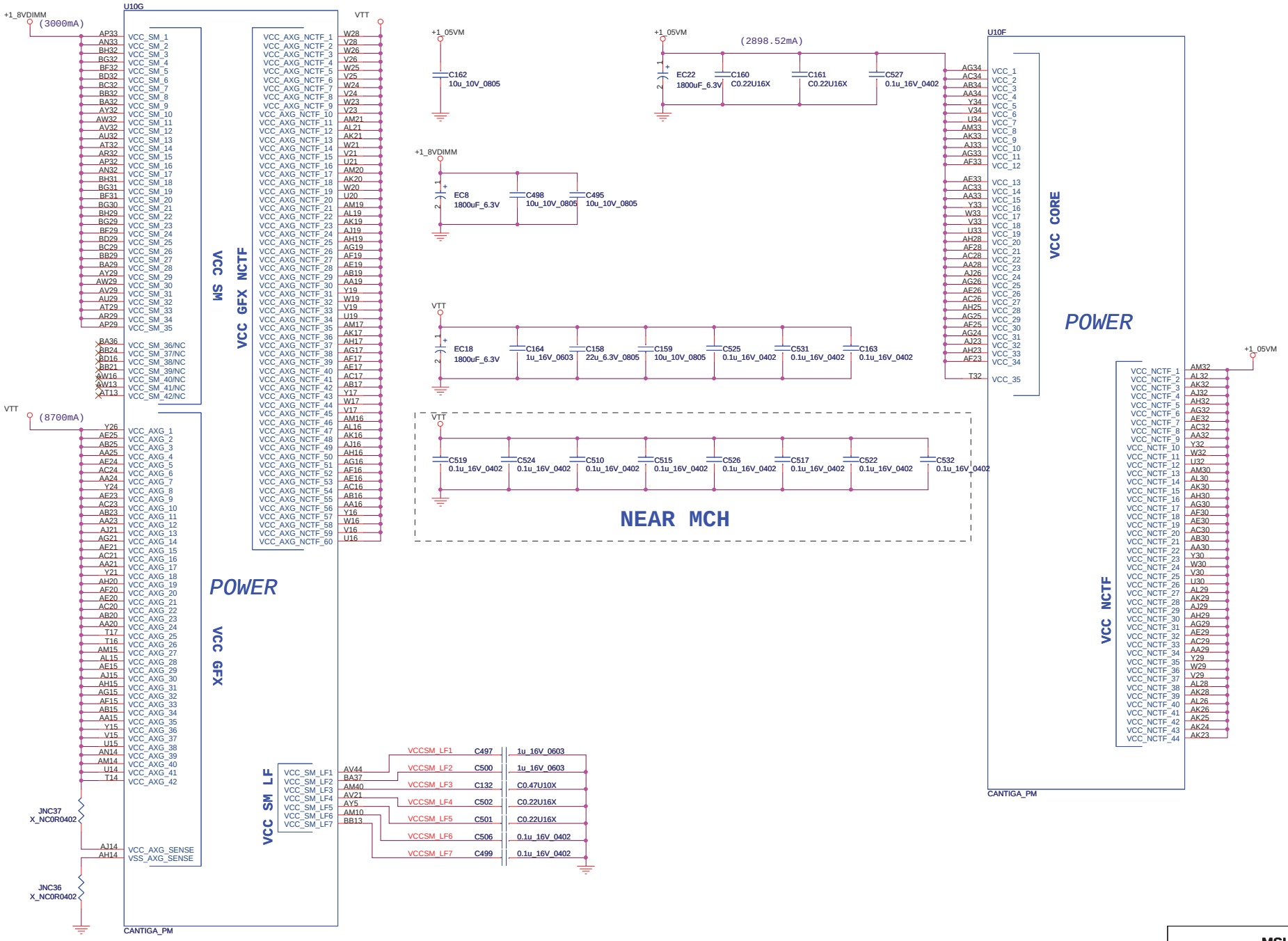


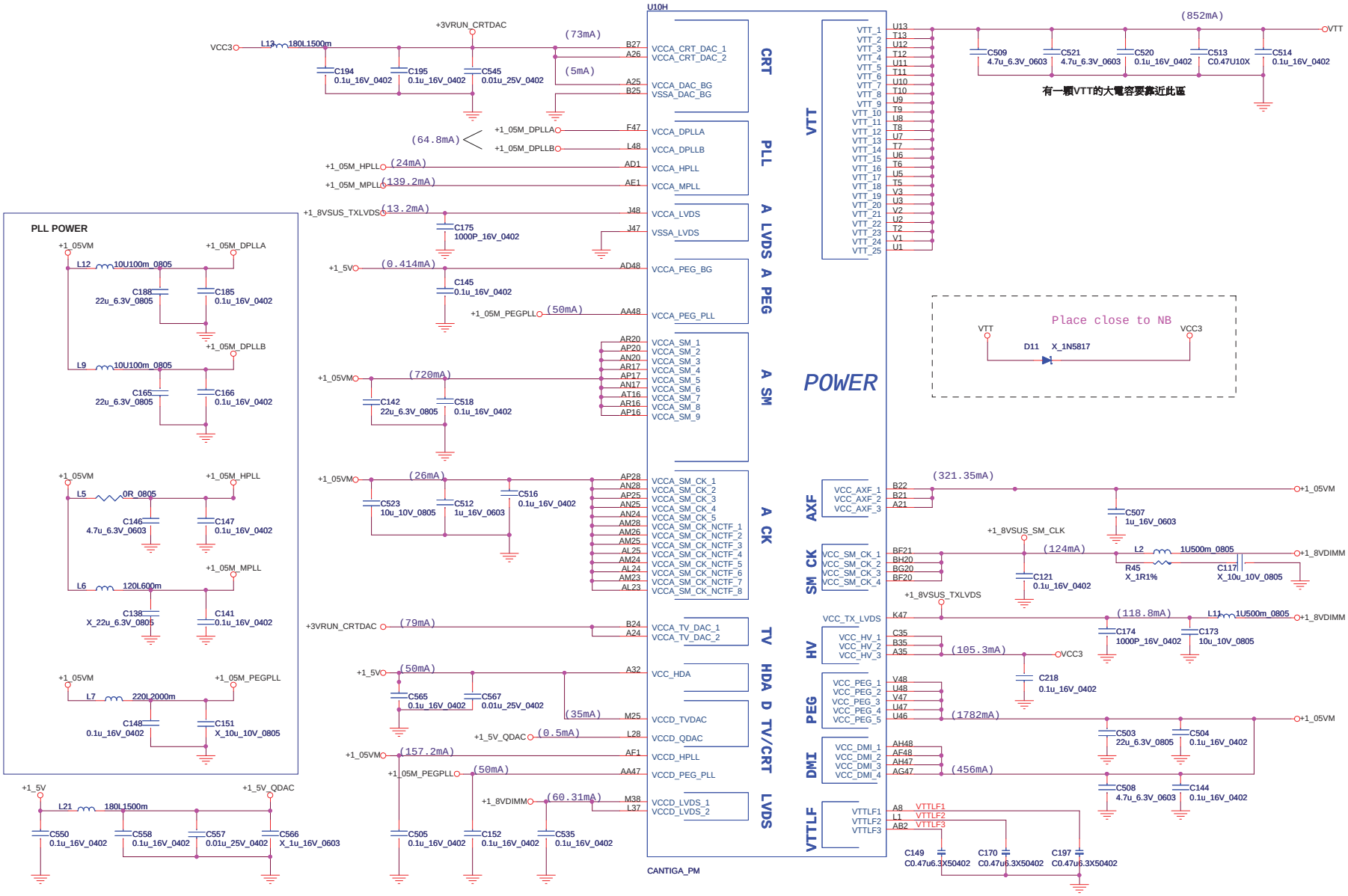


MSI CORPORATION

Title: CANTIGA-4 (POWER-1)

Size: Custom | Document Number: MS-96B9 | Rev: 1.1

Date: Monday, July 21, 2008 | Sheet 11 of 41



Company	MSI CORPORATION
Title	CANTIGA-5 (POWER-2)
Size	Custom
Document Number	MS-96B9
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Date	Monday, July 21, 2008
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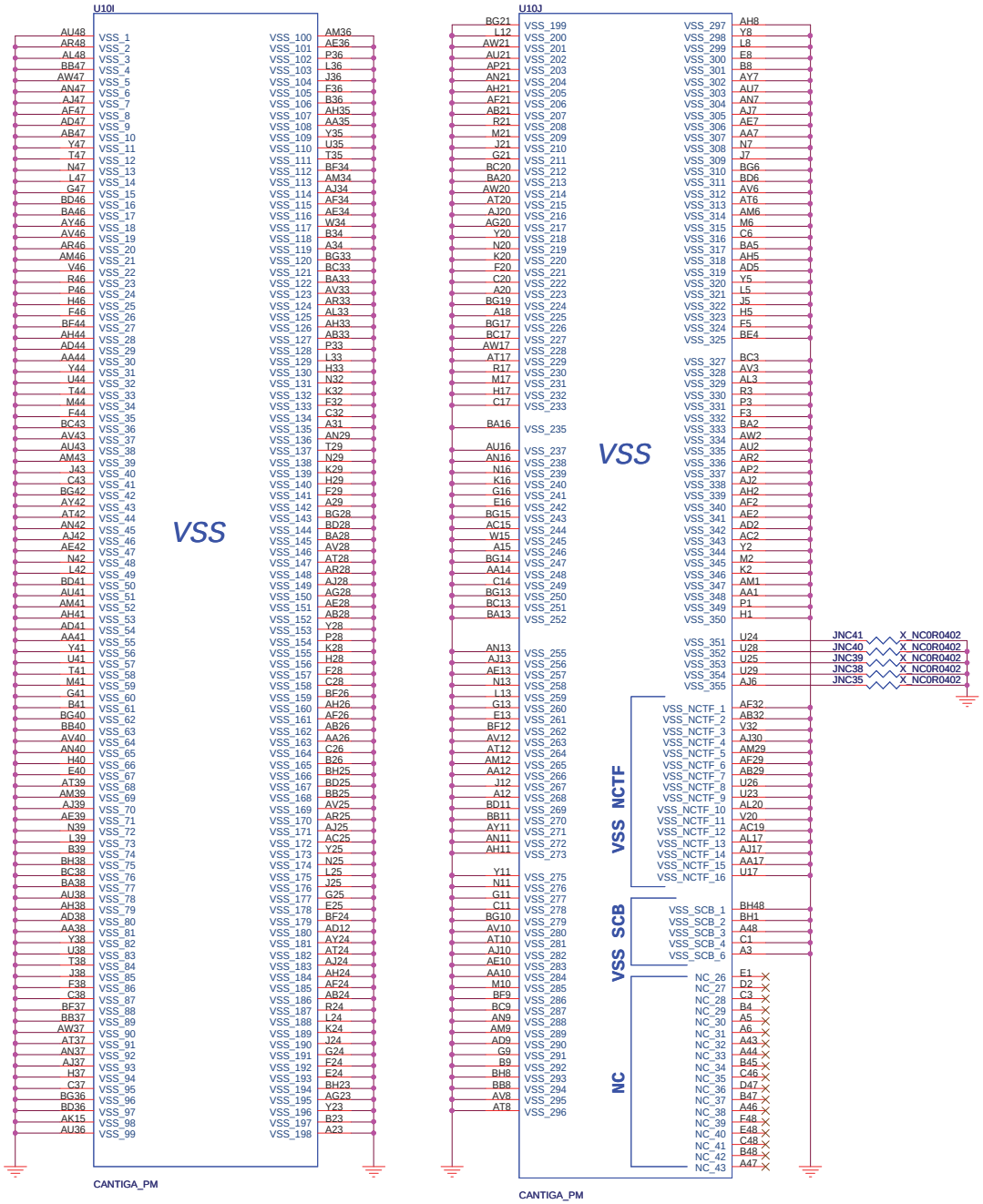
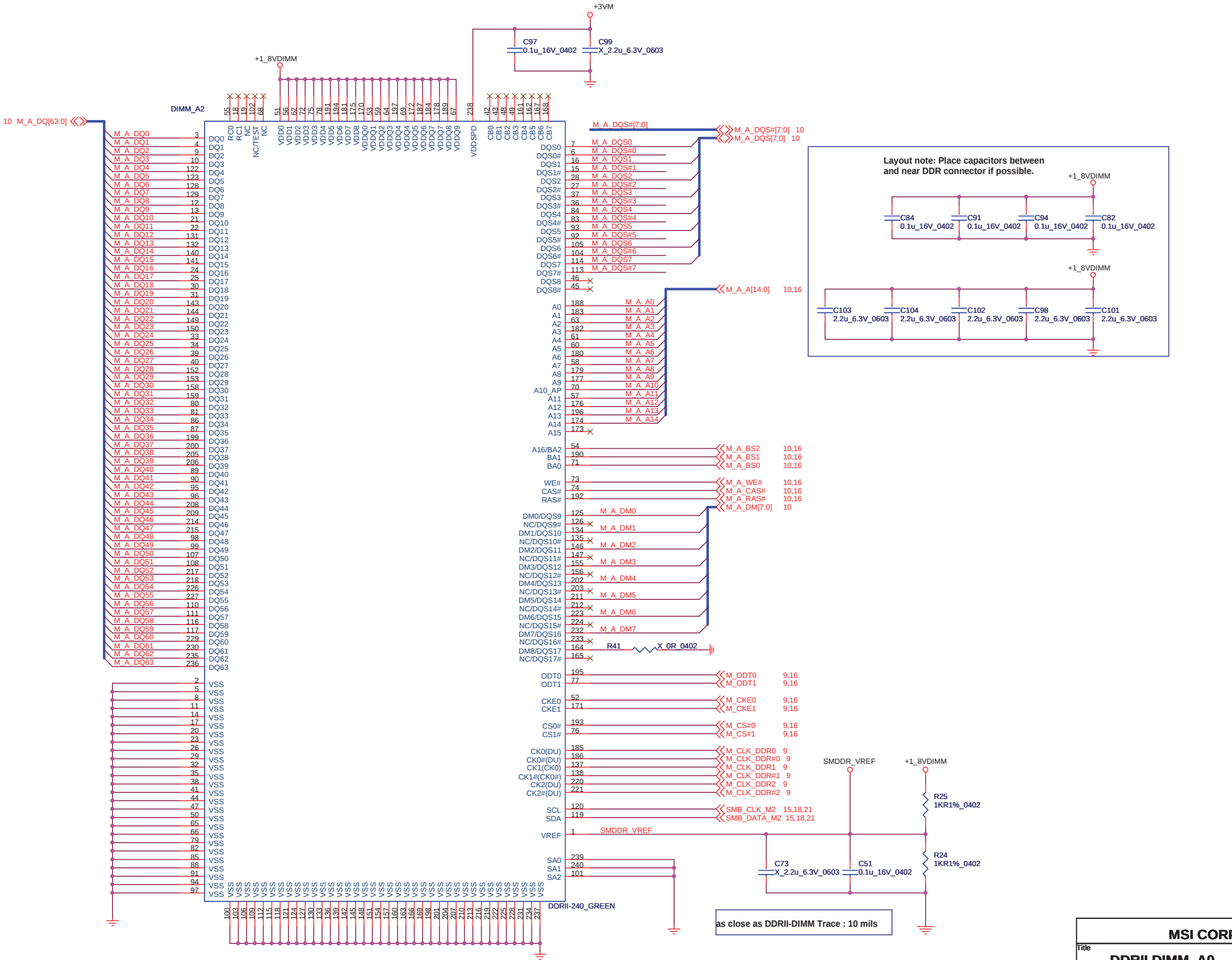


MSI CORPORATION

Title: CANTIGA-6 (VSS)

Size: Custom | Document Number: MS-96B9 | Rev: 1.1

Date: Monday, July 21, 2008 | Sheet 13 of 41



DDRII DIMM_1_CHA

Title	DDRII DIMM_A0
Size	Custom
Document Number	MS-96B9
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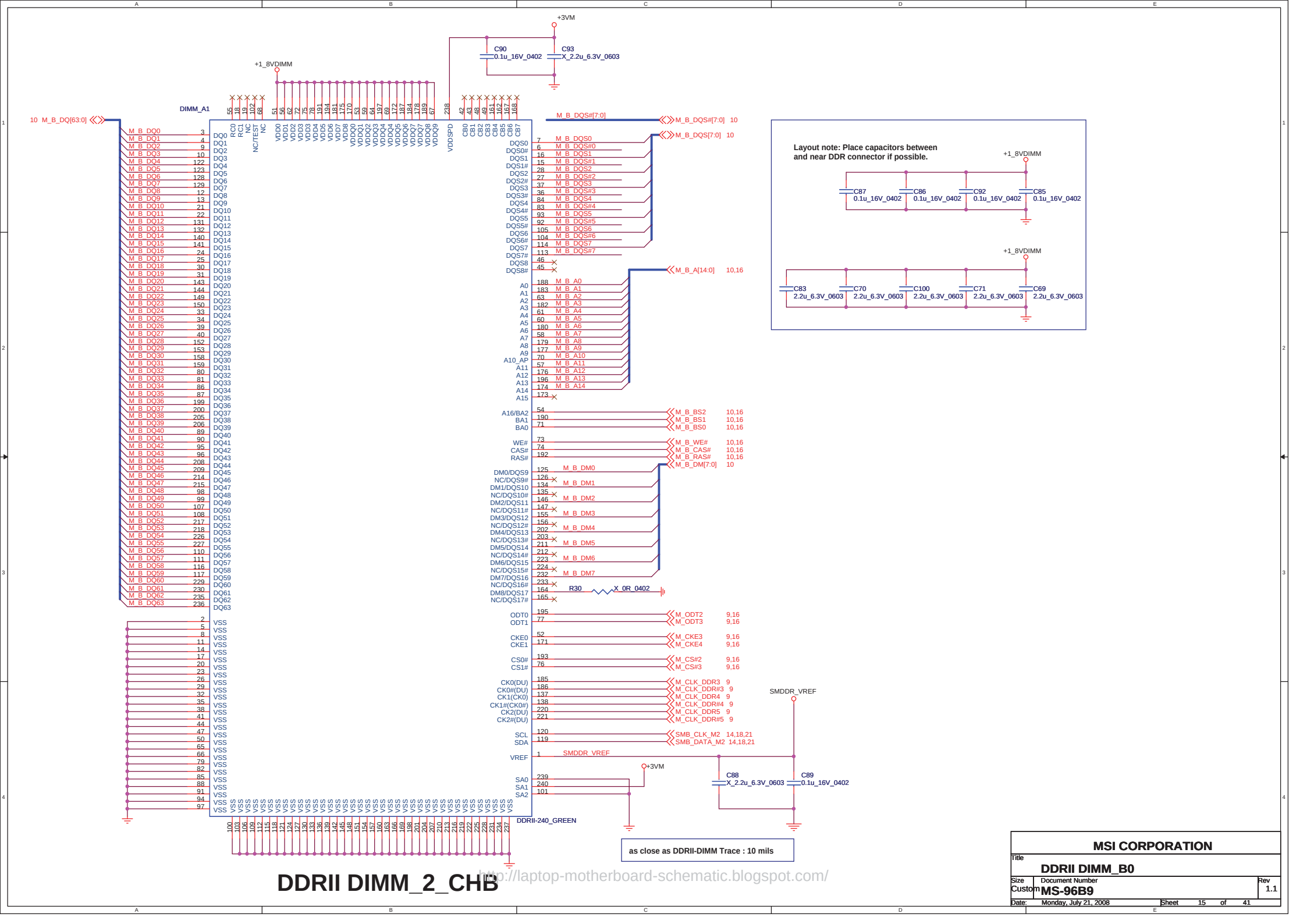
MSI CORPORATION



DDRII DIMM_2_CHB

Title	DDRII DIMM_B0
Size	Custom
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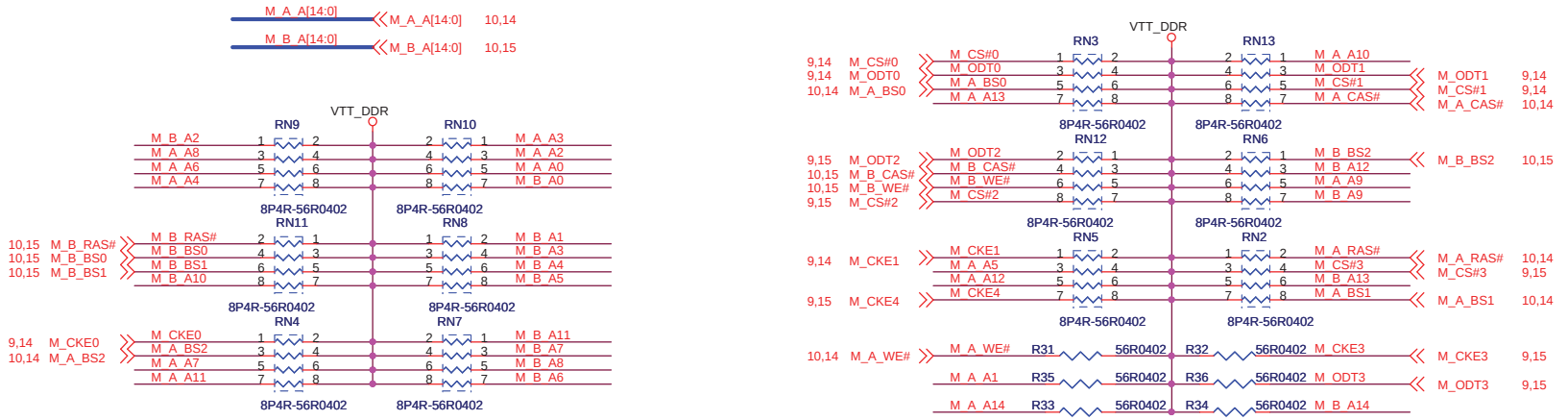
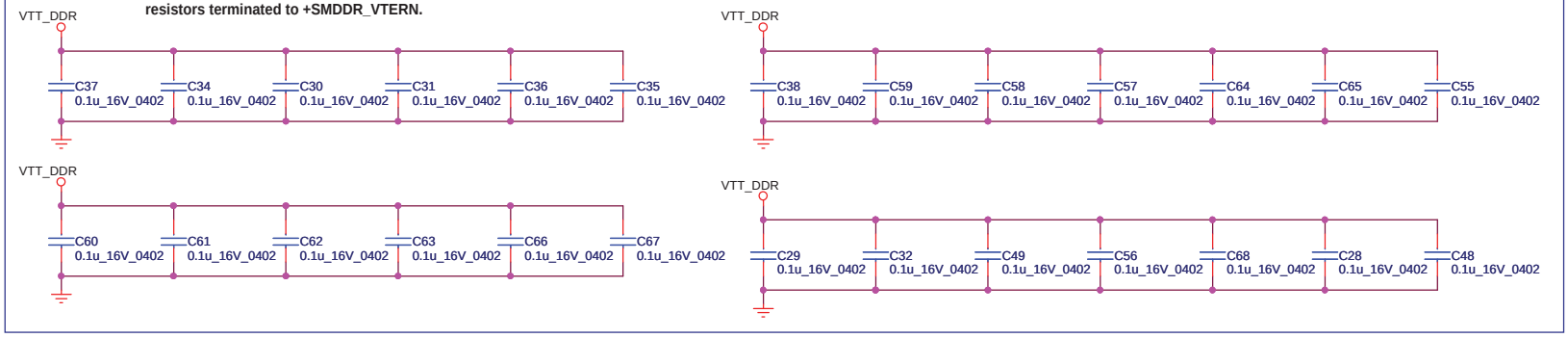
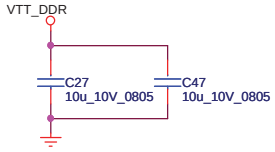
MSI CORPORATION



Layout note: Place one cap close to every 2 pullup resistors terminated to +SMDDR_VTERN.





MSI CORPORATION		
Title: DDRII TREMINATION		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
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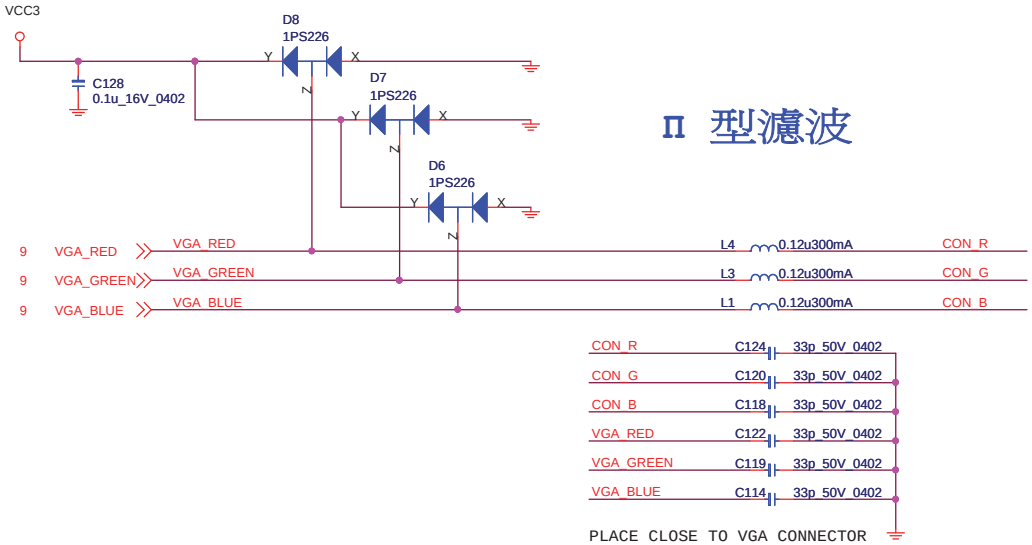
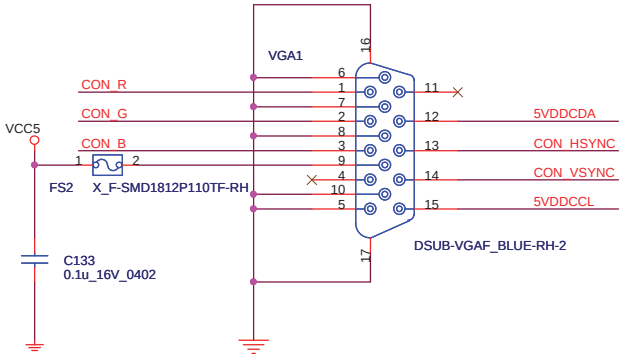
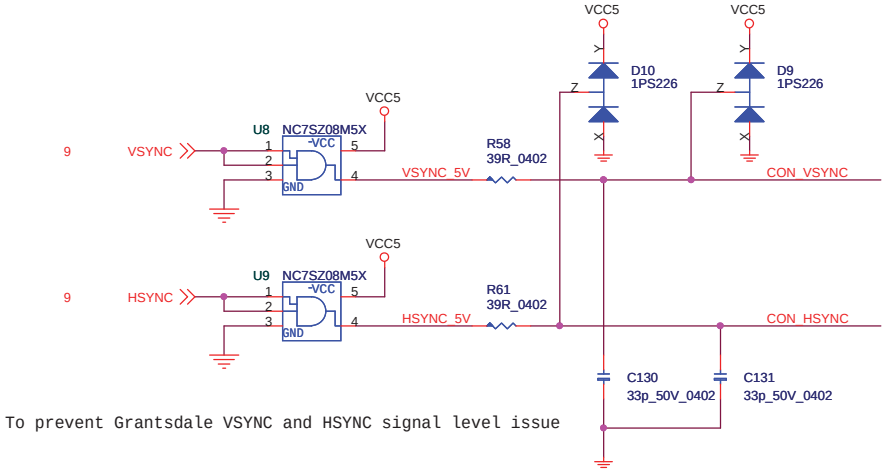
Video Connector



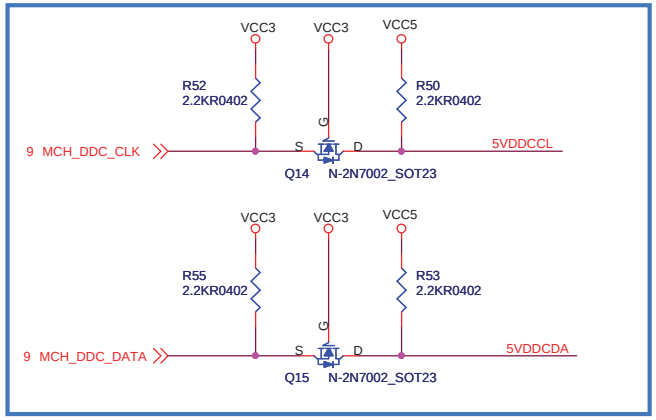
π 型濾波



USE 9628 homology COM New P/N:N51-15F0391-A10



To prevent Grantsdale VSYNC and HSYNC signal level issue



MSI CORPORATION		
Title: D-Sub 15Pin Video Connector		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
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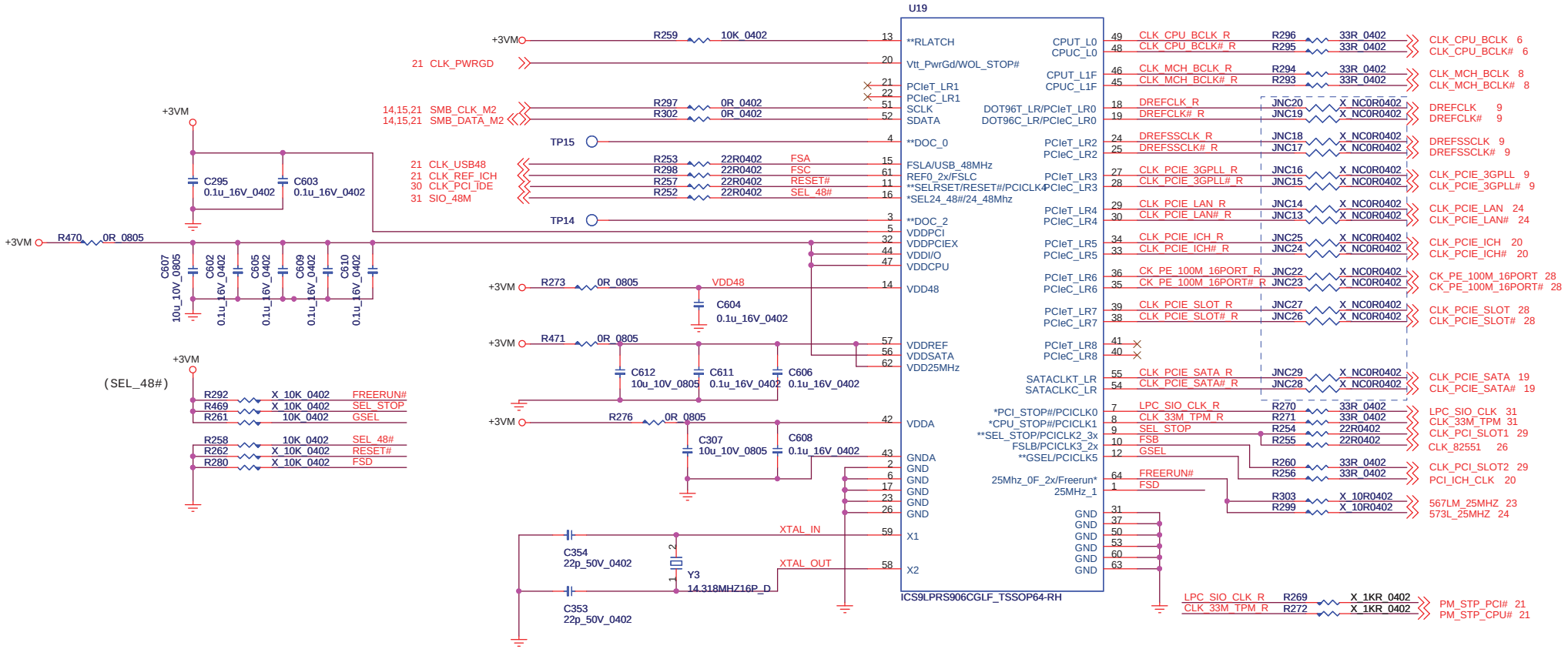

CPU Table			FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]	
L	H	H	667 MHz
L	H	L	800 MHz

MSI CORPORATION

Title: **CLOCK Generator (ICS9LPR906)**

Size	Document Number	Rev
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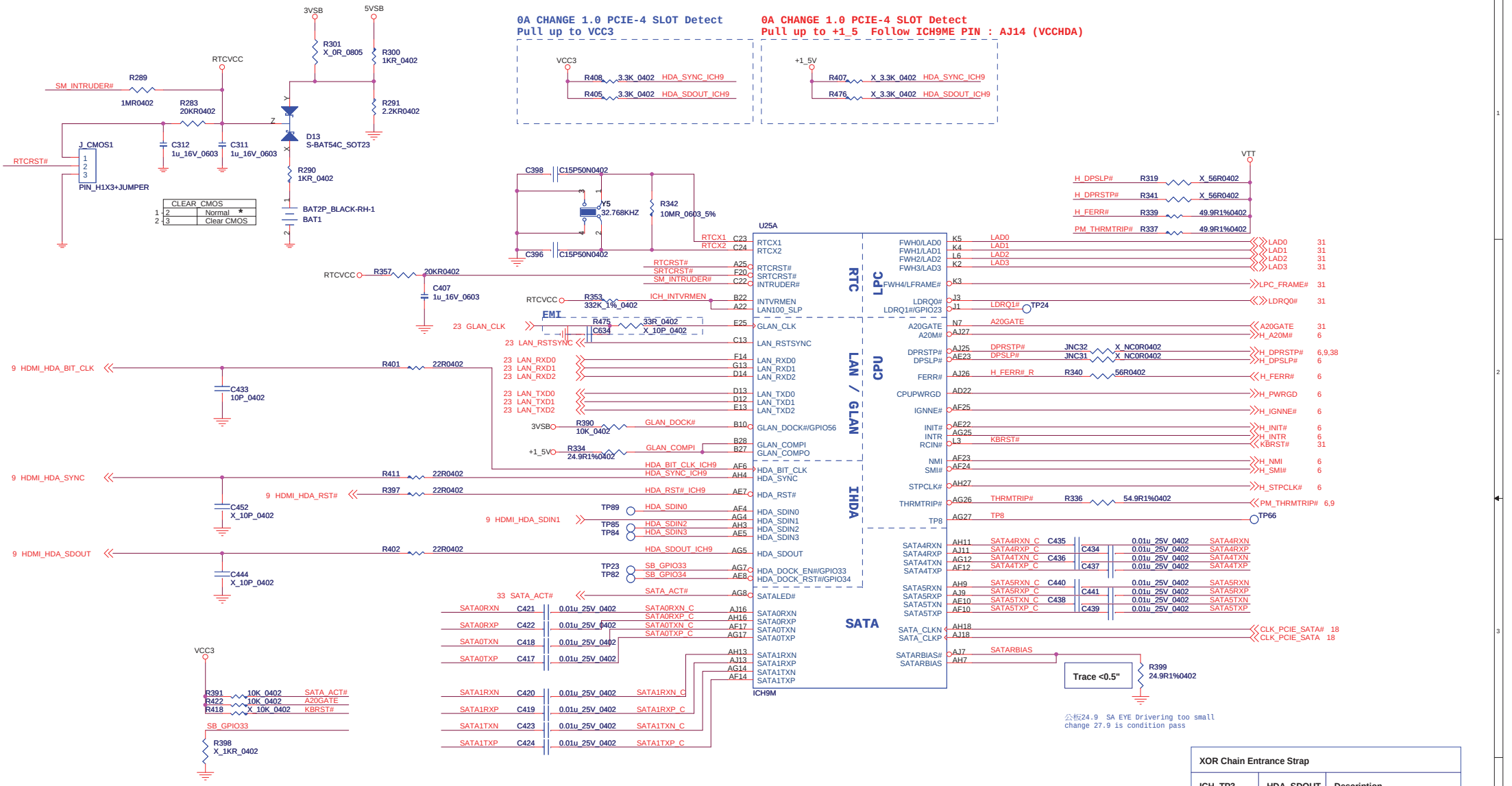

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(Default)
1	1	Set PCIE port config bit 1

MSI CORPORATION		
Title: ICH9ME-1 (CPU/IDE/Azalia)		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
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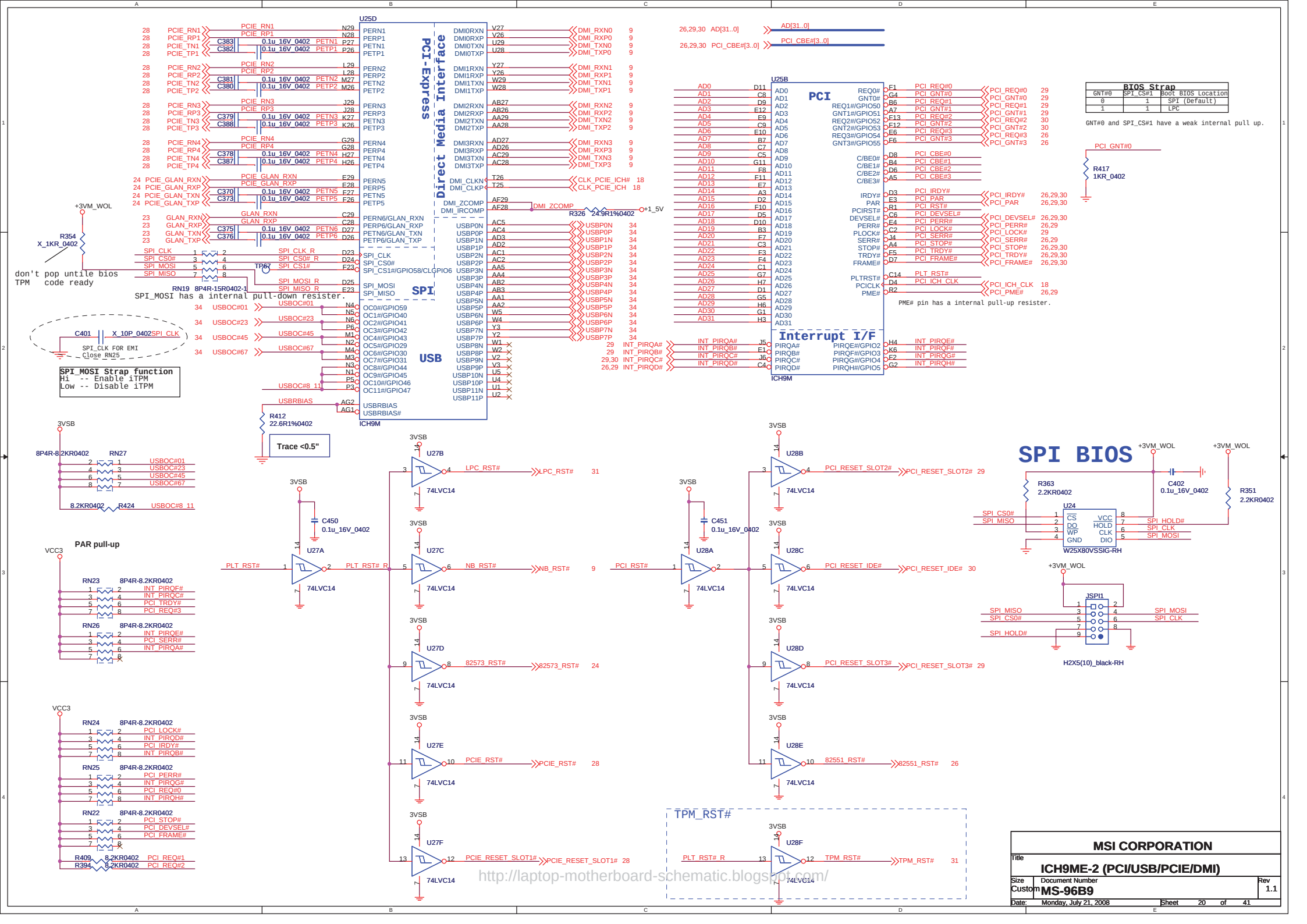
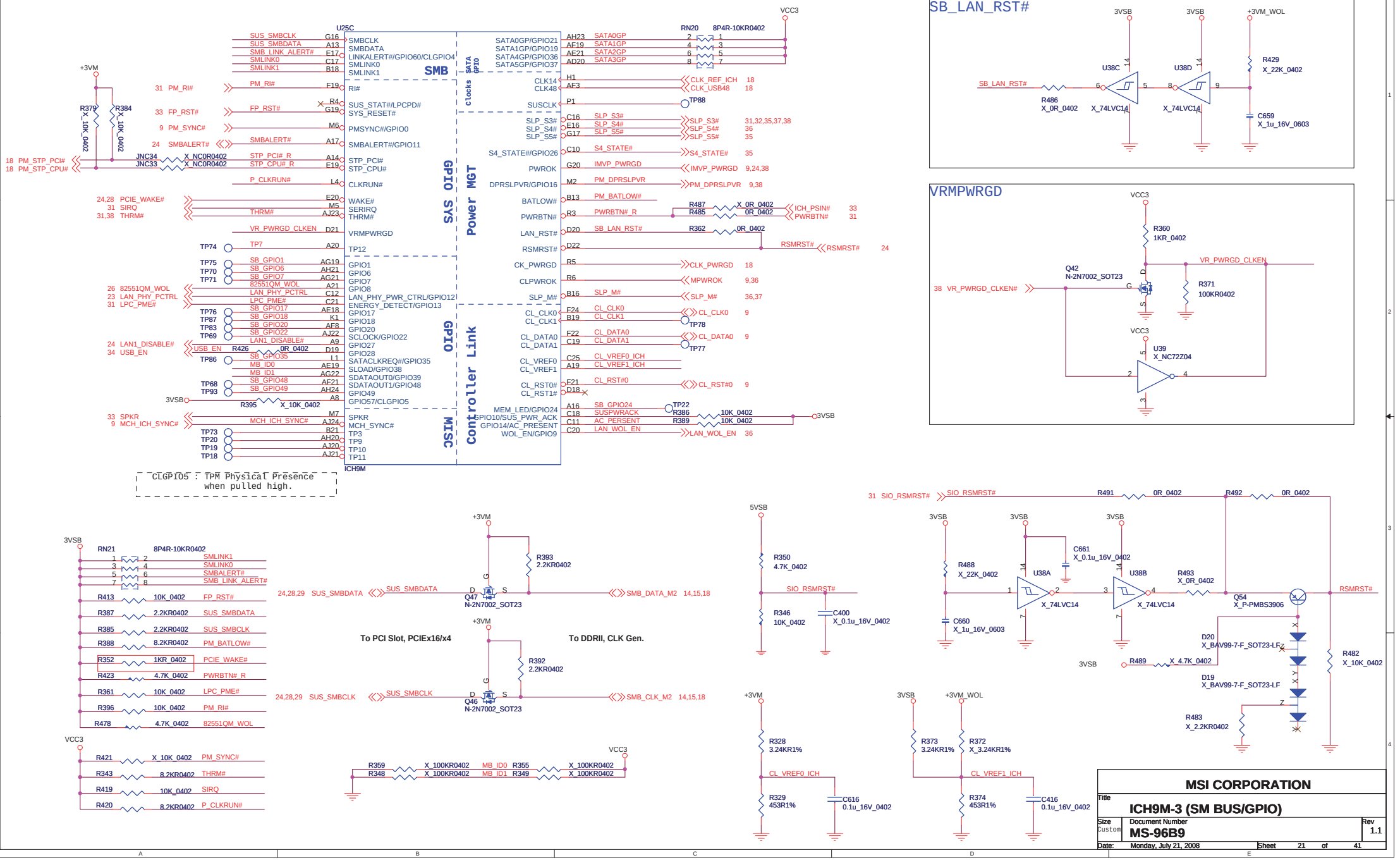
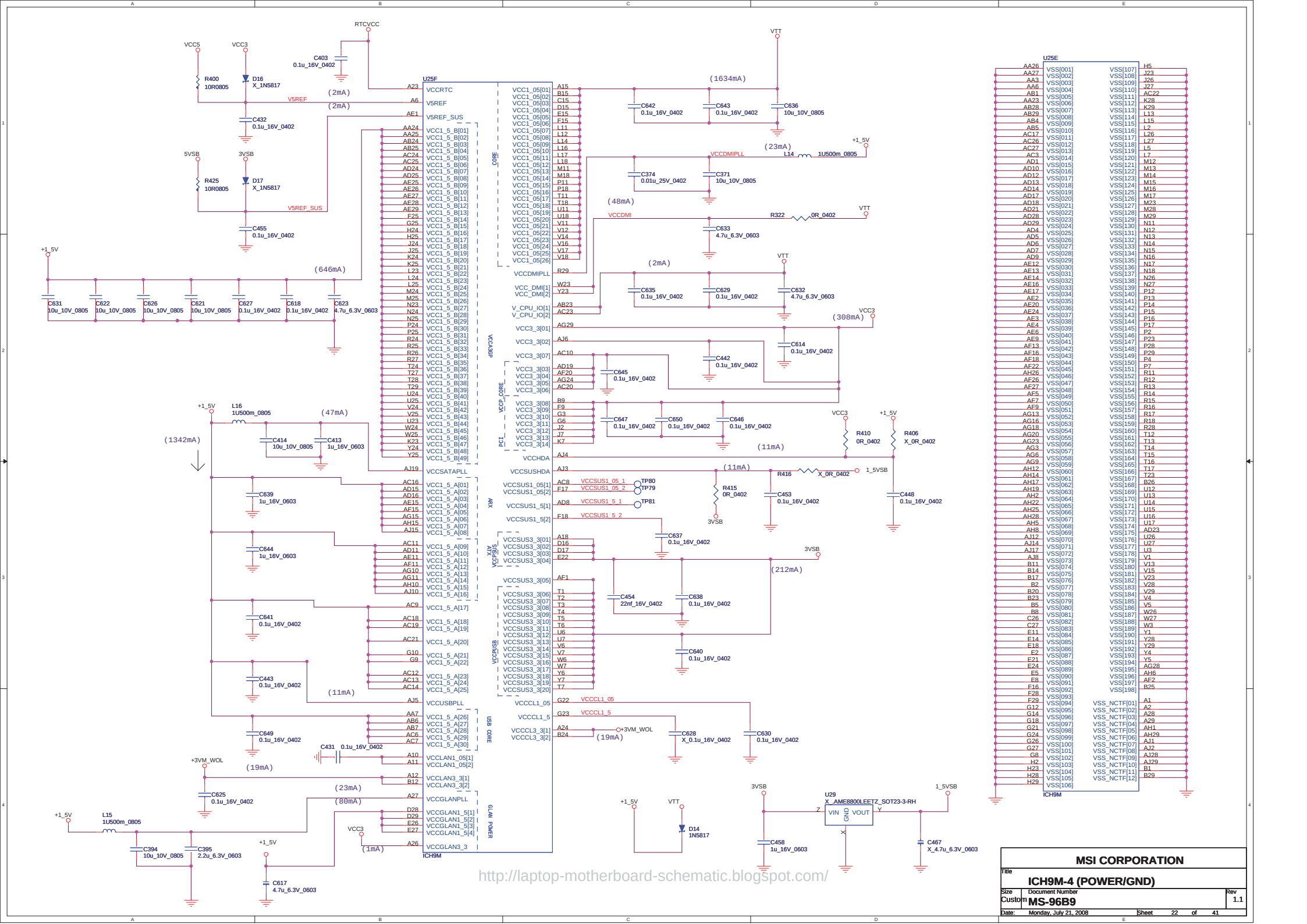

U25D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M
U25B
PCI
Interrupt I/F
ICH9M
BIOS Strap
GNT#0 SPI_CS#1 Boot BIOS Location
0 1 SPI (Default)
1 1 LPC
GNT#0 and SPI_CS#1 have a weak internal pull up.
PME# pin has a internal pull-up resister.
don't pop untile bios TPM code ready
SPI_MOSI has a internal pull-down resister.
SPI_MOSI Strap function
Hi -- Enable iTPM
Low -- Disable iTPM
Trace <0.5"
PAR pull-up
SPI BIOS
W25X80VSSIG-RH
H2X5(10)_black-RH
TPM_RST#
MSI CORPORATION
ICH9ME-2 (PCI/USB/PCIE/DMI)
MS-96B9
Monday, July 21, 2008
http://laptop-motherboard-schematic.blogspot.com/




U25F
U25E
ICH9M
VCCRTC
V5REF
V5REF_SUS
VCCSATAPLL
VCCUSBPLL
VCCLAN1_05[1]
VCCLAN1_05[2]
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN3_3
CORE
VCCA3P
VCCP_CORE
PCI
MEX
VCCP3SUS
ATX
VCCP1SUS
USB CORE
GLAN POWER
VCCDMIPLL
VCCDMI
VCCCL1_05
VCCCL1_5
VCCL3_3[1]
VCCL3_3[2]
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSUS3_3[01]
VCCSUS3_3[02]
VCCSUS3_3[03]
VCCSUS3_3[04]
VCCSUS3_3[05]
VCCSUS3_3[06]
VCCSUS3_3[07]
VCCSUS3_3[08]
VCCSUS3_3[09]
VCCSUS3_3[10]
VCCSUS3_3[11]
VCCSUS3_3[12]
VCCSUS3_3[13]
VCCSUS3_3[14]
VCCSUS3_3[15]
VCCSUS3_3[16]
VCCSUS3_3[17]
VCCSUS3_3[18]
VCCSUS3_3[19]
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VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCCHDA
VCC3_3[01]
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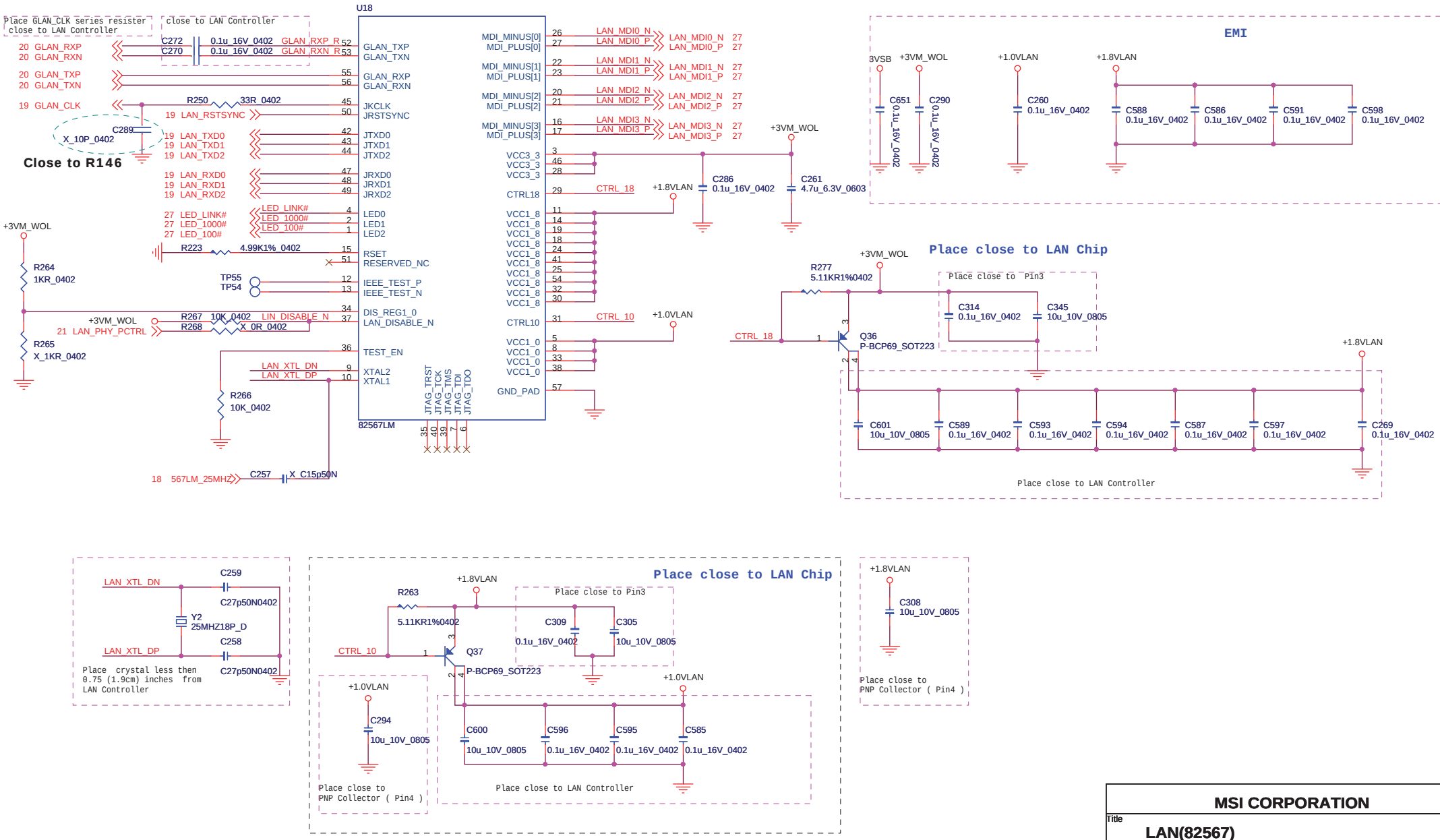
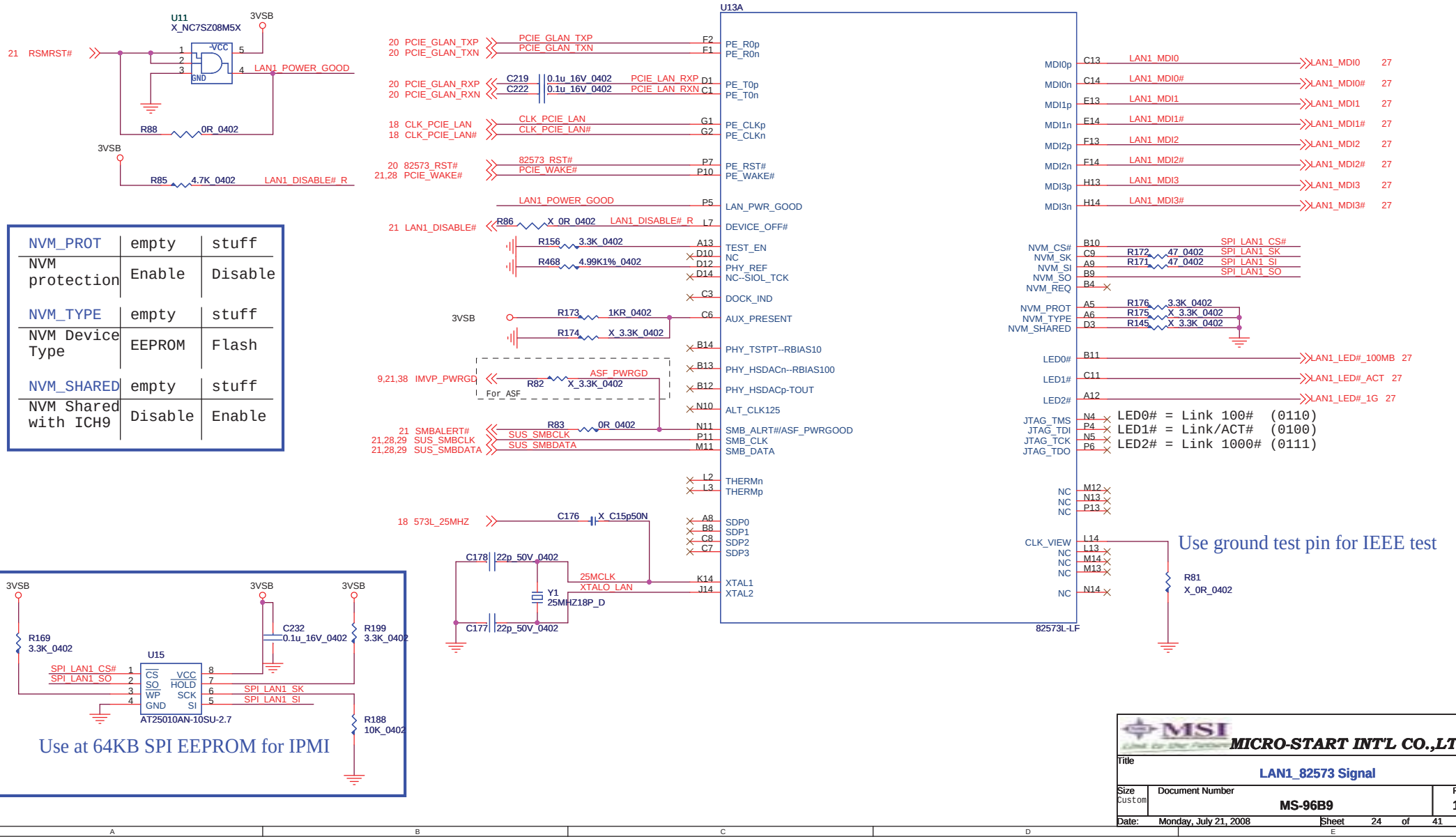
RTCVCC
VCC5
VCC3
5VSB
3VSB
VTT
+1_5V
1_5VSB
+3VM_WOL
R400 10R0805
D16 X_1N5817
R425 10R0805
D17 X_1N5817
C403 0.1u_16V_0402
C432 0.1u_16V_0402
C455 0.1u_16V_0402
C631 10u_10V_0805
C622 10u_10V_0805
C626 10u_10V_0805
C621 10u_10V_0805
C627 0.1u_16V_0402
C618 0.1u_16V_0402
C623 4.7u_6.3V_0603
L16 1U500m_0805
C414 10u_10V_0805
C413 1u_16V_0603
C639 1u_16V_0603
C644 1u_16V_0603
C641 0.1u_16V_0402
C443 0.1u_16V_0402
C649 0.1u_16V_0402
C431 0.1u_16V_0402
C625 0.1u_16V_0402
L15 1U500m_0805
C394 10u_10V_0805
C395 2.2u_6.3V_0603
C617 4.7u_6.3V_0603
C642 0.1u_16V_0402
C643 0.1u_16V_0402
C636 10u_10V_0805
C374 0.01u_25V_0402
C371 10u_10V_0805
L14 1U500m_0805
R322 0R_0402
C633 4.7u_6.3V_0603
C635 0.1u_16V_0402
C629 0.1u_16V_0402
C632 4.7u_6.3V_0603
C614 0.1u_16V_0402
C442 0.1u_16V_0402
C645 0.1u_16V_0402
C647 0.1u_16V_0402
C650 0.1u_16V_0402
C646 0.1u_16V_0402
R410 0R_0402
R406 X_0R_0402
R416 X_0R_0402
R415 0R_0402
C453 0.1u_16V_0402
C448 0.1u_16V_0402
C637 0.1u_16V_0402
C454 22nf_16V_0402
C638 0.1u_16V_0402
C640 0.1u_16V_0402
C628 X_0.1u_16V_0402
C630 0.1u_16V_0402
TP80
TP79
TP81
D14 1N5817
U29 X_AME8800LEETZ_SOT23-3-RH
C458 1u_16V_0603
C467 X_4.7u_6.3V_0603
(1634mA)
(23mA)
(48mA)
(2mA)
(308mA)
(11mA)
(212mA)
(646mA)
(1342mA)
(47mA)
(19mA)
(80mA)
(1mA)
MSI CORPORATION
ICH9M-4 (POWER/GND)
MS-96B9
Custom
1.1
Monday, July 21, 2008
Sheet 22 of 41
http://laptop-motherboard-schematic.blogspot.com/



Title	LAN(82567)
Size	
Document Number	MS-96B9
Rev	1.1
Date:	Monday, July 21, 2008
Sheet	23 of 41

MSI CORPORATION



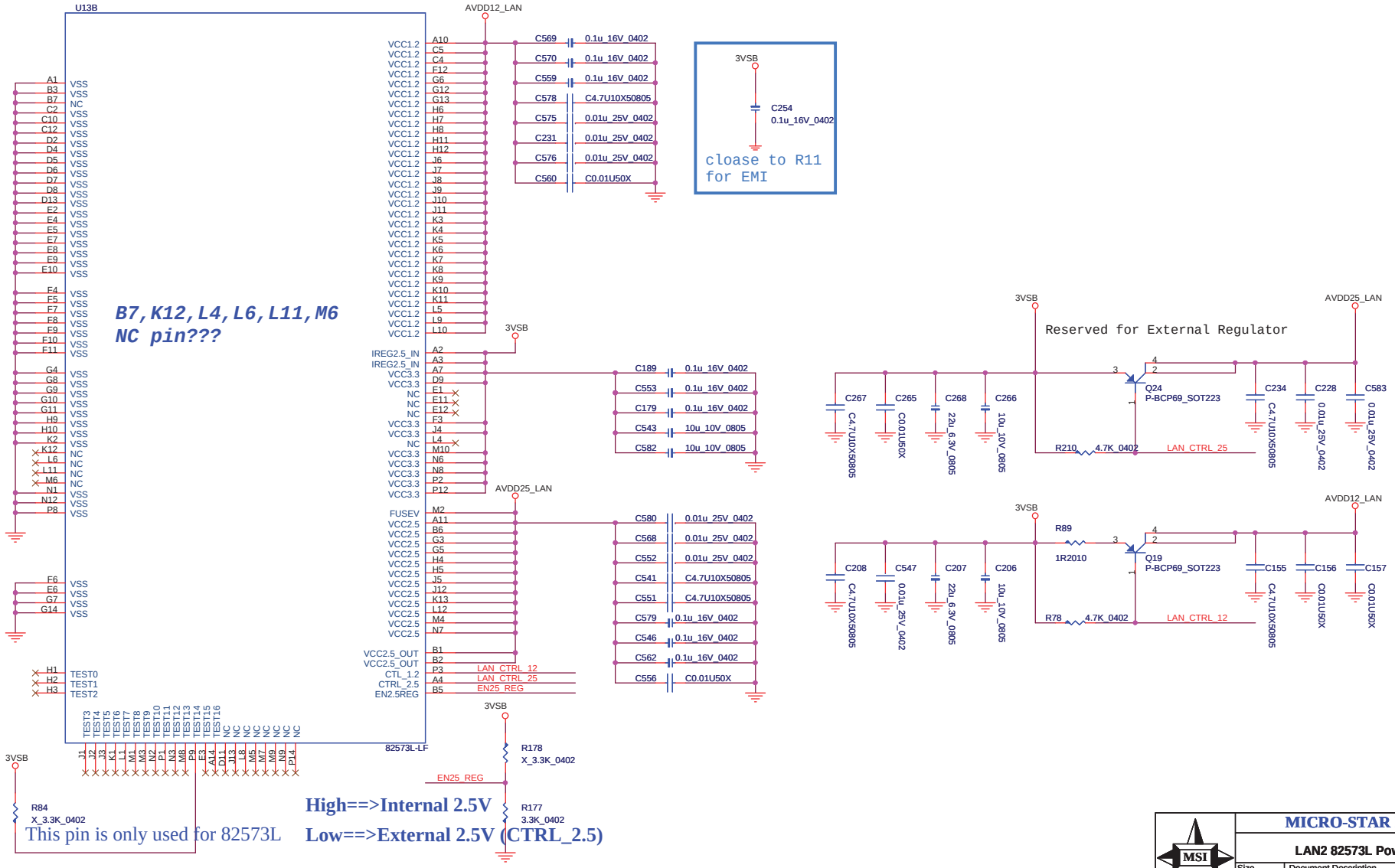
NVM_PROT	empty	stuff
NVM protection	Enable	Disable
NVM_TYPE	empty	stuff
NVM Device Type	EEPROM	Flash
NVM_SHARED	empty	stuff
NVM Shared with ICH9	Disable	Enable

MICRO-START INT'L CO.,LTD.

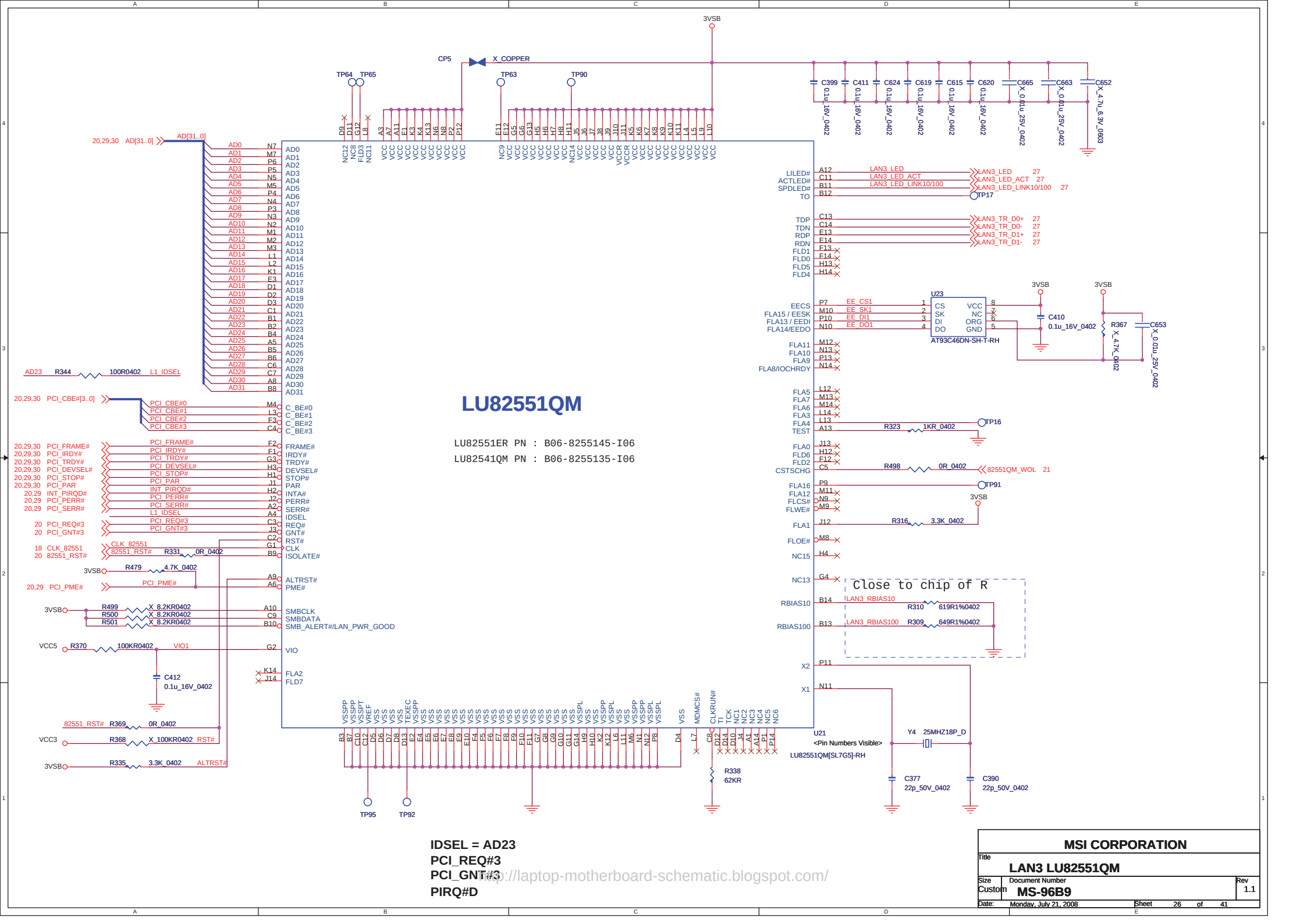
Title: LAN1_82573 Signal

Size: Custom | Document Number: MS-96B9 | Rev: 1.1

Date: Monday, July 21, 2008 | Sheet 24 of 41



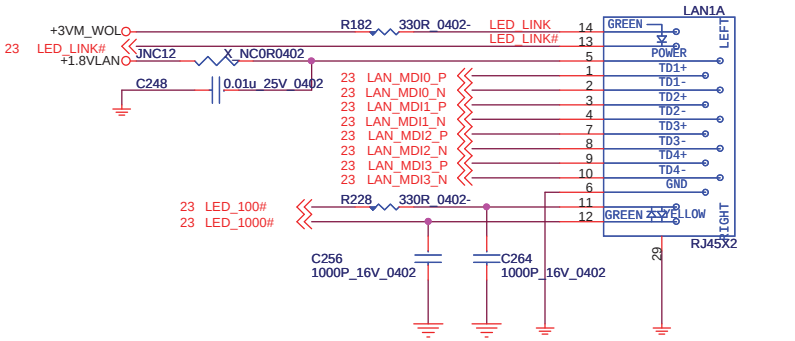
MICRO-STAR INT'L CO.,LTD	
LAN2 82573L Power	
Size: Custom	Document Description: MS-96B9
Rev: 1.1	
Date: Monday, July 21, 2008	Sheet 25 of 41

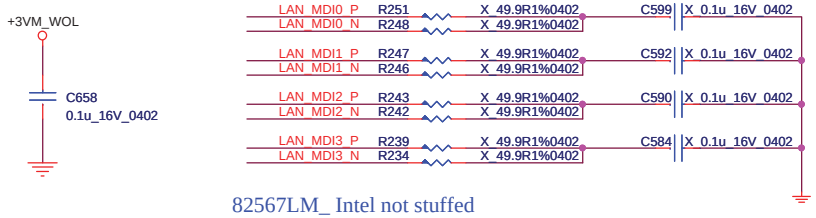


MSI CORPORATION		
Title: LAN3 LU82551QM		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
Date: Monday, July 21, 2008	Sheet 26 of 41	

LAN1&2 82567&82573 GIGA LAN

23 LAN1 82567LM

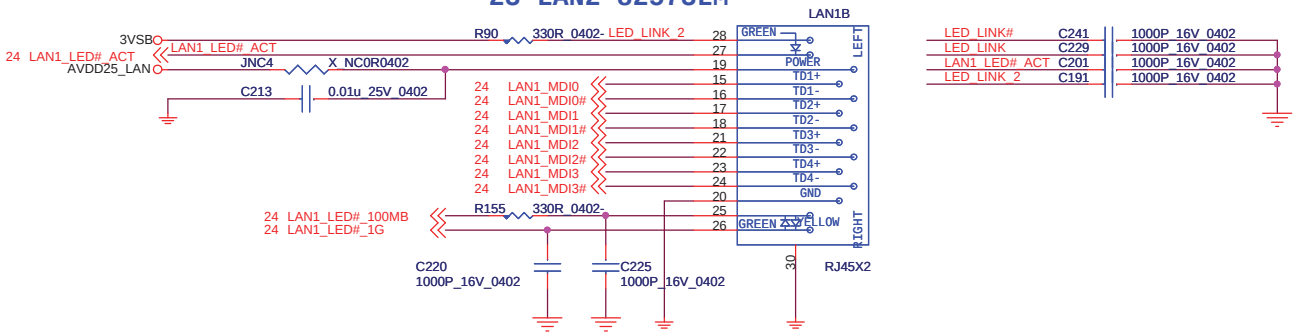


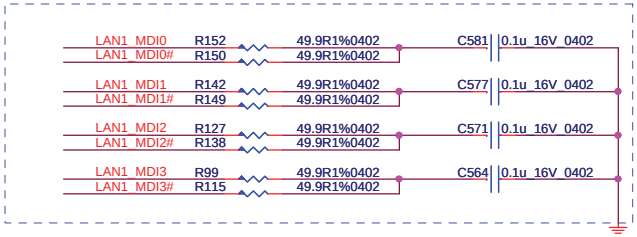


82567LM_ Intel not stuffed

Place these components near 82567LM (LAN CHIPSET) forEMI

23 LAN2 82573LM

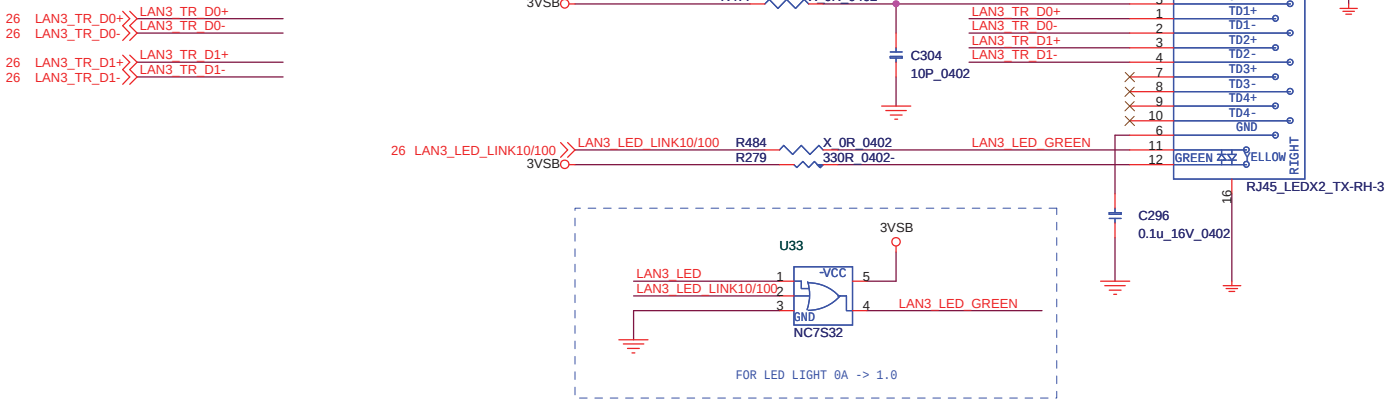


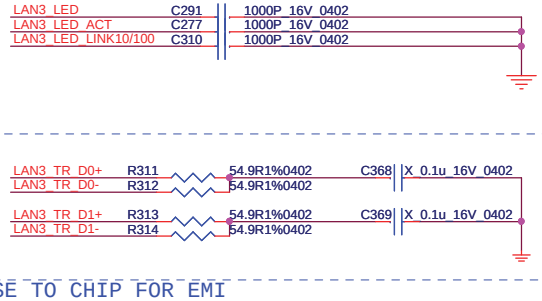


Place these components near 82573L(LAN CHIPSET) for EMI

LAN3 82551QM 10/100M

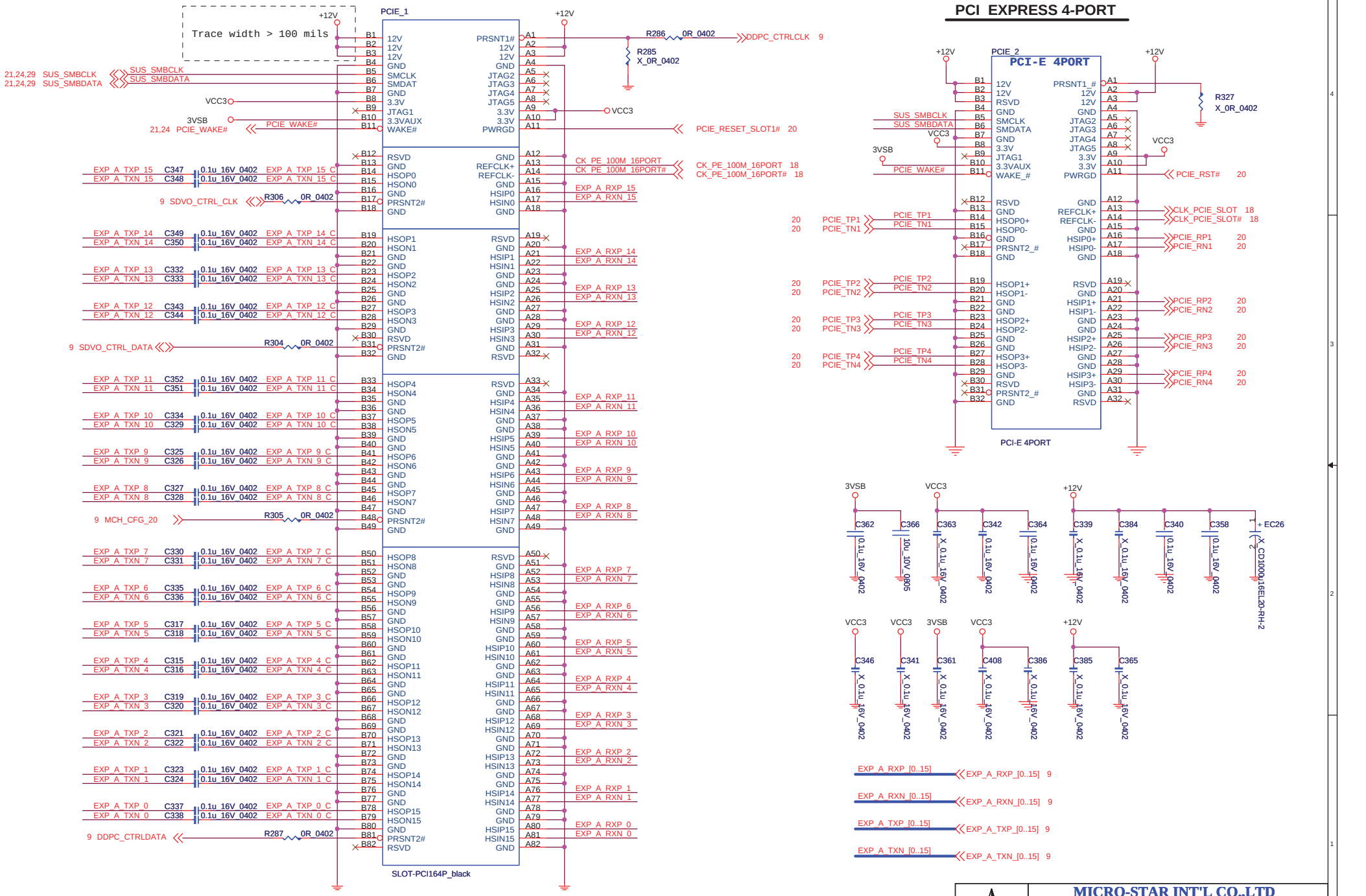
26 LAN3 LU82551QM



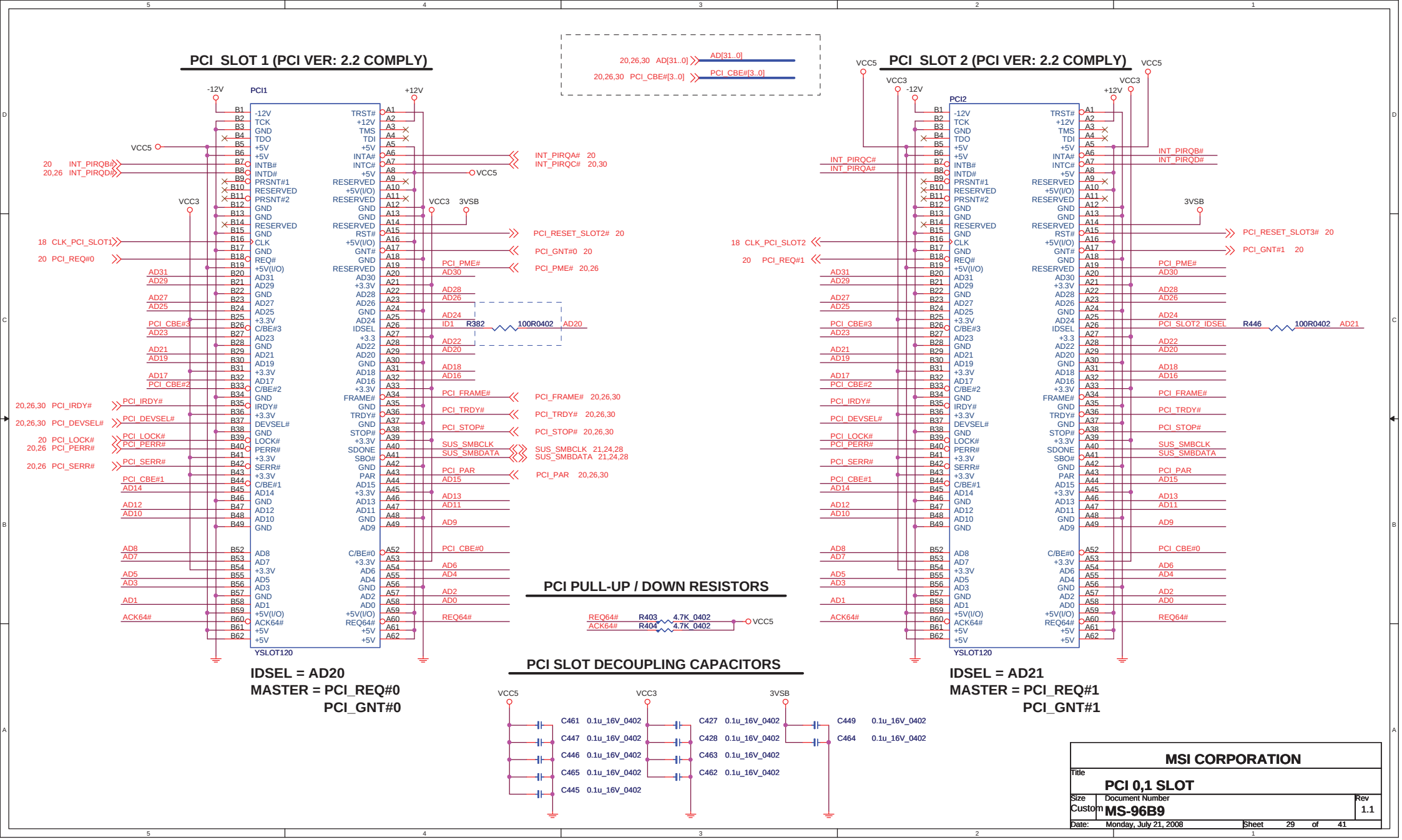


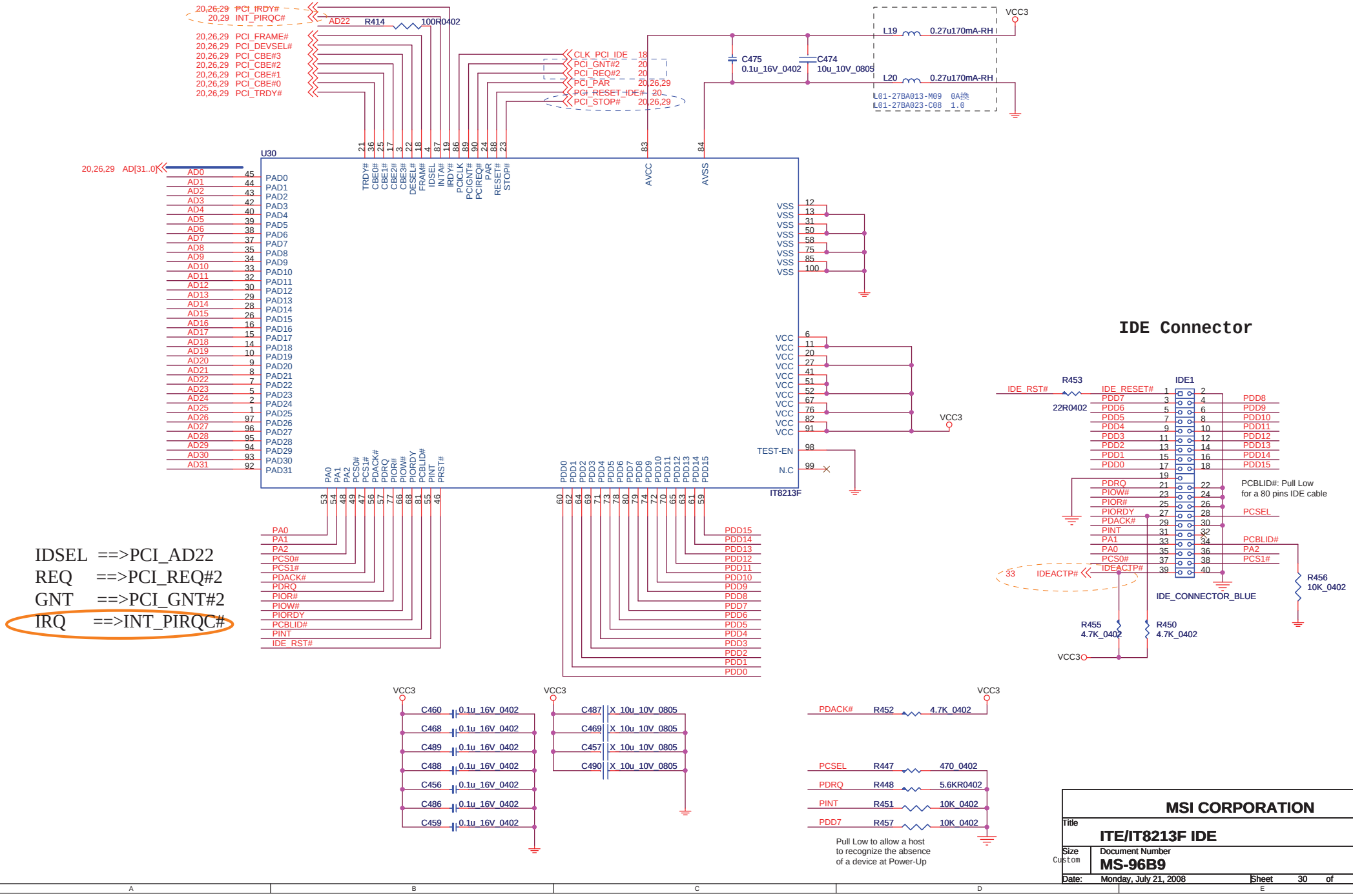
CLOSE TO CHIP FOR EMI

MSI CORPORATION		
Title: LAN CONN		
Size: B	Document Number: MS-96B9	Rev: 1.1
Date: Monday, July 21, 2008	Sheet 27 of 41	



MICRO-STAR INT'L CO.,LTD		
PCI -Express X 16/4 Port		
Size: Custom	Document Description: MS-96B9	Rev: 1.1
Date: Monday, July 21, 2008	Sheet 28 of 41	





INDEX# must be pulled up to 5V oly for A version chip

U22

W83627DHG-RH-1

AUX CHANGE SYSTIN 1.0->1.1 FOR SMART FAN

reserve for 657XHG

BIOS should set to GPO function

Winbond APnote

PS2 KEYBOARD & MOUSE CONNECTOR

F-SMD1812P110TF-RH

JKBMSI MINIDINX2-12P

TPM

JTPM1

H2X7[10]M-2PITCH

CN1 8P4C-220P

CN2 8P4C-220P

COM

COM1

FOR EMI

GD75232_SSOP20

USE 96A8 COM New P/N:N51-09M0091-F02
產線引腳PIN周邊塑材出現輕微熔膠現象
CHANGE TO N51-09M0091-K06
CHANGE TO N51-09M0211-F02

LPC I/O STRAPPING RESISTOR

RTSA#	L: CFAD=2E	H: CFAD=4E
GP50	L: TTL LEVEL	H: GTL LEVEL
SOUTA	L: KBC DISABLE	H: KBC ENABLE
DTRA#	L: DISABLE SPI	H: ENABLE SPI
FAN_SET	L: CPU1 PWM50%	H: CPU1 PWM100%

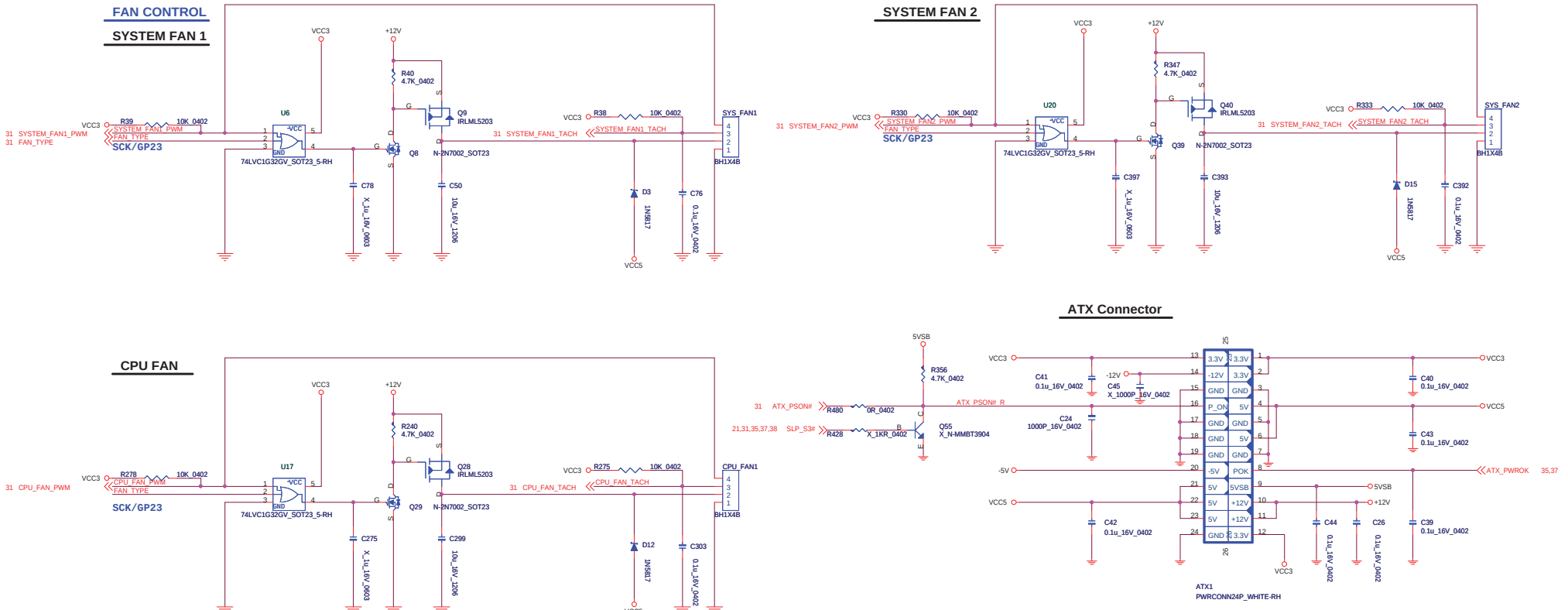
Hardware Monitor

smart fan 1.0->1.1

不上件 電流MODEL
上件 電壓MODEL

TO CPU 1.0->1.1

MSI CORPORATION	
Title	SIO W83627DHG
Size: Custom	Document Number: MS-96B9
Rev	1.1
Date: Wednesday, July 23, 2008	Sheet 31 of 41



MSI CORPORATION		
Title: FAN,ATX		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
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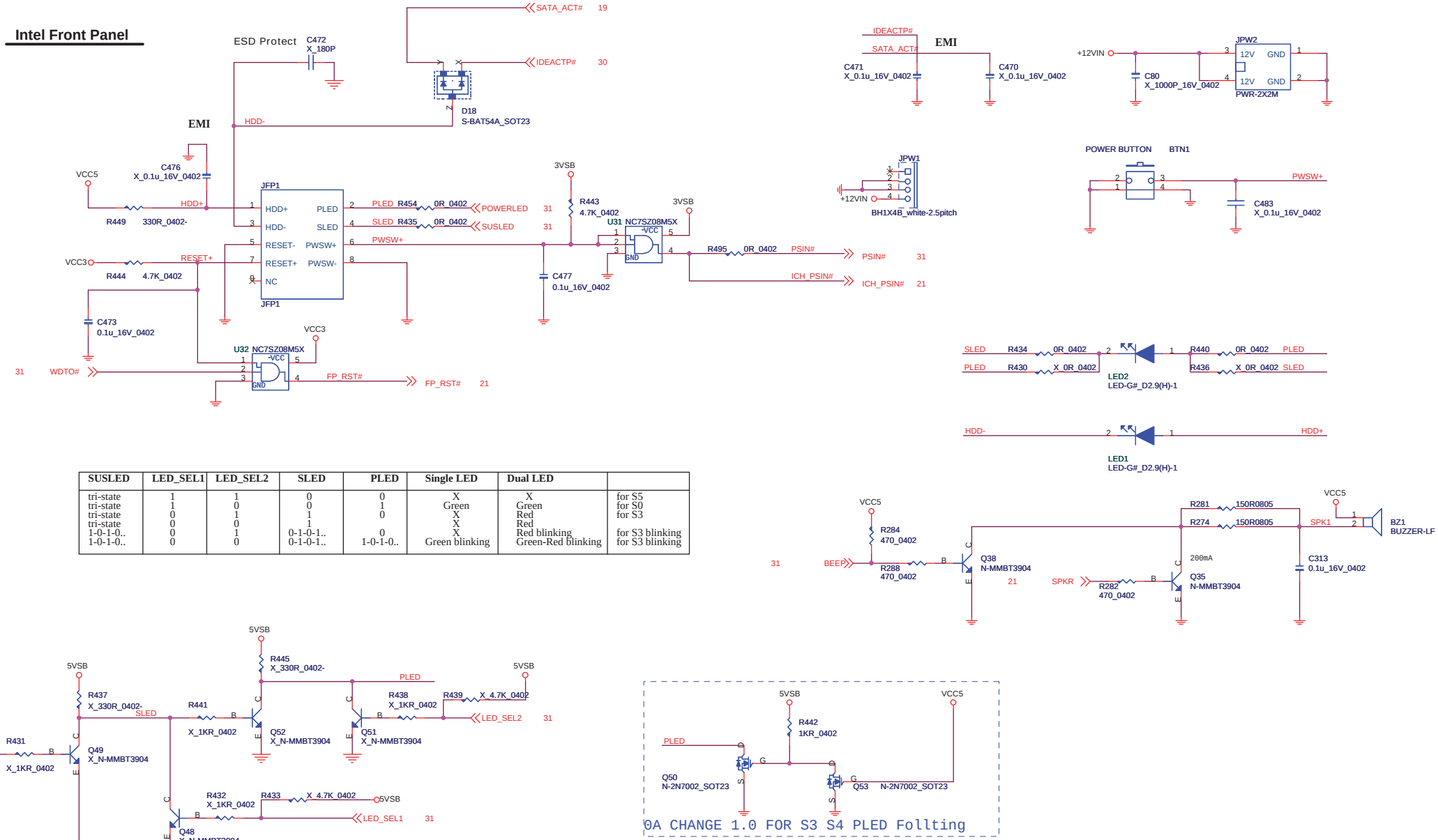
Intel Front Panel



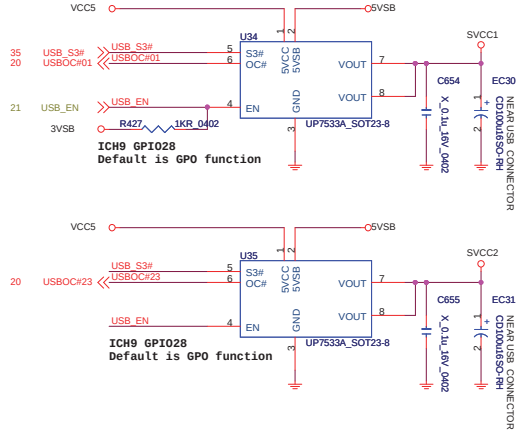
SUSLED	LED_SEL1	LED_SEL2	SLED	PLED	Single LED	Dual LED	
tri-state	1	1	0	0	X	X	for S5
tri-state	1	0	0	1	Green	Green	for S0
tri-state	0	1	1	0	X	Red	for S3
tri-state	0	0	1		X	Red	
1-0-1-0..	0	1	0-1-0-1..	0	X	Red blinking	for S3 blinking
1-0-1-0..	0	0	0-1-0-1..	1-0-1-0..	Green blinking	Green-Red blinking	for S3 blinking

MSI CORPORATION

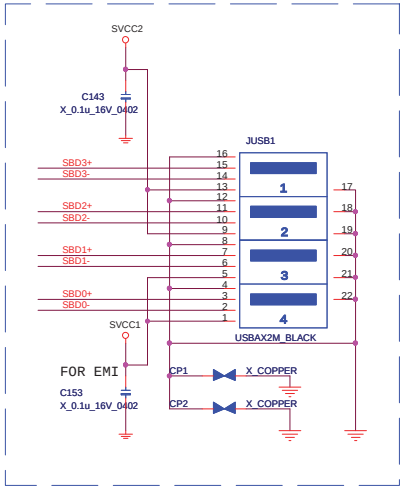
Title: Front Panel

Size: Custom | Document Number: MS-96B9 | Rev: 1.1

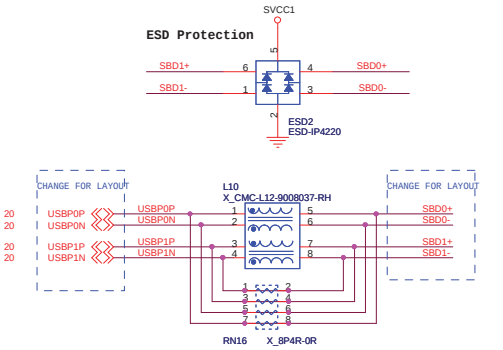
Date: Monday, July 21, 2008 | Sheet 33 of 41

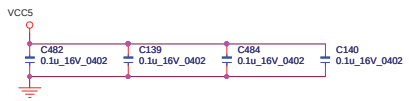


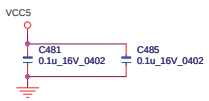
Change to USB x 2 ports for system
2 Port New PN: N53-08M0141-F02
4 Port New PN: N53-16M0041-A10



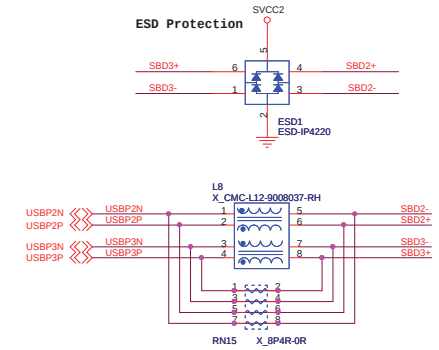
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

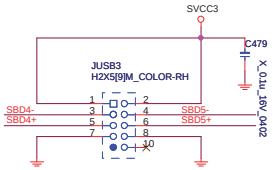




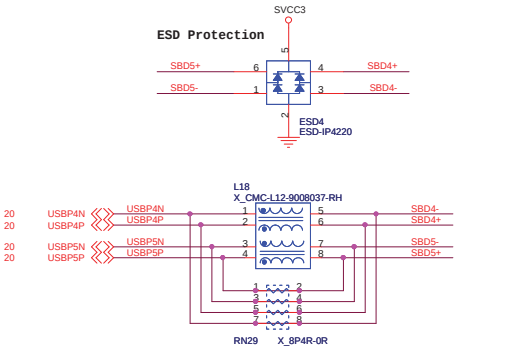


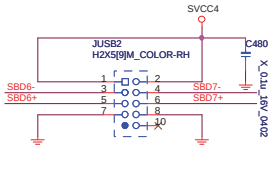
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



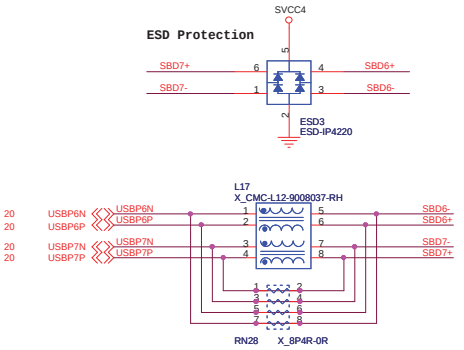


FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

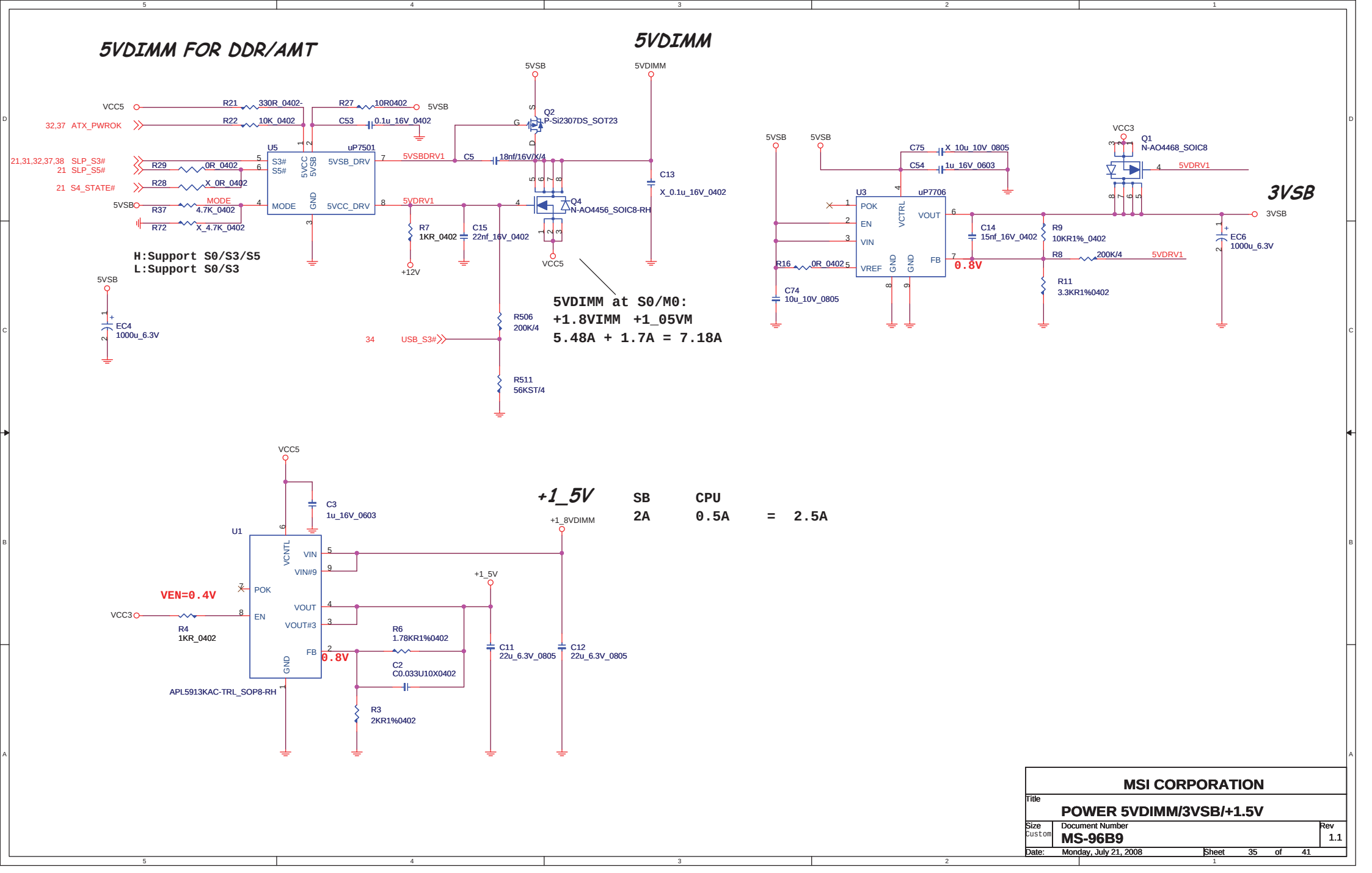




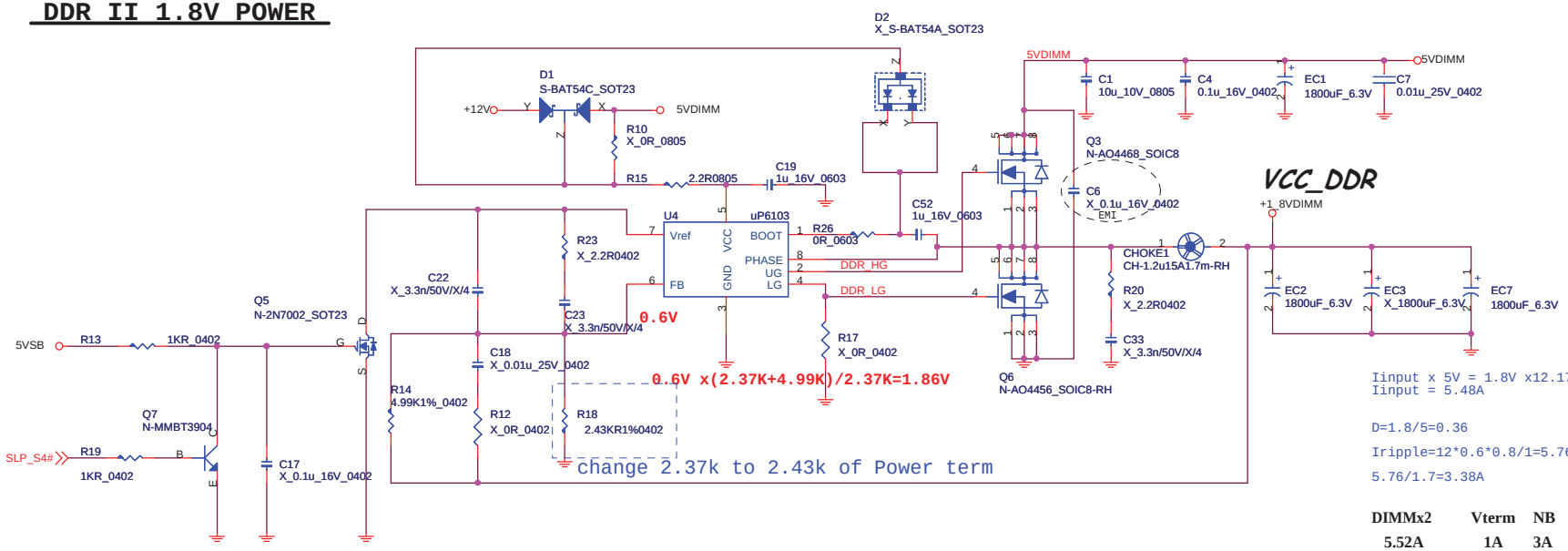
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



MSI CORPORATION		
Title: USB		
Size: Custom	Document Number: MS-96B9	Rev: 1.1
Date: Tuesday, July 22, 2008	Sheet 34 of 41	



DDR II 1.8V POWER



Iinput x 5V = 1.8V x12.17A /0.8
Iinput = 5.48A

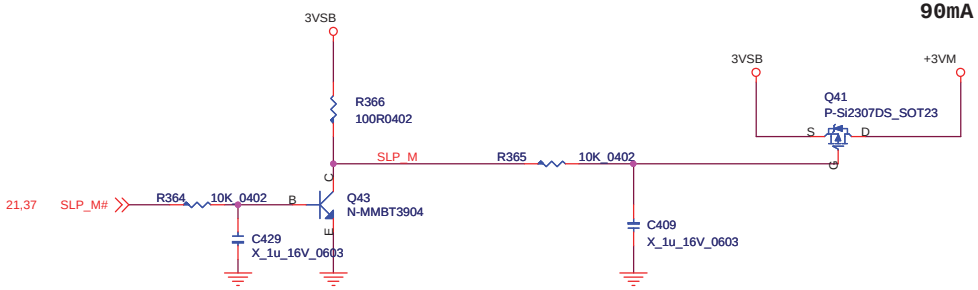
D=1.8/5=0.36

Iripple=12*0.6*0.8/1=5.76A

5.76/1.7=3.38A

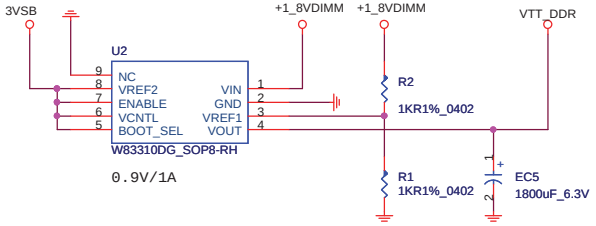
DIMMx2	Vterm	NB	+1_5VRUN		
5.52A	1A	3A	2.65A	=	12.17A

+3VM
90mA at AMT mode



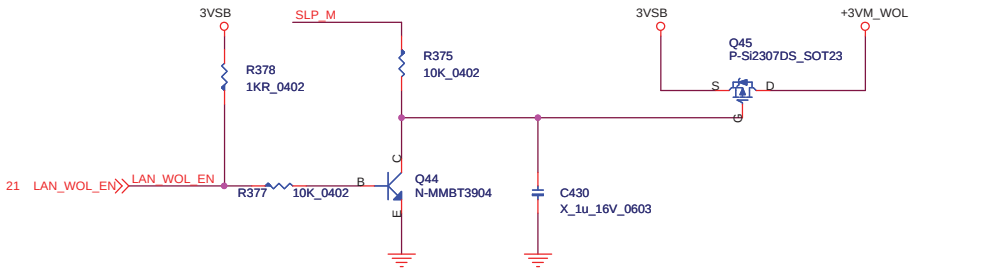
DDR VTT Power

VTT_DDR

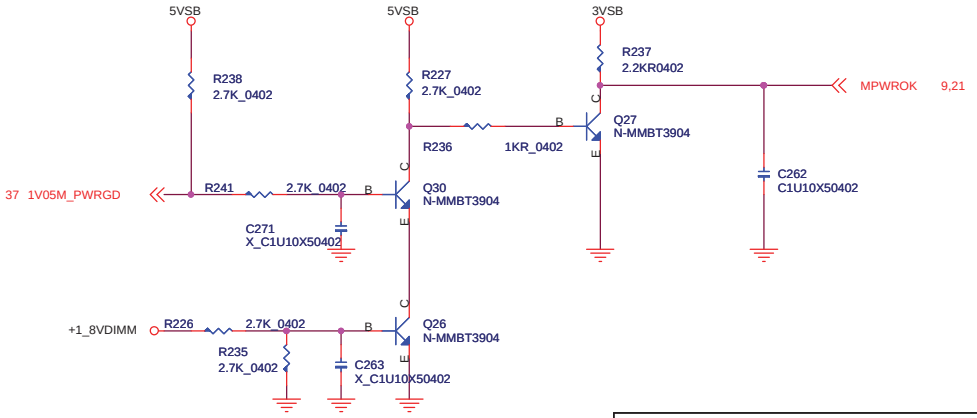


+3VM_WOL for ICH9
150mA at S3/S4/S5

+3VM_WOL

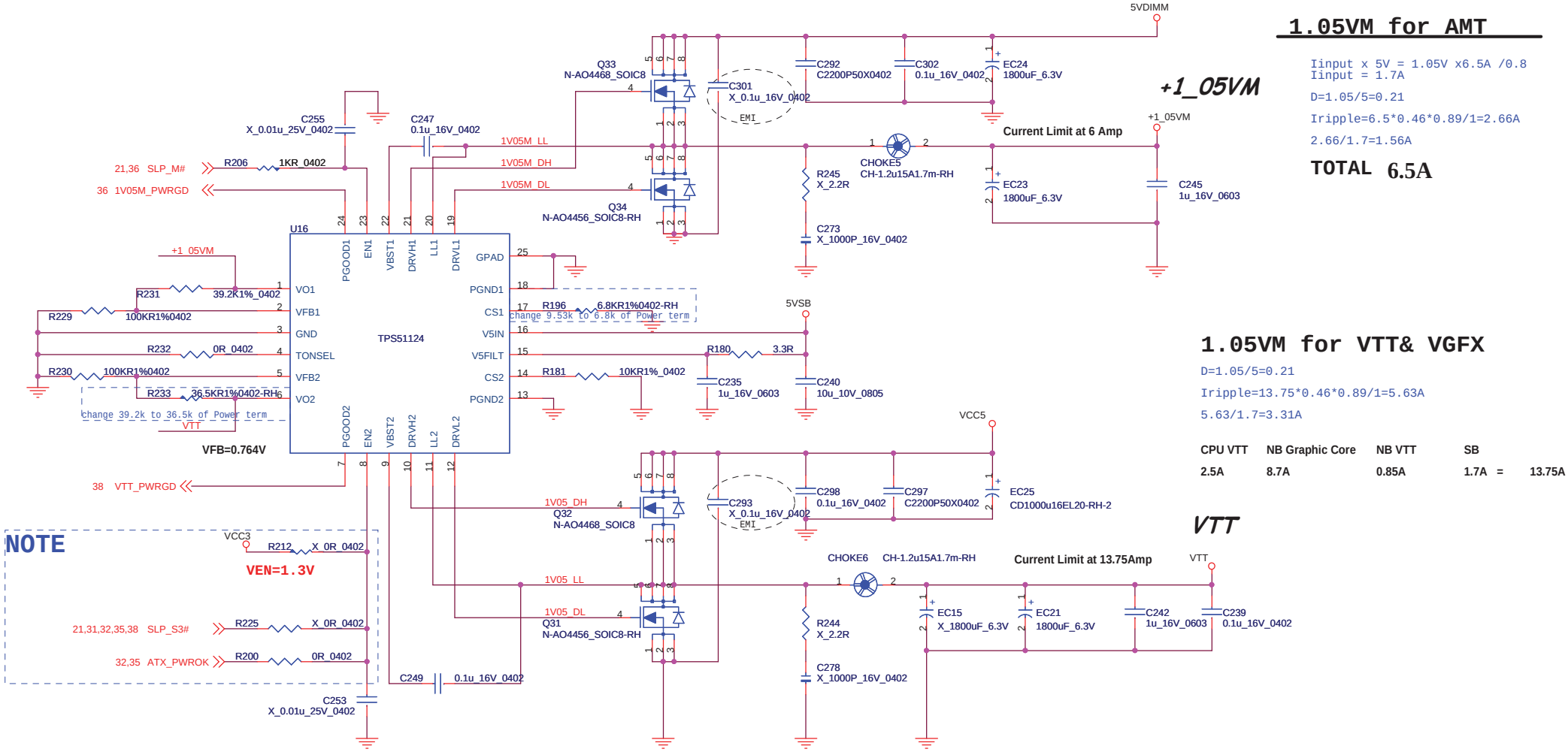


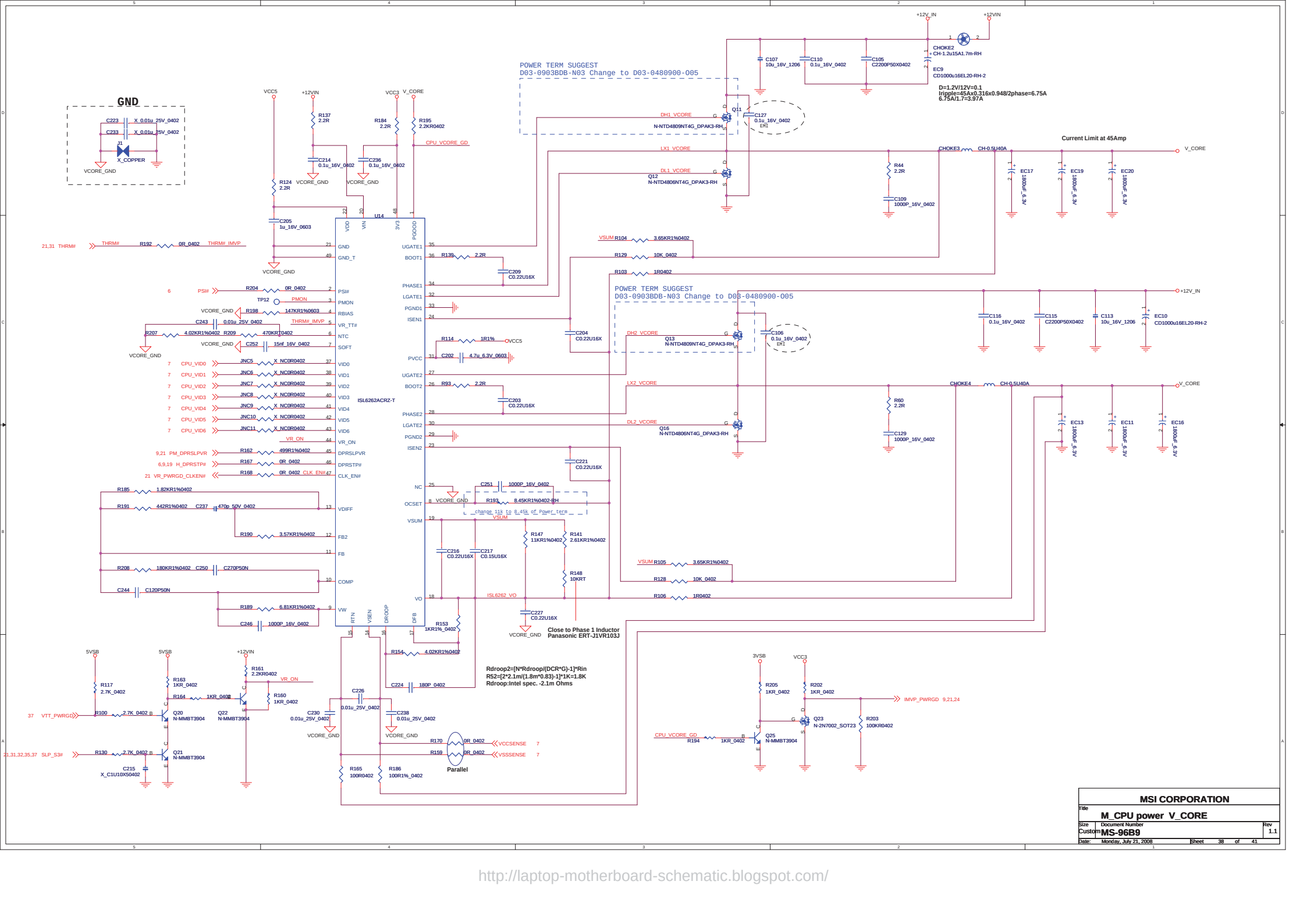
Default Tri-State from ICH9
pull-up for default WOL after G3



MSI CORPORATION

Title	POWER VTT_DDR/+3VM/+3VM_WOL/+1.8VDIMM	
Size: Custom	Document Number: MS-96B9	Rev: 1.1
Date: Monday, July 21, 2008	Sheet 36 of 41	





IMPEDANCE TRACE

TL16 — L1_DIFF_5/6/20_95_OHM- — X_D1x2
Layer 1
DIFF 95 ohm(5/6/20)

TL15 — L1_DIFF_5/6/20_95_OHM+ — X_D1x2
Layer 1
DIFF 95 ohm(5/6/20)

TL11 — L1_DIFF_4/6/20_100_OHM- — X_D1x2
Layer 1
DIFF 100 ohm(4/6/20)

TL12 — L1_DIFF_4/6/20_100_OHM+ — X_D1x2
Layer 1
DIFF 100 ohm(4/6/20)

TL10 — L3_DIFF_4/9/20_100_OHM- — X_D1x2
Layer 3
DIFF 100 ohm(4/9/20)

TL9 — L3_DIFF_4/9/20_100_OHM+ — X_D1x2
Layer 3
DIFF 100 ohm(4/9/20)

TL8 — L4_DIFF_4/9/20_100_OHM- — X_D1x2
Layer 4
DIFF 100 ohm(4/9/20)

TL7 — L4_DIFF_4/9/20_100_OHM+ — X_D1x2
Layer 4
DIFF 100 ohm(4/9/20)

TL2 — L3_DIFF_7/4/20_70_OHM- — X_D1x2
Layer 3
DIFF 70 ohm(7/4/20)

TL5 — L3_DIFF_7/4/20_70_OHM+ — X_D1x2
Layer 3
DIFF 70 ohm(7/4/20)

TL1 — L4_DIFF_5/6.5/20_85_OHM- — X_D1x2
Layer 4
DIFF 85 ohm(5/6.5/20)

TL4 — L4_DIFF_5/6.5/20_85_OHM+ — X_D1x2
Layer 4
DIFF 85 ohm(5/6.5/20)

TL13 — L6_DIFF_5/6/20_95_OHM- — X_D1x2
Layer 6
DIFF 95 ohm(5/6/20)

TL14 — L6_DIFF_5/6/20_95_OHM+ — X_D1x2
Layer 6
DIFF 95 ohm(5/6/20)

TL3 — L6_DIFF_7/4/20_70_OHM- — X_D1x2
Layer 6
DIFF 70 ohm(7/4/20)

TL6 — L6_DIFF_7/4/20_70_OHM+ — X_D1x2
Layer 6
DIFF 70 ohm(7/4/20)

Optics Orientation Holes

FM11 FM7 FM8 FM4 FM3
FM5 FM13 FM6 FM1 FM2
FM12
X_FM

RTC Battery

BAT1_X1
+
BATTERY
-
BAT-CR2032

PCB1
MS-96B9-10

Mounting Holes

MH1 MH2 MH3 MH4
MH6 MH5 MH7 MH8
HOLES_4S_7_5

NB

U22_7 SIP3_NP2
U22_6 SIP3_NP2
U10_X1
MCH Heatsink
X5 X6 X7 X8
X1 X2 X3 X4
GM965_heatsink

U22_3 SIP3_NP2
U22_2 SIP3_NP2
ICH Heatsink
U26
ICH Heatsink

SB

CPU

系統:E91-0000078-A21
單板:E95-0000009-A21
1.1-> 1.1 系統移除所有

CPU_RM
CPU RM
X_CPU_sink duck

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ICH9 GPIO setting

GPIO	Alt Func	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	PMSYNC#	I/O	Core	3.3V	GPI	PM_SYNC#
GPIO[1]	GPIO1	I/O	Core	3.3V	GPI	SB_GPIO1
GPIO[2]	PIRQE#	I/OD	Core	5V	GPI	INT_PIRQE#
GPIO[3]	PIRQF#	I/OD	Core	5V	GPI	INT_PIRQF#
GPIO[4]	PIRQG#	I/OD	Core	5V	GPI	INT_PIRQG#
GPIO[5]	PIRQH#	I/OD	Core	5V	GPI	INT_PIRQH#
GPIO[6]	GPIO6	I/O	Core	3.3V	GPI	SB_GPIO6
GPIO[7]	GPIO7	I/O	Core	3.3V	GPI	SB_GPIO7
GPIO[8]	82551QM_WOL	I/O	Resume	3.3V	GPI	82551QM_WOL
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	LAN_WOL_EN
GPIO[10]	SUS_PWR_ACK	I/O	Resume	3.3V	GPI	SUSPWRACK
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	SMBALERT#
GPIO[12]	LAN_PHY_PWR_CTRL	I/O	Resume	3.3V	GPO	LAN_PHY_PCTRL
GPIO[13]	ENERGY_DETECT	I/O	Resume	3.3V	GPI	LPC_PME#
GPIO[14]	AC_PRESENT	I/O	Resume	3.3V	GPI	AC_PERSENT
GPIO[15]	UNUSED (DP)	I/O	Resume	3.3V	Native	UNUSED (DP)
GPIO[16]	DPRSLPVR	I/O	Core	3.3V	GPO	PM_DPRSLPVR
GPIO[17]	GPIO17	I/O	Core	3.3V	GPI	SB_GPIO17
GPIO[18]	GPIO18	I/O	Core	3.3V	GPO	SB_GPIO18
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	SATA1GP
GPIO[20]	GPIO20	I/O	Core	3.3V	GPO	SB_GPIO20
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	SATA0GP
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	SB_GPIO22
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	LDRQ1#
GPIO[24]	MEM_LED	I/O	Resume	3.3V	GPO	SB_GPIO24
GPIO[25]	UNUSED (DP)	I/O	Resume	3.3V	Native	UNUSED (DP)
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	S4_STATE#
GPIO[27]	GPIO27	I/O	Resume	3.3V	GPO	LAN1_DISABLE#
GPIO[28]	GPIO28	I/O	Resume	3.3V	GPO	USB_EN
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	USBOC#45
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	USBOC#67
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	USBOC#67
GPIO[32]	UNUSED (DP)	I/O	Core	3.3V	GPO	UNUSED (DP)
GPIO[33]	HDA_DOCK_EN#	I/O	Core	3.3V	GPO	SB_GPIO33
GPIO[34]	HDA_DOCK_RST#	I/O	Core	3.3V	GPO	SB_GPIO34
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	SB_GPIO35
GPIO[36]	SATA4GP	I/O	Core	3.3V	GPI	SATA2GP
GPIO[37]	SATA5GP	I/O	Core	3.3V	GPI	SATA3GP
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	MB_ID0
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	MB_ID1
GPIO[40]	OC1#	I/O	Resume	3.3V	Native	USBOC#01
GPIO[41]	OC2#	I/O	Resume	3.3V	Native	USBOC#23
GPIO[42]	OC3#	I/O	Resume	3.3V	Native	USBOC#23
GPIO[43]	OC4#	I/O	Resume	3.3V	Native	USBOC#45
GPIO[44]	OC8#	I/O	Resume	3.3V	Native	USBOC#8_11
GPIO[45]	OC9#	I/O	Resume	3.3V	Native	USBOC#8_11
GPIO[46]	OC10#	I/O	Resume	3.3V	Native	USBOC#8_11
GPIO[47]	OC11#	I/O	Resume	3.3V	Native	USBOC#8_11
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	SB_GPIO48
GPIO[49]	GPIO49	I/O	Core	3.3V	GPO	SB_GPIO49
GPIO[50]	REQ1#	I/O	Core	5V	Native	PCI_REQ#1
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PCI_GNT#1
GPIO[52]	REQ2#	I/O	Core	5V	Native	PCI_REQ#2
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PCI_GNT#2
GPIO[54]	REQ3#	I/O	Core	5V	Native	PCI_REQ#3
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PCI_GNT#3
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	GLAN_DOCK#
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	3VSB
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC0#	I/O	Resume	3.3V	Native	USBOC#01
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	SMB_LINK_ALERT#

Super IO GPIO setting

GPIO	Alt Func	Power	Signal Name	I/O
GPIO[20]	CPUFANIN1	Core	CPU_FANPWM	Output
GPIO[21]	CPUFANOUT1	Core	CPUFANIN	Input
GPIO[22]	SCE#/PLED/WDTO#	Core	unused	
GPIO[23]	SCK	Core	FAN_TYPE	Output
GPIO[24]	MSDATA	Resume	MSDATA	
GPIO[25]	MSCLK	Resume	MSCLK	
GPIO[26]	KBDATA	Resume	KBDATA	
GPIO[27]	KBCLK	Resume	KBCLK	
GPIO[30]	GP30	Resume	unused	Output
GPIO[31]	GP31	Resume	unused	Output
GPIO[32]	RSTOUT2#/SCL	Resume	unused	
GPIO[33]	RSTOUT3#/SDA	Resume	unused	
GPIO[34]	RSTOUT4#	Resume	unused	Output
GPIO[35]	GP35	Resume	unused	Output
GPIO[36]	GP36	Resume	unused	Output
GPIO[37]	GP37	Resume	unused	Output
GPIO[40]	RIB#	Resume	unused	
GPIO[41]	DCDB#	Resume	LED_SEL1	
GPIO[42]	RTX/SOUTB	Resume	unused	
GPIO[43]	RRX/SINB	Resume	unused	
GPIO[44]	DTRB#	Resume	unused	
GPIO[45]	RTSB#	Resume	unused	
GPIO[46]	DSRB#	Resume	LED_SEL2	
GPIO[47]	CTSB#	Resume	unused	
GPIO[50]	EN_VRM10/WDTO#	Resume	WDTO#	Output
GPIO[51]	RSMRST#	Resume	RSMRST#	Output
GPIO[52]	SUSB#	Resume	SLP_S3#	Intput
GPIO[53]	PSON#	Resume	ATX_PSON#	Output
GPIO[54]	PWROK	Resume	unused	Output
GPIO[55]	SUSLED	Resume	SUSLED	Output
GPIO[56]	PSIN#	Resume	PSIN#	Input
GPIO[57]	PSOUT#	Resume	PWRBTN#	Output
GPIO[60]	RIA#	Core	RIA#	
GPIO[61]	DCDA#	Core	DCDA#	
GPIO[62]	SOUTA/PENKBC	Core	SOUTA	
GPIO[63]	SINA	Core	SINA	
GPIO[64]	DTRA#/PENROM	Core	DTRA#	
GPIO[65]	RTSA#/HEFRAS	Core	RTSA#	
GPIO[66]	DSRA#	Core	DSRA#	
GPIO[67]	CTSA#	Core	CTSA#	

PCI rounting

Device	Interrupt	ID select	REQ&GNT
PCI slot 1	INT_PIRQ#A INT_PIRQ#B INT_PIRQ#C INT_PIRQ#D	AD20	PCI_REQ#0 PCI_GNT#0
PCI slot 2	INT_PIRQ#B INT_PIRQ#C INT_PIRQ#D INT_PIRQ#A	AD21	PCI_REQ#1 PCI_GNT#1
ITE IT8213F	INT_PIRQC#	AD22	PCI_REQ#2 PCI_GNT#2
LAN 82551QM	INT_PIRQD#	AD23	PCI_REQ#3 PCI_GNT#3

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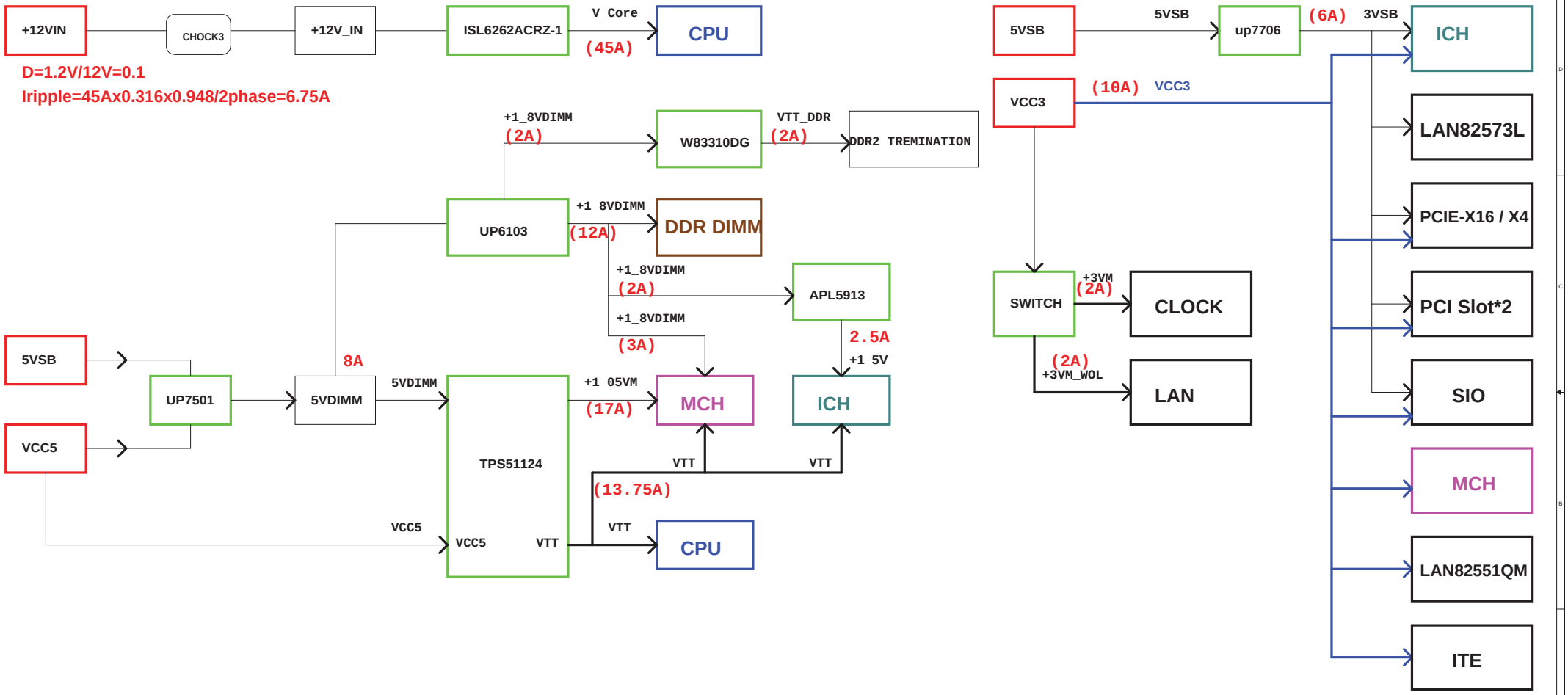
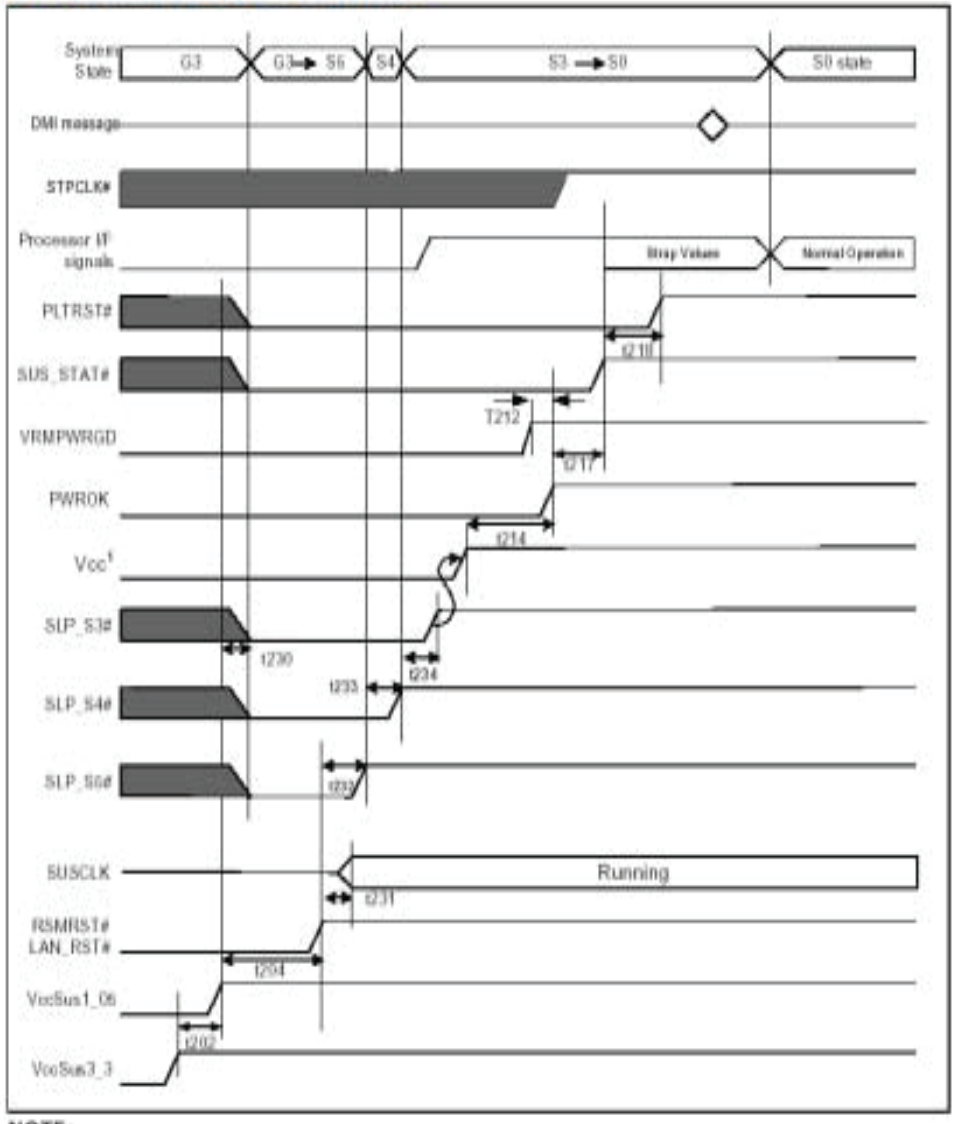


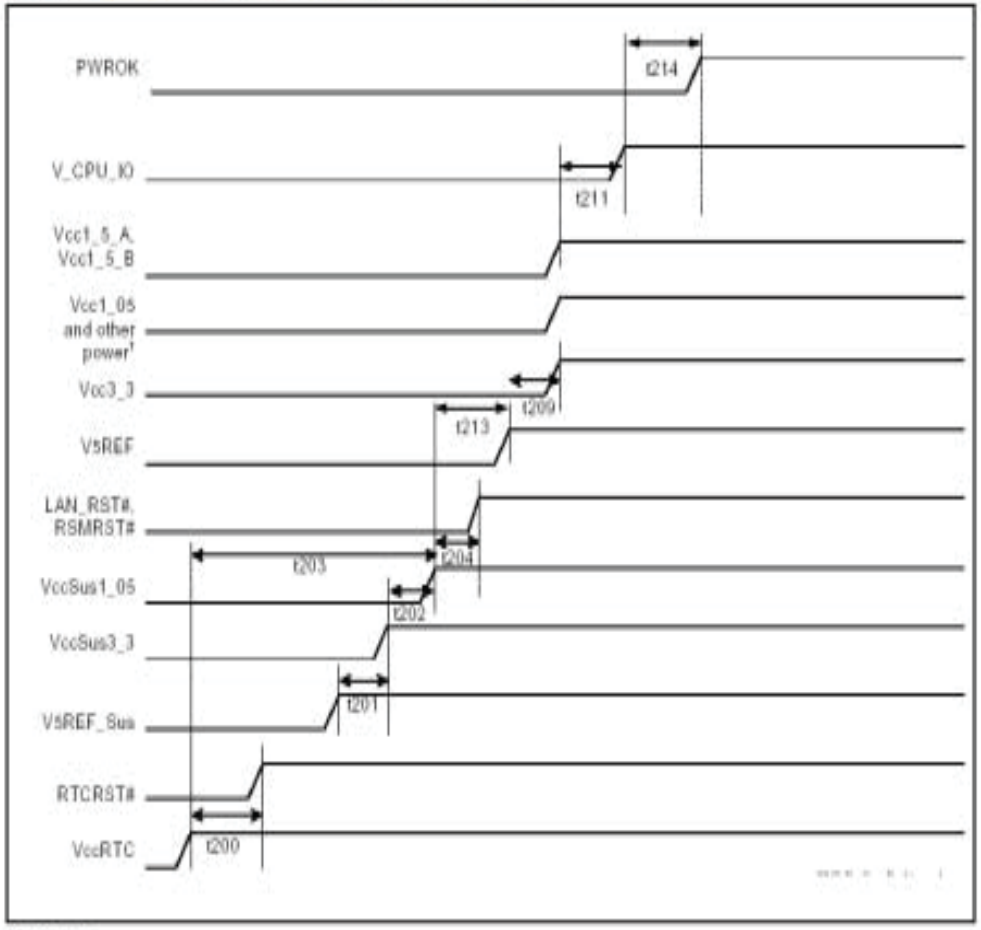
G3 (Mechanical Off) to S0 Timings



NOTE:

1. Vcc includes Vcc1_5_A, Vcc1_5_B, Vcc3_3, Vcc1_05, VccUSBPLL, VccDMIPLL, VccSATAPLL, V5REF and V_CPU_IO.

Power Sequencing and Reset Signal Timings



NOTES:

1. Other power includes VccUSBPLL, VccDMIPLL, and VccSATAPLL. All of these power signals must independently meet the timings shown in the figure. There are no timing interdependencies between Vcc1_05 and these other power signals. There are also no timing interdependencies for these power signals, including Vcc1_05, to Vcc3_3 and Vcc1_5_A/Vcc1_5_B.
2. PWROK must not glitch, even if RSMRST# is low.

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