



MS-96B6

Version: 0B

11/04/2008

PAGE	TITLE
01	Cover Sheet
02	System Block Diagram
03	Clock Block Diagram
04	Power Block Diagram
05	GPIO Table
06	Power On Sequence
07	SMBus Block Diagram
08	Tolapai PMI/ MISC
09	Tolapai GBe/ SATA/ USB
10	Tolapai PCIe/ CAN/ BIOS
11	Tolapai DDRII
12	Tolapai LEB/ GPIO/ UART
13	Tolapai VCC
14	Tolapai GND
15	DDRII-667 Memory Down-1
16	DDRII-667 Memory Down-2
17	DDRII Termination
18	CK410 Clock Gen
19	Marvell 88SB2211-1
20	Marvell 88SB2211-2
21	Fortinet CP6
22	Com Port/ Modem/ SATA Con.
23	Express Card/Mini-PCI
24	PS2232/ Nand Flash
25	USB/ GL850G
26	Marvell 88E1121R-1
27	Marvell 88E1121R-2
28	Marvell 88E6096A2-1
29	Marvell 88E6096A2-2
30	Marvell 88E6096A2-3
31	Marvell 88E6096A2-4
32	W83L786NG/LED
33	SYSTEM FAN
34	Reset Logic
35	EMI Caps
36	CPU POWER & 1.2V
37	DDR POWER & +12V
38	AUX POWER
39	DC-IN POWER
40	MISC
41	HYNIX MEMORY
42	NANYA MEMORY
43	HISTORY

System Chipset:

Intel Tolapai 600/1.2G W/O Acceleration 1088-FCBGA

On Board Chipset:

Clock Gen -- CK410

PS2232 Nand Flash

PCIe to PCI -- Marvell 88SB2211

Fortinet CP6

PHY0 -- Marvell 88E6096A2

Dual PHY -- Marvell 88E1121R

USB Hub -- GL850G

Main Memory:

DDRII-667 Memory Down 1G

Expansion Slot:

Mini-PCI *1

Express Card *1

SATA *1

USB *3 (One Internal)

Com Port *1

Modem *1

RJ45 *8

DMZ *1

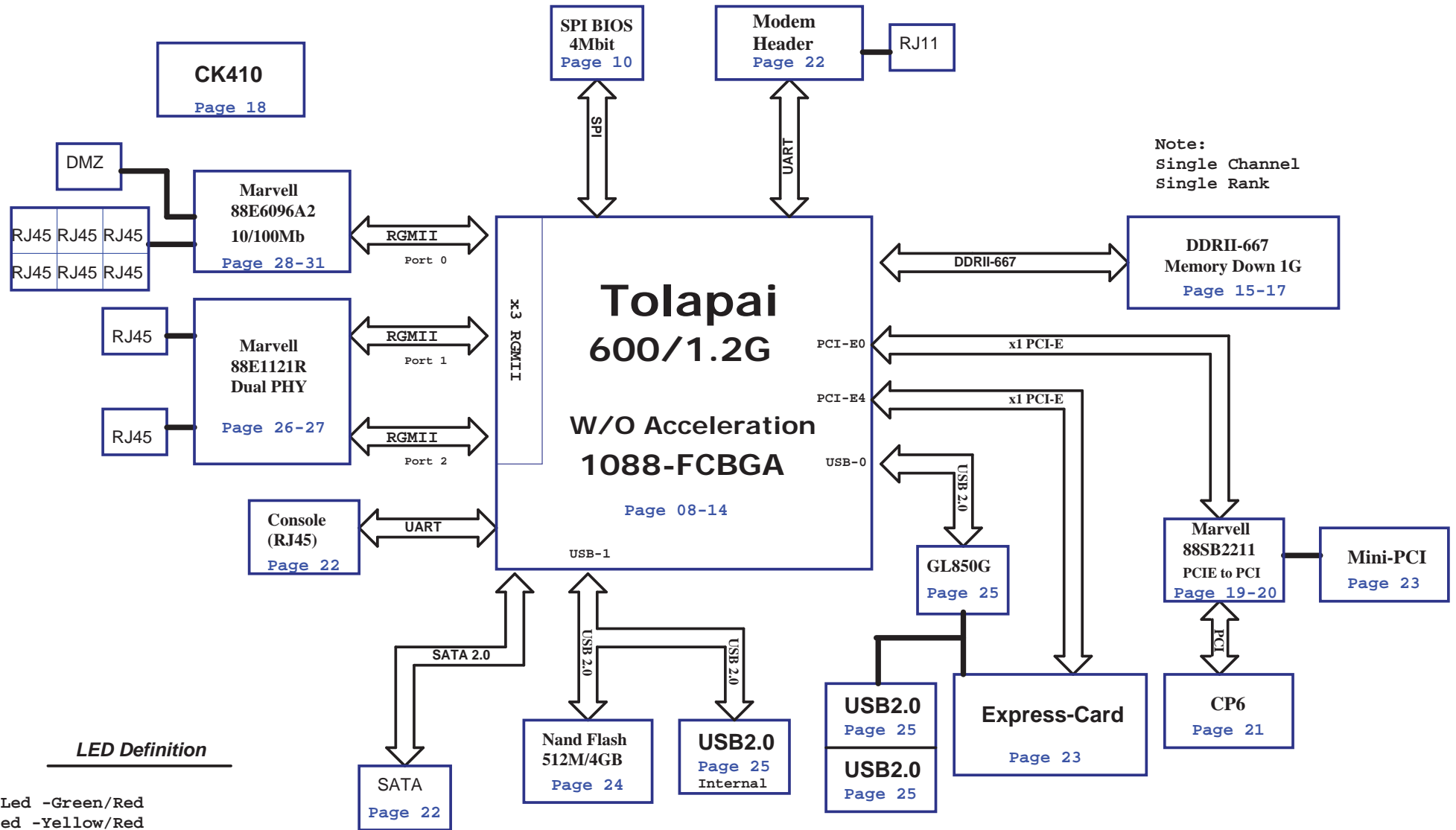
RJ11 *1



MICRO-STAR INT'L CO.,LTD

MS-96B6

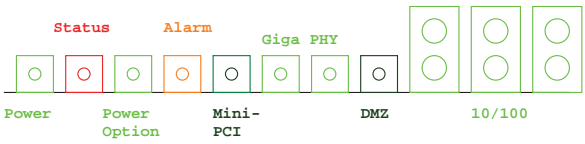
Size Custom	Document Description Cover Sheet	Rev 0B
Date: Tuesday, November 25, 2008	Sheet 1 of	43



Note:
Single Channel
Single Rank

LED Definition

Status Led -Green/Red
Alarm Led -Yellow/Red
Other Led - Green

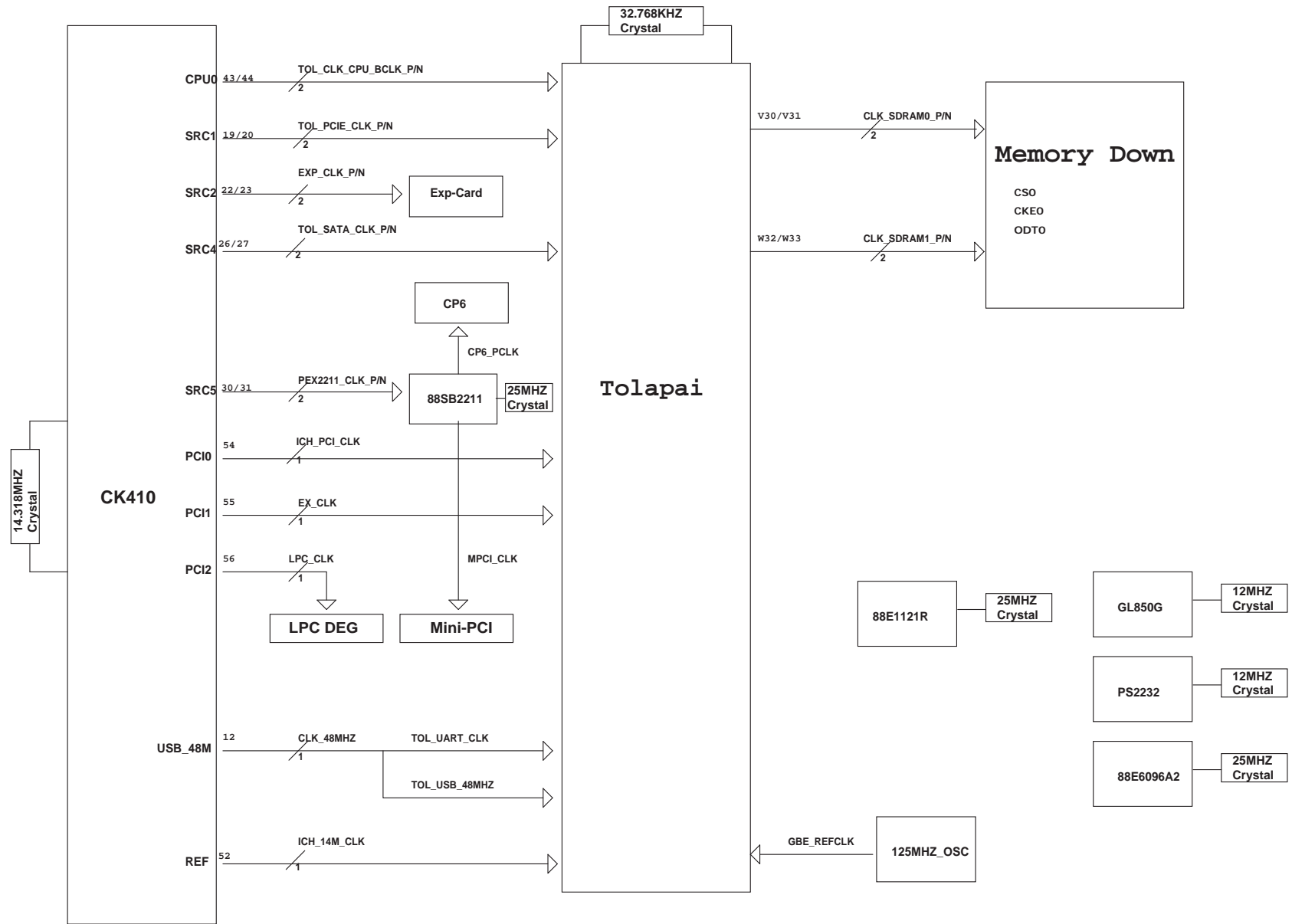


FortiGate 60C And Deviations

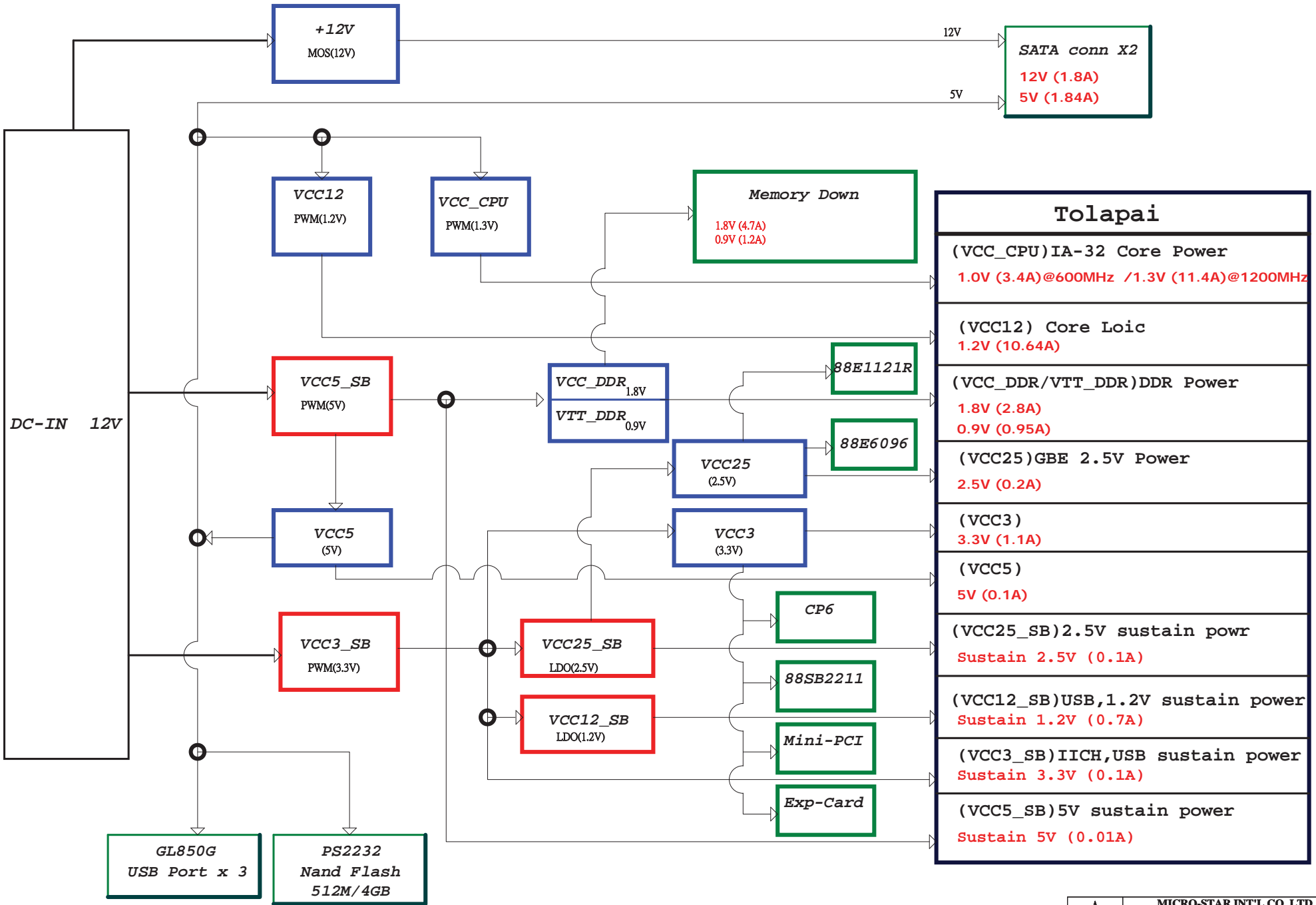
<http://laptop-motherboard-schematic.blogspot.com/>

MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description System Block Diagram	Rev 0B
Date: Tuesday, November 25, 2008 Sheet 2 of 43		

MS-96B6 CLOCK BLOCK DIAGRAM



MS-96B6 POWER DELIVERY DIAGRAM



Tolapai	
(VCC_CPU) IA-32 Core Power	1.0V (3.4A)@600MHz / 1.3V (11.4A)@1200MHz
(VCC12) Core Ioic	1.2V (10.64A)
(VCC_DDR/VTT_DDR) DDR Power	1.8V (2.8A) 0.9V (0.95A)
(VCC25) GBE 2.5V Power	2.5V (0.2A)
(VCC3)	3.3V (1.1A)
(VCC5)	5V (0.1A)
(VCC25_SB) 2.5V sustain power	Sustain 2.5V (0.1A)
(VCC12_SB) USB, 1.2V sustain power	Sustain 1.2V (0.7A)
(VCC3_SB) IICH, USB sustain power	Sustain 3.3V (0.1A)
(VCC5_SB) 5V sustain power	Sustain 5V (0.01A)


Tolapai GPIO Setting

EDS,Page895

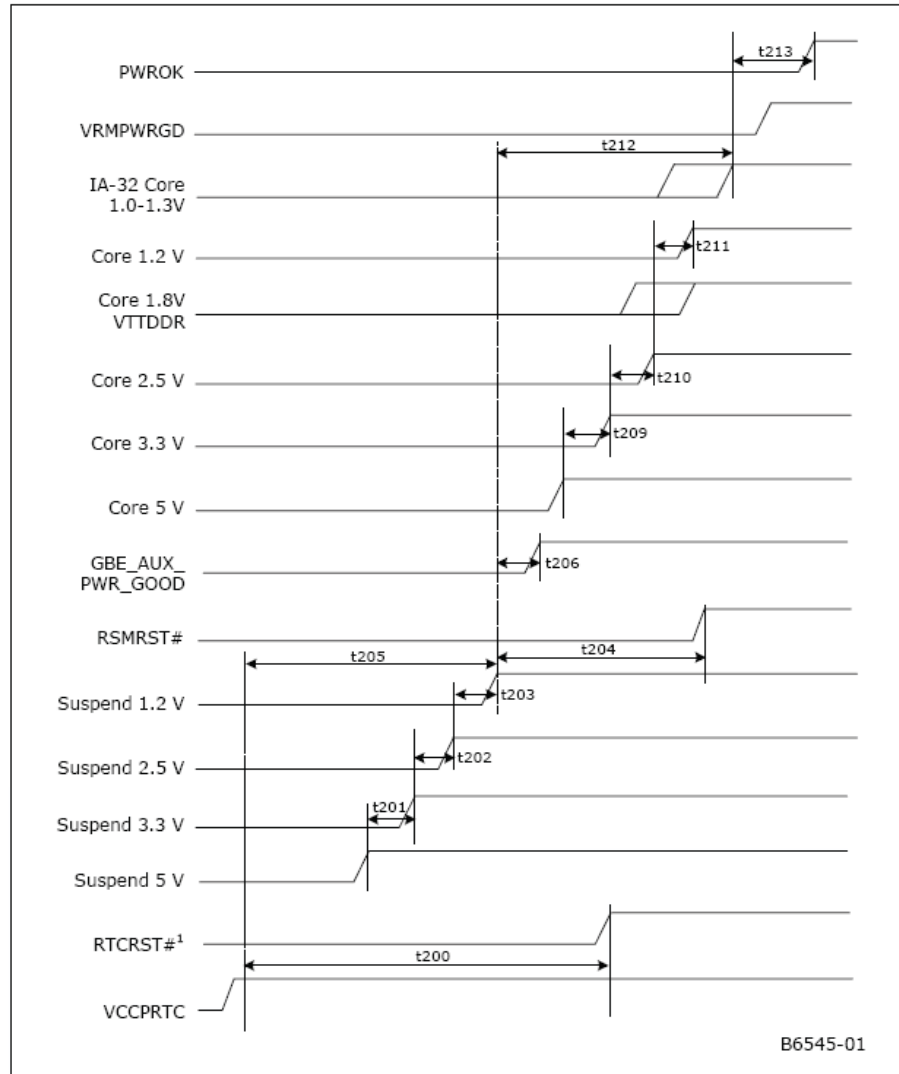
	Mode Capability	Default I/O Type	Default Value	Default Function	Alternate Function	Power Well	MSI Function
GPI0	I	I	n/a	GPI	n/a	Core	
GPI1	I	I	n/a	GPI	n/a	Core	
GPI2	I	I	n/a	GPI	PIRQE#	Core	PIRQE#
GPI3	I	I	n/a	GPI	PIRQF#	Core	PIRQF#
GPI4	I	I	n/a	GPI	PIRQG#	Core	
GPI5	I	I	n/a	GPI	PIRQH#	Core	
GPI6	I	I	n/a	GPI	n/a	Core	SMI#
GPI7	I	I	n/a	GPI	n/a	Core	
GPI8	I	I	n/a	GPI	n/a	Suspend	
GPI9	I	I	n/a	GPI	n/a	Suspend	
GPI10	I	I	n/a	GPI	n/a	Suspend	
GPI11	I	I	n/a	SMBALERT#	GPI11	Suspend	
GPI12	I	I	n/a	GPI	n/a	Core	
GPI13	I	I	n/a	GPI	n/a	Core	
GPI14	I	I	n/a	GPI	n/a	Suspend	CPUSB#
GPI15	I	I	n/a	GPI	n/a	Suspend	CPPE#
GPIO16	O	O	High	GPO	IRQ24	Core	
GPIO17	O	O	High	GPO	IRQ25	Core	
GPIO18	O	O	High	GPO	IRQ36	Core	NAND_PWR_ON
GPIO19	O	O	High	GPO	IRQ37	Core	STATUS_A_RED#
GPIO20	O	O	High	GPO	IRQ26	Core	POWER_LED#
GPIO21	O	O	High	GPO	IRQ27	Core	STATUS_B_YEL#
GPIO23	O	O	Low	GPO	IRQ28	Core	
GPIO24	I/O	O	High	GPO	IRQ29	Suspend	STATUS_24
GPIO25	I/O	O	High	GPO	IRQ38	Suspend	STATUS_25
GPI26	I	I	n/a	GPI	SATA0GP	Core	
GPIO27	I/O	O	High	GPO	IRQ39	Suspend	STATUS_27
GPIO28	I/O	O	High	GPO	IRQ30	Suspend	EXP_SHDN#
GPI29	I	I	n/a	GPI	SATA1GP	Core	
GPI30	I	I	n/a	GPI	IRQ31	Core	
GPI31	I	I	n/a	GPI	IRQ32	Core	
GPIO33	I/O	O	High	GPO	IRQ33	Core	
GPIO34	I/O	O	High	GPO	IRQ34	Core	USB_PWR_ON
GPI40	I	I	n/a	GPI	IRQ35	Core	IERR#
GPI41	I	I	n/a	LDRQ1#	GPI41	Core	
GPO48	O	O	High	GPO	n/a	Core	HOST_PERST#

PCI routing

Device	Interrupt	ID select	REQ&GNT
Fortinet CP6	PIRQ#A	AD16	PREQ#0 PGNT#0
Mini-PCI	PIRQ#B PIRQ#C	AD17	PREQ#1 PGNT#1

			MICRO-STAR INT'L CO.,LTD	
			MS-96B6	
Size B	Document Description			Rev 0B
	GPIO Table			
Date: Tuesday, November 25, 2008		Sheet 5 of 43		

Power Rail Sequence Timings (Suspend Well Power Management)



Notes:

1. RTCRST# is a platform signal that is typically tied to RTEST# - RTC Well Test.
2. "Suspend" refers to operating under sustain voltage and "Core" refers to the main power supply.

Power Rail Signal Timings

Sym	Parameter	Min	Max	Units	Notes
t200	VCCPRTC active to RTCRST# inactive	18	-	ms	1
t201	Suspend 5V active to Suspend 3.3V active	0	-	ms	2
t202	Suspend 3.3V active to Suspend 2.5V active	0	-	ms	3
t203	Suspend 2.5V active to Suspend 1.2V active	0	-	ms	4
t204	Suspend supplies active to RSMRST# inactive	10	-	ms	
t205	VCCPRTC supply active to Suspend supplies active	0	-	ms	5
t206	Suspend supplies active to GBE_AUX_PWR_GOOD active	0	-	ms	-
t209	Core 5V active to Core 3.3V active	0	-	ms	2
t210	Core 3.3V active to Core 2.5V active	0	-	ms	6
t211	Core 2.5V active to Core 1.2V active	0	-	ms	7
t212	Suspend supplies active to Core supplies active	0	-	ms	5
t213	All core supplies active to SYS_PWROK active	99	-	ms	-

Notes:

1. RTCRST# is a platform signal that is typically tied to RTEST# - RTC Well Test.
2. The 5V supply must power up before its associated 3.3V supply within 0.3V, and must power down after the 3.3V supply within 0.3V.
3. Ensure the following:
 - a) Suspend 3.3V must power up before Suspend 2.5V or after Suspend 2.5 within 0.3V
 - b) Suspend 2.5V must power down before Suspend 3.3V or after Suspend 3.3V within 0.3V.
4. Ensure the following:
 - a) Suspend 2.5V must power up before Suspend 1.2V or after Suspend 1.2V within 0.3V
 - b) Suspend 1.2V must power down before Suspend 2.5 V or after Suspend 2.5 V within 0.3V.
 The VccSus supplies must never be active while the VCCPRTC supply is inactive.
5. Ensure the following:
 - a) Core 3.3 V must power up before Core 2.5V or after Core 2.5V within 0.3V
 - b) Core 2.5V must power down before Core 3.3 V or after Core 3.3V within 0.3V.
6. Ensure the following:
 - a) Core 2.5V must power up before Vcc1.2V or after Core 1.2V within 0.3V
 - b) Core 1.2V must power down before Core 2.5V or after Core 2.5V within 0.3V.
7. "Suspend" refers to operating under sustain voltage and "Core" refers to the main power supply.



MICRO-STAR INT'L CO.,LTD

MS-96B6

Size
B

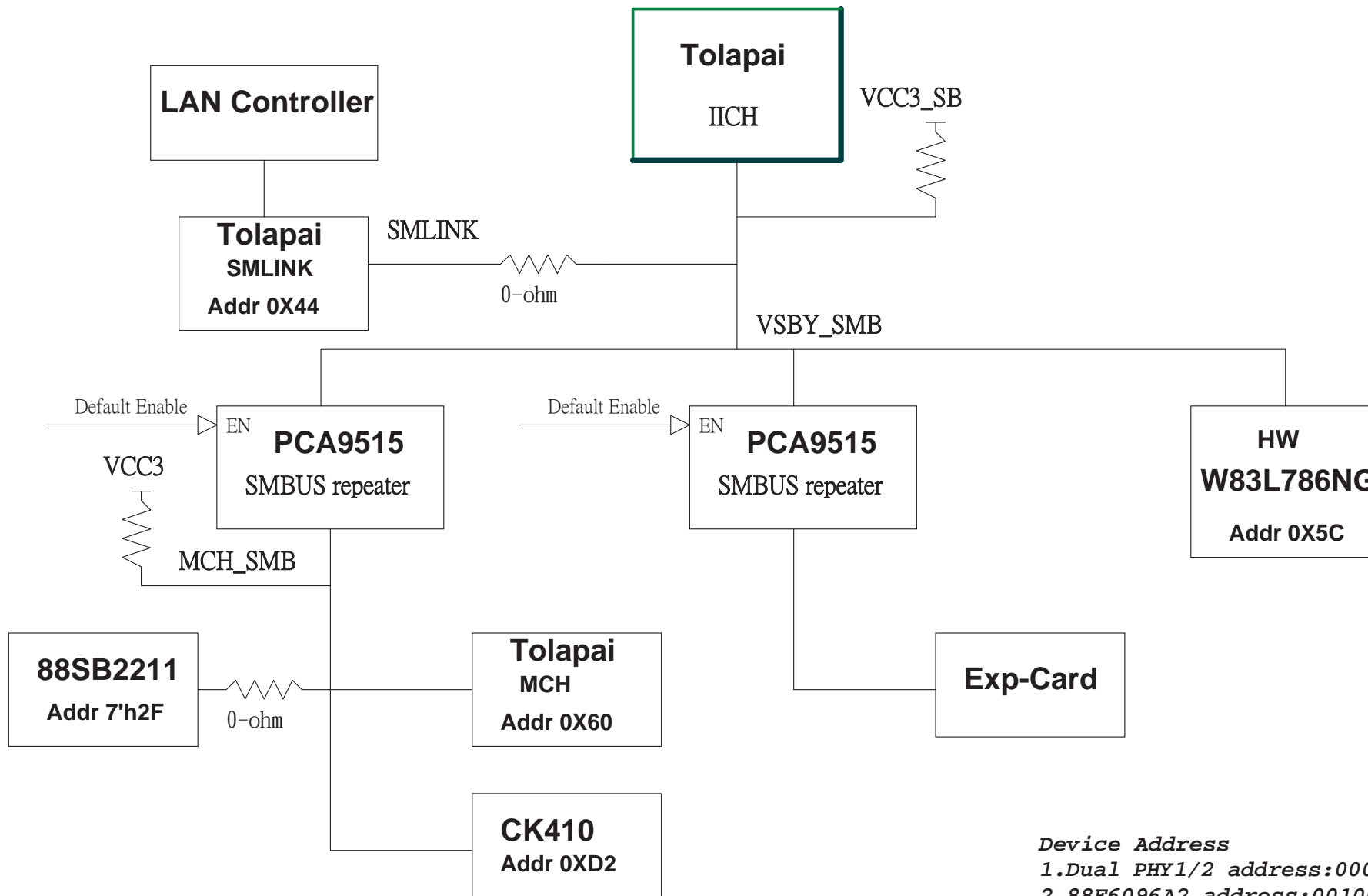
Document Description

Power On Sequence

Rev
0B

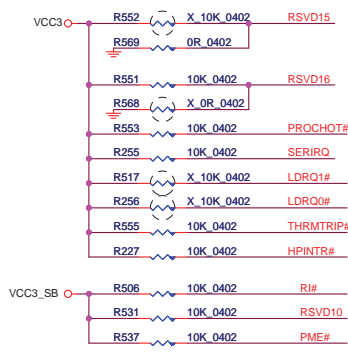
Date: Tuesday, November 25, 2008

Sheet 6 of 43

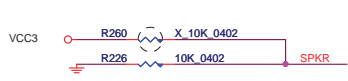
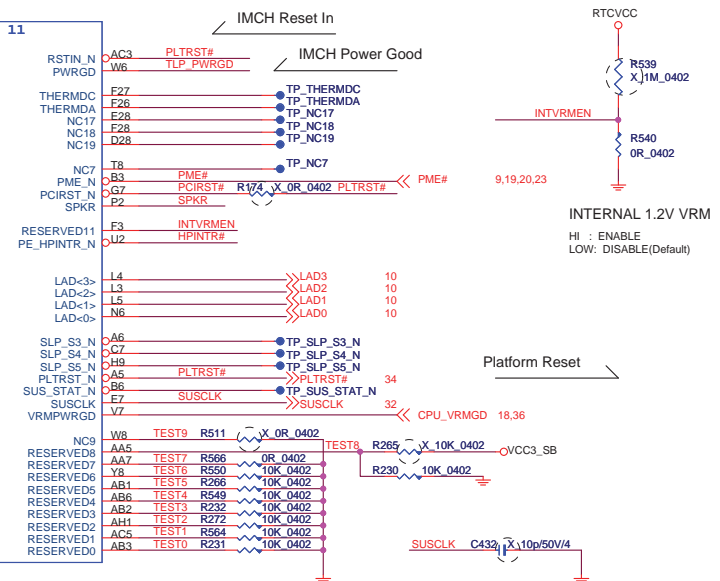
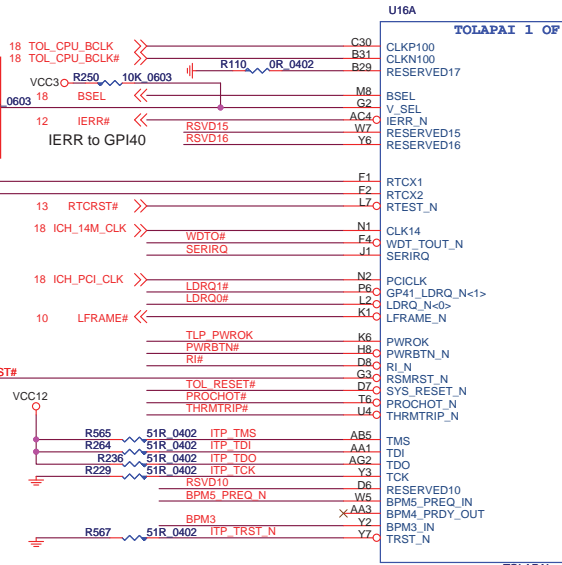
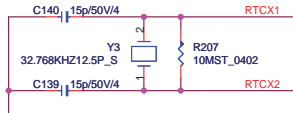


Device Address
 1. Dual PHY1/2 address: 00010/00011
 2. 88E6096A2 address: 00100



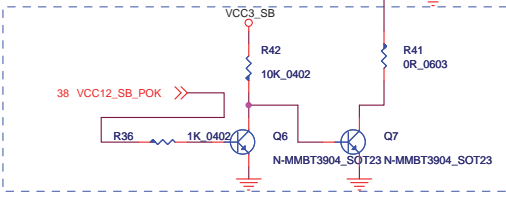


For 600 SKU Insert

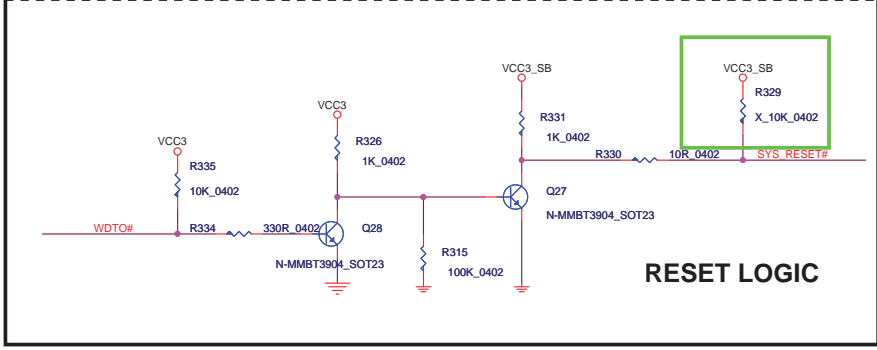
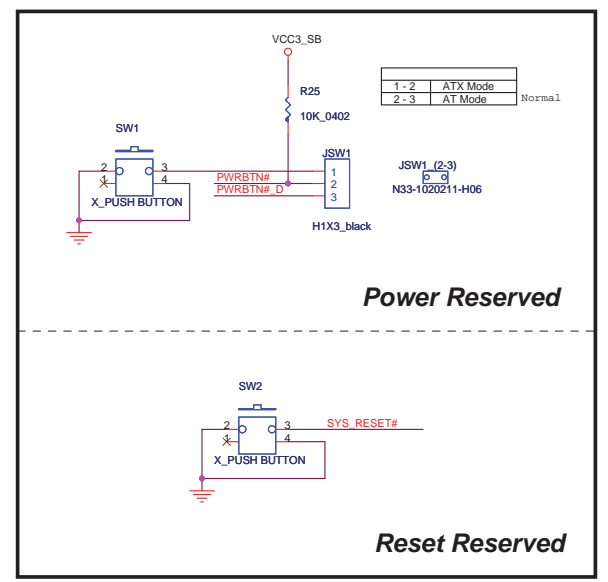
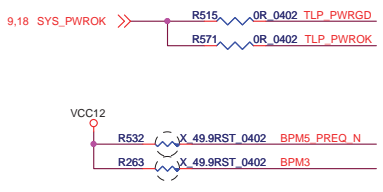
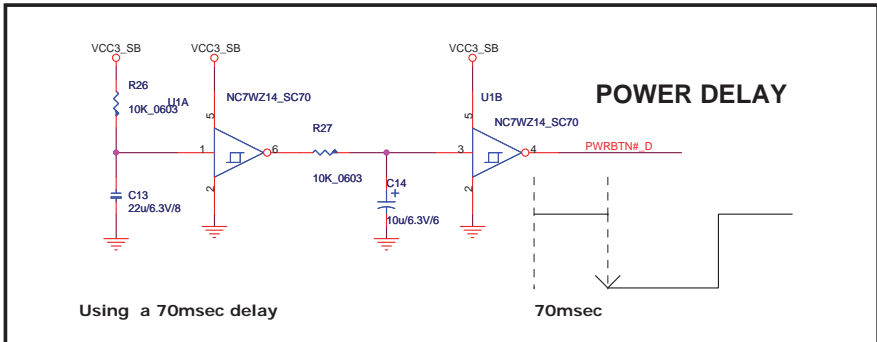


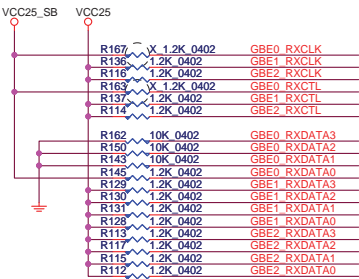
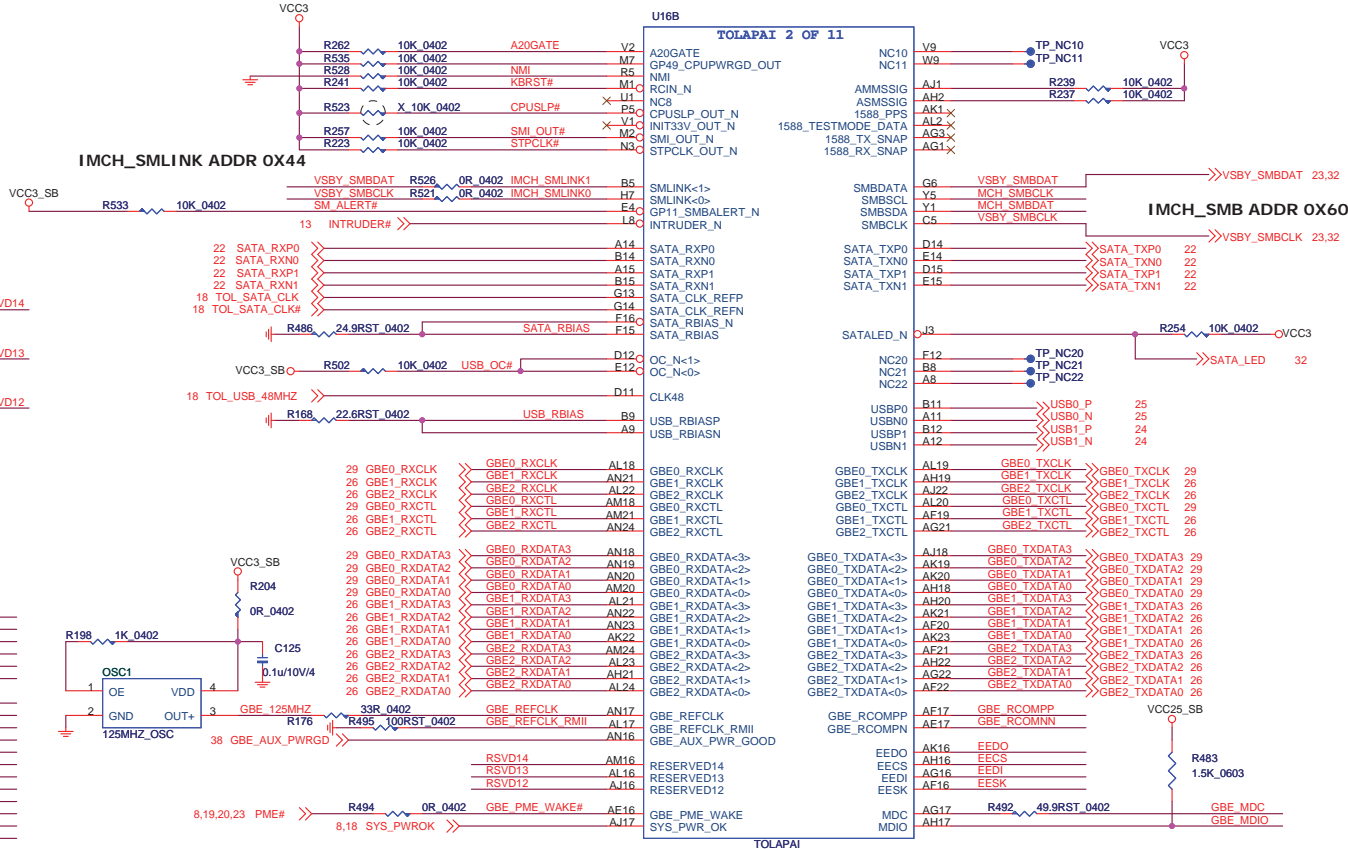
No Reboot Strap (SPKR)

0 = Reboot on second timeout of TCO timer
1 = No Reboot on second timeout of TCO timer

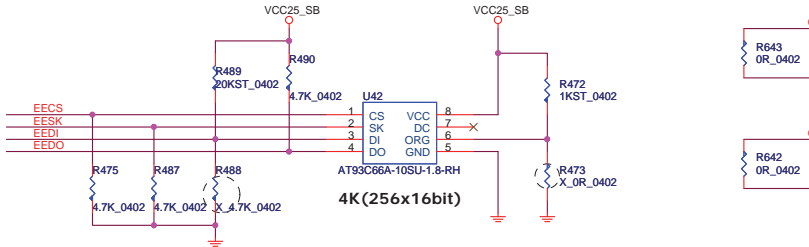
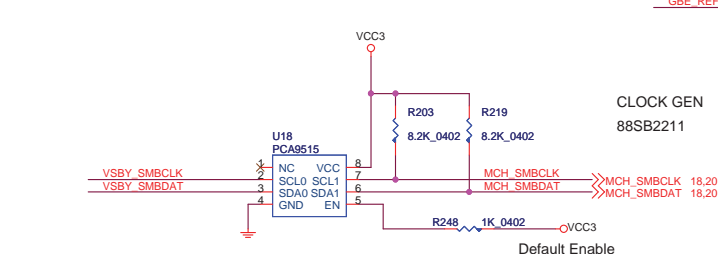


Delay 20ms

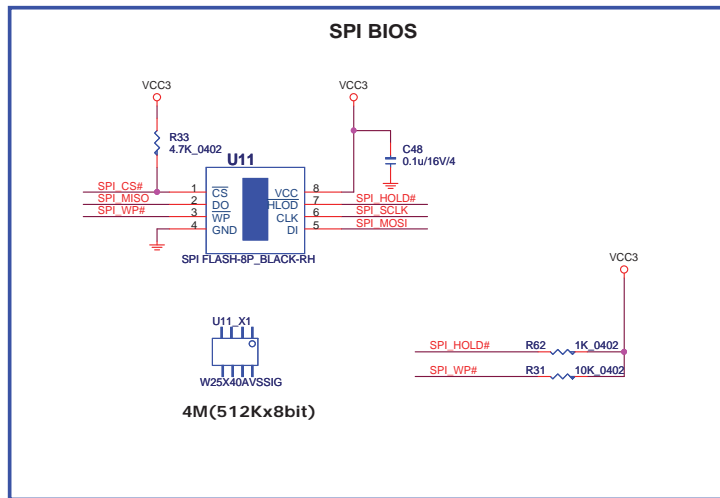
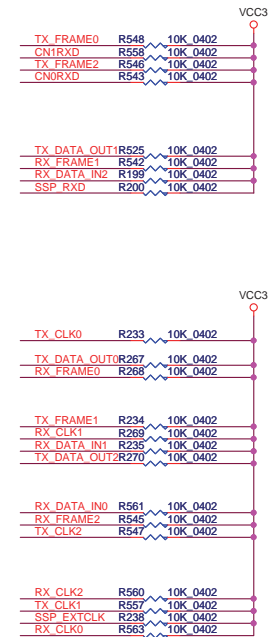
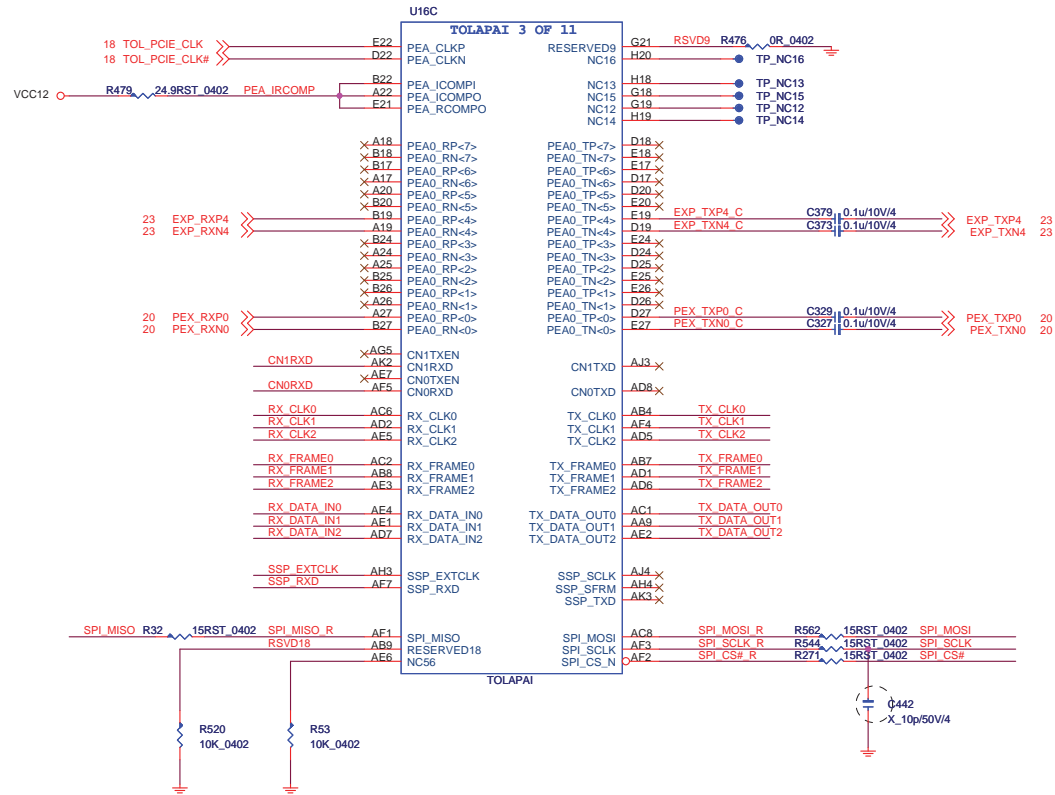




GBE_REFCLK is 125 MHz for RGMII Mode

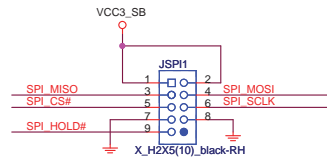


MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description Tolapai GBE/ SATA/ USB	Rev 0B
Date: Saturday, December 20, 2008	Sheet 9	of 43

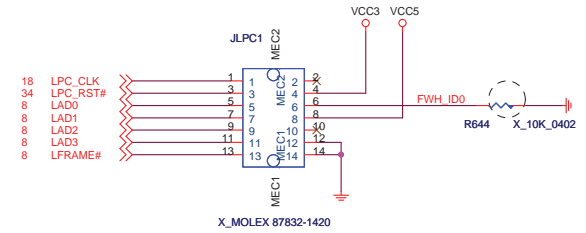


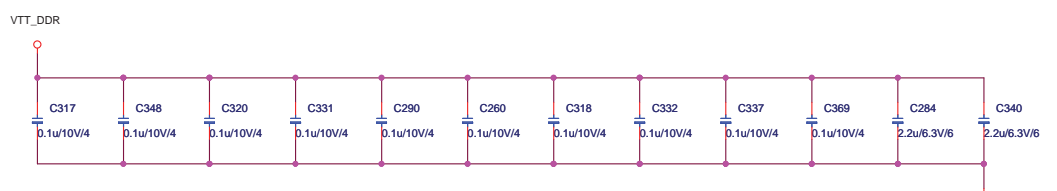
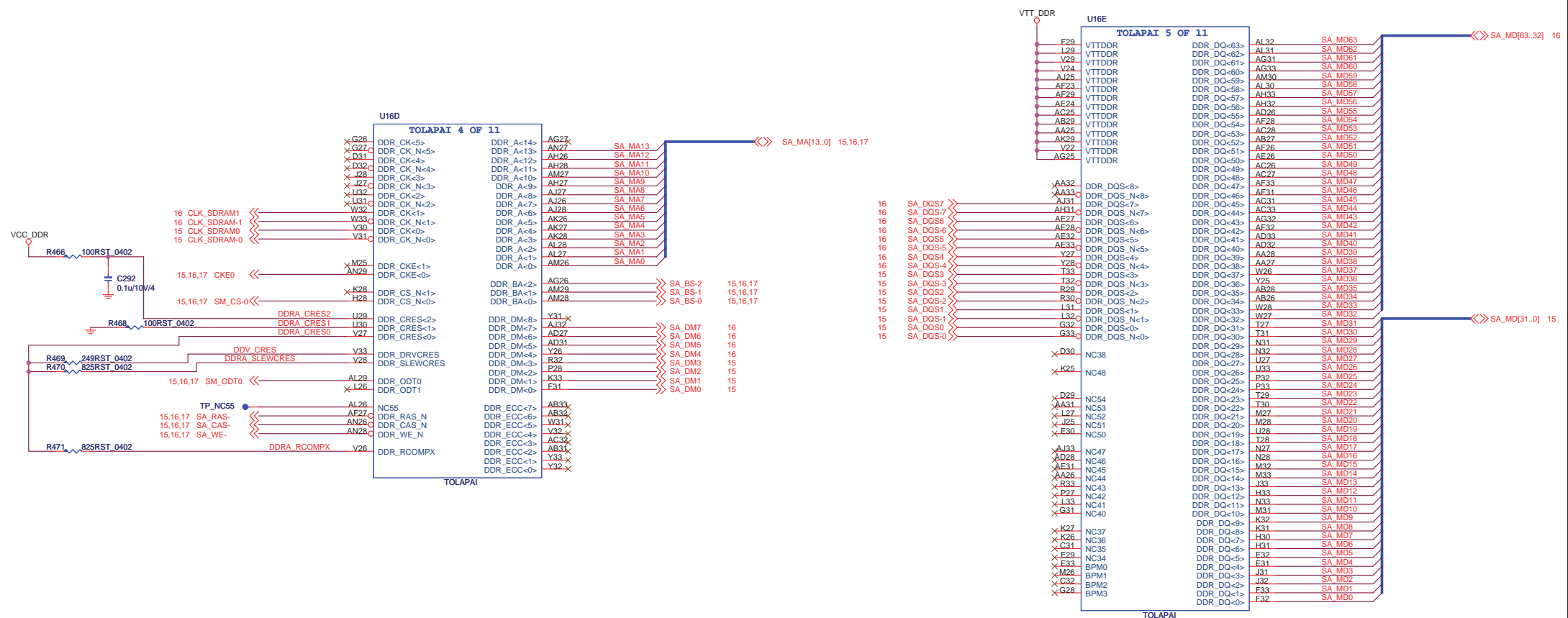
SPI DEBUG PORT

Place close to SPI ROM



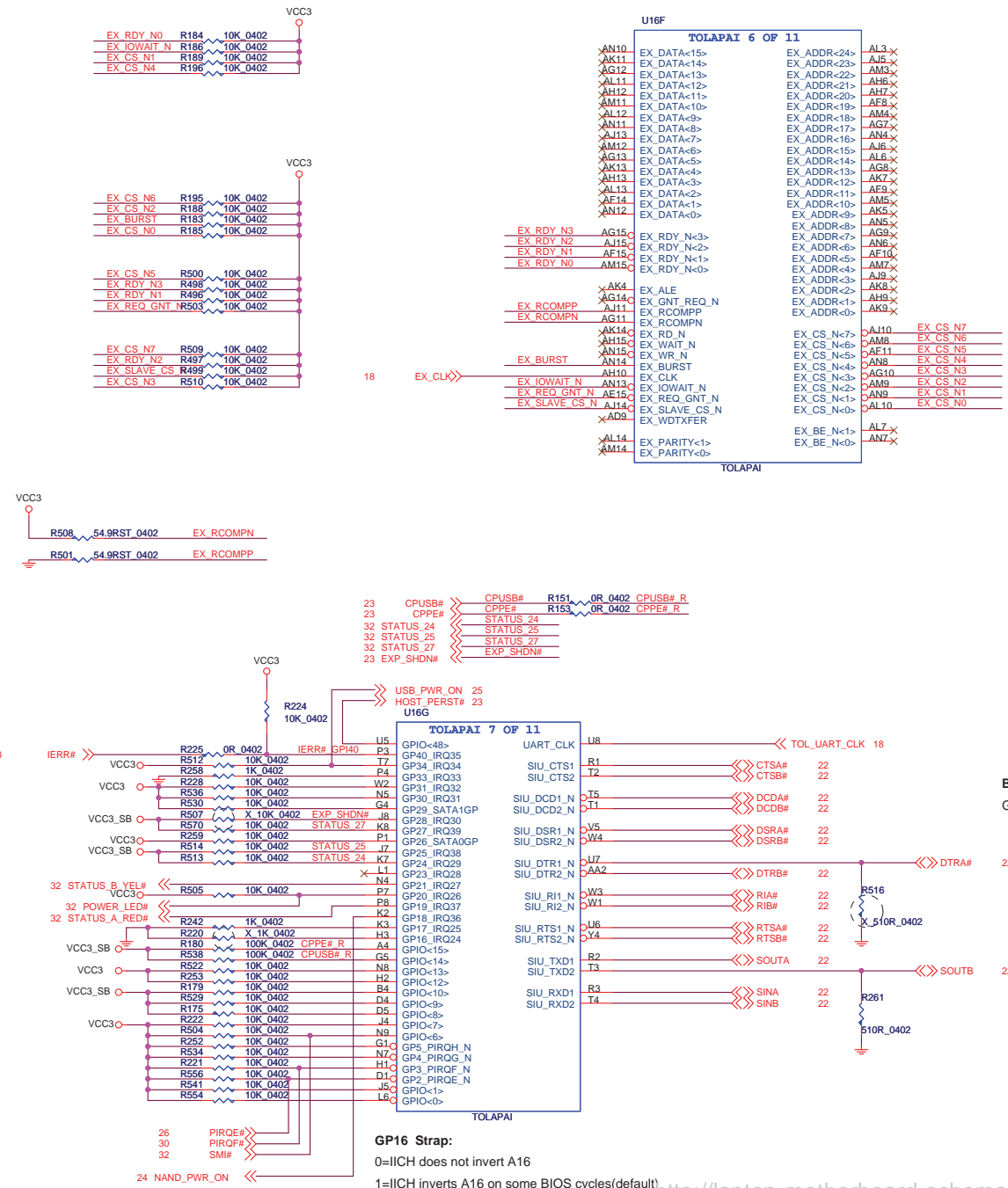
LPC Debug Port





MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description Tolapai DDRII	Rev 0B
Date: Saturday, December 20, 2008		Sheet 11 of 43

Mode Capability	Default I/O Type	Default Value	Default Function	Alternate Function	Power Well	MSI Function
GPIO	I	I	n/a	GPI	n/a	Core
GPIO	I	I	n/a	GPI	n/a	Core
GPIO	I	I	n/a	GPI	PIRQE#	Core PIRQE#
GPIO	I	I	n/a	GPI	PIRQF#	Core PIRQF#
GPIO	I	I	n/a	GPI	PIRQG#	Core
GPIO	I	I	n/a	GPI	PIRQH#	Core
GPIO	I	I	n/a	GPI	n/a	Core SMI#
GPIO	I	I	n/a	GPI	n/a	Core
GPIO	I	I	n/a	GPI	n/a	Suspend
GPIO	I	I	n/a	GPI	n/a	Suspend
GPIO	I	I	n/a	GPI	n/a	Suspend
GPIO	I	I	n/a	SMBALERT#	GP111	Suspend
GPIO	I	I	n/a	GPI	n/a	Core
GPIO	I	I	n/a	GPI	n/a	Core
GPIO	I	I	n/a	GPI	n/a	Suspend CPUSB#
GPIO	I	I	n/a	GPI	n/a	Suspend CPPE#
GPIO	O	O	High	GPO	IRQ24	Core
GPIO	O	O	High	GPO	IRQ25	Core
GPIO	O	O	High	GPO	IRQ36	Core NAND_PWR_ON
GPIO	O	O	High	GPO	IRQ37	Core STATUS_A_RED#
GPIO	O	O	High	GPO	IRQ26	Core POWER_LED#
GPIO	O	O	High	GPO	IRQ27	Core STATUS_B_YEL#
GPIO	O	O	Low	GPO	IRQ28	Core
GPIO	I/O	O	High	GPO	IRQ29	Suspend STATUS_24
GPIO	I/O	O	High	GPO	IRQ38	Suspend STATUS_25
GPIO	I	I	n/a	GPI	SATA0GP	Core
GPIO	I/O	O	High	GPO	IRQ39	Suspend STATUS_27
GPIO	I/O	O	High	GPO	IRQ30	Suspend EXP_SHDN#
GPIO	I	I	n/a	GPI	SATA1GP	Core
GPIO	I	I	n/a	GPI	IRQ31	Core
GPIO	I	I	n/a	GPI	IRQ32	Core
GPIO	I/O	O	High	GPO	IRQ33	Core
GPIO	I/O	O	High	GPO	IRQ34	Core USB_PWR_ON
GPIO	I	I	n/a	GPI	IRQ35	Core IERR#
GPIO	I	I	n/a	LDRQ1#	GP141	Core
GPO	O	O	High	GPO	n/a	Core HOST_PERST#



Boot Option

GPIO17	GPIO33	Boot Option
0	0	Boot BIOS from SPI (Default)
0	1	Reserved
22	0	Reserved
1	1	Boot BIOS from LPC

PORT ADDRESS
 0 = IO ADDRESSES 02EH AND 02FH
 1 = IO ADDRESSES 04EH AND 04FH
 (DEFAULT WITH INTERNAL PULL-UP)

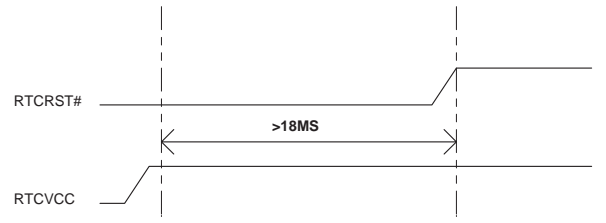
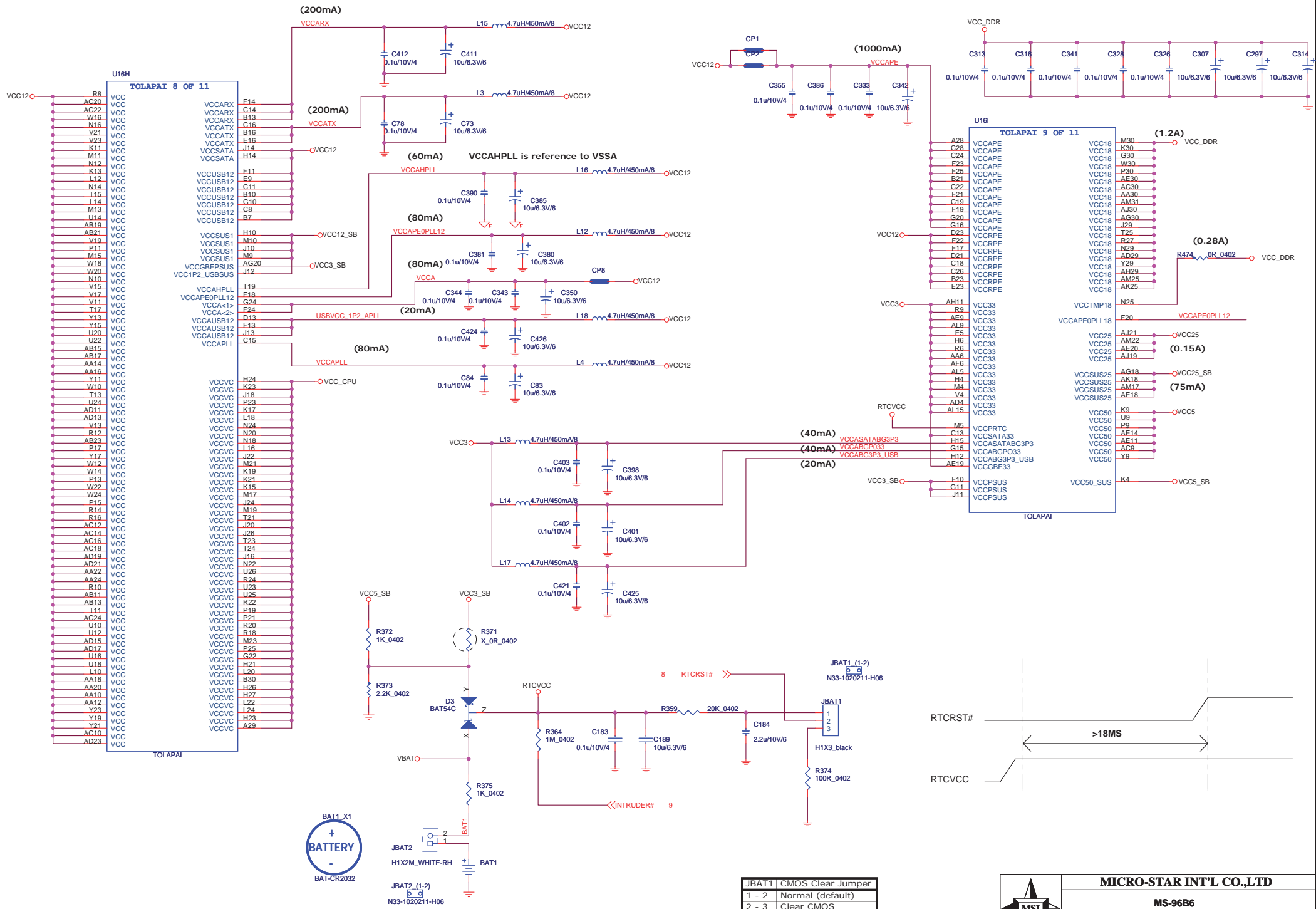
THIS PULLDOWN ENABLES LEB
 IRQ MODE WHEN POWER OK GOES HIGH
 0 = GPIO IRQ CAPABILITY ENABLED
 1 = GPIO IRQ CAPABILITY DISABLED
 (DEFAULT WITH INTERNAL PULL-UP)

GP16 Strap:
 0=IICH does not invert A16
 1=IICH inverts A16 on some BIOS cycles(default)

MICRO-STAR INT'L CO.,LTD

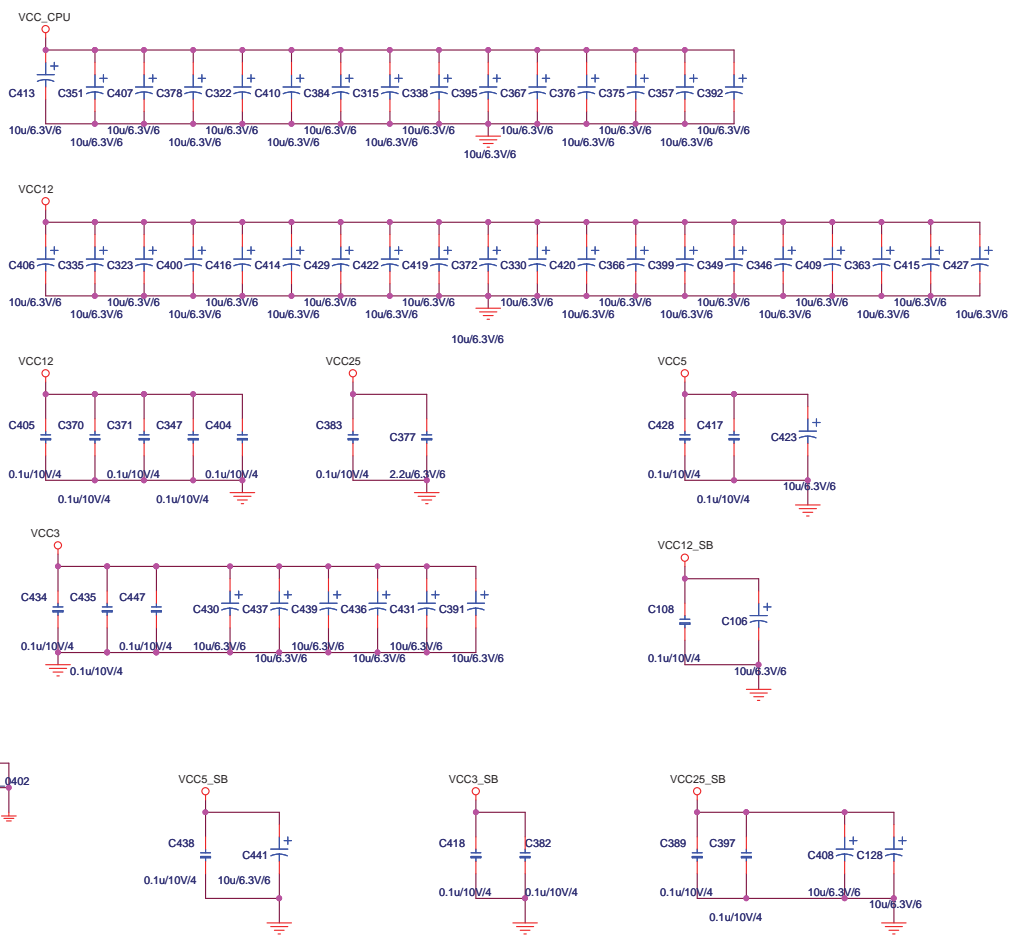
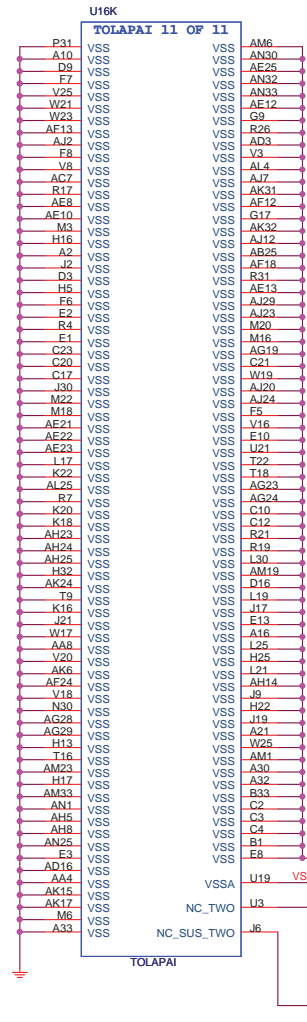
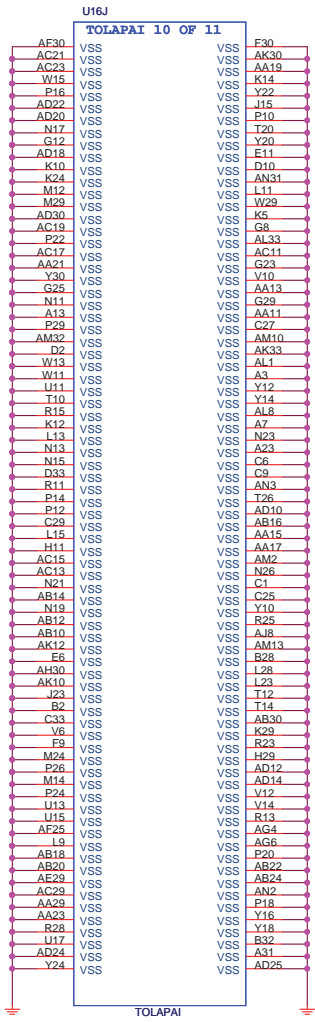
MS-96B6


Size	Document Description	Rev
Custom	Tolapai LEB/ GPIO/ UART	0B
Date: Saturday, December 20, 2008		Sheet 12 of 43



JBAT1	CMOS Clear Jumper
1 - 2	Normal (default)
2 - 3	Clear CMOS

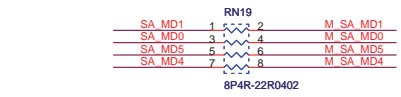
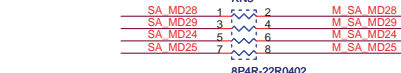
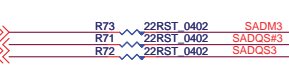
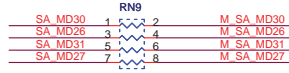
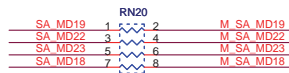
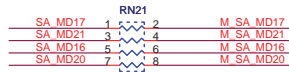
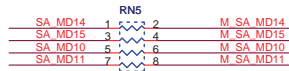
MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size	Document Description	Rev
Custom	Tolapai VCC	0B
Date: Saturday, December 20, 2008	Sheet 13 of 43	



			MICRO-STAR INT'L CO.,LTD	
			MS-96B6	
Size Custom	Document Description Tolapai GND		Rev 0B	
Date: Saturday, December 20, 2008		Sheet 14 of 43		

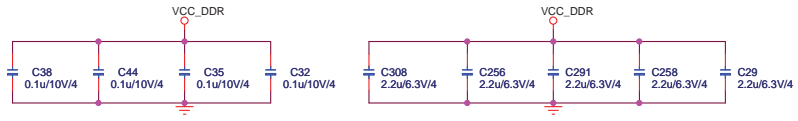
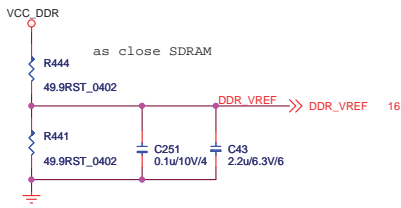
DDRII-667D 5-5-5 (128M X 8 bit)

11,16,17 SA_MA[13..0] <<> SA_MA[13..0]
 11 SA_MD[31..0] <<> SA_MD[31..0]

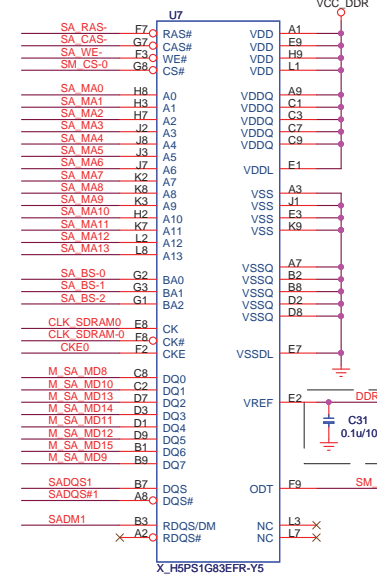
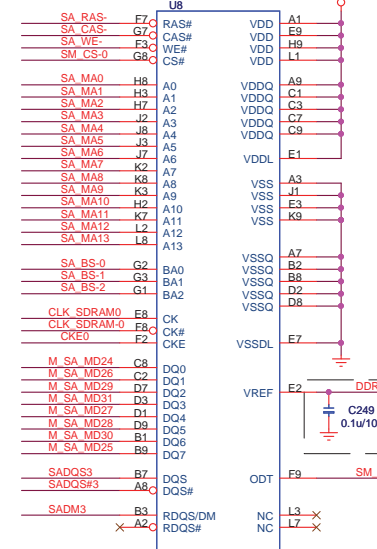
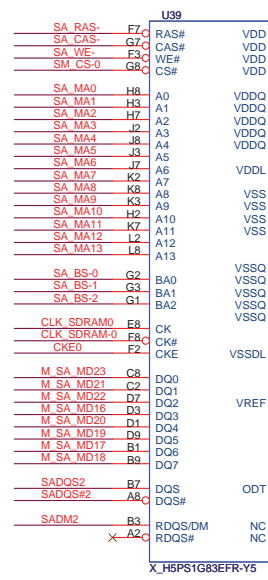
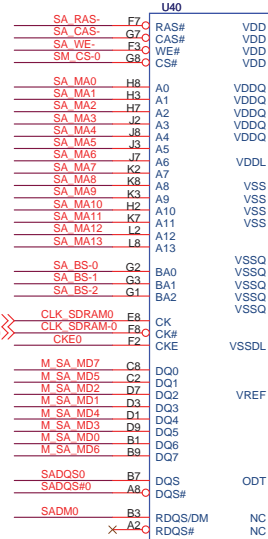


11,16,17 SA_BS-0 >> SA_BS-0
 11,16,17 SA_BS-1 >> SA_BS-1
 11,16,17 SA_BS-2 >> SA_BS-2
 11,16,17 SA_WE- >> SA_WE-
 11,16,17 SA_CAS- >> SA_CAS-
 11,16,17 SA_RAS- >> SA_RAS-

11,16,17 CKE0 >> CKE0
 11,16,17 SM_ODT0 >> SM_ODT0
 11,16,17 SM_CS-0 >> SM_CS-0



Layout note: Place capacitors between and near DDR Down if possible.



MICRO-STAR INT'L CO.,LTD

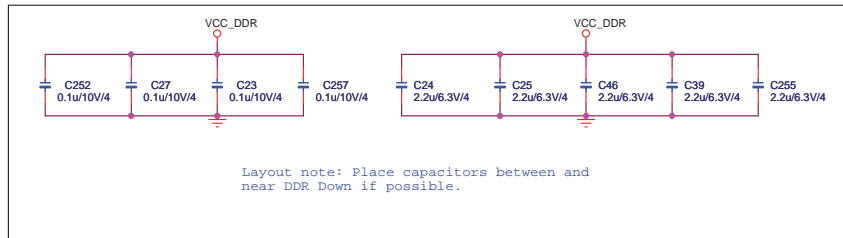
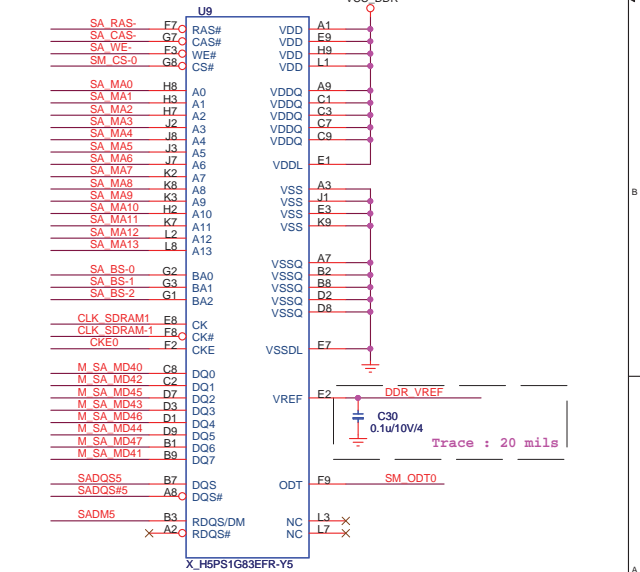
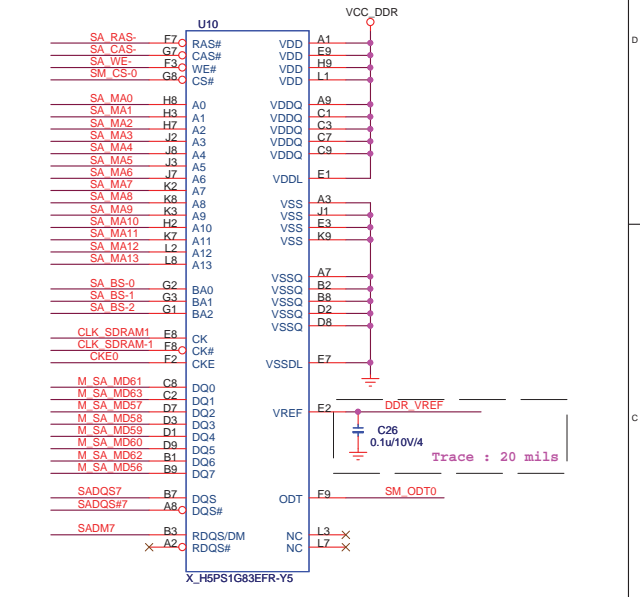
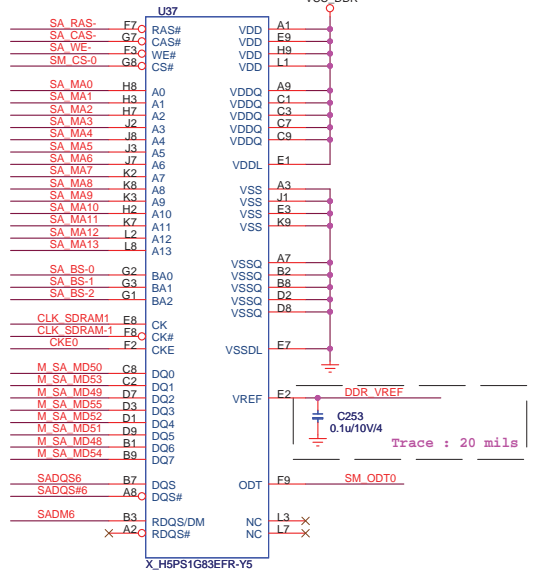
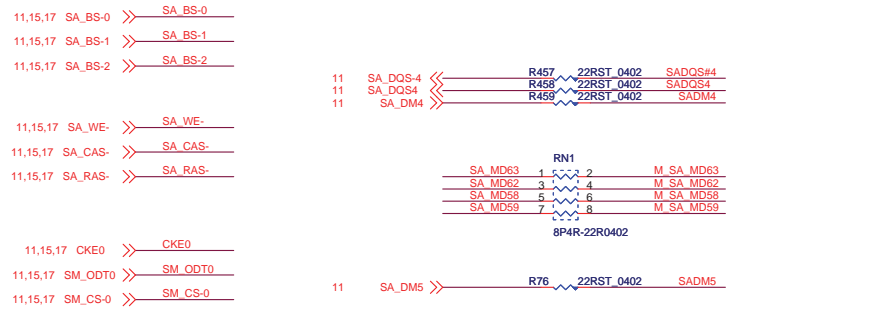
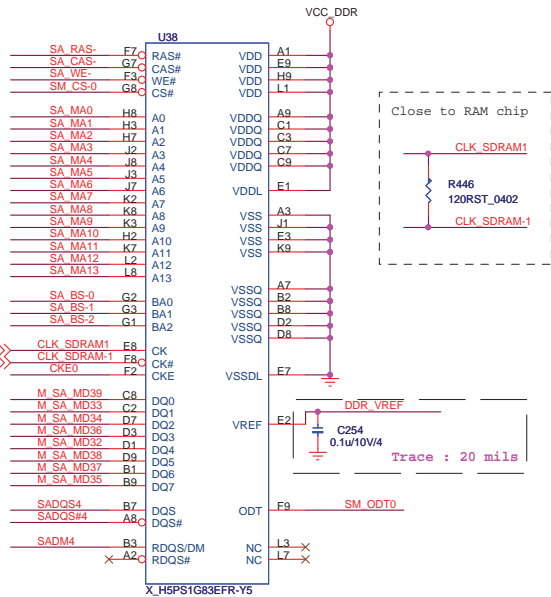
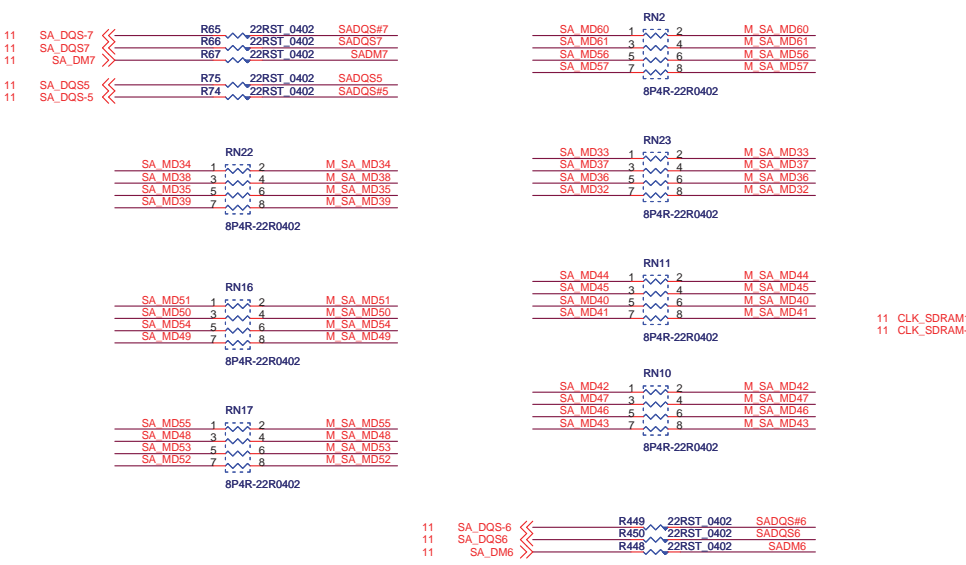
MS-96B6

Size Custom Document Description **DDRII-667 Memory Down-1** Rev 0B

Date: Saturday, December 20, 2008 Sheet 15 of 43

DDRII-667D 5-5-5 (128M X 8 bit)

11,15,17 SA_MA[13..0] <<> SA_MA[13..0]
 11 SA_MD[63..32] <<> SA_MD[63..32]

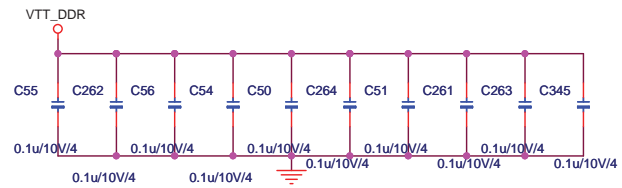
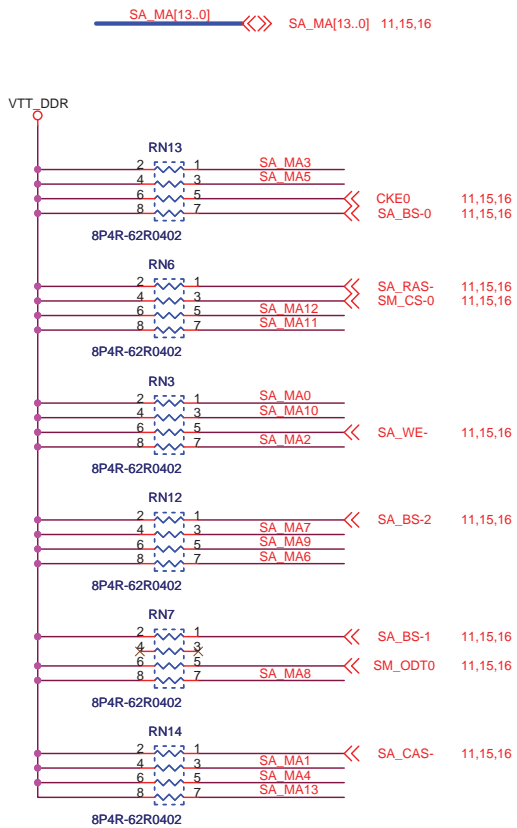


MICRO-STAR INT'L CO.,LTD


MS-96B6

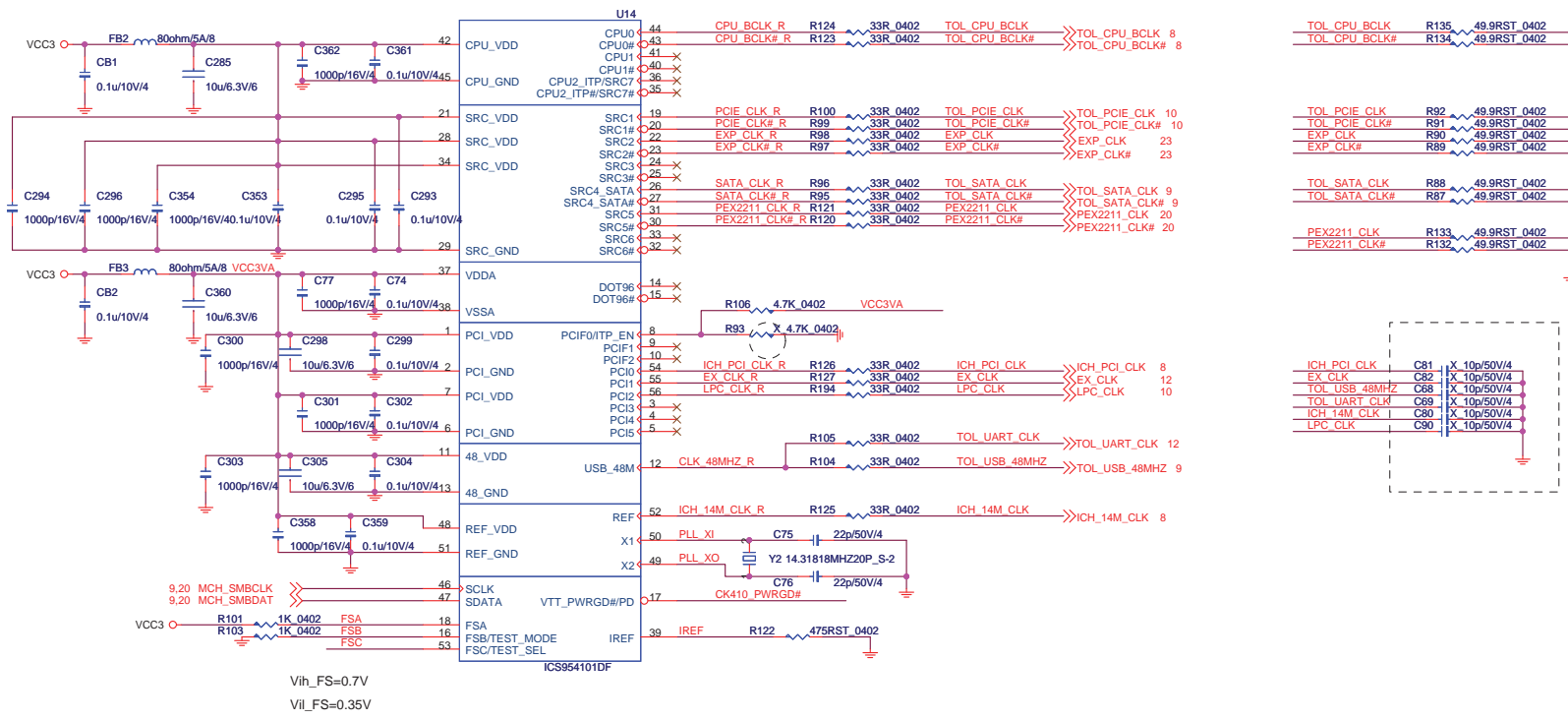
Size Custom Document Description **DDRII-667 Memory Down-2** Rev 0B

Date: Saturday, December 20, 2008 Sheet 16 of 43



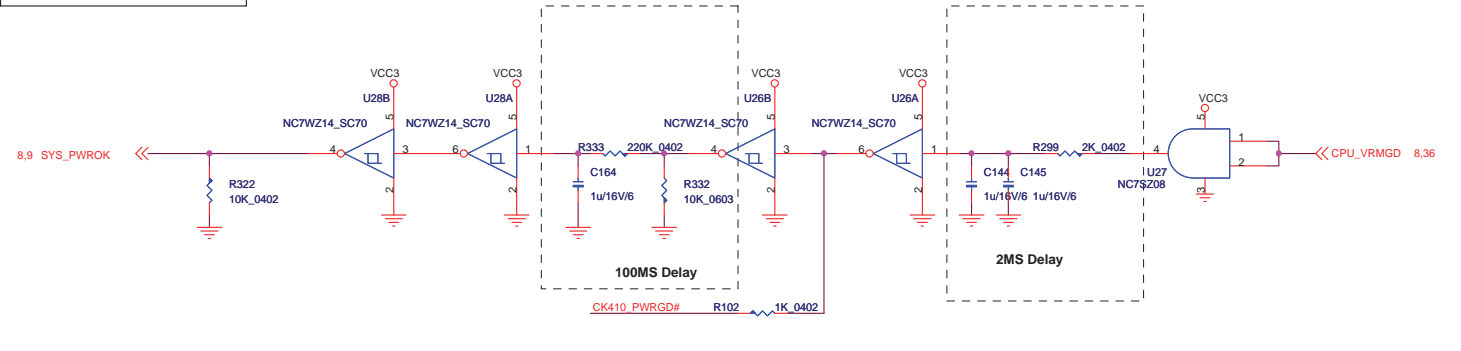
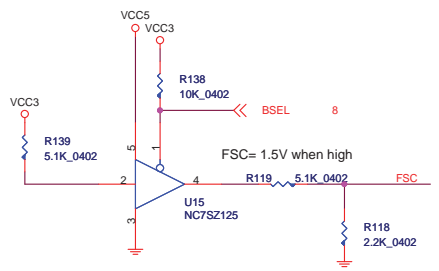
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V.

			MICRO-STAR INT'L CO.,LTD	
			MS-96B6	
Size B	Document Description DDRII Termination			Rev 0B
Date: Saturday, December 20, 2008		Sheet 17 of 43		



Vih_FS=0.7V
Vil_FS=0.35V

FSB	BSEL	BCLK	FSA	FB	FSC
400	0	100MHz	1	0	1
533	1	133MHz	1	0	0



100MS Delay 2MS Delay
SYS_PWROK CK410 BSEL LATCH CPU VRMGD

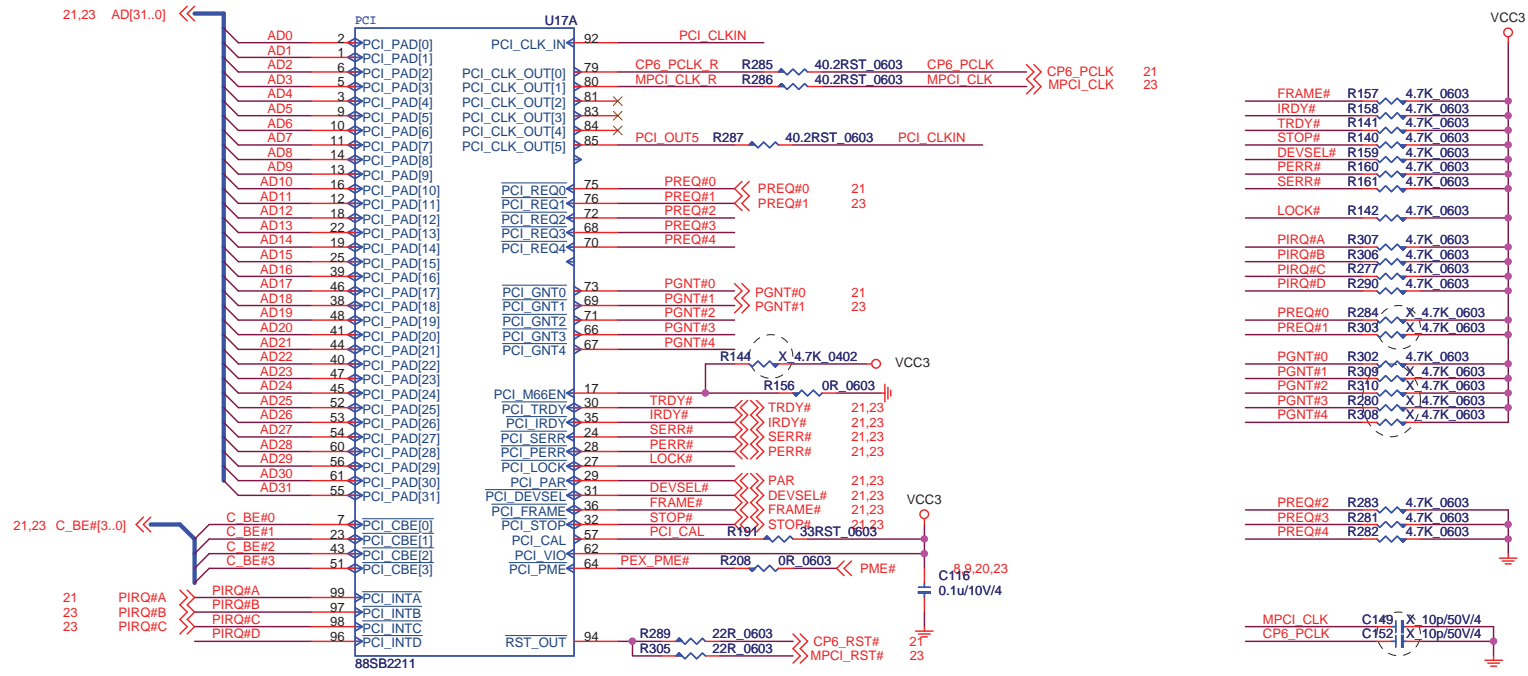
<http://laptop-motherboard-schematic.blogspot.com/>

MICRO-STAR INT'L CO.,LTD

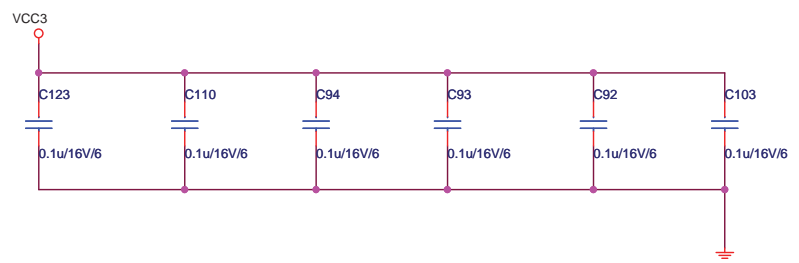
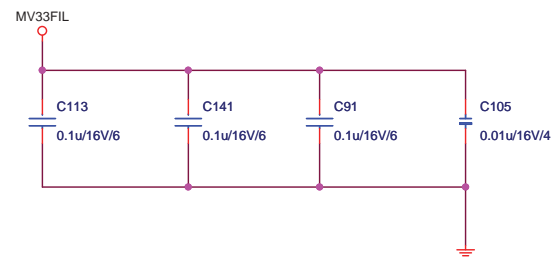
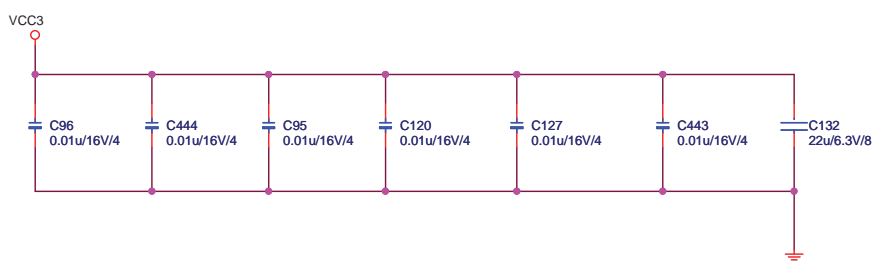
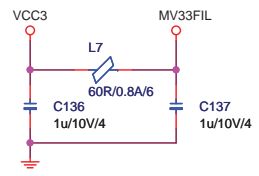
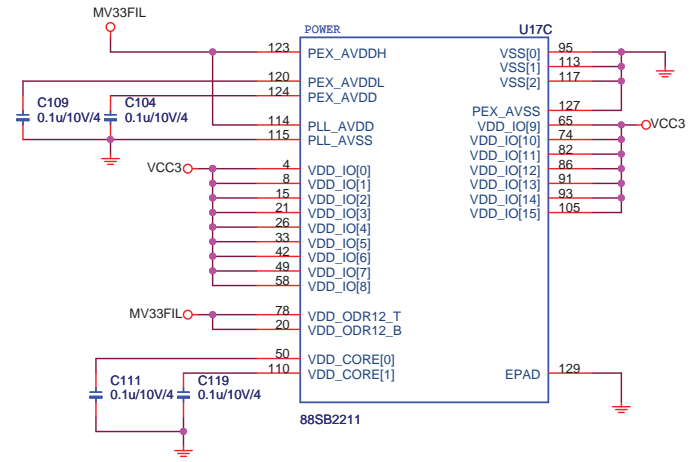
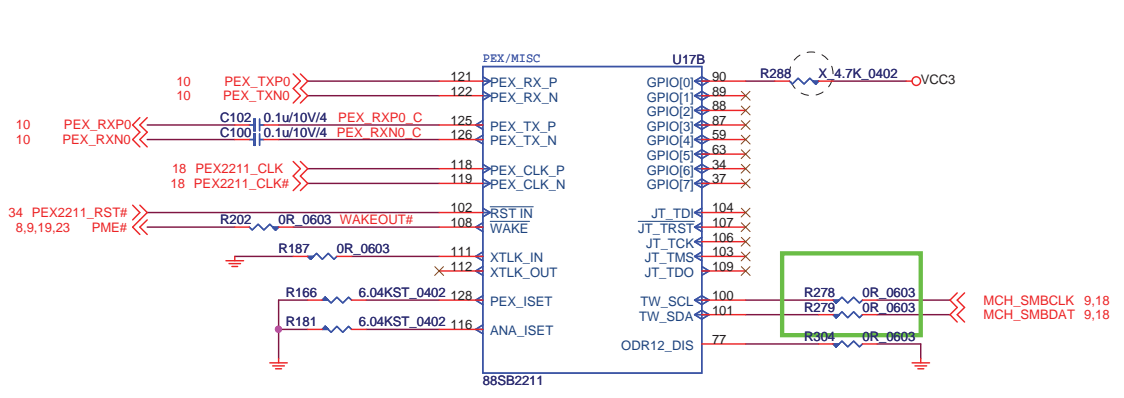
MS-96B6

Size Custom Document Description **CK410 Clock Gen** Rev 0B

Date: Saturday, December 20, 2008 Sheet 18 of 43

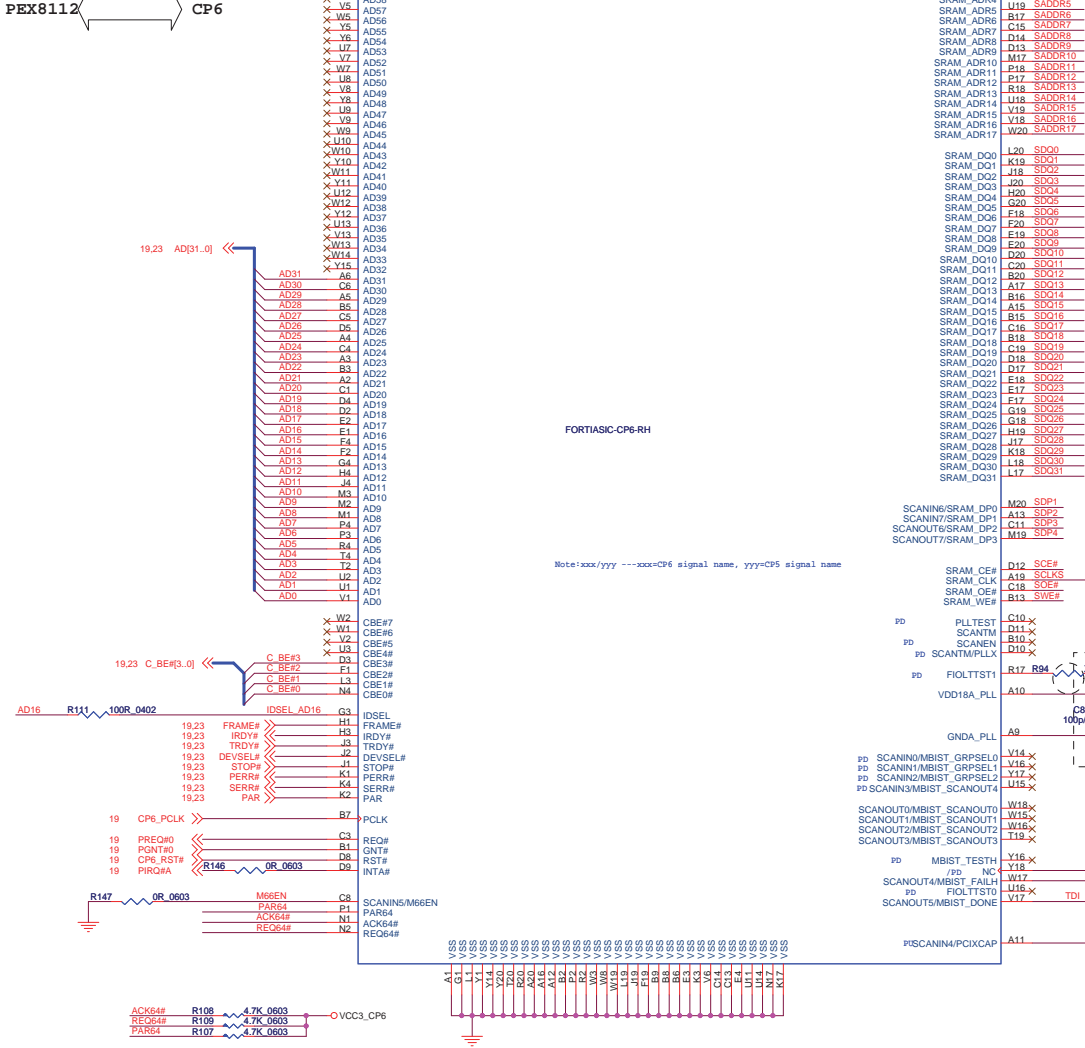


MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size B	Document Description	Rev 0B
	Marvell 88SB2211-1	
Date: Saturday, December 20, 2008 Sheet 19 of 43		



MSI		
MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size B	Document Description Marvell 88SB2211-2	Rev 0B
Date: Saturday, December 20, 2008	Sheet 20 of 43	

PCI 32/33
PEX8112 <-> CP6

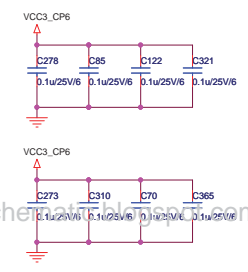
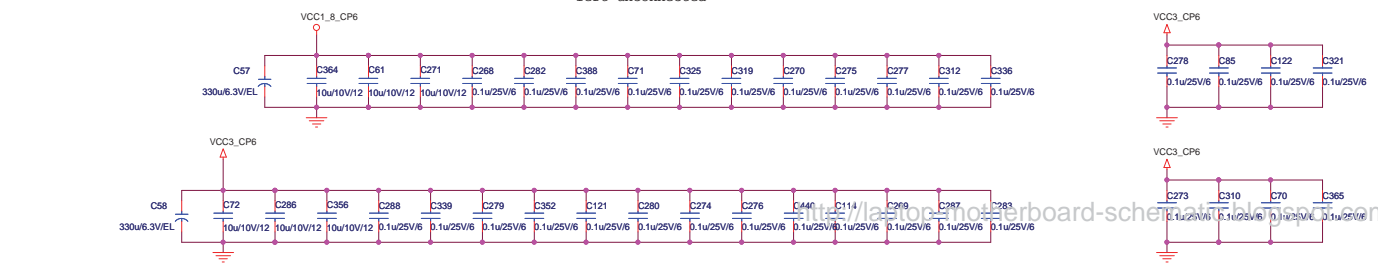
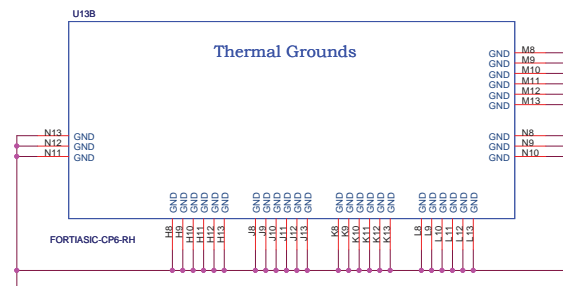
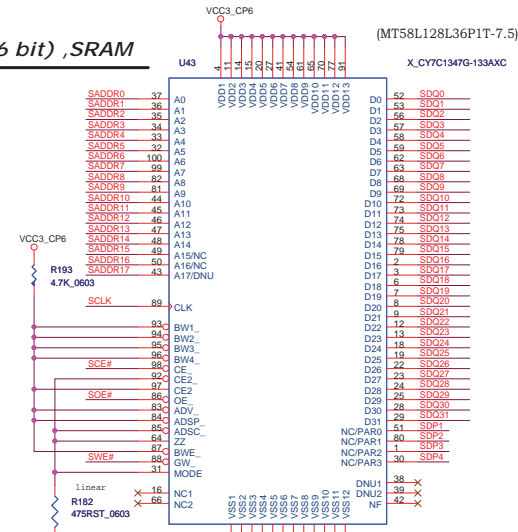


Power -ON: VDDI (for internal) -> VDEE (for external) -> Signal
 Power -OFF: signal -> VDEE (for external) -> VDDI (for internal)

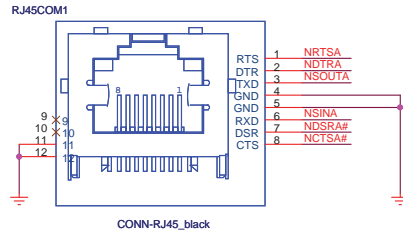
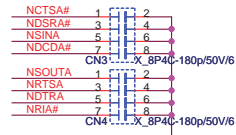
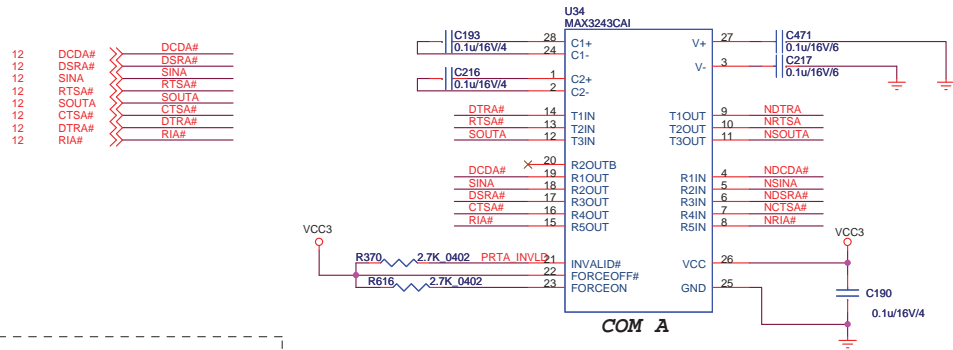
Note: TDI/TMS/TCK to be pulled up when not used, while TRST# to be left unconnected

PCI control signals always require pull-up resistors on the system board (not the add-in card) to ensure that they contain stable values when no agent is actively driving the bus. This includes **FRAME#**, **TRDY#**, **IRDY#**, **DEVSEL#**, **STOP#**, **SERR#**, **PERR#**, **LOCK#**, **INTA#**, **INTB#**, **INTC#**, **INTD#**, **REQ64#**, and **ACK64#**. The point-to-point and shared 32-bit signals do not require pull-ups; bus parking ensures their stability. Refer to Section 3.8.1. for special requirements for terminating **AD[63:32]**, **C/BE[7:4]#**, and **PAR64**. Refer to Section 4.3.7. for pull-up and decoupling requirements for **PRSENT1#** and **PRSENT2#**. Refer to Section 7.7.7. for pull-up and decoupling requirements for **M66EN**.

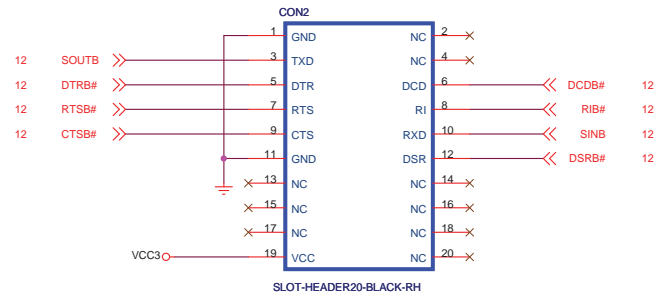
4Mb(128K X 36 bit) ,SRAM



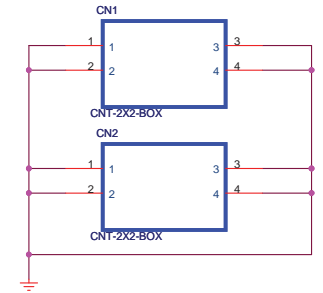
SERIAL PORT 1



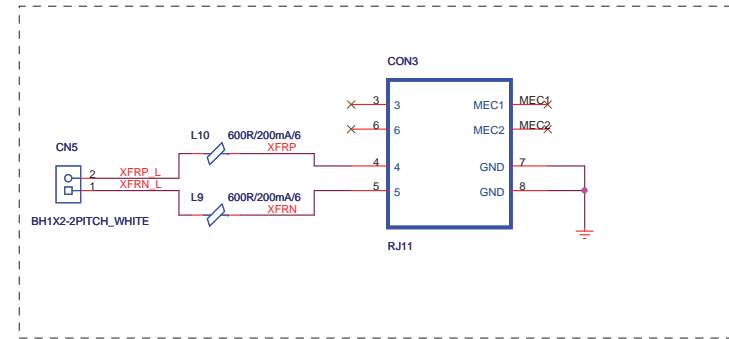
MODEM HEADER



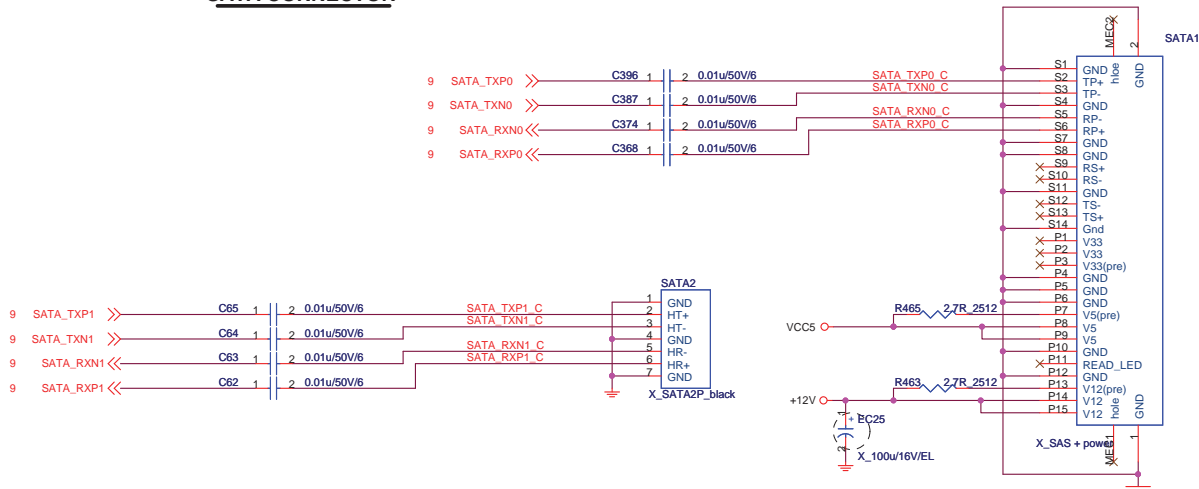
MODEM FIX



RJ-11



SATA CONNECTOR



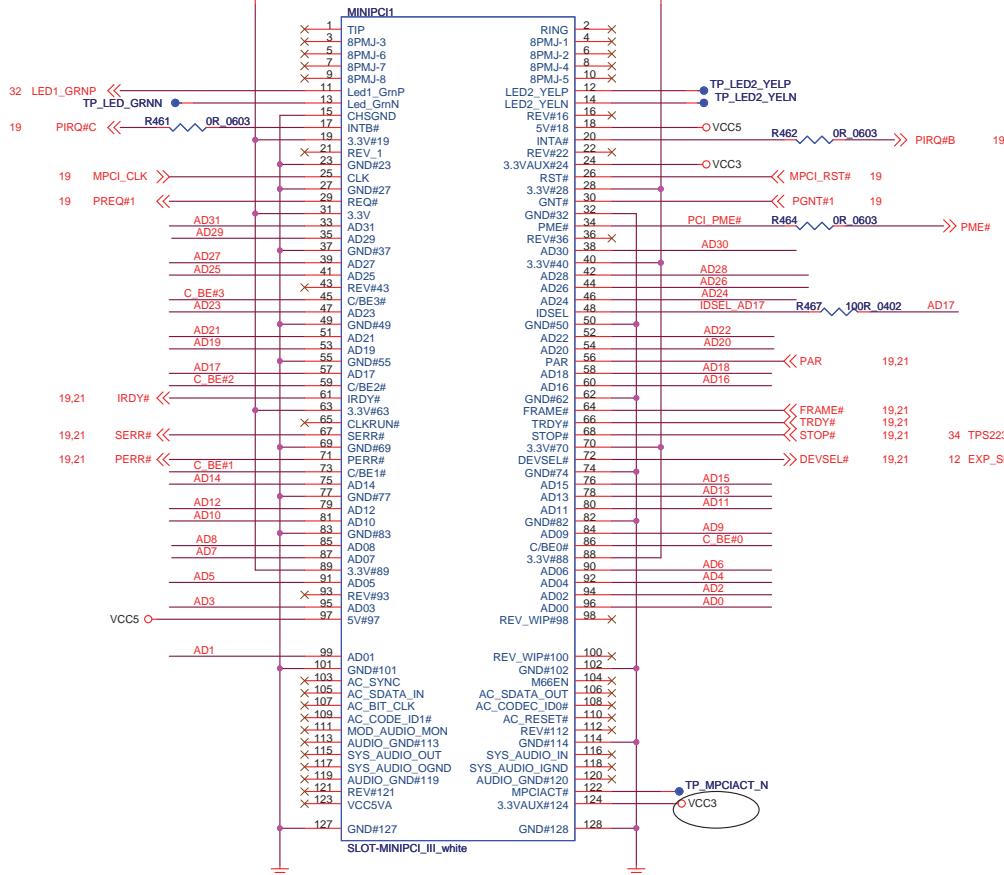
<http://laptop-motherboard-schematic.blogspot.com/>



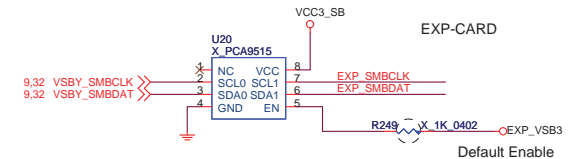
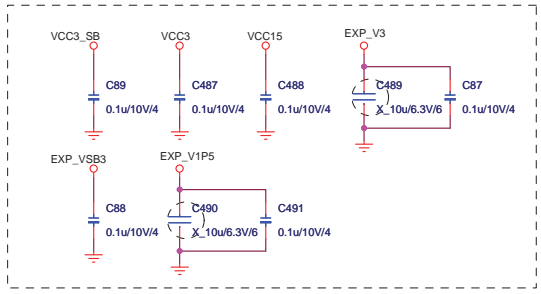
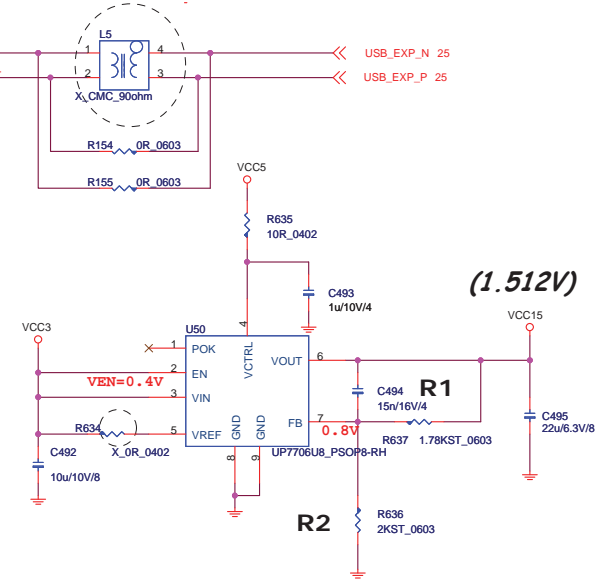
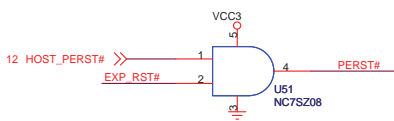
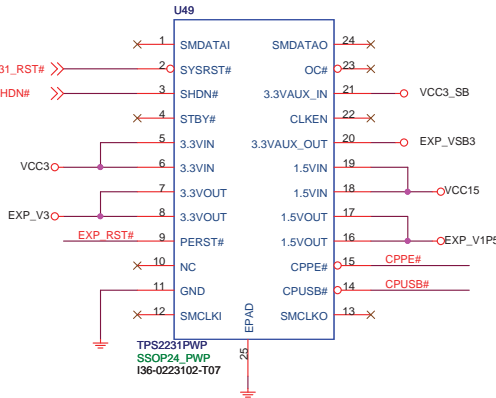
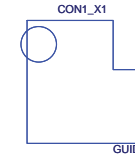
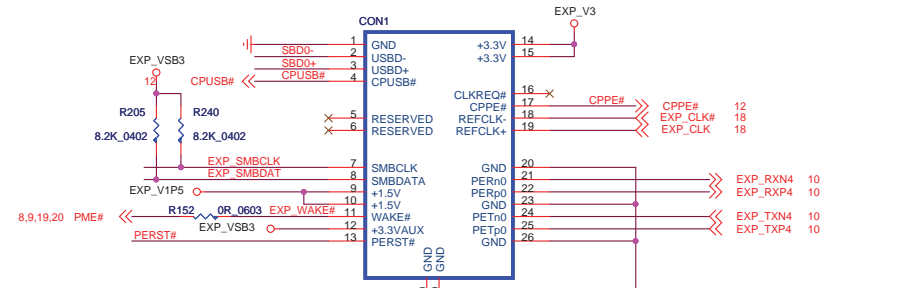
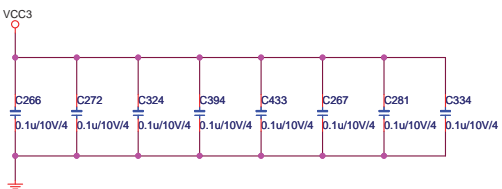
MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description Com Port/ Modem/ SATA Con.	Rev 0B
Date: Saturday, December 20, 2008	Sheet 22	of 43

19,21 AD[31..0] << AD[31..0]
 19,21 C_BE#[3..0] << C_BE#[3..0]

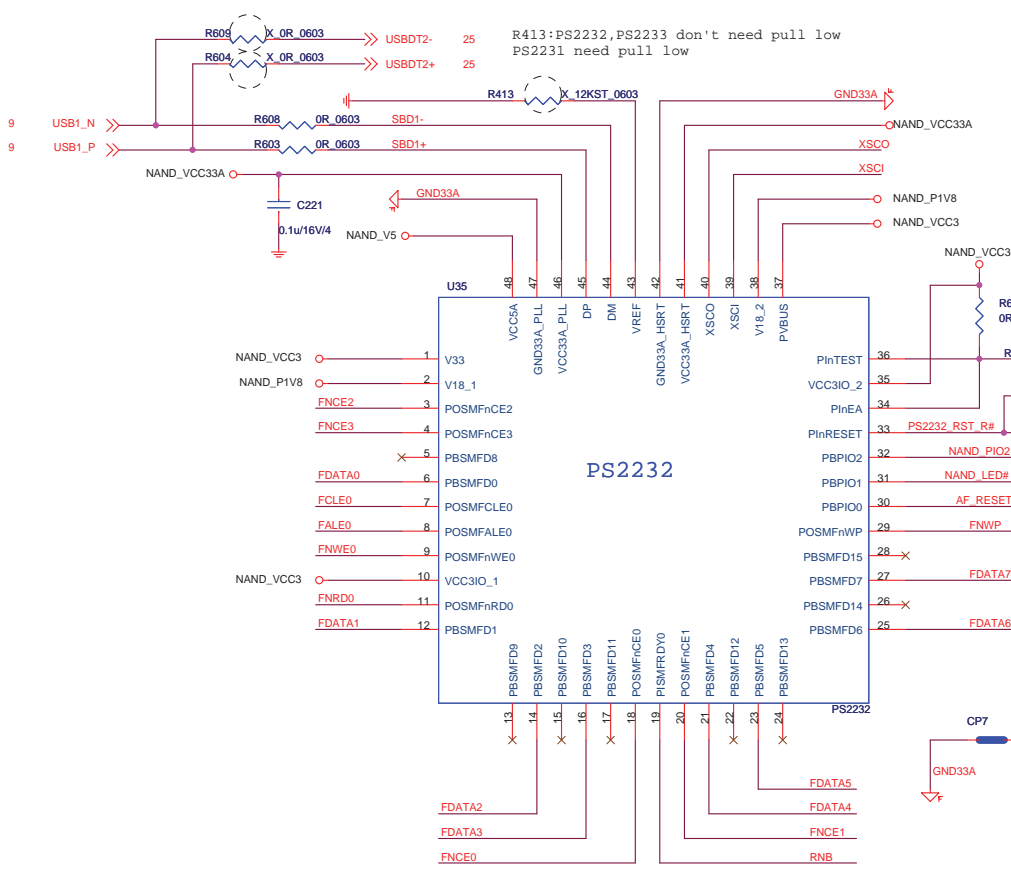
Mini PCI SOCKET



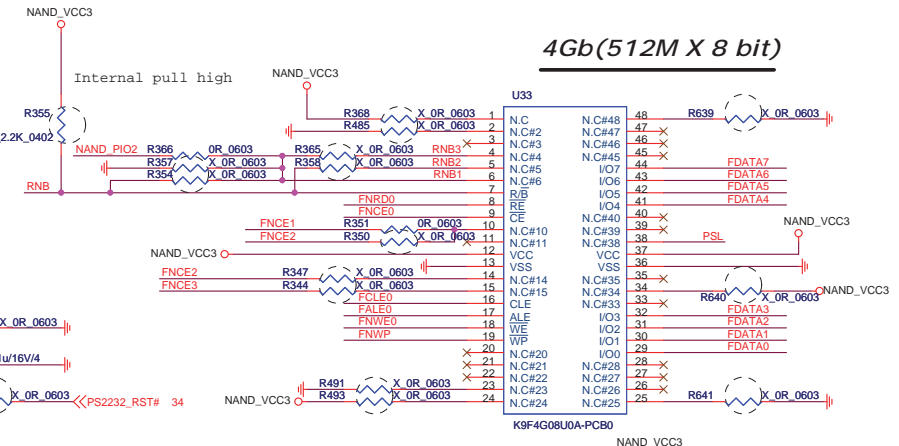
IDSEL = AD17
MASTER = PREQ#1
PIRQ#BC



MICRO-STAR INT'L CO.,LTD			
MS-96B6			
Size	Document Description		Rev
Custom	Express Card/Mini-PCI		0B
Date:	Saturday, December 20, 2008	Sheet	23 of 43



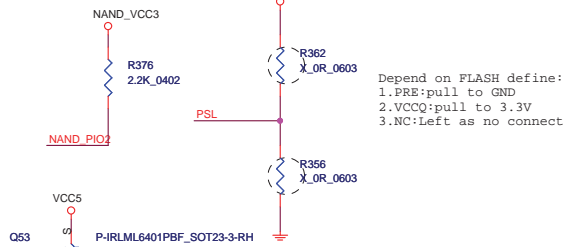
R413:PS2232,PS2233 don't need pull low
PS2231 need pull low



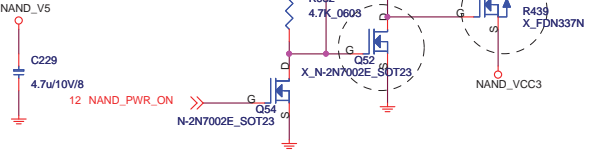
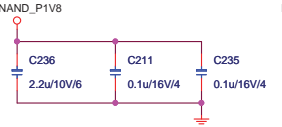
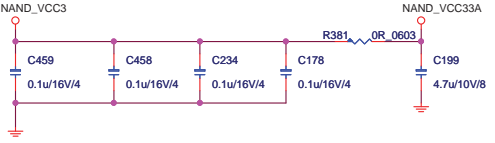
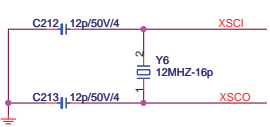
4Gb(512M X 8 bit)



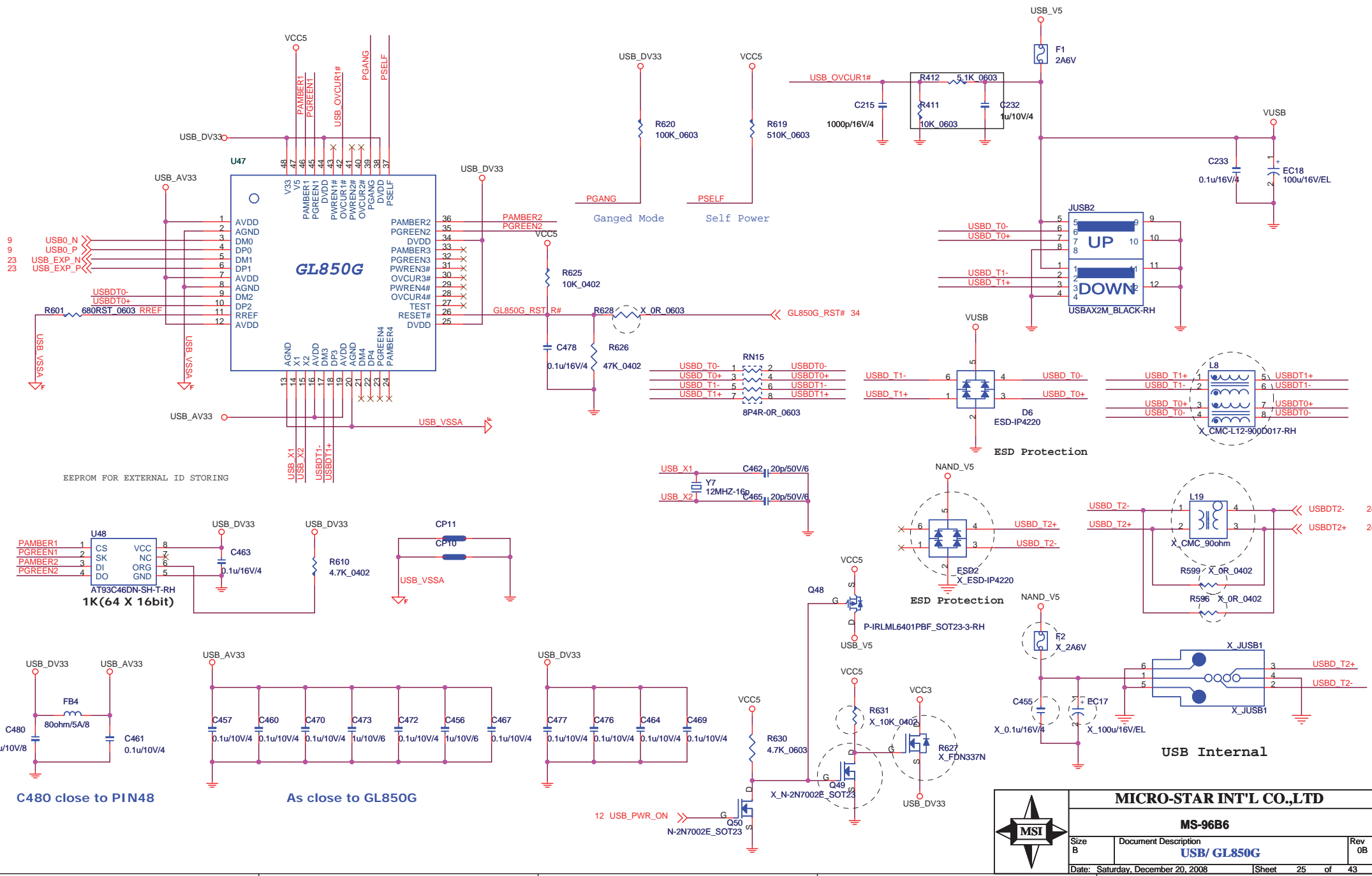
ESD Protection



Depend on FLASH define:
1.PRE:pull to GND
2.VCCQ:pull to 3.3V
3.NC:left as no connect



MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description PS2232/ NAND Flash	Rev 0B
Date:	Saturday, December 20, 2008	Sheet 24 of 43

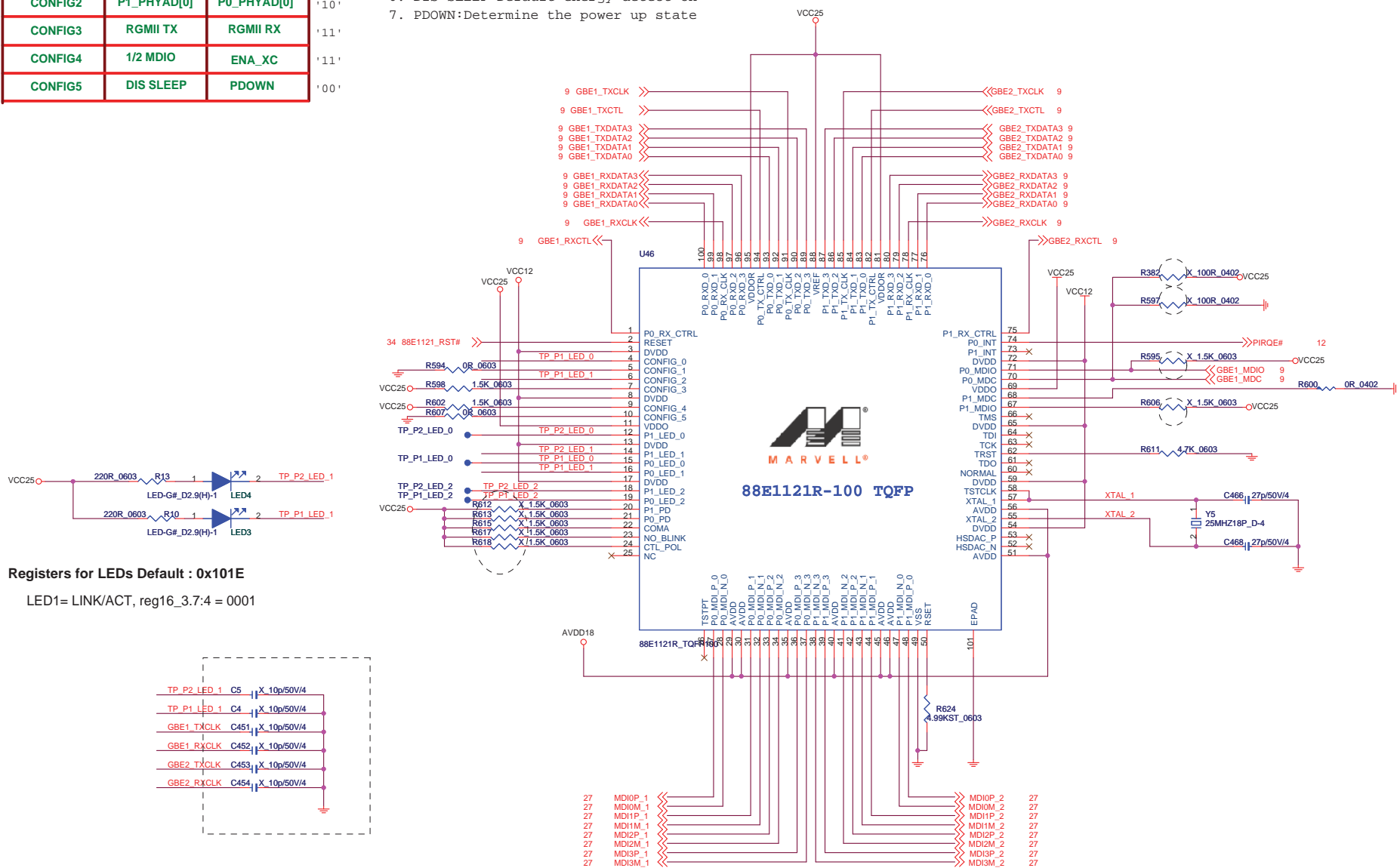


E1121R Pin To Configuration Mapping

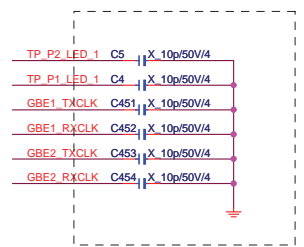
PIN	BIT [1]	BIT [0]
CONFIG0	PHYADR[2]	PHYADR[1]
CONFIG1	PHYADR[3]	PHYADR[4]
CONFIG2	P1_PHYAD[0]	P0_PHYAD[0]
CONFIG3	RGMII TX	RGMII RX
CONFIG4	1/2 MDIO	ENA_XC
CONFIG5	DIS SLEEP	PDOWN

Hardware Configuration

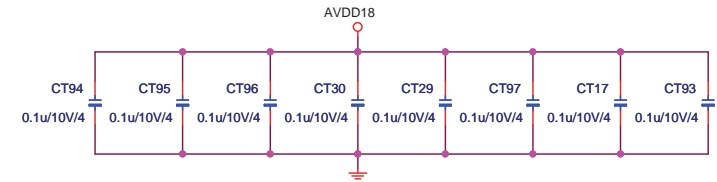
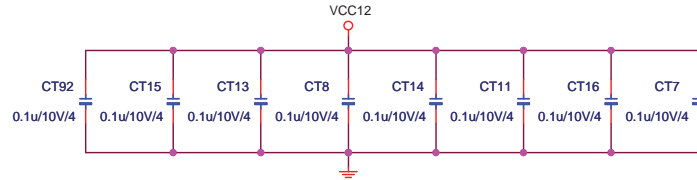
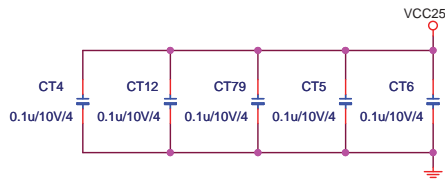
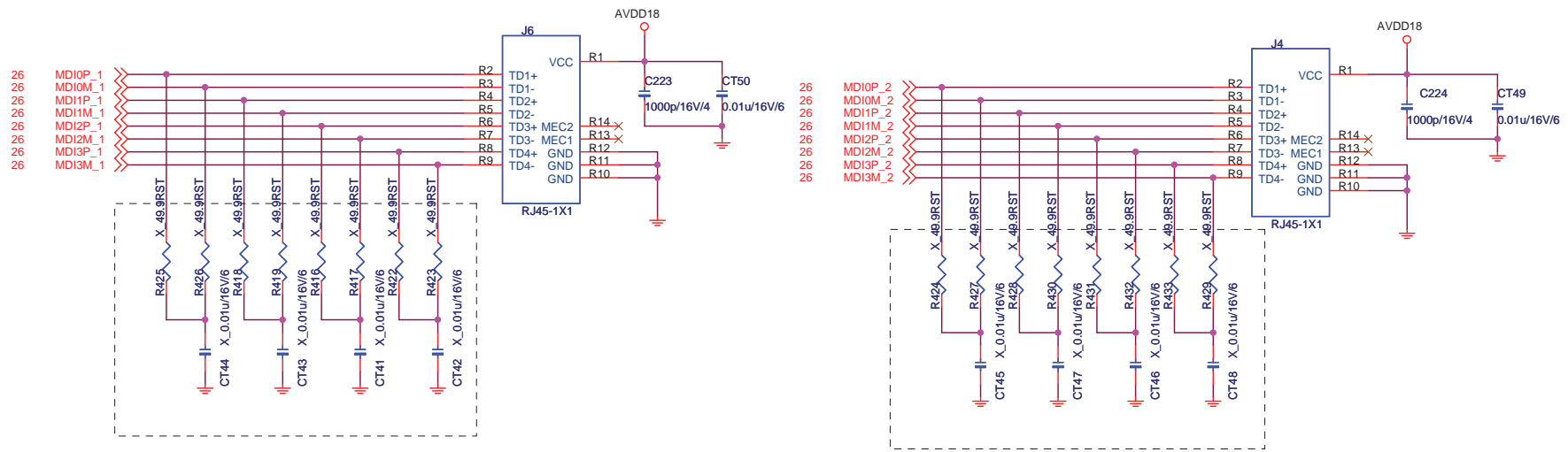
- PHY1/2 address:00010/00011
- RGMII_TX:Transmit clock internally delayed
- RGMII_RX:Receive clock transition when data stable
- 1/2 MDIO:Single MDC/MDIO shared for all ports
- ENA_XC:Enable Auto-Crossover
- DIS SLEEP:Default energy detect on
- PDOWN:Determine the power up state



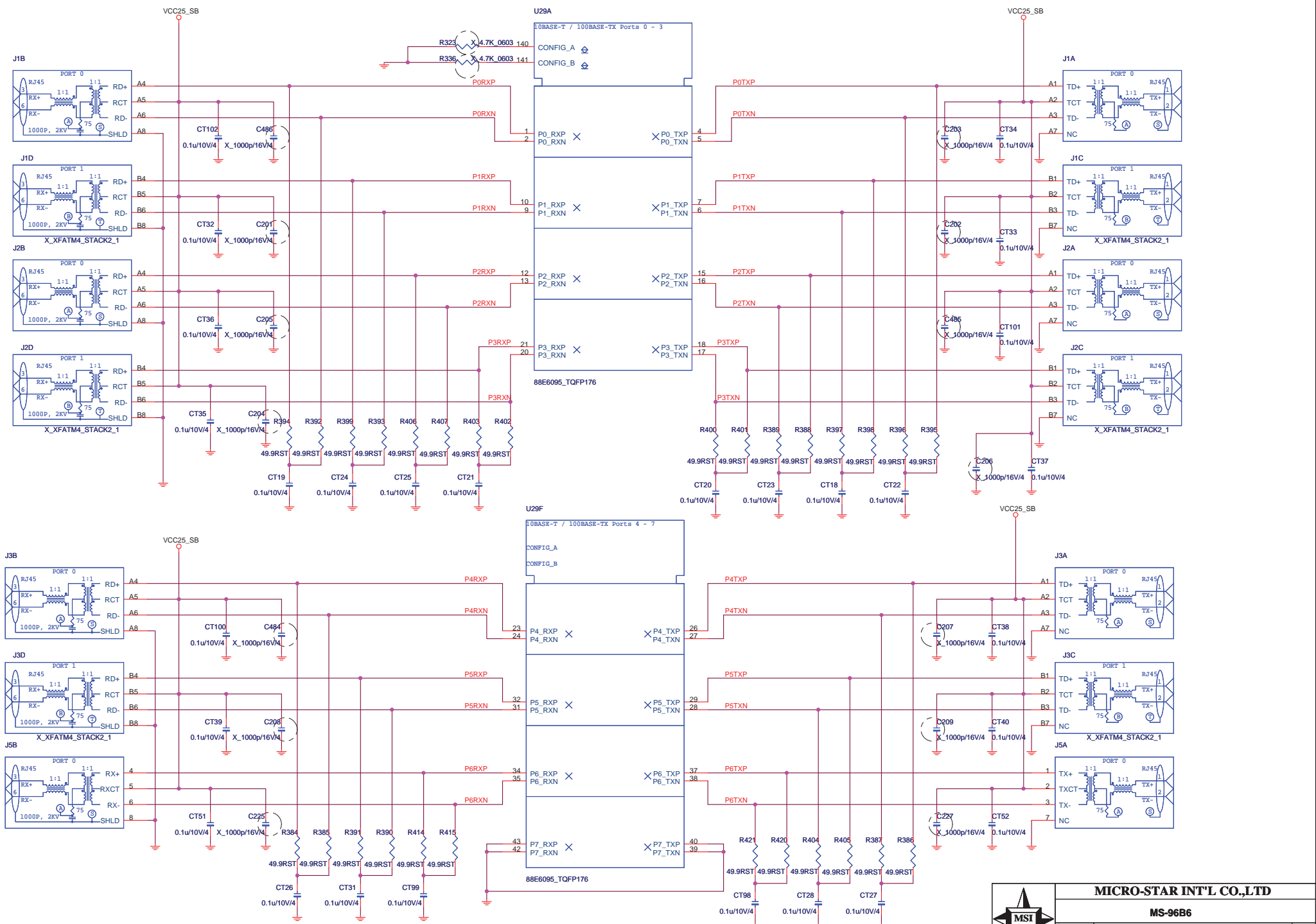
Registers for LEDs Default : 0x101E
 LED1= LINK/ACT, reg16_3:7:4 = 0001




MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description	Rev 0B
Marvell 88E1121R-1		
Date: Tuesday, December 23, 2008	Sheet 26 of 43	

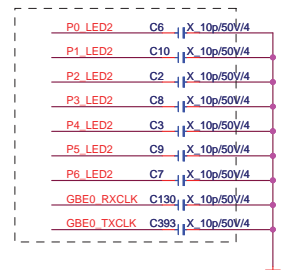
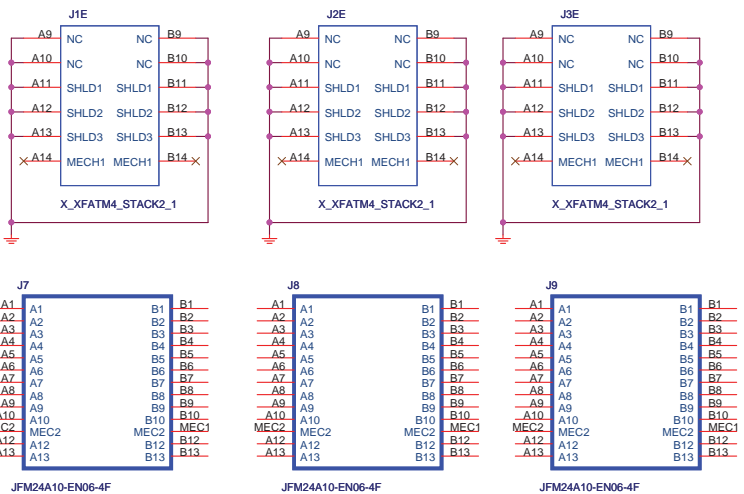
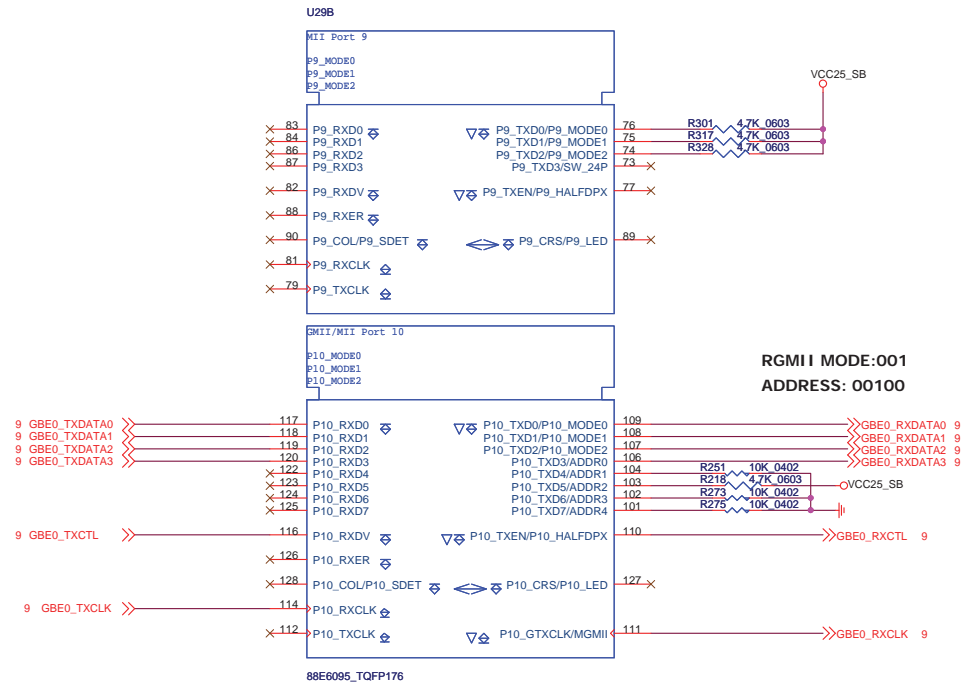
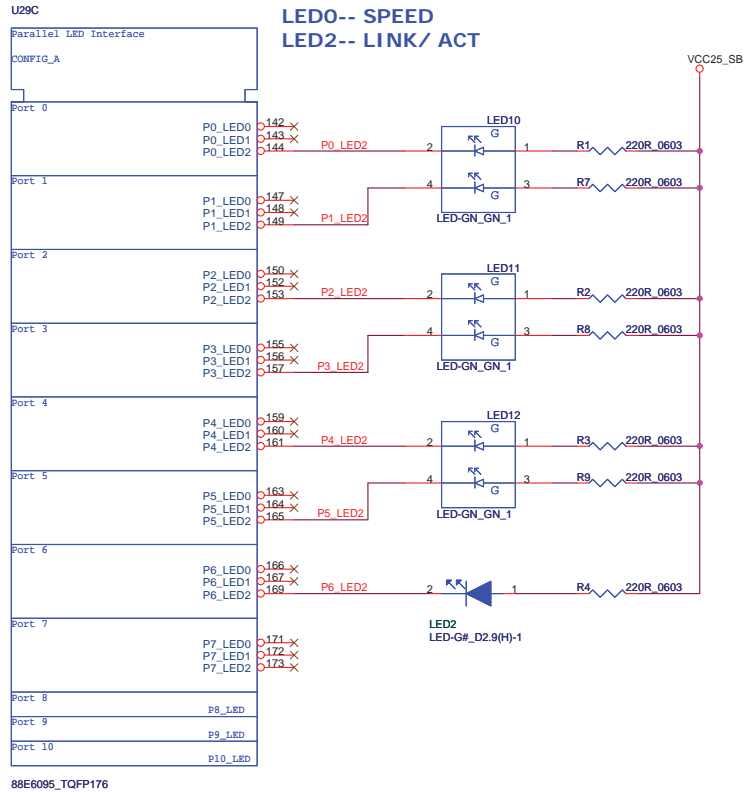


	MICRO-STAR INT'L CO.,LTD		
	MS-96B6		
	Size B	Document Description Marvell 88E1121R-2	Rev 0B
Date: Tuesday, December 23, 2008		Sheet 27 of 43	



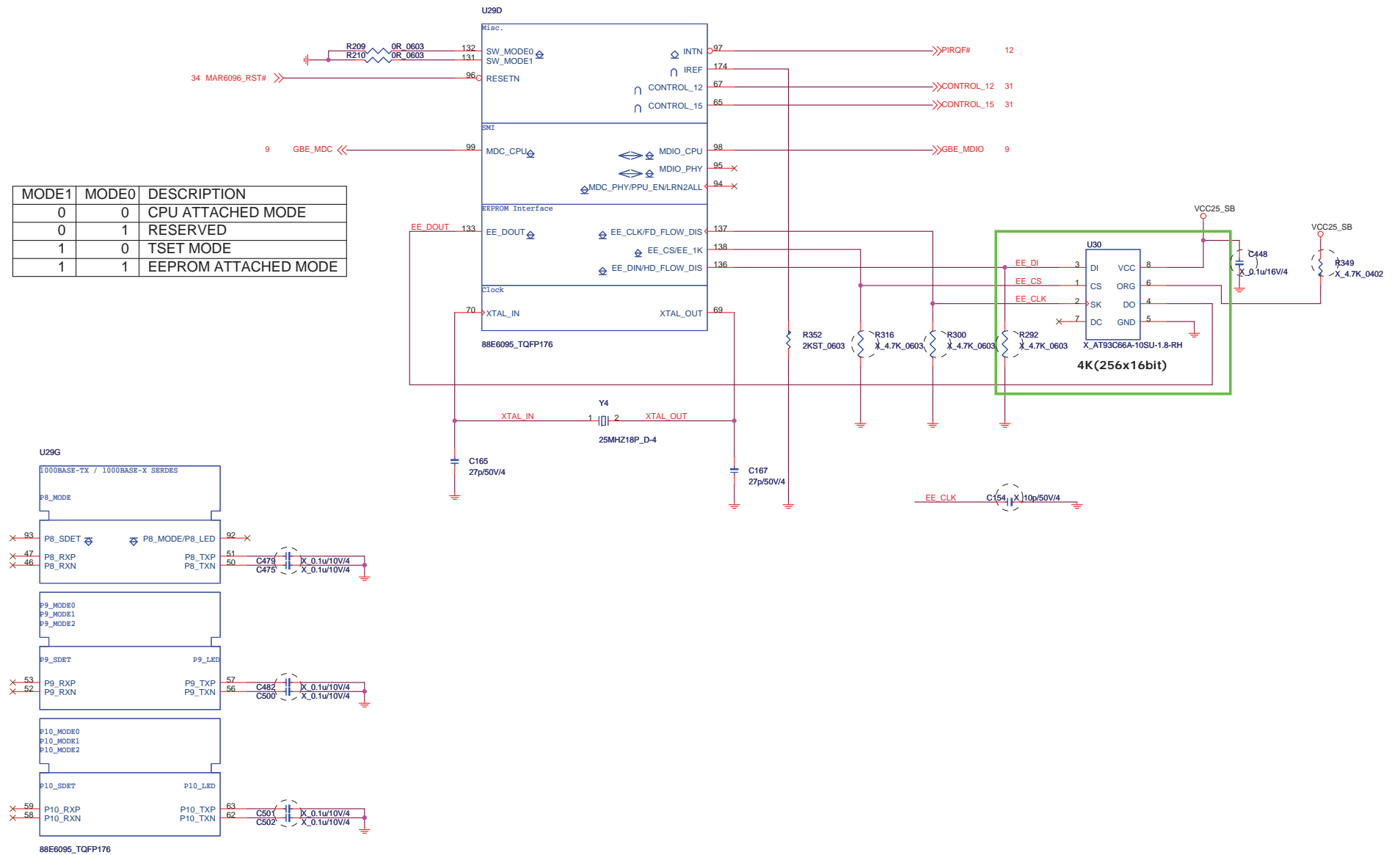
<http://laptop-motherboard-schematic.blogspot.com/>


			MICRO-STAR INT'L CO.,LTD	
			MS-96B6	
Size	Document Description			Rev
Custom	Marvell 88E6096A2-1			0B
Date: Tuesday, December 23, 2008		Sheet 28 of 43		

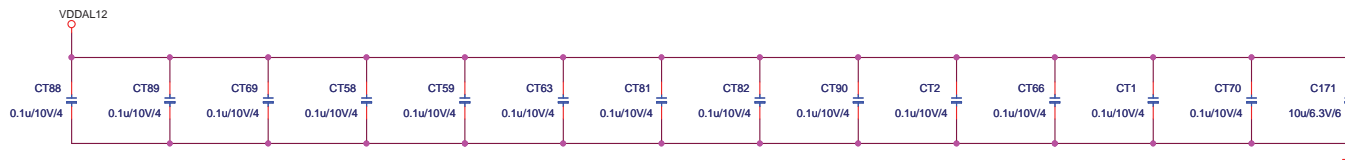
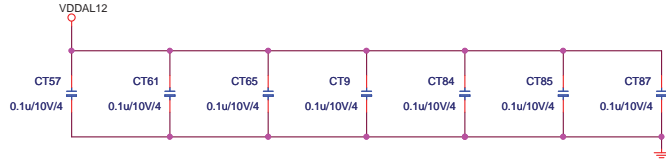
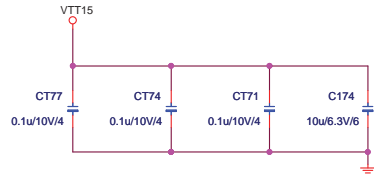
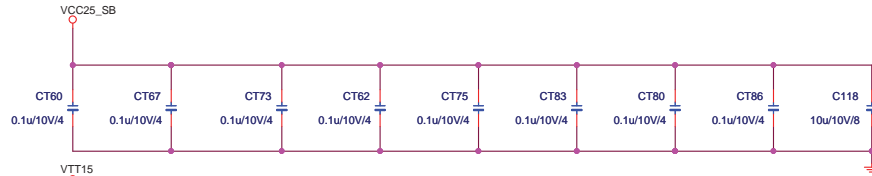
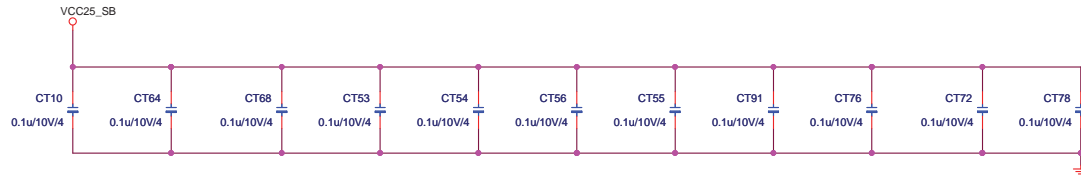
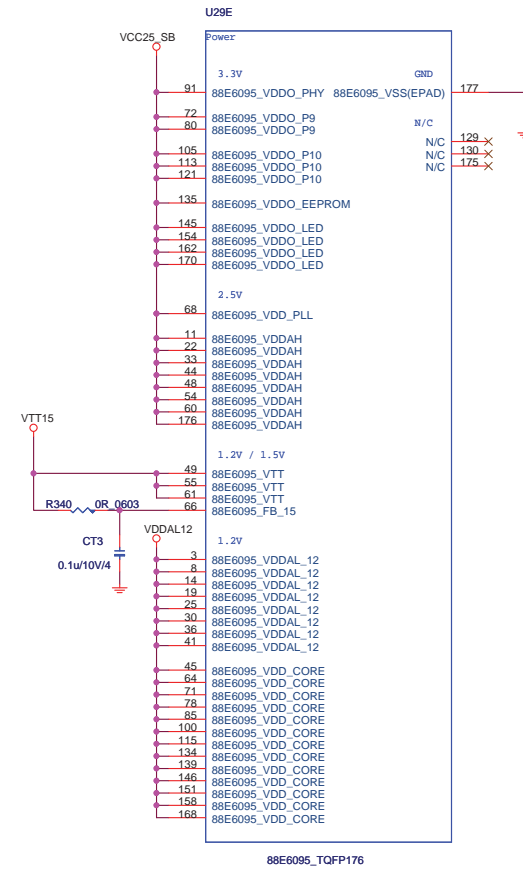
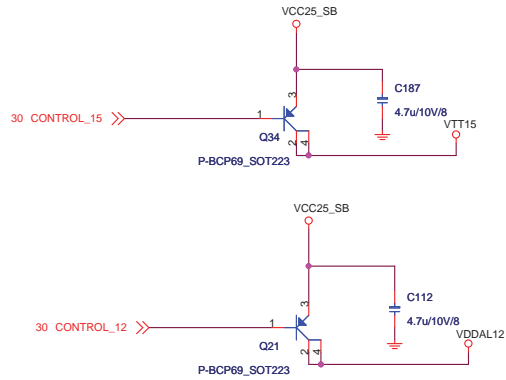


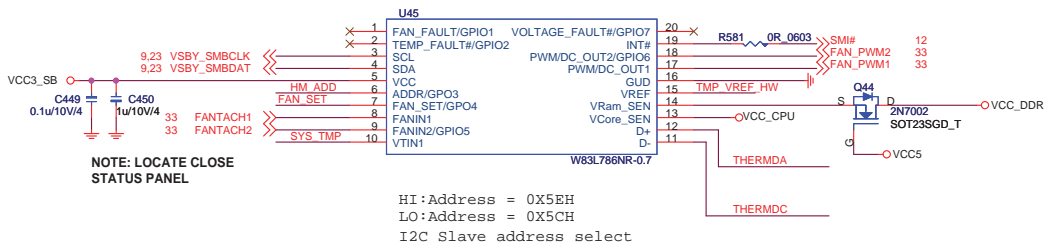
MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description Marvell 88E6096A2-2	Rev 0B
Date: Tuesday, December 23, 2008	Sheet 29	of 43

MODE1	MODE0	DESCRIPTION
0	0	CPU ATTACHED MODE
0	1	RESERVED
1	0	TSET MODE
1	1	EEPROM ATTACHED MODE



	MICRO-STAR INT'L CO.,LTD		
	MS-96B6		
Size Custom	Document Description Marvell 88E6096A2-3	Rev 0B	
Date: Saturday, December 20, 2008	Sheet	30	of 43



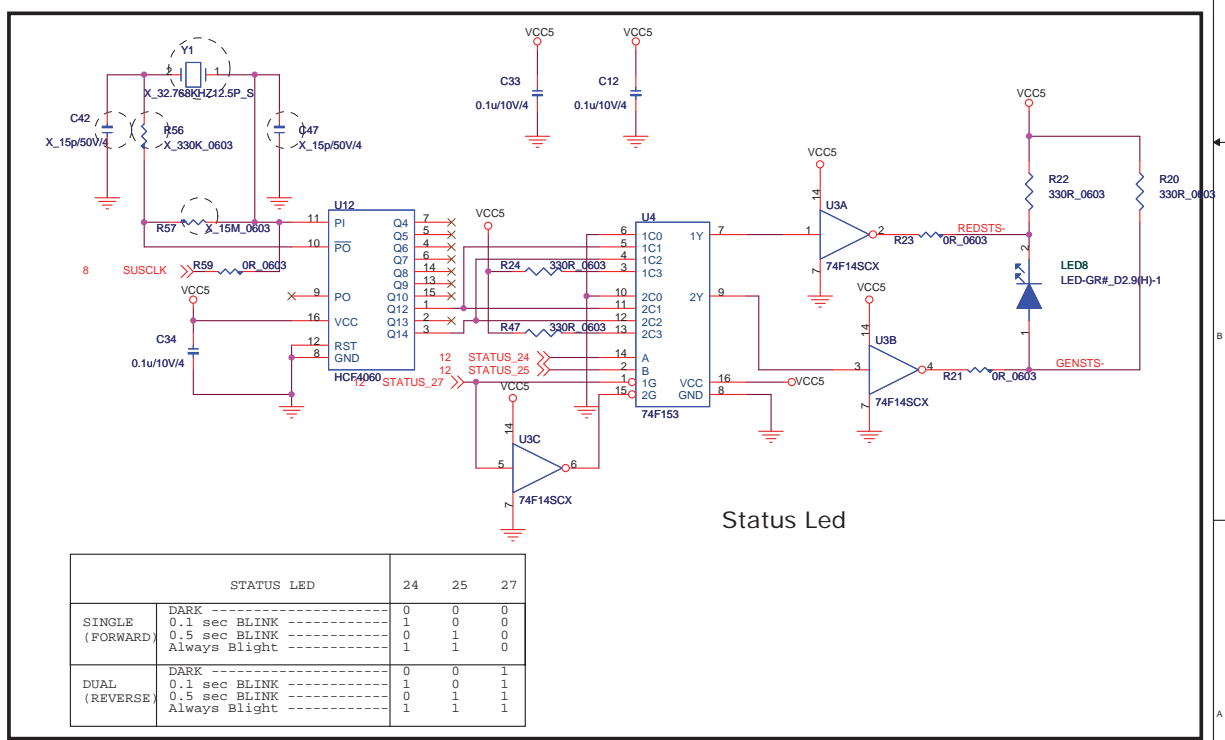
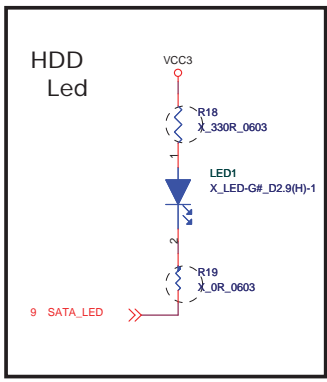
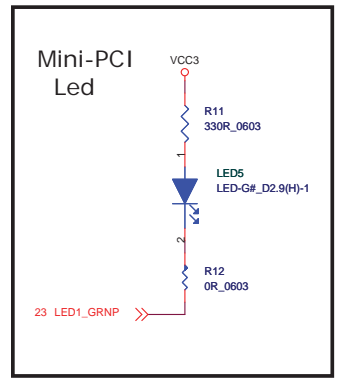
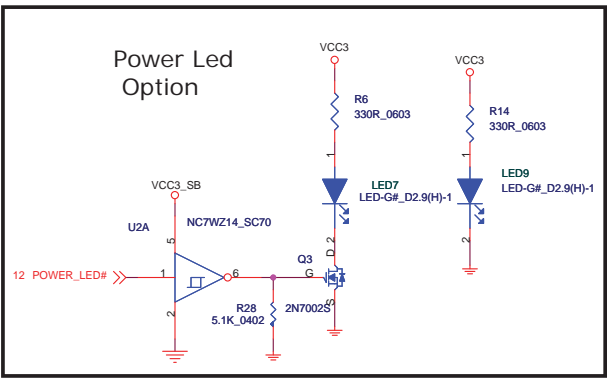
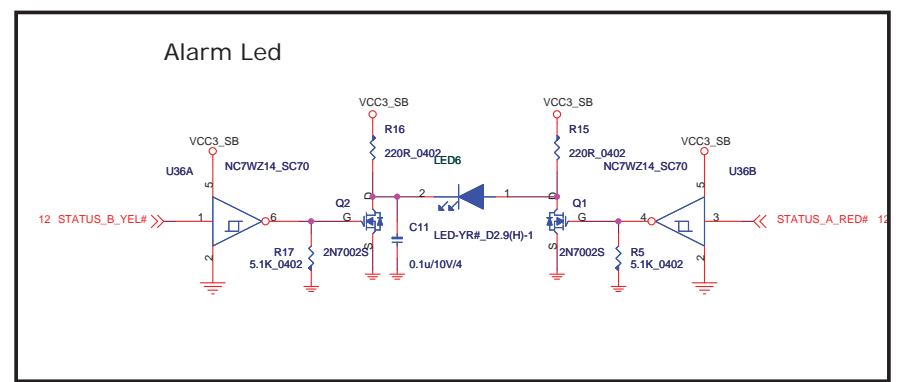
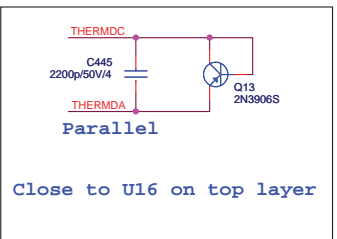
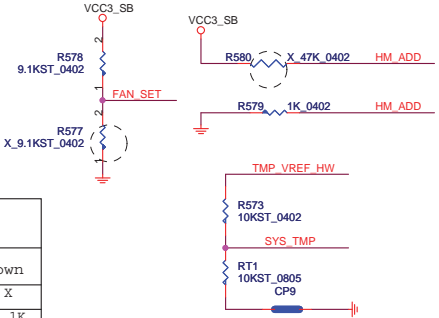


NOTE: LOCATE CLOSE STATUS PANEL

HI:Address = 0X5EH
 LO:Address = 0X5CH
 I2C Slave address select

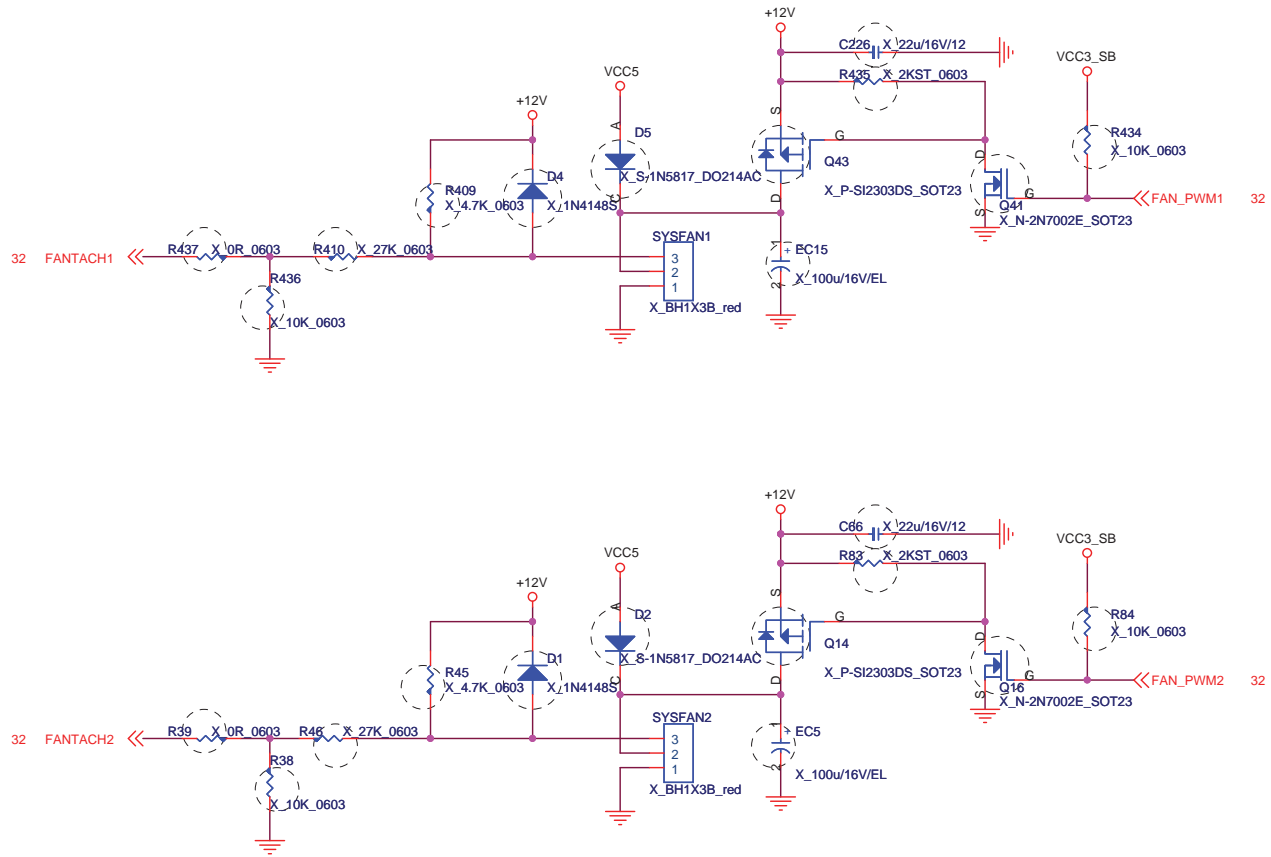
Fan Initial speed setting default: 100%

Section	Fan Speed rate	UP	Down
3	100%	9.1K	X
2	81%	4.7K	9.1K
1	62%	9.1K	4.7K
0	43%	X	9.1K



STATUS LED		24	25	27
SINGLE (FORWARD)	DARK	0	0	0
	0.1 sec BLINK	1	0	0
	0.5 sec BLINK	0	1	0
	Always Blight	1	1	0
DUAL (REVERSE)	DARK	0	0	1
	0.1 sec BLINK	1	0	1
	0.5 sec BLINK	0	1	1
	Always Blight	1	1	1

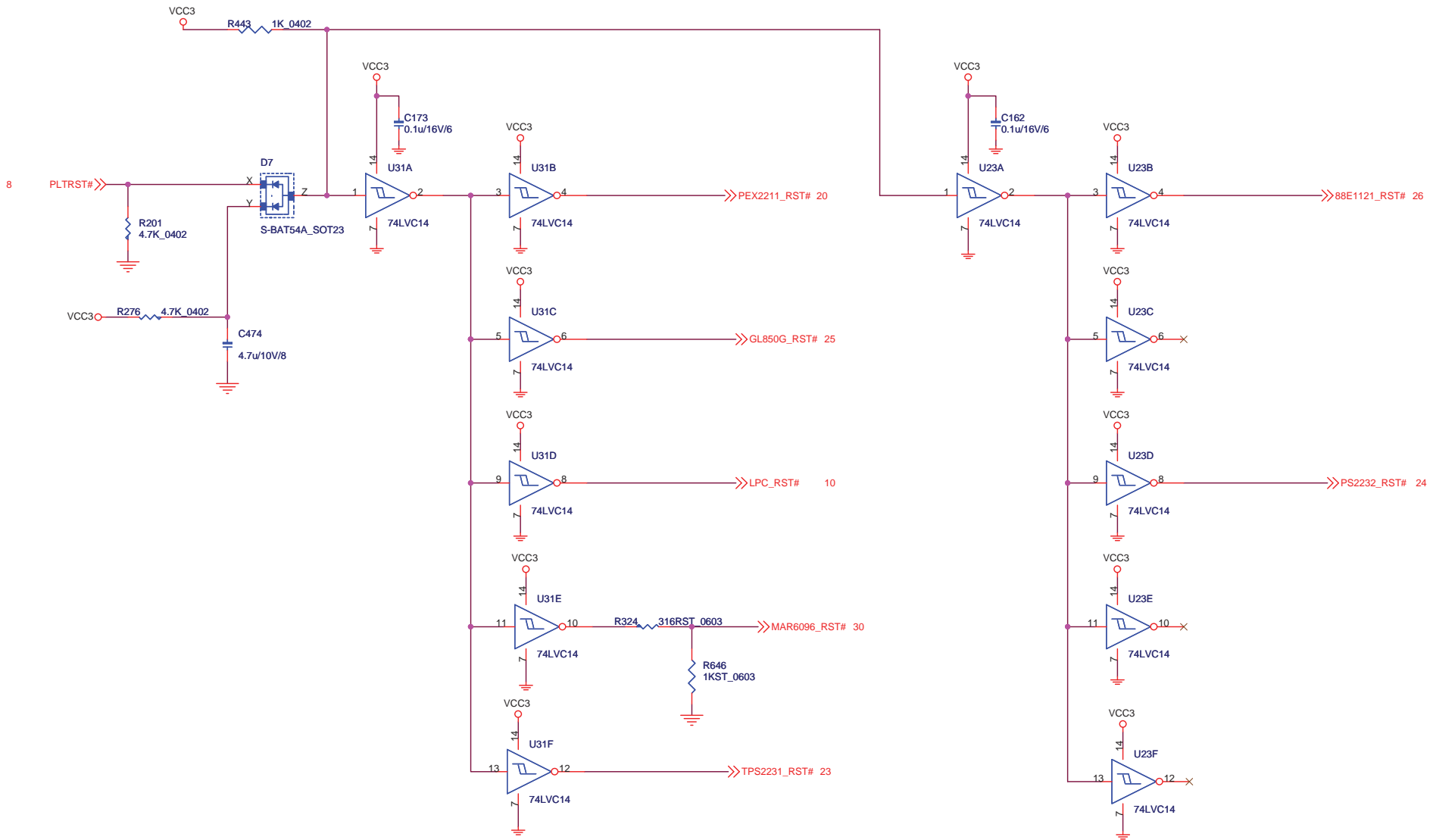
SYSTEM FAN



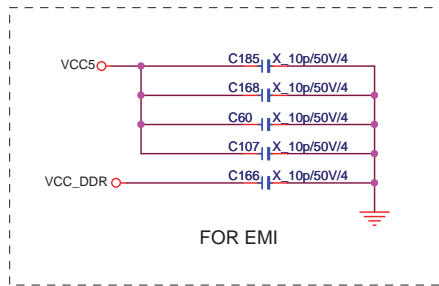
MICRO-STAR INT'L CO.,LTD


MS-96B6

Size B	Document Description SYSTEM FAN	Rev 0B
Date: Saturday, December 20, 2008		Sheet 33 of 43

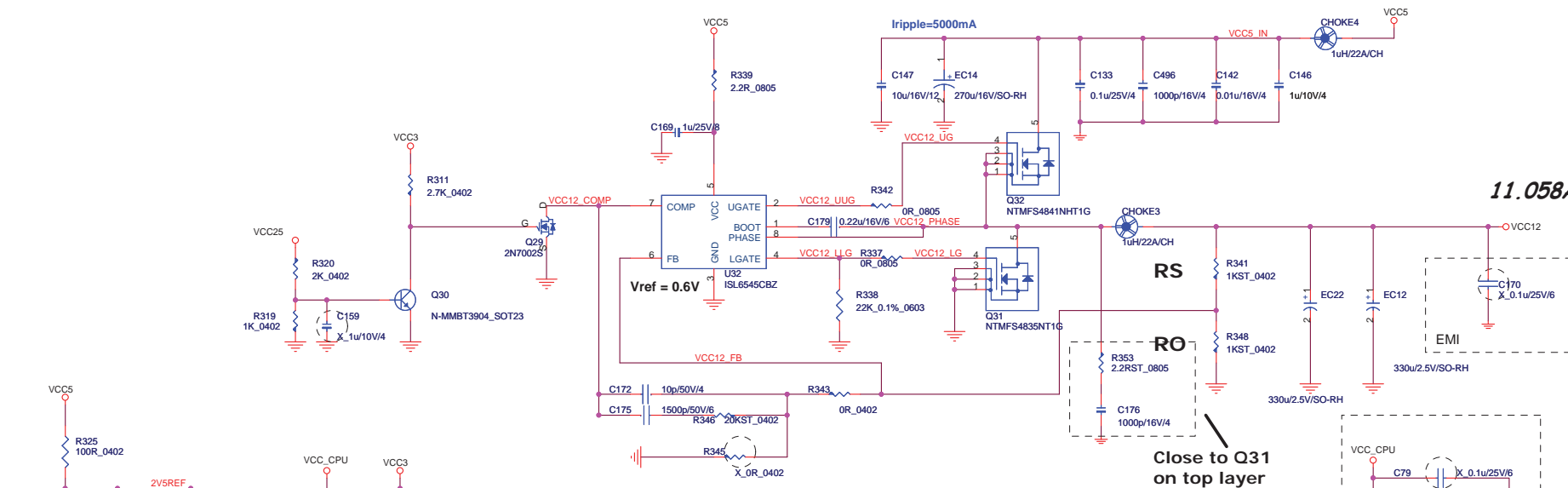


MSI			MICRO-STAR INT'L CO.,LTD		
MS-96B6			Reset Logic		
Size B	Document Description				Rev 0B
Date: Saturday, December 20, 2008		Sheet 34 of 43			



			MICRO-STAR INT'L CO.,LTD		
			MS-96B6		
Size B	Document Description EMI Caps			Rev 0B	
Date: Saturday, December 20, 2008			Sheet 35 of 43	1	

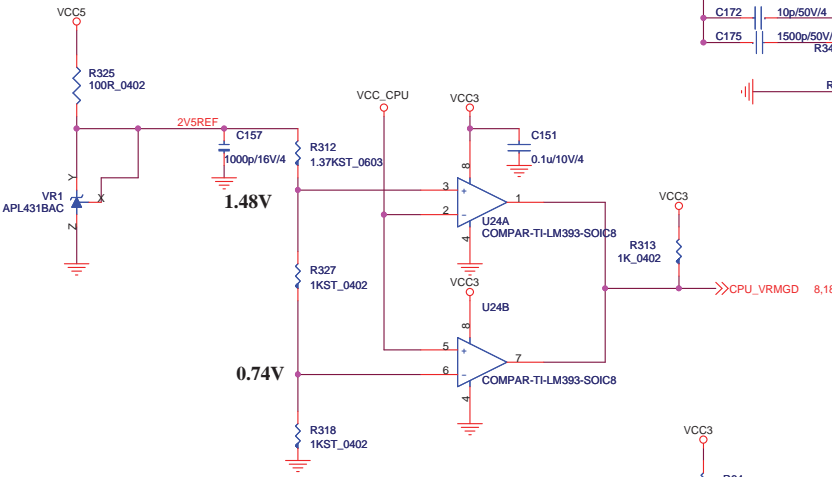
3.3A



11.058A

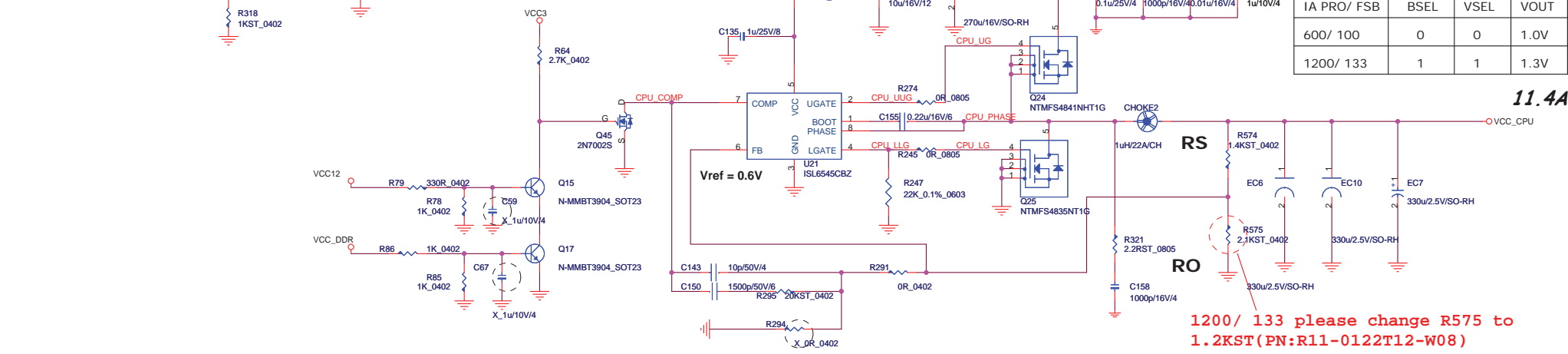
$$VOUT = 0.6 * (RS + RO) / RO$$

3.7A



$I_{input} \times 5V = 1.3V \times 11.4A / 0.8$
 $I_{input} = 3.7A$
 $D = 1.3 / 5 = 0.26$
 $I_{cap-rms} = 11.4 * 0.51 * 0.86 / 1 = 5A$

IA PRO/ FSB	BSEL	VSEL	VOUT
600/ 100	0	0	1.0V
1200/ 133	1	1	1.3V



11.4A

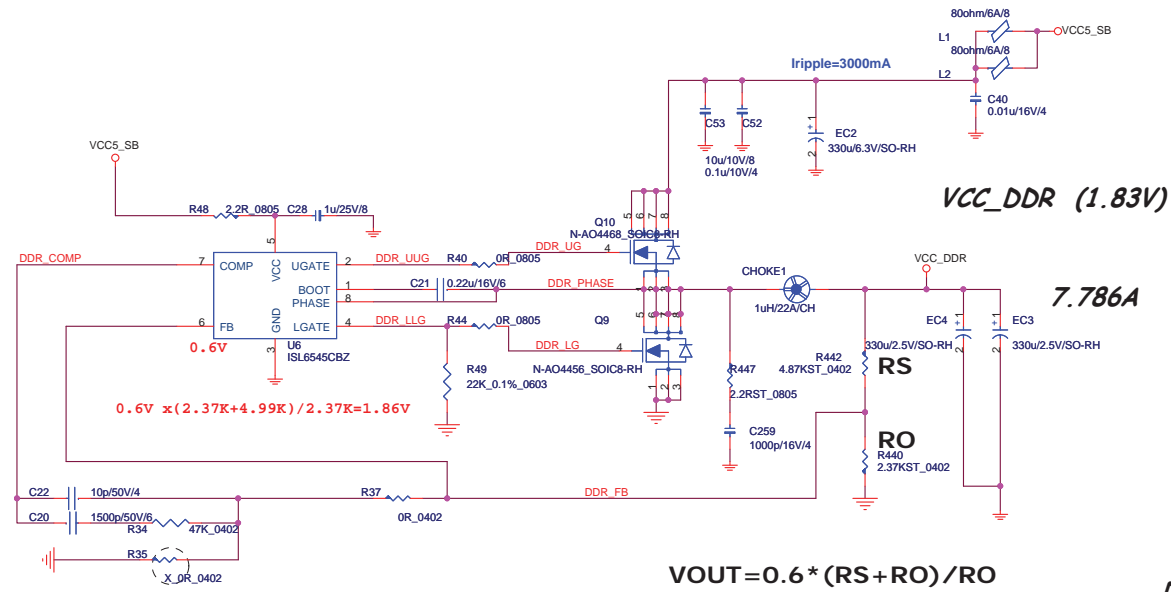
$$VOUT = 0.6 * (RS + RO) / RO$$

MICRO-STAR INT'L CO.,LTD

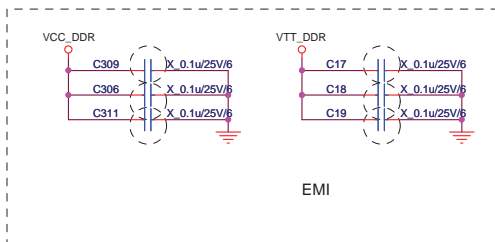
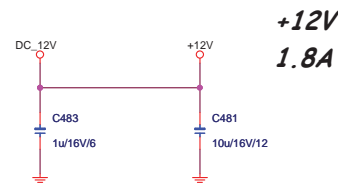
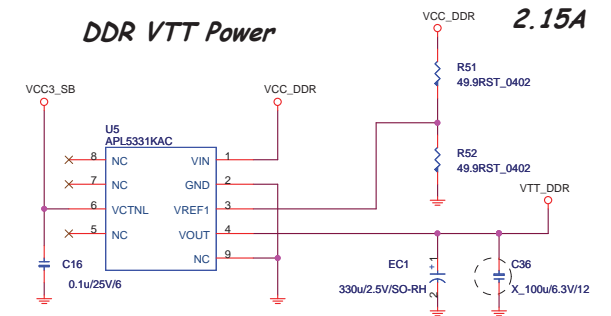
MS-96B6

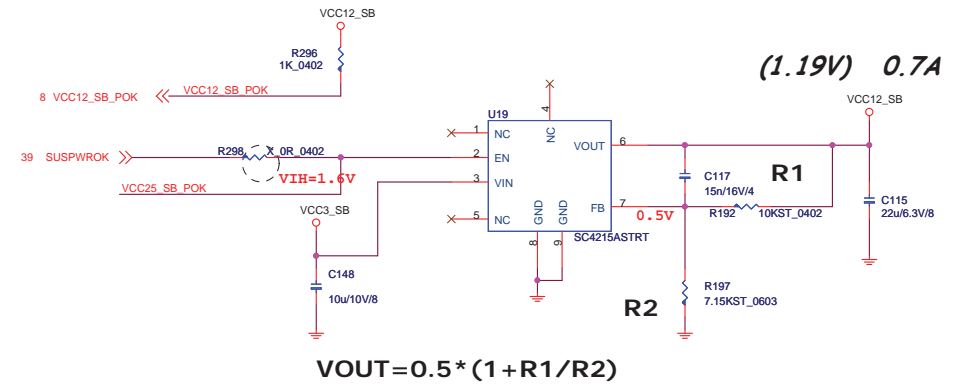
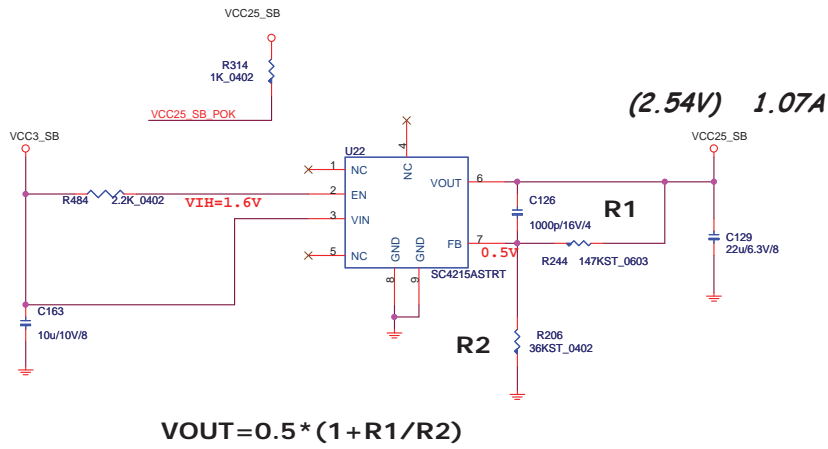
Size Custom	Document Description	Rev 0B
CPU POWER & 1.2V		
Date: Tuesday, December 23, 2008	Sheet 36	of 43

DDR II 1.8V POWER

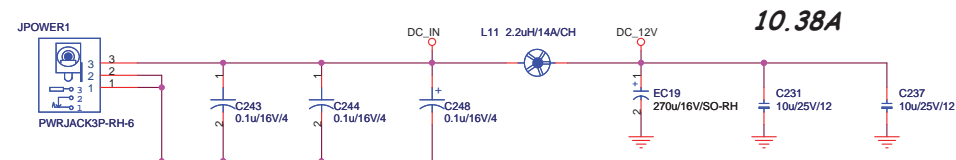
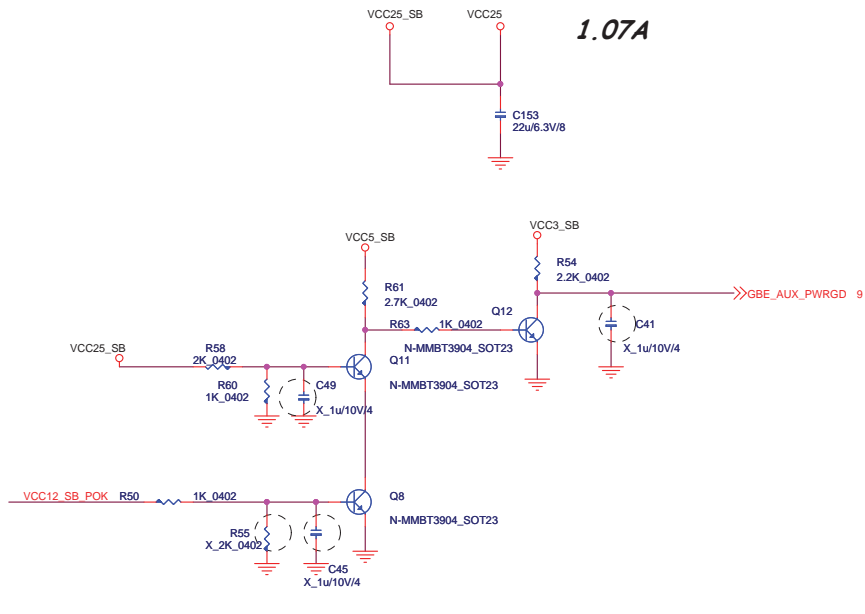
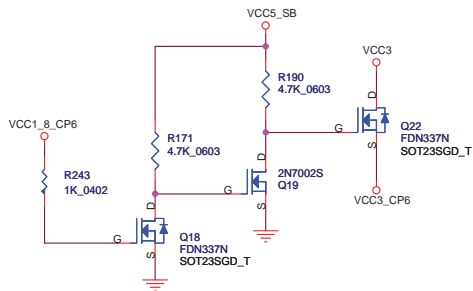
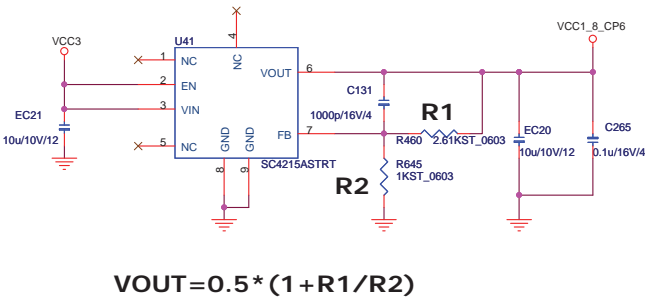


DDR VTT Power





VCC1_8_CP6 for CP6



<http://laptop-motherboard-schematic.blogspot.com/>

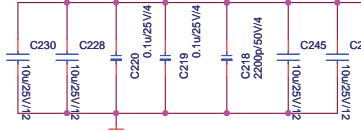
MSI		
MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description AUX POWER	Rev 0B
Date: Saturday, December 20, 2008	Sheet 38	of 43

3.38A

$V_{OUT} = 2 * (1 + R1/R2)$

6.7A

Place these CAPs close to FETs

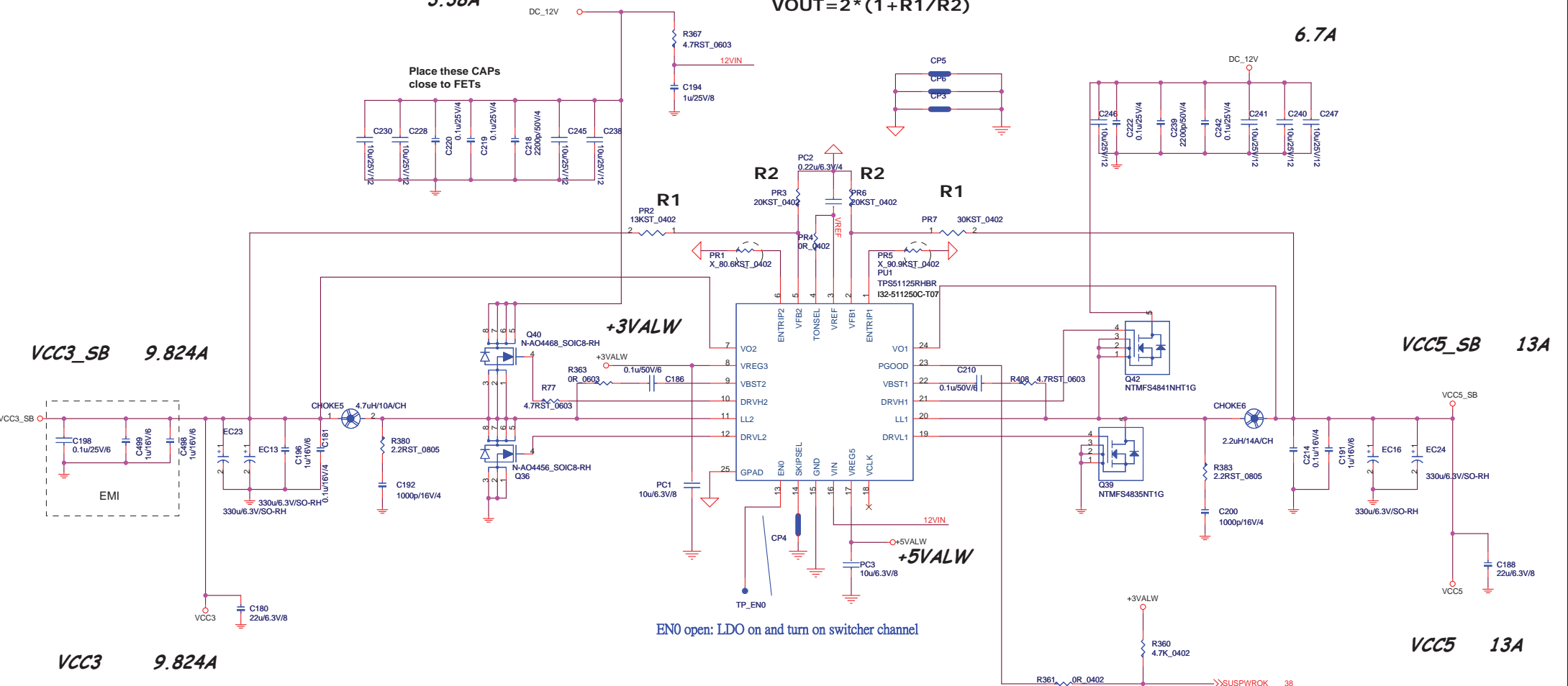


VCC3_SB 9.824A

VCC5_SB 13A

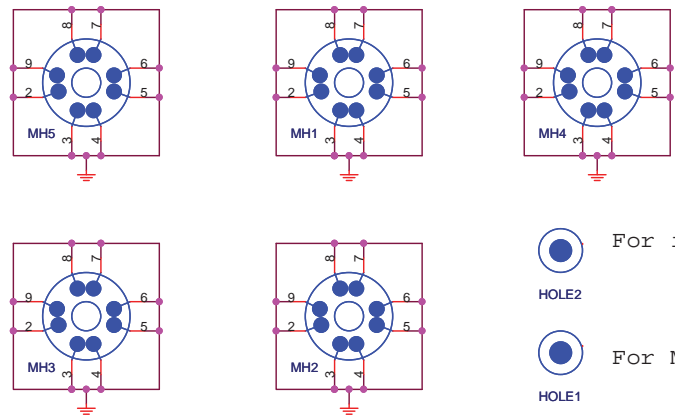
VCC3 9.824A

VCC5 13A



EN0 open: LDO on and turn on switcher channel

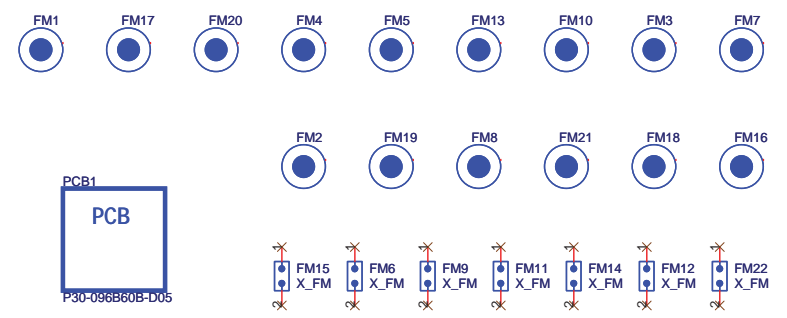
MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size Custom	Document Description	Rev 0B
DC-IN POWER		
Date: Saturday, December 20, 2008	Sheet 39	of 43



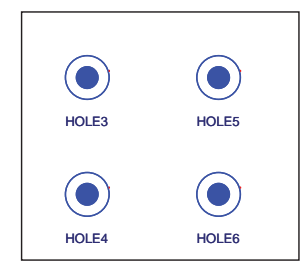
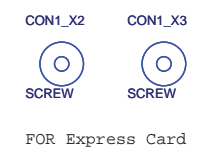
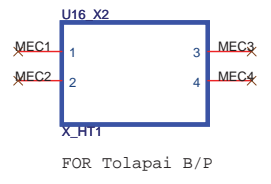
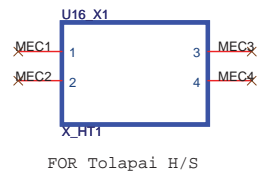
SN_LABEL

 SN_LABEL
 SN_LABEL1

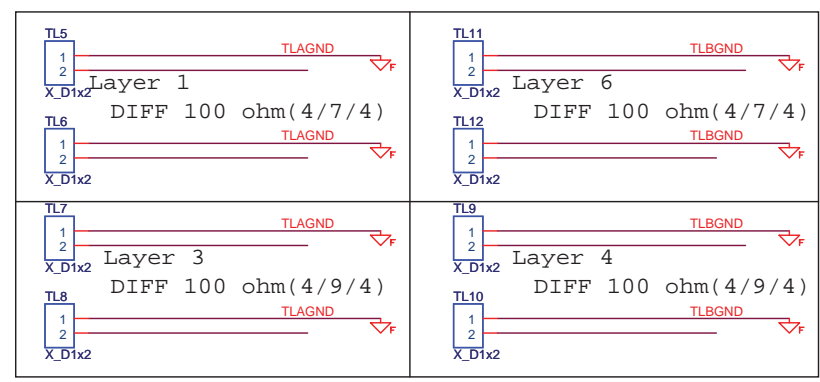
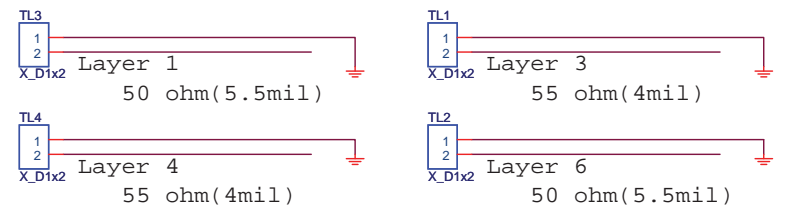
 SN_LABEL



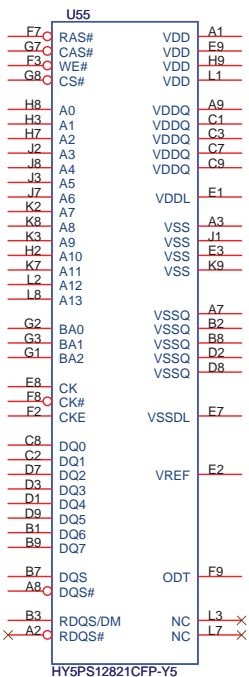
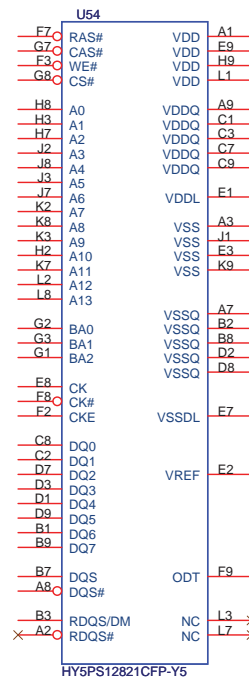
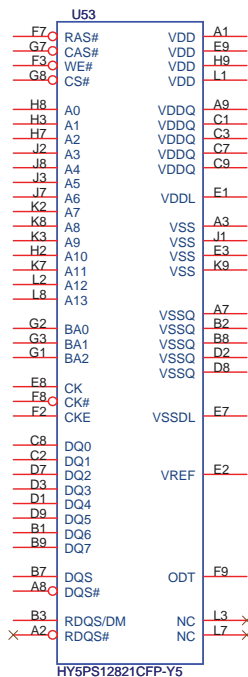
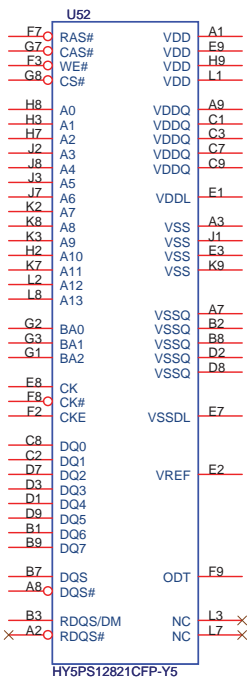
Optics Orientation Holes



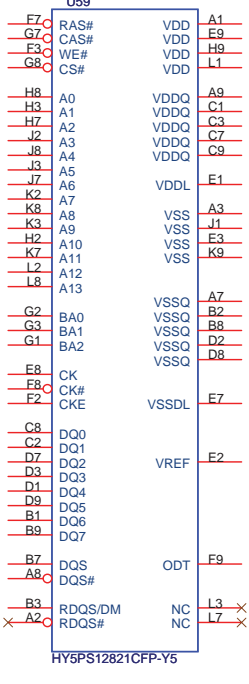
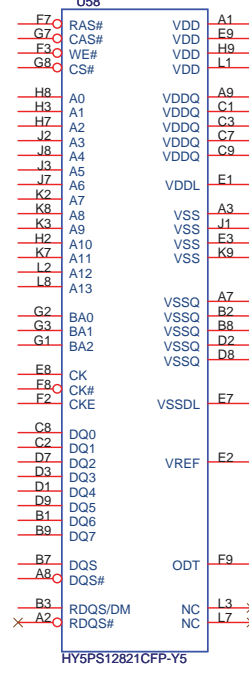
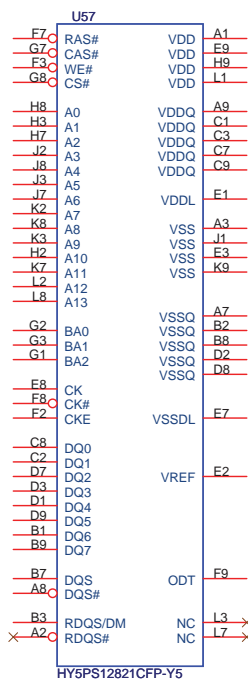
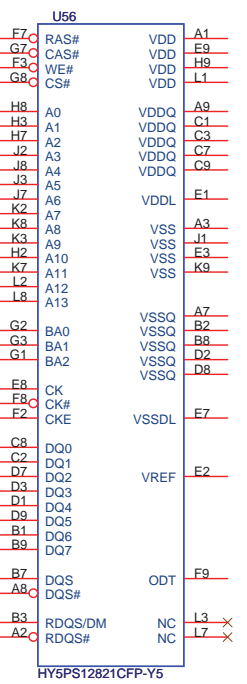
IMPEDANCE TRACE



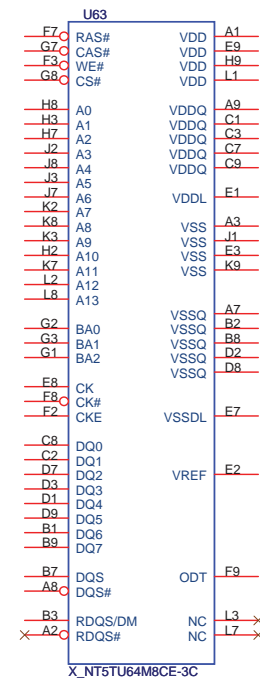
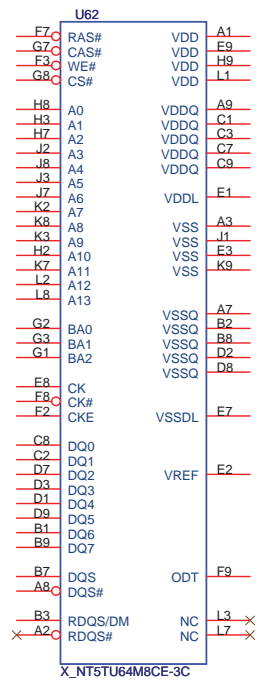
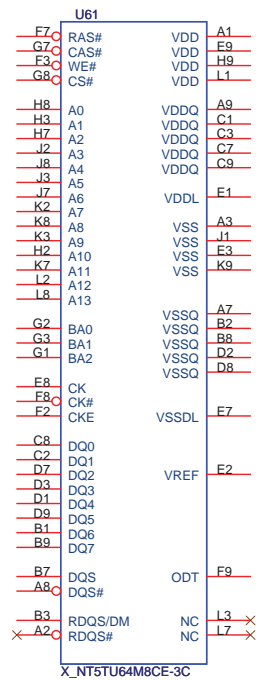
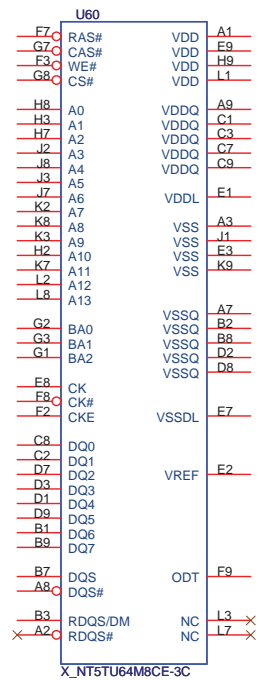
	MICRO-STAR INT'L CO.,LTD	
	MS-96B6	
	Size B	Document Description MISC
Date: Tuesday, December 23, 2008		Sheet 40 of 43



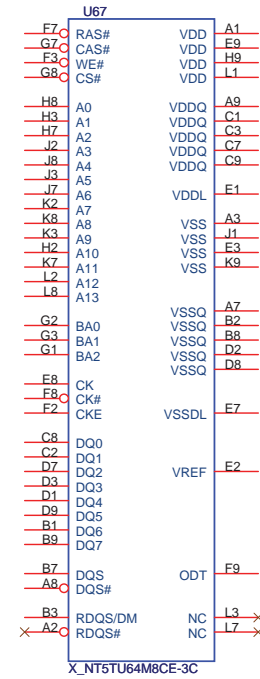
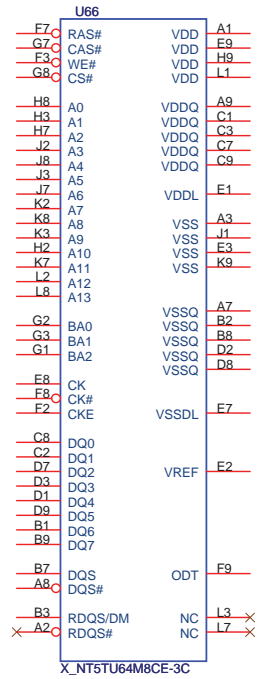
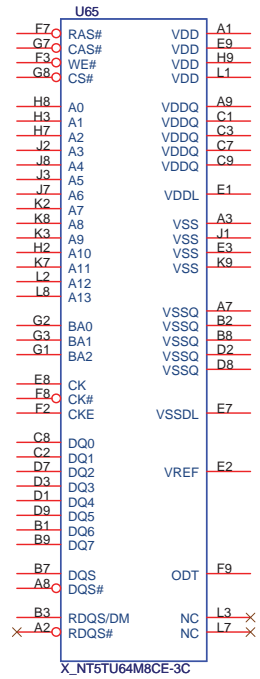
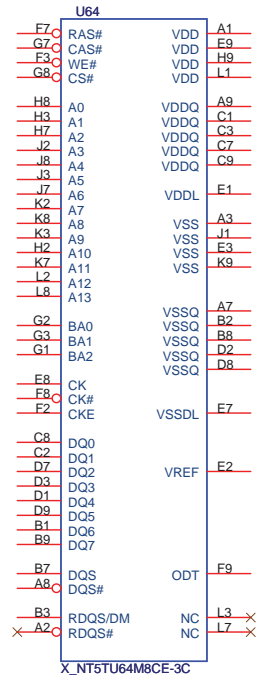
DDR2 SDRAM, 512M(64Mx8bit)



MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size B	Document Description	Rev 0B
HYNIX MEMORY		
Date: Saturday, December 20, 2008		Sheet 41 of 43



DDR2 SDRAM, 512M(64Mx8bit)




MICRO-STAR INT'L CO.,LTD		
MS-96B6		
Size B	Document Description	Rev 0B
NANYA MEMORY		
Date: Saturday, December 20, 2008	Sheet 42 of 43	

2008/7/23 by Henry

1. Page 32, add SATA LED, LED12 and R900, R901
2. Page 18, add R383 for MS-9668 suggestion to fix abnormal on-off issue, primarily to discharge leakage
3. Page 37, add C704 for DC_IN and 12V switch delay
4. Page 8, add 1.2V_SB power squence to RSMRST#

2008/7/25 by Henry

1. Page 38, Change U32 and U26 to UPI7706
2. Page 40, add HOLE19 for MOSFET push pin
3. Add R233~R240

			MICRO-STAR INT'L CO.,LTD		
			MS-96B6		
Size B	Document Description HISTORY		Rev 0B		
Date: Tuesday, November 25, 2008			Sheet	43 of 43	