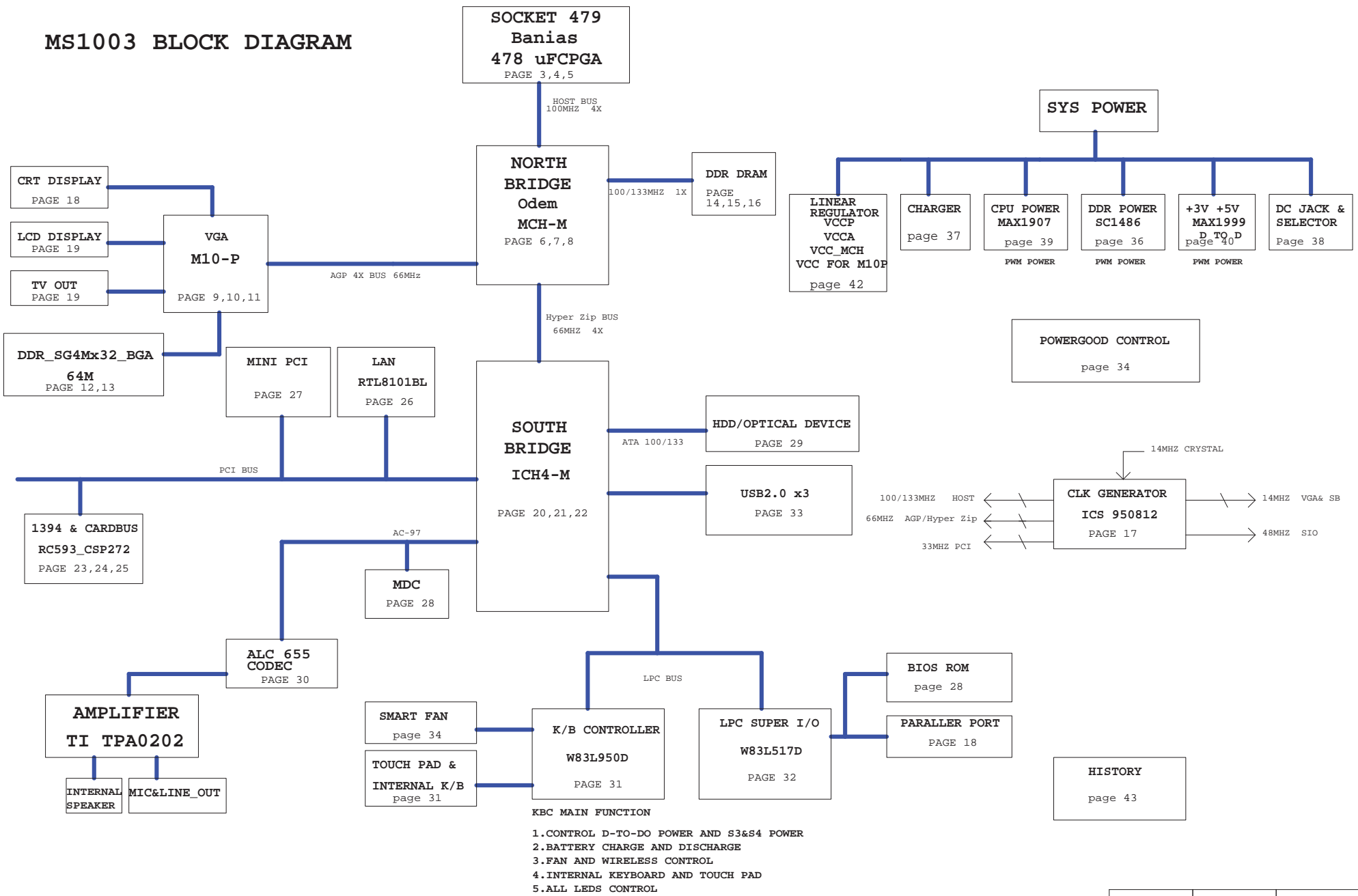


MS1003 BLOCK DIAGRAM



- KBC MAIN FUNCTION**
- 1.CONTROL D-TO-DO POWER AND S3&S4 POWER
 - 2.BATTERY CHARGE AND DISCHARGE
 - 3.FAN AND WIRELESS CONTROL
 - 4.INTERNAL KEYBOARD AND TOUCH PAD
 - 5.ALL LEDS CONTROL

Approved by	Checked by	Designed by
MSI CORPORATION		
BLOCK DIAGRAM		
P. Leader	File	Rev
	MS-1003	0.C
Date	Thursday, February 05, 2004	Sheet 1 of 43

Voltage Rails

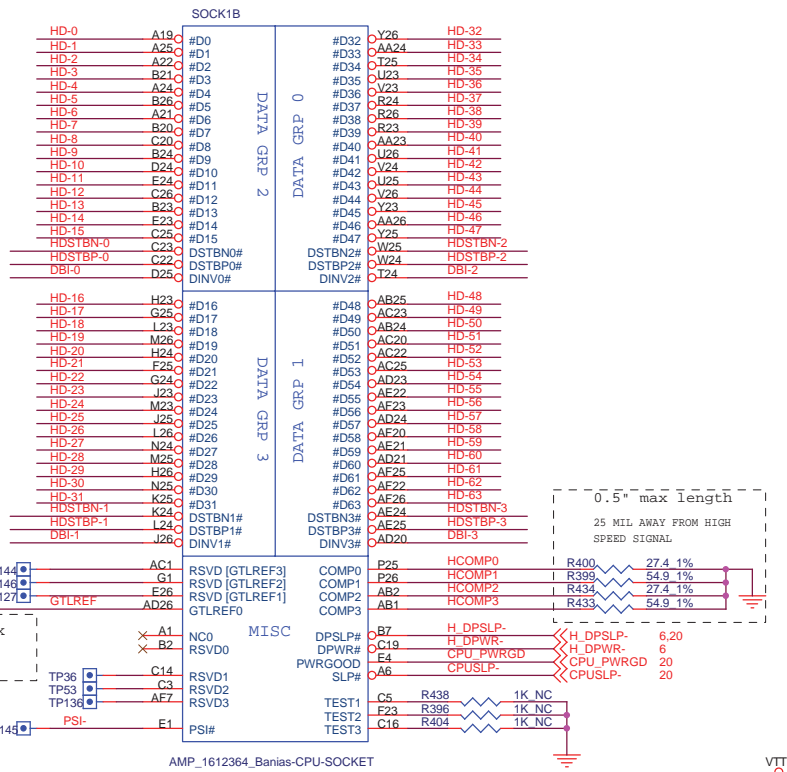
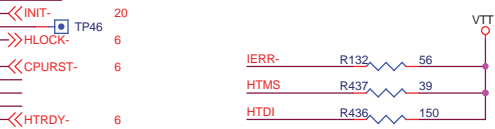
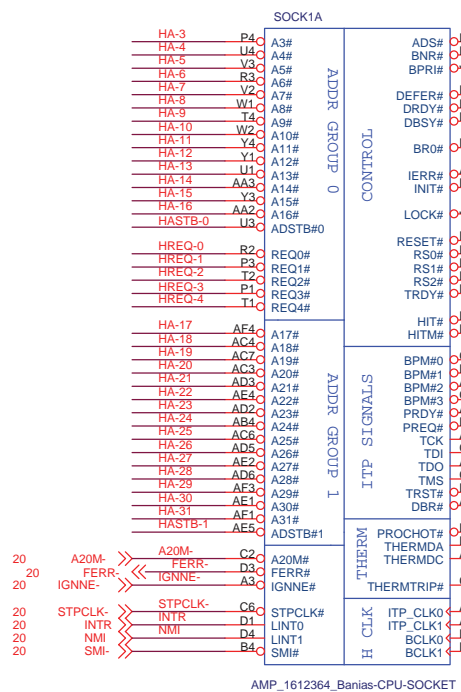
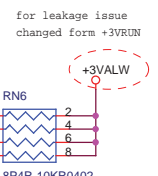
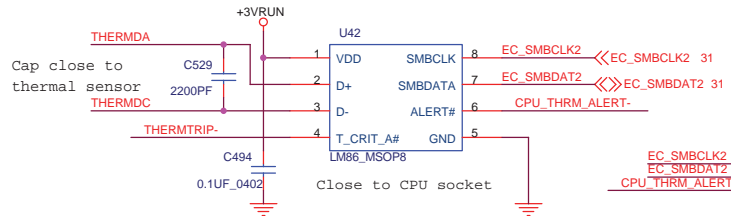
Vol tage	Descri pti on	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHCORE	Core voltage for Processor	VTT_PWRGD
VTT	1.05V rail for Processor I/O	RUNPWROK
+VCC1_2_MCH	1.2V For 855PM Core(off in S3-S5)	RUNPWROK
M10_CORE	1.0/1.2V core voltage for M10(off in S3-S5)	RUN_ON
SMDDDR_VTERM	1.25V DDR Termination voltage(off in S4-S5)	+5VRUN
+1_5VSUS	1.5V power rail (off in S4-S5)	+5VSUS
+1_5VRUN	1.5V switched power rail(off in S3-S5)	RUN_ON
+1_8VRUN	1.8V switched power rail (off in S3-S5)	+1_5VRUN
+2_5VSUS	2.5V power rail for DDR(off in S4-S5)	+5VSUS
M10_MEM	2.5V power rail for M10(off in S3-S5)	RUN_ON
+3VALW	3.3V always on power rail	PWR_SRC
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+3VRUN	3.3V switched power rail(off in S3-S5)	RUN_ON
+5VALW	5.0V always on power rail	PWR_SRC
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+5VRUN	5.0V switched power rail(off in S3-S5)	RUN_ON

POWER STATES

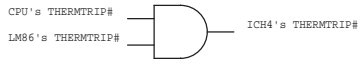
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

*Note : WHEN AC MODE , System turn on then +V*SUS will always keep high*

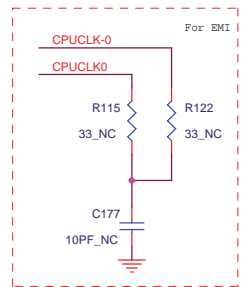
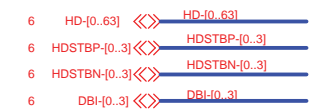
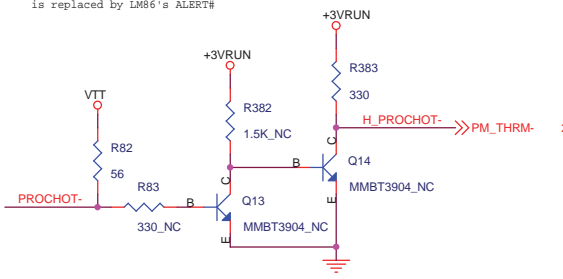
MSI CORPORATION		
Title MS1003 PLATFORM		
Size Custom	Document Number MS-1003	Rev 0.C
Date: Thursday, February 05, 2004	Sheet 2	of 43



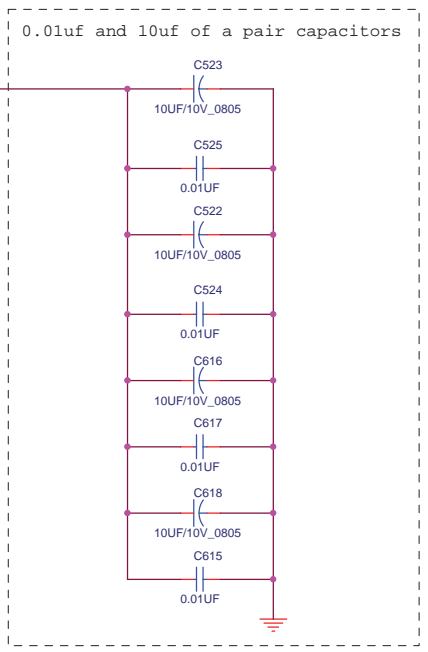
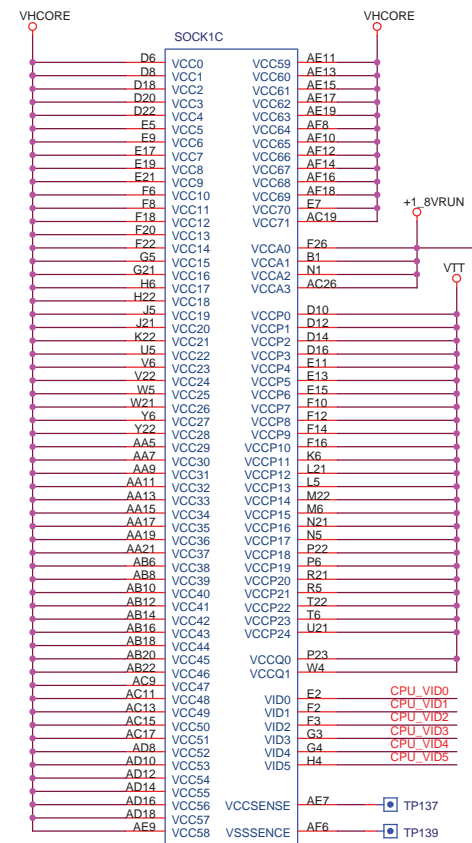
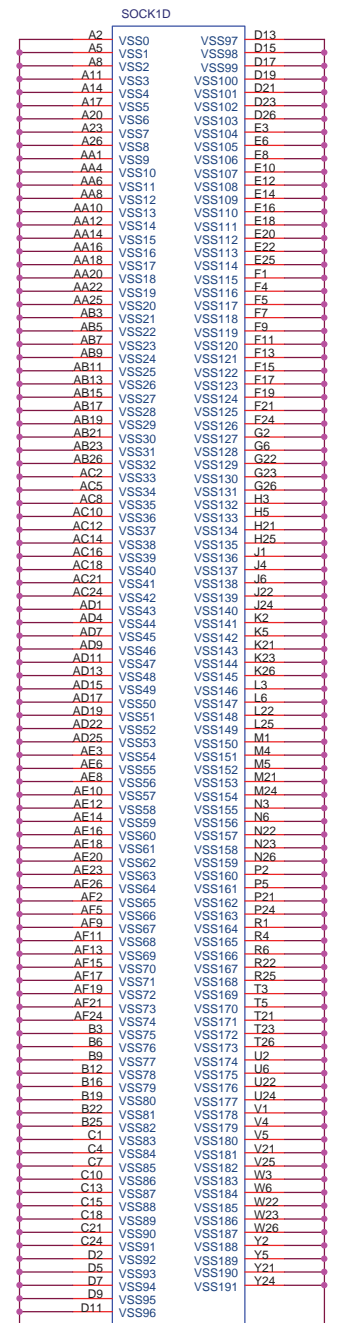
0.5" max length
25 MIL AWAY FROM HIGH SPEED SIGNAL



The PROCHOT#(ICH4:THRM#) function is replaced by LM86's ALERT#



MSI CORPORATION			
Title	Banias-1		
Size	Document Number	Rev	
Custom	MS-1003	0.C	
Date:	Thursday, February 05, 2004	Sheet	3 of 43



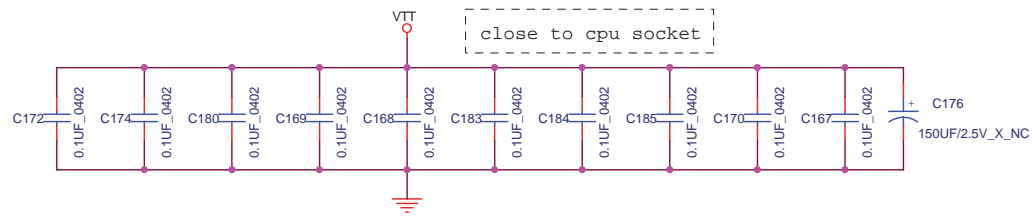
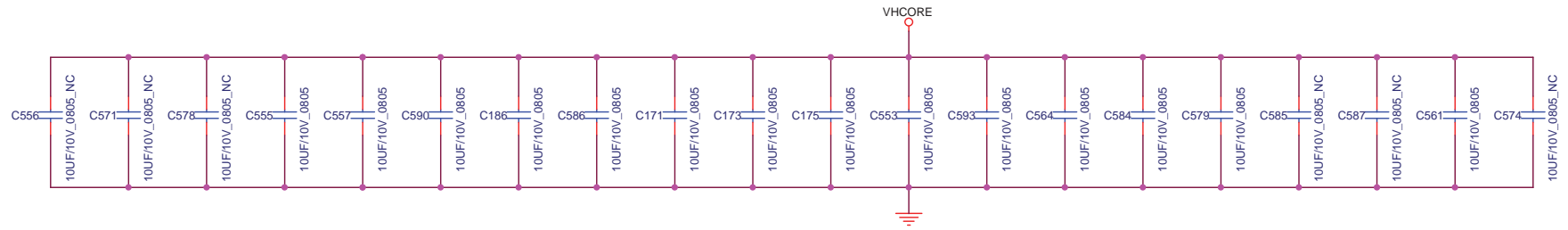
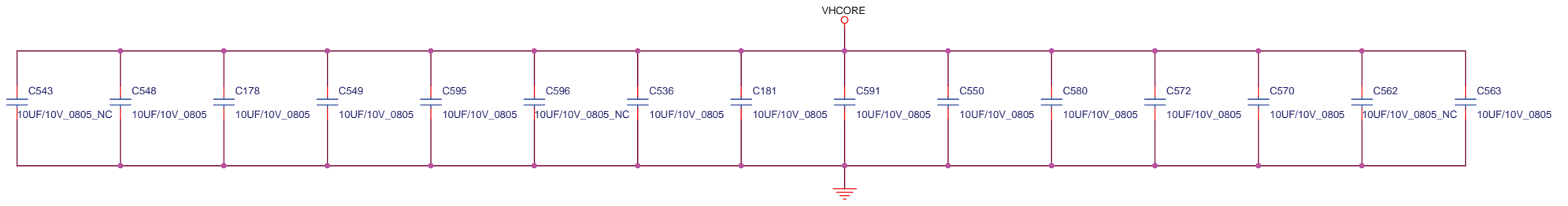
AMP_1612364_Banias-CPU-SOCKET

39 CPU_VID[0..5] ← CPU_VID[0..5]

LAYOUT NOTE: Provide a test point (with no stub) to connect differential probe between VCCSENSE and VSSSENCE at the location where the two 54.9 ohm resistors terminate the 55 ohm transmission lines.

AMP_1612364_Banias-CPU-SOCKET

MSI CORPORATION			
Title Banias-2			
Size	Document Number	Rev	
Custom	MS-1003	0.C	
Date:	Thursday, February 05, 2004	Sheet	4 of 43

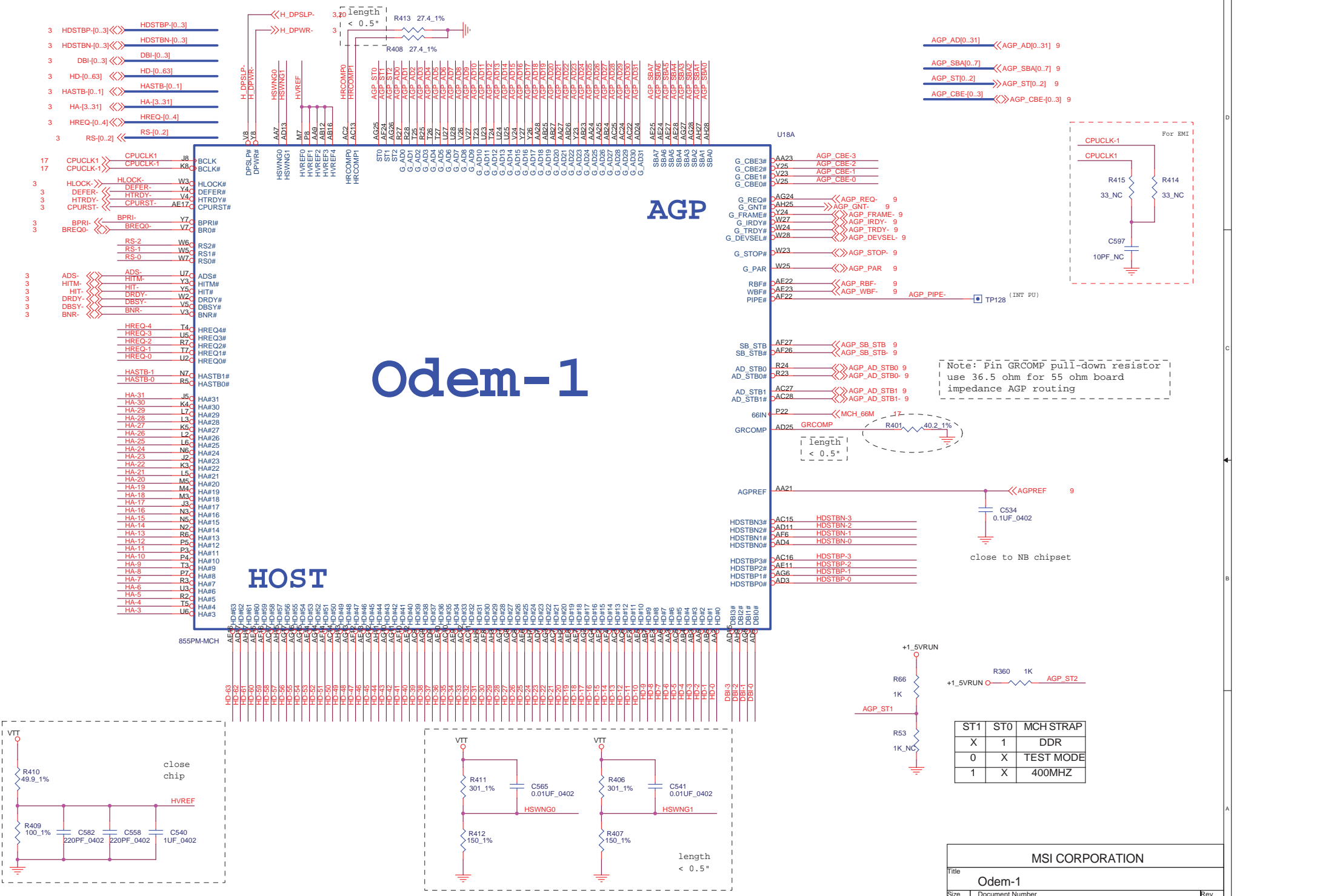


MSI CORPORATION		
Title		
Banias-3		
Size	Document Number	Rev
B	MS-1003	0.C
Date:	Thursday, February 05, 2004	Sheet 5 of 43

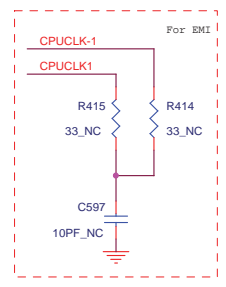
Odem-1

AGP

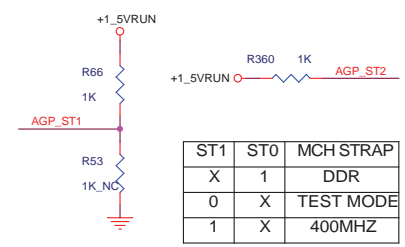
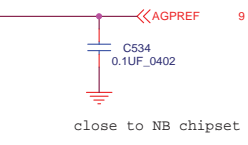
HOST



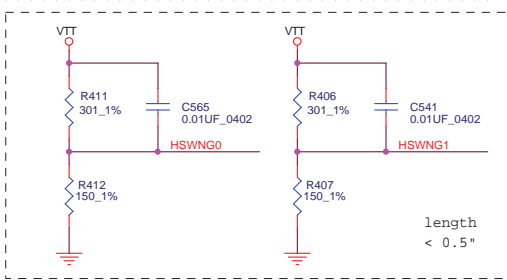
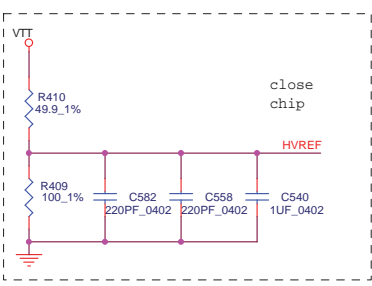
- AGP_AD[0..31] <<> AGP_AD[0..31] 9
- AGP_SBA[0..7] <<> AGP_SBA[0..7] 9
- AGP_ST[0..2] <>> AGP_ST[0..2] 9
- AGP_CBE[0..3] <<> AGP_CBE[0..3] 9



Note: Pin GRCOMP pull-down resistor use 36.5 ohm for 55 ohm board impedance AGP routing



ST1	ST0	MCH STRAP
X	1	DDR
0	X	TEST MODE
1	X	400MHZ



MSI CORPORATION

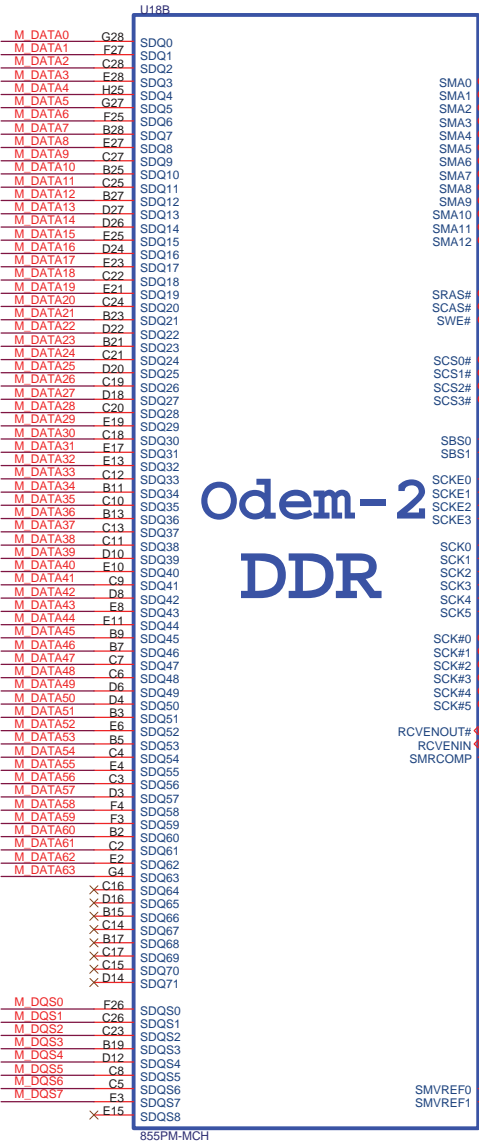
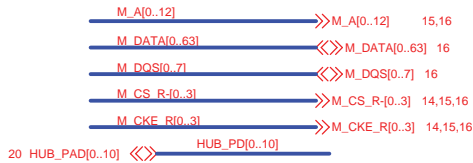
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Size: Custom MS-1003

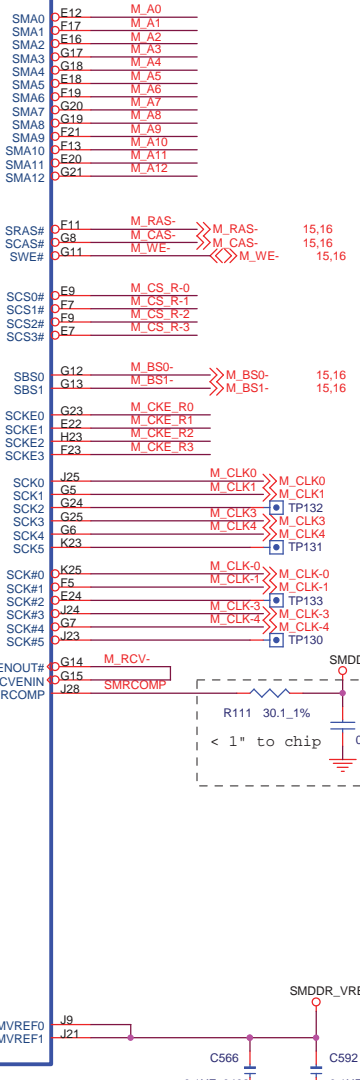
Date: Thursday, February 05, 2004

Sheet: 6 of 43

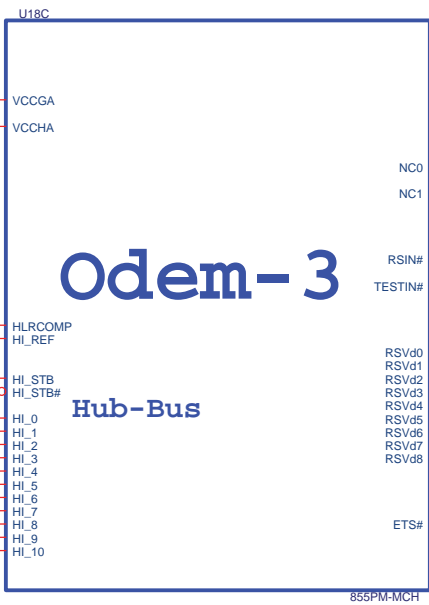
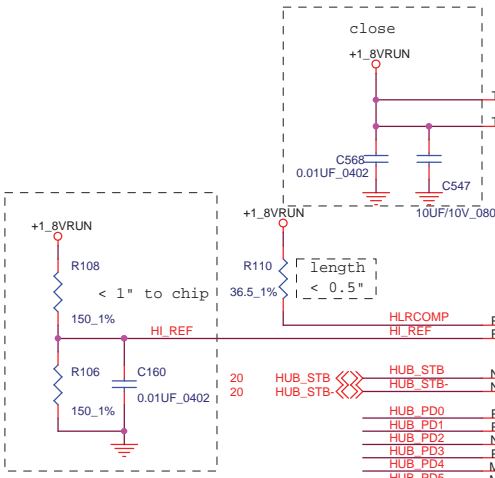
Rev: 0.C



Odem-2 DDR

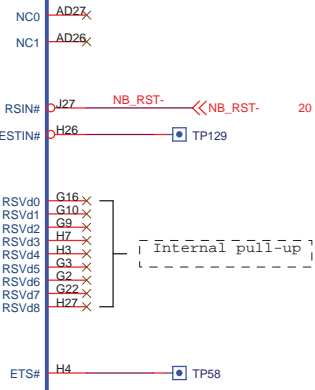


AS CLOSE AS POSSIBLE TO NB chipset



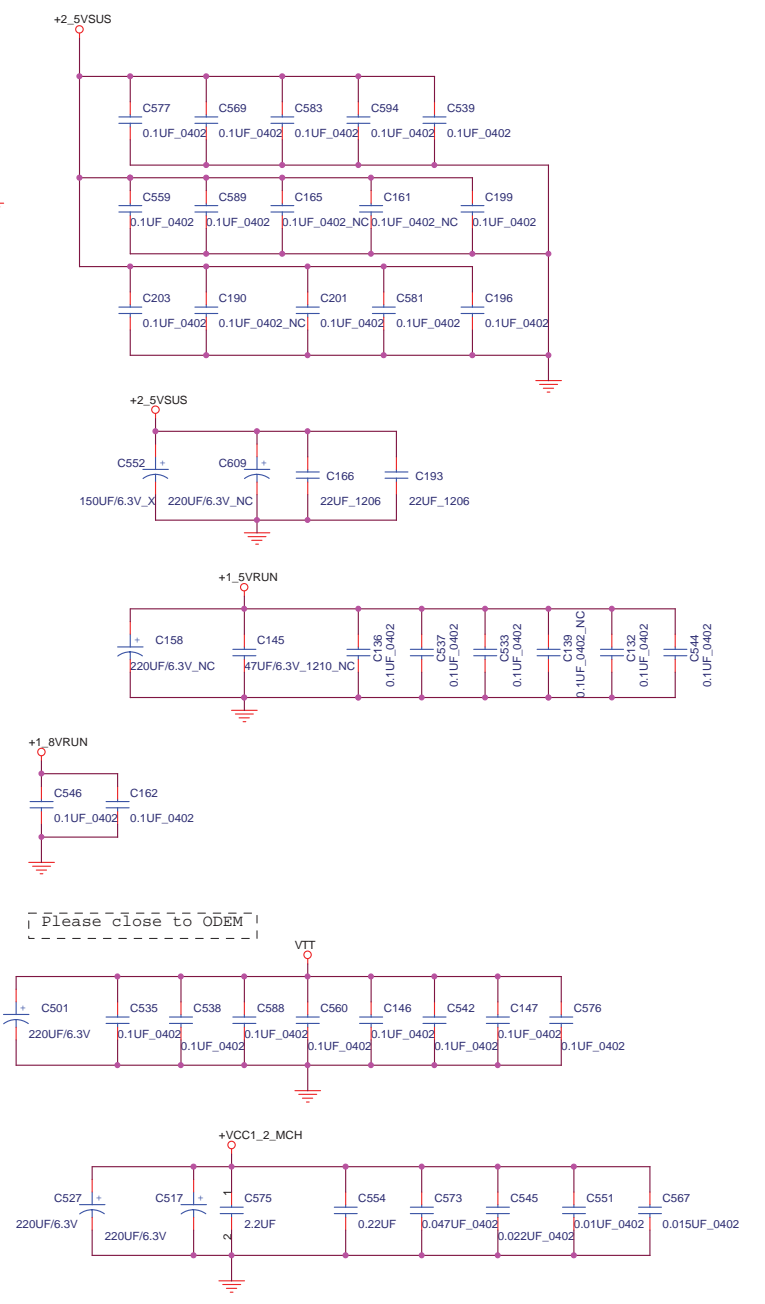
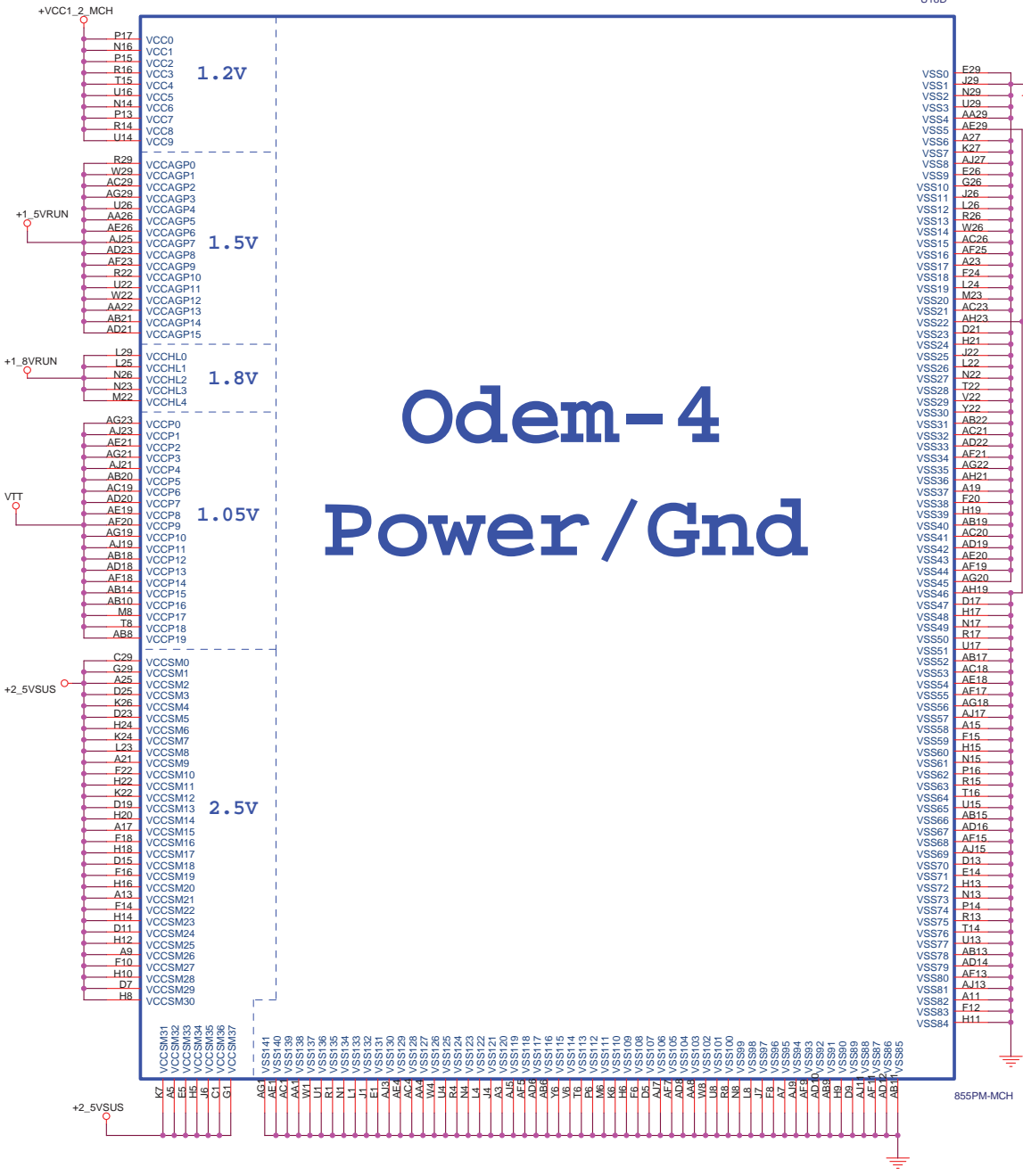
Odem-3

Hub-Bus



MSI CORPORATION		
Title Odem-2		
Size Custom	Document Number MS-1003	Rev 0.C
Date: Thursday, February 05, 2004	Sheet 7 of 43	

Odem-4 Power / Gnd

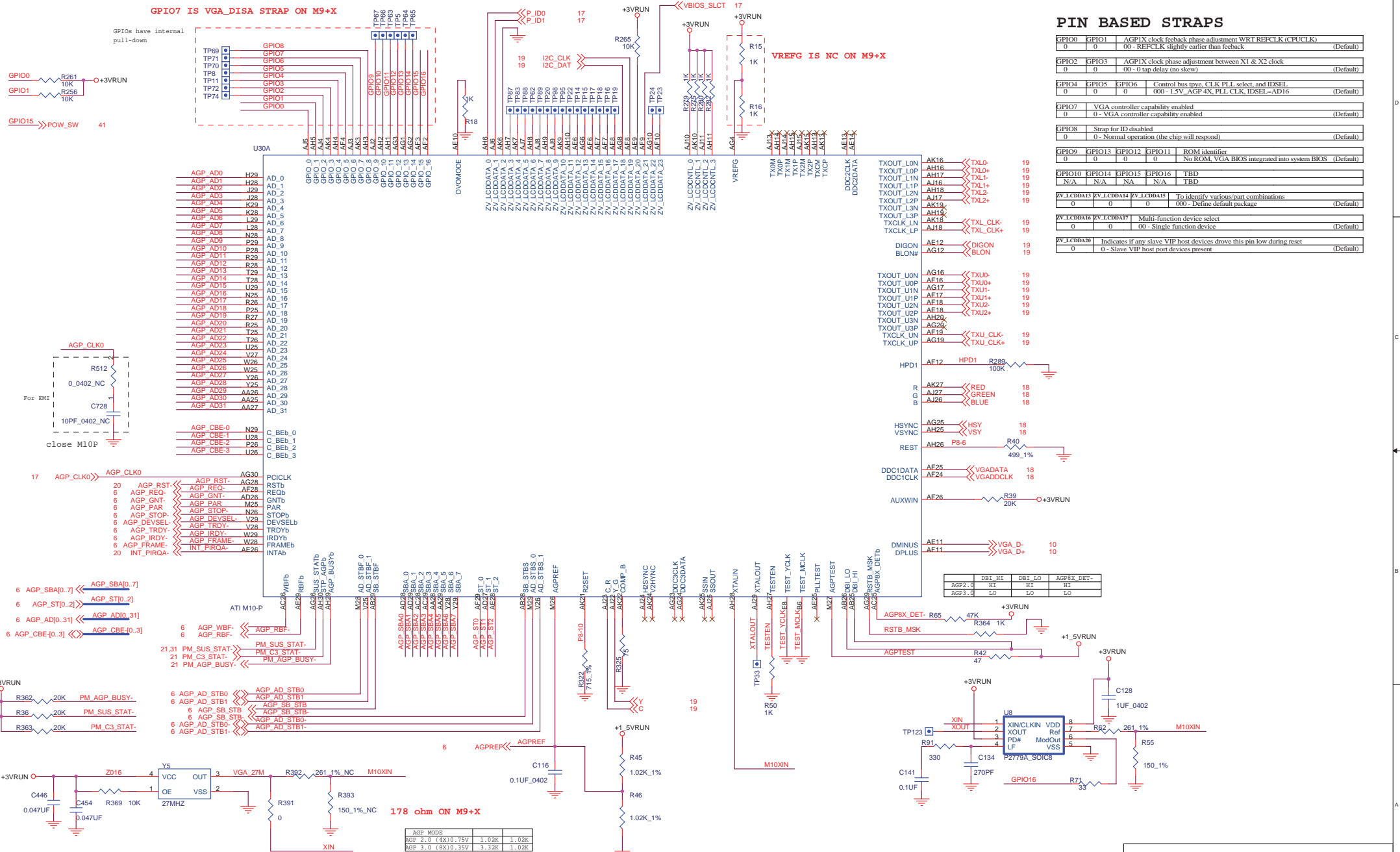


MSI CORPORATION			
Title			
Odem-3			
Size	Document Number	Rev	
Custom	MS-1003	0.C	
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GPIO7 IS VGA_DISA STRAP ON M9+X

PIN BASED STRAPS

GPIO0	GPIO1	AGPIX clock feedback phase adjustment WRT REFCLK (CPUCLK)		
0	0	00 - REFCLK slightly earlier than feedback	(Default)	
GPIO2	GPIO3	AGPIX clock phase adjustment between X1 & X2 clock		
0	0	00 - 0 tap delay (no skew)	(Default)	
GPIO4	GPIO5	GPIO6	Control bus type, CLK, PLL, select, and IDSEL	
0	0	000 - 1.5V, AGP 4X, PLL, CLK, IDSEL - AD16	(Default)	
GPIO7	VGA controller capability enabled			
0	0 - VGA controller capability enabled			
GPIO8	Strap for ID disabled			
0	0 - Normal operation (the chip will respond)			
GPIO9	GPIO13	GPIO12	GPIO11	ROM Identifier
0	0	0	0	No ROM, VGA BIOS integrated into system BIOS (Default)
GPIO10	GPIO14	GPIO15	GPIO16	TBD
N/A	N/A	N/A	N/A	TBD
ZV_LCD0A13	ZV_LCD0A14	ZV_LCD0A15	ZV_LCD0A16	To identify various part combinations
0	0	0	000 - Define default package	(Default)
ZV_LCD0A16	ZV_LCD0A17	Multi-function device select		
0	0	00 - Single function device		
ZV_LCD0A20		Indicates if any slave VIP host devices drove this pin low during reset		
0		0 - Slave VIP host port devices present		



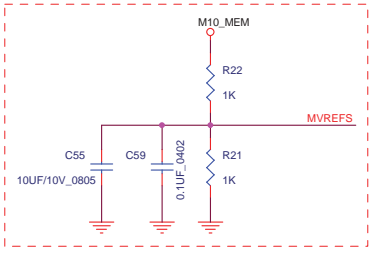
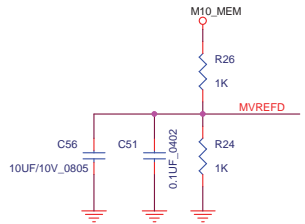
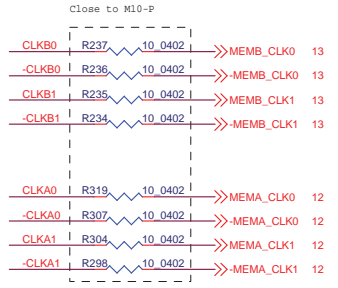
AGP MODE	AGP 2.0 (4x) 10.75V	1.02K	1.02K
AGP 2.0	(8x) 10.35V	3.32K	1.02K

MSI CORPORATION

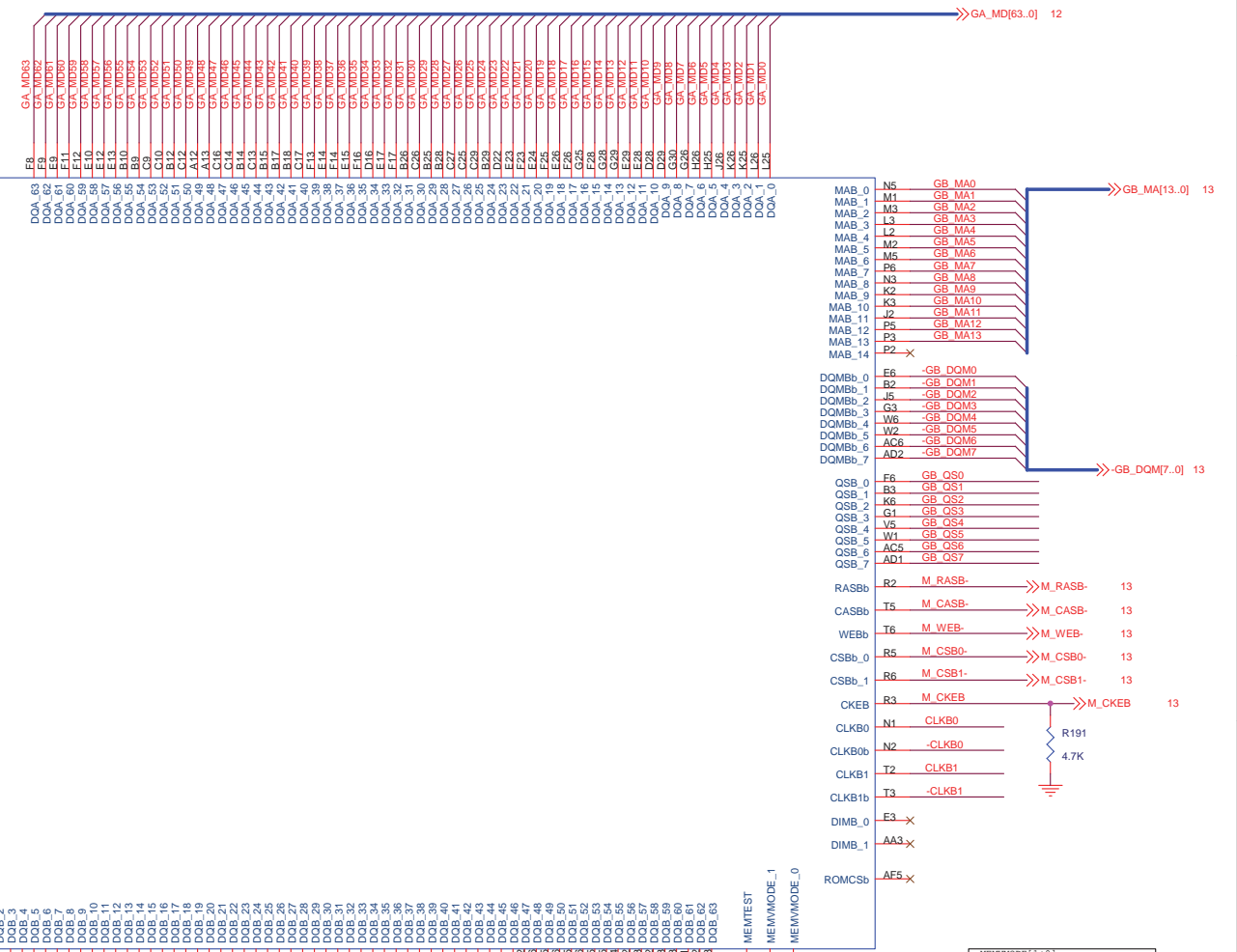
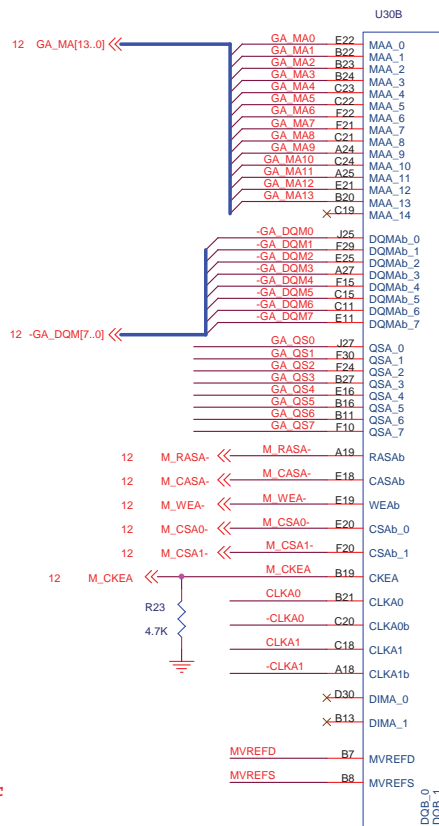
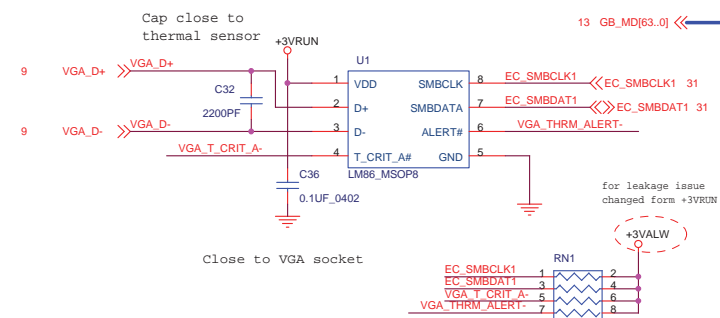
Title: M10-P_VGA/IO

Size: Document Number
 Custom MS-1003

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MVREFS(B8) IS A NC ON M9+X



MEMMODE[1:0]	
01	:VDDR1 2.5V (SSTL-2/DDR)
10	:VDDR1 1.8V (SLP1DA/DDR)
11	:VDDR1 2.8V (SST-2/DDR)

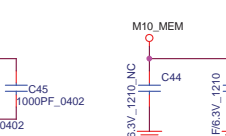
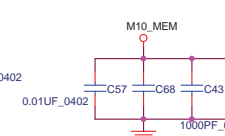
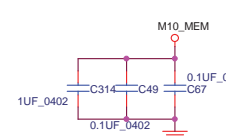
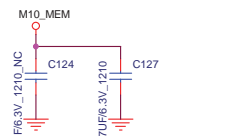
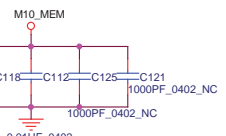
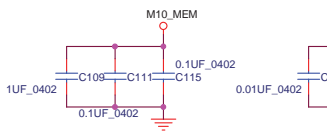
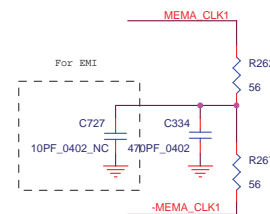
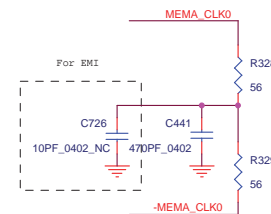
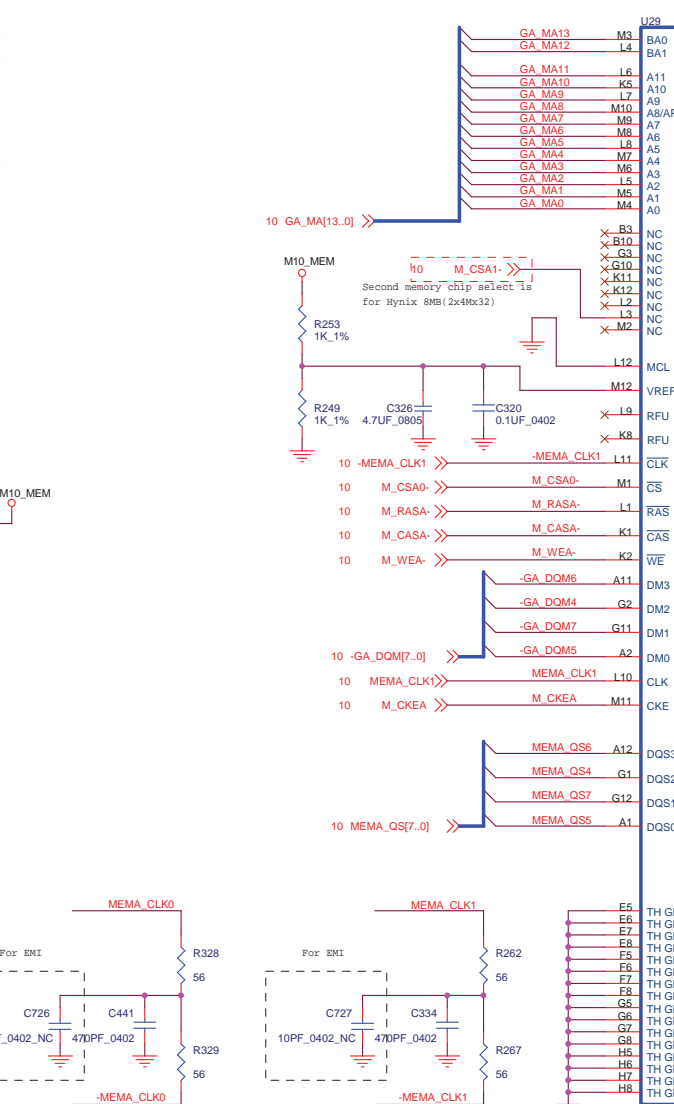
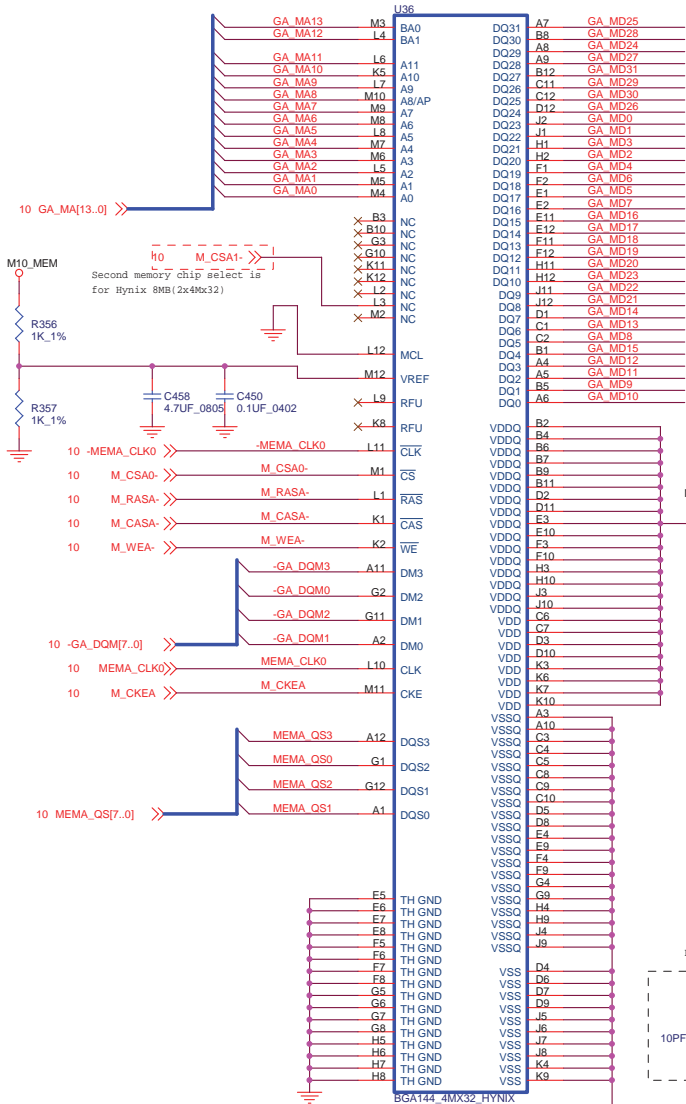
MSI CORPORATION

Title: M10-P_MEM

Size: Custom | Document Number: MS-1003 | Rev: 0.C

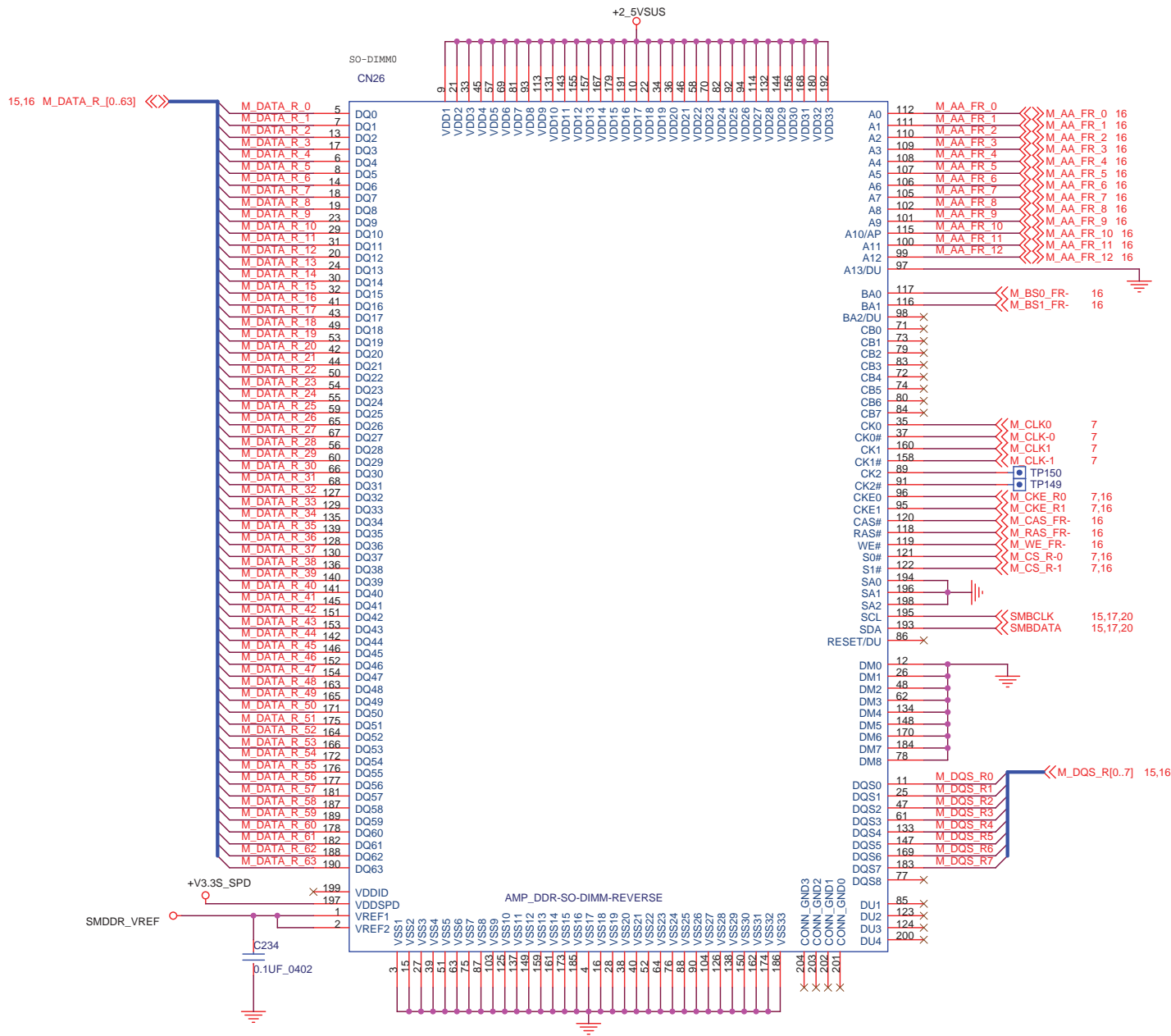
Date: Thursday, February 05, 2004 | Sheet: 10 of 43

All of signal trace 5mil spacing 10mil .

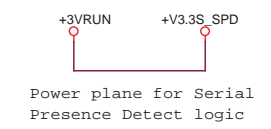
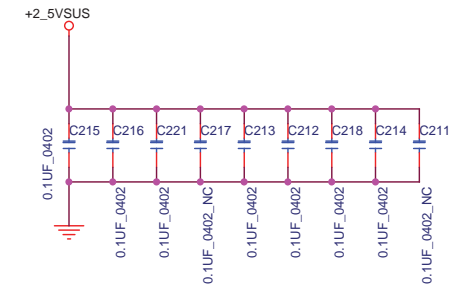
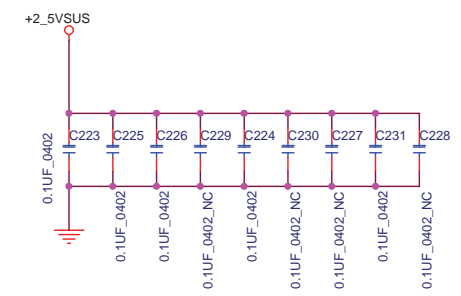
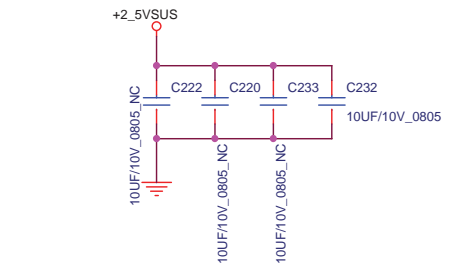


GA_MD[63..0] 10

MSI CORPORATION		
Title DDR_SG4Mx32_BGA_A		
Size Custom	Document Number MS-1003	Rev 0.C
Date: Thursday, February 05, 2004	Sheet 12	of 43



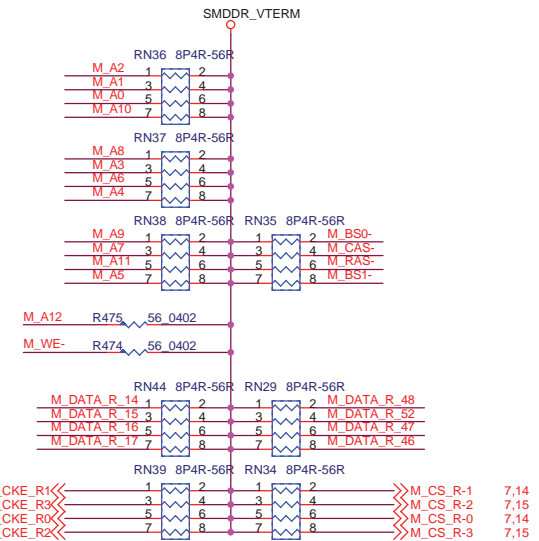
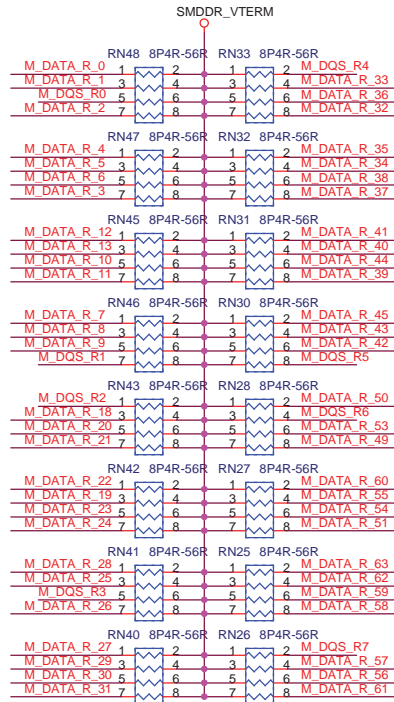
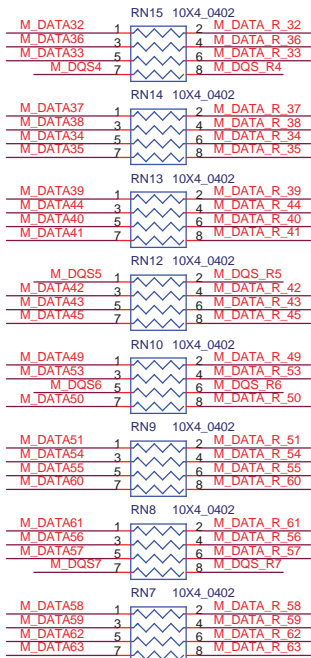
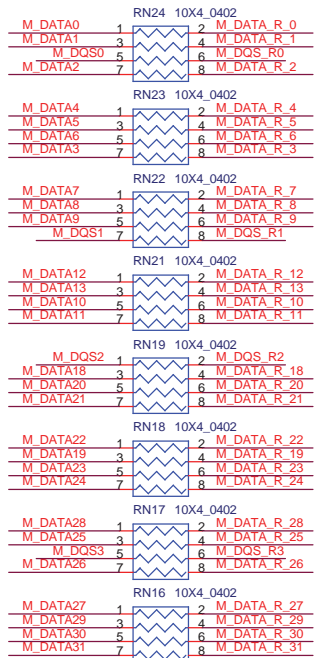
Layout note: Place capacitors between and near DDR connector if possible.



MSI CORPORATION		
Title DDR_CONNECTOR_0		
Size Custom	Document Number MS-1003	Rev 0.C
Date: Thursday, February 05, 2004	Sheet 14	of 43

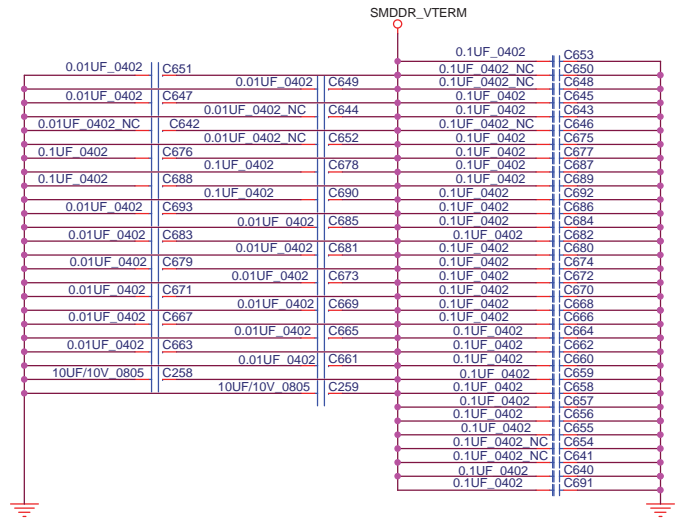
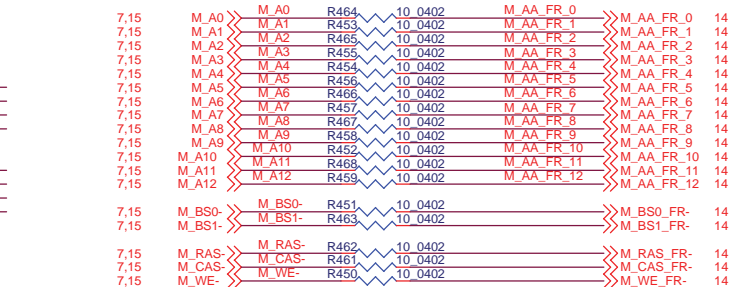
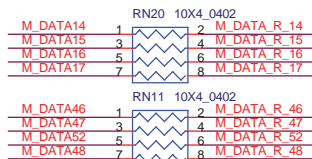
7 M_DQS[0..7] 14,15

M_DATA[0..63] 7
M_DATA_R[0..63] 14,15



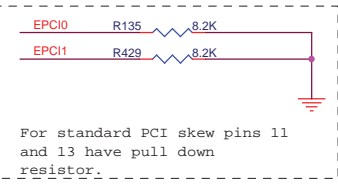
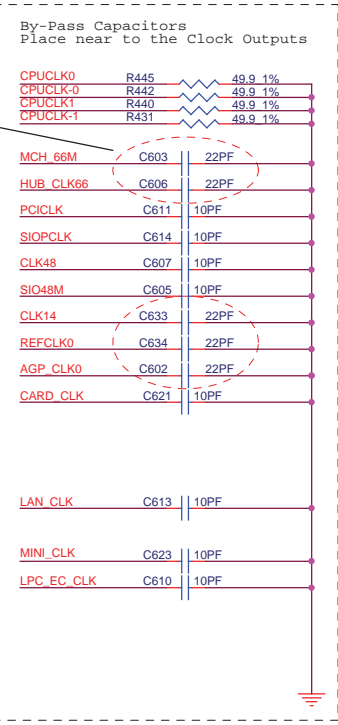
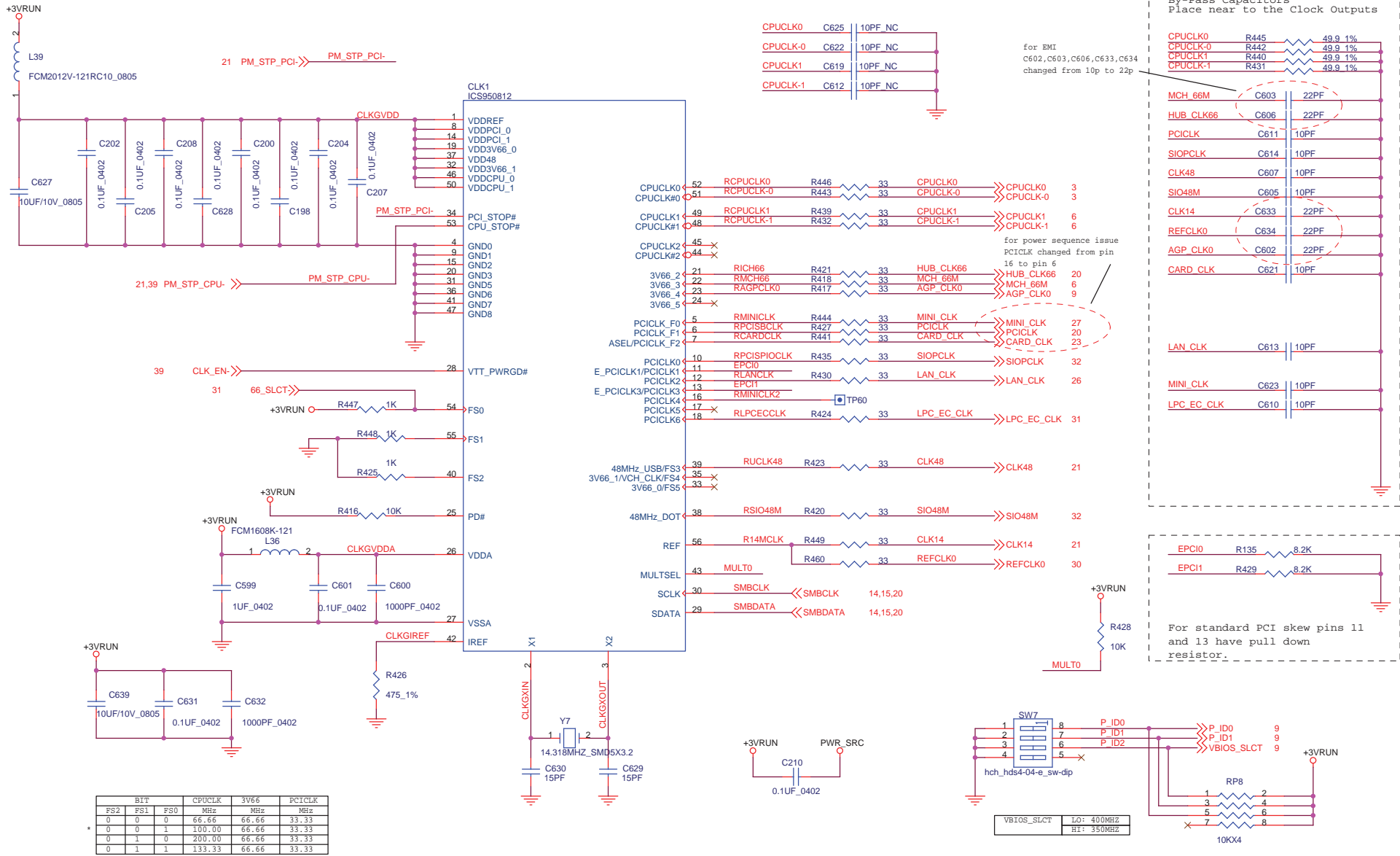
7,14 M_CKE R1<<< 1 2 3 4 >>> M_CS-R1 7,14
7,15 M_CKE R3<<< 3 4 5 6 >>> M_CS-R2 7,15
7,14 M_CKE R5<<< 5 6 7 8 >>> M_CS-R0 7,14
7,15 M_CKE R7<<< 7 8 >>> M_CS-R3 7,15

Layout note: Place one cap close to every 2 pullup resistors terminated to +V1.25.



MSI CORPORATION			
Title DDR_Series_Termination			
Size	Document Number	Rev	
Custom	MS-1003	0.C	
Date:	Thursday, February 05, 2004	Sheet	16 of 43

Main Clock Generator



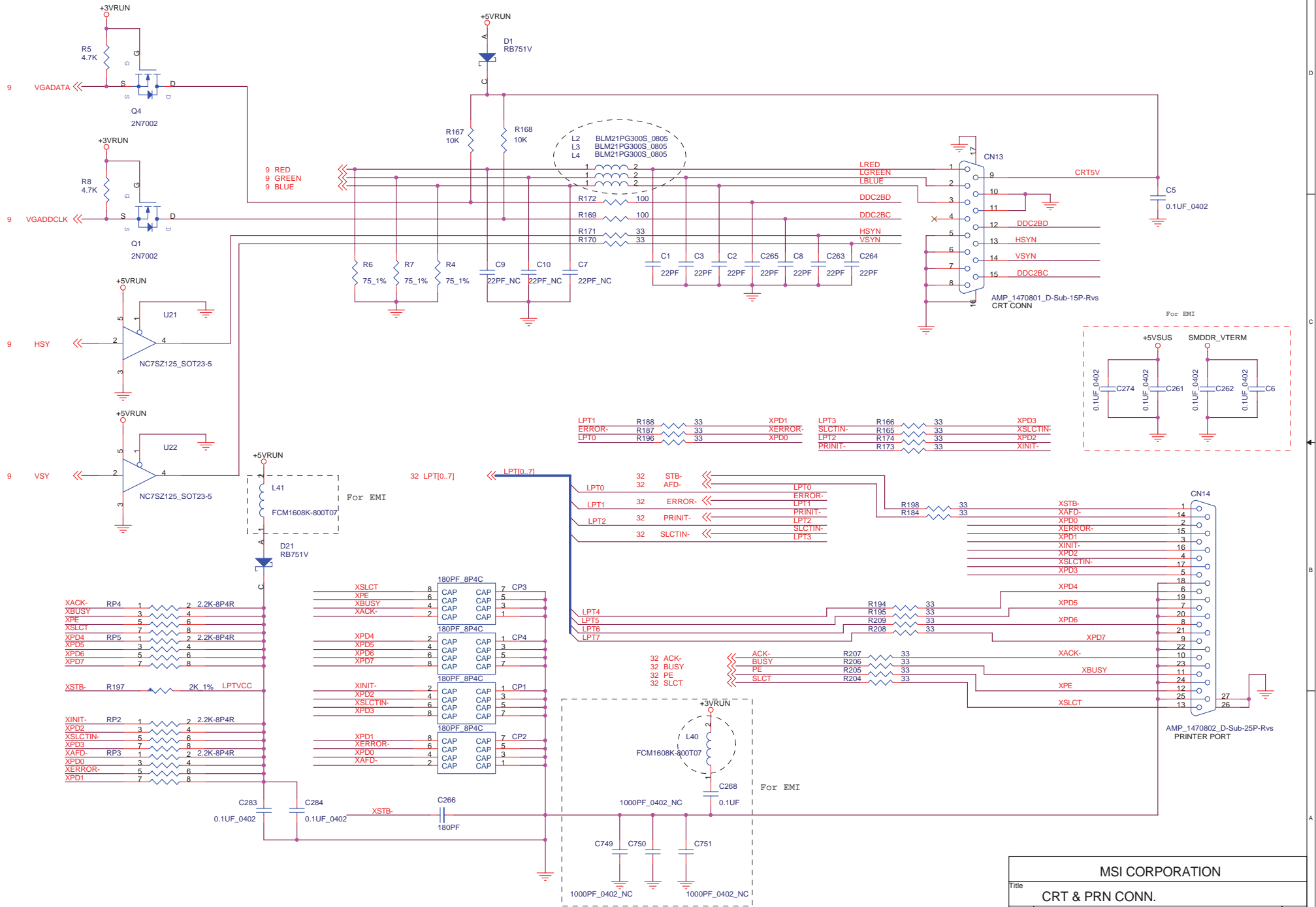
MSI CORPORATION

Title
CLOCK GENERATOR

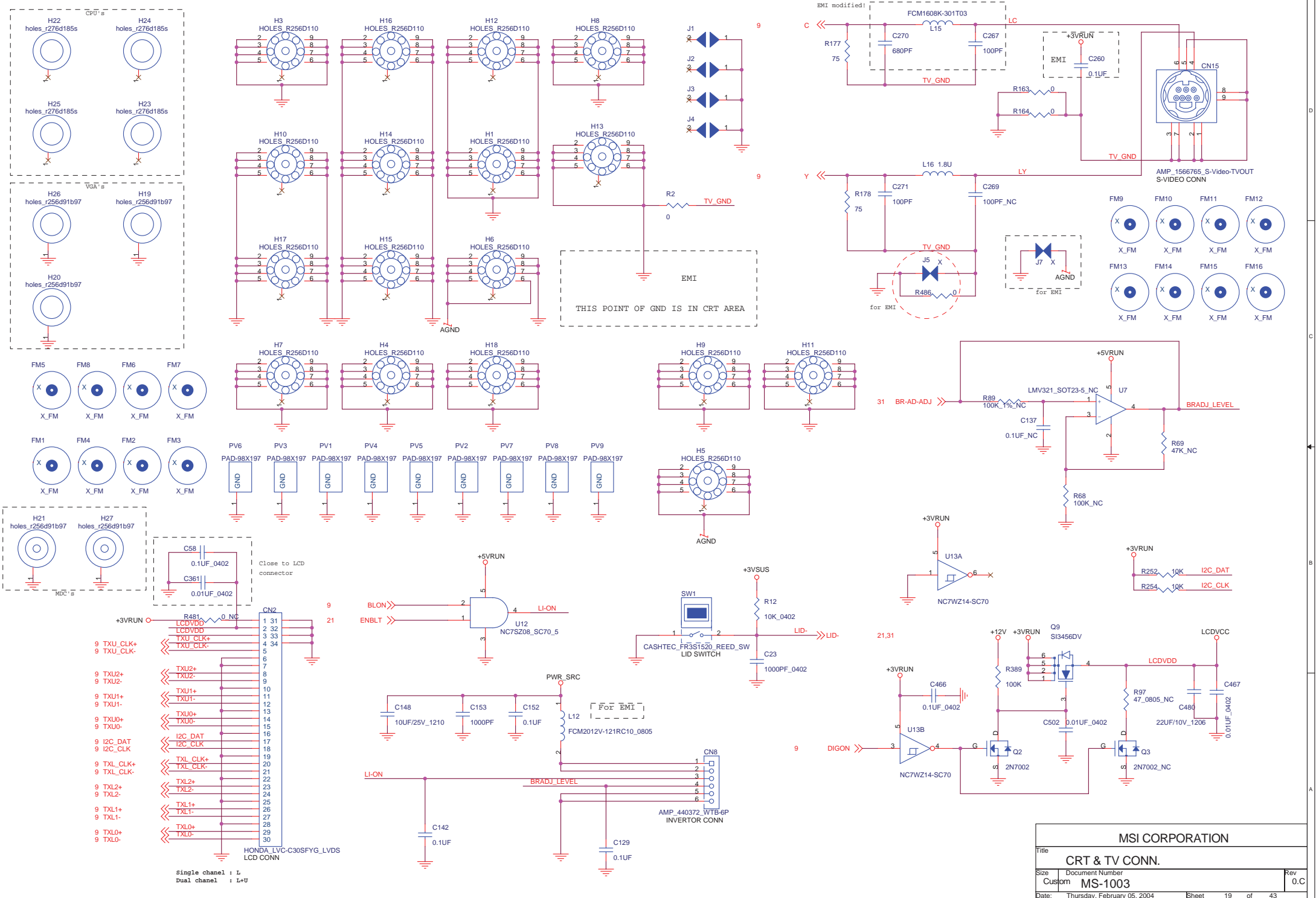
Size Custom
Document Number
MS-1003

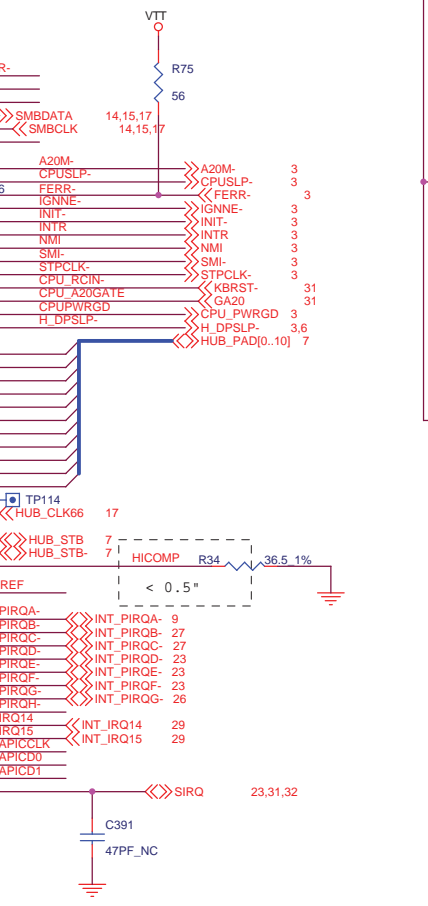
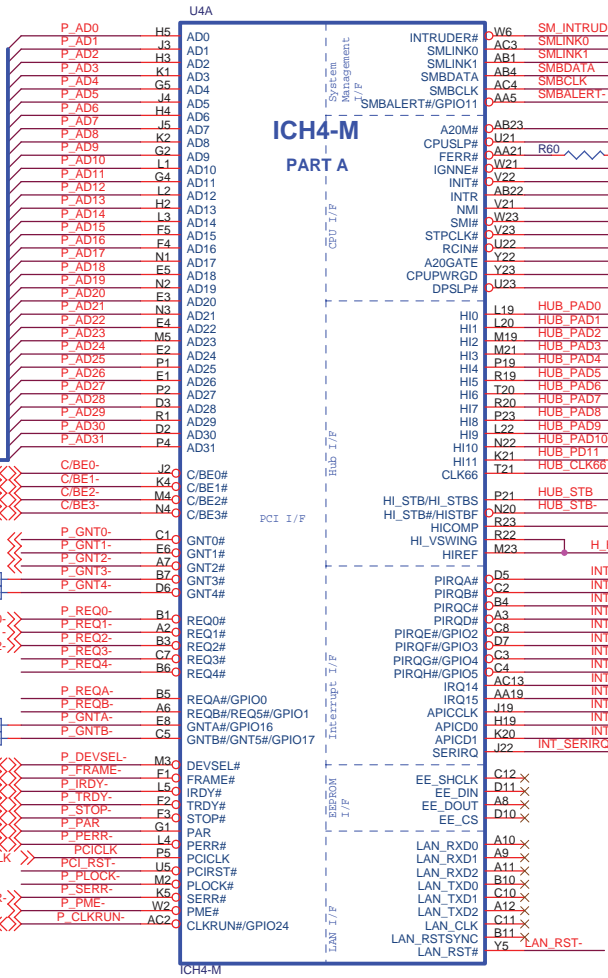
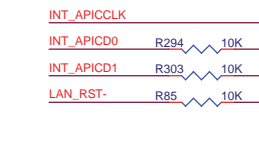
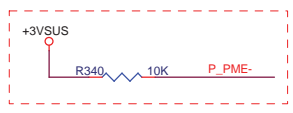
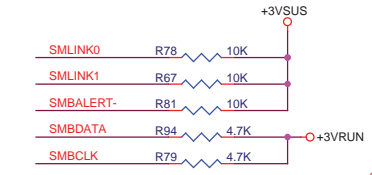
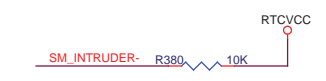
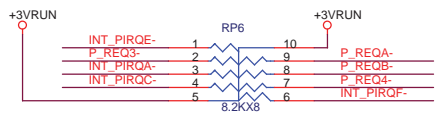
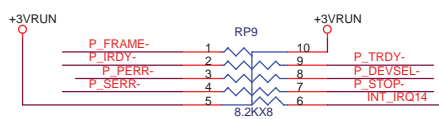
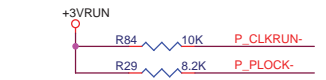
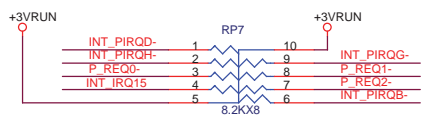
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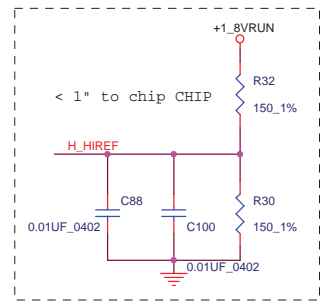
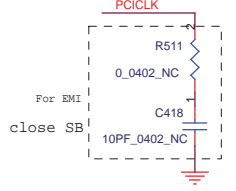
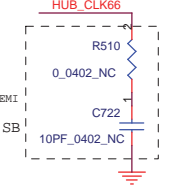
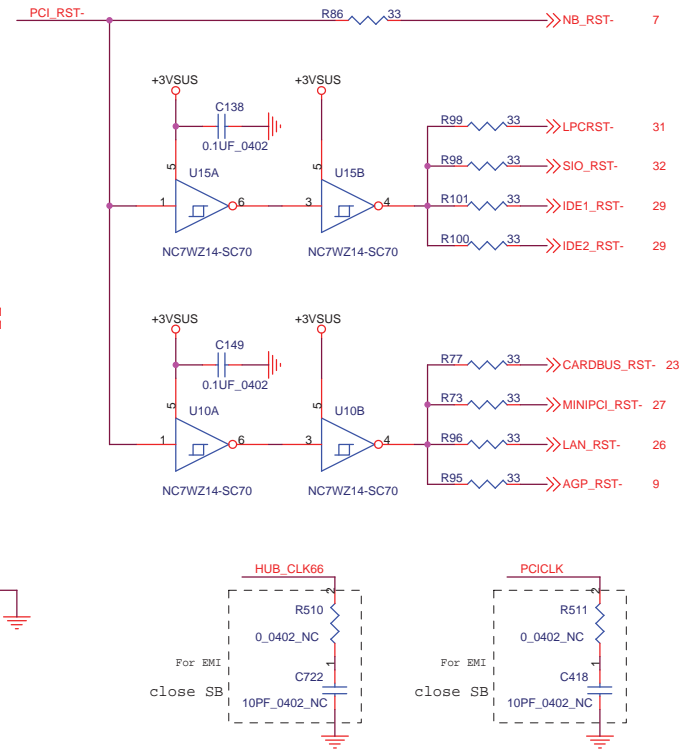


MSI CORPORATION			
Title CRT & PRN CONN.			
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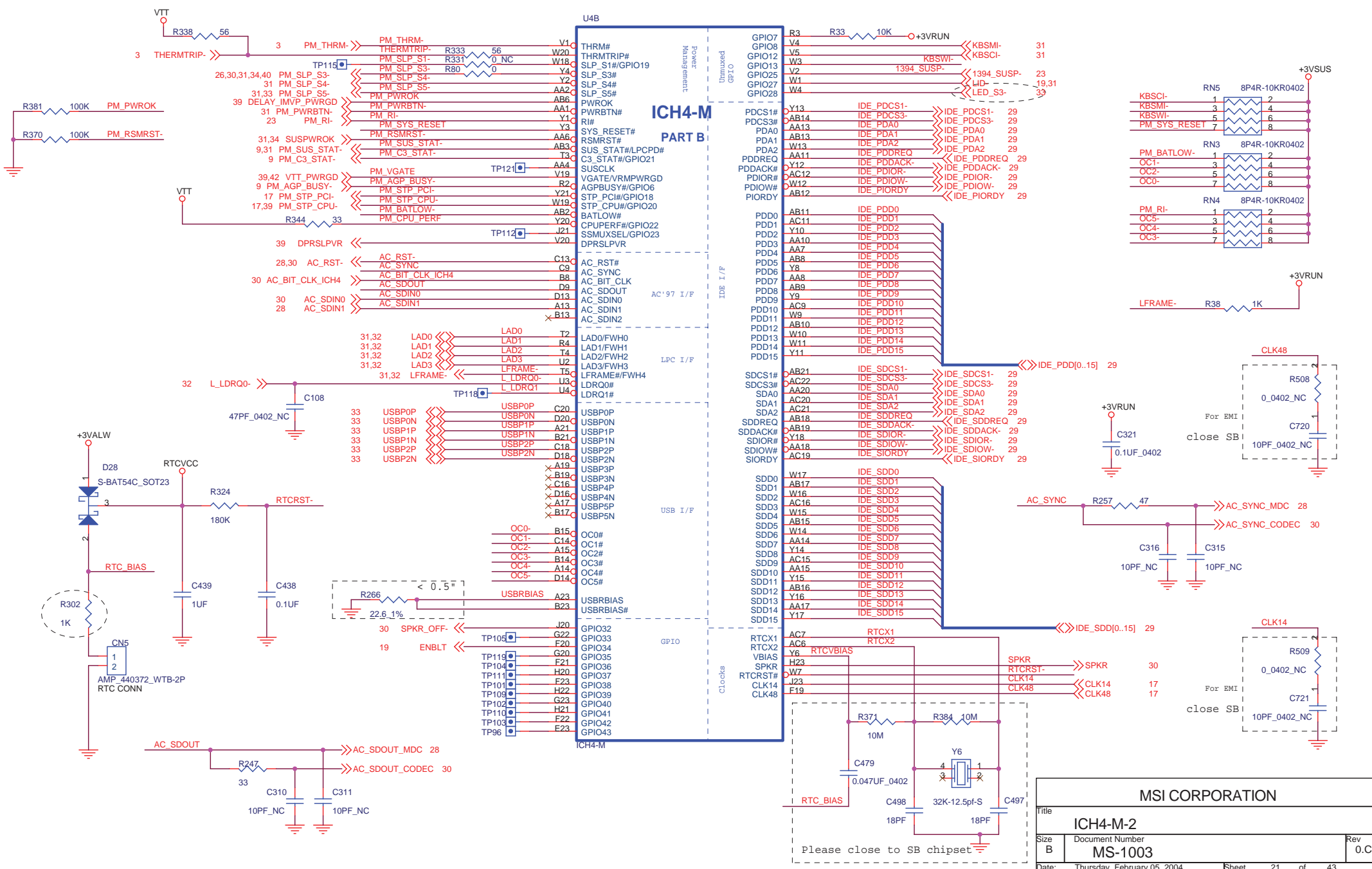




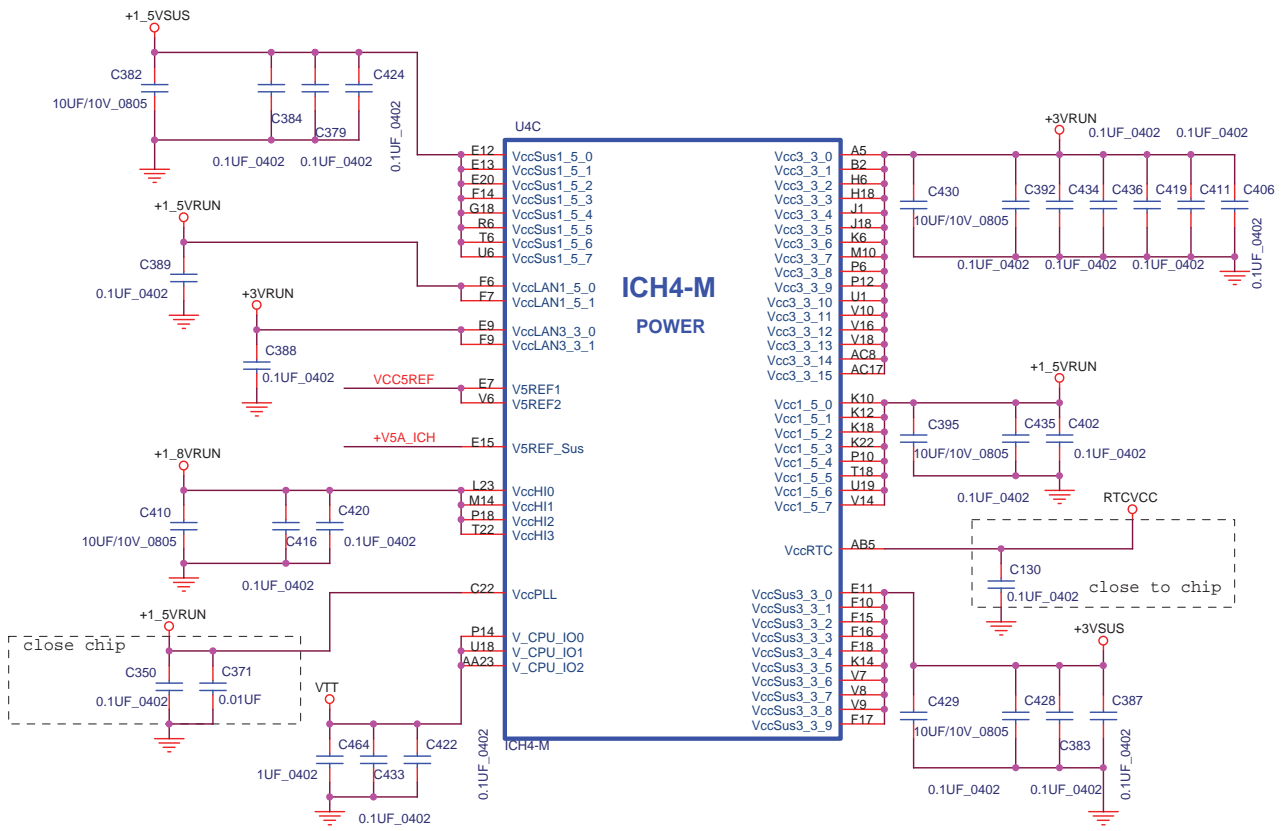
FOR PCIRST-



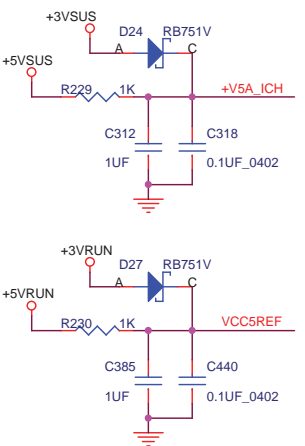
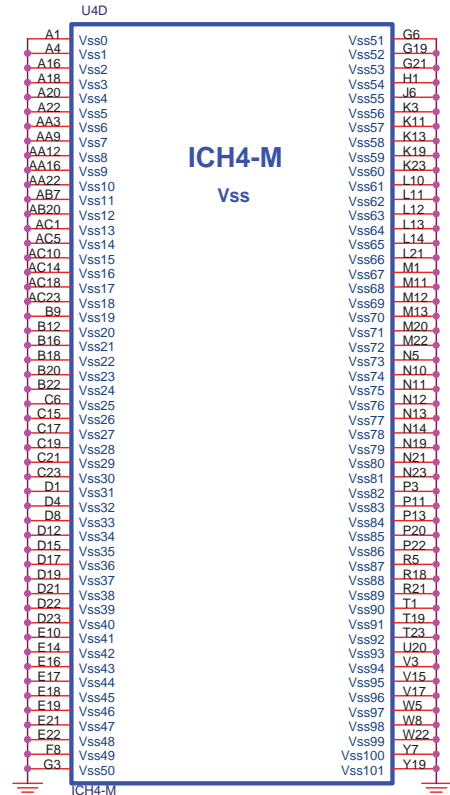
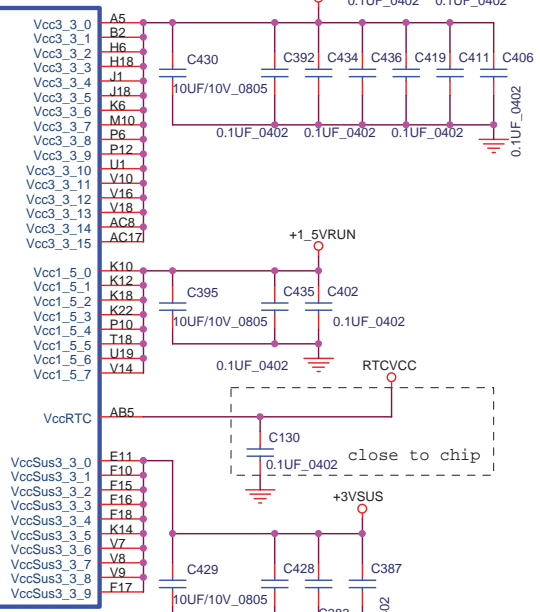
MSI CORPORATION		
Title ICH4-M-1		
Size Custom	Document Number MS-1003	Rev 0.C
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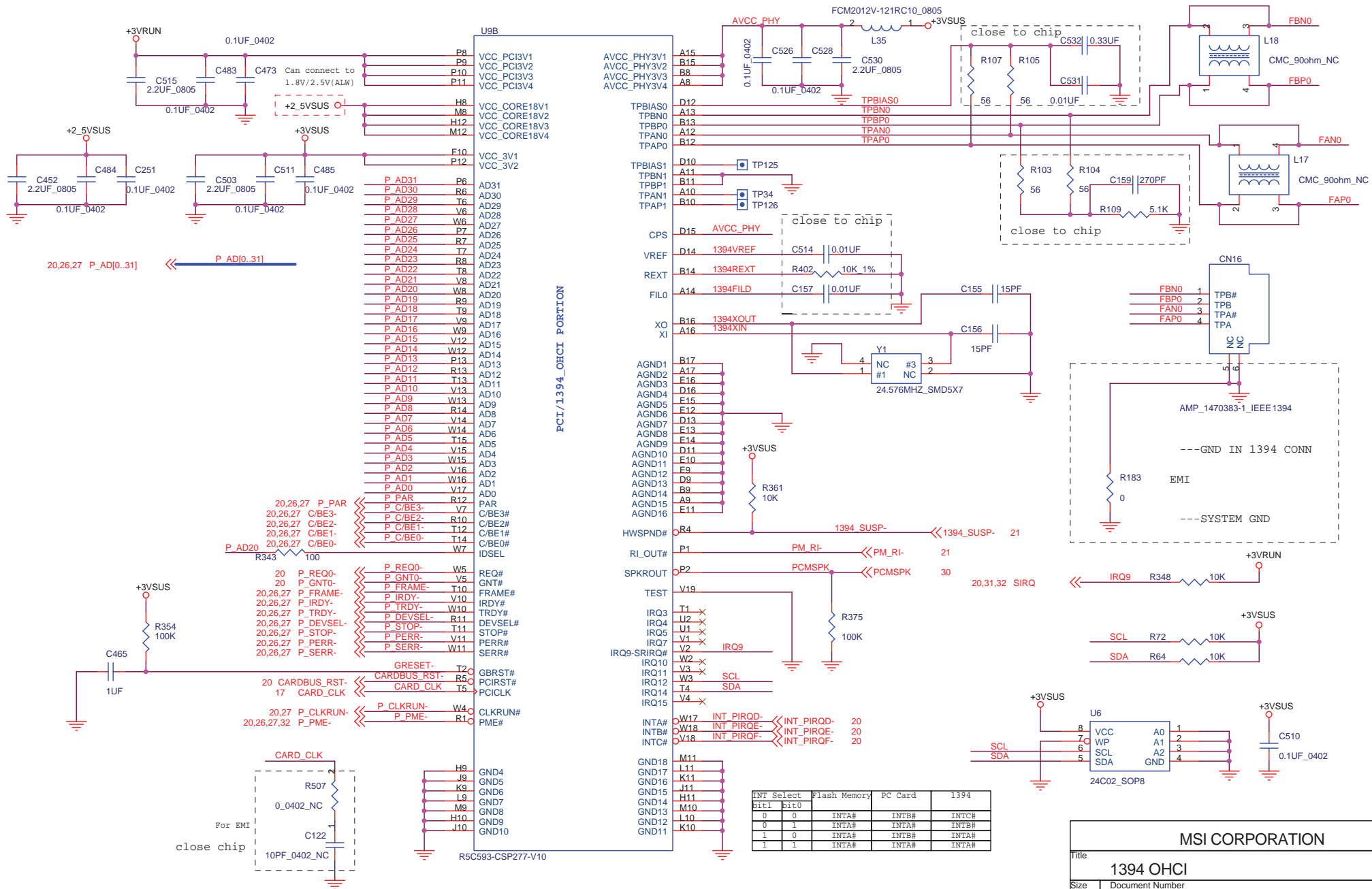
MSI CORPORATION		
Title	ICH4-M-2	
Size	Document Number	Rev
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**ICH4-M
POWER**



MSI CORPORATION		
Title ICH4-M-3 (POWER)		
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- 20,26,27 P_AD[0..31] << P_ADI0..31
- 20,26,27 P_PAR
- 20,26,27 C/BE3-
- 20,26,27 C/BE2-
- 20,26,27 C/BE1-
- 20,26,27 C/BE0-
- 20,26,27 P_REQ0-
- 20,26,27 P_GNT0-
- 20,26,27 P_FRAME-
- 20,26,27 P_IRDY-
- 20,26,27 P_TRDY-
- 20,26,27 P_DEVSEL-
- 20,26,27 P_STOP-
- 20,26,27 P_PERR-
- 20,26,27 P_SERR-
- 20 CARDBUS_RST-
- 17 CARD_CLK
- 20,27 P_CLKRUN-
- 20,26,27,32 P_PME-

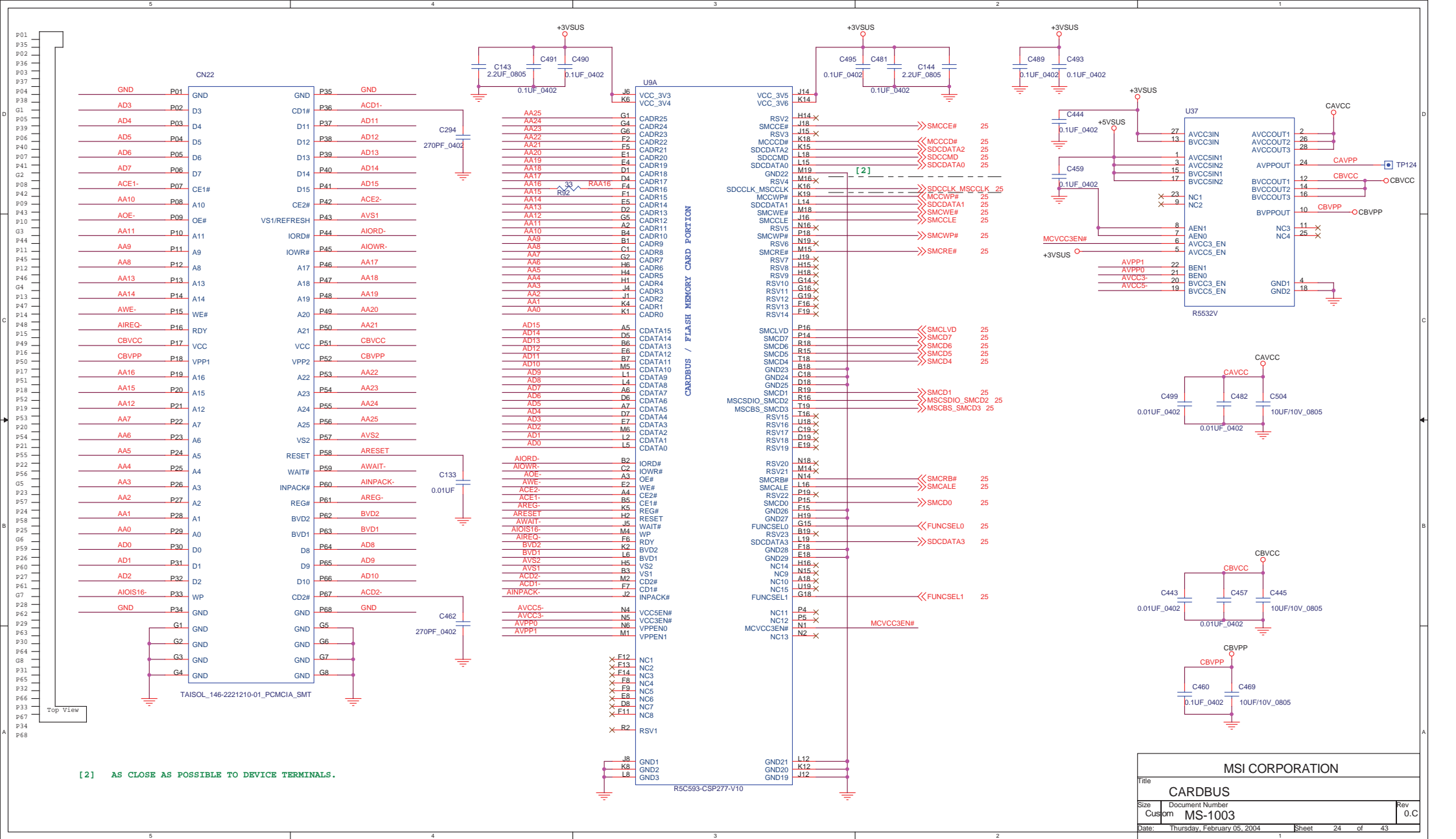
INT Select	Flash Memory	PC Card	1394
0 0	INTFA#	INTB#	INTC#
0 1	INTFA#	INTFA#	INTB#
1 0	INTFA#	INTB#	INTFA#
1 1	INTFA#	INTFA#	INTFA#

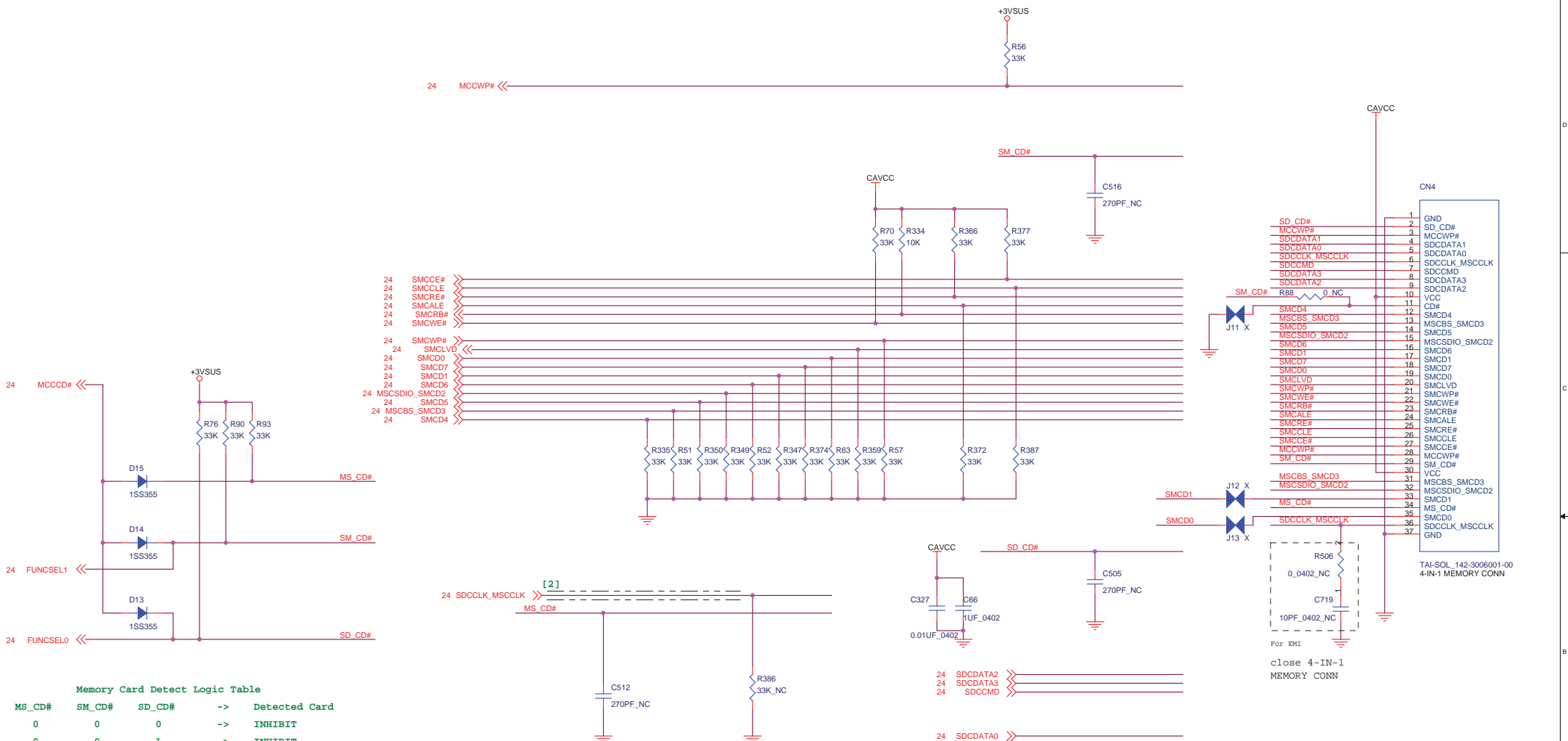
MSI CORPORATION

Title: **1394 OHCI**

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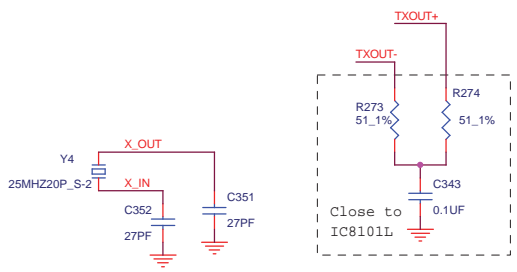
Memory Card Detect Logic Table

MS_CD#	SM_CD#	SD_CD#	Detected Card
0	0	0	-> INHIBIT
0	0	1	-> INHIBIT
0	1	0	-> INHIBIT
0	1	1	-> MemoryStick Detected
1	0	0	-> INHIBIT
1	0	1	-> SmartMedia Detected
1	1	0	-> SD/MMC Detected
1	1	1	-> Not Detected

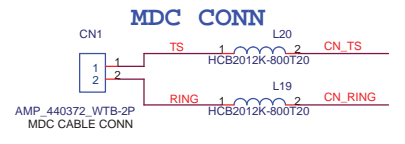
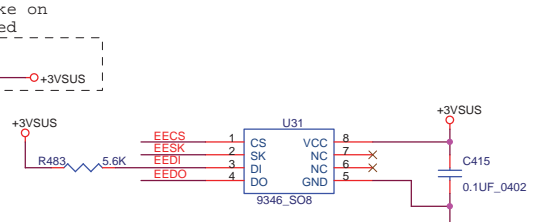
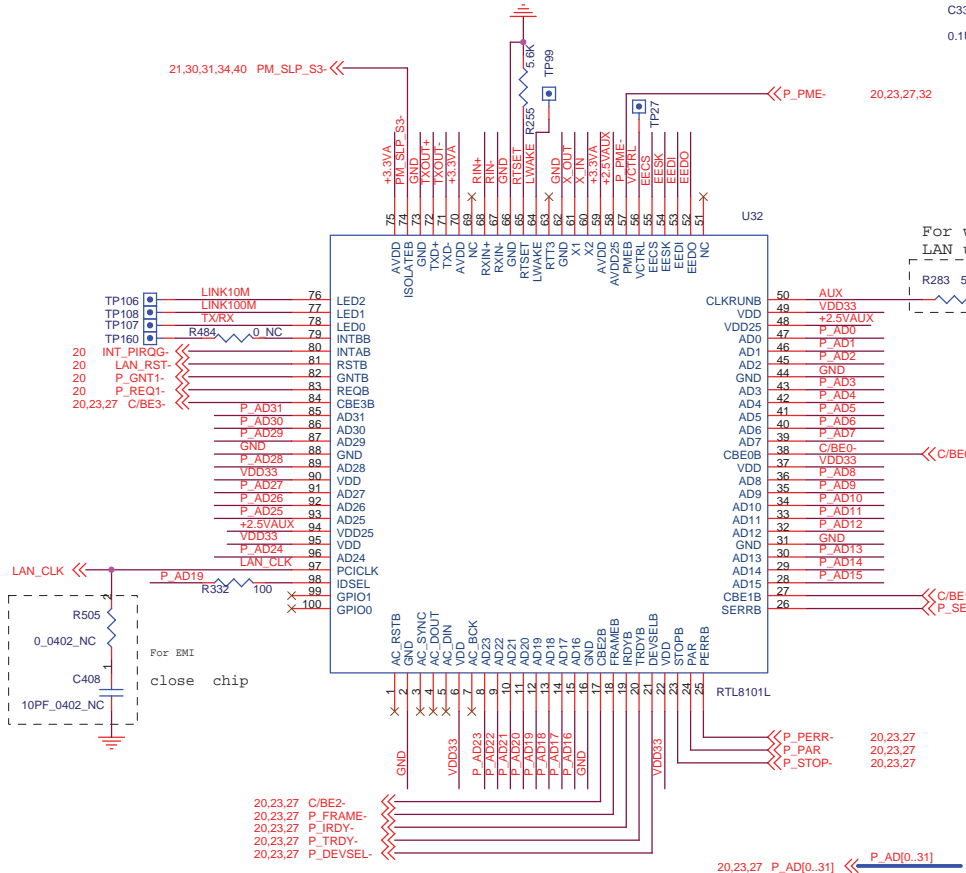
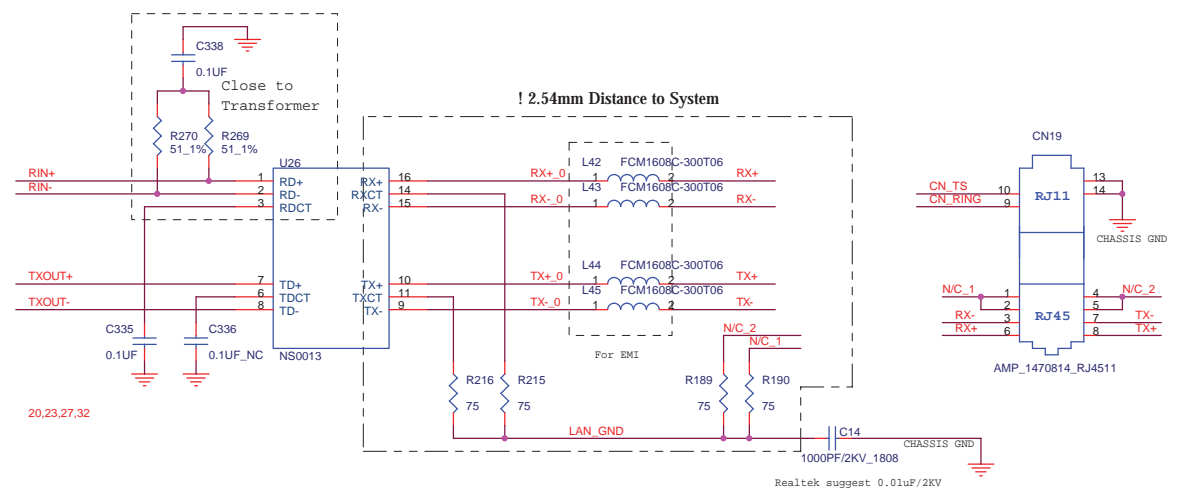
DO NOT INSERT SMARTMEDIA, SD/MMC AND MEMORYSTICK SIMULTANEOUSLY.

[2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.

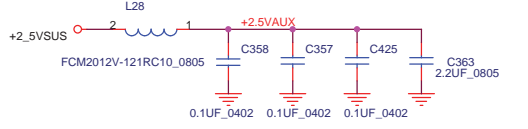
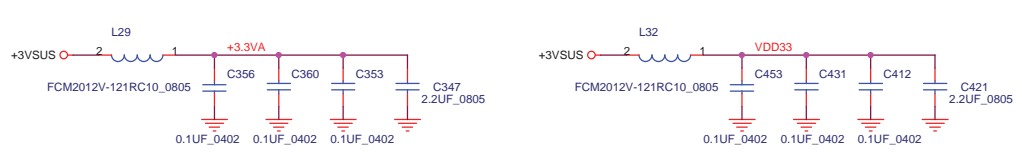
MSI CORPORATION			
Title FLASH CARD CONN.			
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Lay out Rule :
 1. Tx+/- and Rx+/- length : +100mil
 2. Through hole less .
 3. Tx+/- _____
 Rx+/- _____
 Ground separates Tx/Rx .



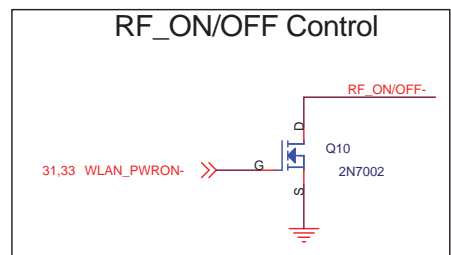
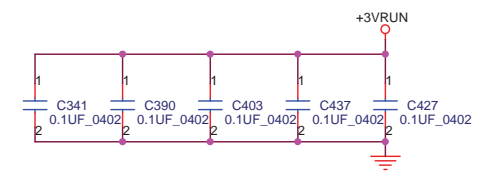
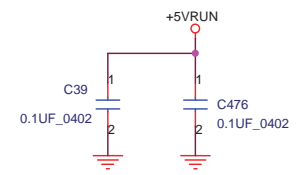
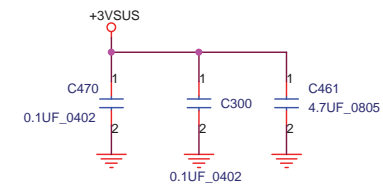
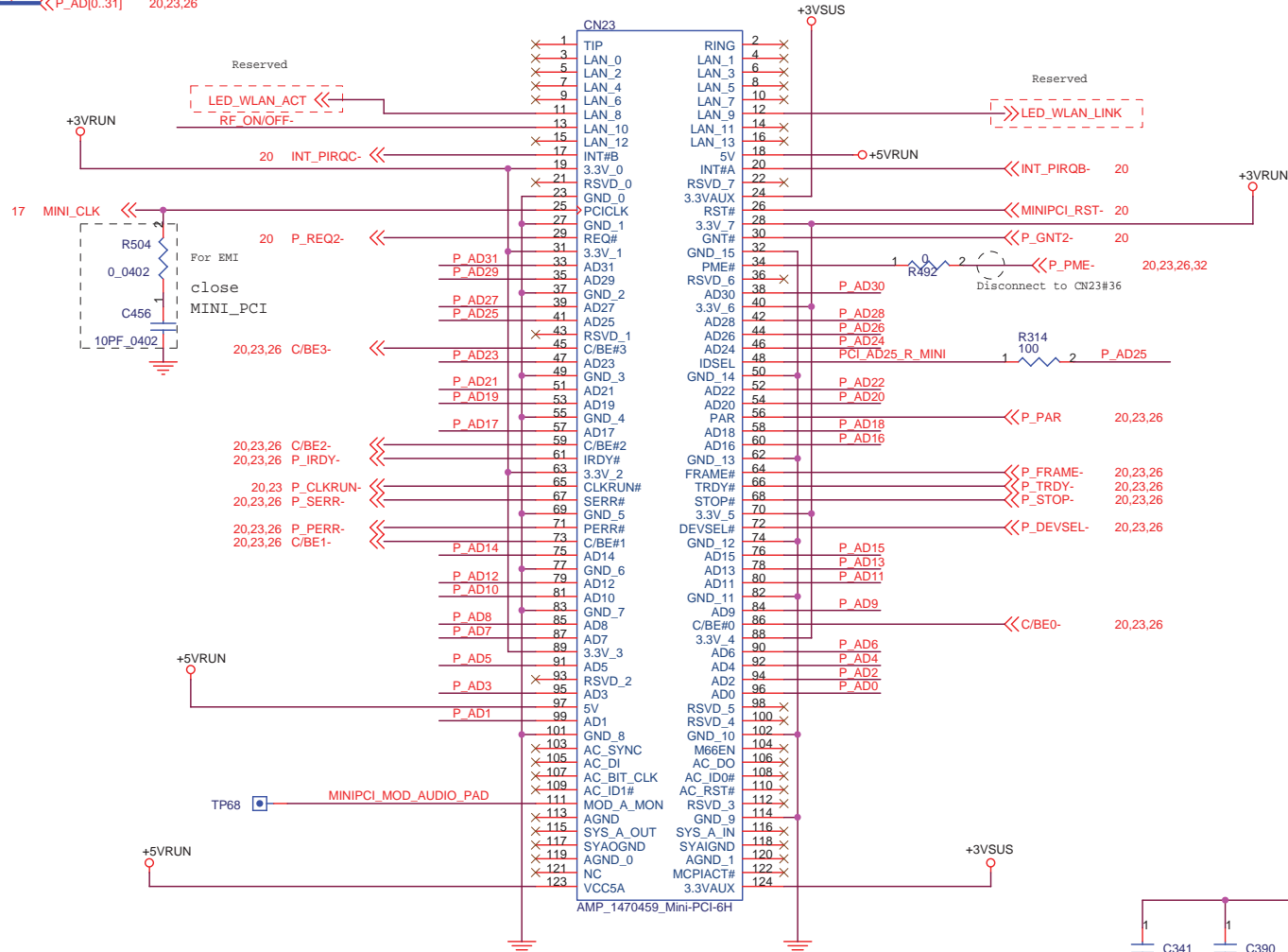
OTHER SIGNALS ARE FAR AWAY THIS TWO TRACES.
 *** THIS DISTANCE IS MIN. 2.5mm***
 ***THIS SPACE IS IN 3D SPACE AND INCLUDE ANY ***
 ***POWER ANG GROUND ***



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Title LAN		
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MINI PCI SOCKET

P_AD10..31 << P_AD[0..31] 20,23,26



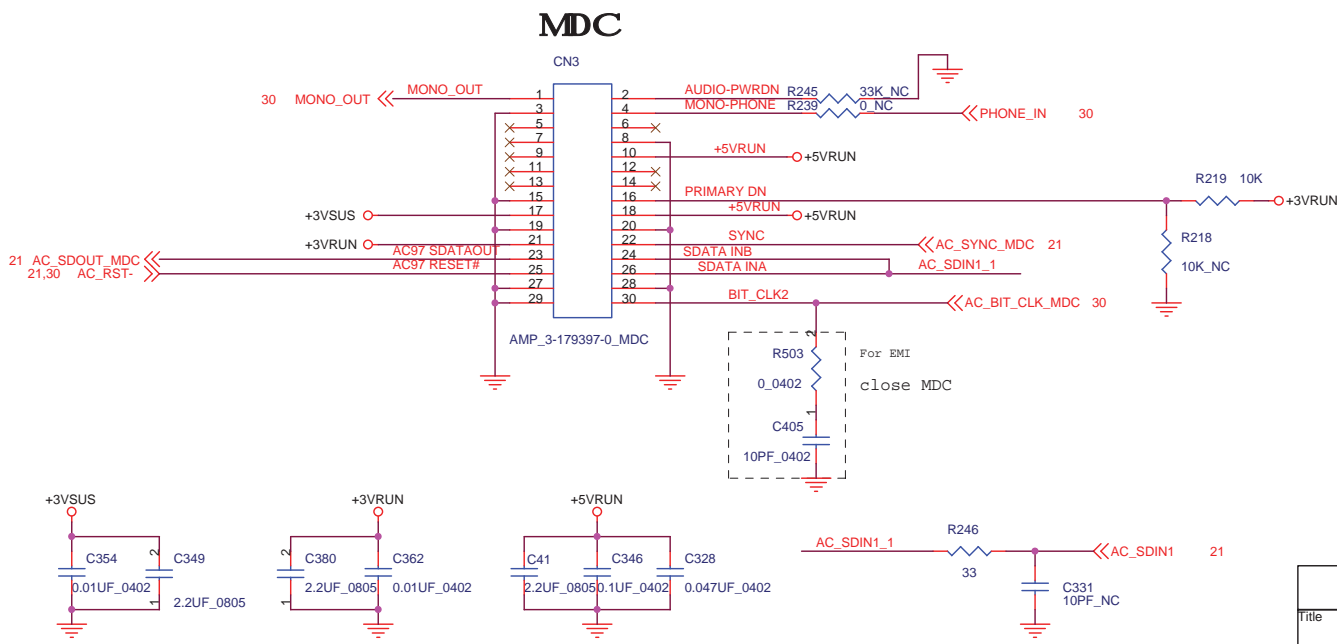
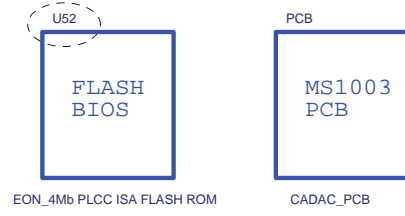
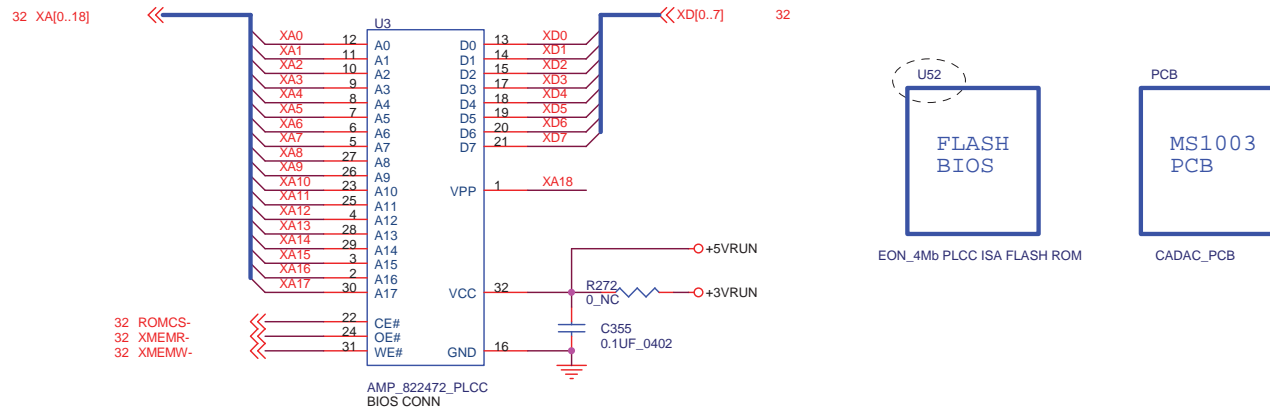
**OPEN RF ON (HiZ)
 LOW RF OFF**

FOR G551 :
 PHONE AND MONO_OUT NOT USE

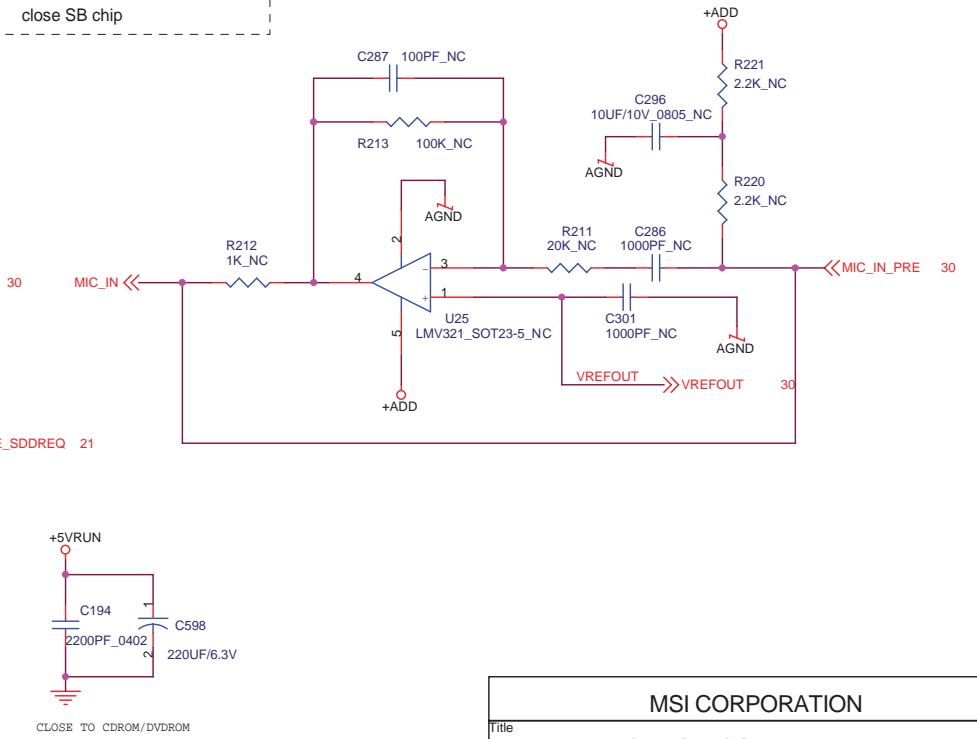
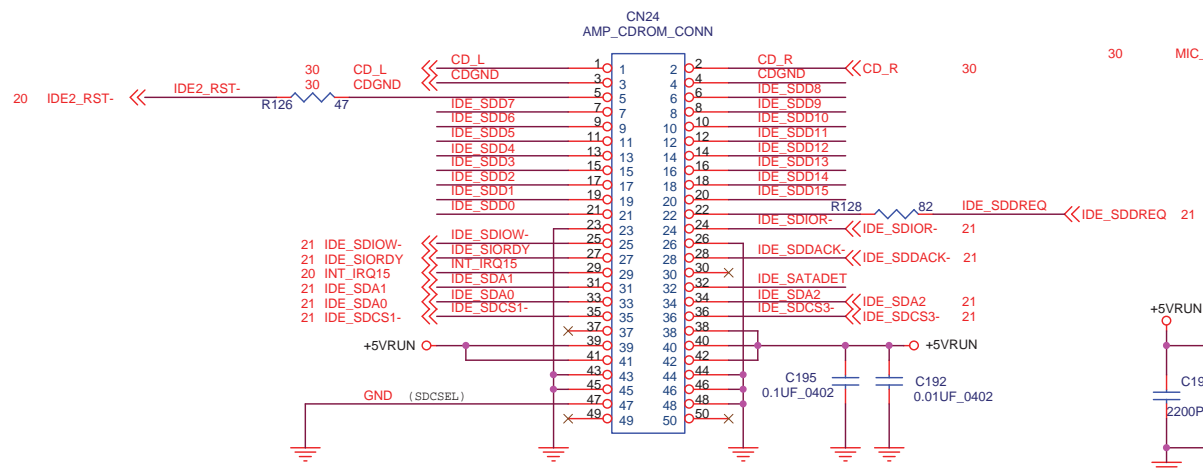
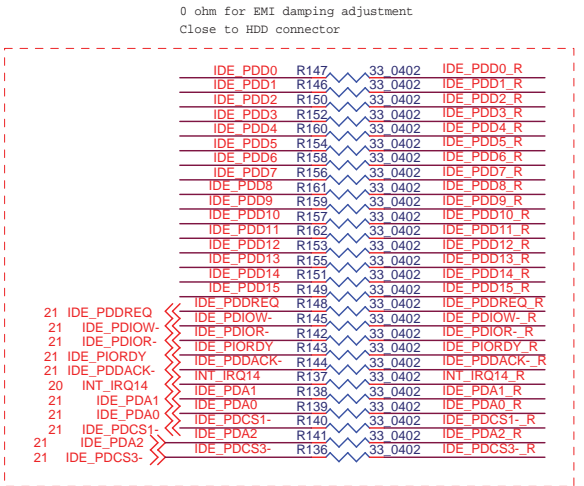
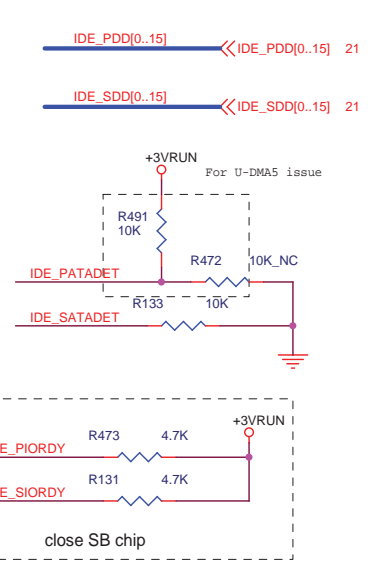
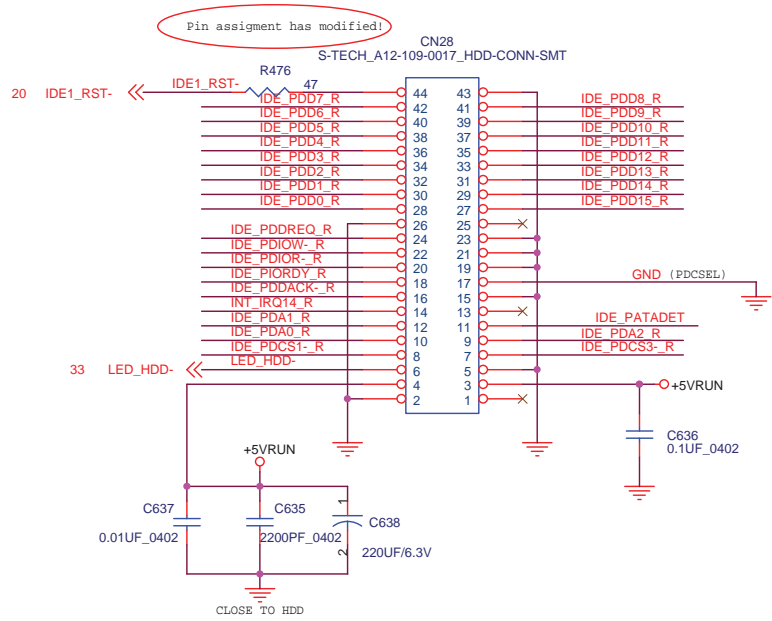
MINI PCI POWER SPEC.

TOYAL	: 2W
+5V	: 100mA
3.3VAUX	: 5/200/375mA
VCC5A	: 100mA
+3V	

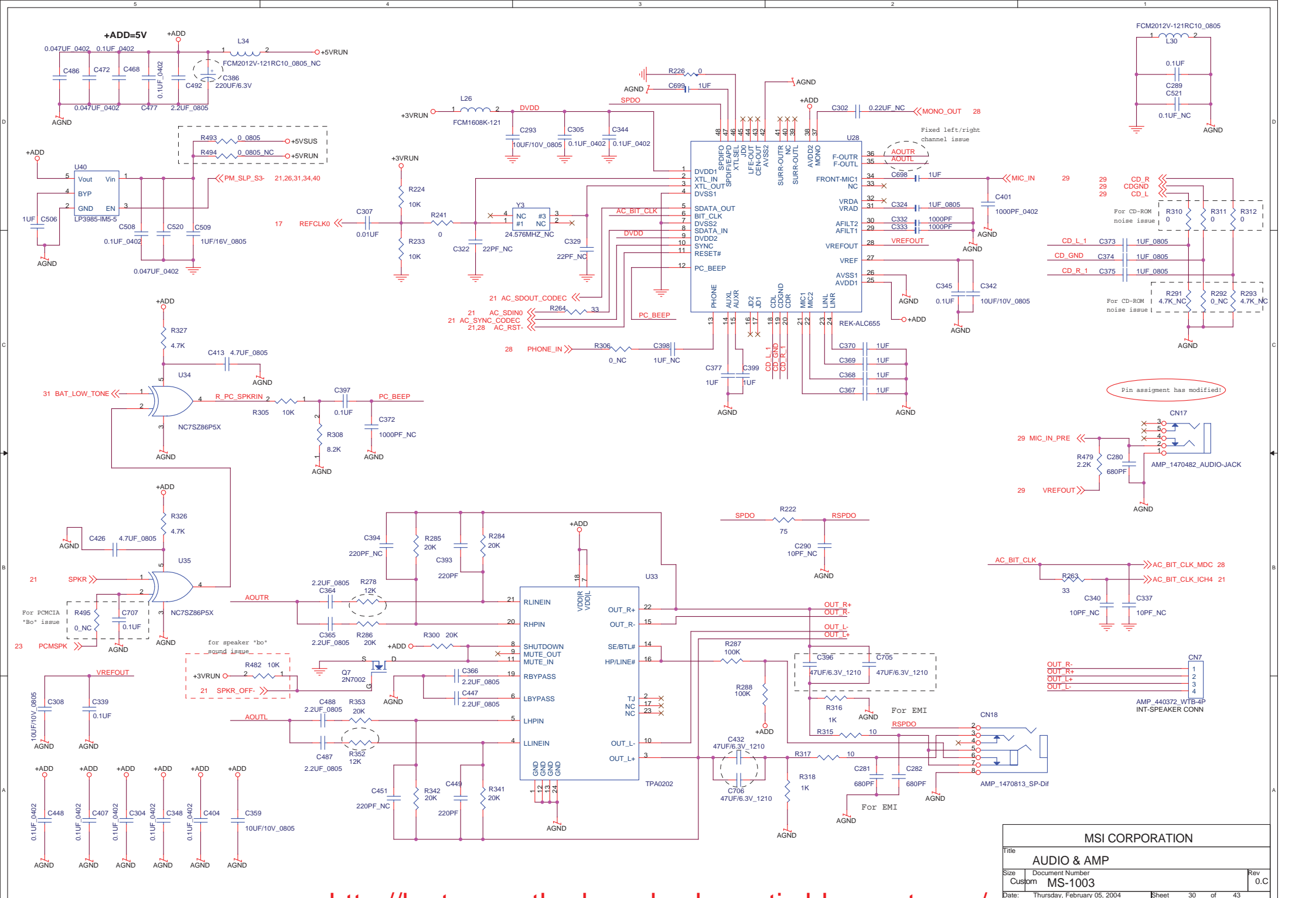
MSI CORPORATION		
Title MINIPCI		
Size B	Document Number MS-1003	Rev 0.C
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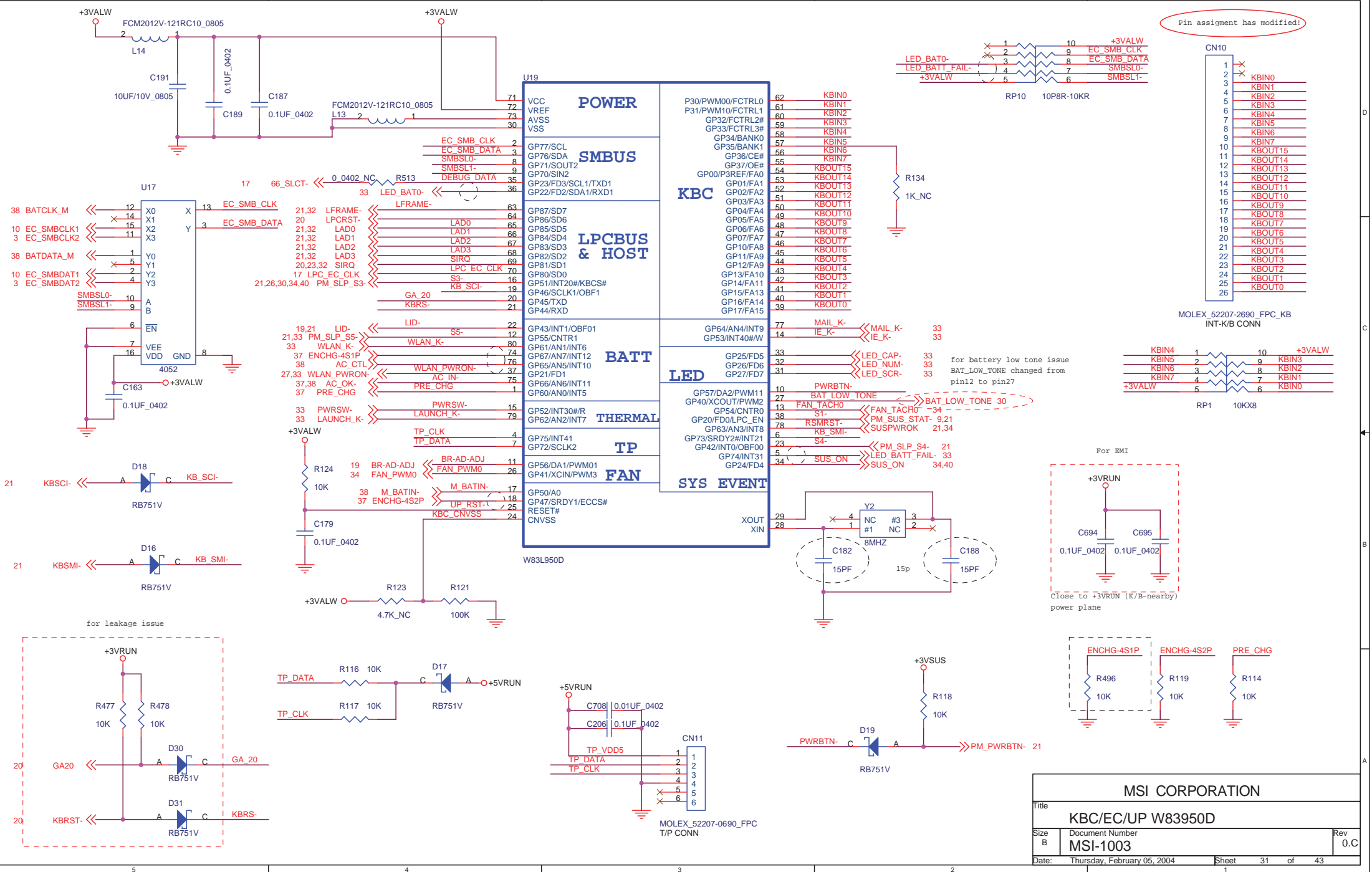
MSI CORPORATION		
Title BIOS & MDC		
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MSI CORPORATION		
Title HDD & CDROM CONN.		
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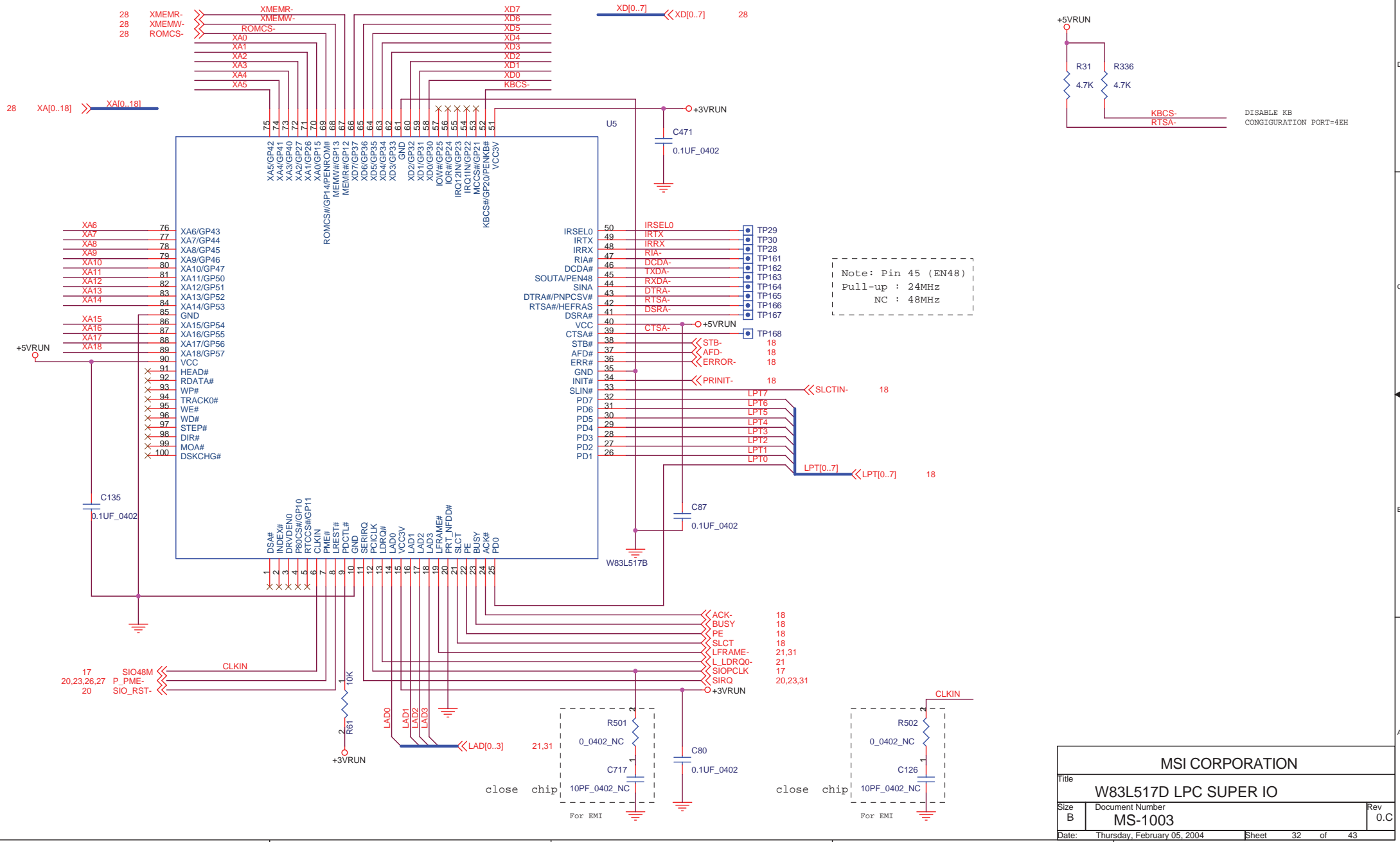


MSI CORPORATION			
Title	AUDIO & AMP		
Size	Document Number	Rev	0.C
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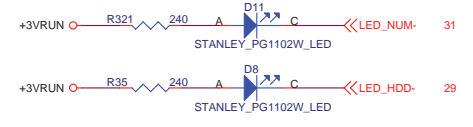
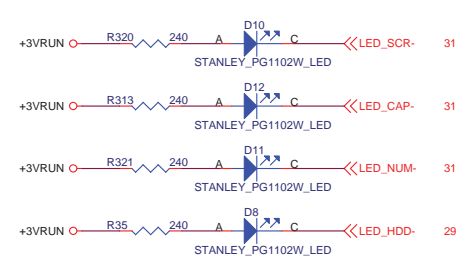
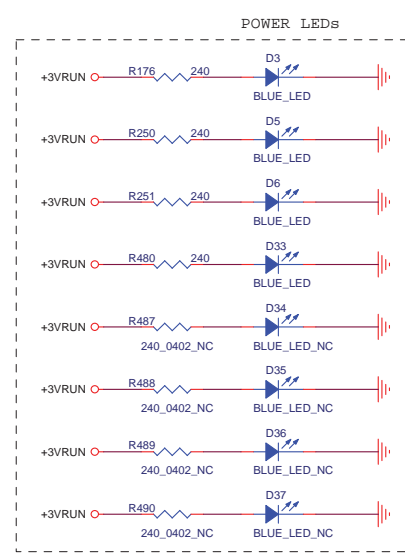
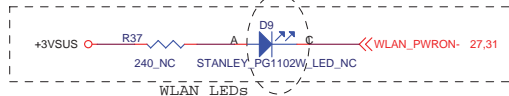
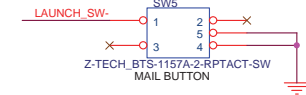
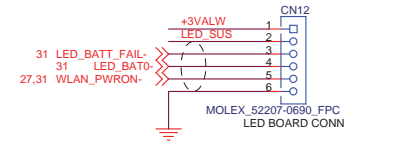
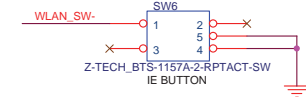
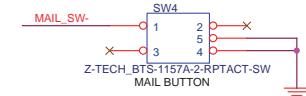
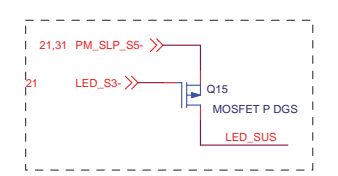
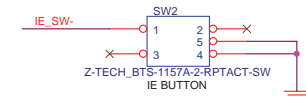
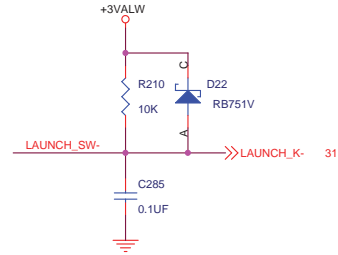
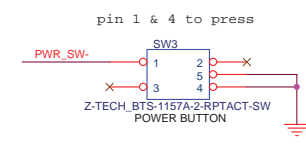
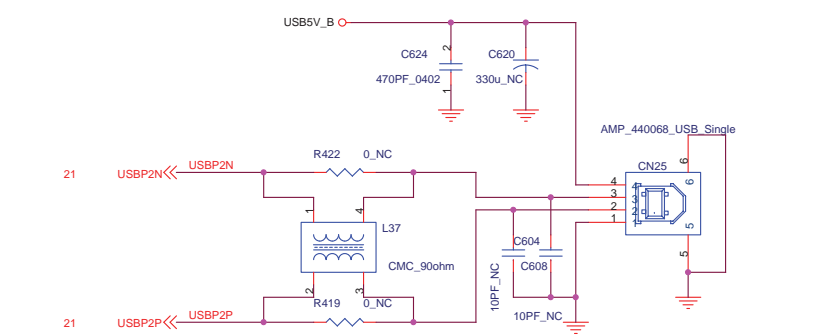
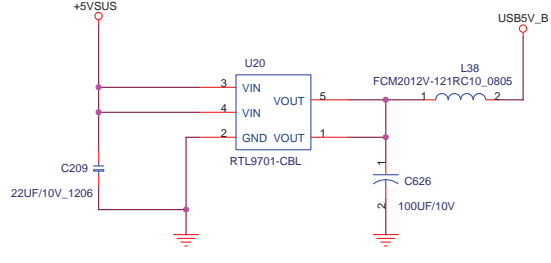
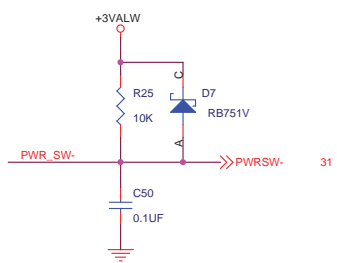
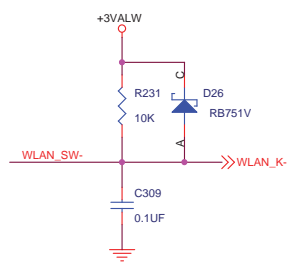
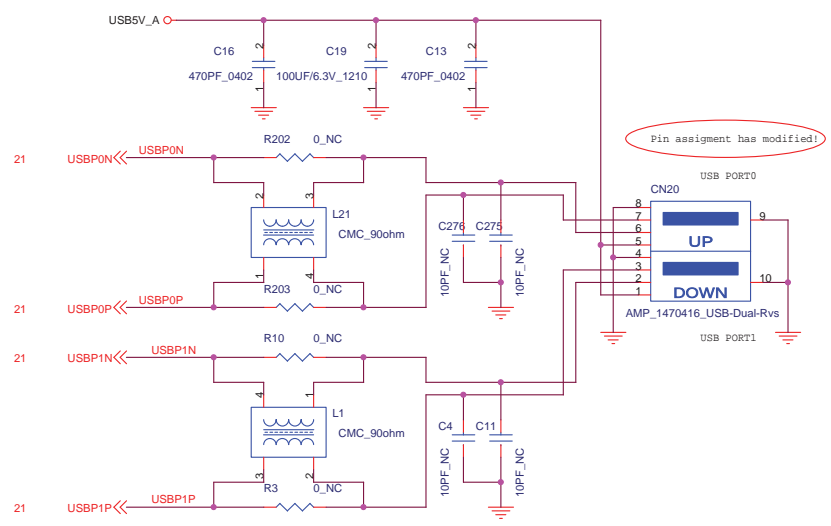
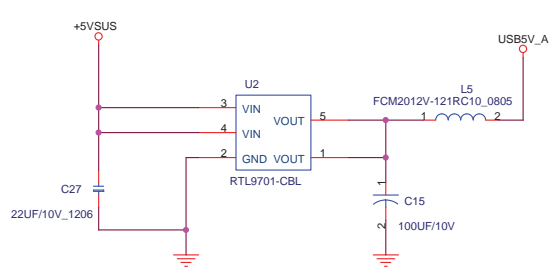
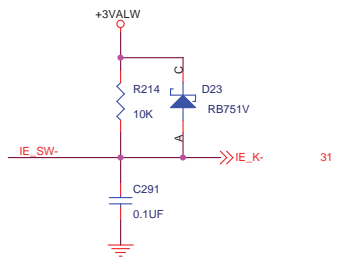
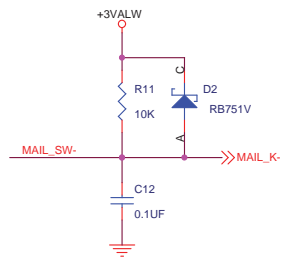


Pin assignment has modified!

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Title	KBC/EC/UP W83950D	
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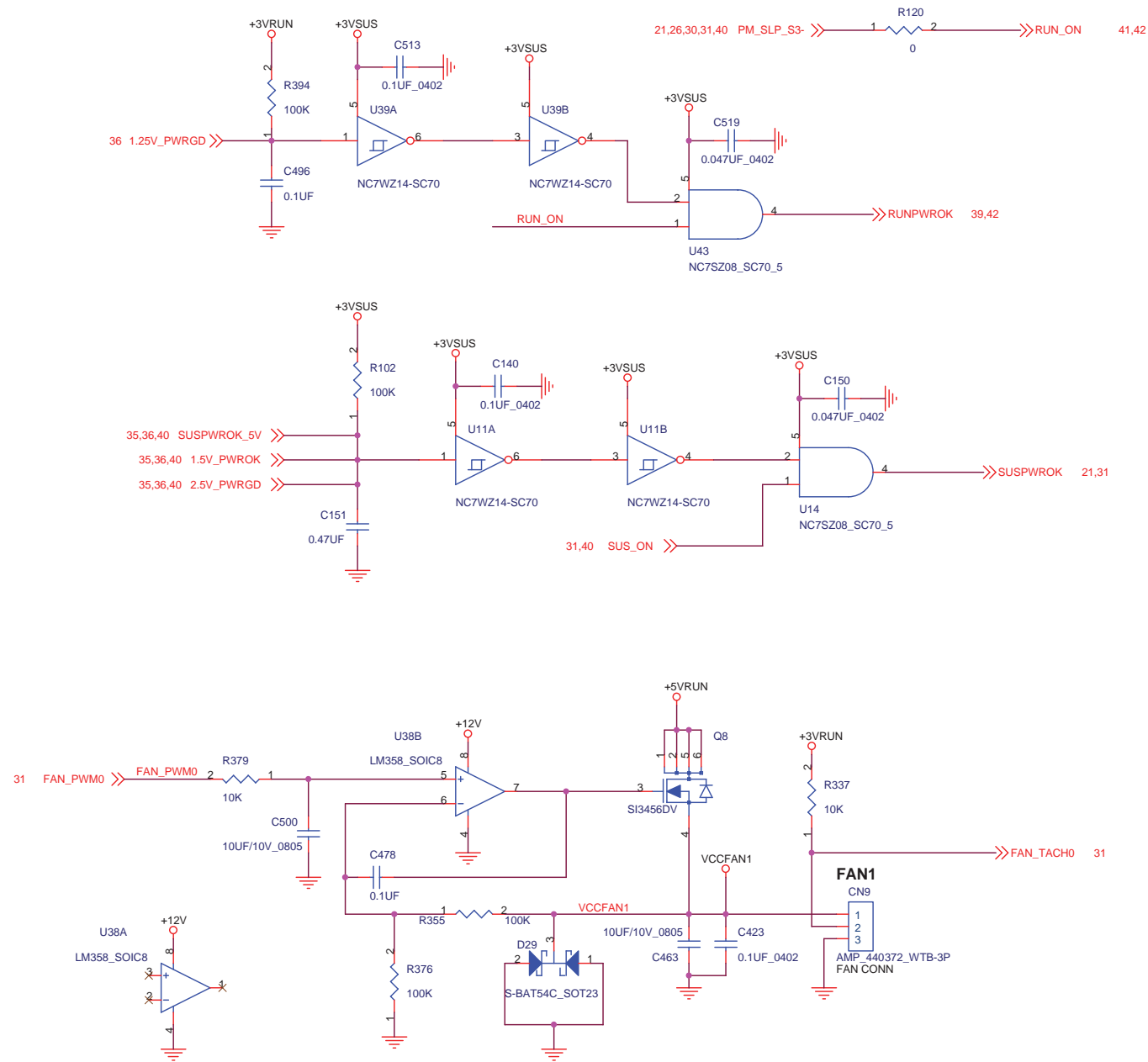


MSI CORPORATION		
Title W83L517D LPC SUPER IO		
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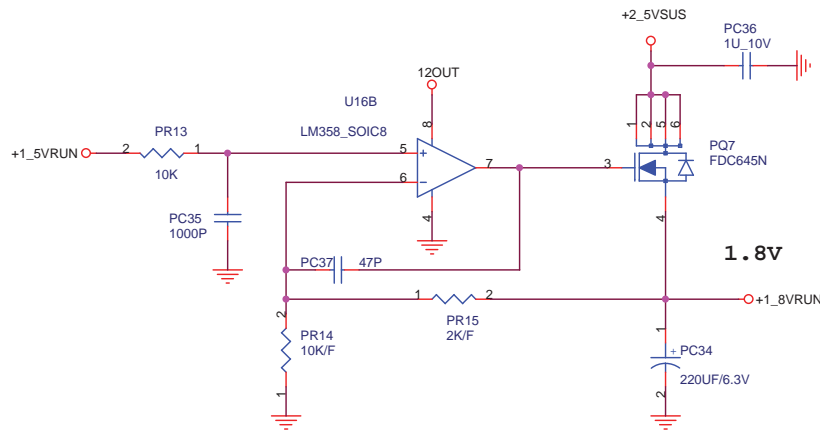
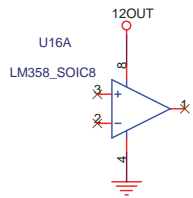
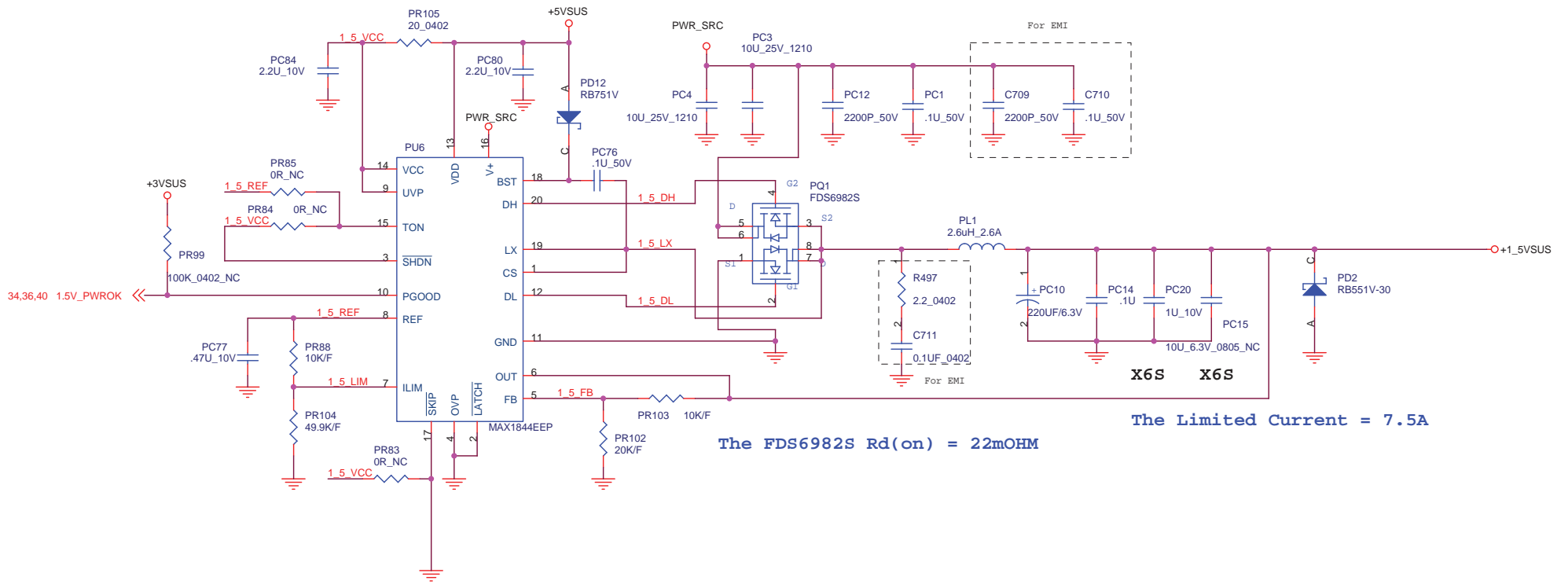


MSI CORPORATION		
Title	USB PORT & LEDs	
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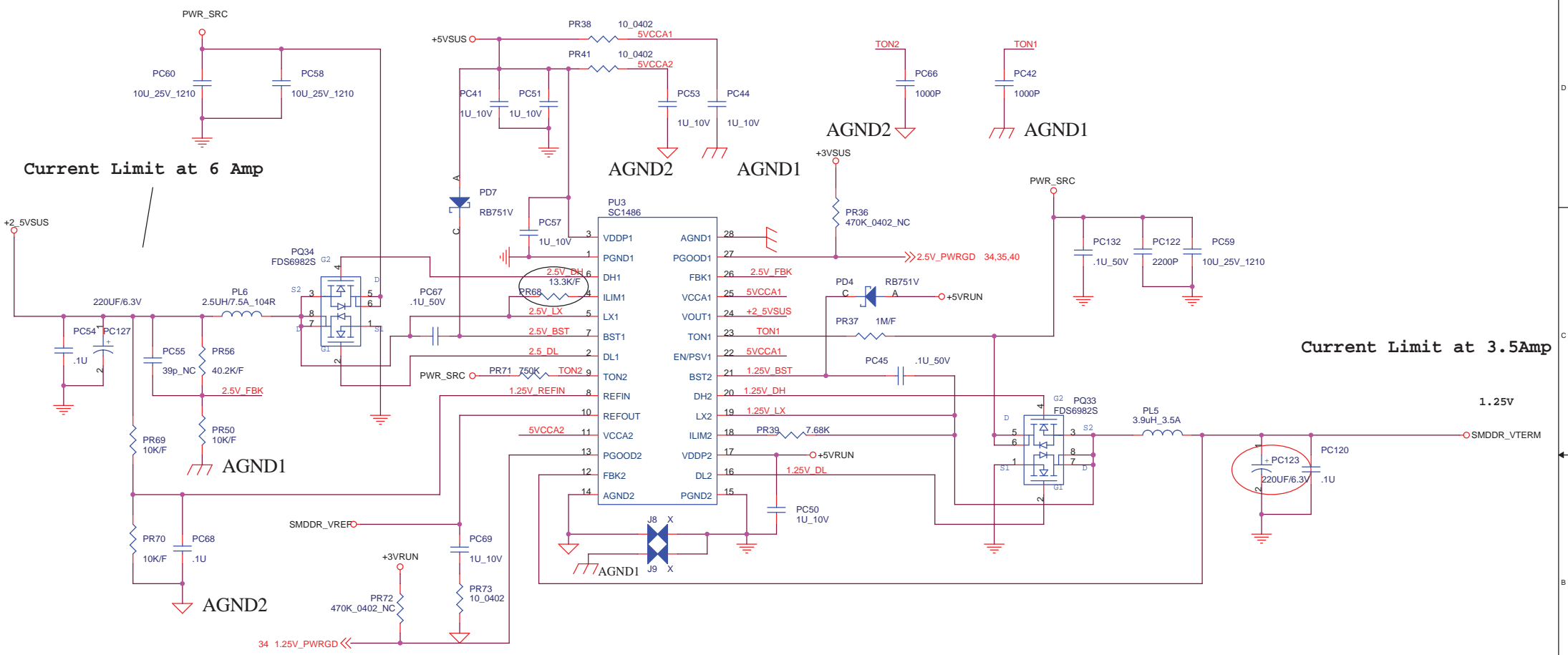
Keep Away from high speed buses



MSI CORPORATION		
Title POWER GOOD		
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MSI CORPORATION		
Title		
+1.5V & +1.8V		
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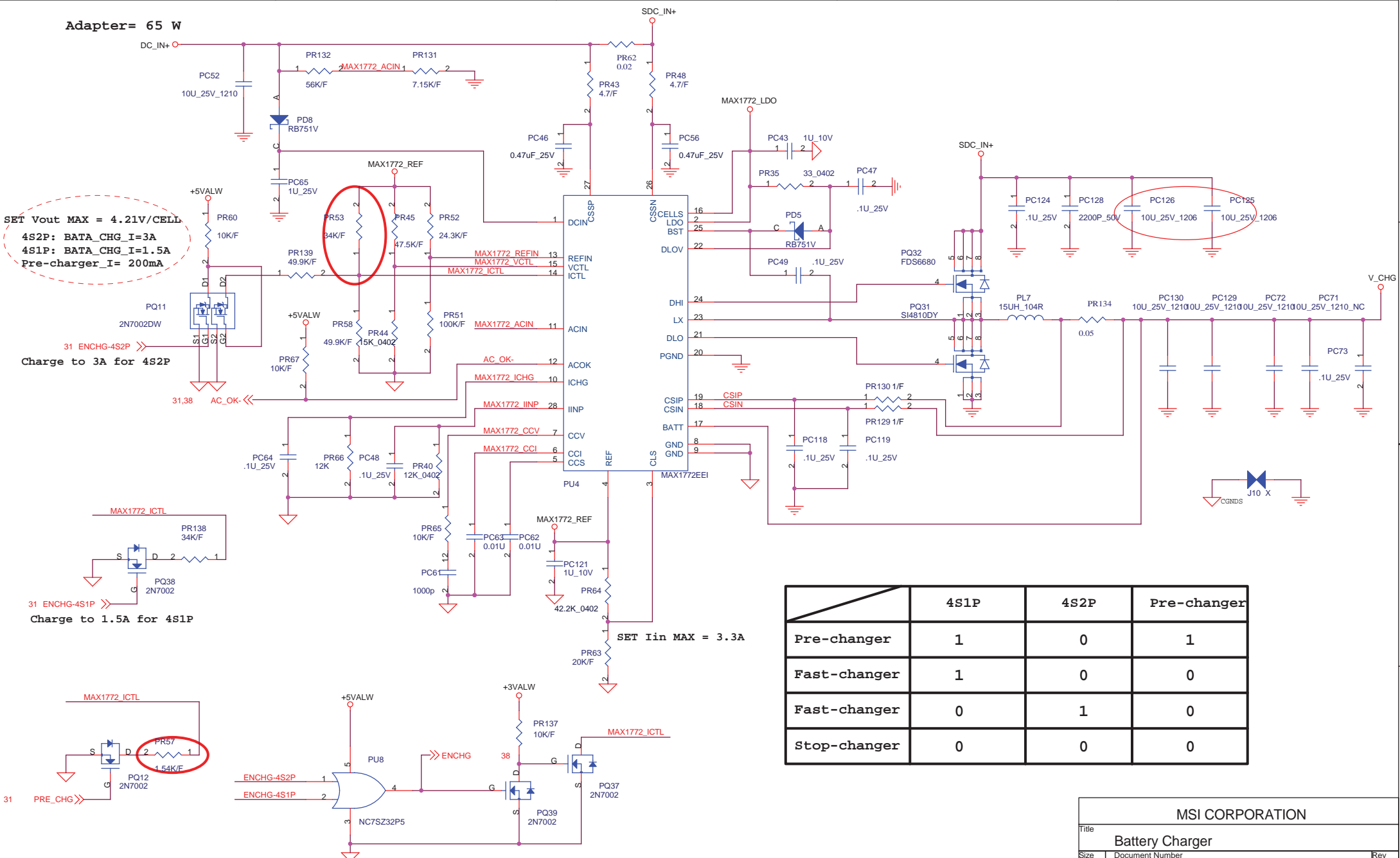


Current Limit at 6 Amp

Current Limit at 3.5Amp

MSI CORPORATION		
Title: +2.5V +1.25V		
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Adapter= 65 W



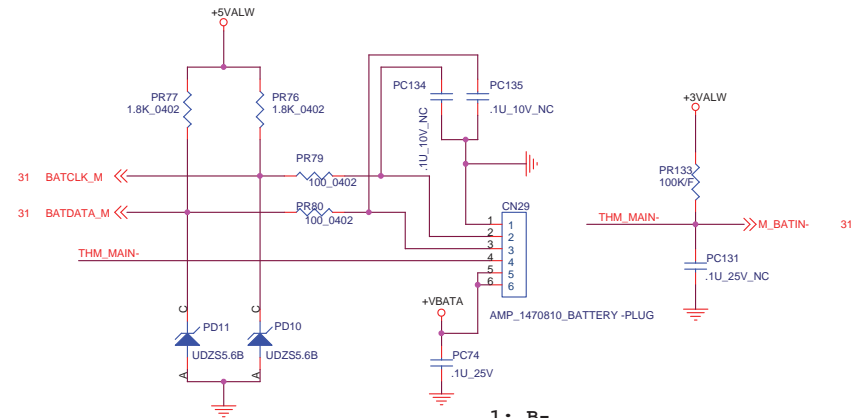
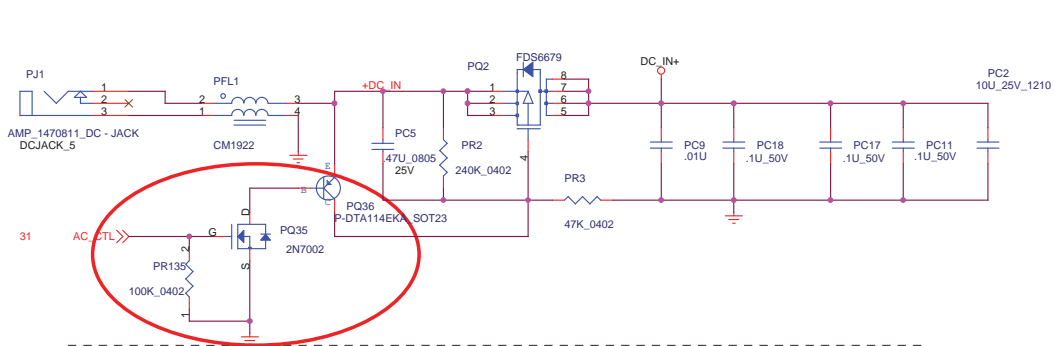
	4S1P	4S2P	Pre-charger
Pre-charger	1	0	1
Fast-charger	1	0	0
Fast-charger	0	1	0
Stop-charger	0	0	0

MSI CORPORATION

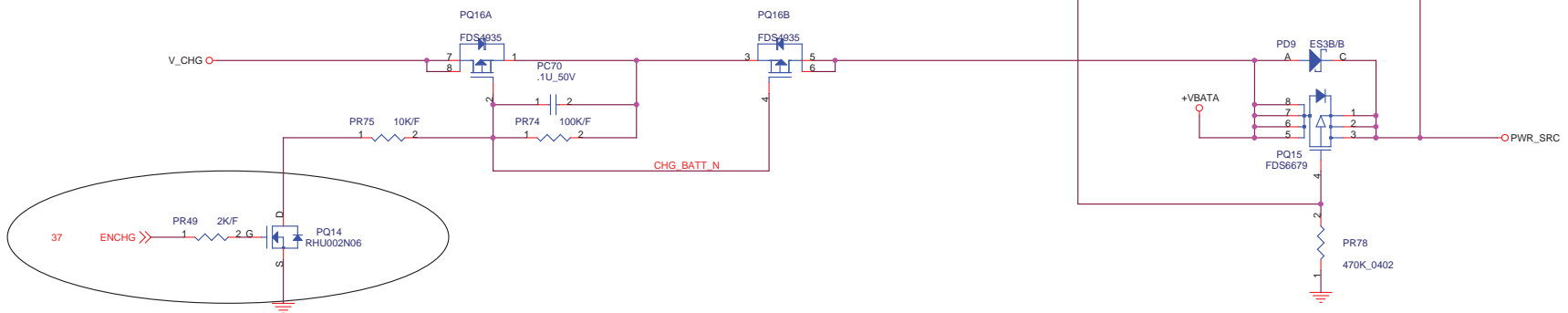
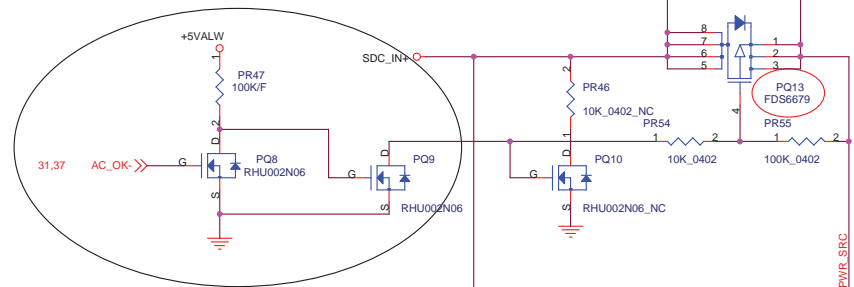
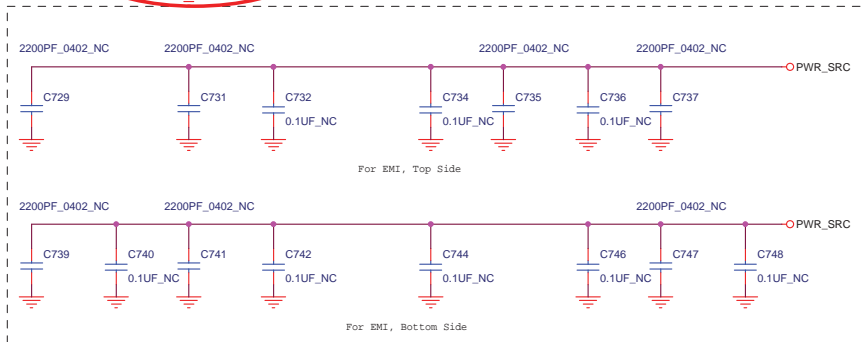
Title: **Battery Charger**

Size: Document Number
 Custom: **MS-1003** Rev: 0.C

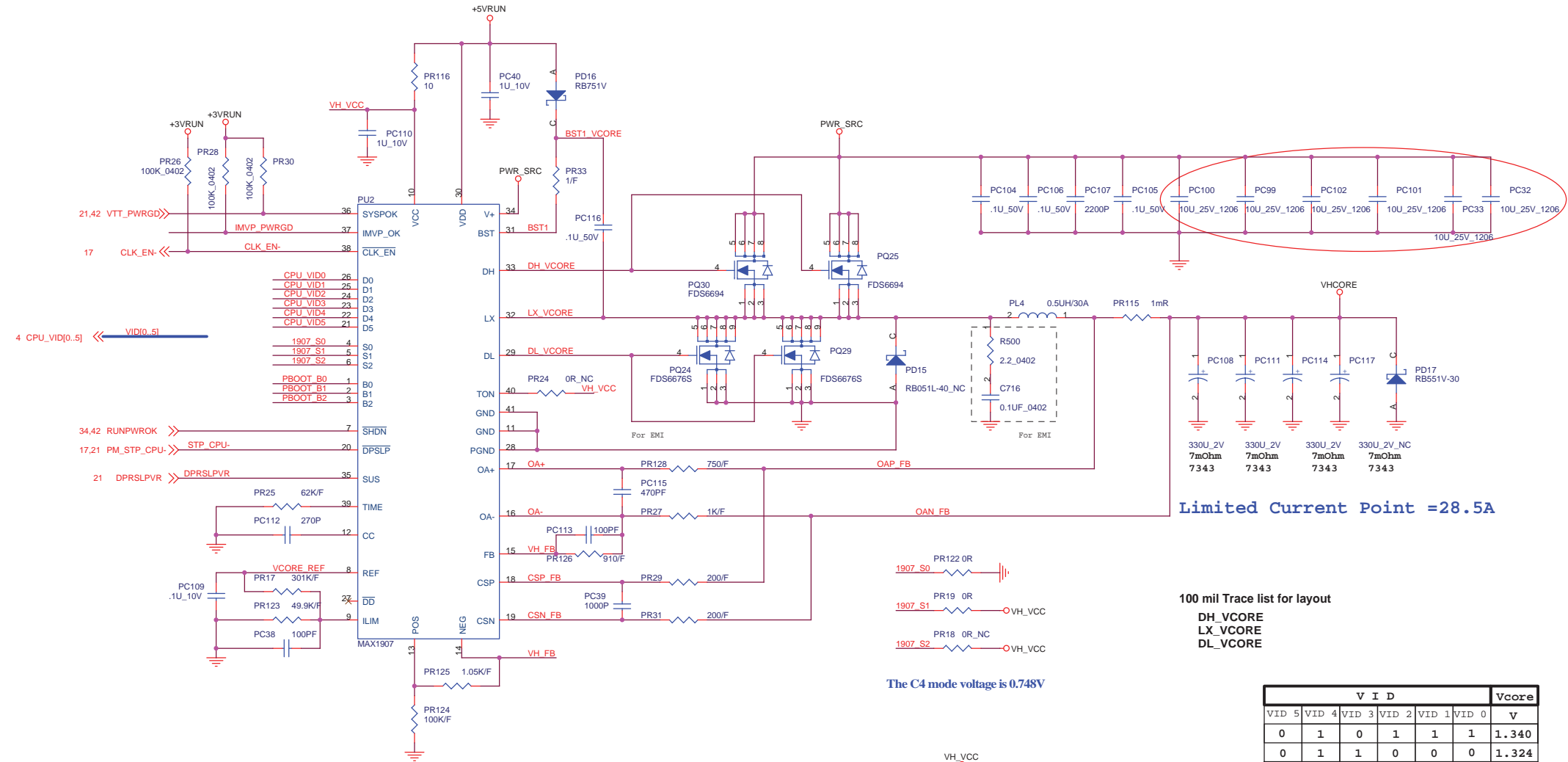
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- 1: B-
- 2: SMCLK
- 3: SMDATA
- 4: BT Thermal
- 5: VBATA
- 6: VBATA



MSI CORPORATION		
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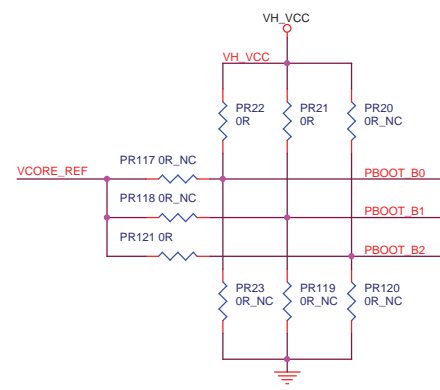
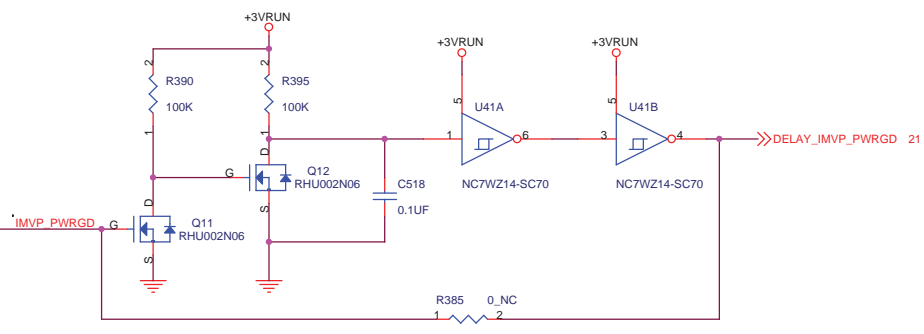


Limited Current Point = 28.5A

100 mil Trace list for layout

- DH_VCORE
- LX_VCORE
- DL_VCORE

The C4 mode voltage is 0.748V

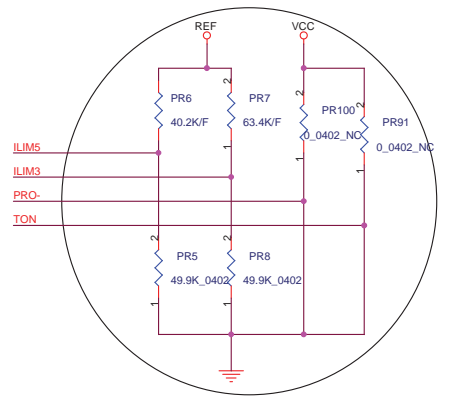
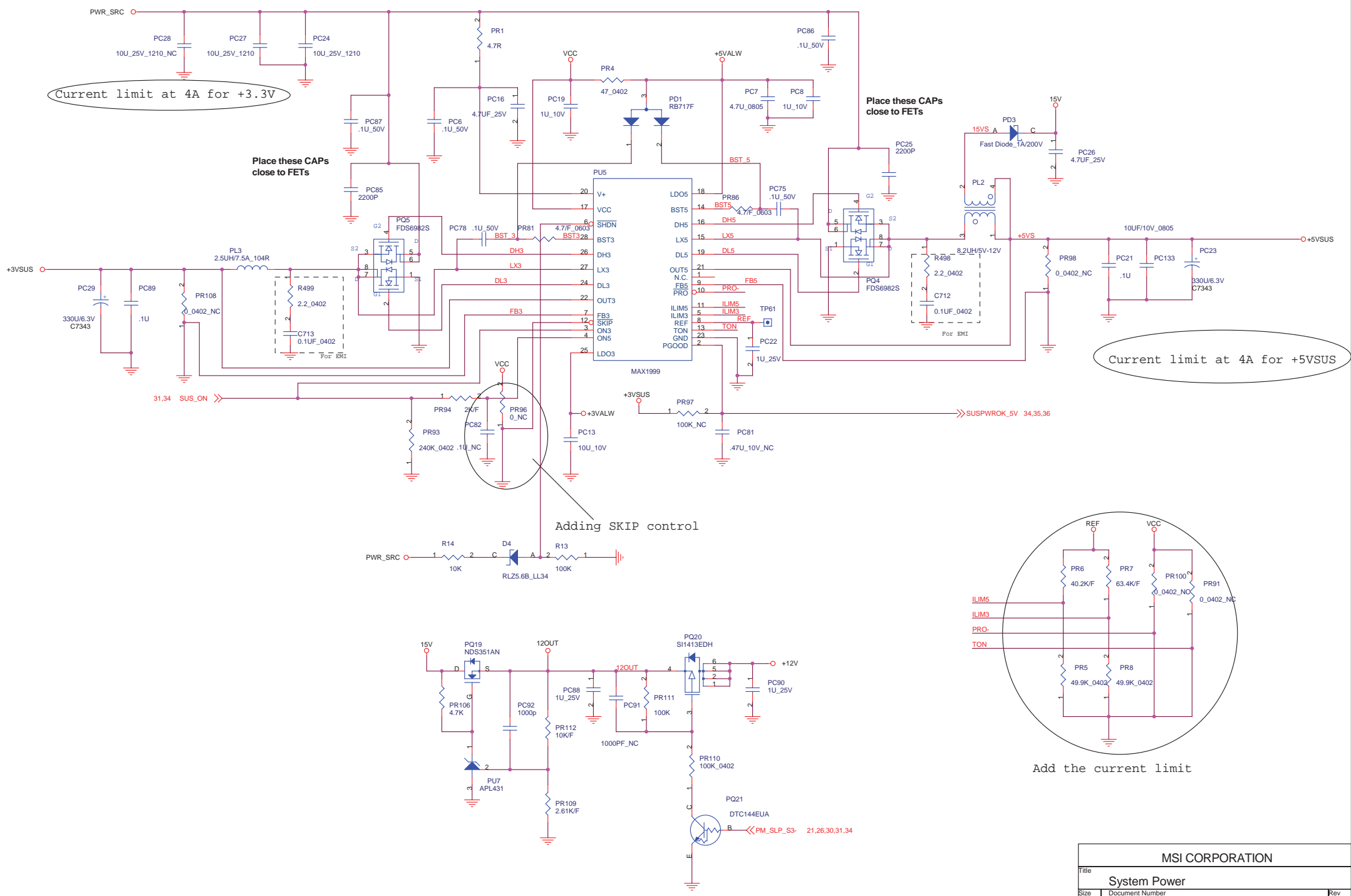


PBOOT VOLTAGE SETTING UP ON 1.212V

V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0		v
0	1	0	1	1	1		1.340
0	1	1	0	0	0		1.324
0	1	1	0	1	0		1.292
0	1	1	1	0	0		1.260
0	1	1	1	0	1		1.244
0	1	1	1	1	1		1.212
1	0	0	0	0	1		1.180
1	0	0	0	1	1		1.148
1	0	0	1	1	0		1.100
1	0	1	0	0	1		1.052
1	0	1	0	1	1		1.020
1	0	1	1	1	0		0.972
1	1	0	0	0	0		0.940

MSI CORPORATION

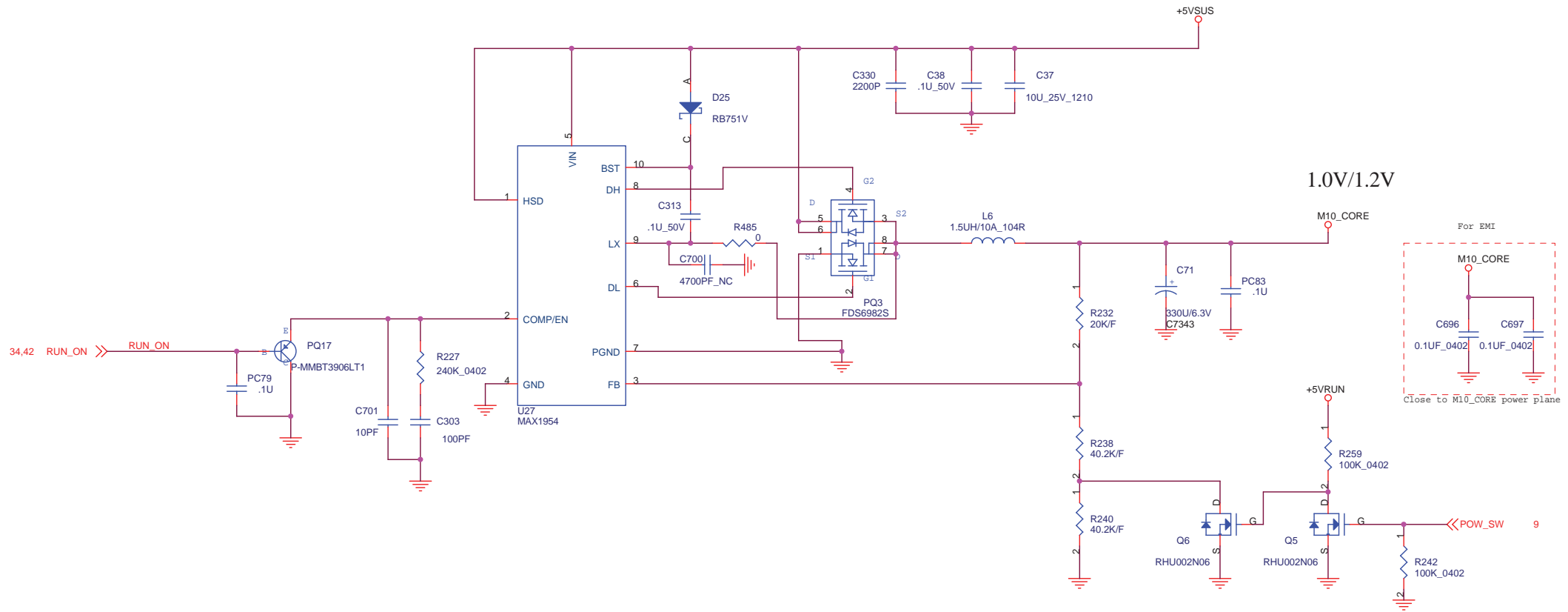
File		CPU Power	
Size	Document Number	Rev	
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Add the current limit

MSI CORPORATION		
Title: System Power		
Size: Custom	Document Number: MS-1003	Rev: 0.C
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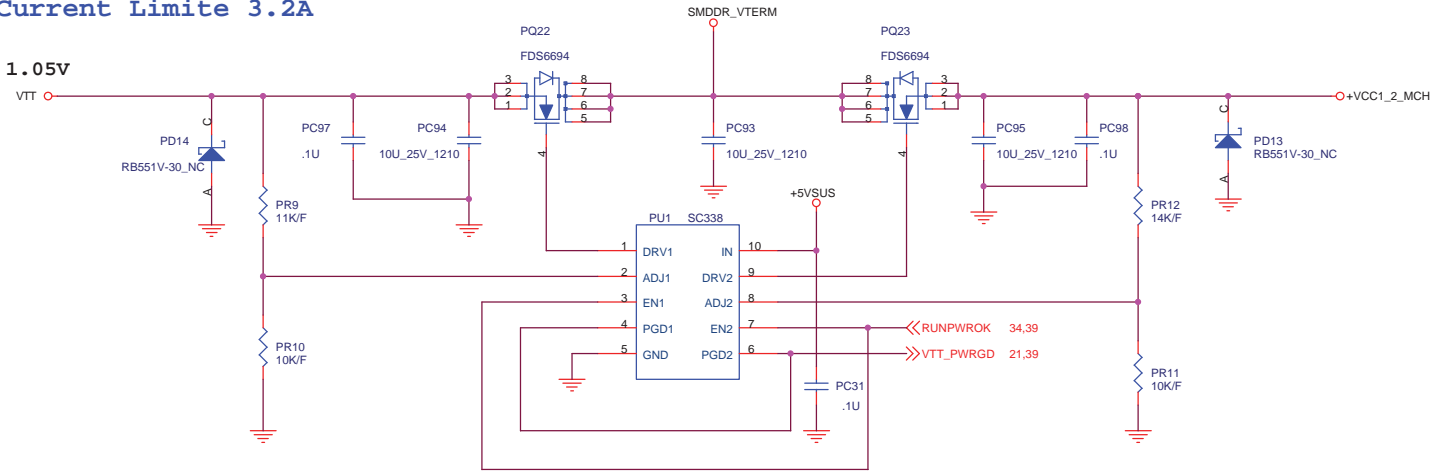
POW_SW	ATI M10
1	1.0V
0	1.2V



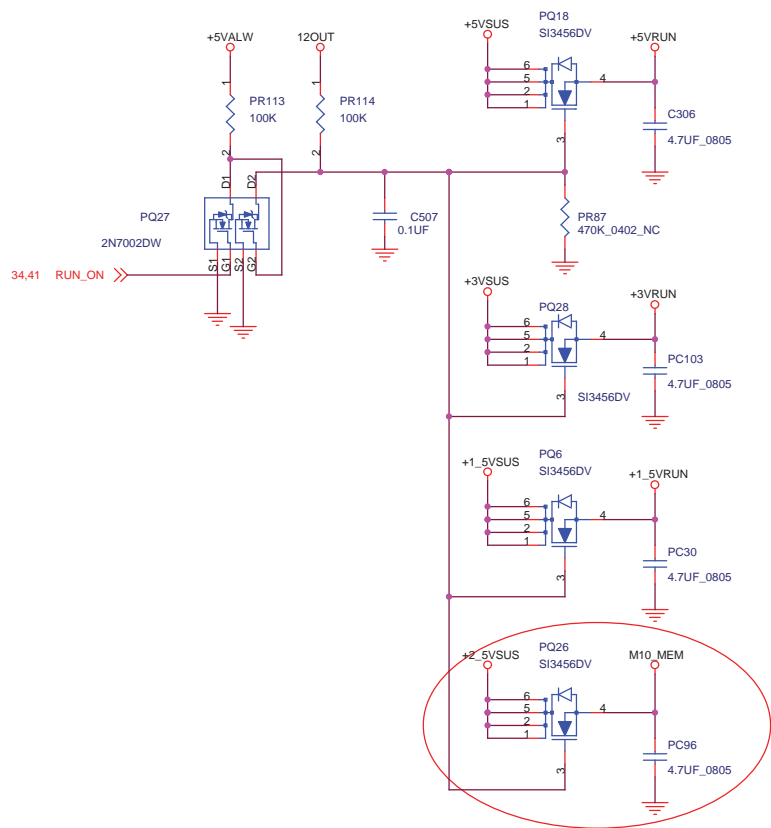
MSI CORPORATION		
Title	VGA POWER	
Size	Document Number	Rev
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VTT Current Limite 3.2A

1.05V



1.20V - GM, PR145=14.0K/F
 1.35V - GM+ PR145=16.9K/F
 +VCC1_35_GMCH Current Limite 3.2A



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Title VTT, MCH		
Size Custom	Document Number MS-1003	Rev 0.C
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0.C : (1) For audio issue:

R310,R311,R312 change to 0 ohm; R291,R292,R293 changed to NC;
C386 changed to 220uF; R278,R352 change to 12K ohm;
Add C705 parallel connection with C396(both 47uF);
Add C706 parallel connection with C432(both 47uF);
+ADD turn from +5VSUS instead of +5VRUN;
Add R495(0,NC) and C707(0.1u) on PCMSPK signal;
Fixed AOUTL and AOUTR signals;

(2) For HDD UDMA-5 mode detecting issue:

R472 changed to NC; Add R491(10k), pull-up(+3VRUN);

(3) For battery LED color issue:

The signals LED_BATT_FAIL# and LED_BAT0# had exchanged(layout & LED board need not modify);

(4) For Suspend LED always on at S3-S5 issue:

Use LED_S3# signal(form ICH4 GPIO) instead of PM_SLP_S3# to control Suspend LED;

(5) Change AC_OK LED signal to WLAN_PWRON# signal;

(6) CN21(debug port) and CN30(touch oanel) had deleted;

(7) Implement KBC ENCHG_4S1P, ENCHG_4S2P, and AC_CTL function;

MSI CORPORATION			
Title			
HISTORY			
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