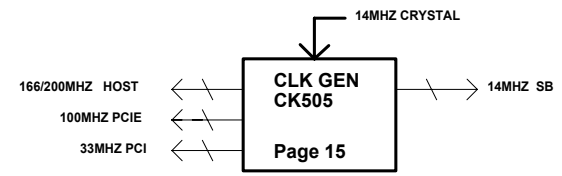
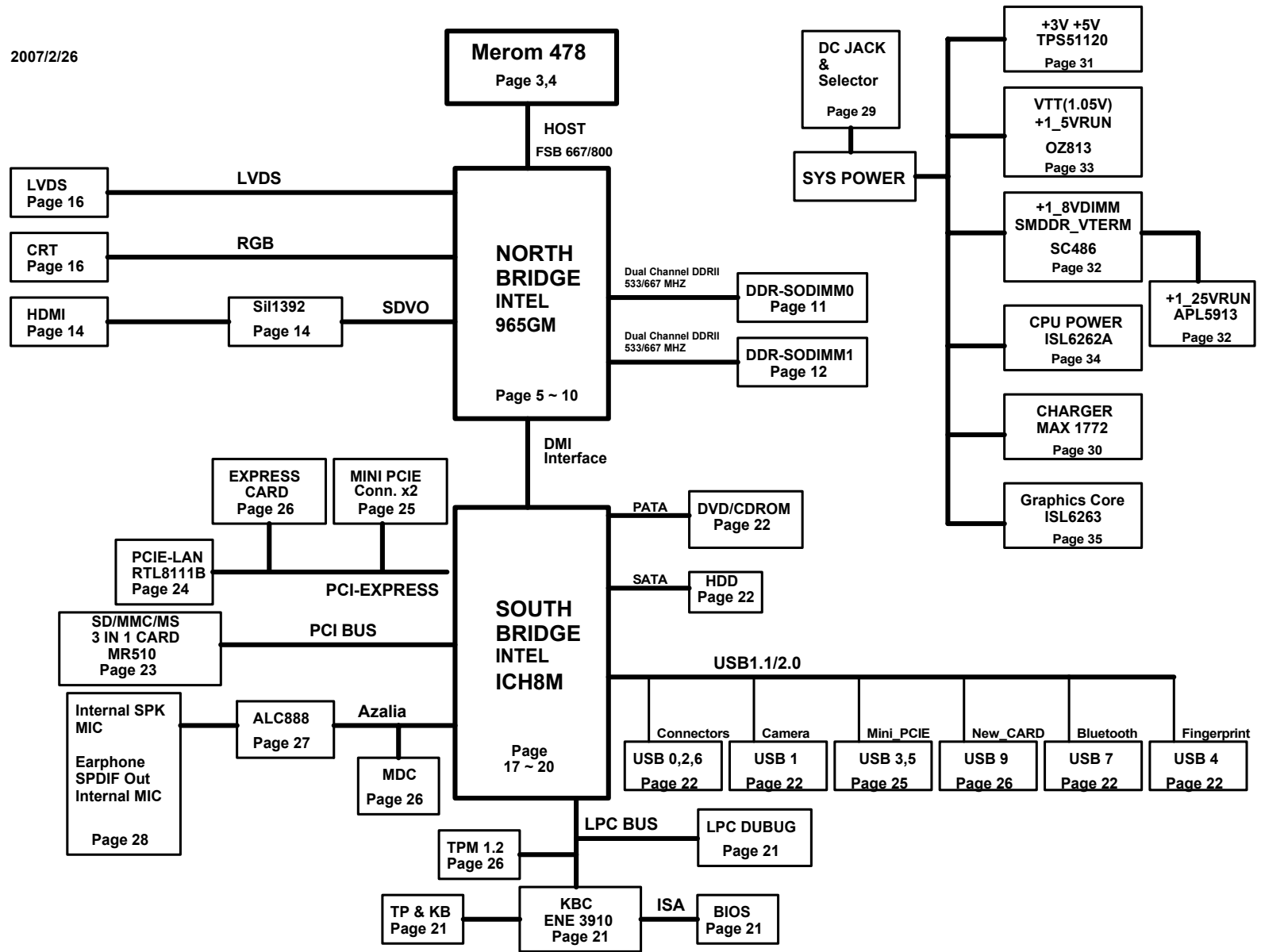


- 01 : BLOCK DIAGRAM
- 02 : PLATFORM
- 03 : Merom-1 CPU (HOST BUS)
- 04 : Merom-2 CPU (POWER/GND)
- 05 : 965GM-1 (HOST)
- 06 : 965GM-2 (DMI / VGA)
- 07 : 965GM-3 (DDR2)
- 08 : 965GM-4 (Power-1)
- 09 : 965GM-5 (Power-2)
- 10 : 965GM-6 (GND)
- 11 : DDR2_SODIMM0
- 12 : DDR2_SODIMM1
- 13 : DDR2_Termination
- 14 : SDVO- SiI1392
- 15 : CLOCK GEN (CK505)
- 16 : VGA, LVDS ,BL
- 17 : ICH8M-1 (CPU/IDE/Azalia)
- 18 : ICH8M-2 (PCI/USB/PCIE/DMI)
- 19 : ICH8M-3 (SM BUS/GPIO)
- 20 : ICH8M-4 (POWER/GND)
- 21 : ENE3910(KBC) & BIOS
- 22 : HDD,CDROM,CIR,USB CONN.
- 23 : Card Reader (MR510)
- 24 : PCIE LAN (RTL 8111B)
- 25 : MINI_PCIE, LED, SW
- 26 : NEWCARD, MDC, TPM, FAN
- 27 : AZALIA CODEC(ALC888)
- 28 : Audio Amp. & Jacks
- 29 : M_Battery Select
- 30 : M_Battery Charger
- 31 : M_System Power
- 32 : DDR2 RAM POWER, +1.25V
- 33 : M_VTT, +1.5V
- 34 : M_CPU power
- 35 : M_Graphics Core
- 36 : Screw / EMI
- 37 : Non-Footprint for BOM
- 38 : KBC_CTR_PWR_BD
- 39 : Power Sequency
- 40 : Change History



Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VH CORE	Core Voltage for Processor	VR_ON
VTT	1.05 rail for Processor & 965GM I/O	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+2_5VRUN	2.5V powe rail for CH7315A (off in S3-S5)	+3VRUN
+3VRUN	3.3V switched power rail (off in S3-S5)	RUN_ON
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
SMD DR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	DIMM_ON
+1_8VDIMM	1.8V power rail DDR (off in S4-S5)	DIMM_ON
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
ADD5V	5.0V Power rail Audio codec(off in S3-S5)	+5VRUN
+1_25VRUN	1.25V LDO power rail (off in S3-S5)	RUN_ON
+V GFX_CORE	Graphic core of GMCH switched power rail (off in S3-S5)	GFX_VR_EN

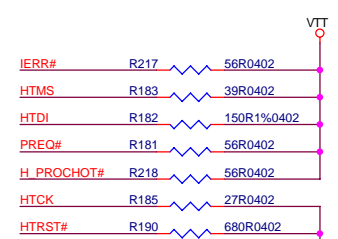
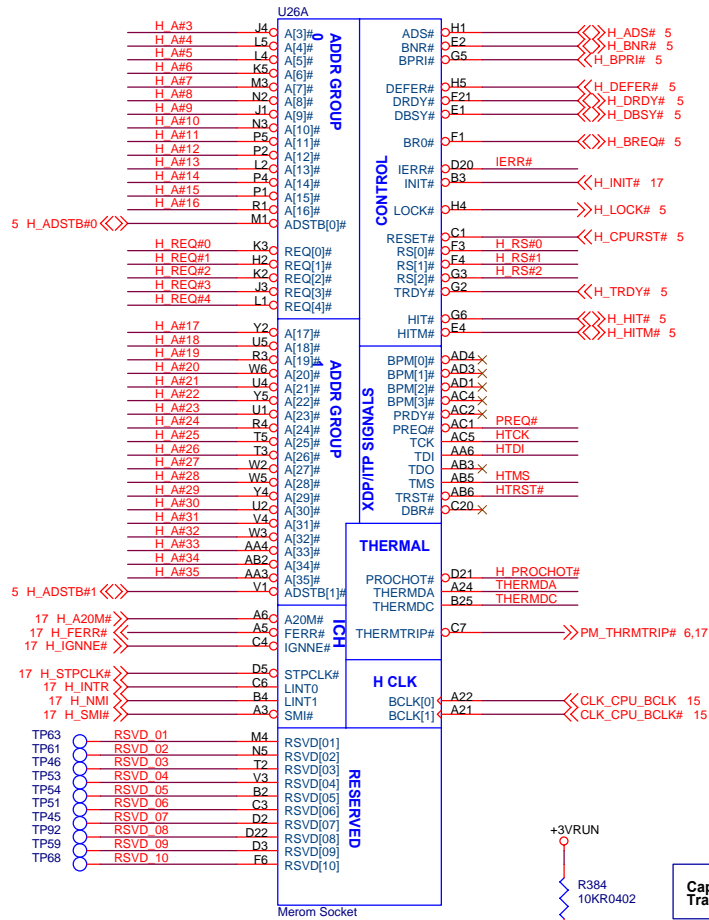
POWER STATES

SIGNAL STATE	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1M(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

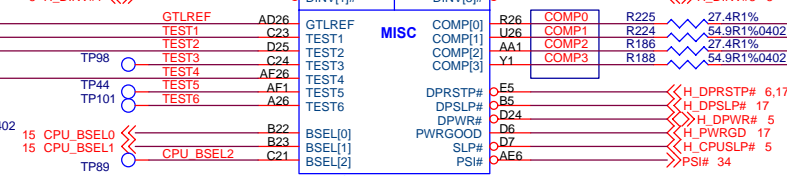
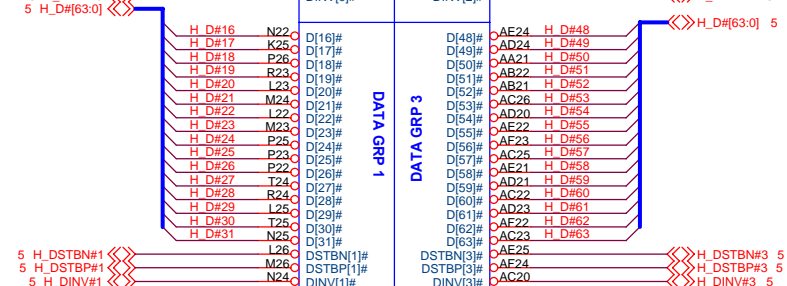
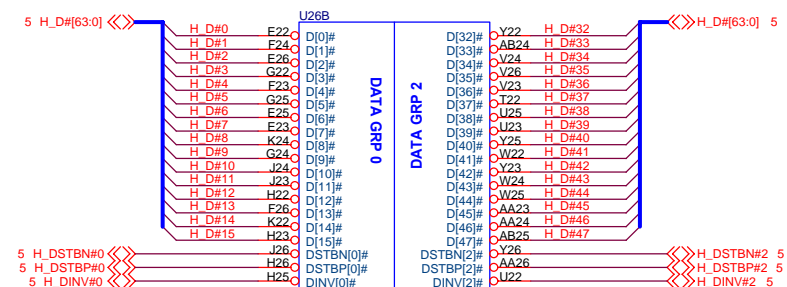
Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

MSI CORPORATION		
Title		
PLATFORM		
Size	Document Number	Rev
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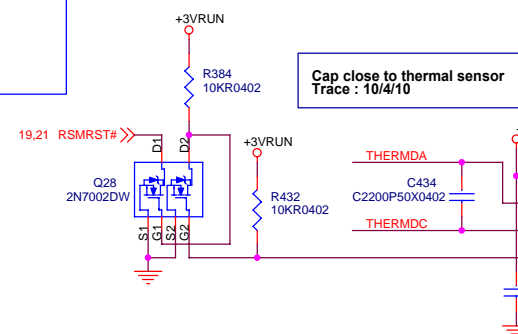
5 H_A#[35:3] <<> H_A#[35:3]
 5 H_RS#[2:0] <<> H_RS#[2:0]
 5 H_REQ#[4:0] <<> H_REQ#[4:0]



Within 0.5"

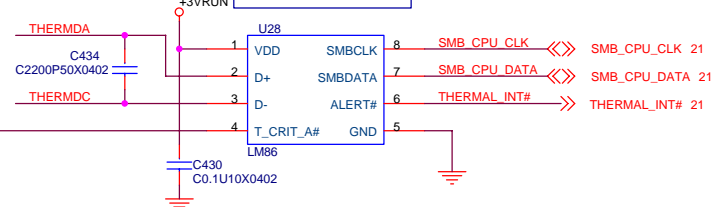


Within 0.5"
 25mils Spacing
 COMP0,2 -> 18mils
 COMP1,3 -> 5mils

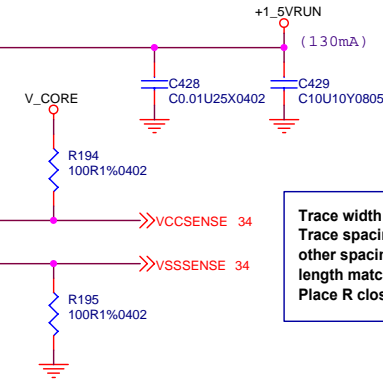
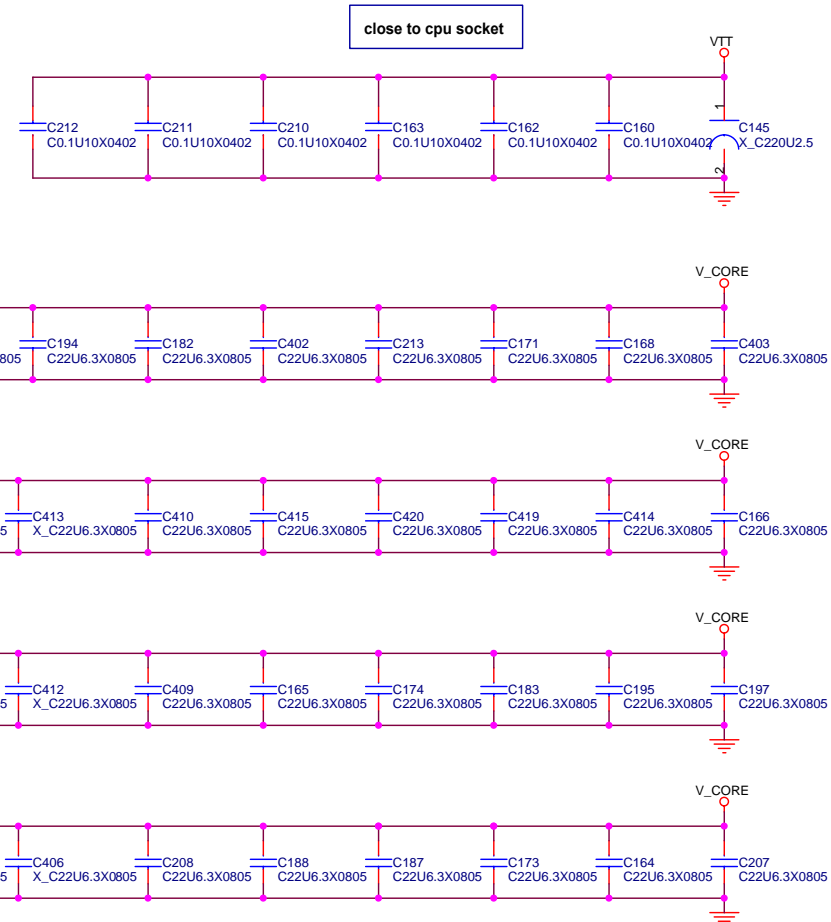
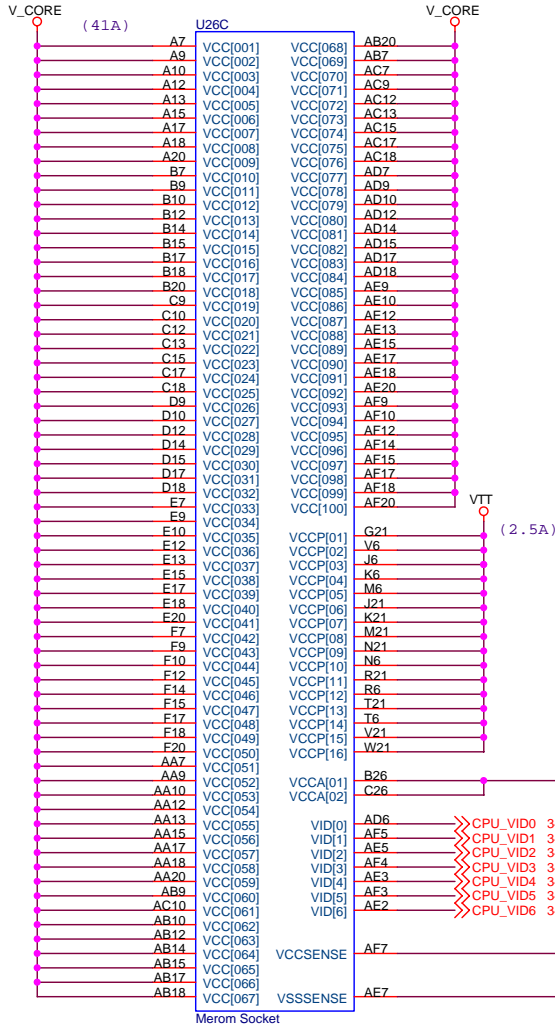
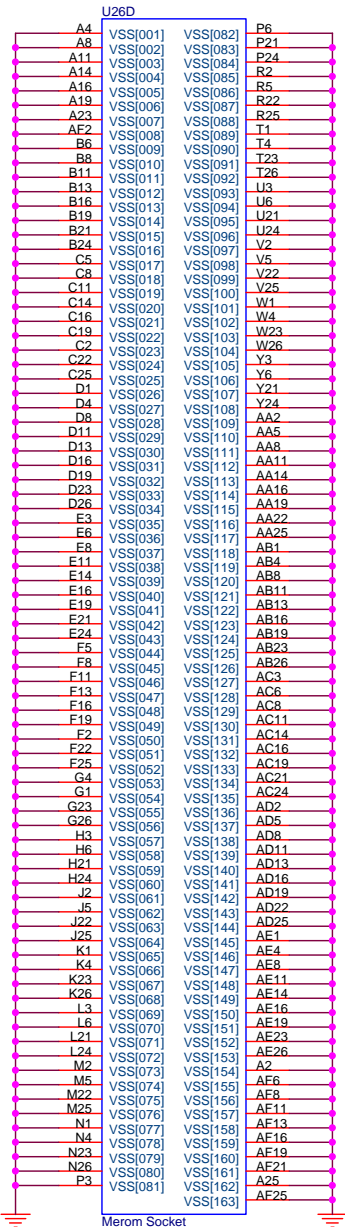


Cap close to thermal sensor
 Trace : 10/4/10

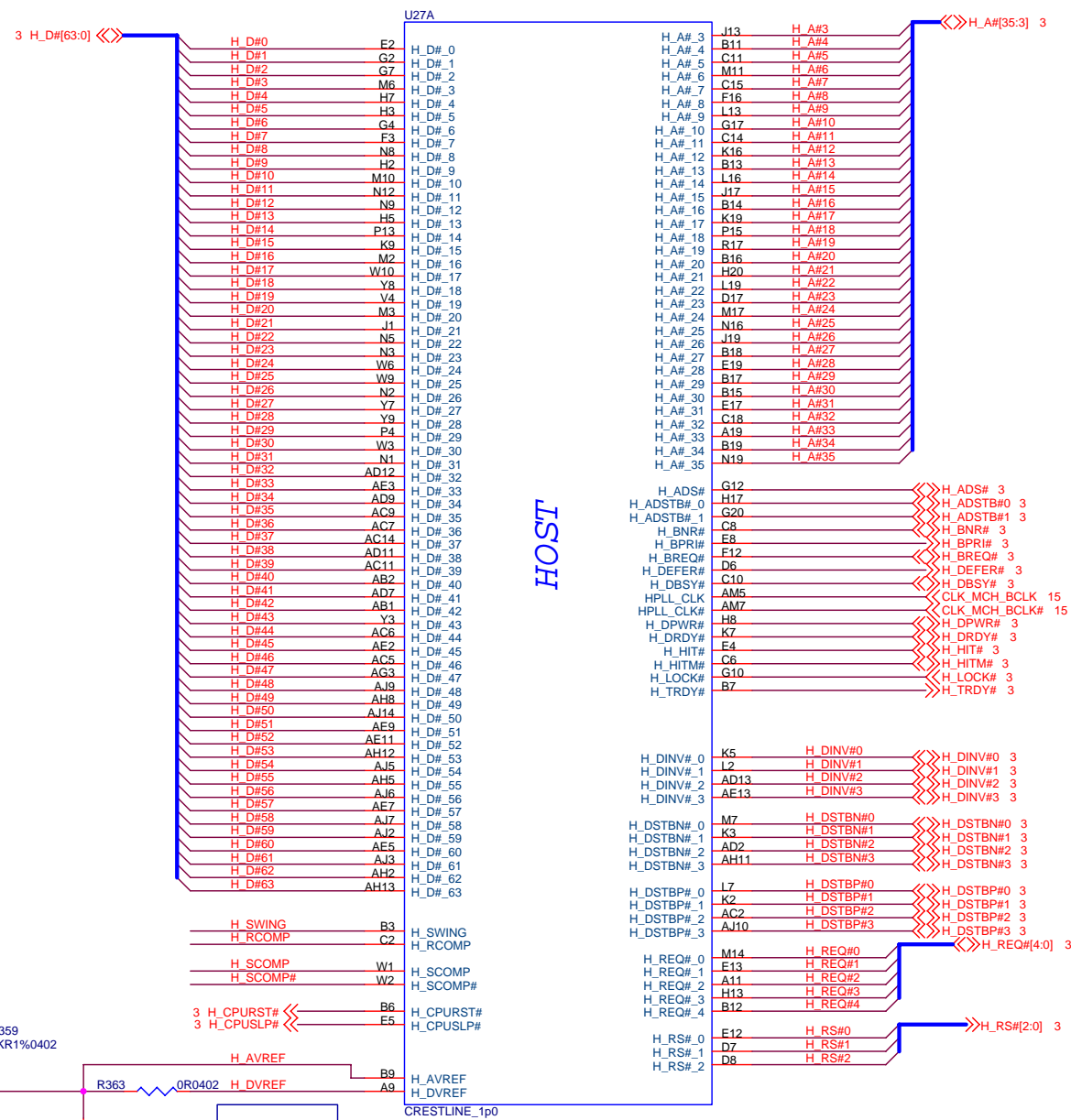
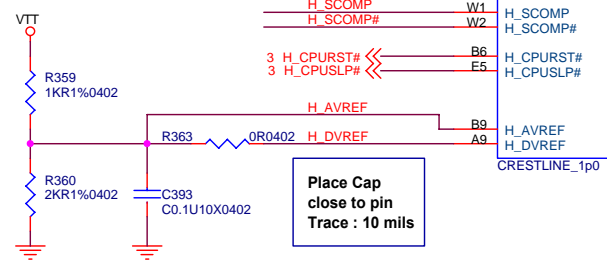
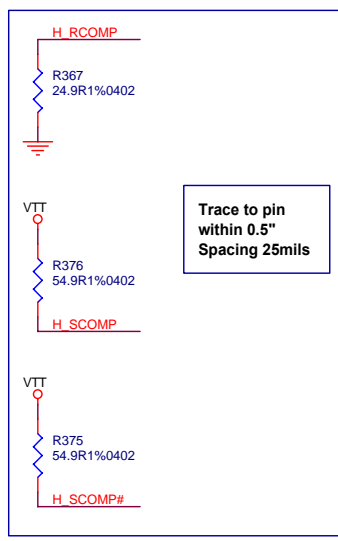
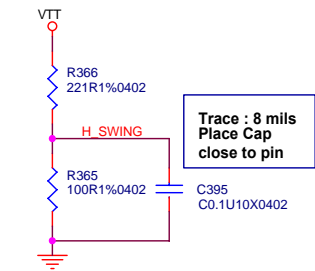
Close to CPU socket



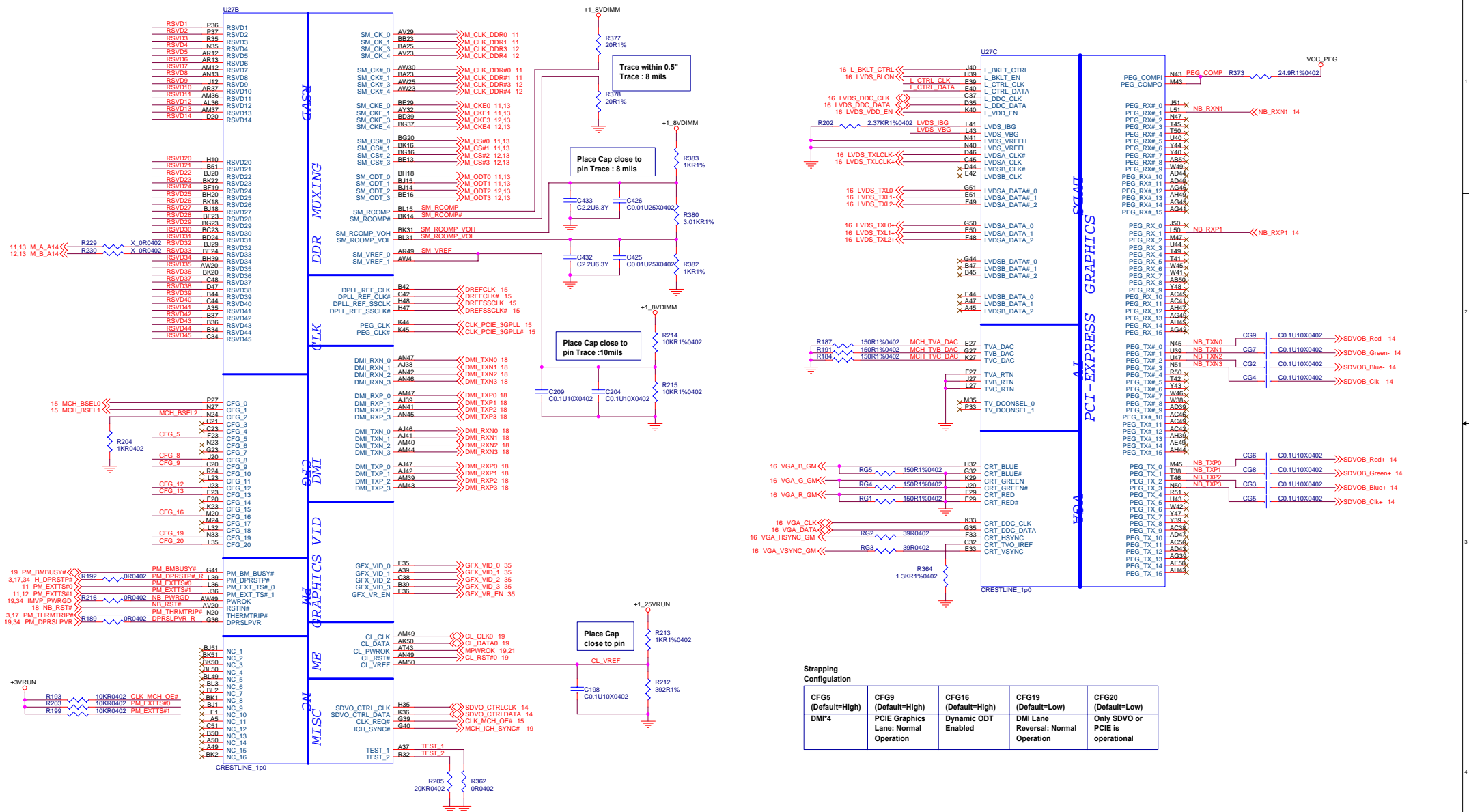
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Title Merom-1 (HOST BUS)			
Size	Document Number	Rev	
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MSI CORPORATION		
Title: Merom-2 (POWER/GND)		
Size: Custom	Document Number: MS-1221	Rev: 1.0
Date: Tuesday, March 13, 2007	Sheet: 4	of 41



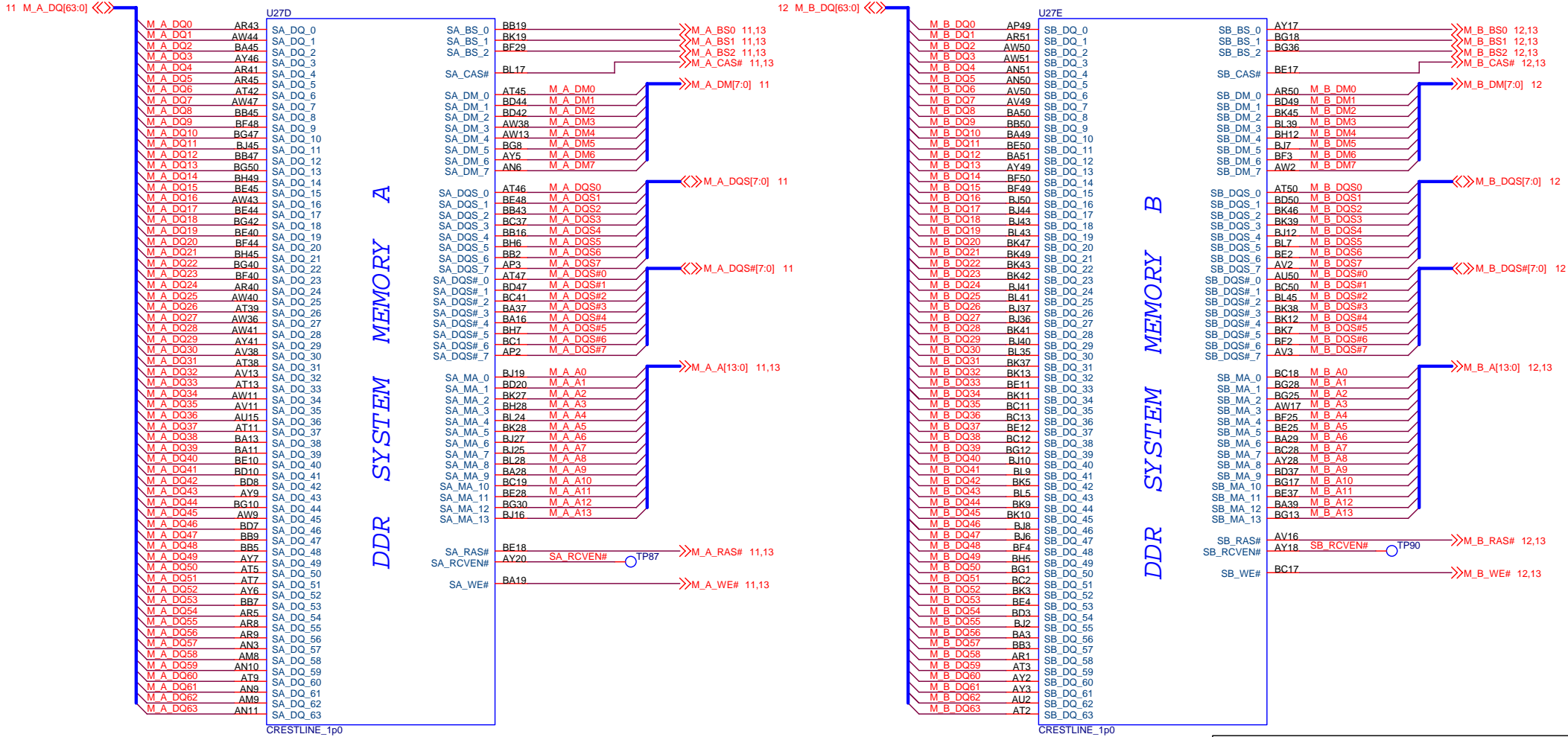
MSI CORPORATION		
CRESTLINE-1 (HOST BUS)		
Title		
Size	Document Number	Rev
B	MS-1221	1.0
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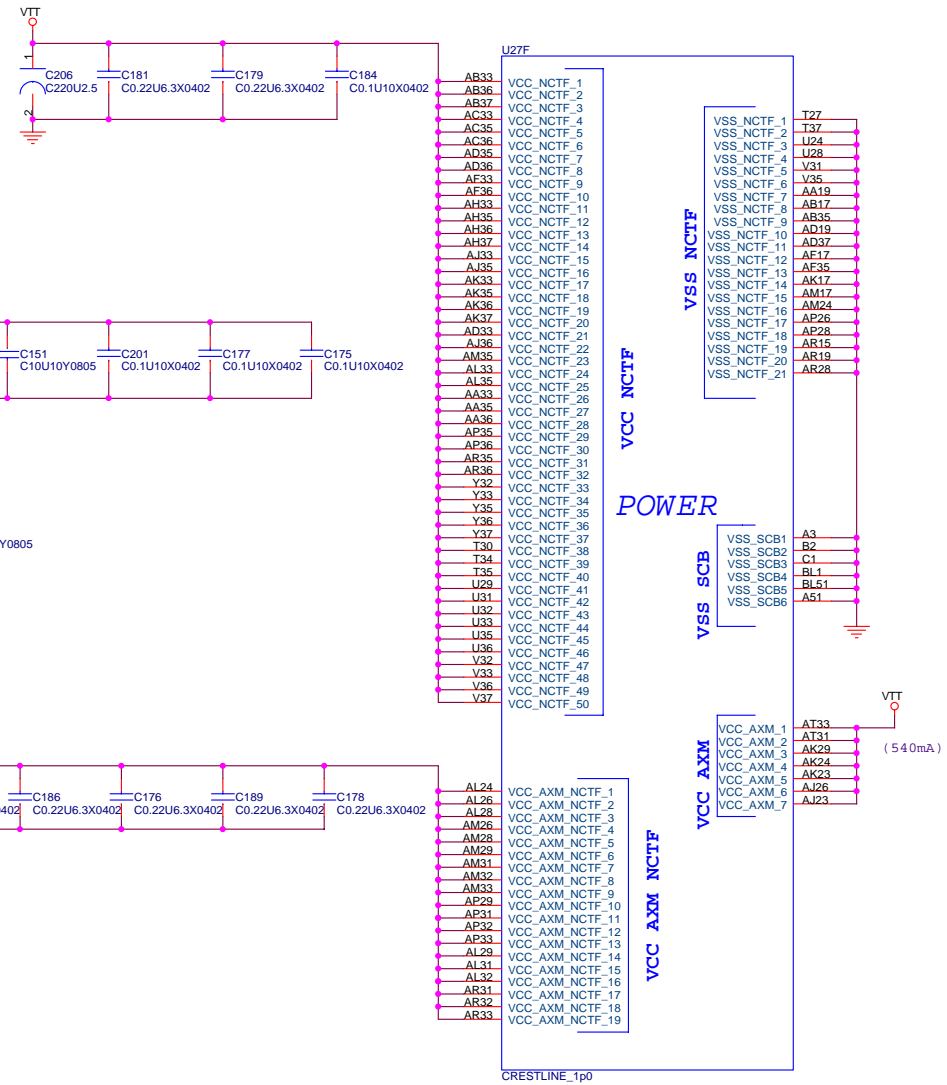
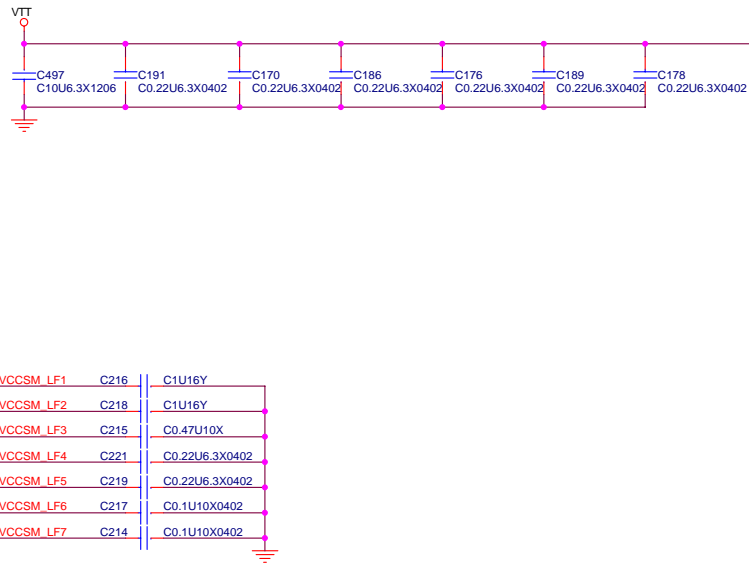
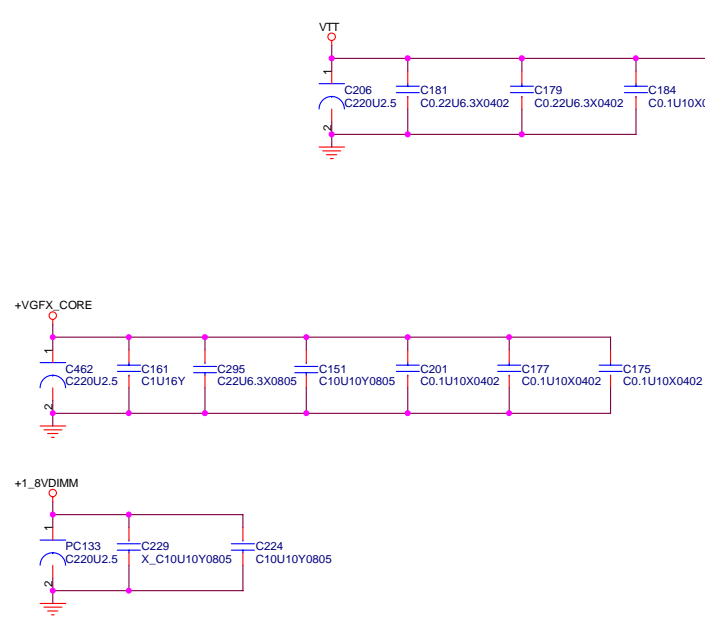
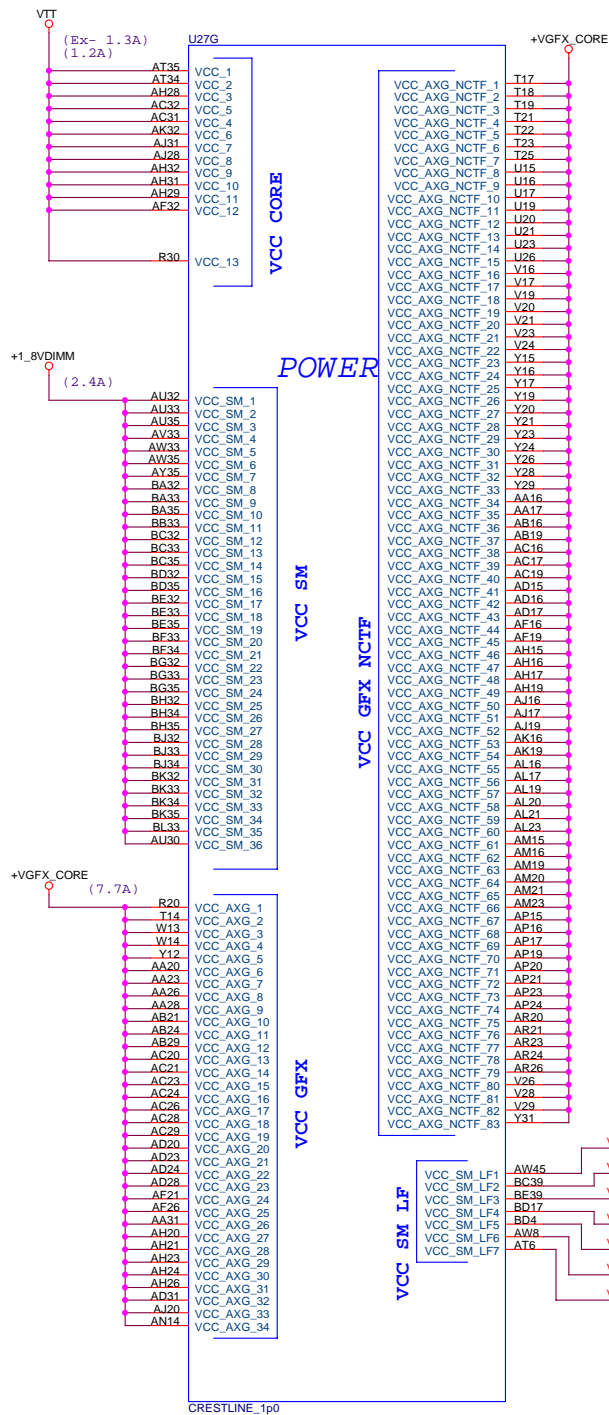
Strapping Configuration

CFG5 (Default=High)	CFG9 (Default=High)	CFG16 (Default=High)	CFG19 (Default=Low)	CFG20 (Default=Low)
DMI*4	PCIe Graphics Lane: Normal Operation	Dynamic ODT Enabled	DMI Lane Reverse: Normal Operation	Only SDVO or PCIe is operational

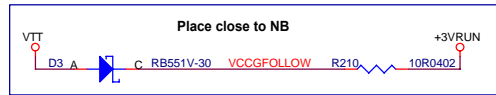
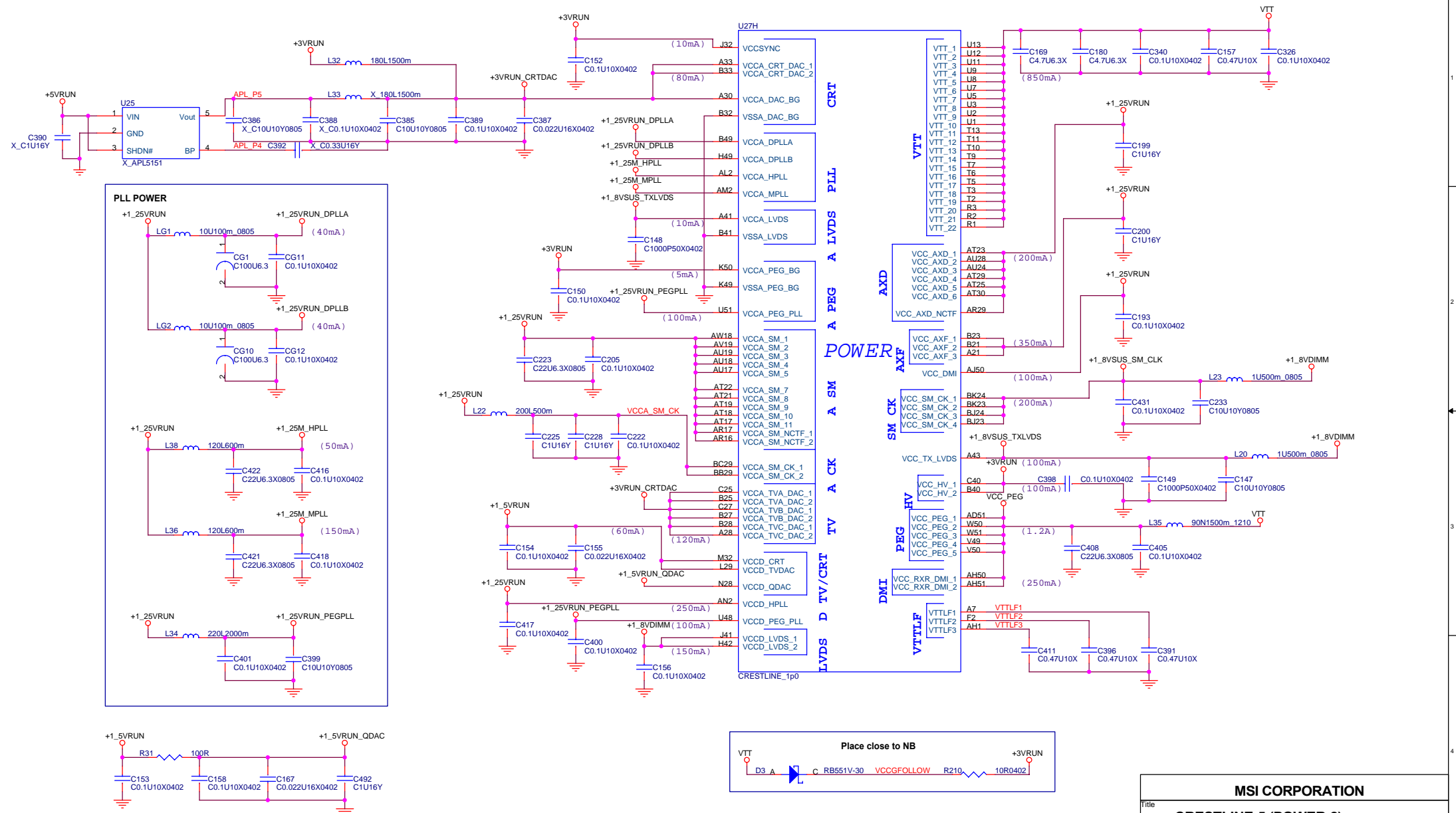
MSI CORPORATION	
Title: CRESTLINE-2 (DMI/VGA)	
Size: Custom	Document Number: MS-1221
Date: Friday, March 16, 2007	Rev: 1.0
Sheet 6 of 41	



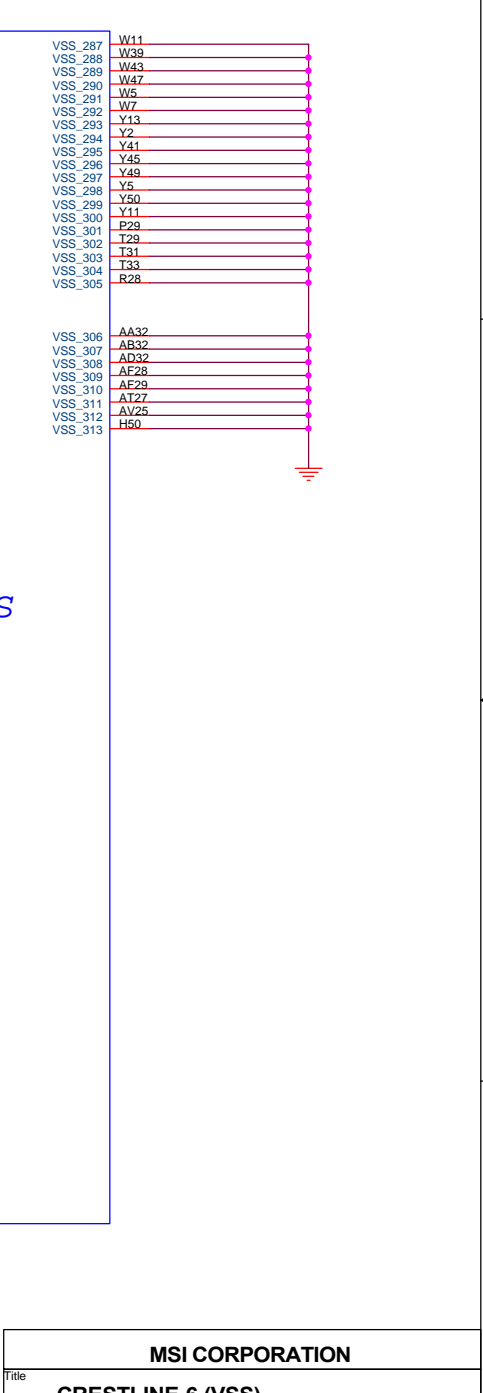
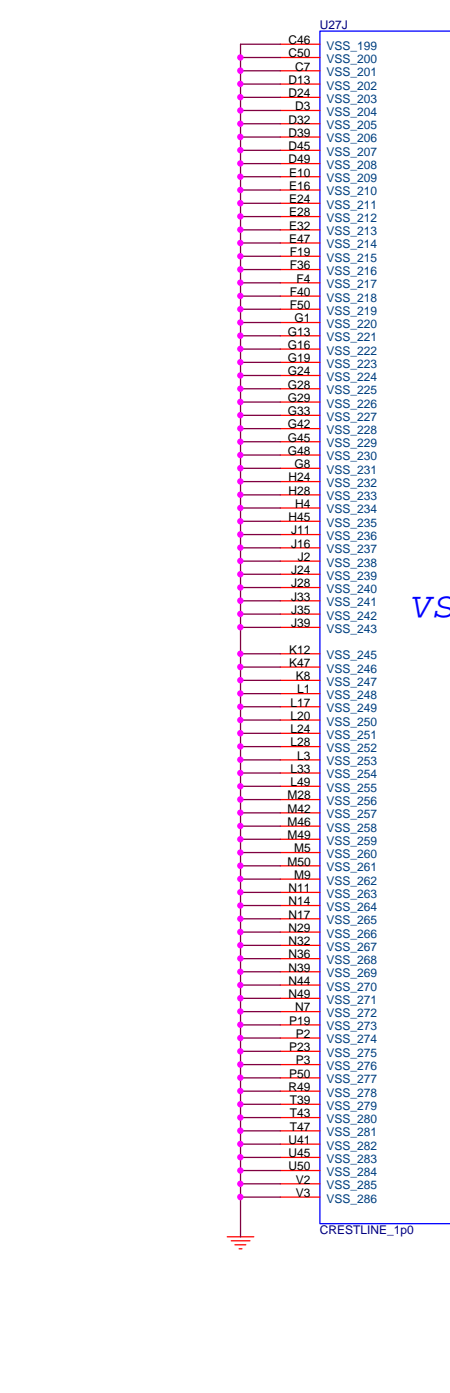
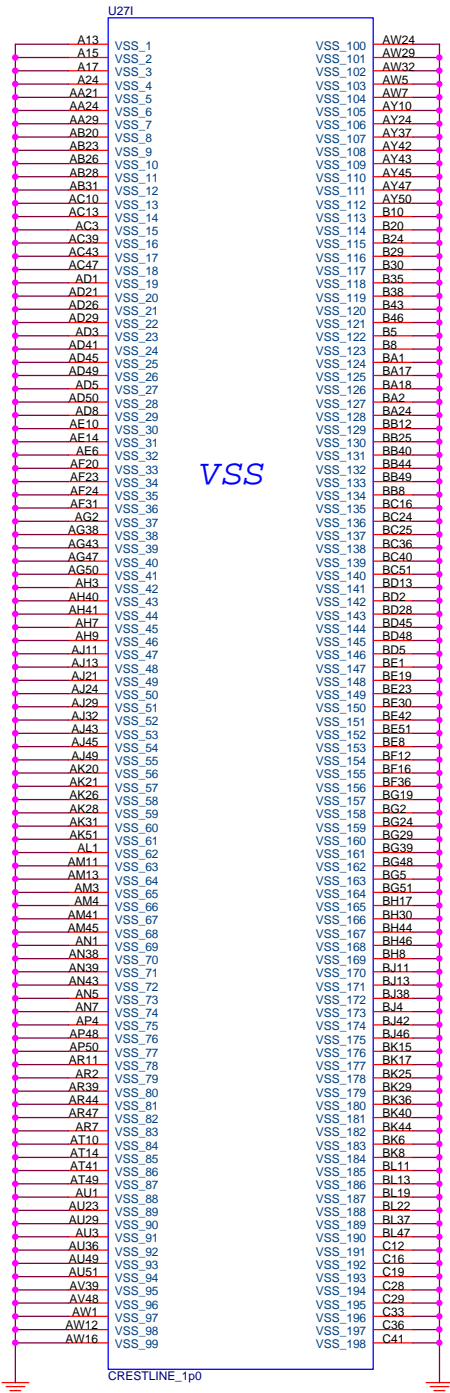
MSI CORPORATION			
Title			
CRESTLINE-3 (DDR)			
Size		Document Number	
Custom		MS-1221	
Date:	Friday, March 16, 2007	Sheet	7 of 41
		Rev 1.0	



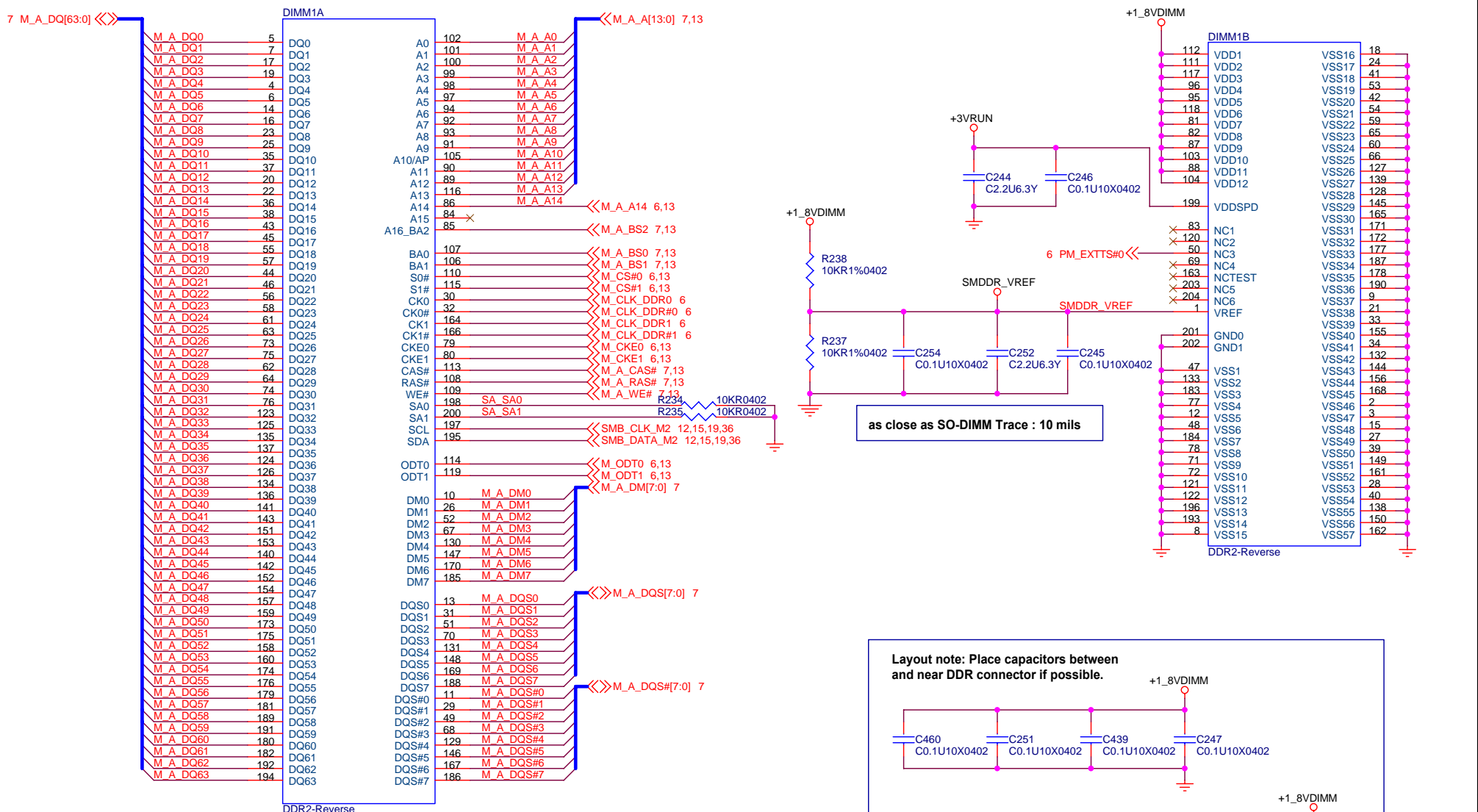
MSI CORPORATION			
Title			
CRESTLINE-4 (POWER-1)			
Size	Document Number	Rev	
Custom	MS-1221	1.0	
Date:	Friday, March 16, 2007	Sheet	8 of 41



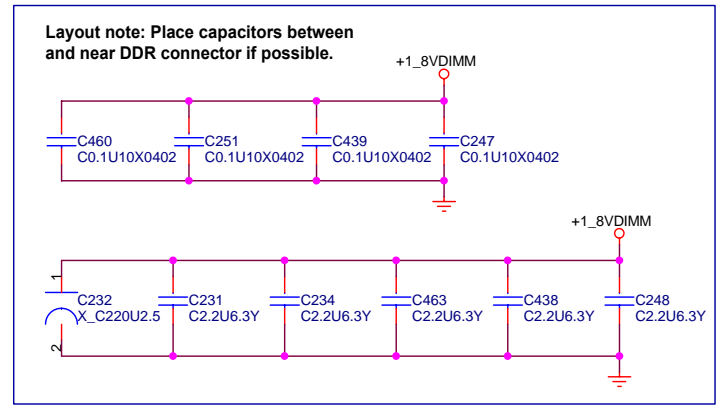
MSI CORPORATION		
Title		
CRESTLINE-5 (POWER-2)		
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Monday, March 19, 2007	Sheet 9 of 41



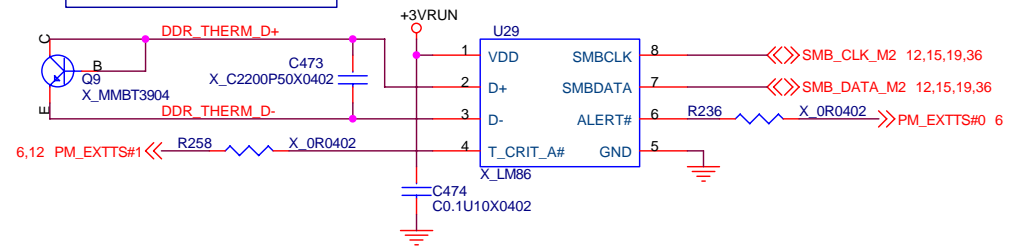
MSI CORPORATION		
Title		
CRESTLINE-6 (VSS)		
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Monday, March 26, 2007	Sheet 10 of 41



as close as SO-DIMM Trace : 10 mils

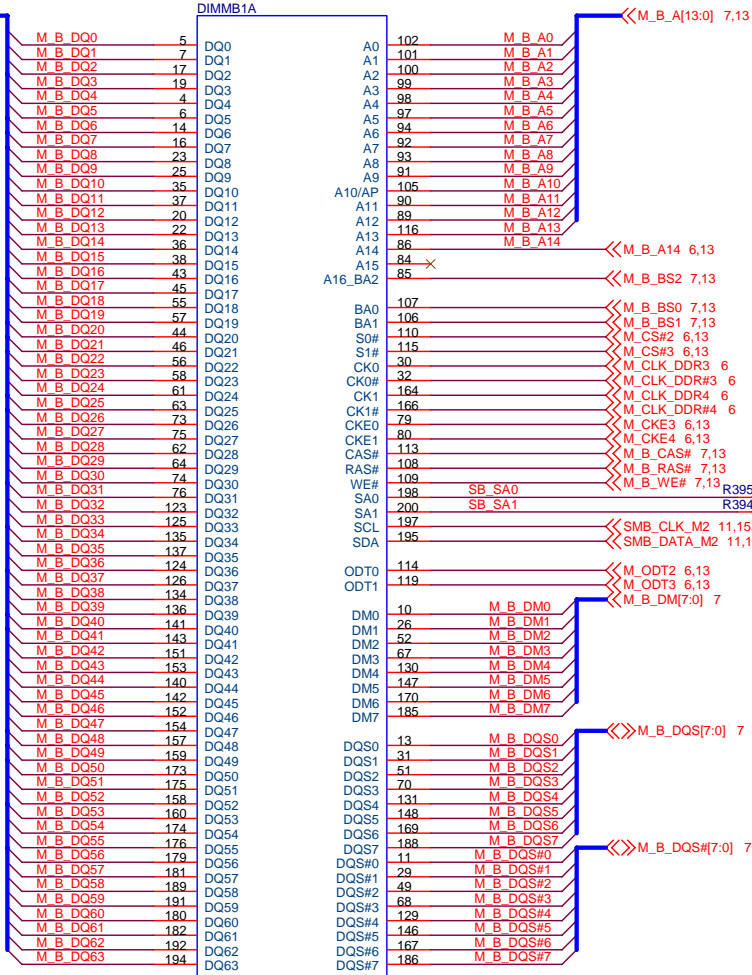


Cap close to thermal sensor
Trace : 10/4/10

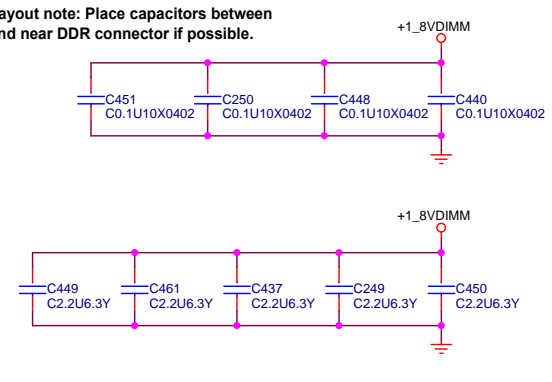


MSI CORPORATION		
DDR2 SODIMM 0		
Title	Document Number	Rev
	Custom MS-1221	1.0
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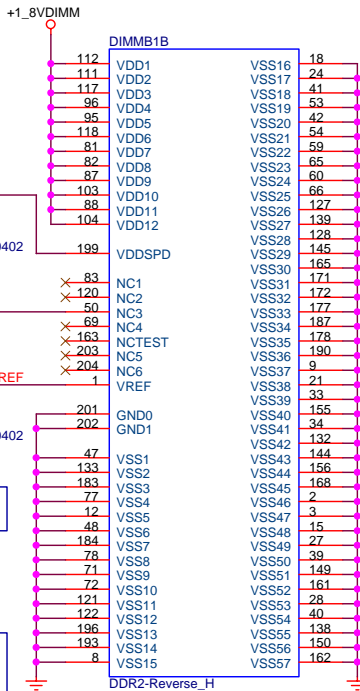
7 M_B_DQ[63:0] <<>



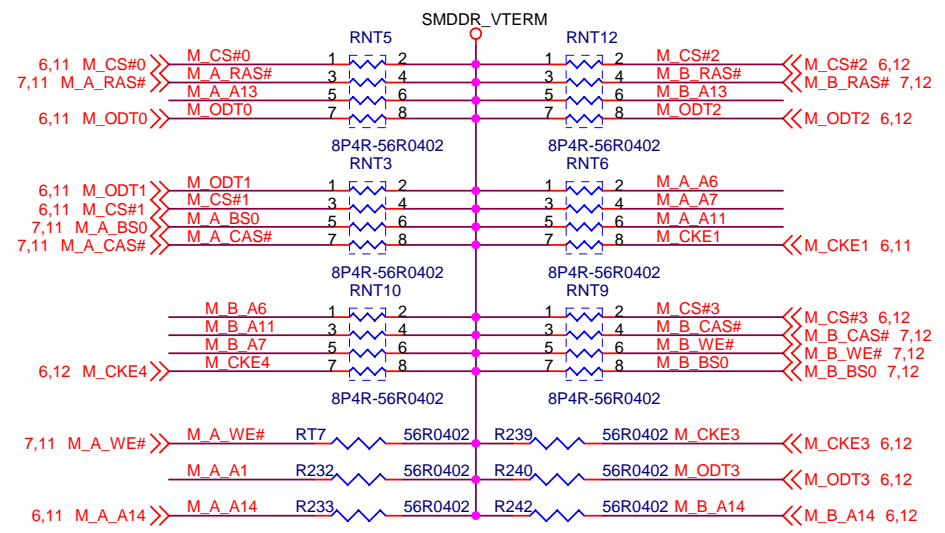
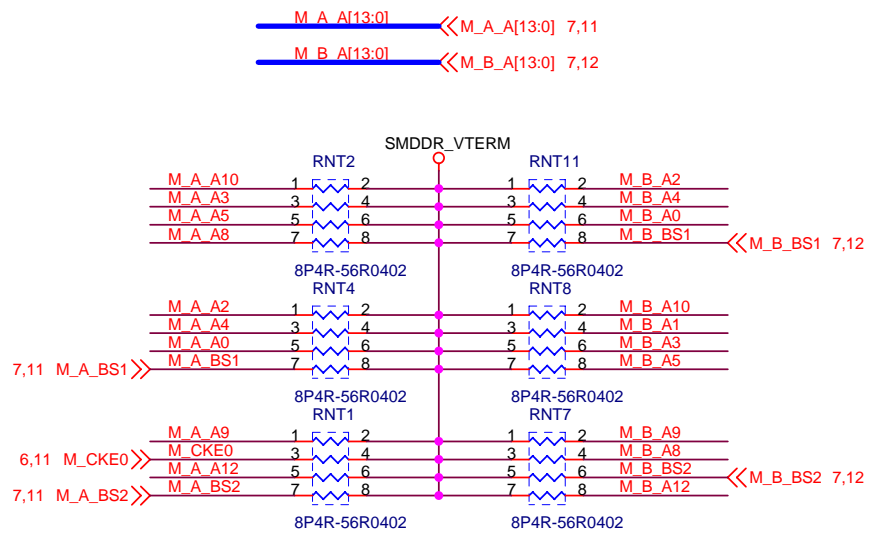
DDR2-Reverse_H



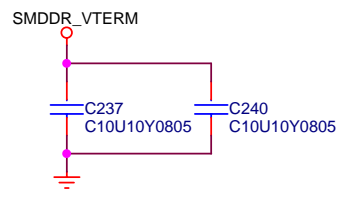
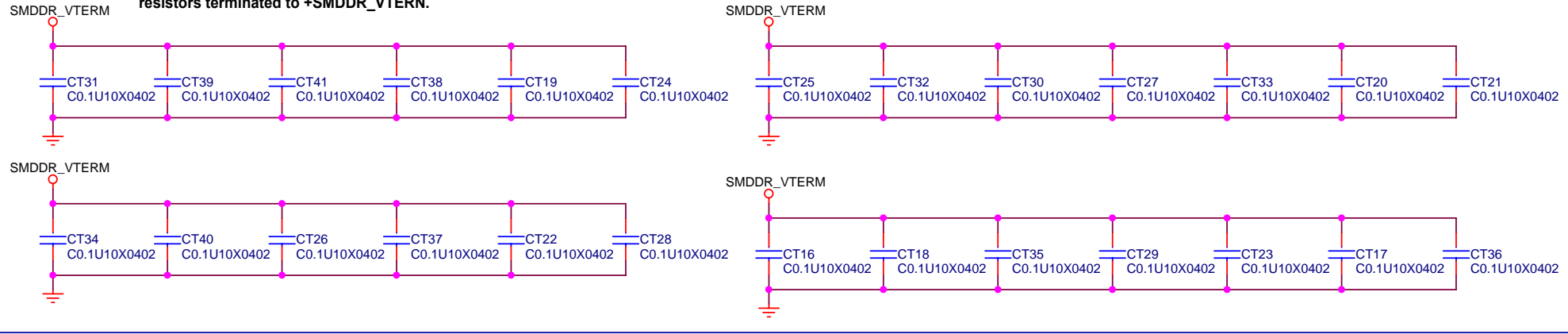
as close as SO-DIMM Trace : 10 mils



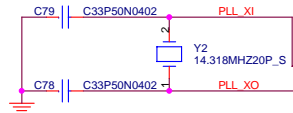
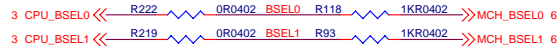
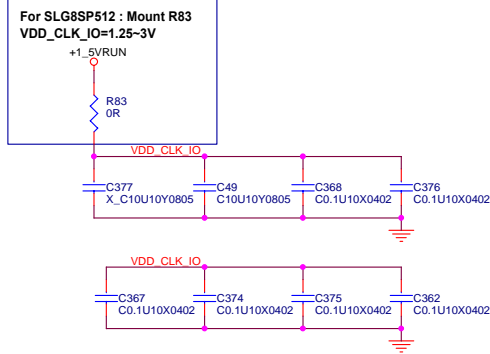
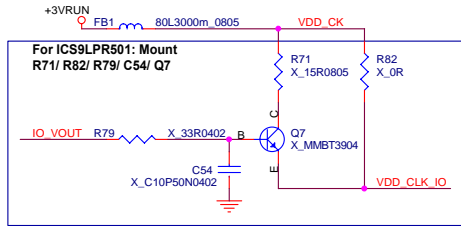
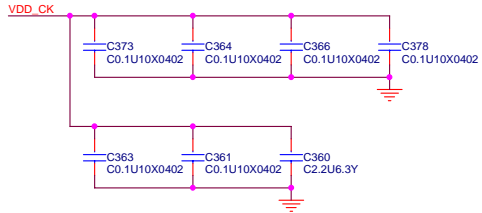
MSI CORPORATION			
Title			
DDR2 SODIMM 1			
Size	Document Number	Rev	
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Layout note: Place one cap close to every 2 pullup resistors terminated to +SMDDR_VTERN.



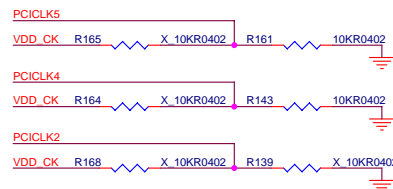
MSI CORPORATION		
DDR2 TREMINATION		
Title		
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Tuesday, March 13, 2007	Sheet 13 of 41



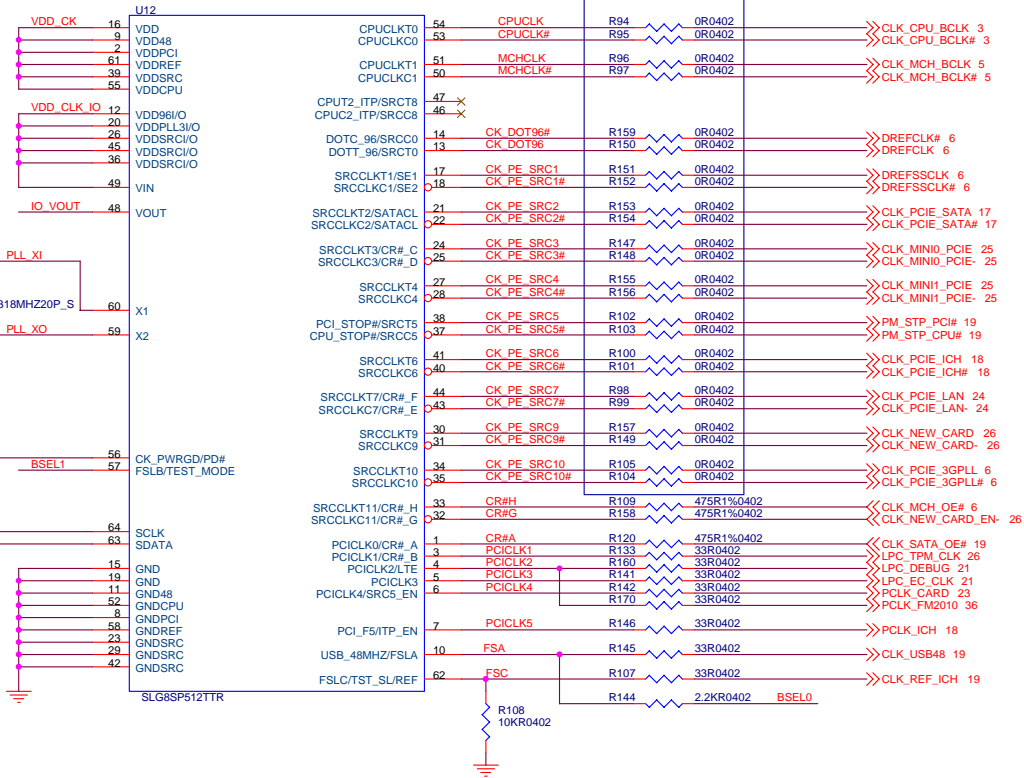
19 CLK_PWRGD >> BSEL1

11,12,19,36 SMB_CLK_M2 >>
11,12,19,36 SMB_DATA_M2 >>

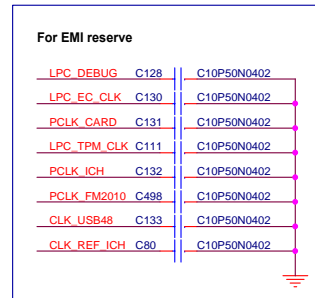
PIN#	DESCRIPTION	USAGE
1	Control SRC2 pair	CR#_A
32	Control SRC9 pair	CR#_G
33	Control SRC10 pair	CR#_H

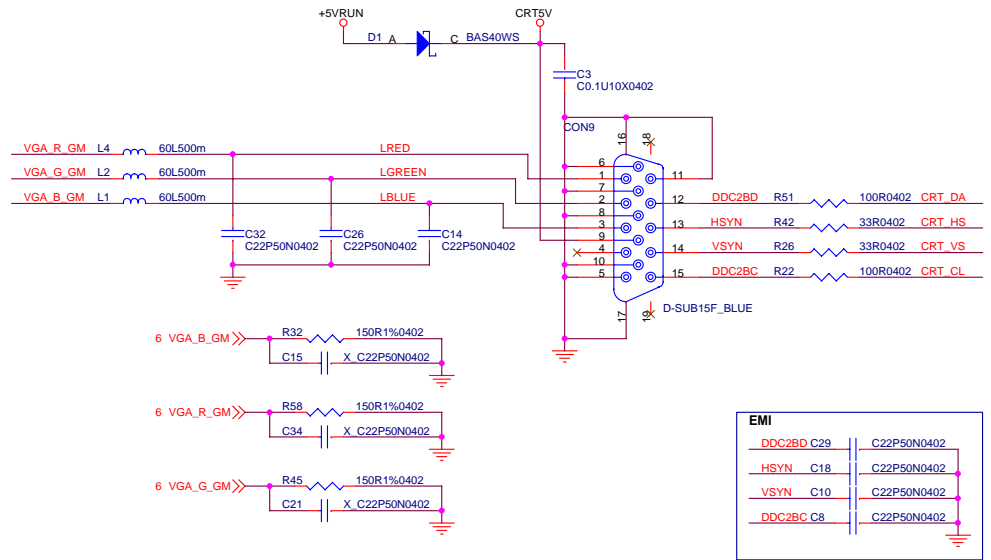
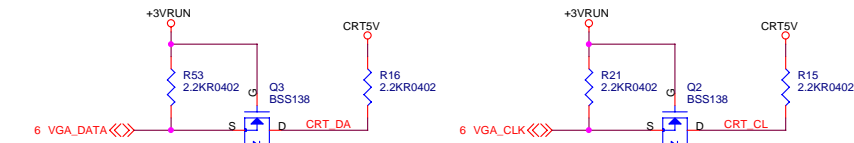
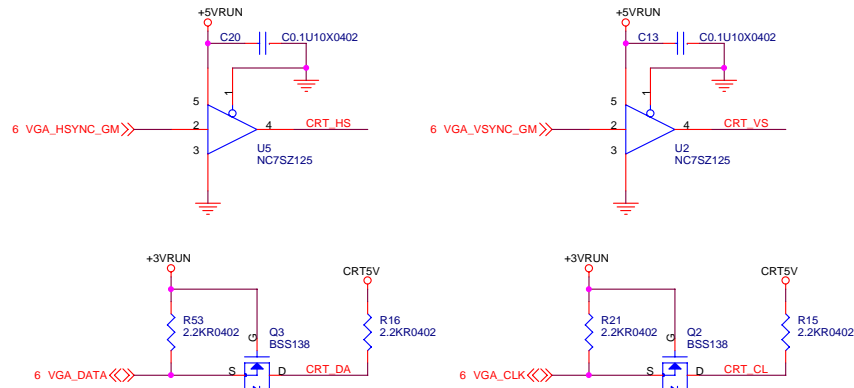


The serial resistors
of differential pairs
SLG8SP512 : pop 0R
ICS9LP505 : pop 33R



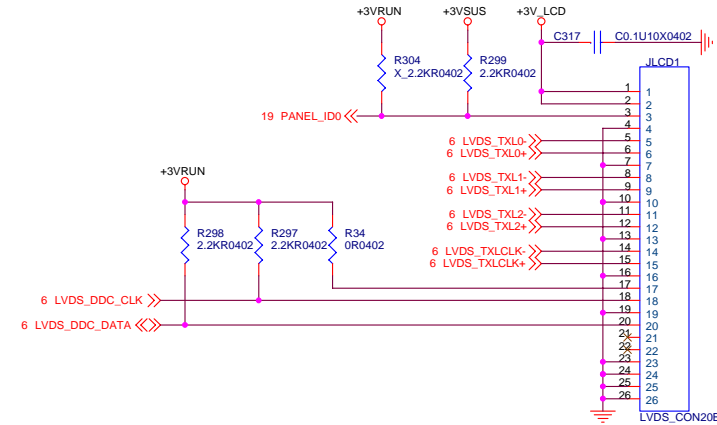
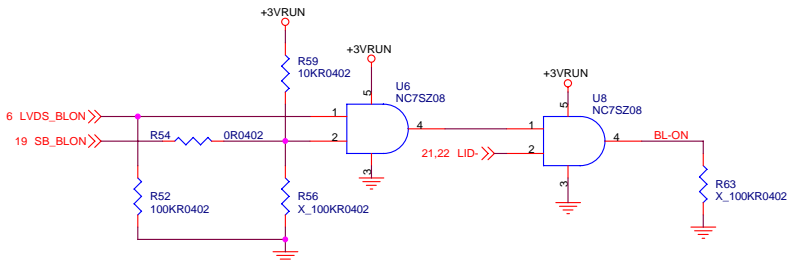
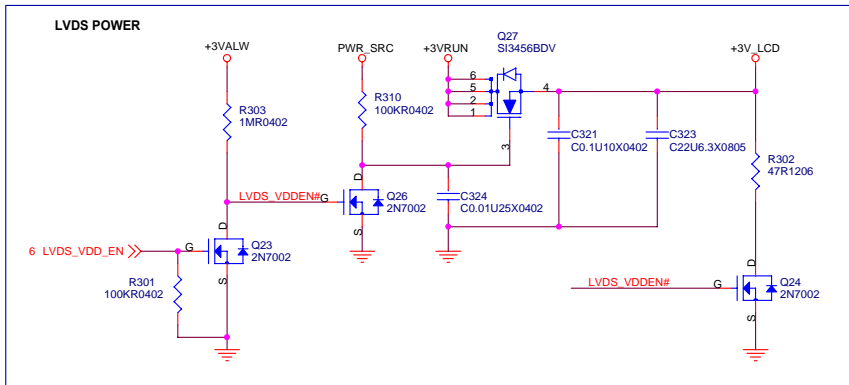
FSC	FSB	FSA	CPU
Bit7	Bit6	Bit5	MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00





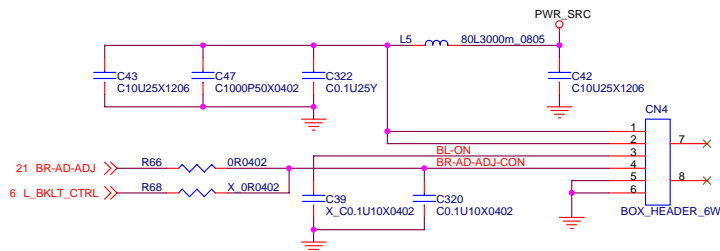
EMI

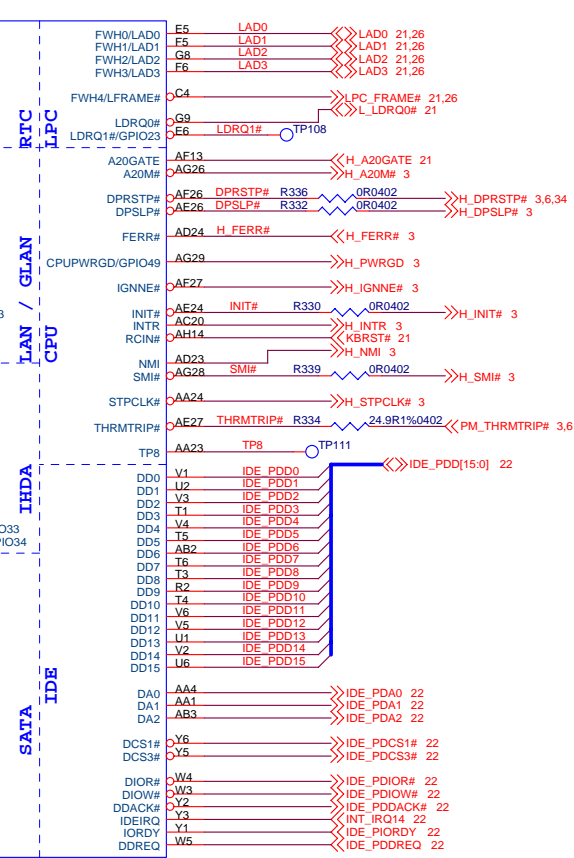
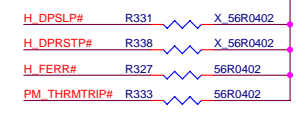
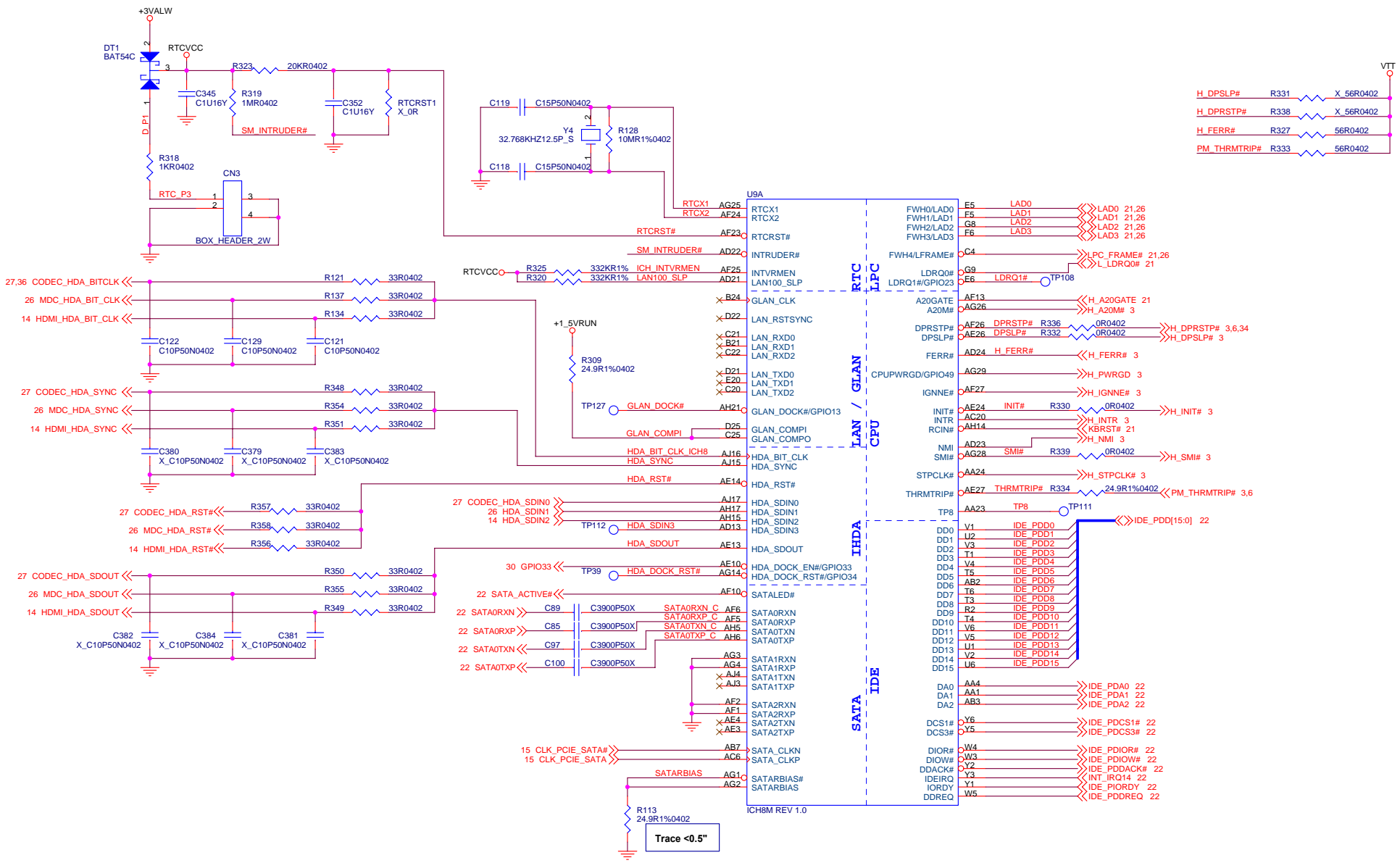
DDC2BD C29	C22P50N0402
HSYN C18	C22P50N0402
VSYN C10	C22P50N0402
DDC2BC C8	C22P50N0402



CABLE PIN DEFINE

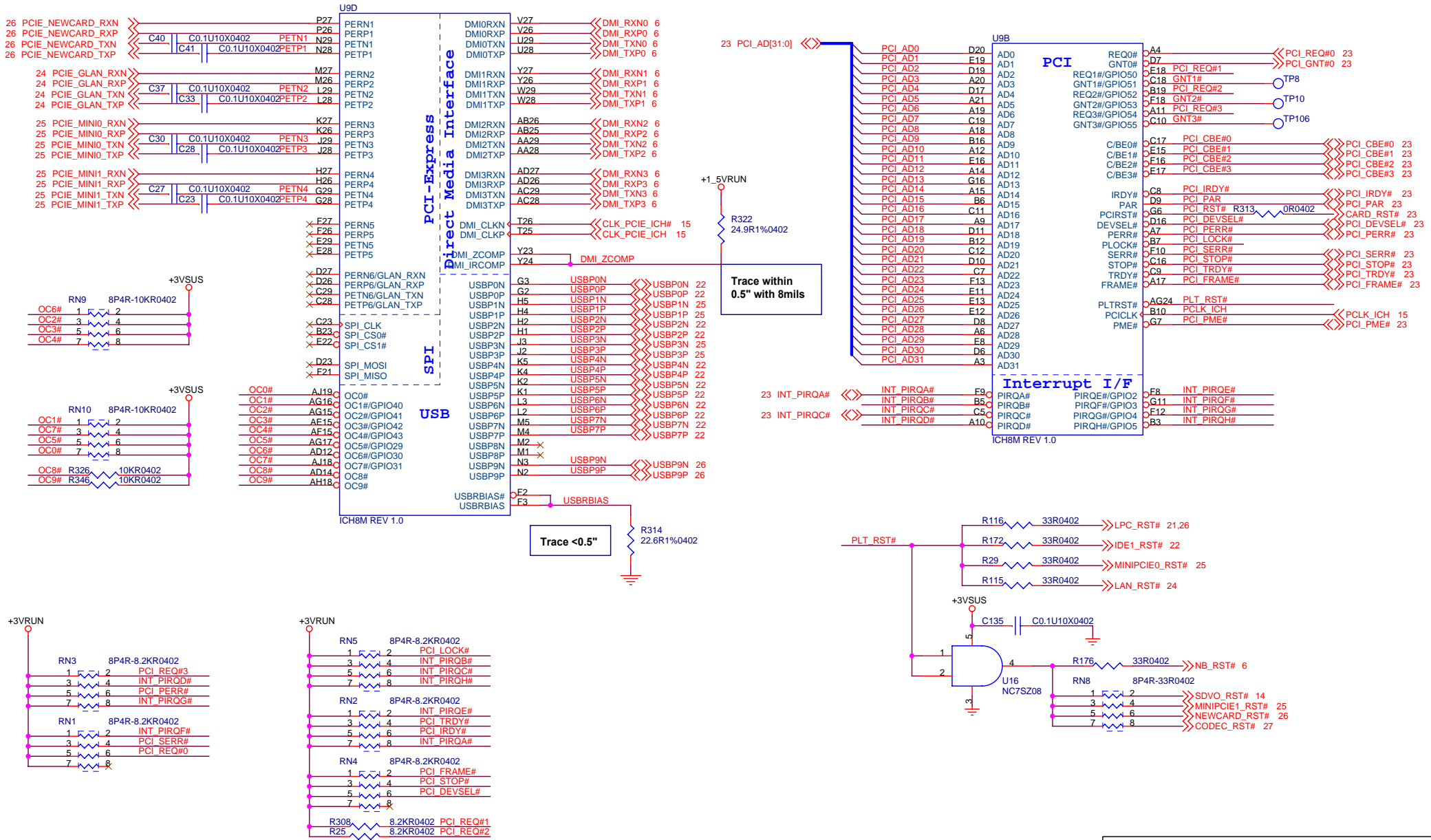
LCD CABLE	JLCD1
1	===== GND
2	===== 1
3	===== 2
4	===== 17
5	===== NC
6	===== 18
7	===== 20
8	===== 5
9	===== 6
10	===== GND
11	===== 8
12	===== 9
13	===== GND
14	===== 11
15	===== 12
16	===== GND
17	===== 14
18	===== 15
19	===== GND
20	===== GND



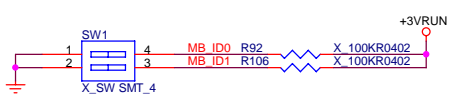
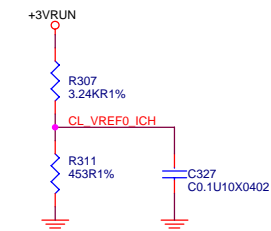
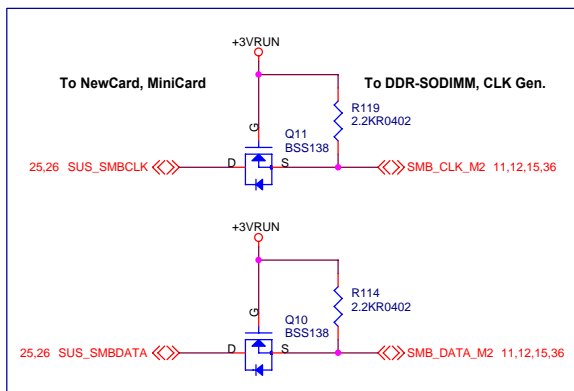
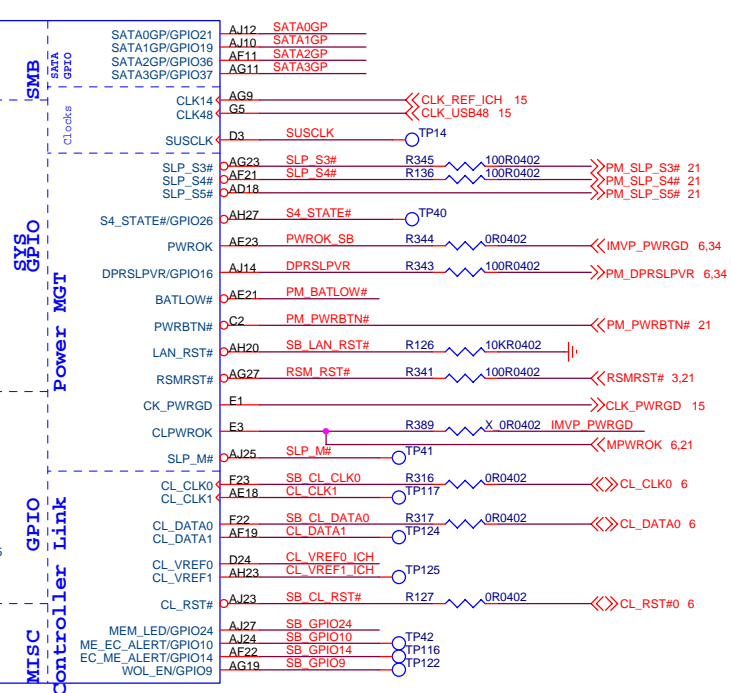
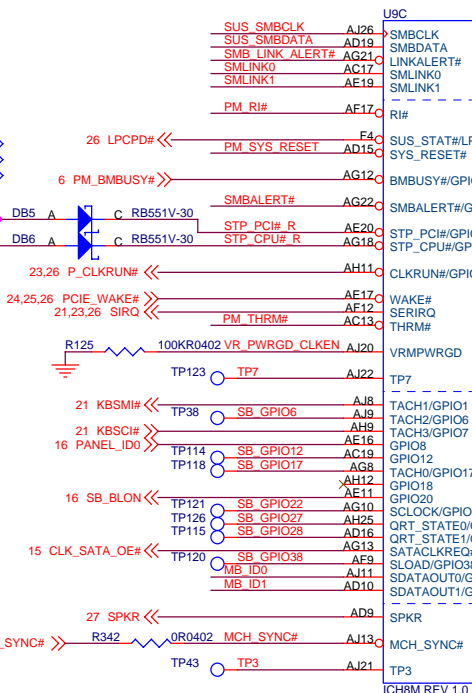
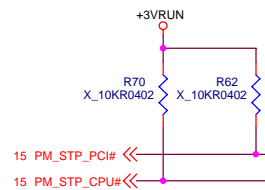
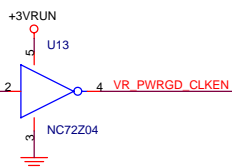
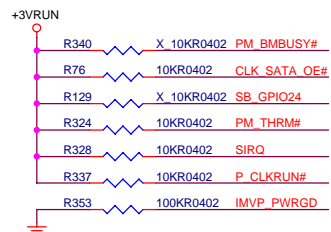
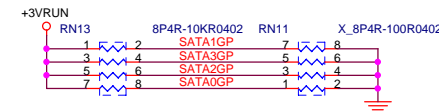
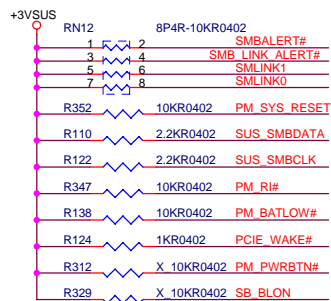


MSI CORPORATION		
Title		
ICH8M-1 (CPU/IDE/Azalia)		
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Monday, March 19, 2007	Sheet 17 of 41

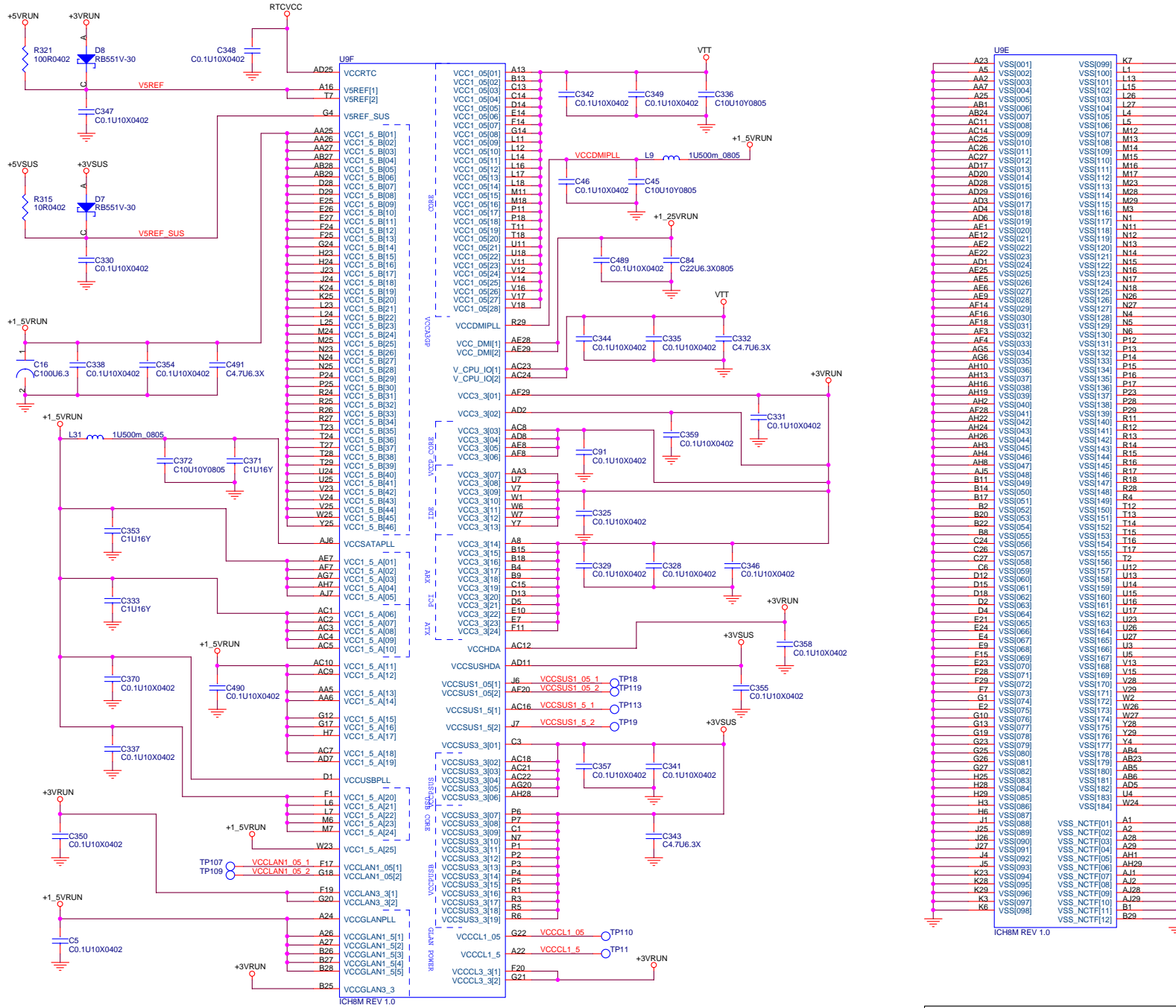
place Cap close to ICH8
within 250mils



MSI CORPORATION			
Title			
ICH8M-2 (PCI/USB/PCIE/DMI)			
Size	Document Number		Rev
Custom	MS-1221		1.0
Date:	Monday, March 19, 2007	Sheet	18 of 41

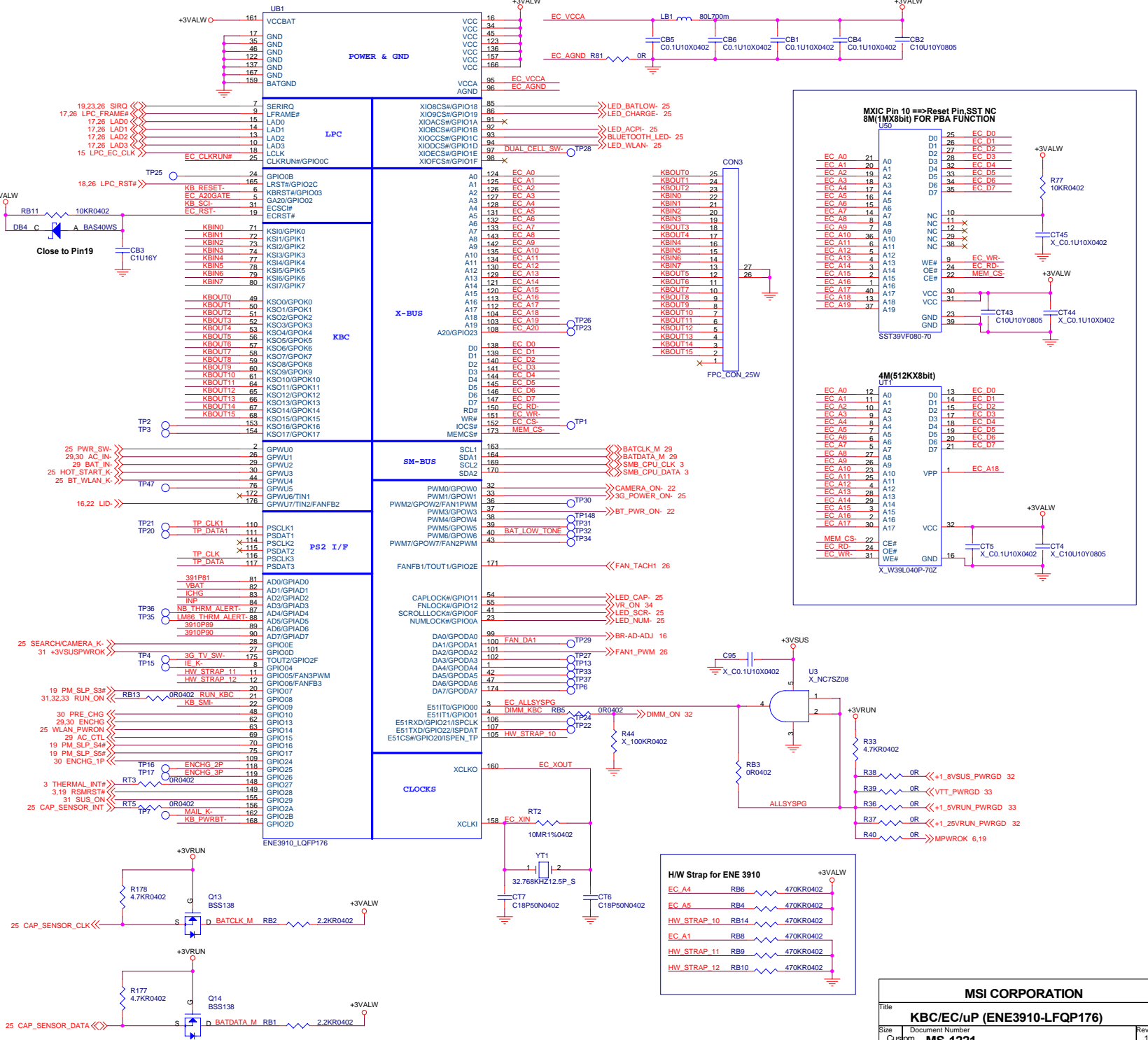
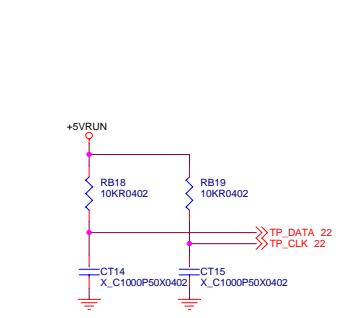
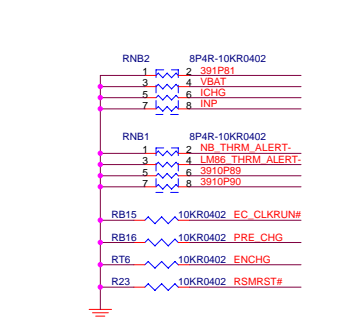
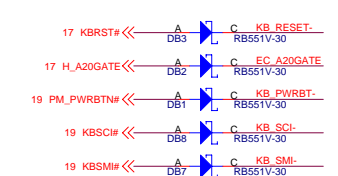
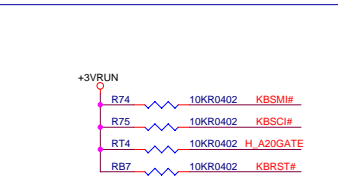
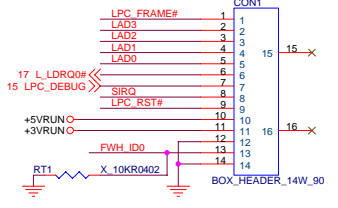


MSI CORPORATION		
Title		
ICH8M-3 (SM BUS/GPIO)		
Size	Document Number	Rev
A3	MS-1221	1.0
Date:	Monday, March 19, 2007	Sheet 19 of 41



U9E	VSS[099]	K7
A23	VSS[001]	L1
A5	VSS[002]	L3
AA7	VSS[003]	L13
AA7	VSS[004]	L15
A25	VSS[005]	L26
AB1	VSS[006]	L37
AB24	VSS[007]	L4
AC11	VSS[008]	L5
AC14	VSS[009]	M12
AC25	VSS[010]	M3
AC26	VSS[011]	M14
AC27	VSS[012]	M15
AD17	VSS[013]	M16
AD20	VSS[014]	M17
AD28	VSS[015]	M23
AD29	VSS[016]	M28
AD3	VSS[017]	M29
AD4	VSS[018]	M3
AD6	VSS[019]	N1
AE1	VSS[020]	N11
AE12	VSS[021]	N12
AE2	VSS[022]	N13
AE22	VSS[023]	N14
AD1	VSS[024]	N15
AE25	VSS[025]	N17
AE6	VSS[026]	N18
AE9	VSS[027]	N26
AF14	VSS[028]	N27
AF16	VSS[029]	N4
AF18	VSS[030]	N5
AF3	VSS[031]	N6
AF4	VSS[032]	P12
AG5	VSS[033]	P13
AG6	VSS[034]	P14
AH10	VSS[035]	P15
AH13	VSS[036]	P16
AH16	VSS[037]	P17
AH19	VSS[038]	P23
AH2	VSS[039]	P28
AH28	VSS[040]	P29
AH42	VSS[041]	R11
AH26	VSS[042]	R12
AH24	VSS[043]	R13
AH4	VSS[044]	R14
AH4	VSS[045]	R15
AH6	VSS[046]	R16
AH5	VSS[047]	R17
B1	VSS[048]	R18
B14	VSS[049]	R28
B2	VSS[050]	R4
B17	VSS[051]	R7
B20	VSS[052]	T13
B22	VSS[053]	T14
B8	VSS[054]	T15
C24	VSS[055]	T16
C26	VSS[056]	T17
C27	VSS[057]	T2
D6	VSS[058]	T2
D15	VSS[059]	U12
D12	VSS[060]	U13
D18	VSS[061]	U14
D2	VSS[062]	U15
D4	VSS[063]	U16
E4	VSS[064]	U17
E9	VSS[065]	U23
E15	VSS[066]	U26
E23	VSS[067]	U27
F28	VSS[068]	U3
F7	VSS[069]	U5
G1	VSS[070]	U13
E2	VSS[071]	U16
G10	VSS[072]	U19
G13	VSS[073]	U26
G19	VSS[074]	U29
G23	VSS[075]	U28
G25	VSS[076]	U27
G26	VSS[077]	U28
G27	VSS[078]	U29
H25	VSS[079]	U4
H28	VSS[080]	U4
H29	VSS[081]	U4
H3	VSS[082]	U4
H6	VSS[0	

For SW Debug



H/W Strap for ENE 3910

EC_A4	RB6	470KR0402
EC_A5	RB4	470KR0402
HW_STRAP_10	RB14	470KR0402
EC_A1	RB8	470KR0402
HW_STRAP_11	RB9	470KR0402
HW_STRAP_12	RB10	470KR0402

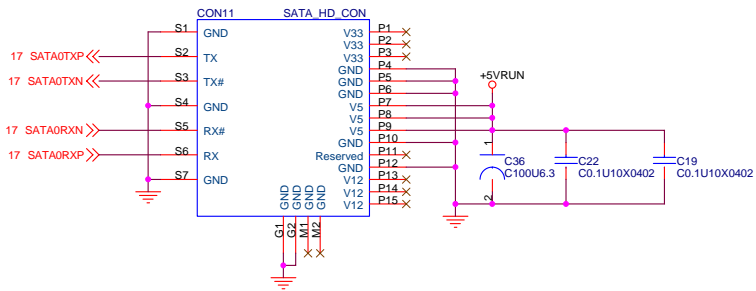
MSI CORPORATION

Part No: **KBC/EC/uP (ENE3910-LFQP176)**

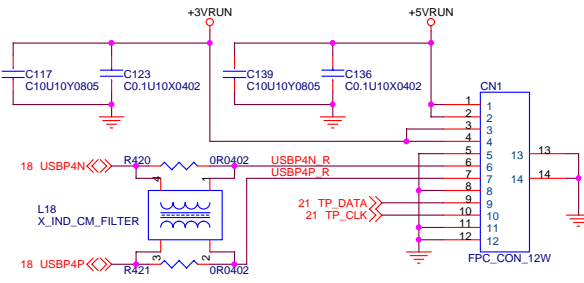
Size: Custom Document Number: **MS-1221** Rev: 1.0

Date: Wednesday, March 14, 2007 Sheet 21 of 41

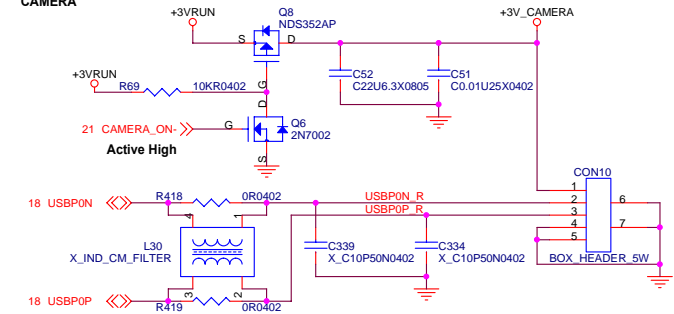
SATA HDD



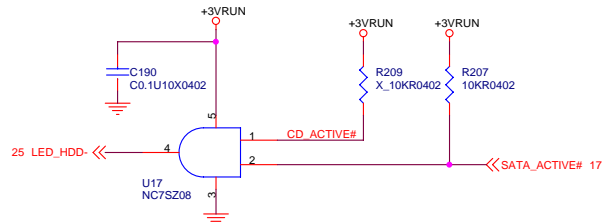
FINGERPRINT & TOUCH PAD



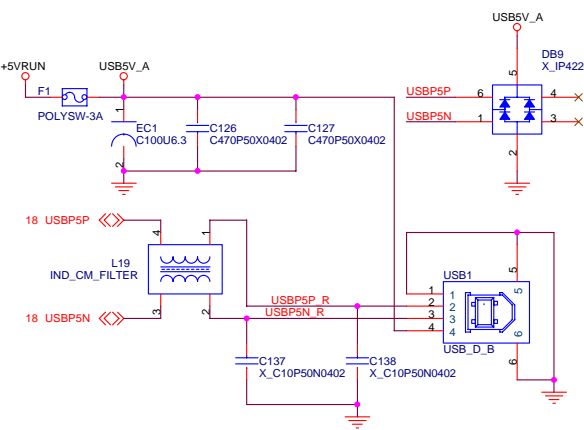
CAMERA



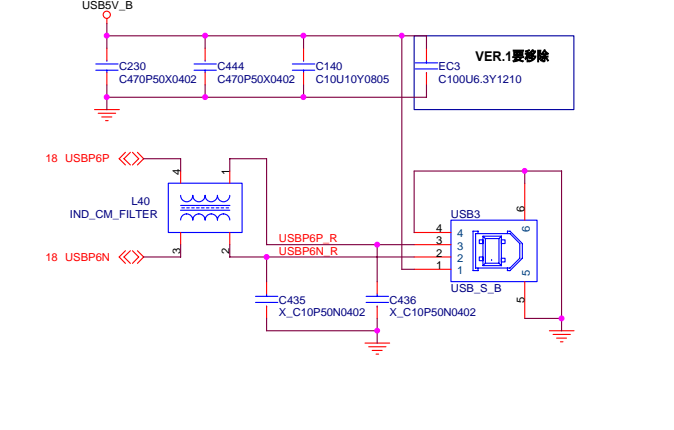
PATA CDROM/DVD



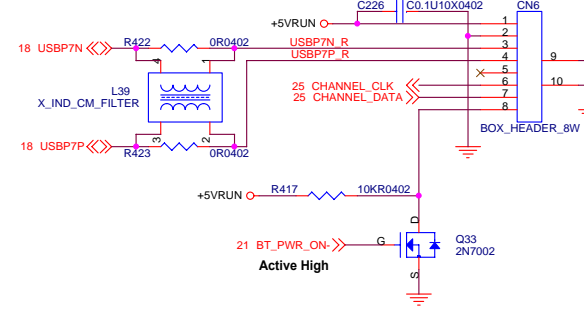
LEFT USB



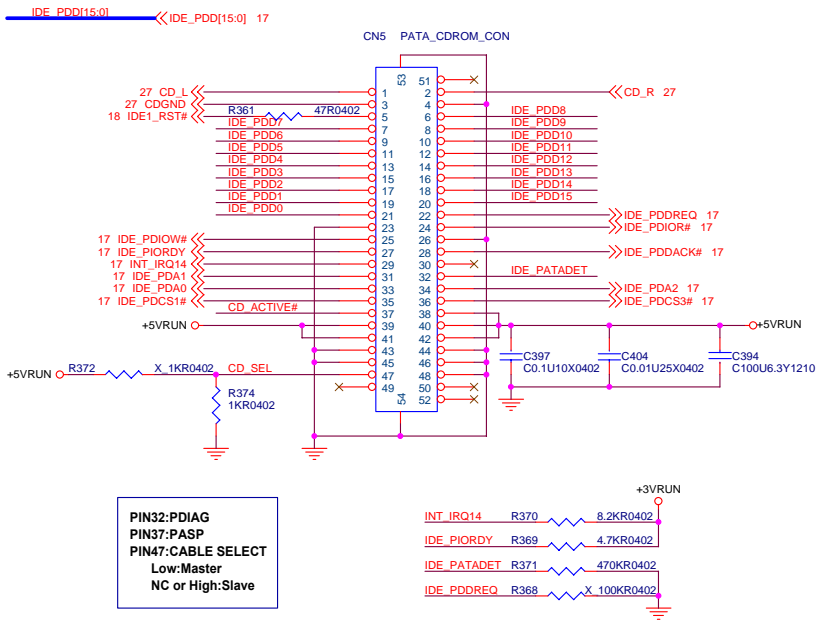
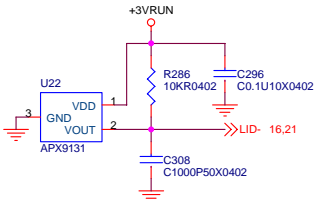
RIGHT USB



BLUETOOTH

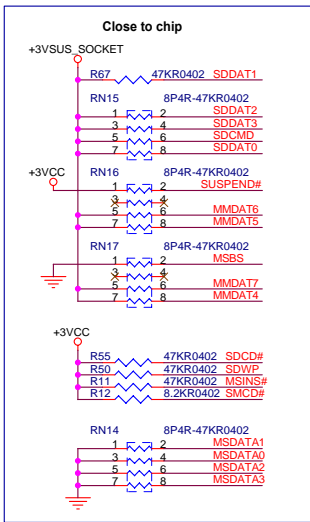


LID

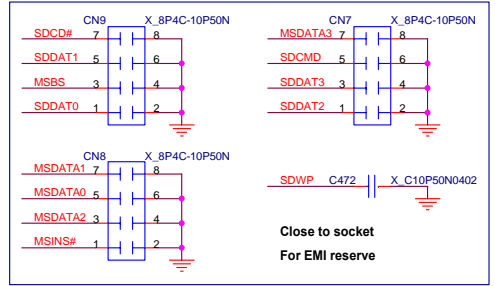
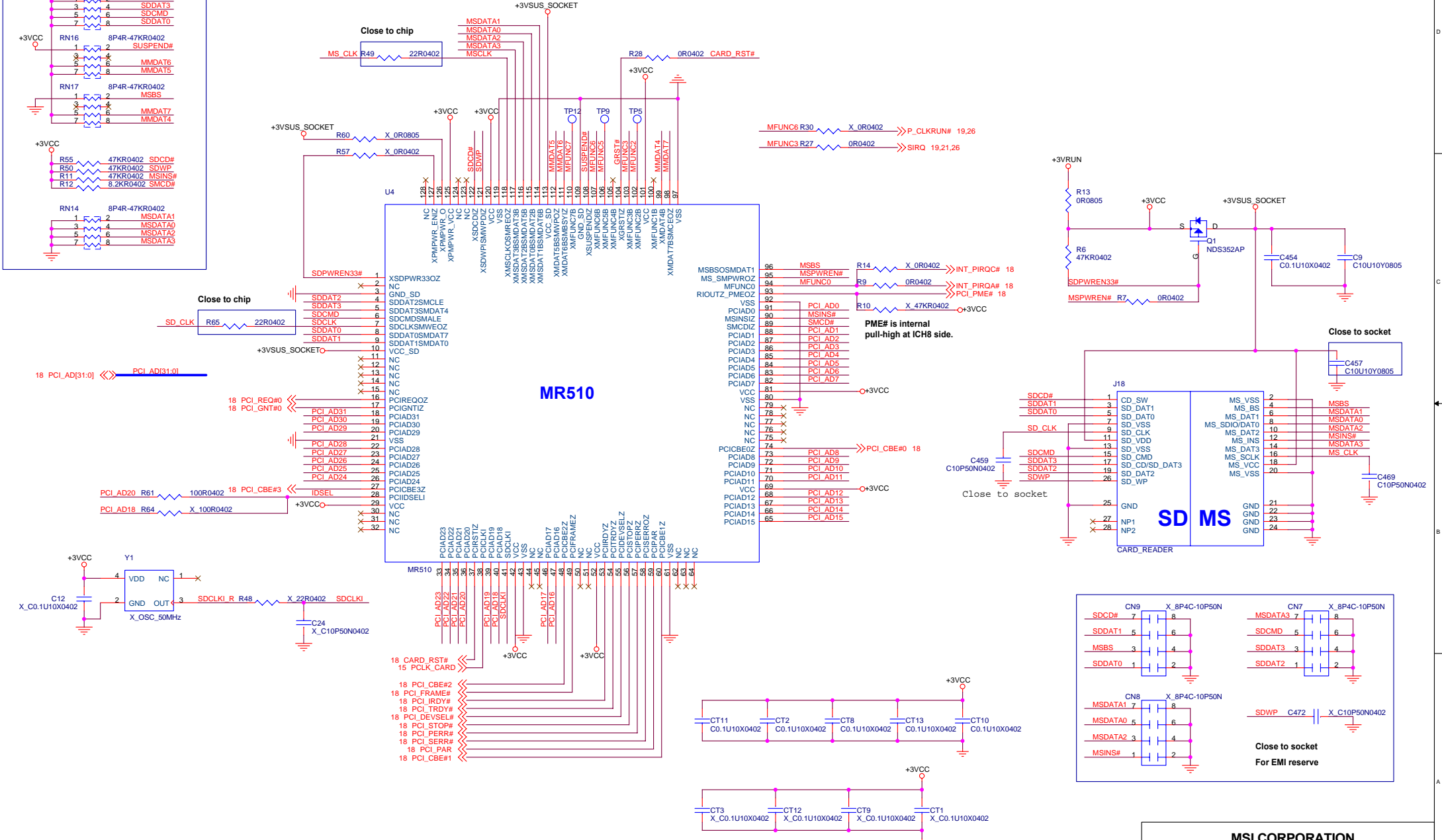


PIN32:PDIAG
PIN37:PASP
PIN47:CABLE SELECT
Low:Master
NC or High:Slave

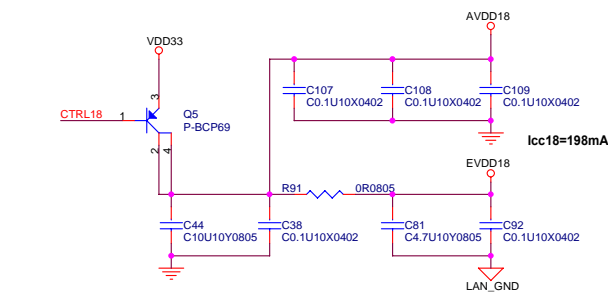
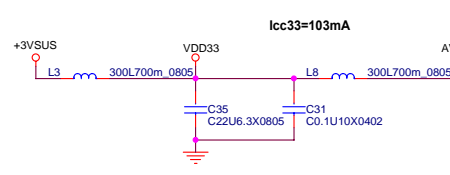
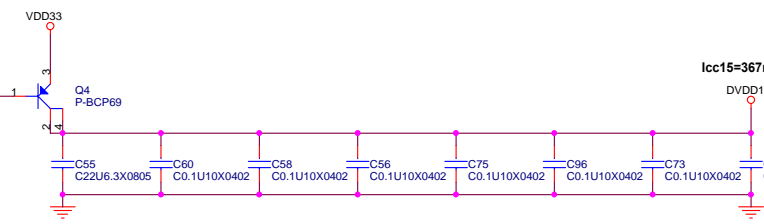
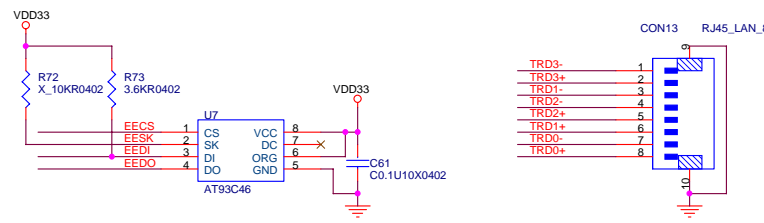
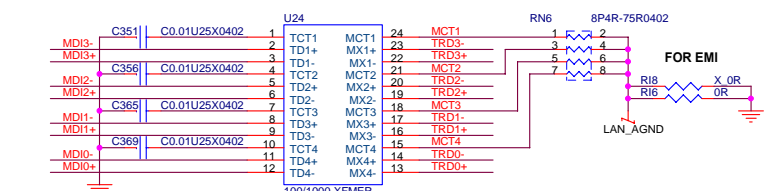
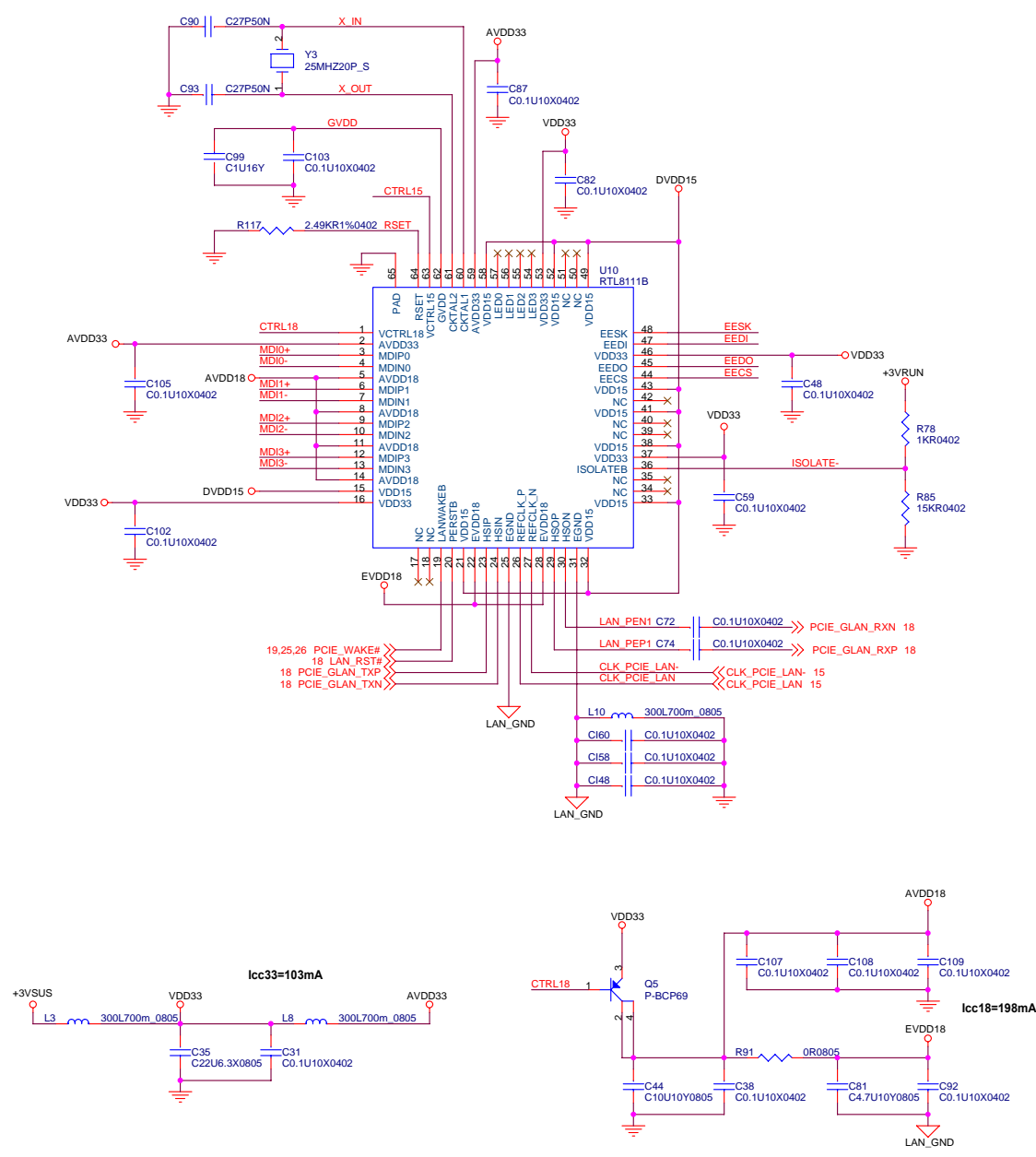
MSI CORPORATION		
Title HDD,CDROM,LID,USB		
Size Custom	Document Number MS-1221	Rev 1.0
Date: Monday, March 19, 2007	Sheet 22	of 41



GRST# should connect to Power
On reset if support S3

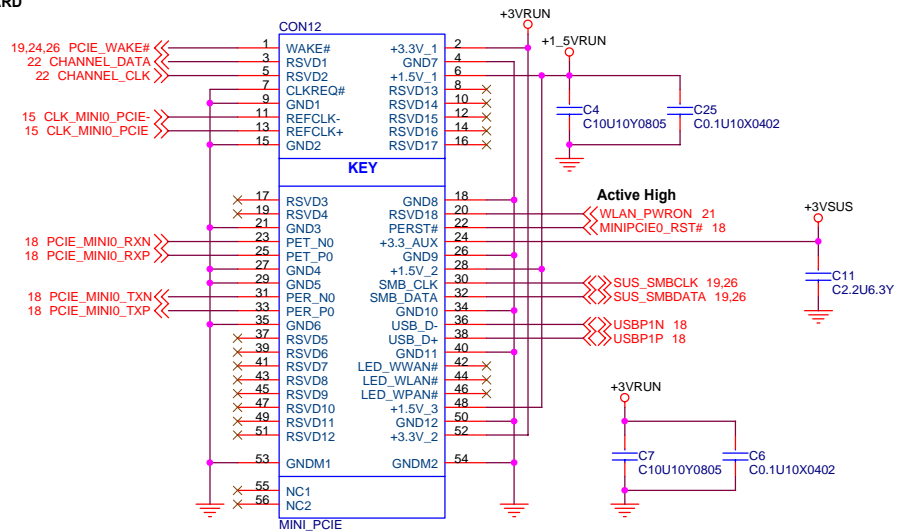


MSI CORPORATION		
Title	Card Reader (MR510)	
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Tuesday, March 13, 2007	Sheet 23 of 41

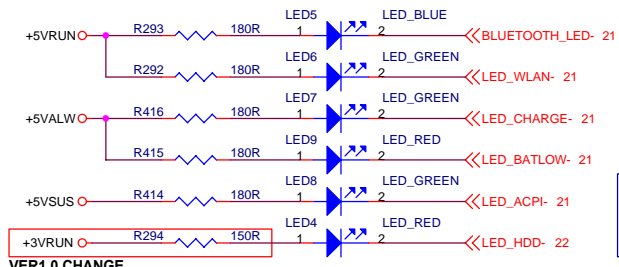
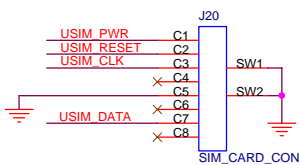
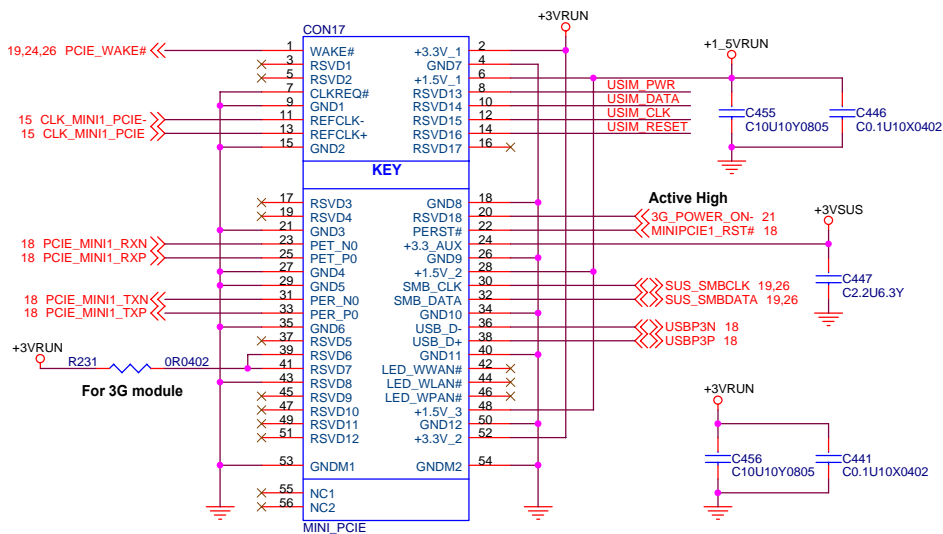


MSI CORPORATION		
Title PCIE LAN (RTL 8111B)		
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Wednesday, March 14, 2007	Sheet 24 of 41

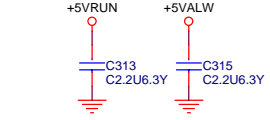
WLAN CARD



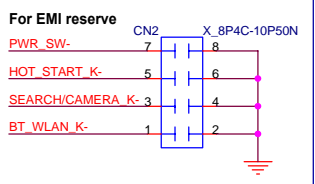
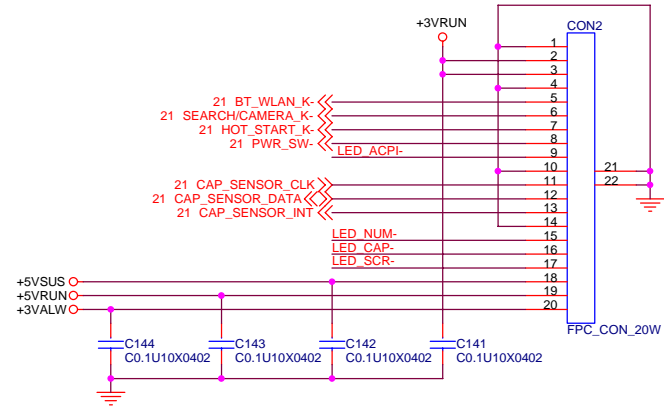
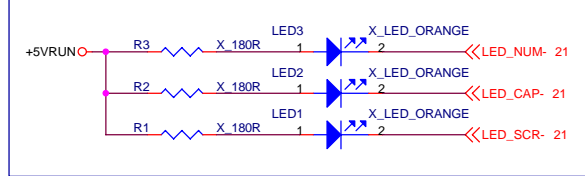
TV TUNER /3G CARD



VER1.0 CHANGE

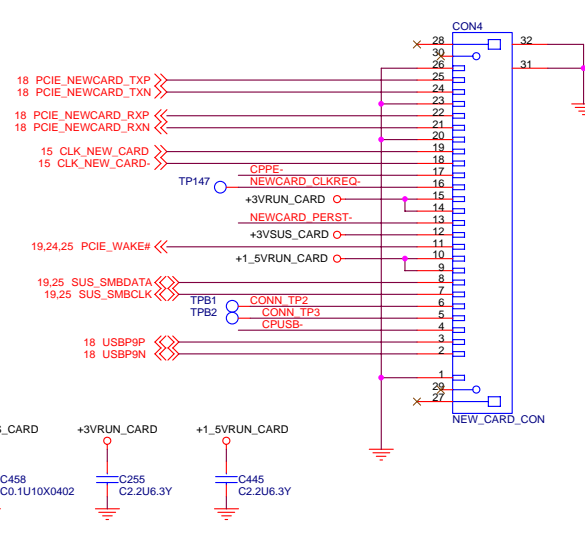
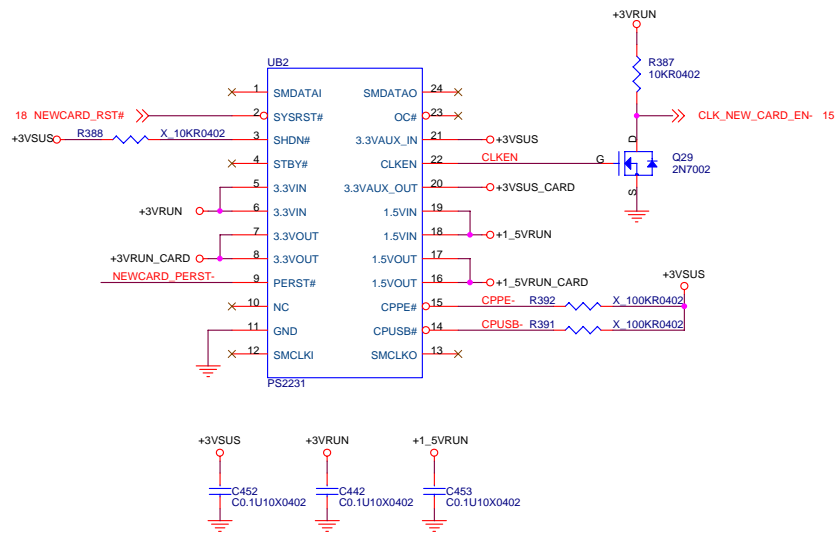


FOR DIFFERENT CUSTOMER REQUEST

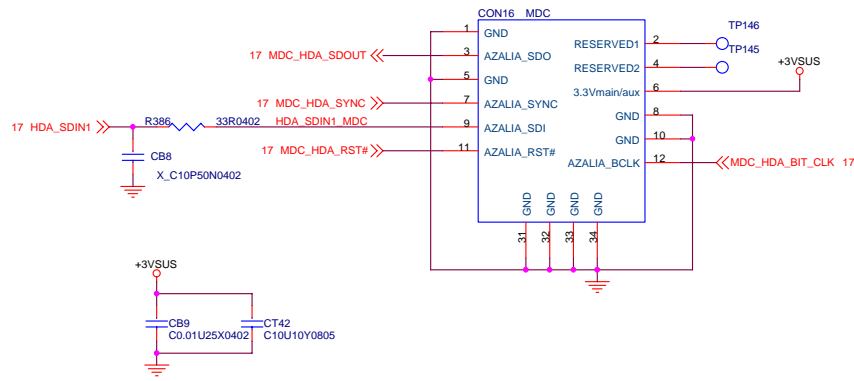


MSI CORPORATION		
Title		
MINI_PCIE, LED, SW		
Size	Document Number	Rev
Custom	MS-1221	0D
Date:	Tuesday, March 13, 2007	Sheet 25 of 41

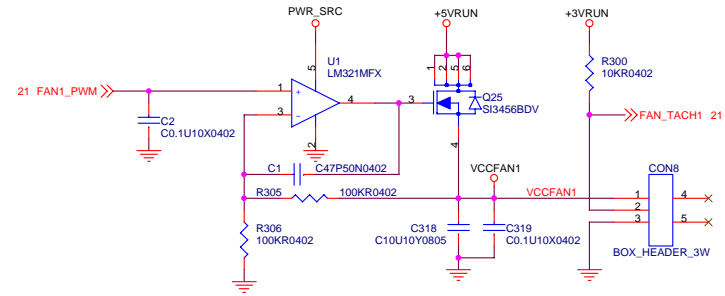
NEW CARD



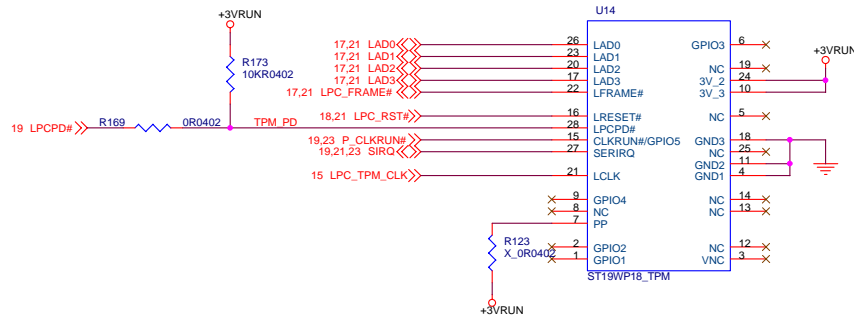
MDC Connector



CPU FAN

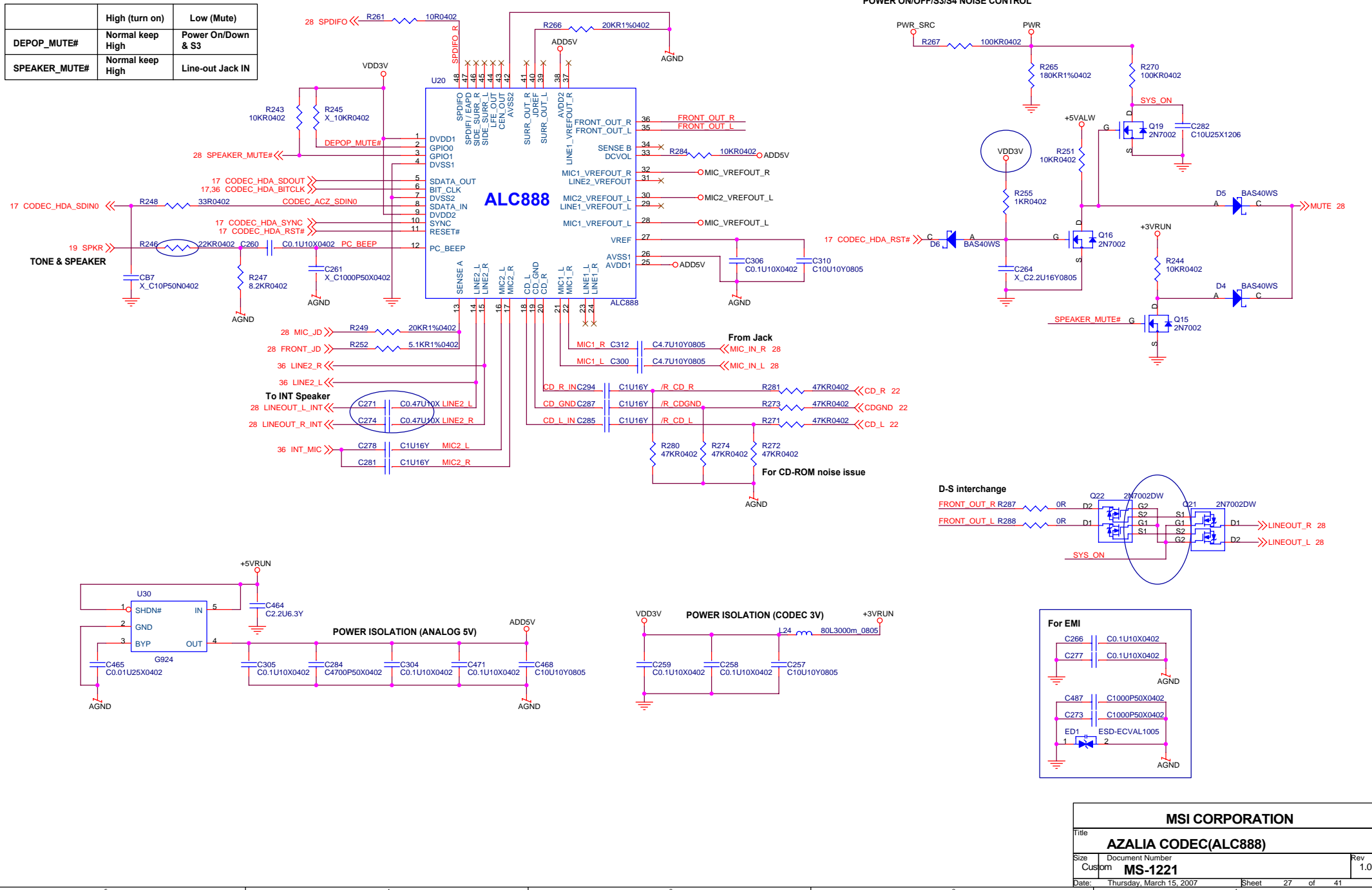


TPM 1.2



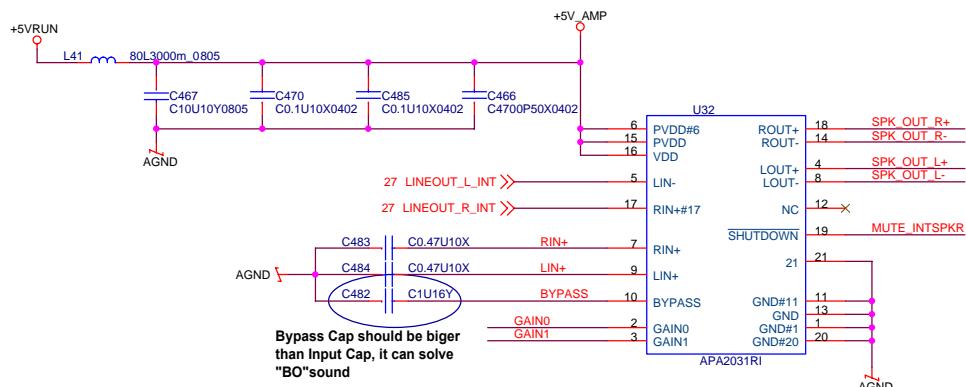
MSI CORPORATION		
Title	NEWCARD, MDC, TPM, FAN	
Size	Document Number	Rev
Custom	MS-1221	1.0
Date	Tuesday, March 13, 2007	Sheet 26 of 41

	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
SPEAKER_MUTE#	Normal keep High	Line-out Jack IN

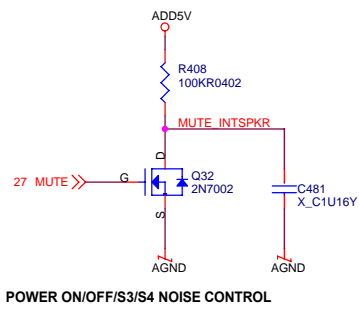


MSI CORPORATION		
Title	AZALIA CODEC(ALC888)	
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Thursday, March 15, 2007	Sheet 27 of 41

Internal Speaker Circuit



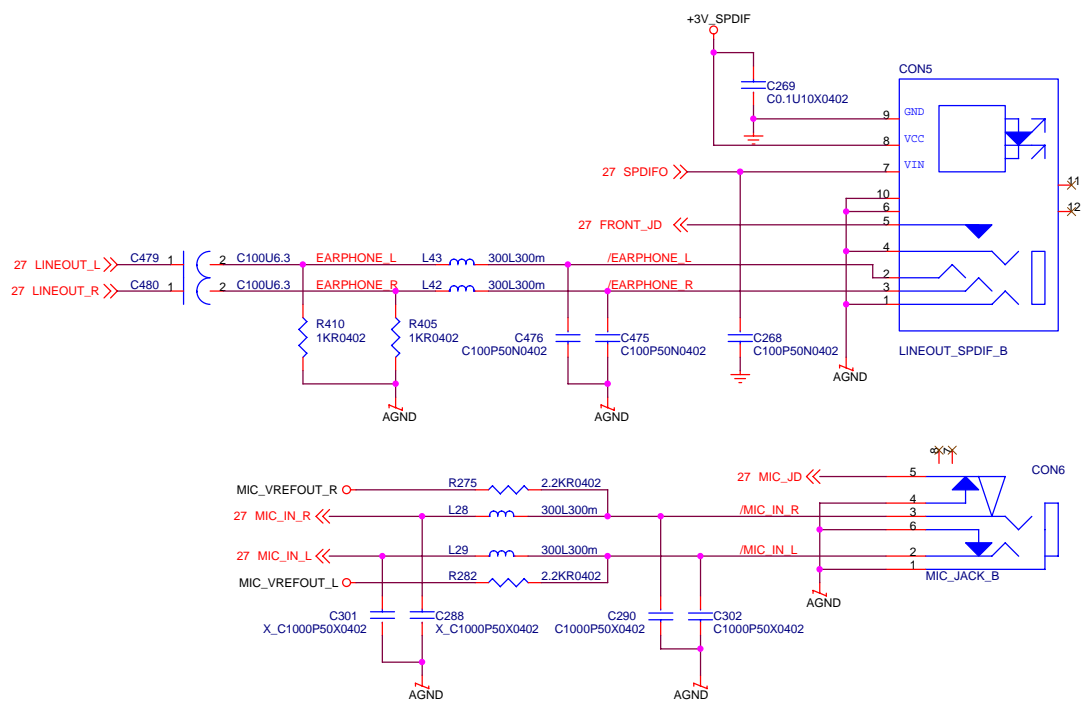
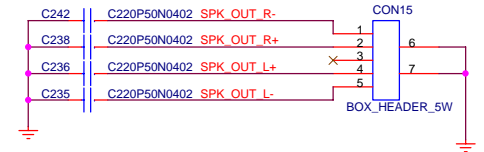
(MUTE SPEAKER)



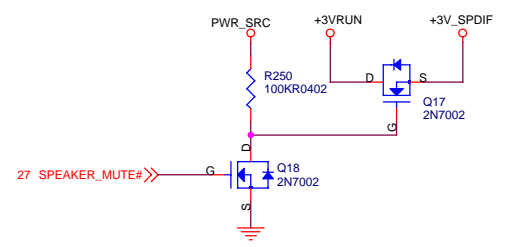
FOR APA2031

GAIN0	GAIN1
6dB	0 0
10dB	0 1
15.6dB	1 0
21.6dB	1 1
4.3dB	X X

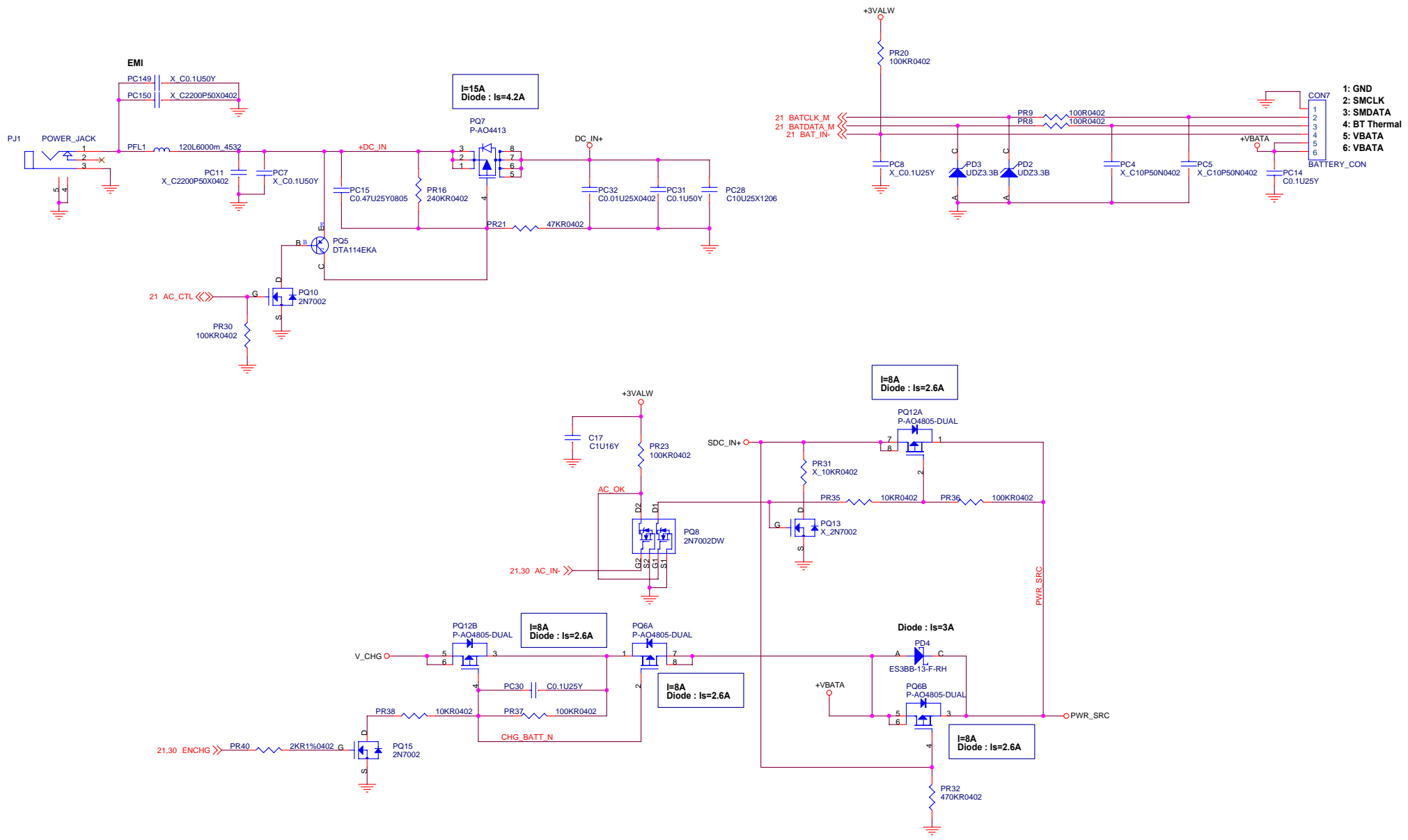
Internal Speaker Connector



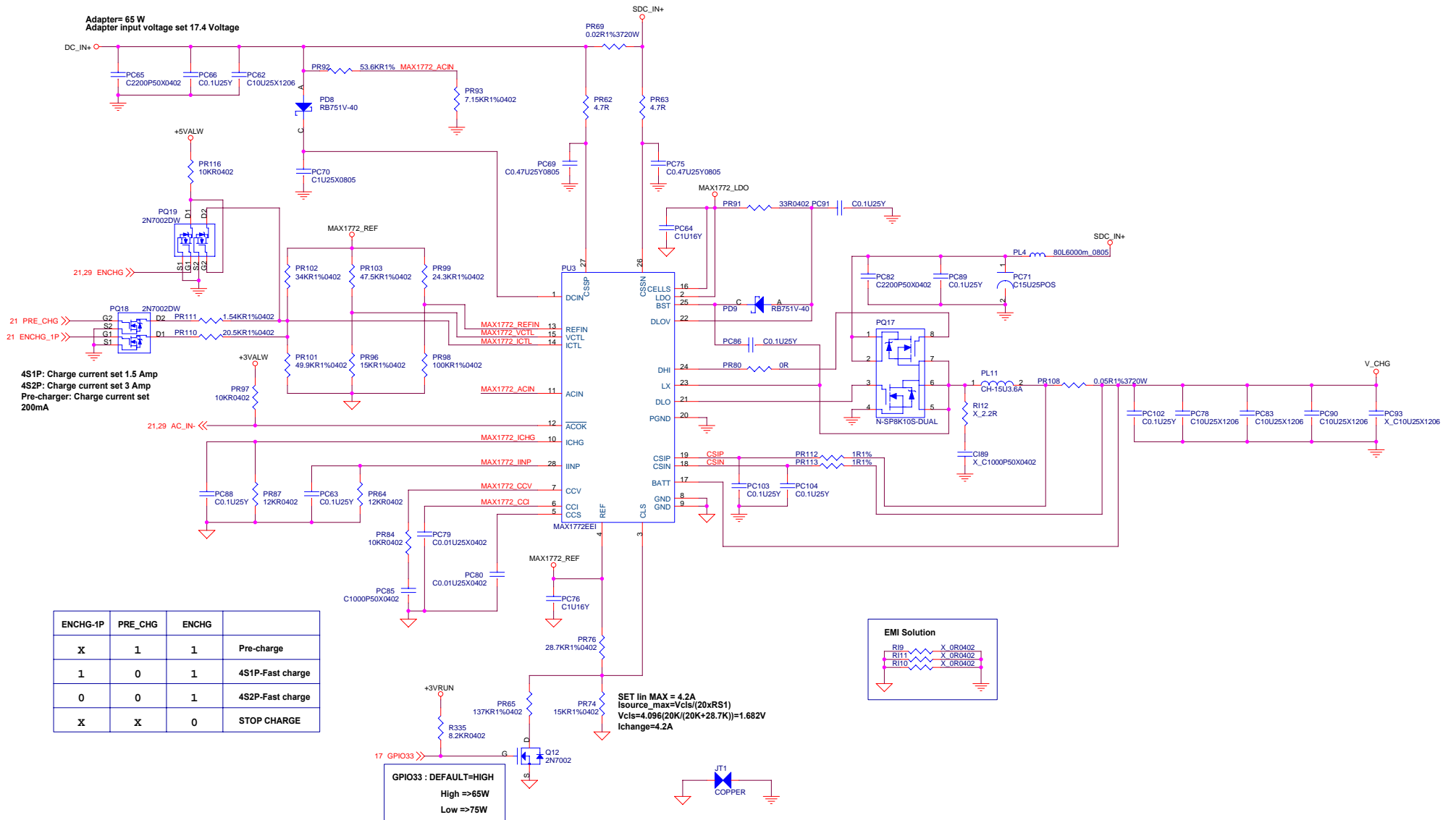
SPDIF ON/OFF CONTROL



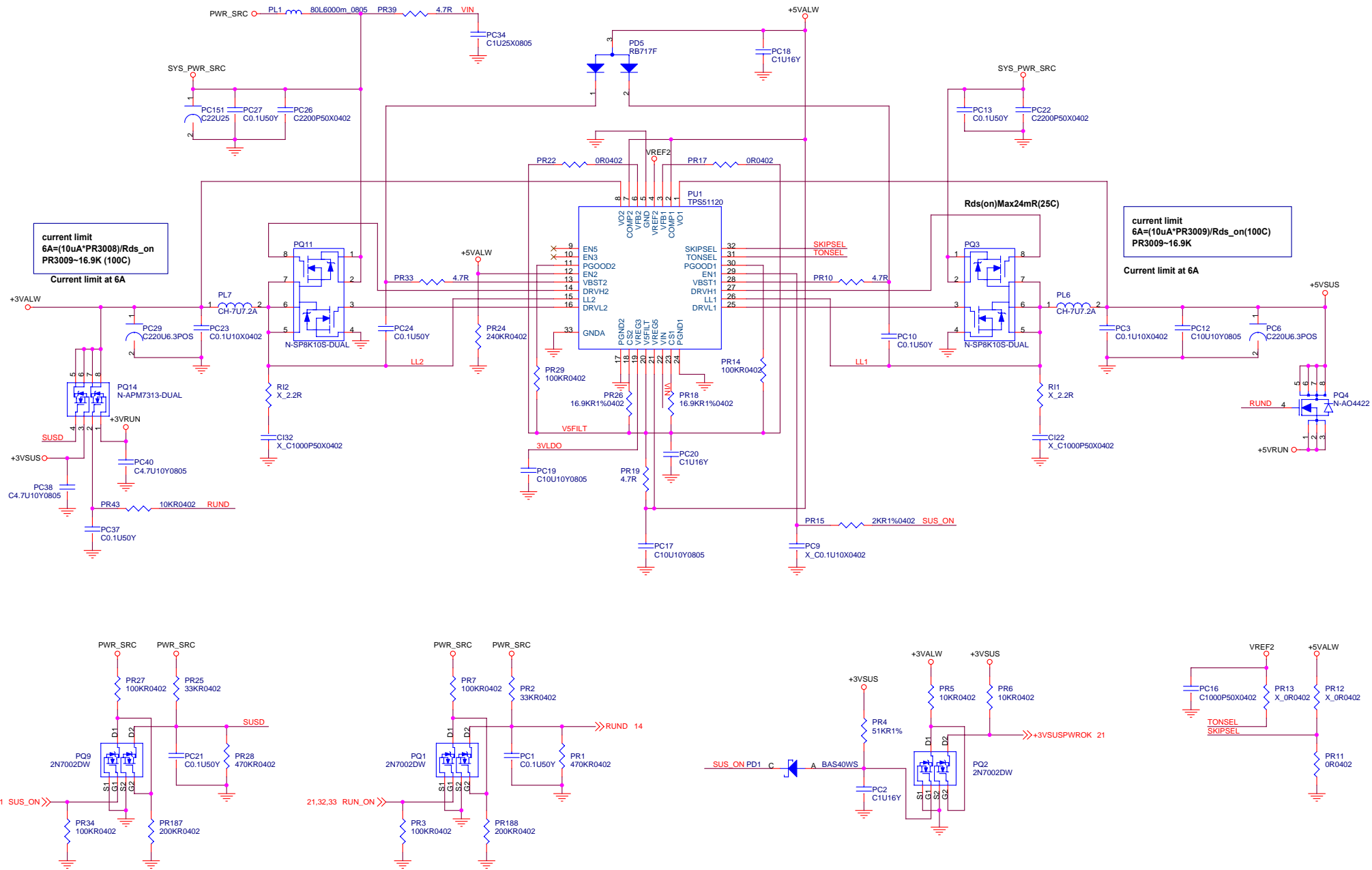
MSI CORPORATION		
Title	Audio Amp. & Jacks	
Size	Document Number	Rev
A3	MS-1221	1.0
Date:	Monday, March 19, 2007	Sheet 28 of 41



MSI CORPORATION		
Title Battery Select		
Size Custom	Document Number MS-1221	Rev 1.0
Date: Wednesday, March 14, 2007	Sheet 29	of 41

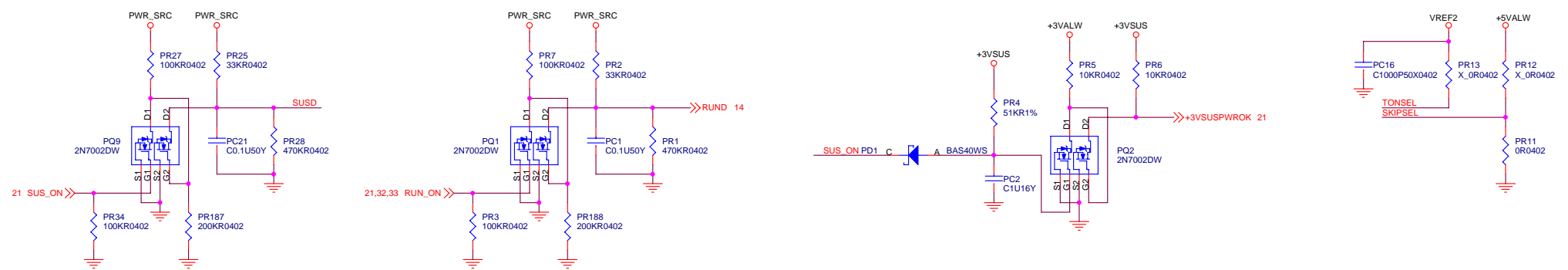


ENCHG-1P	PRE_CHG	ENCHG	
X	1	1	Pre-charge
1	0	1	4S1P-Fast charge
0	0	1	4S2P-Fast charge
X	X	0	STOP CHARGE

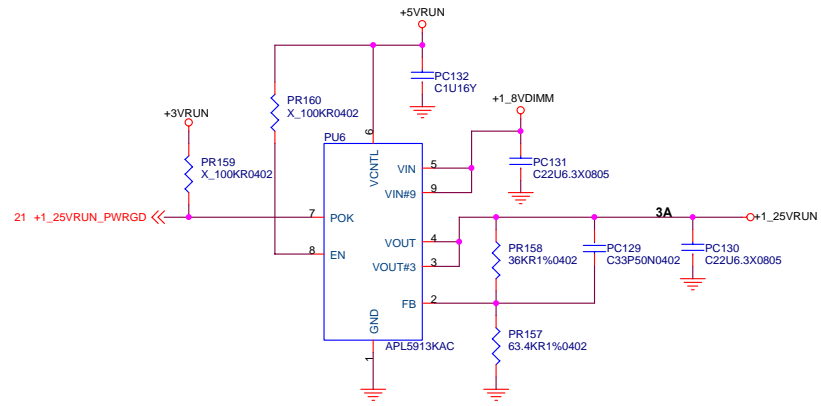
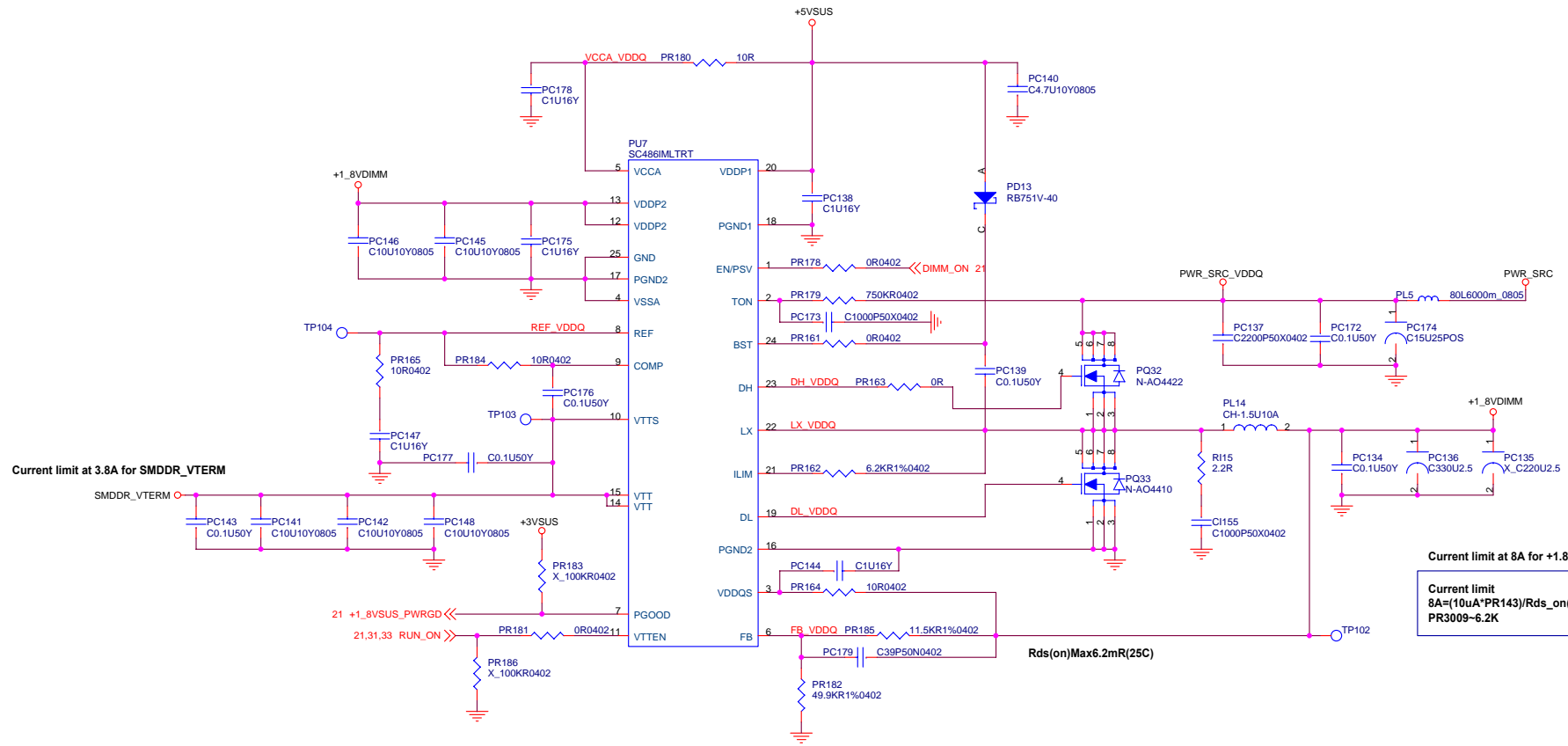


current limit
 $6A = (10\mu A \cdot PR3008) / R_{ds_on}$
 PR3009-16.9K (100C)
 Current limit at 6A

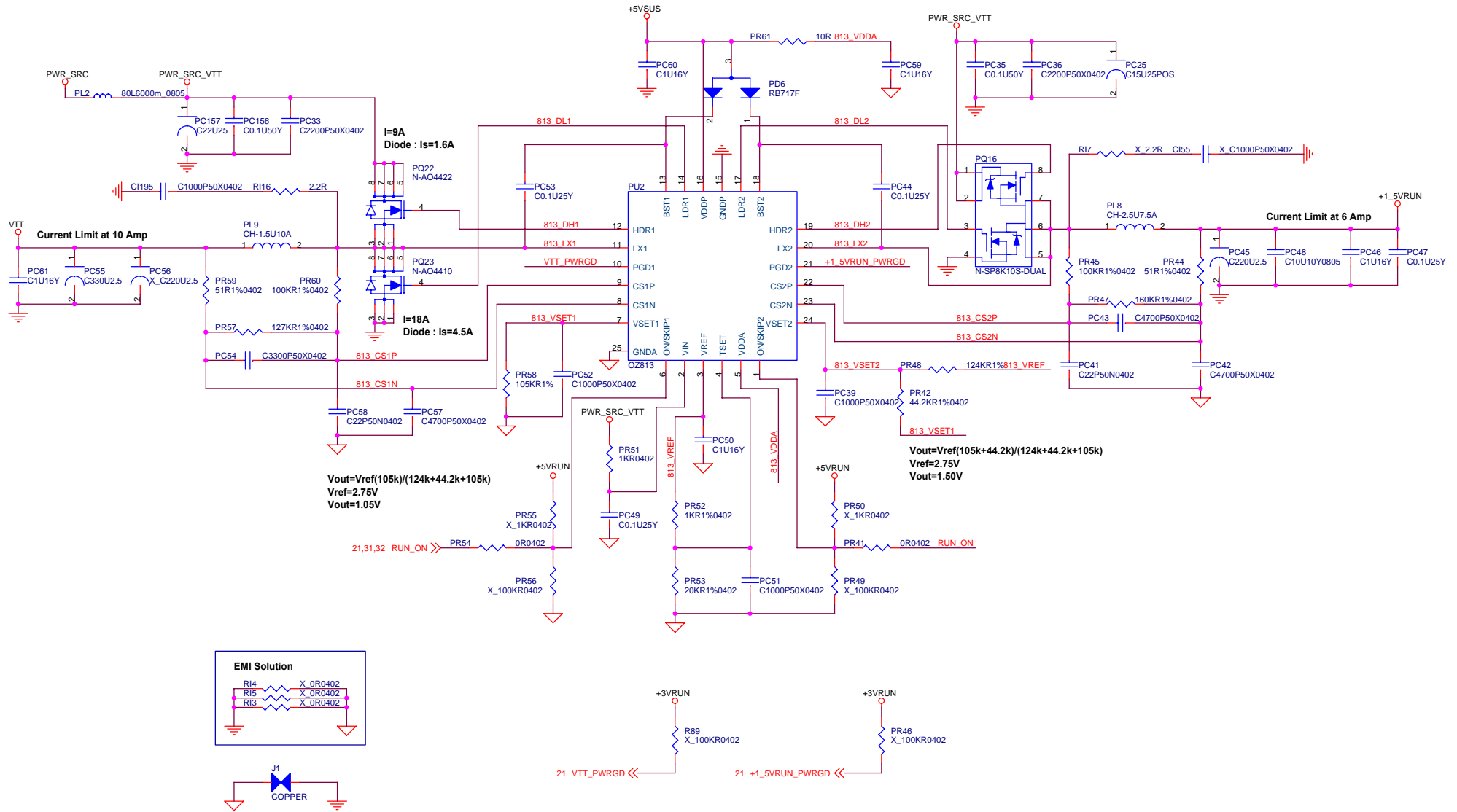
current limit
 $6A = (10\mu A \cdot PR3009) / R_{ds_on}(100C)$
 PR3009-16.9K
 Current limit at 6A



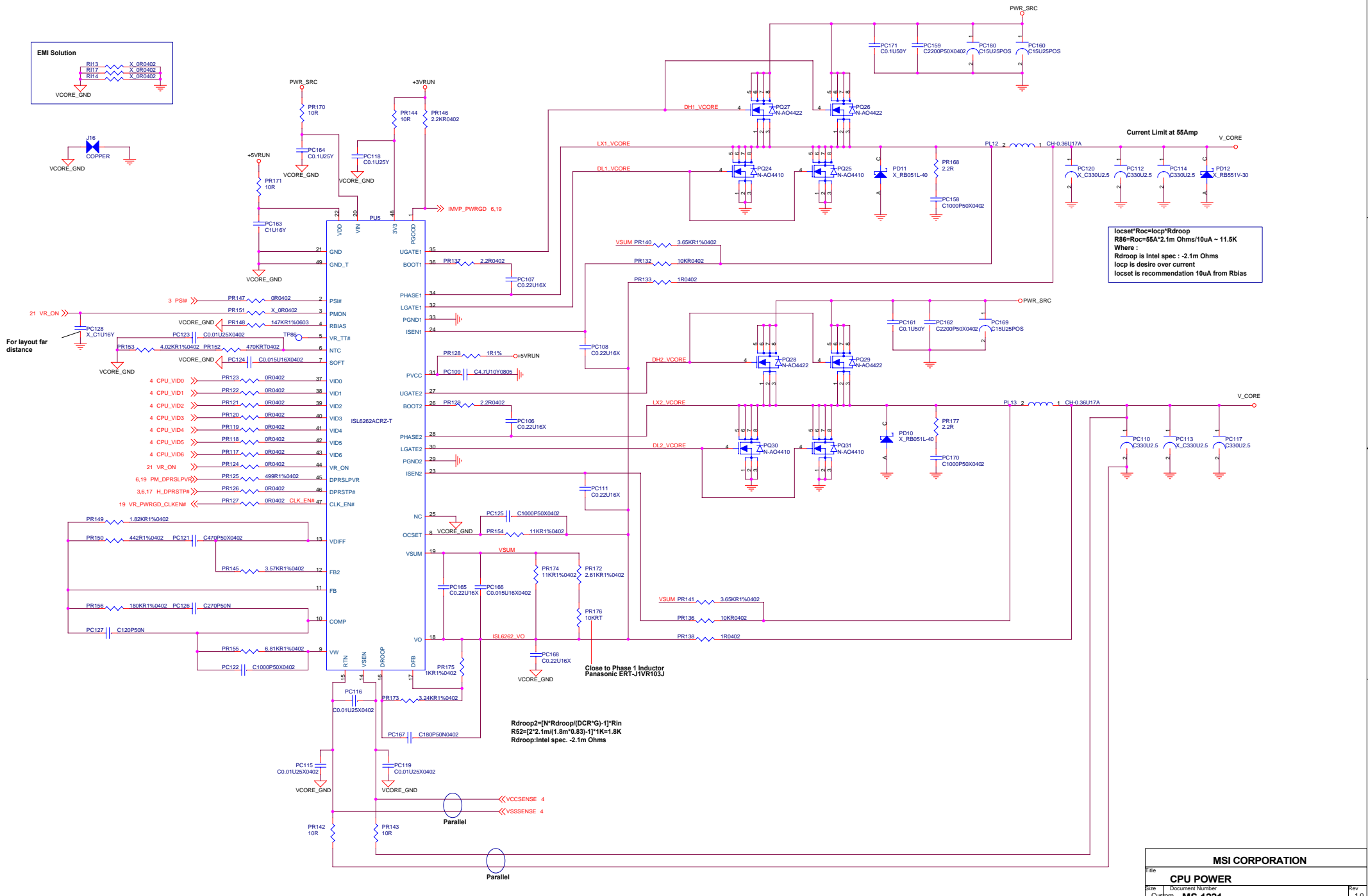
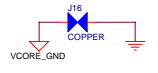
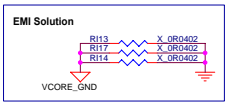
MSI CORPORATION		
Title		
SYSTEM POWER 3/5V		
Size	Document Number	Rev
Custom	MS-1221	1.0
Date:	Wednesday, March 14, 2007	Sheet 31 of 41



MSI CORPORATION			
Title			
DDR2 RAM POWER, +1.25V			
Size	Document Number	Rev	
Custom	MS-1221	1.0	
Date:	Wednesday, March 14, 2007	Sheet	32 of 41



MSI CORPORATION			
Title			
+1_5VRUN , VTT POWER			
Size	Document Number	Rev	
Custom	MS-1221	1.0	
Date:	Monday, April 02, 2007	Sheet	33 of 41



For layout far distance

Current Limit at 55Amp

$l_{ocset} \cdot R_{oc} = l_{ocp} \cdot R_{droop}$
 $R_{88} = R_{oc} = 55A \cdot 2.1m \text{ Ohms} / 10uA \sim 11.5K$
 Where :
 Rdroop is Intel spec : -2.1m Ohms
 locp is desire over current
 locset is recommendation 10uA from Rbias

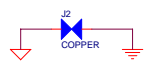
$R_{droop2} = [N \cdot R_{droop} (DCR \cdot G) - 1] \cdot R_{in}$
 $R_{S2} = [2 \cdot 2.1m (1.8m \cdot 0.83) - 1] \cdot 1K = 1.8K$
 Rdroop Intel spec : -2.1m Ohms

Close to Phase 1 Inductor
Panasonic ER1-J1VR103J

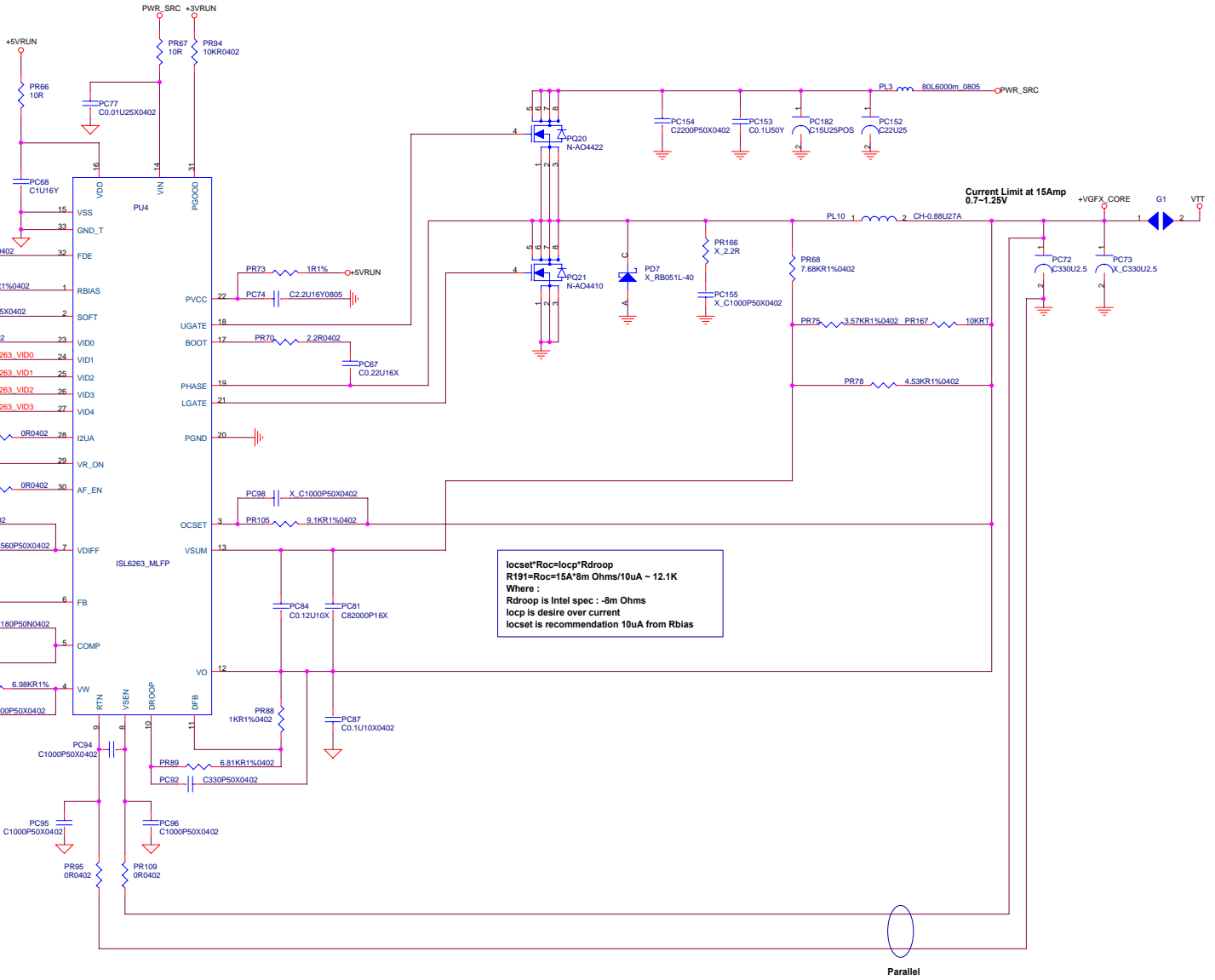
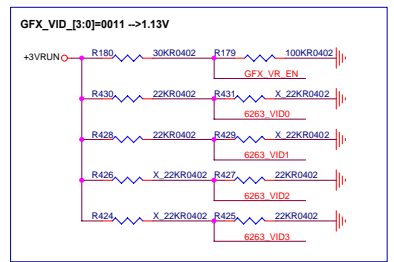
Parallel

Parallel

MSI CORPORATION			
Title			
CPU POWER			
Size	Document Number	Rev	
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FDE single high should be < 3.3V

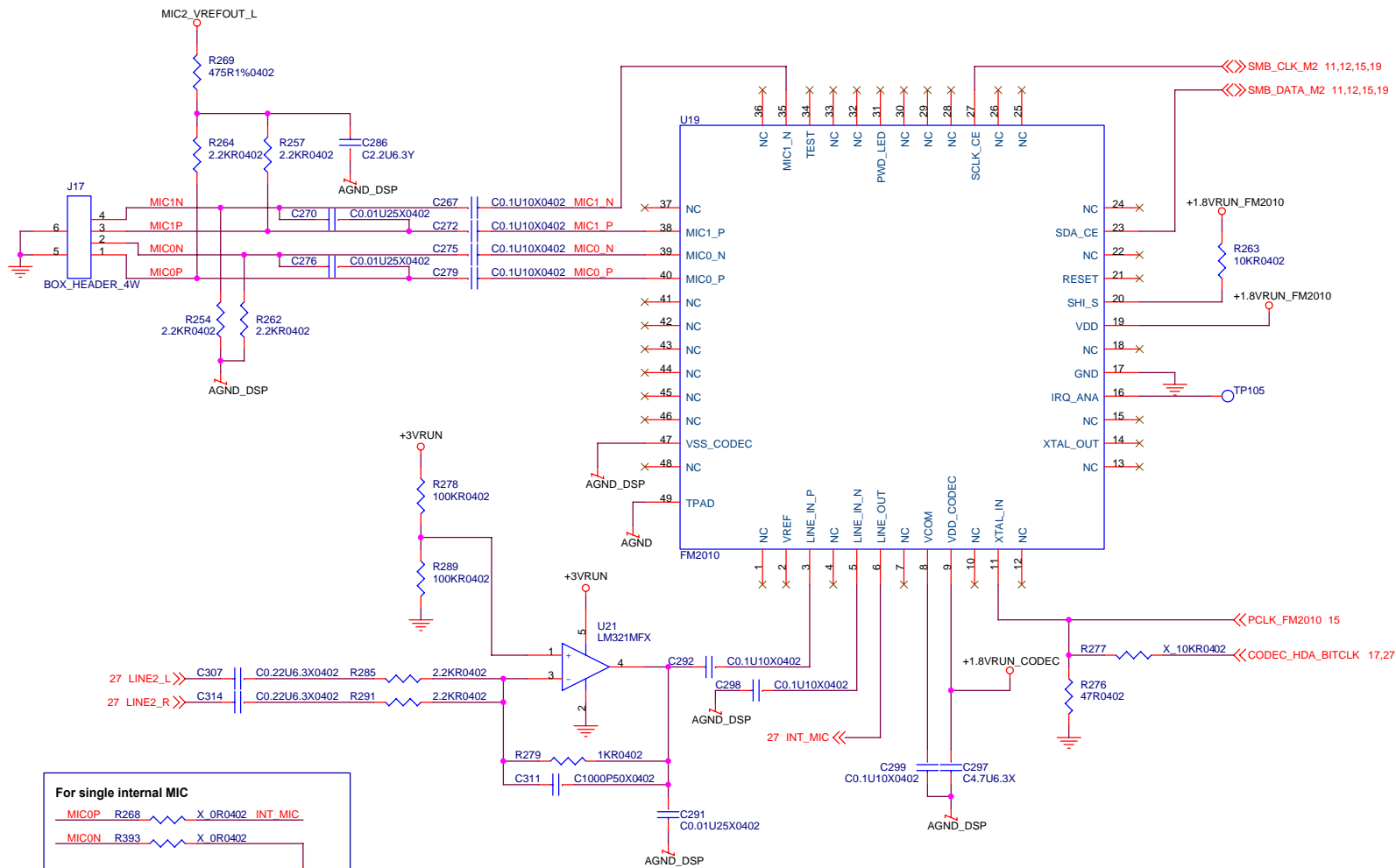


locset*Roc=locp*Rdroop
 $R191 = Roc = 15A * 8m\ Ohms / 10uA = 12.1K$
 Where :
 Rdroop is Intel spec : -8m Ohms
 locp is desire over current
 locset is recommendation 10uA from Rbias

Current Limit at 15Amp
 0.7-1.25V

Parallel

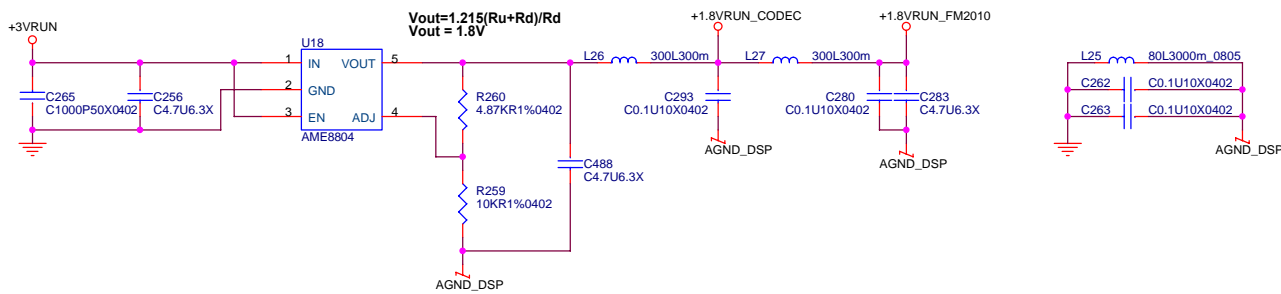
MSI CORPORATION			
File	Graphics Core		
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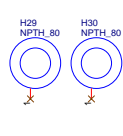
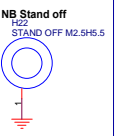
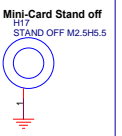
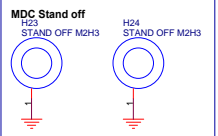
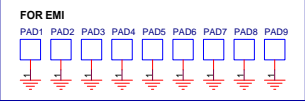
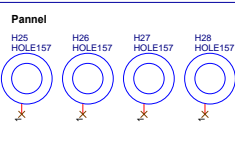
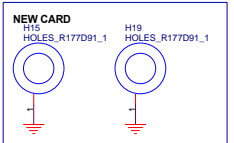
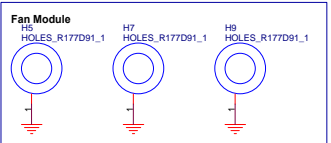
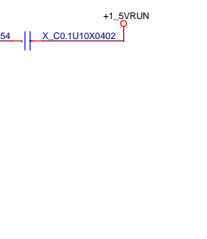
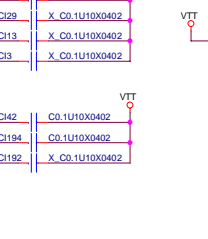
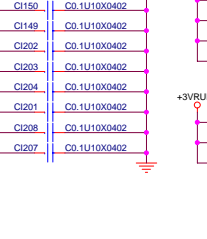
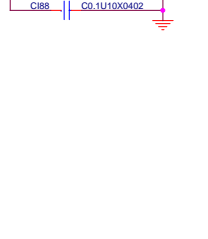
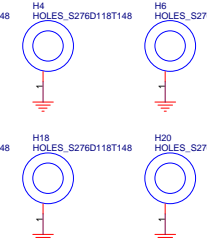
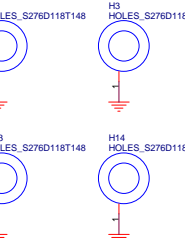
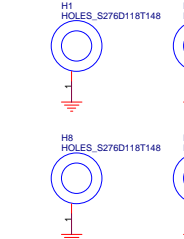
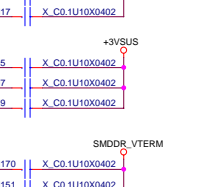
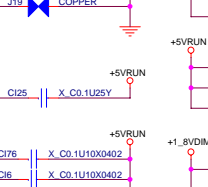
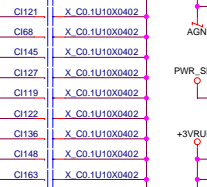
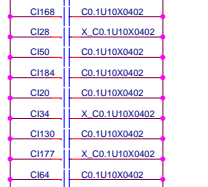
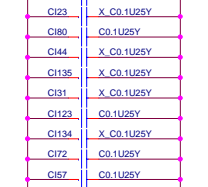
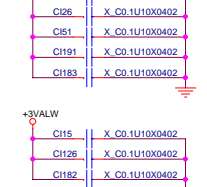
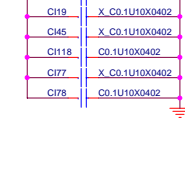
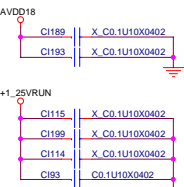
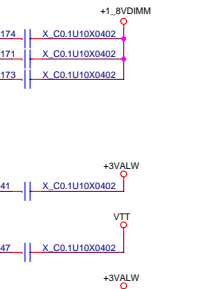
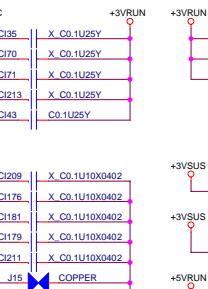
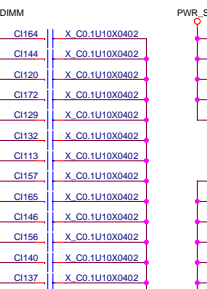
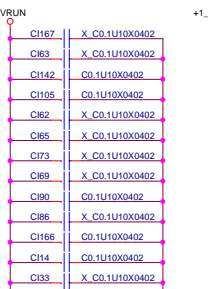
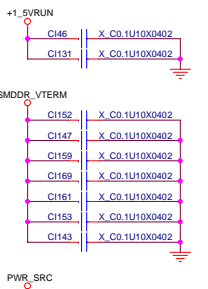
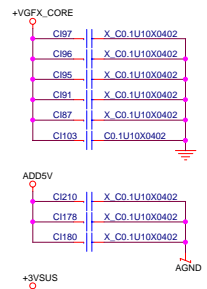
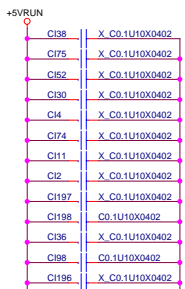
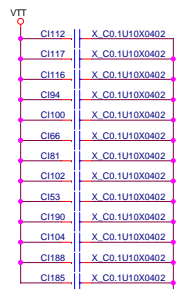
For single internal MIC

MIC0P R268 X 0R0402 INT_MIC
 MIC0N R393 X 0R0402

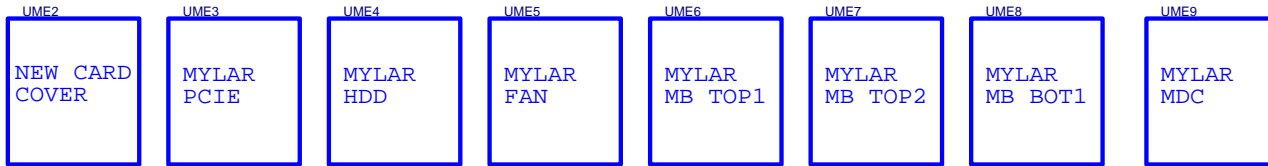
AGND_DSP



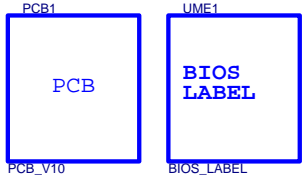
MSI CORPORATION		
Title		
Array Mic FM2010		
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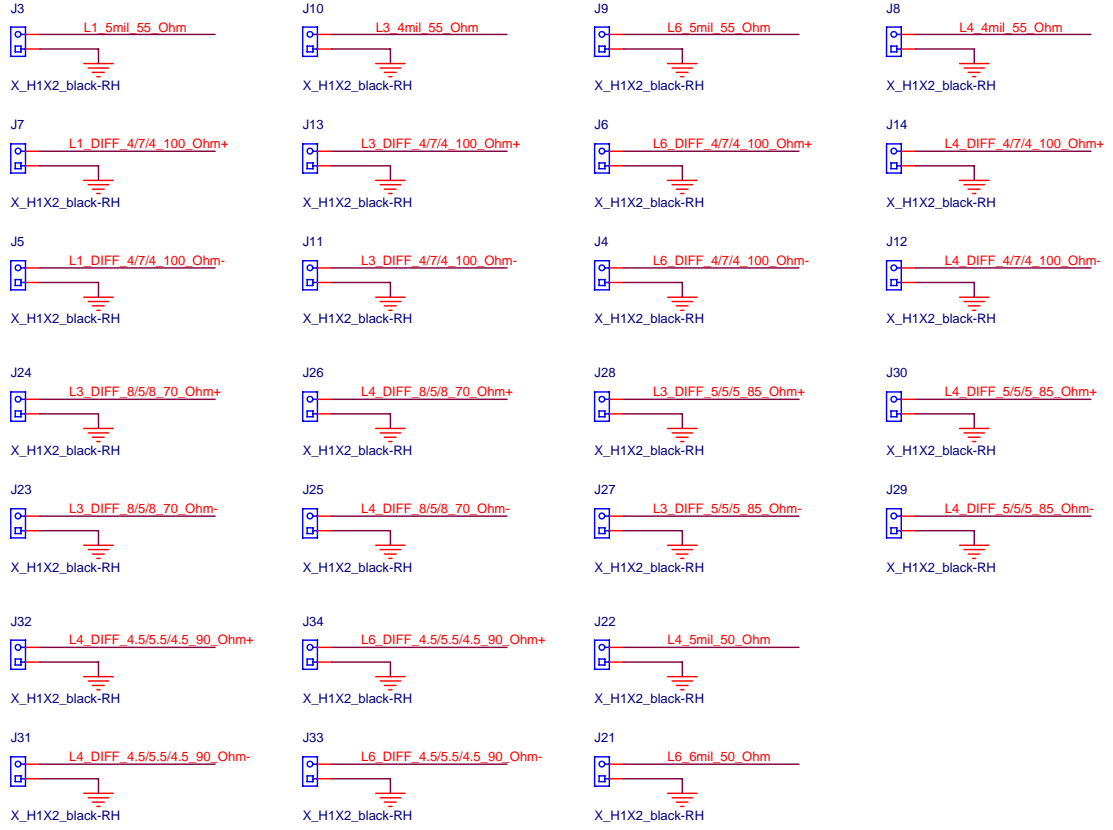
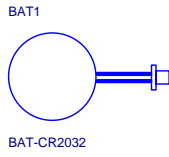
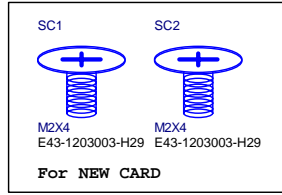
MSI CORPORATION		
File	Screw & EMI	
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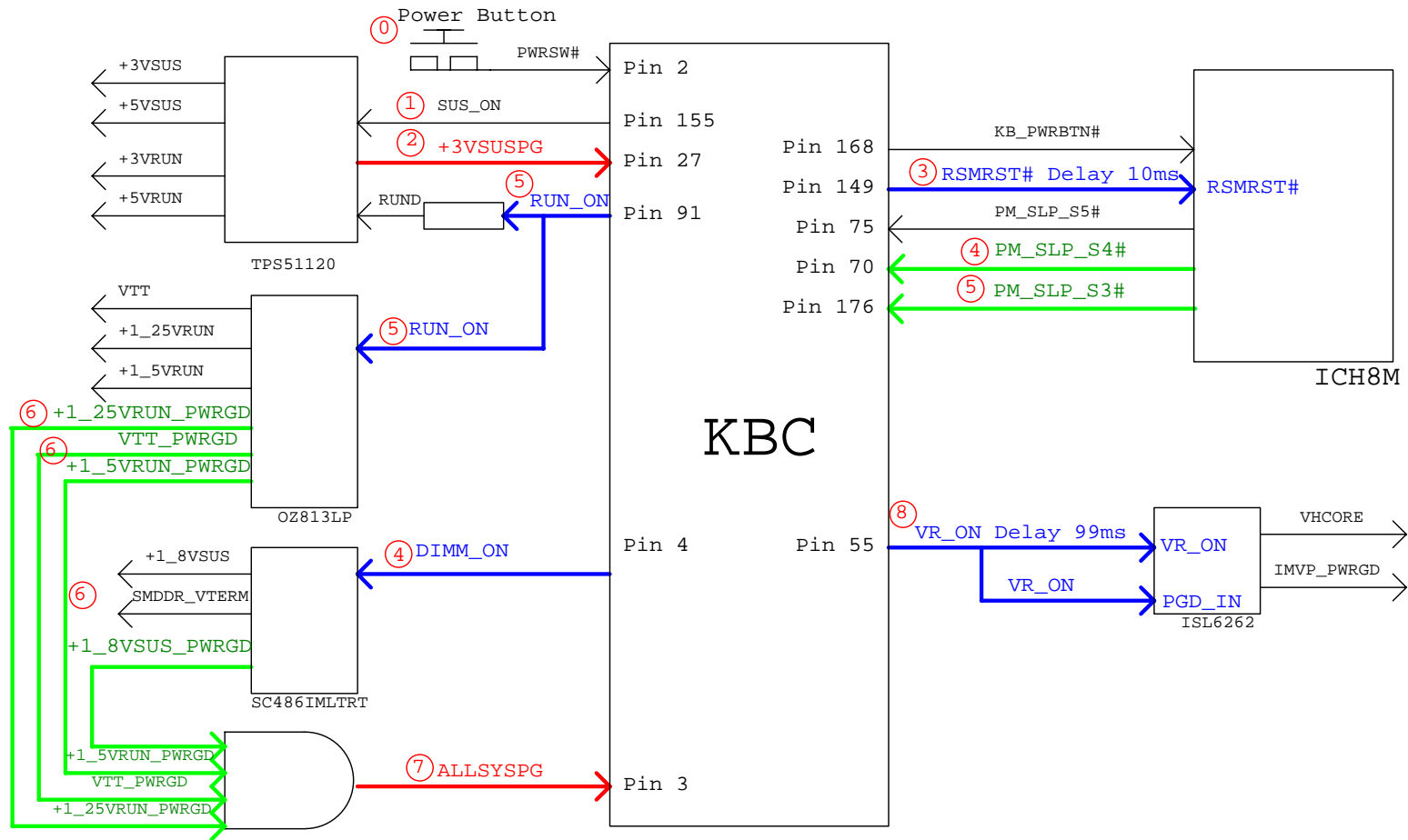
NEW CARD SHIELDING E2M-2210111-SH4
 MYLAR PCIE E2Y-2210211-G40
 MYLAR HDD E2Y-2210311-G40
 MYLAR FAN E2Y-2210411-G40
 MYLAR MB TOP1 E2P-2211611-G40
 MYLAR MB TOP2 E2P-2211711-G40
 MYLAR MB BOT1 E2P-2211511-G40
 MYLAR MDC E2P-2213211-G40



PCB_V10
 BIOS_LABEL
P30-1221110-T53,健鼎
P30-1221110-D05,昆穎
P30-1221110-Y34,元茂

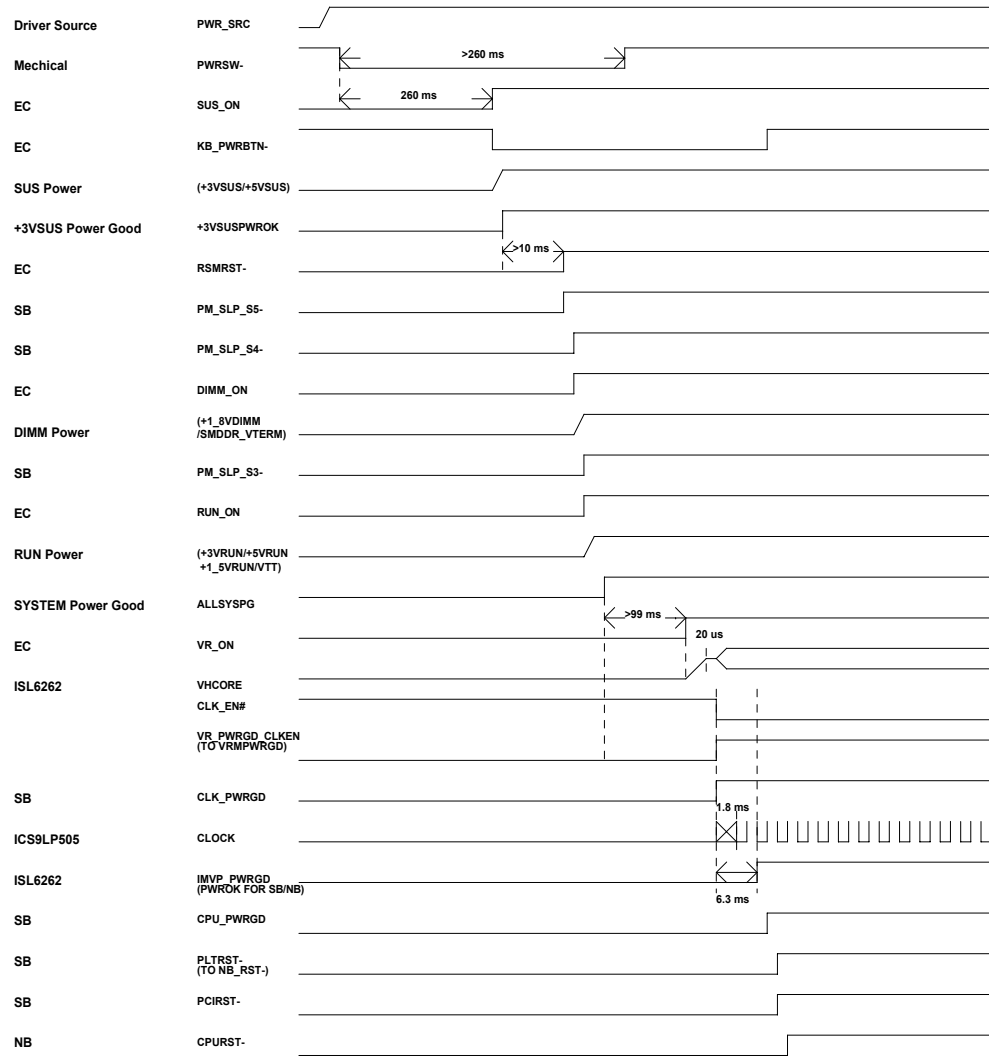


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Title		
Non-Footprint for BOM		
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B	MS-1221	1.0
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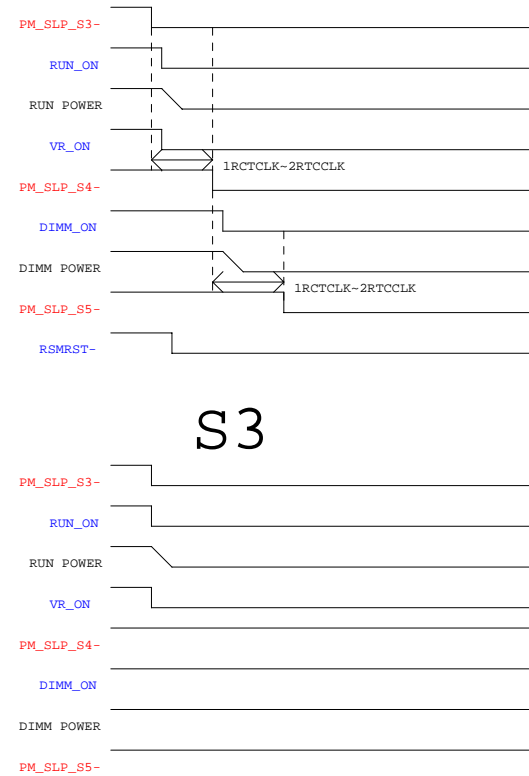


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Title		
KBC_CTR_PWR_BD		
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Power Up



Power Down



MS-1221 Revision: 0D

Rev	Date	Page	Description	Rev	Date	Page	Description
0A	2006/08/07		<ul style="list-style-type: none"> ● first version be released. 				
0B	2006/09/05		<ul style="list-style-type: none"> ● 2nd version be released. 				
0C	2006/10/24	- 34 -	<ul style="list-style-type: none"> ● change PR150 -1.4K to 442R,PR145 -2K to 3.57K ,PR156 -61.9K to 180K,PC126 -0.033U to 270p ,PC127 -390p to 120p,PR155 -4.42K to 6.81K ,PC122 -47p to 1000p,PR173 -3.6K to 3.24K ,PR154 -11.5K to 11K for load line and transient. 				
		- 35 -	<ul style="list-style-type: none"> ● change PR89 -6.04K to 6.81K,PR105 -12.1K to 9.1K for load line and transient. 				
		- 31 -	<ul style="list-style-type: none"> ● add PR187,PR188 -200K for decreasing Gate voltage of 2N7002DW. 				
	2006/10/31	- 27 -	<ul style="list-style-type: none"> ● change ALC883 to ALC888 chip. 				
		- 21 -	<ul style="list-style-type: none"> ● change R33 -100K to 4.7K for pulling up level of voltage. ● pop R38,RB13,RB5,RT3 and no-pop RB12,RB17 ● remove UT1 -BIOS socket. 				
		- 34 -	<ul style="list-style-type: none"> ● change PR146 -100K to 2.2K for pulling up level of voltage. 				
		- 06 -	<ul style="list-style-type: none"> ● change GFX_VID[3:0] H/W strap to adjustable setting. 				
		- 09 -	<ul style="list-style-type: none"> ● change L21 to R31 -100R and add C492 -1uF to eliminate CRT/TV noise. 				
		- 15 -	<ul style="list-style-type: none"> ● change ICS9LP505 to SLG8SP512. 				
		- 36 -	<ul style="list-style-type: none"> ● change R276 -10K to 47R and no-pop R277, connect CLK_IN of FM2010 from PCI clock to fix FM2010 no function. 				
		- 16 -	<ul style="list-style-type: none"> ● add R34 for DDC power. 				
	2006/11/03	- 23 -	<ul style="list-style-type: none"> ● no-pop R10,CT1,CT3,CT9,CT12. 				
		- 22 -	<ul style="list-style-type: none"> ● change EC1,EC2,C36 to 100uF POS Cap for ME height limitation. ● change USB3 to SMT type for ME height limitation. 				
		- 25 -	<ul style="list-style-type: none"> ● change J20 to new SIM card for ME request. 				
		- 21 -	<ul style="list-style-type: none"> ● change CON1 to R/A type for ME request. 				
		- 14 -	<ul style="list-style-type: none"> ● change U11 -Sil1390 to Sil1392 chip. 				
	2006/11/06	- 26 -	<ul style="list-style-type: none"> ● change CON8 to another P/N. 				
	2006/11/13	- 26 -	<ul style="list-style-type: none"> ● add RT5, pop R177,R178,Q13,Q14 for Cap Sense Launch board. 				
		- 11 -	<ul style="list-style-type: none"> ● add DDR2 thermal sensor circuit. 				
		- 22 -	<ul style="list-style-type: none"> ● remove CIR circuit. 				
		- 21 -	<ul style="list-style-type: none"> ● define pin-30 of UB1 to be as HOT_START_K- function. (Vista Hot Start) 				
	2006/11/20	- 09 -	<ul style="list-style-type: none"> ● pop D3,R210. 				
		- 19 -	<ul style="list-style-type: none"> ● no-pop R92,R106,R340,R129,R312,R329,R70 and pop DB6. 				
		- 21 -	<ul style="list-style-type: none"> ● no-pop UT1,CT4 and pop U50,CT43 for 8M FLASH. 				
0D	2006/12/27~ 2007/1/10	- 03 -	<ul style="list-style-type: none"> ● Change HW thermal shunt down circuit 				
		- 13 -	<ul style="list-style-type: none"> ● Change RNT1, RNT2, RNT3 trace connect 				
		- 15 -	<ul style="list-style-type: none"> ● Add C498 for EMI 				
		- 21 -	<ul style="list-style-type: none"> ● Change RB6, RT6, R23 pull-high from 100K to 10K 				
		- 25 -	<ul style="list-style-type: none"> ● Change R292, R293, R414, R415, R416 from 220R to 180R ● Change LED6 from D0C-0400500-L05 to D0C-0403520-L05 ● Change LED7 from D0C-0401000-R06 to LED7: D0C-0403520-L05 to LED9: D0C-0403000-E07 ● Change LED8 from D0C-0403000-L05 to D0C-0403520-L05 				
		- 32 -	<ul style="list-style-type: none"> ● Change PR185 from 10K to 11.5K to improve DIMM power 				
		- 34 -	<ul style="list-style-type: none"> ● SWAP PQ24, PQ25, PQ26, PQ27, PR168, PC158 with PQ28, PQ29, PQ30, PQ31, PR177, PC170 				
		- 37 -	<ul style="list-style-type: none"> ● Change footprint H5, H7, H9, H15, H19 from mask to non-mask for SMT DFM request ● Change H10 footprint for SMT DFM request ● Change H17 from Top to Bottom ● Add CI213 for EMI request 				

MSI CORPORATION			
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Change History			
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