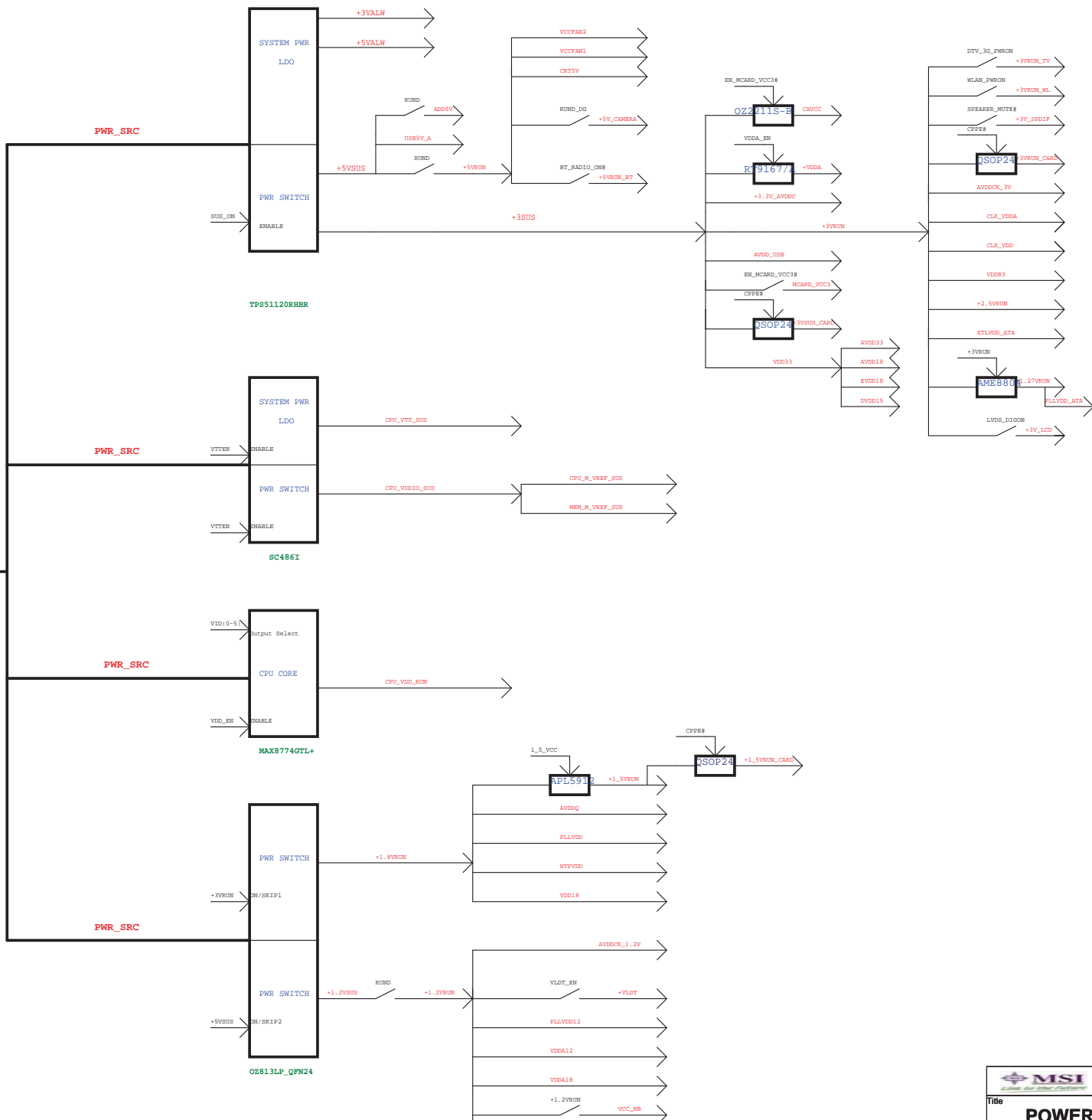

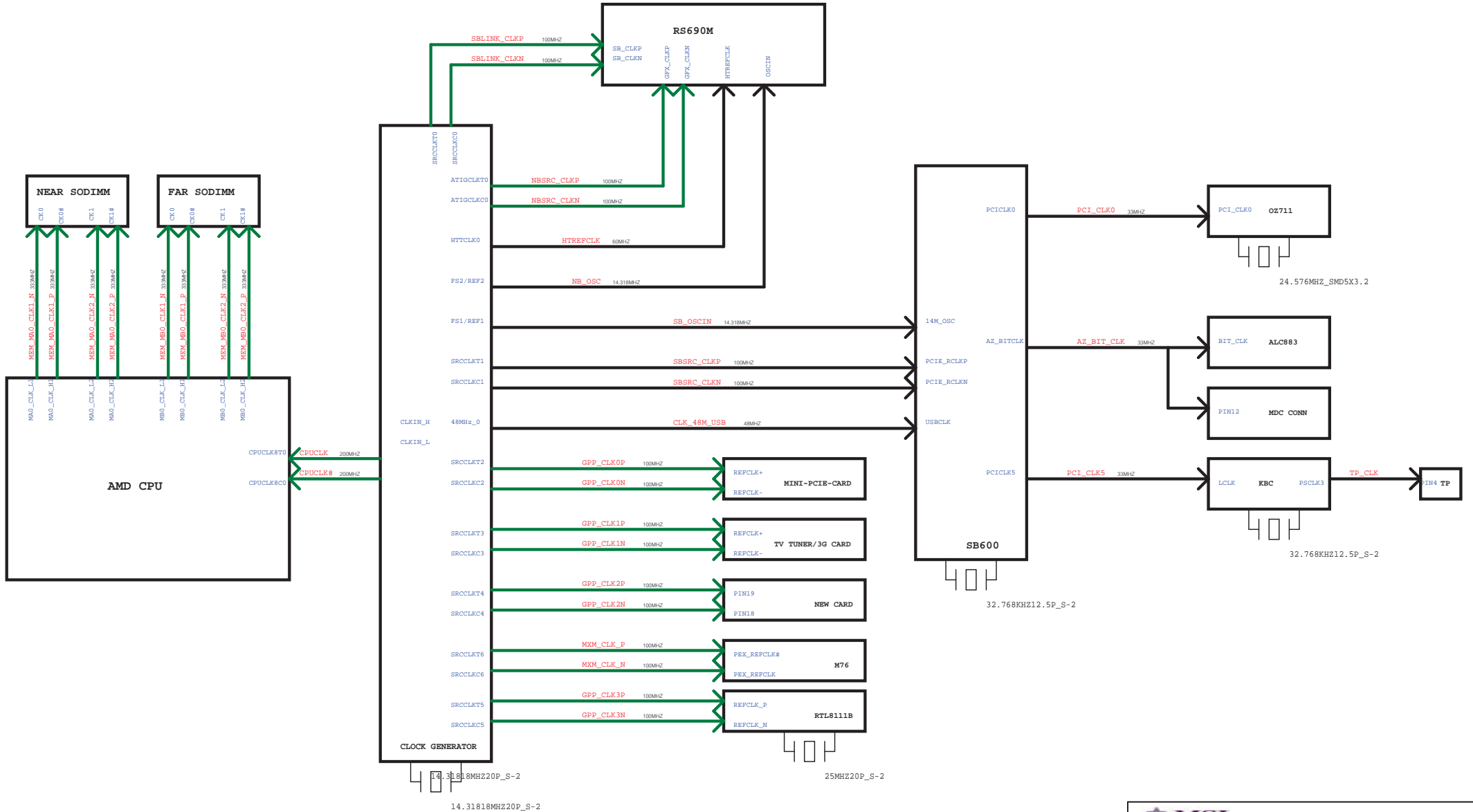



ADAPTER & BATTERY



<http://hobi-elektronika.net>

 MICRO-STAR INT'L CO.,LTD.	
POWER DELIVERY CHART	
Size	Document Number
Custom	MS-171A1
Date:	Friday, September 14, 2007
Sheet	2 of 48
Rev	10

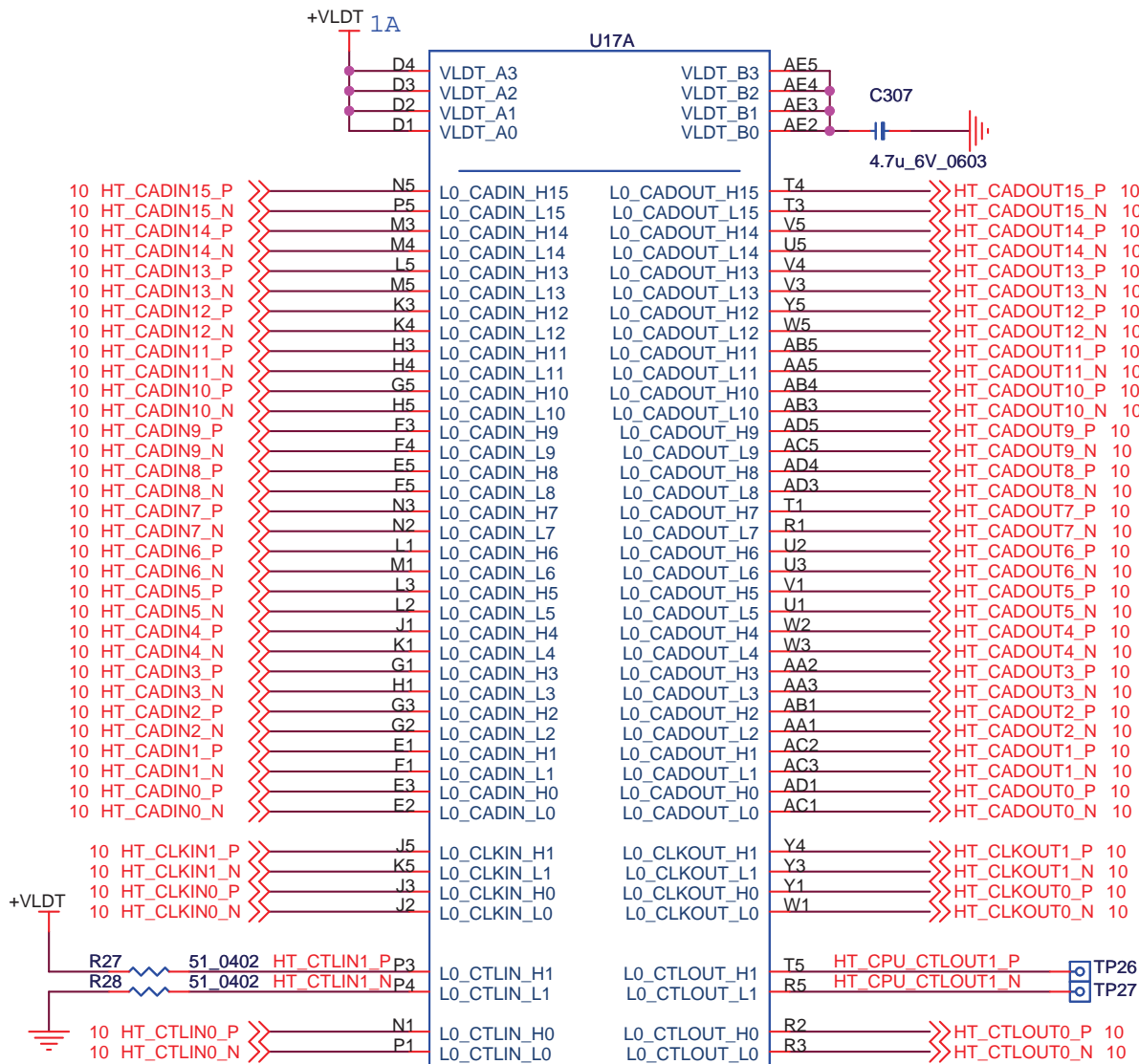


 MICRO-STAR INT'L CO.,LTD.	
Title CLOCK DISTRIBUTION	
Size B	Document Number MS-171A1
Date: Friday, September 14, 2007	Rev 10
Sheet 3	of 48

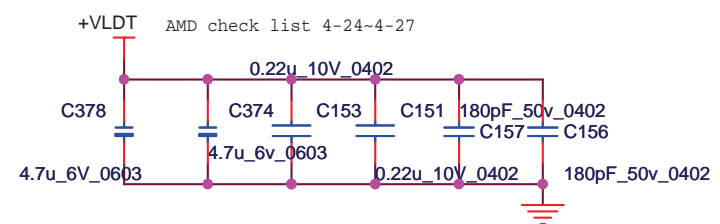


PROCESSOR HYPERTRANSPORT INTERFACE


VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor
Socket

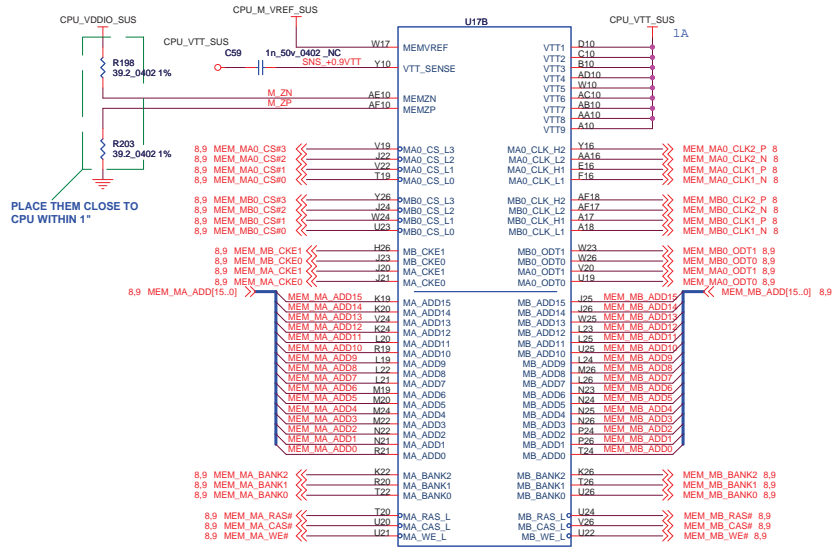


LAYOUT: Place bypass cap on topside of board
 NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDT0 POWER PINS

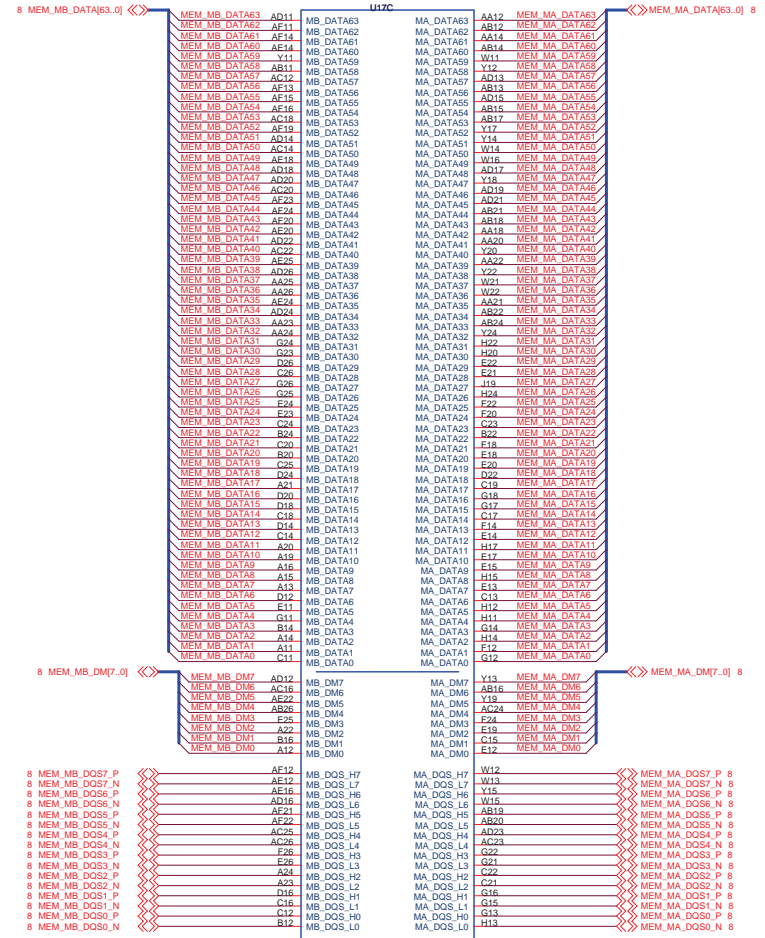
 Link to the Future		MICRO-STAR INT'L CO.,LTD.	
Title			
SOCKET S1 HT I/F			
Size	Document Number		Rev
Custom	MS-171A1		10
Date:	Friday, September 14, 2007	Sheet	4 of 48

Processor DDR2 Memory Interface

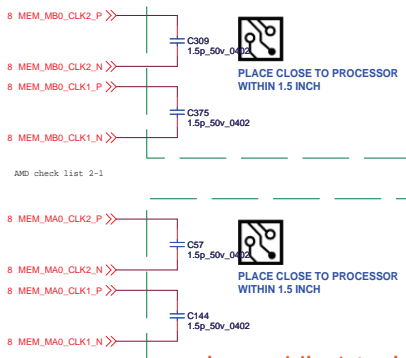
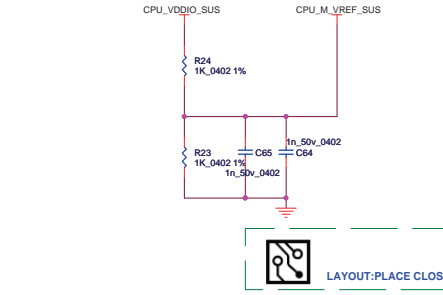
VDD VTT SUS_CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE.



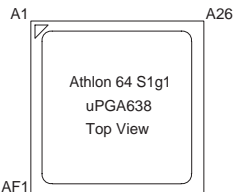
PLACE THEM CLOSE TO CPU WITHIN 1"



VDD_VREF_SUS_CPU



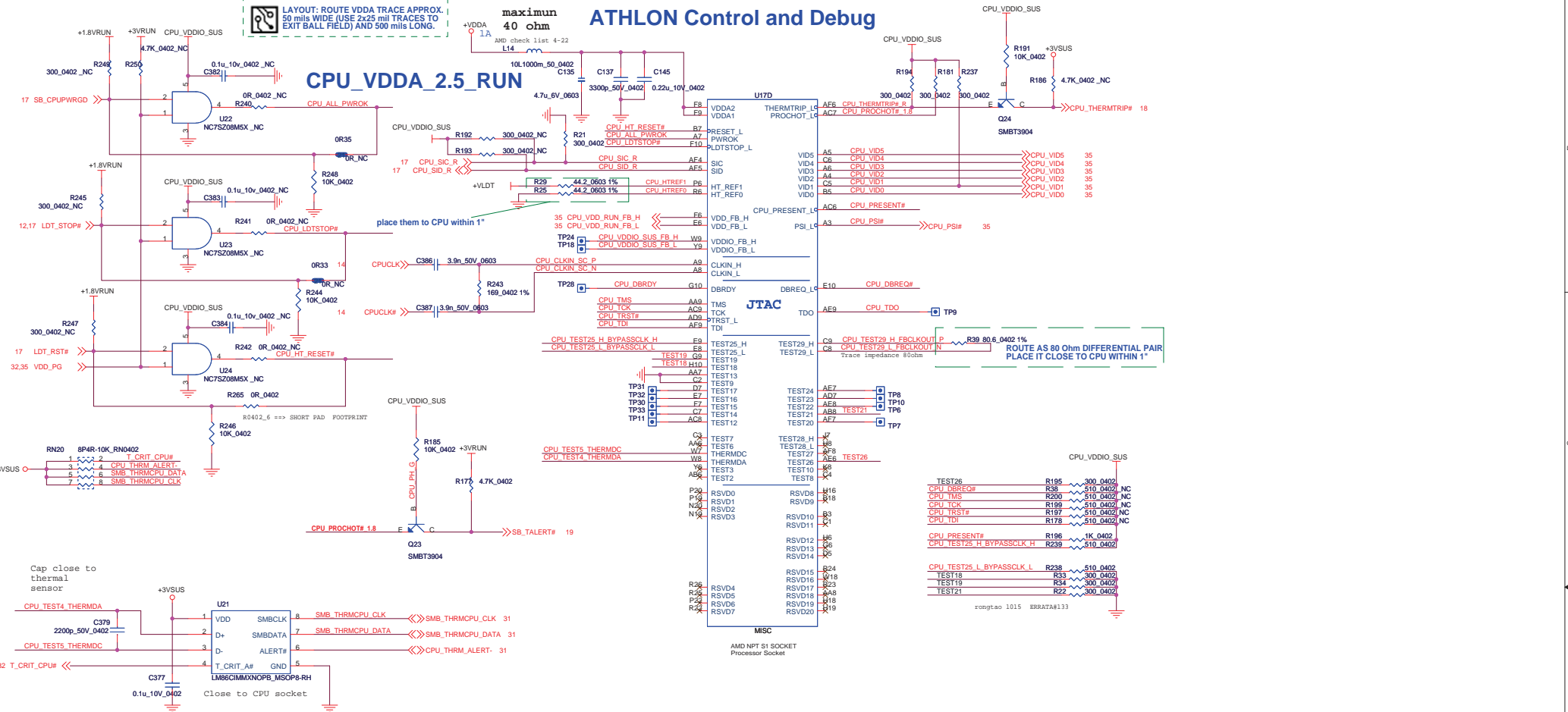
<http://hobi-elektronika.net>



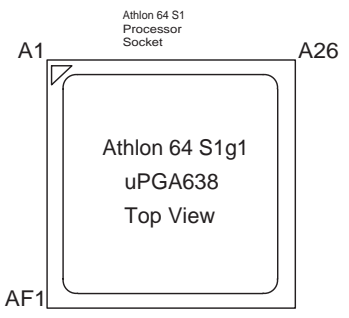
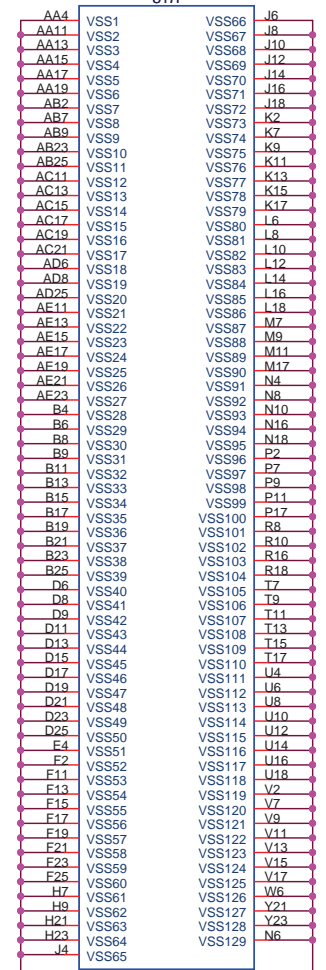
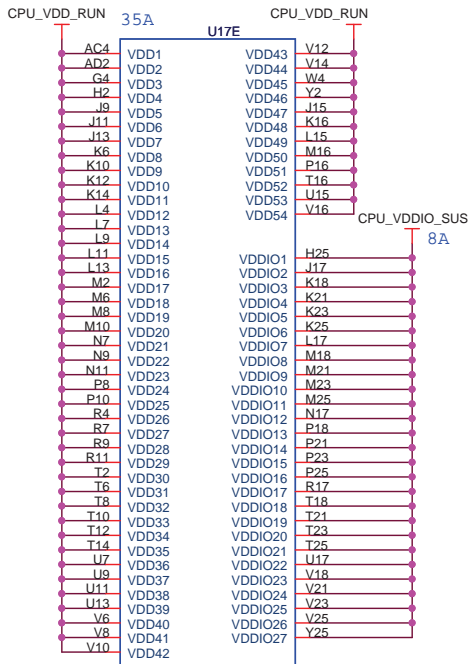
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

ATHLON Control and Debug

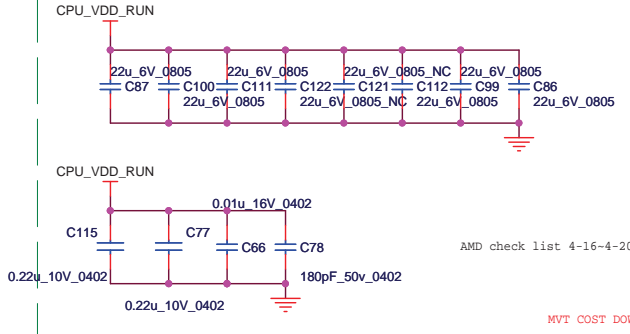
CPU_VDDA_2.5_RUN



<http://hobi-elektronika.net>

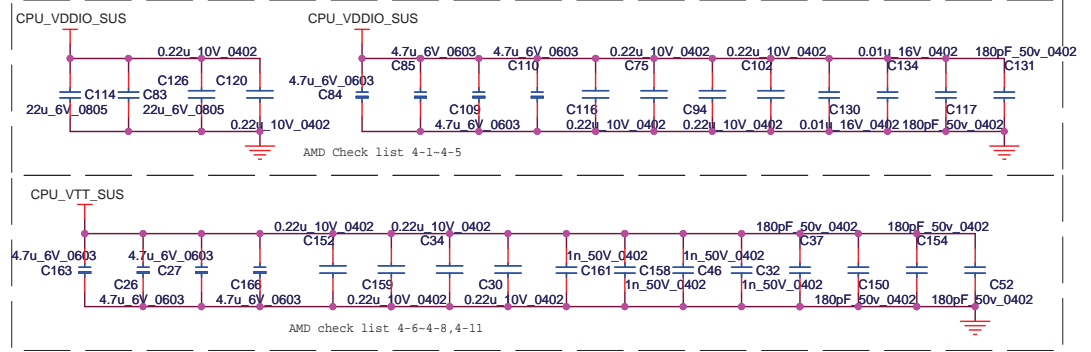


BOTTOMSIDE DECOUPLING



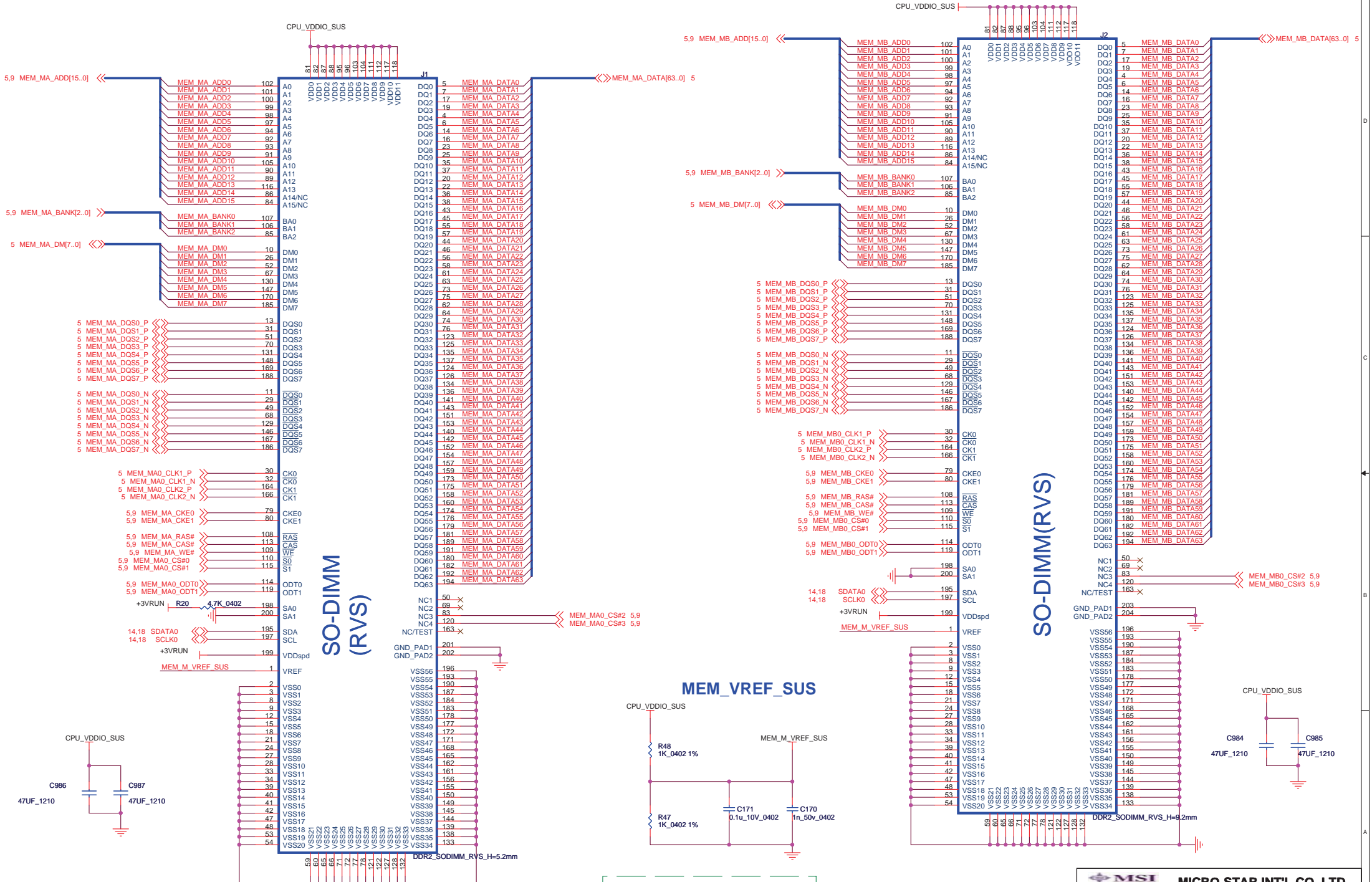
DECOUPLING BETWEEN PROCESSOR AND DIMMs

PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND

		MICRO-STAR INT'L CO.,LTD.	
Title			
SOCKET S1 PWR & GND			
Size	Document Number		Rev
B	MS-171A1		10
Date:	Friday, September 14, 2007	Sheet	7 of 48



LAYOUT: PLACE CLOSE TO DIMMS

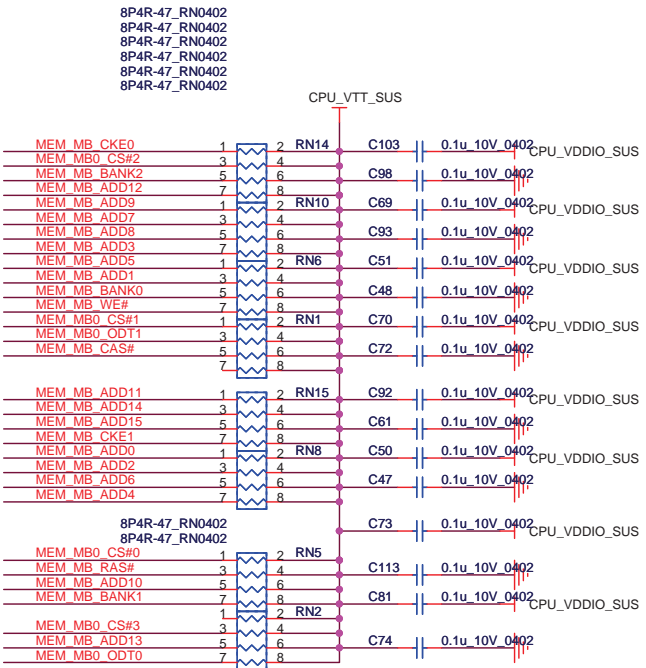
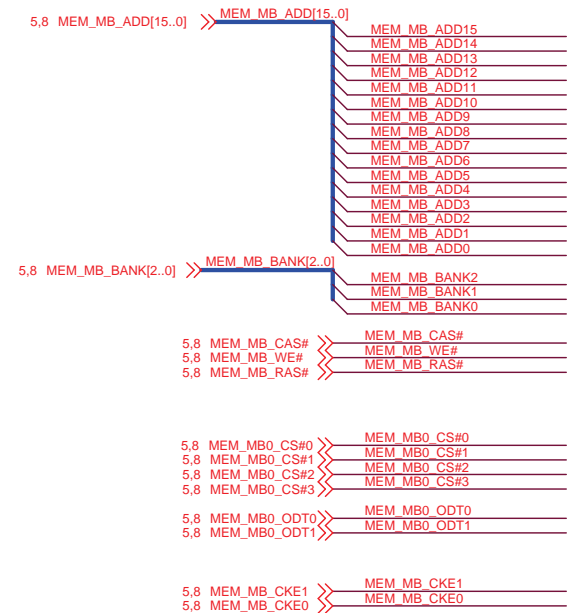
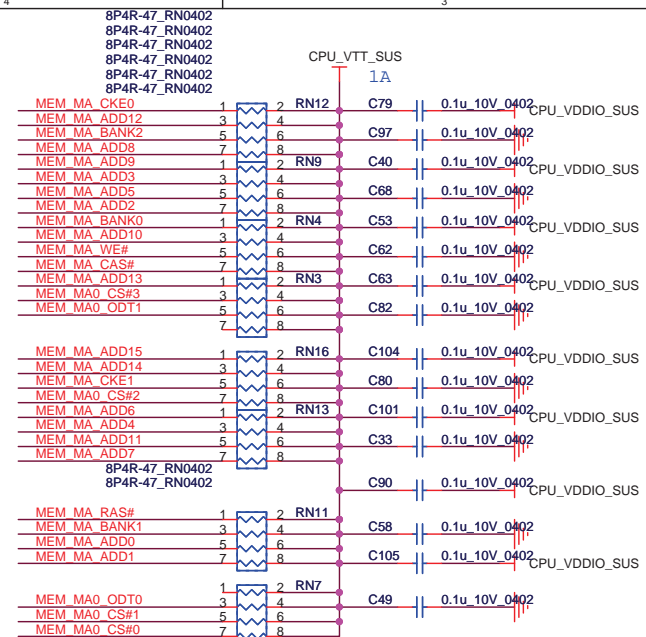
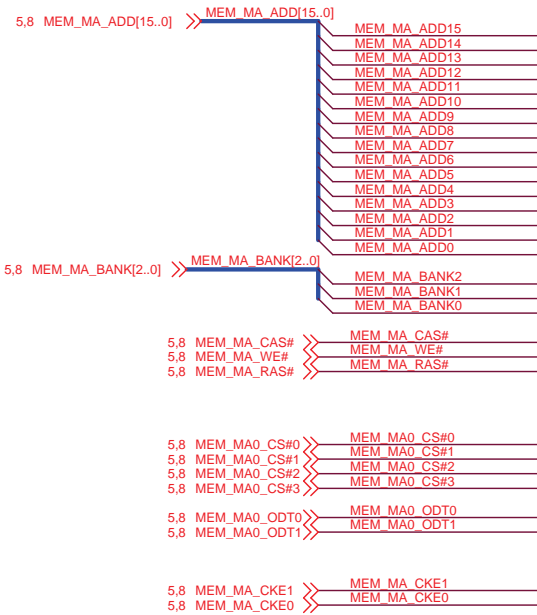
<http://hobi-elektronika.net>

MSI MICRO-STAR INT'L CO.,LTD.

Title: **DDR2 SODIMMS A/B CHANNEL**

Size: Custom Document Number: **MS-171A1** Rev: 10

Date: Friday, September 14, 2007 Sheet: 8 of 48

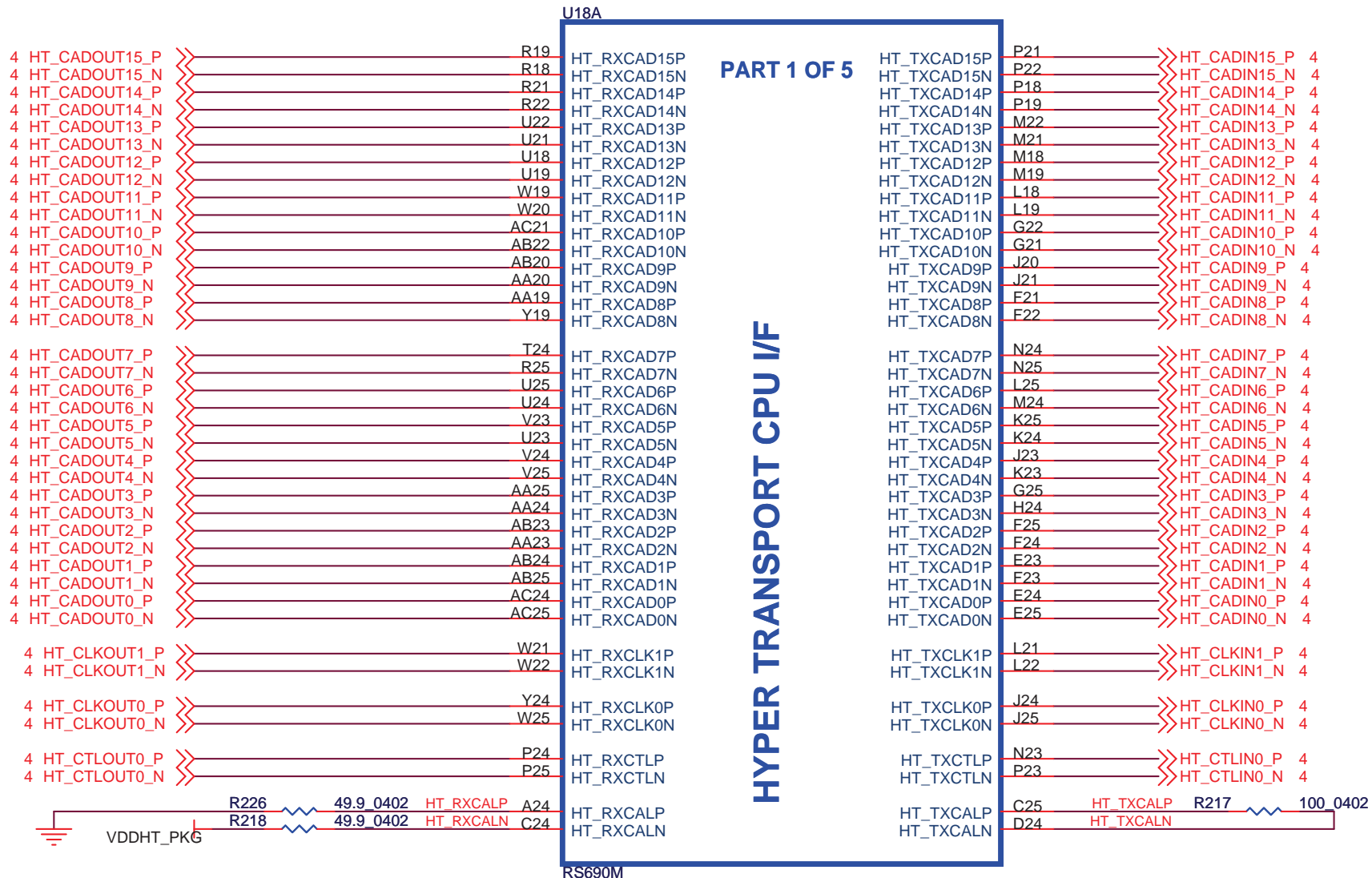


MSI MICRO-STAR INT'L CO.,LTD.


Title: **DDR2 SODIMMS TERMINATIONS**

Size: Custom Document Number: **MS-171A1** Rev: 10

Date: Friday, September 14, 2007 Sheet: 9 of 48



<http://hobi-elektronika.net>

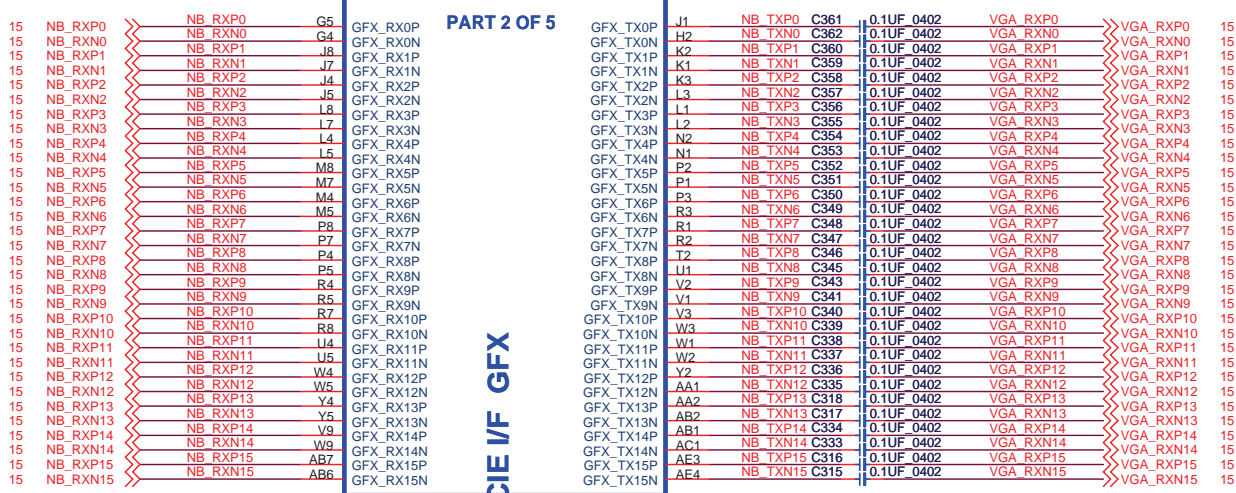
 MICRO-STAR INT'L CO.,LTD.	
Title	
RS690M HT LINK I/F	
Size	Document Number
A	MS-171A1
Date:	Friday, September 14, 2007
Sheet	10 of 48
Rev	10

NB_RXN[0..15] << NB_RXN[0..15] 15 VGA_RXP[0..15] >> VGA_RXP[0..15] 15
 NB_RXP[0..15] << NB_RXP[0..15] 15 VGA_RXN[0..15] >> VGA_RXN[0..15] 15

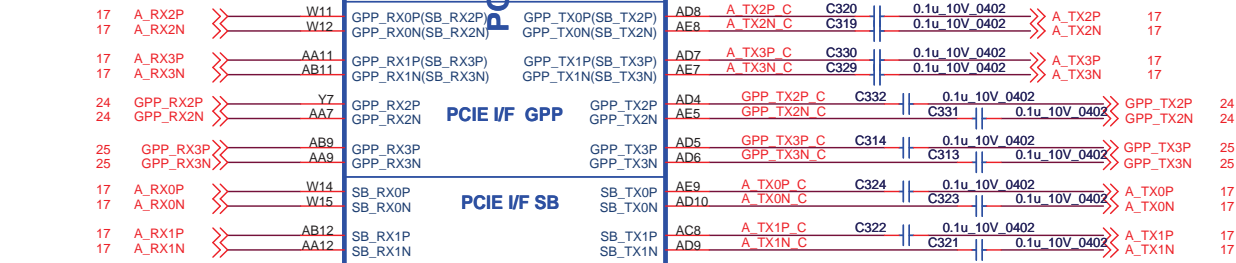
version A12

U18B

PART 2 OF 5



PCIE I/F GFX




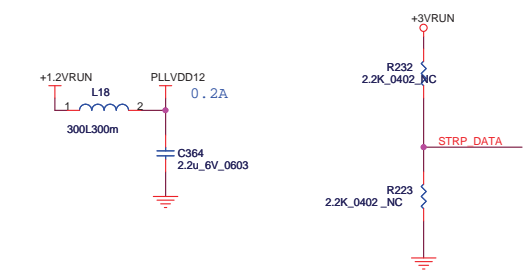
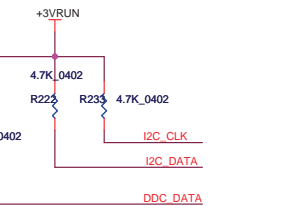
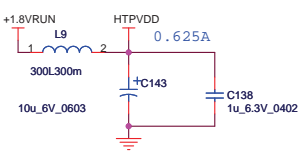
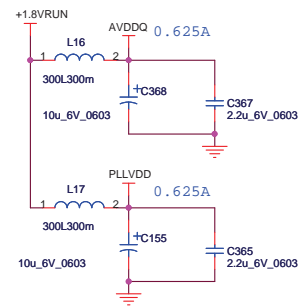
PCIE I/F SB



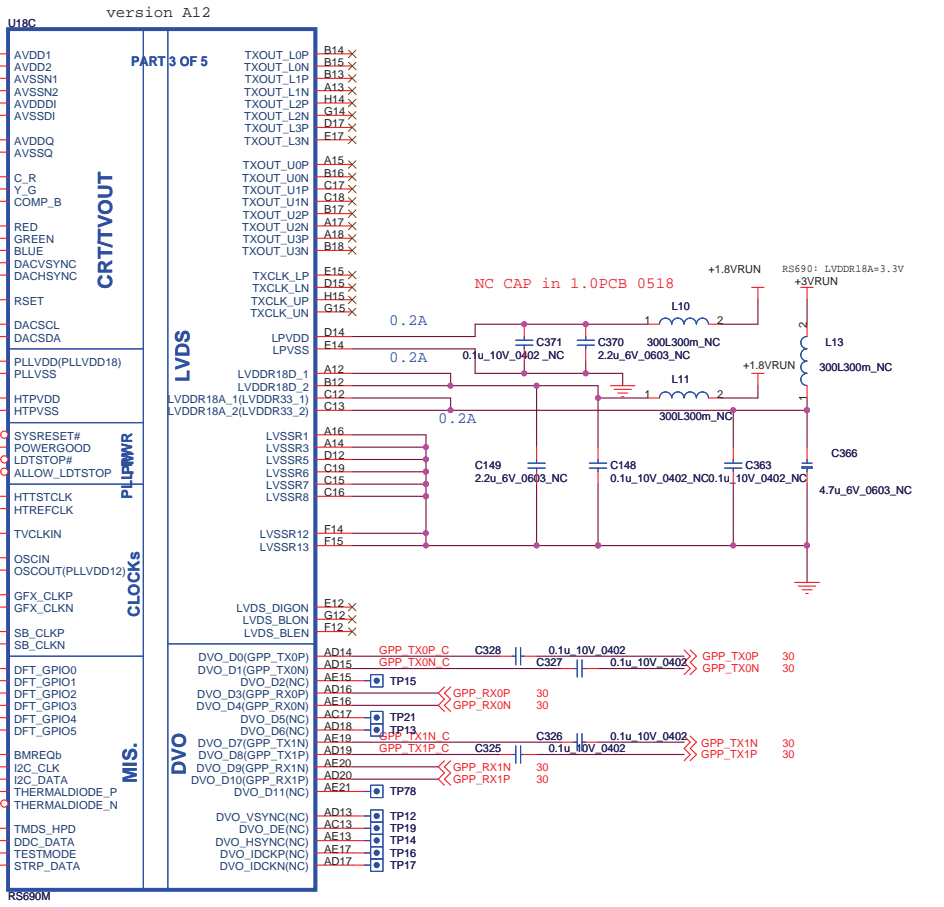
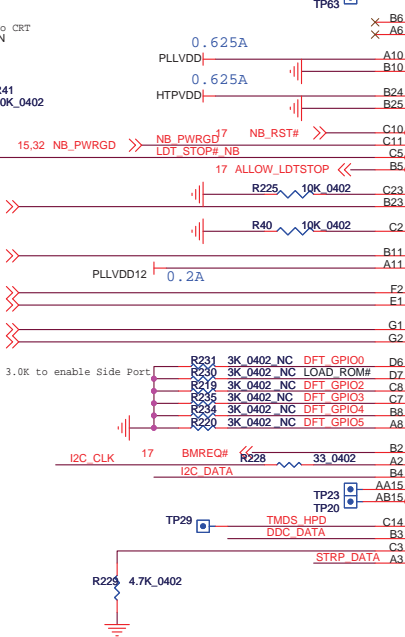
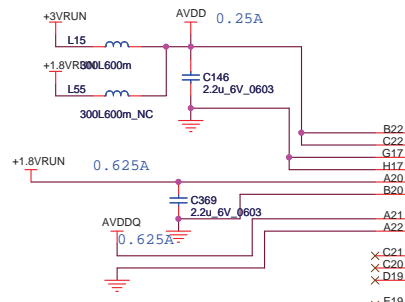
RS690M

R50 5620hm
R52 2K0hm

		MICRO-STAR INT'L CO.,LTD.	
Title			
RS690T PCI-E LINK&HDMI I/F			
Size	Document Number	Rev	
B	MS-171A1	10	
Date:	Friday, September 14, 2007	Sheet	11 of 48



FOR RS690M : +3VRUN
 FOR RX690 : +1.8VRUN
 change to +3VRUN for AMD recommend 0308



	RS485/RS690	RS690 only (NC for RS485)		
	DFT_GPIO1	DFT_GPIO0	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Bypass the loading of EEPROM straps and use Hardware default values DEFAULT	Memory side port not available DEFAULT	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) DEFAULT 110: 4-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1 Config D 010: 4-1-1-1-1 Config E others: register defined (register default to Config E)	Enable debug bus via the memory I/O pads, if available in the package use default values DEFAULT
PULL LOW	I2C Master can load strap values from EEPROM if connected, or use default values if not connected	Memory side port available		use the memory data bus to output the debug bus

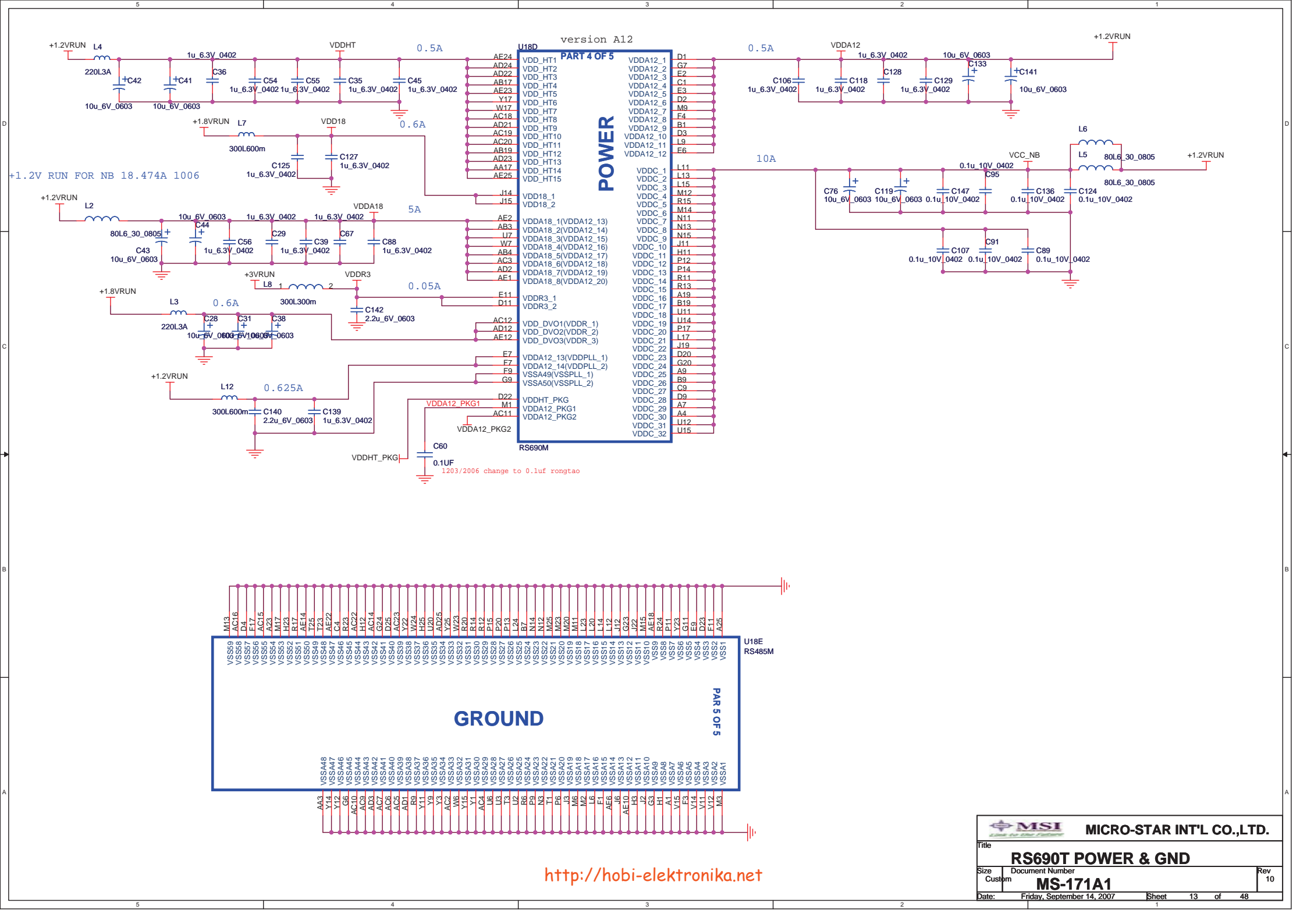
LOAD_ROM#: LOAD ROM STRAP ENABLE
 High, LOAD ROM STRAP DISABLE
 Low, LOAD ROM STRAP ENABLE

MSI MICRO-STAR INT'L CO.,LTD.

Title: **RS690T SYSTEM I/F&CLK**

Size: Document Number
 Custom: **MS-171A1** Rev 10

Date: Friday, September 14, 2007 Sheet 12 of 48



version A12


PART 4 OF 5

POWER

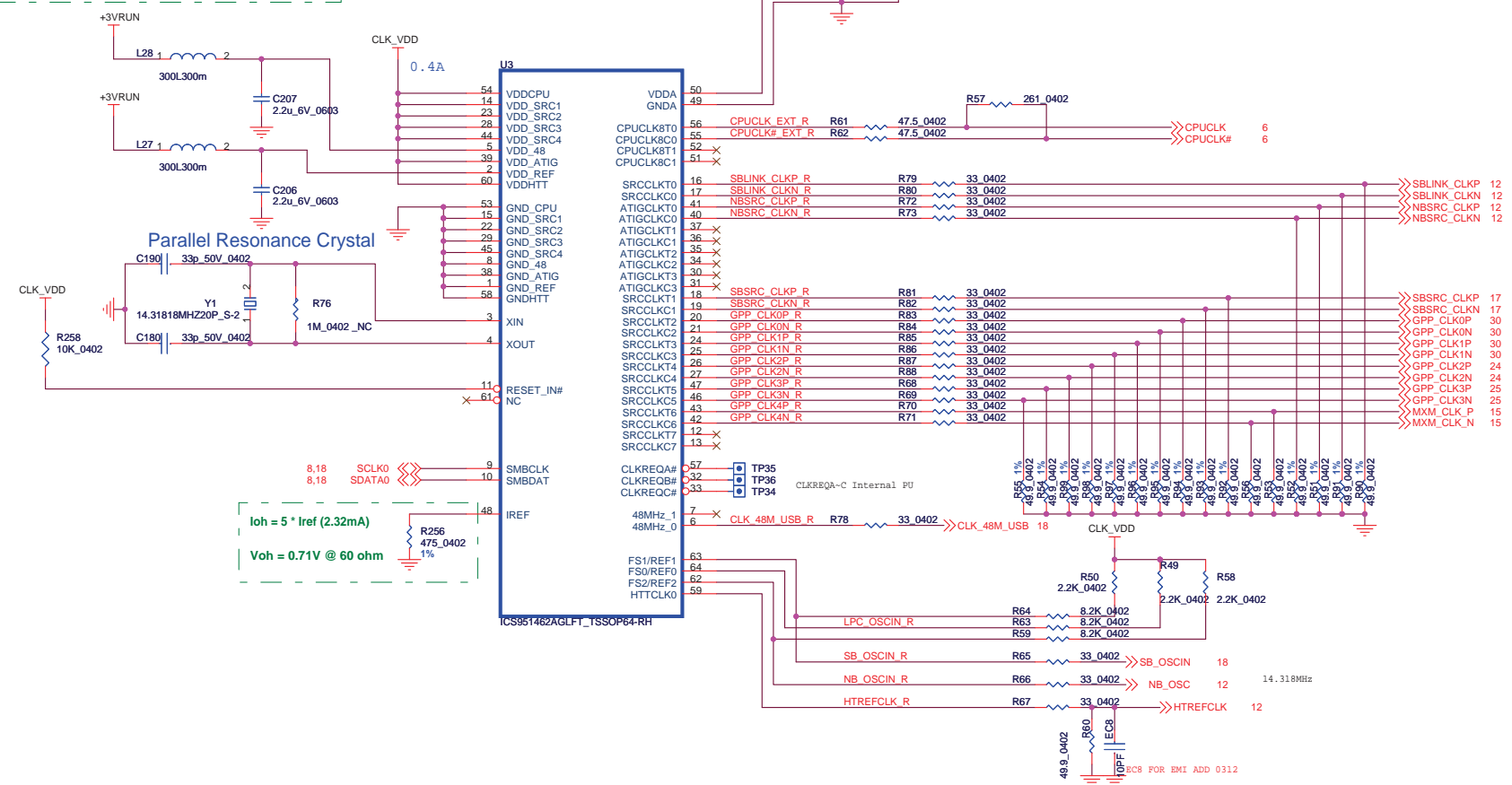
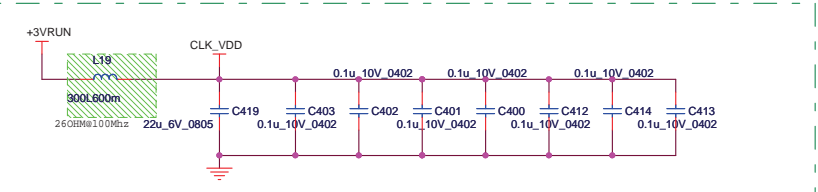
GROUND

PART 4 OF 5

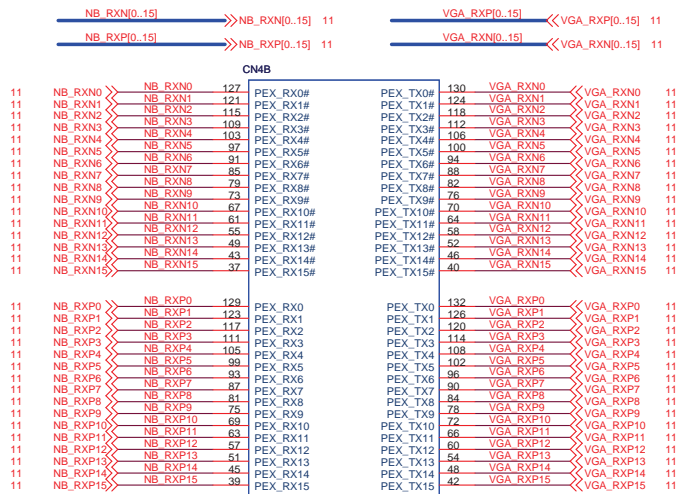
<http://hobi-elektronika.net>

 MICRO-STAR INT'L CO.,LTD.	
RS690T POWER & GND	
Size	Document Number
Custom	MS-171A1
Date:	Friday, September 14, 2007
Sheet	13 of 48
Rev	10

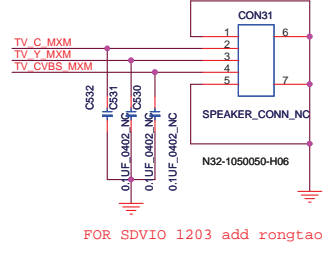
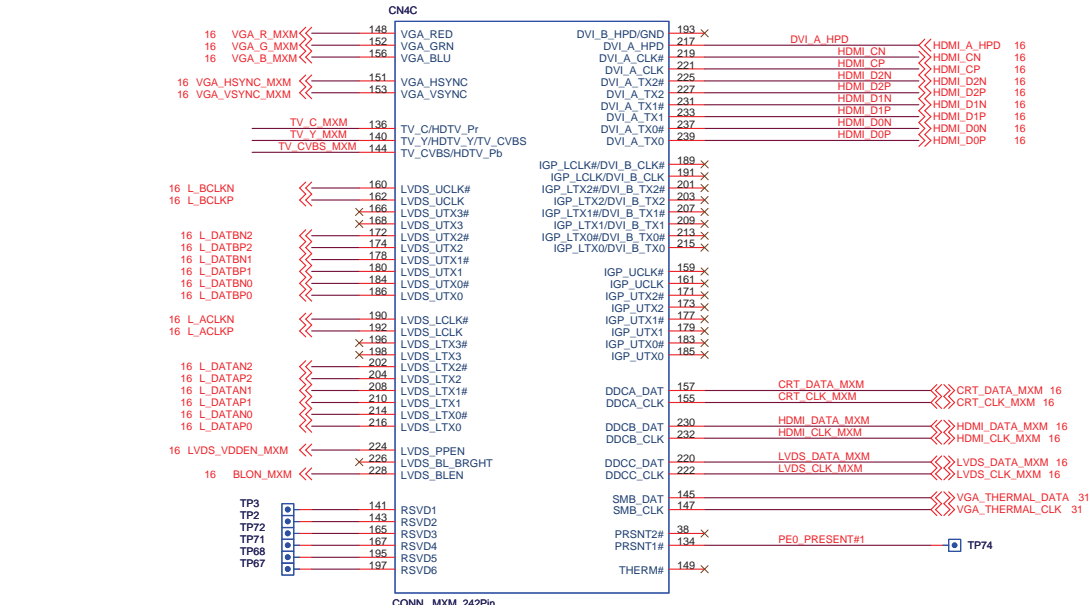
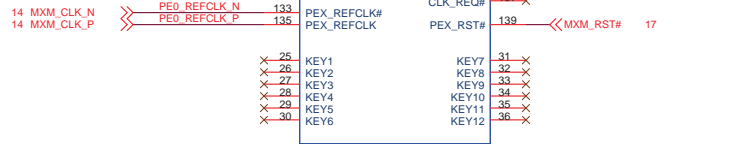
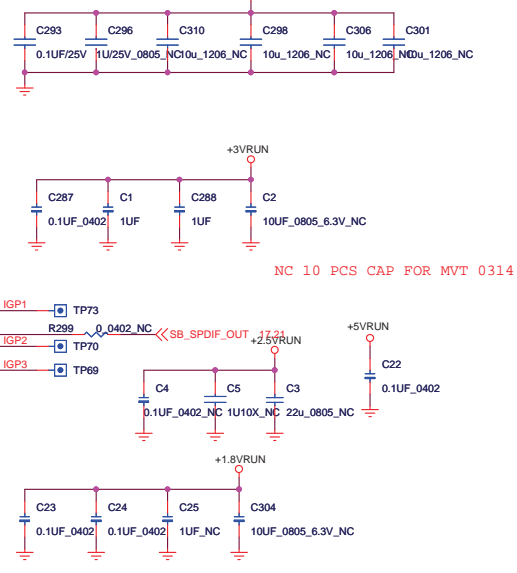
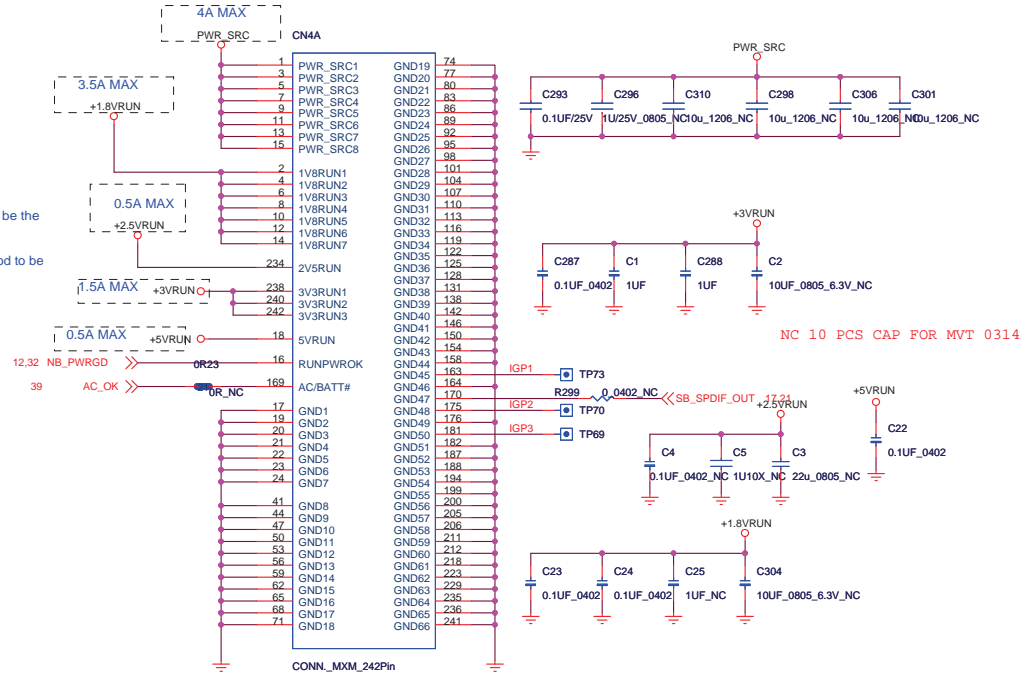
- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U11
- 2- PUT DECOUPLING CAPS CLOSE TO U11 POWER PIN

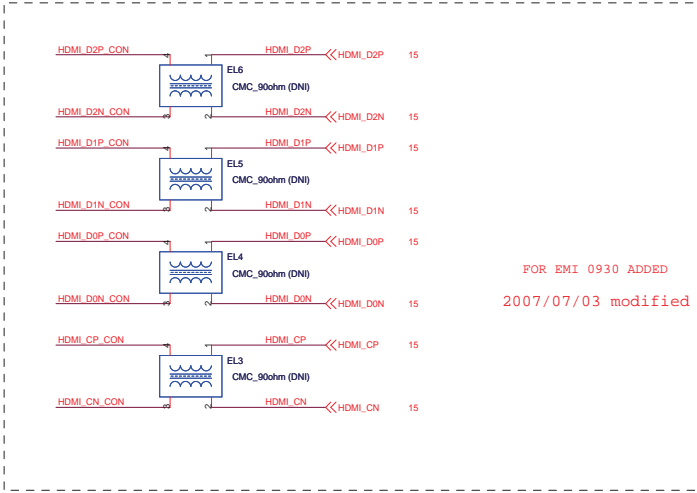
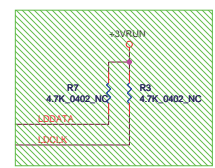
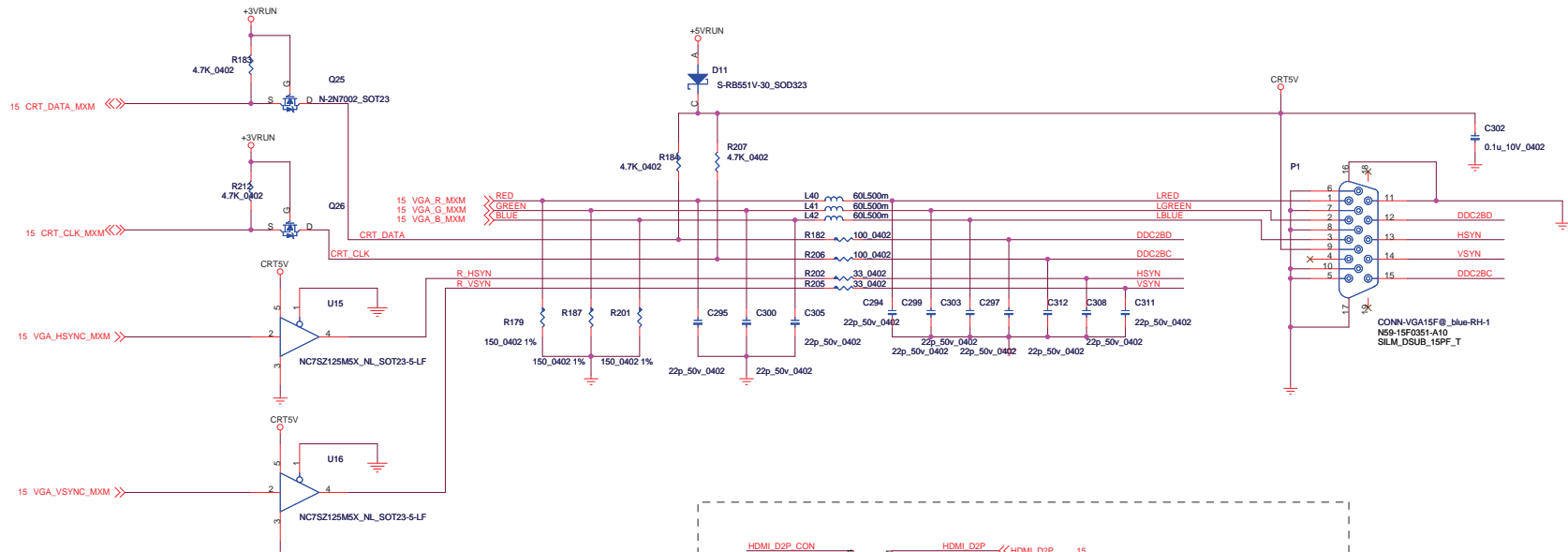


$I_{oh} = 5 \cdot I_{ref} (2.32mA)$
 $V_{oh} = 0.71V @ 60 ohm$



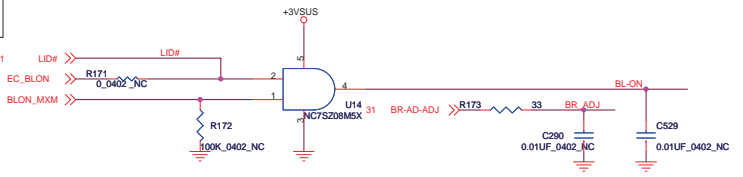
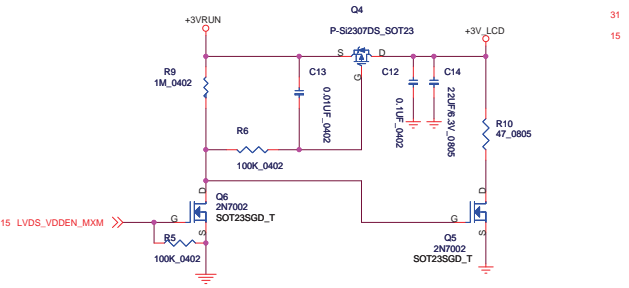
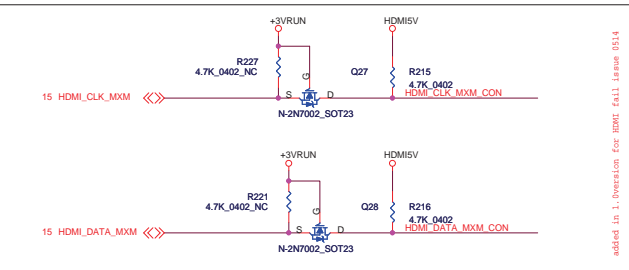
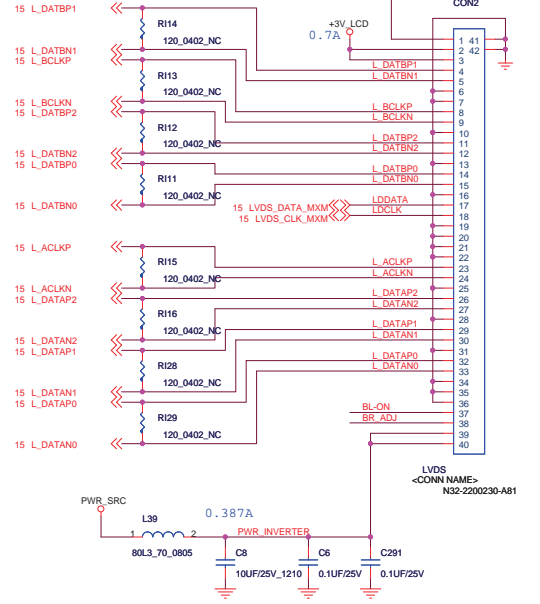
Ati:NC, and use +3VRUN to be the control signal on MXM
 nVIDIA:use system power good to be the control signal





FOR EMI 0930 ADDED
2007/07/03 modified

Bridge R for EMI
2007/07/06 modified



<http://hobi-elektronika.net>



PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB600

	SB600
C325 to C332	0.1uF
R165	562 Ohm 1%
R166	2.05k 1%
R167	0 Ohm
R179	10K

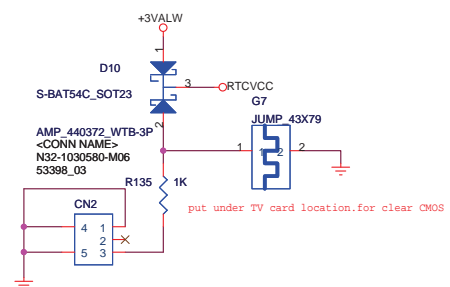
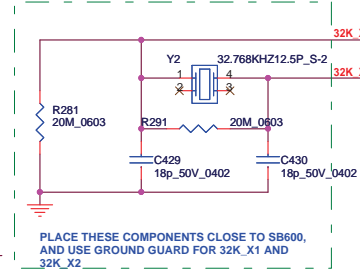
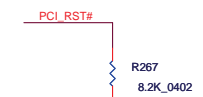
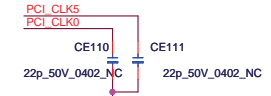
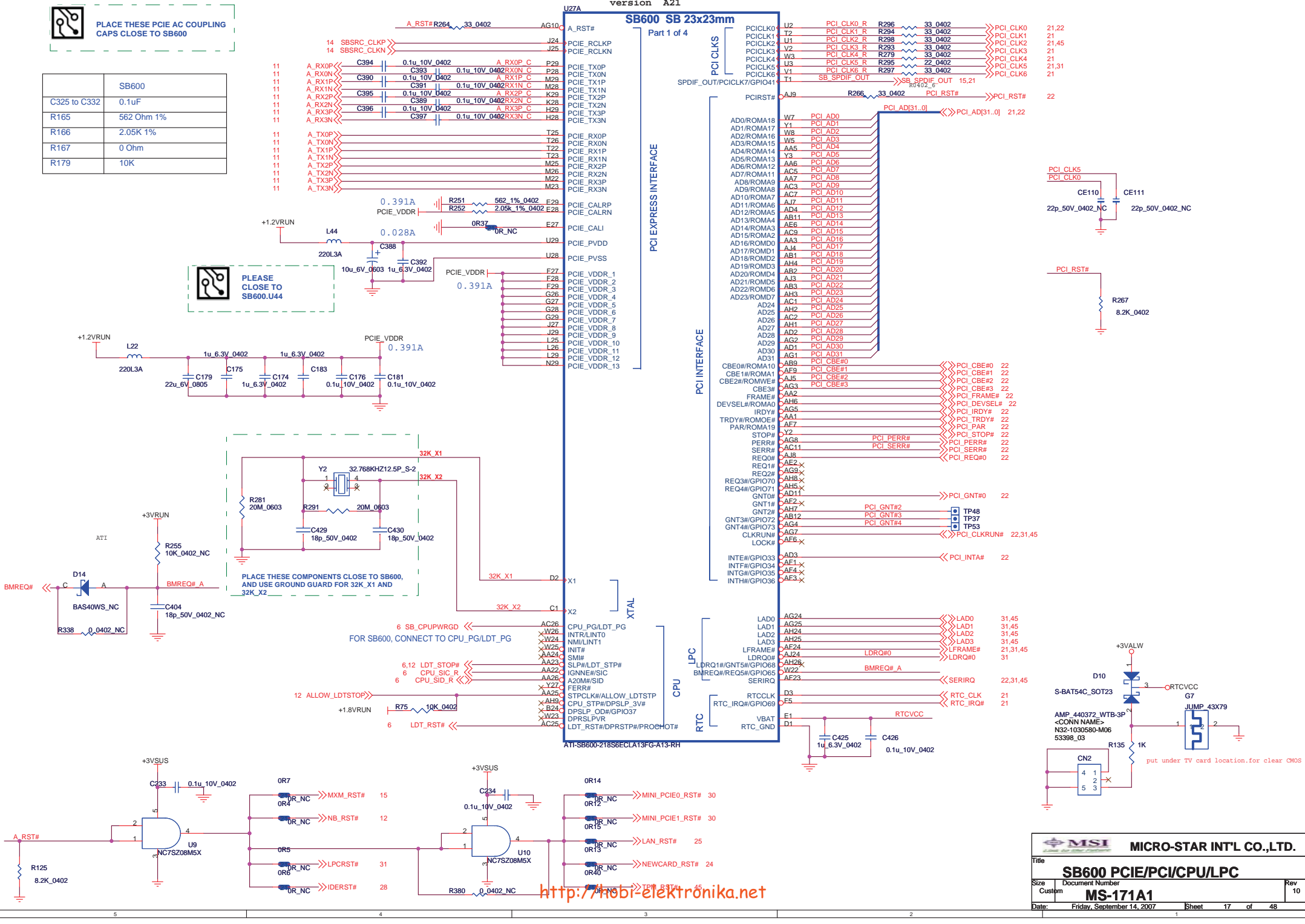


PLEASE CLOSE TO SB600,U44

version A21

SB600 SB 23x23mm

Part 1 of 4



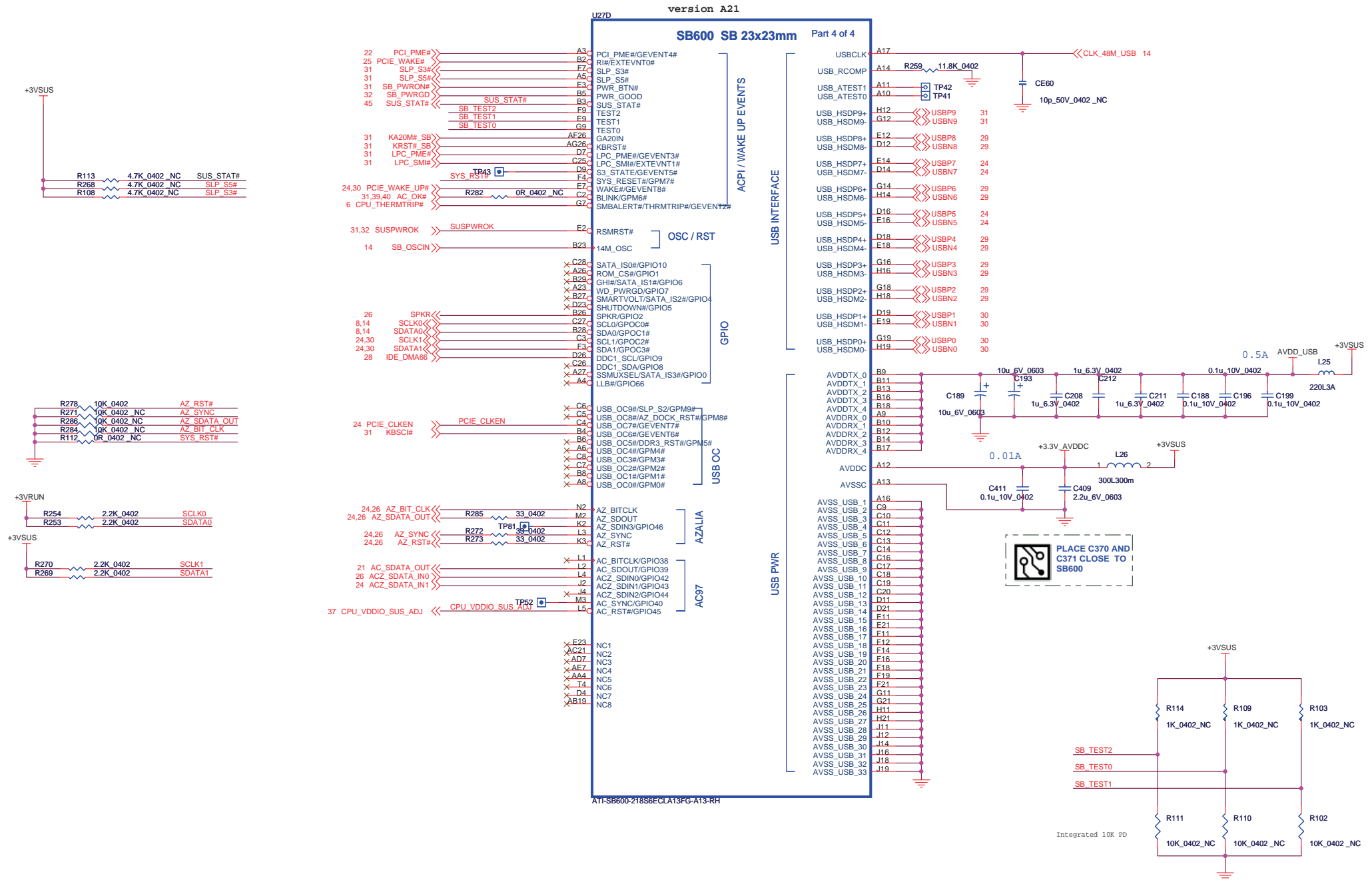
<http://hobi-elektronika.net>

MSI MICRO-STAR INT'L CO.,LTD.

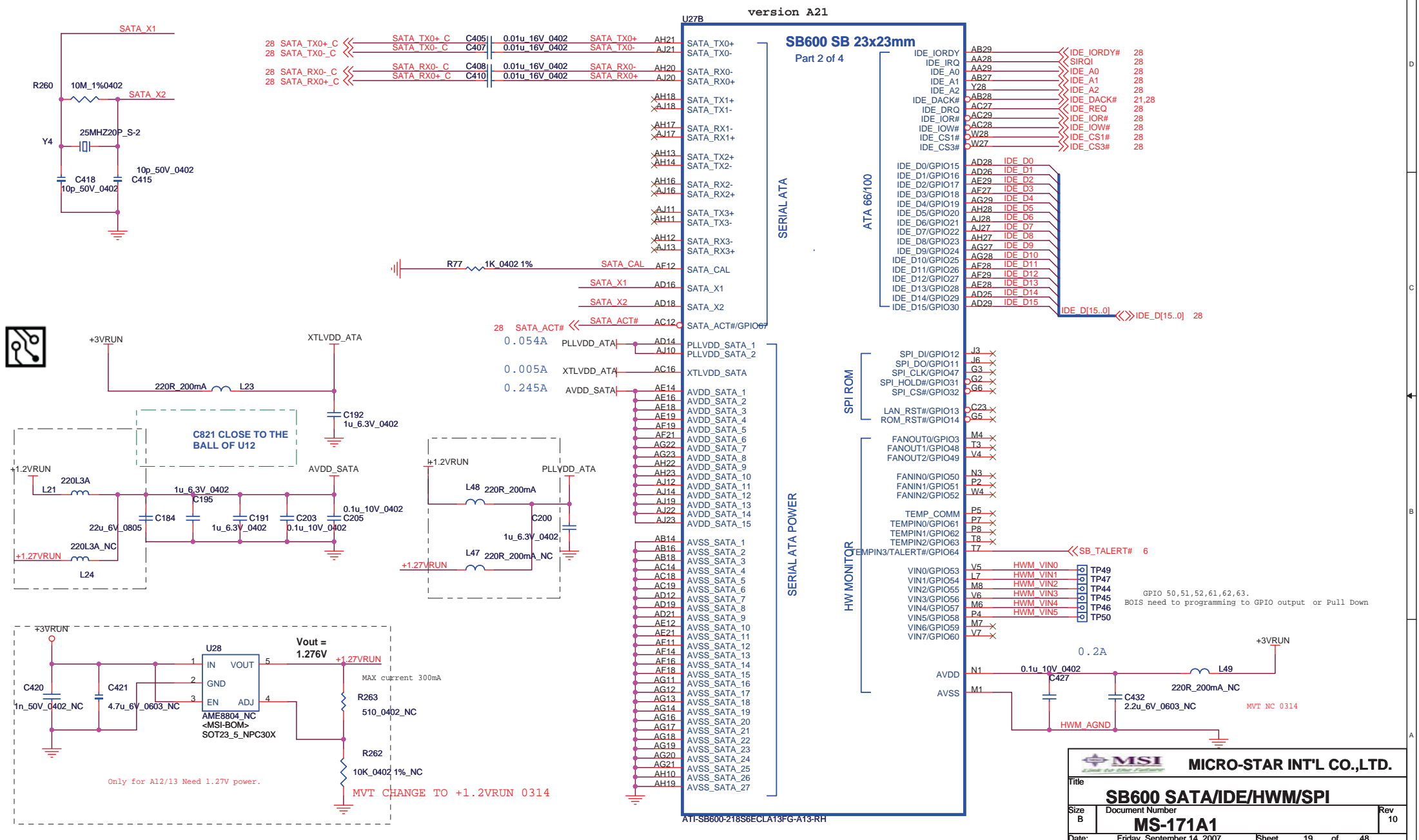
Title: **SB600 PCIE/PCI/CPU/LPC**


Size: Custom Document Number: **MS-171A1** Rev: 10

Date: Friday, September 14, 2007 Sheet: 17 of 48



<http://hobi-elektronika.net>

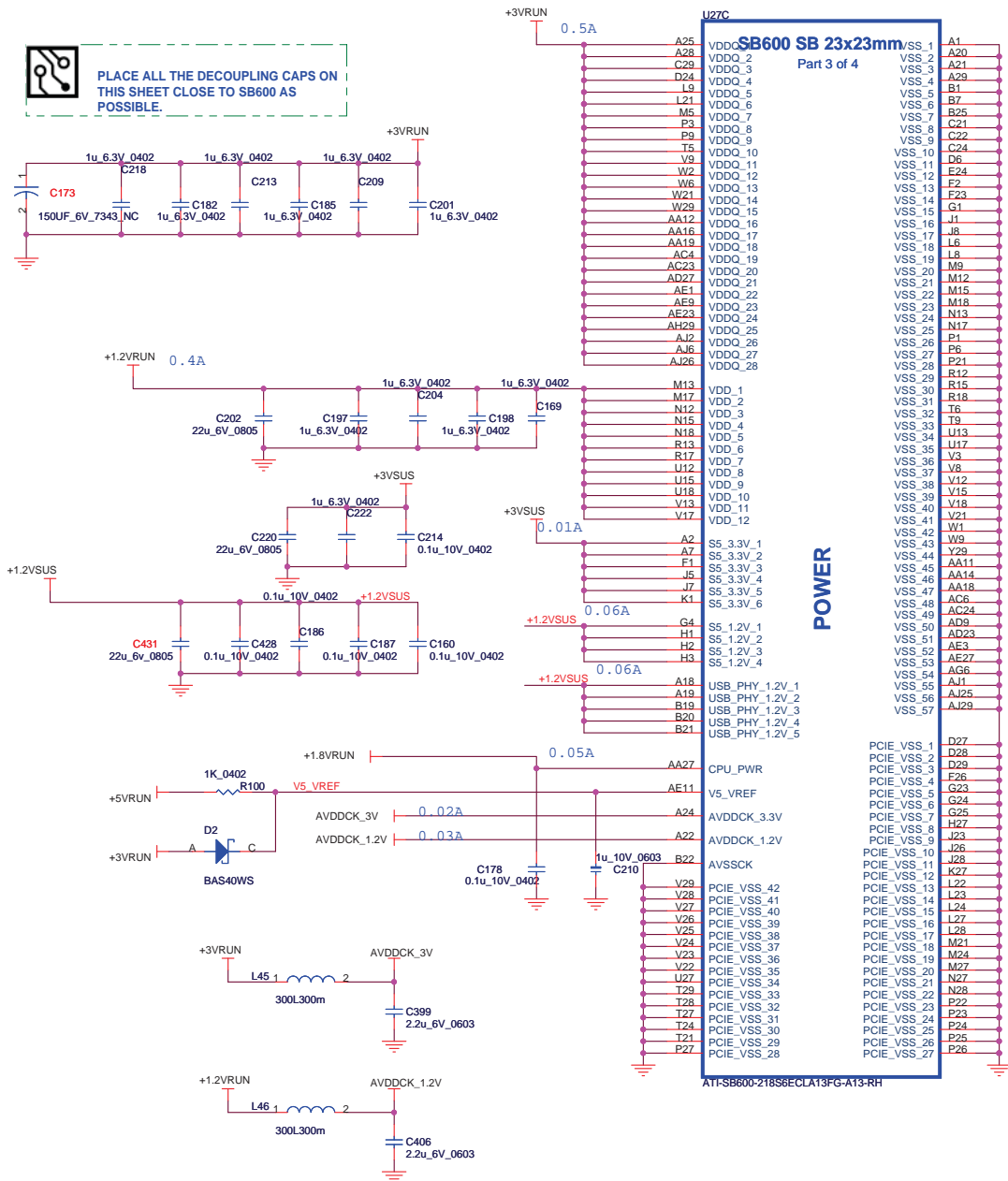


		MICRO-STAR INT'L CO.,LTD.	
Title			
SB600 SATA/IDE/HWM/SPI			
Size B	Document Number		Rev 10
MS-171A1			
Date:	Friday, September 14, 2007	Sheet	19 of 48



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB600 AS POSSIBLE.

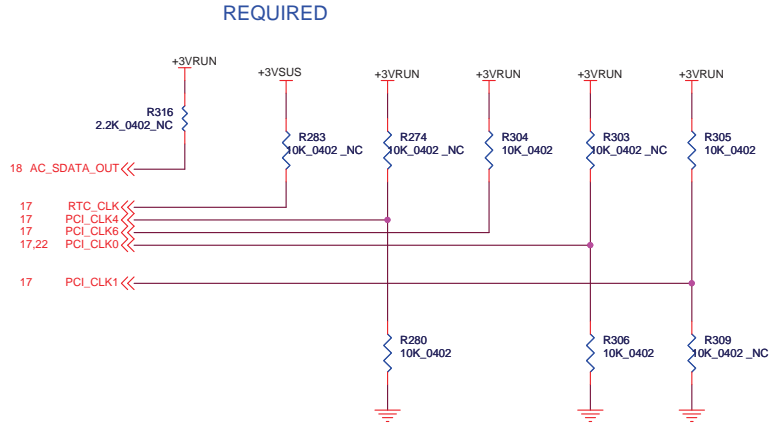
MVT NC 0314



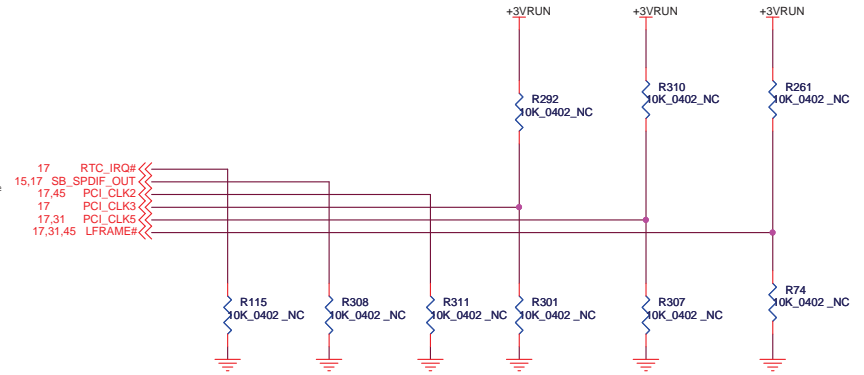
POWER

REQUIRED STRAPS

NPTE: FOR SB460, EXTERNAL PU/PD ARE REQUIRED



SPDIF_OUT Integrated 10K
PM2_EbH. Default: PU/PD not enable
BIOS must confirm with AMI/ATI.

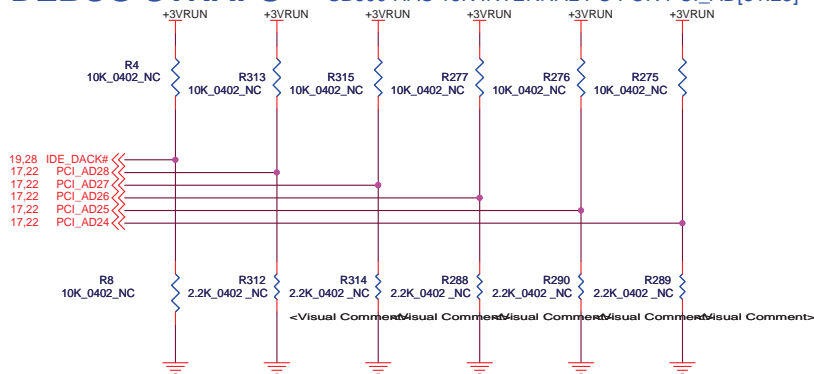


SB600						
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	L, L = FWH ROM	

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

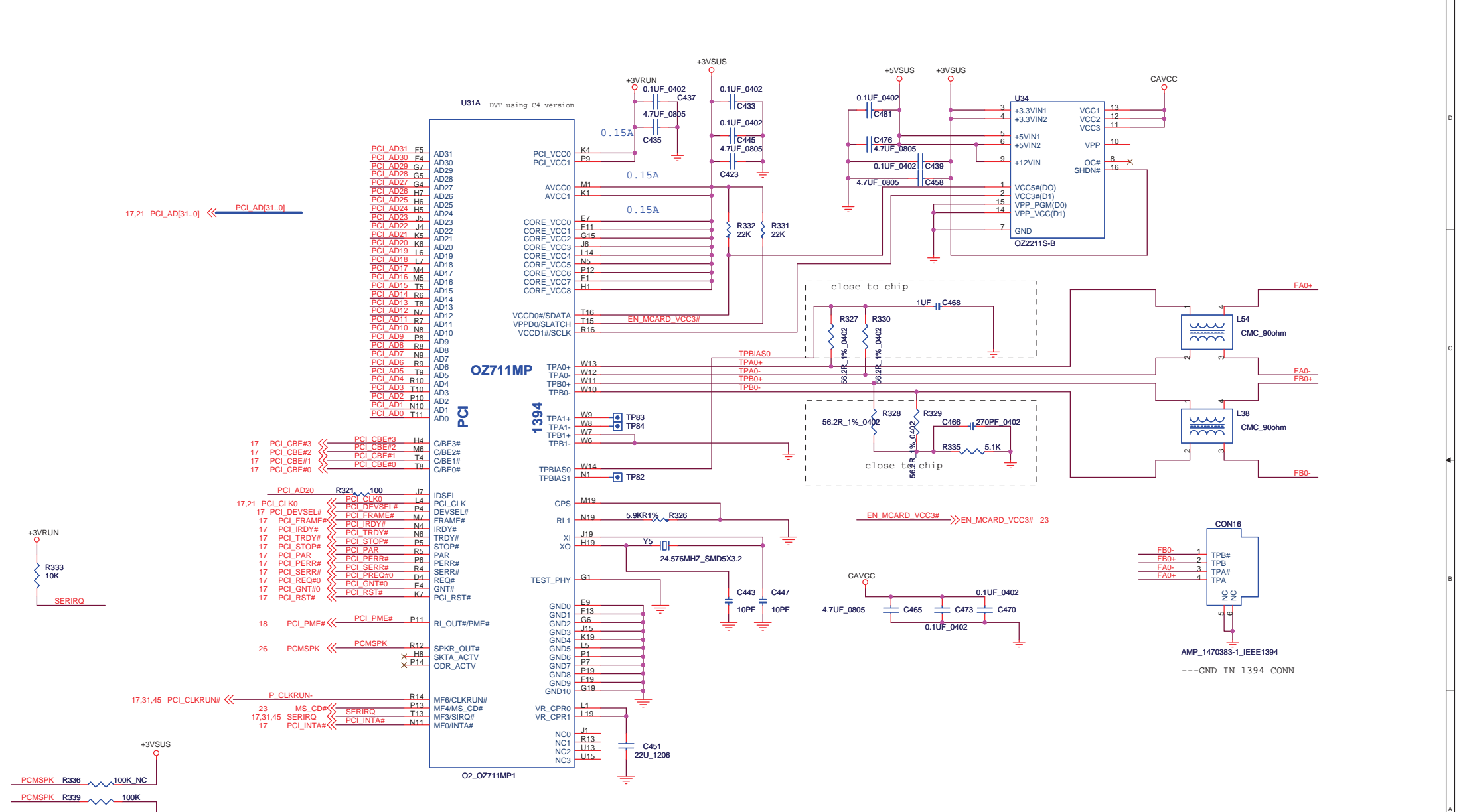
DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[31:23]



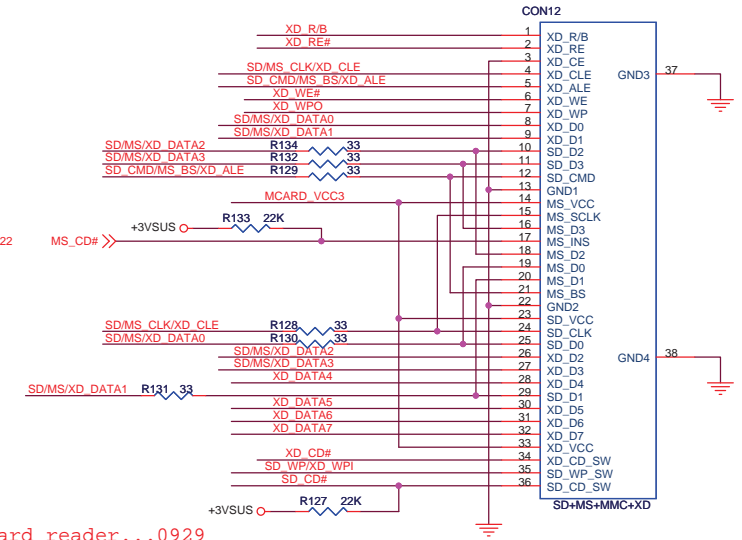
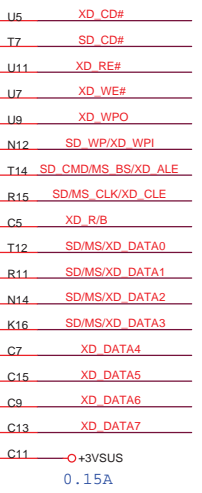
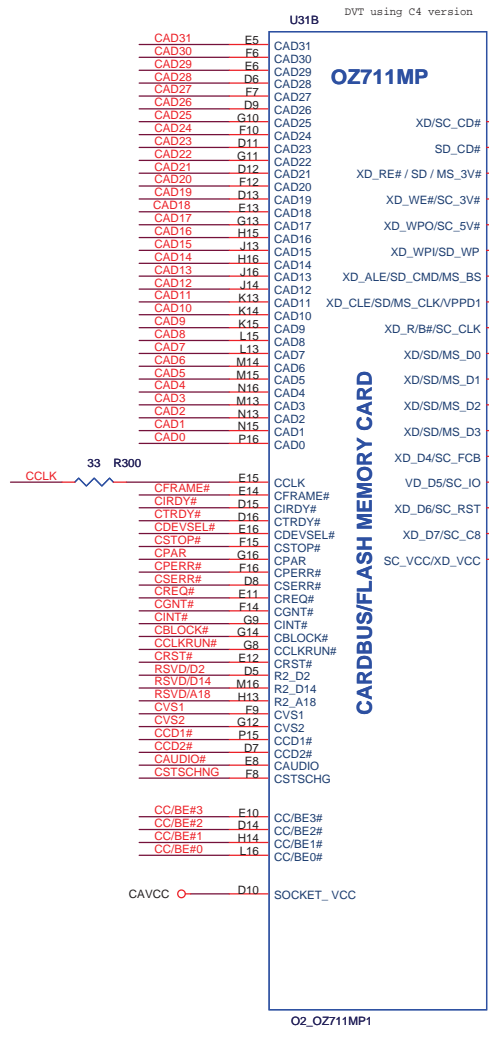
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS



171A DVT phase in C4 version

		MICRO-STAR INT'L CO.,LTD.	
Title PCI BUS / 1394 (OZ711MP)			
Size	Document Number	Rev	
Custom	MS-171A1	10	
Date:	Thursday, October 04, 2007	Sheet	22 of 48



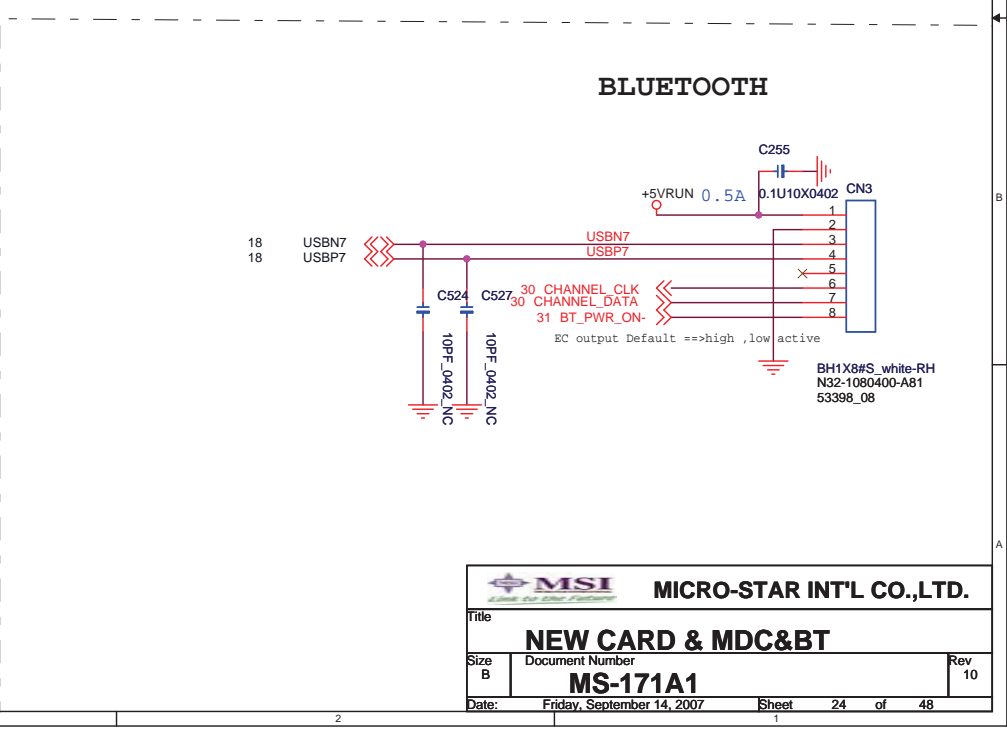
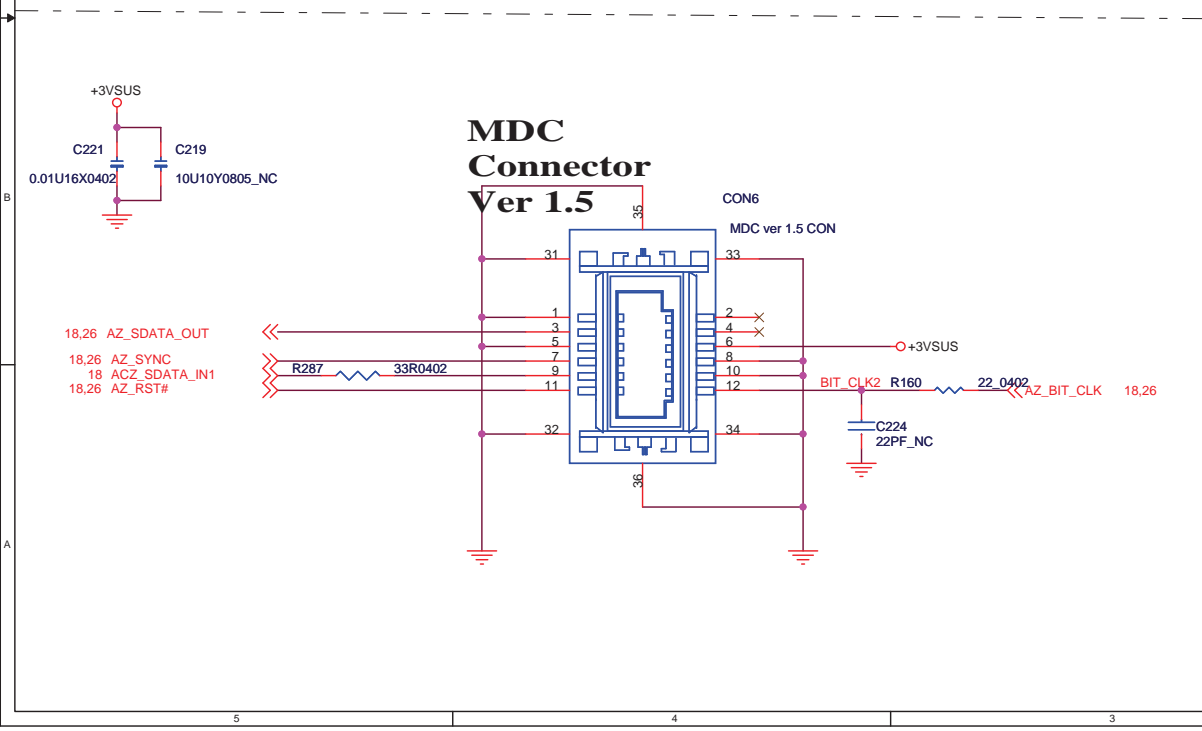
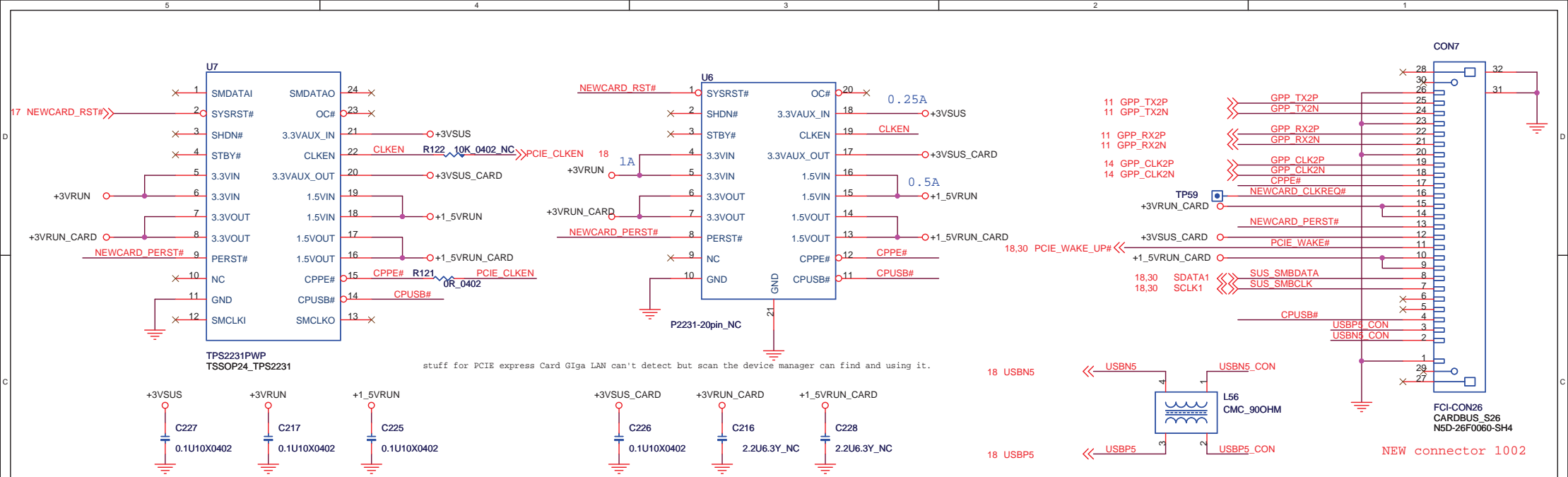
new card reader...0929

MSI MICRO-STAR INT'L CO.,LTD.

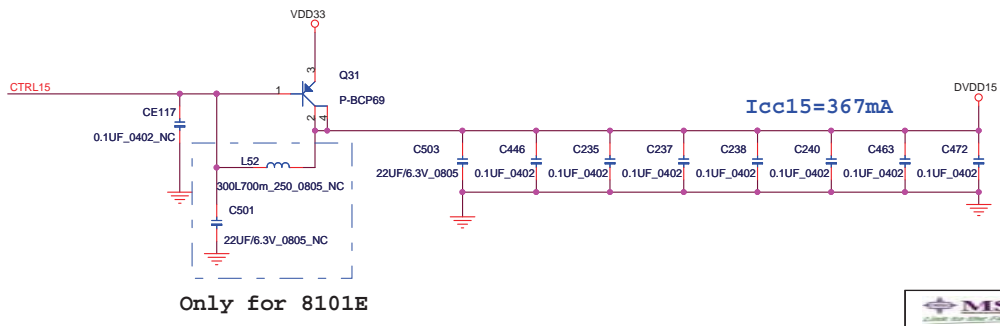
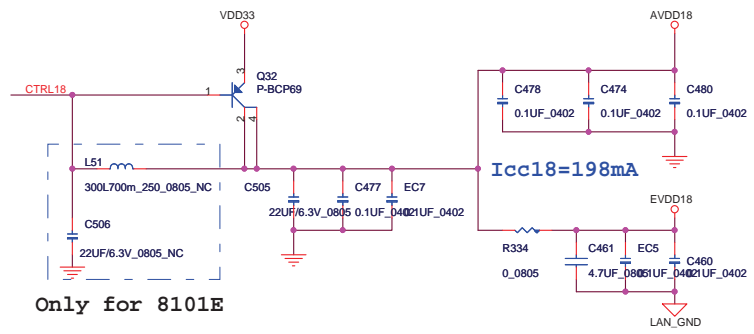
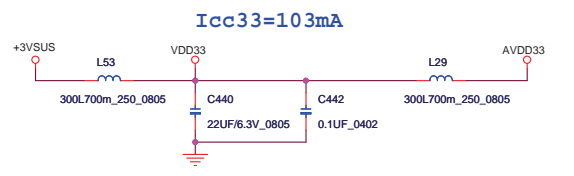
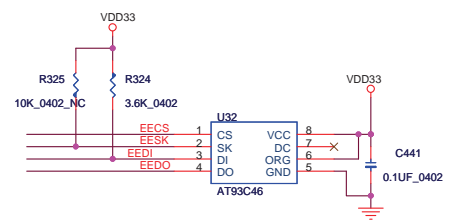
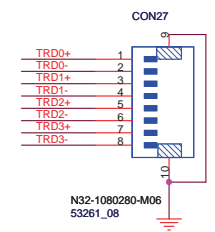
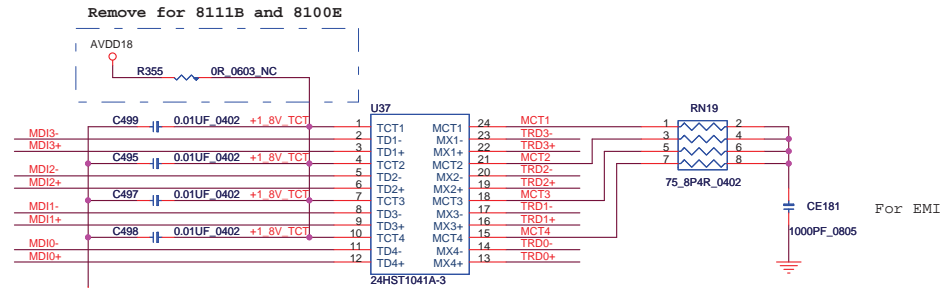
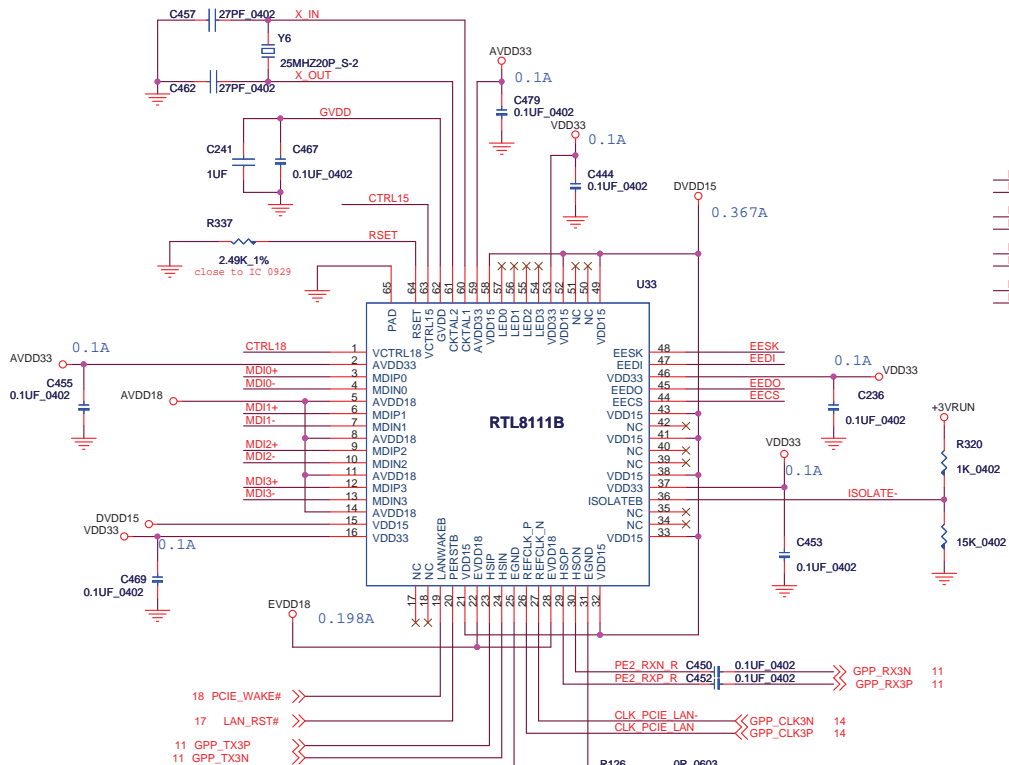
Title: **CARBUS / FLASH CARD CONN.**

Size: Custom Document Number: **MS-171A1** Rev: 10

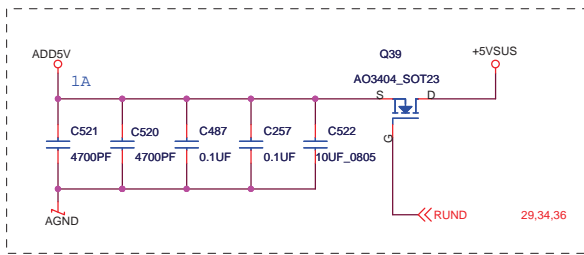
Date: Friday, September 14, 2007 Sheet: 23 of 48



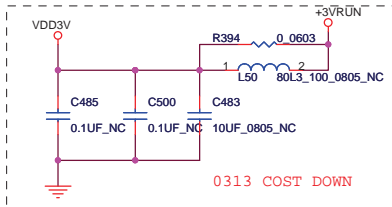
		MICRO-STAR INT'L CO.,LTD.	
Title			
NEW CARD & MDC&BT			
Size	Document Number		Rev
B	MS-171A1		10
Date:	Friday, September 14, 2007	Sheet	24 of 48



<http://hobi-elektronika.net>

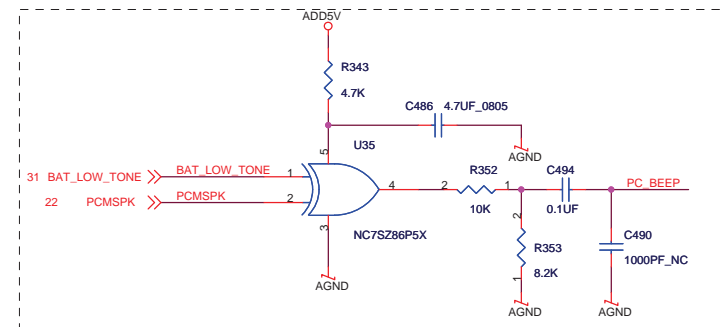


POWER ISOLATION (ANALOG 5V)

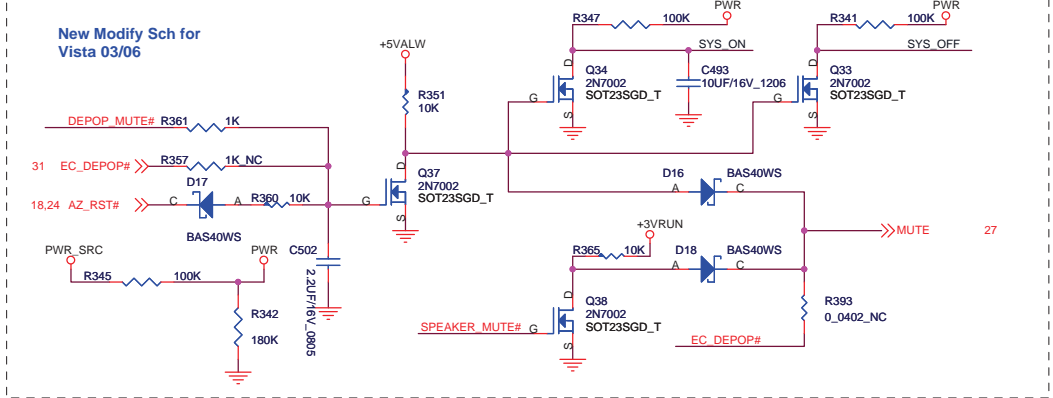


POWER ISOLATION (CODEC 3V)

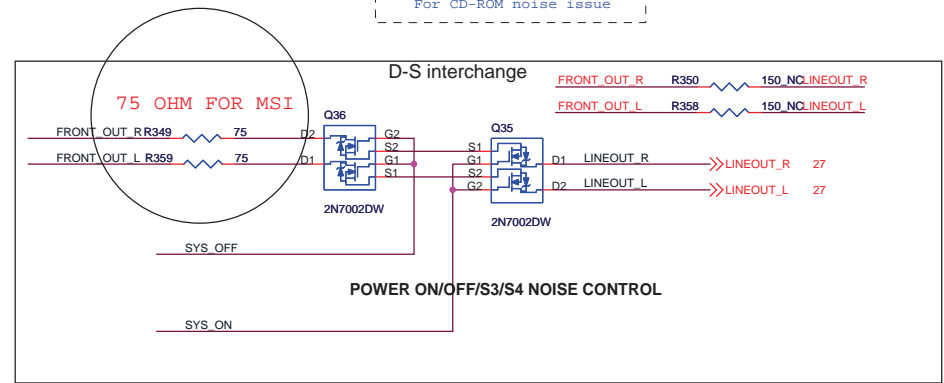
	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
SPEAKER_MUTE#	Normal keep High	Line-out Jack IN



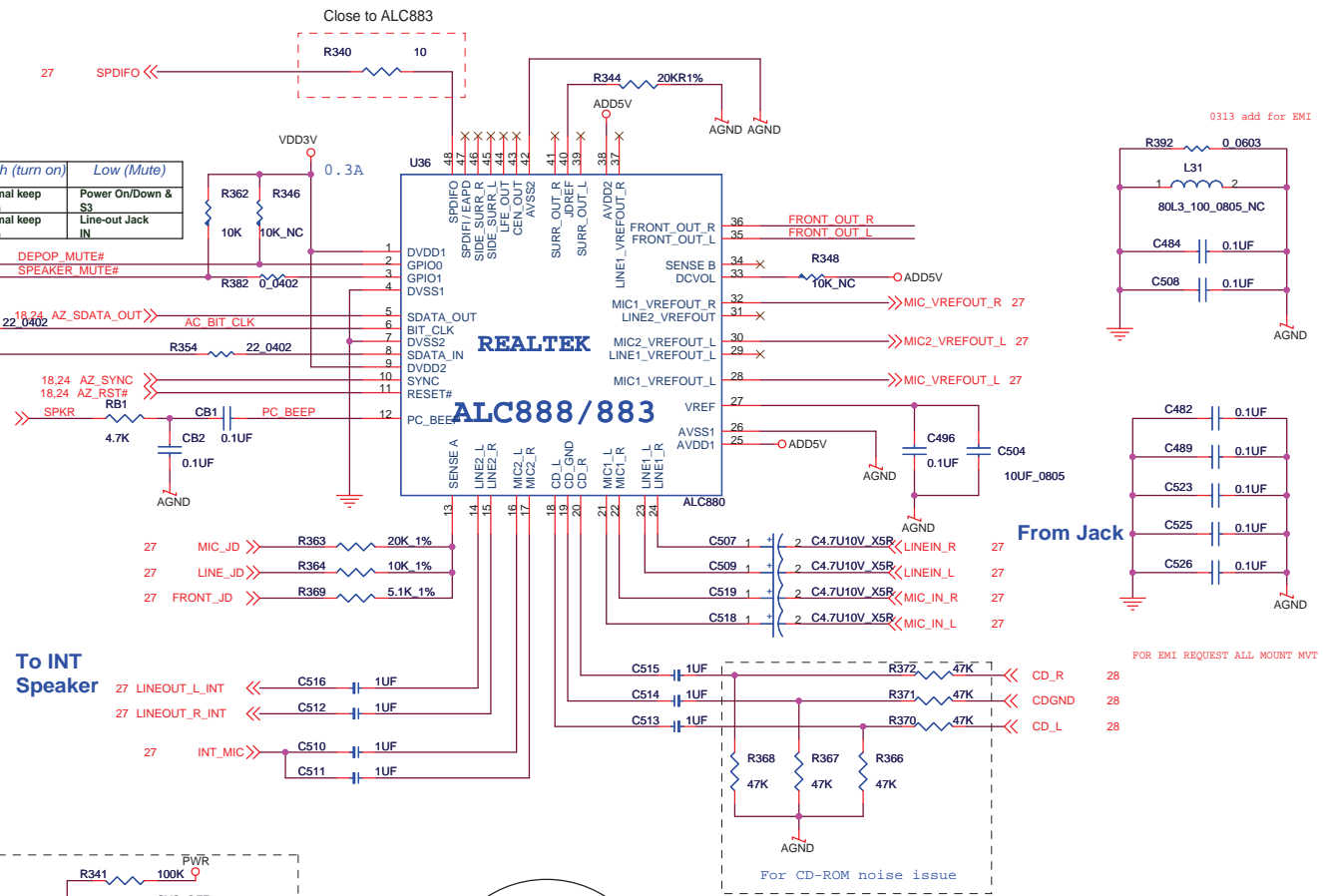
TONE & SPEAKER



Close To Power Source
POWER ON/OFF/S3/S4 NOISE CONTROL



POWER ON/OFF/S3/S4 NOISE CONTROL



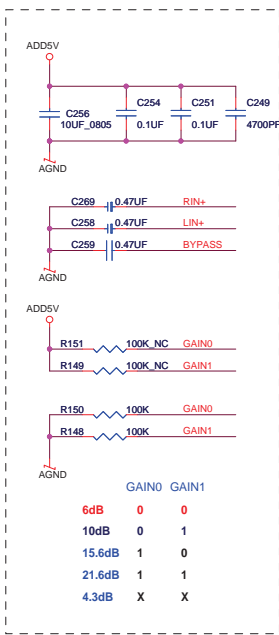
REALTEK
ALC888/883

To INT Speaker

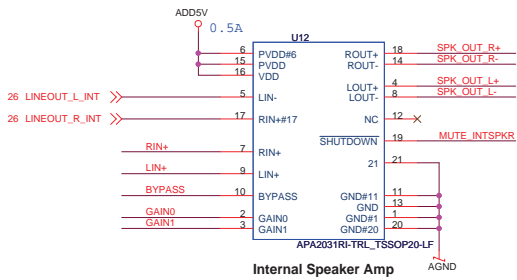
From Jack

For CD-ROM noise issue

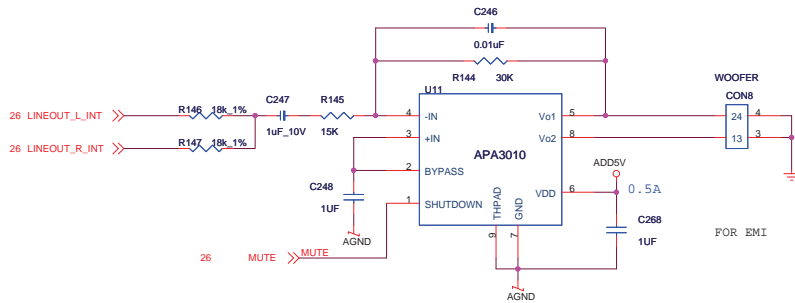
<http://hobi-elektronika.net>



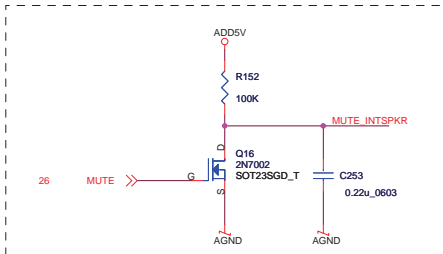
FOR APA2031



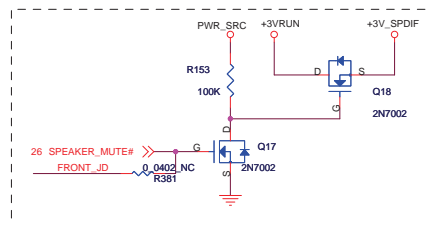
Internal Speaker Amp



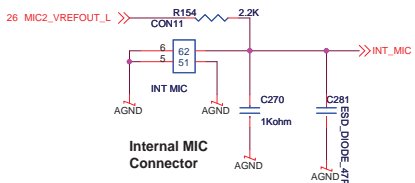
Internal Woofer Amp & Connector



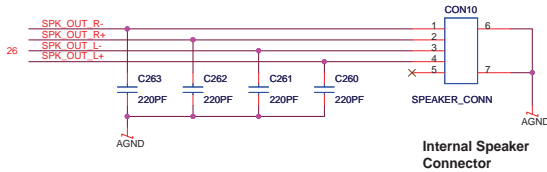
POWER ON/OFF/S3/S4 NOISE CONTROL



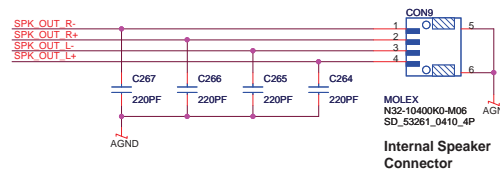
SPDIF ON/OFF CONTROL



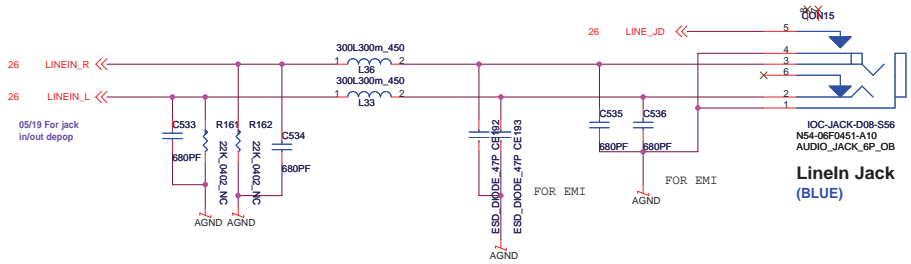
Internal MIC Connector



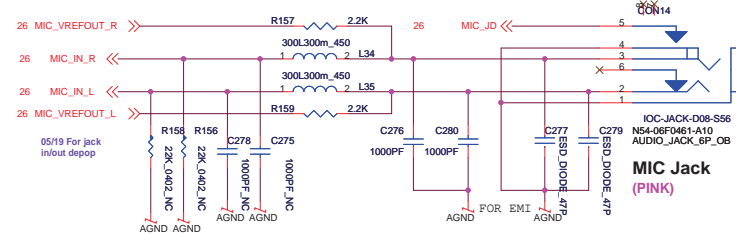
Internal Speaker Connector



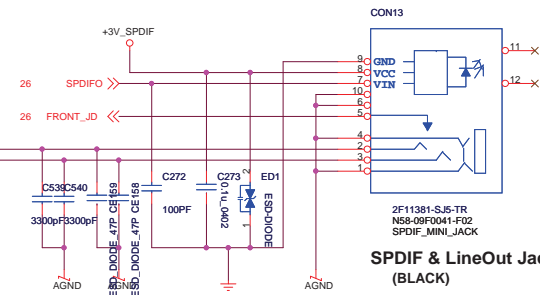
Internal Speaker Connector



LineIn Jack (BLUE)

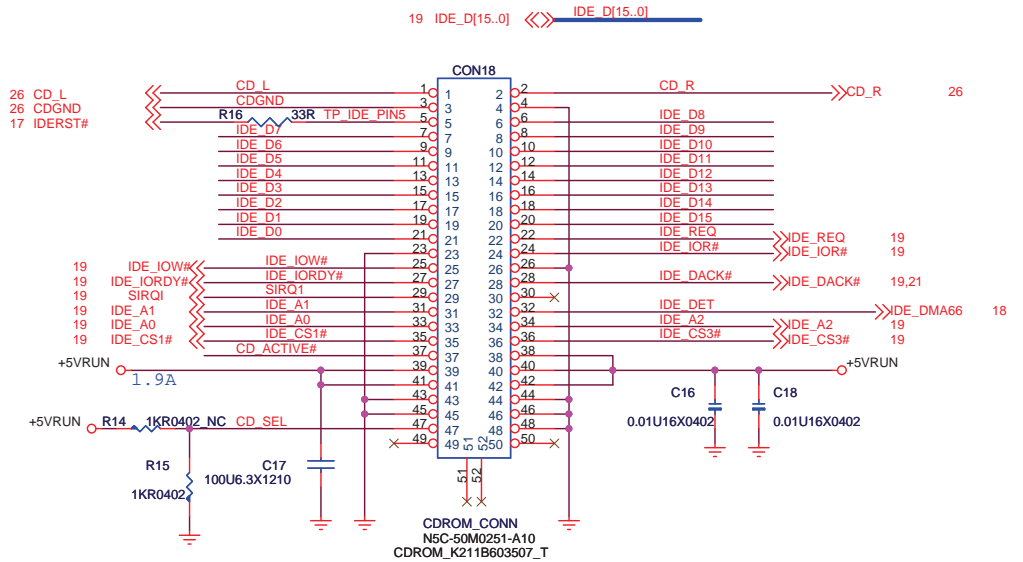
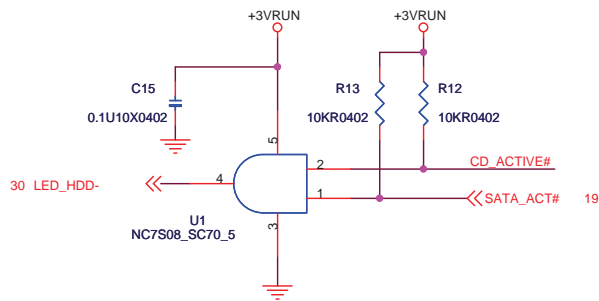
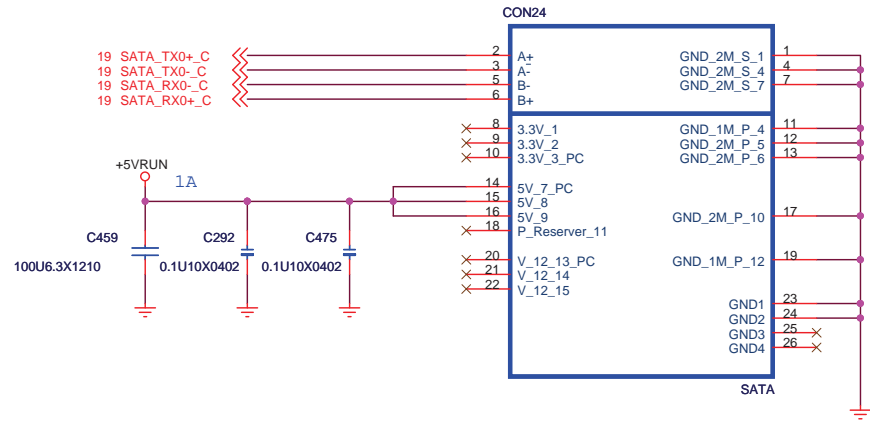


MIC Jack (PINK)

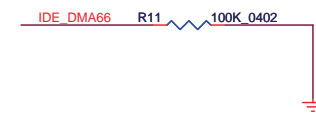



SPDIF & LineOut Jack (BLACK)

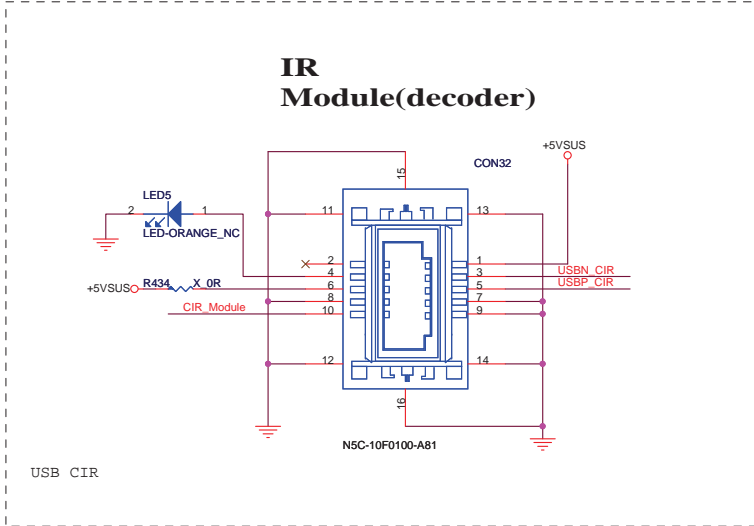
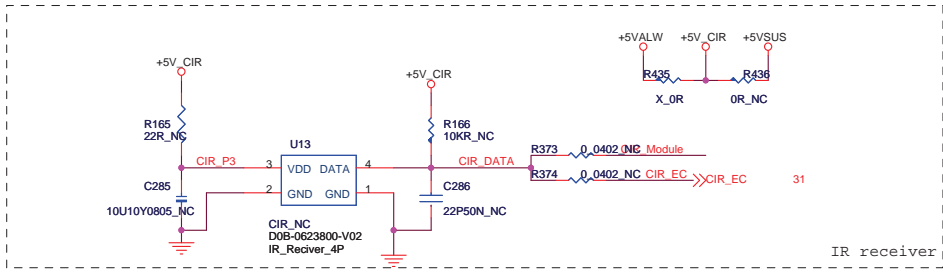
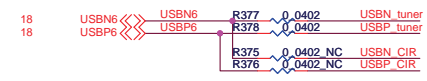
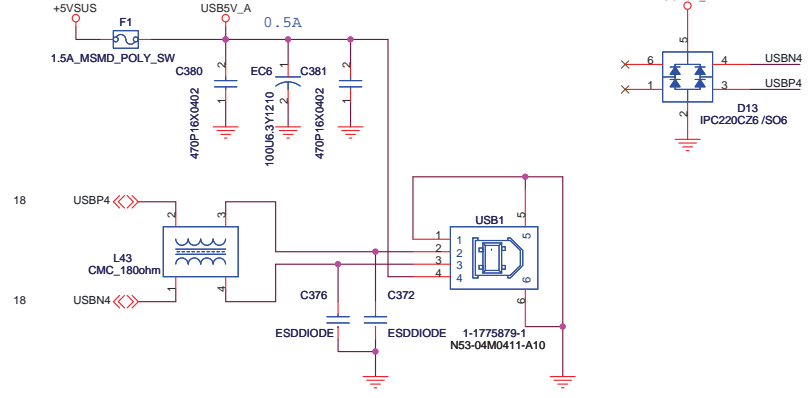
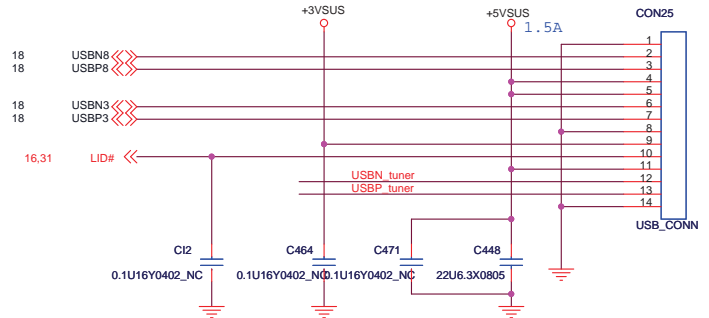
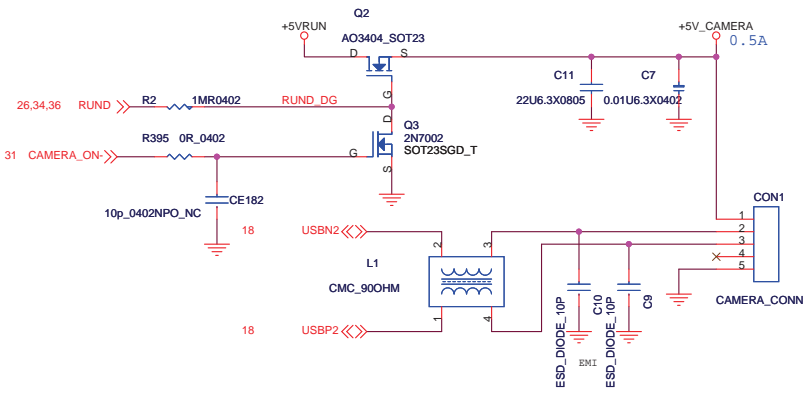
MSI MICRO-STAR INT'L CO.,LTD.		
Title	AMP & SPK & MIC & SPK	
Size	Document Number	Rev
Custom	MS-171A1	10
Date	Thursday, October 04, 2007	Sheet 27 of 48




PIN32:PDIAG
PIN37:PASP
PIN47:CABLE SELECT
Low:Master
NC or
High:Slave

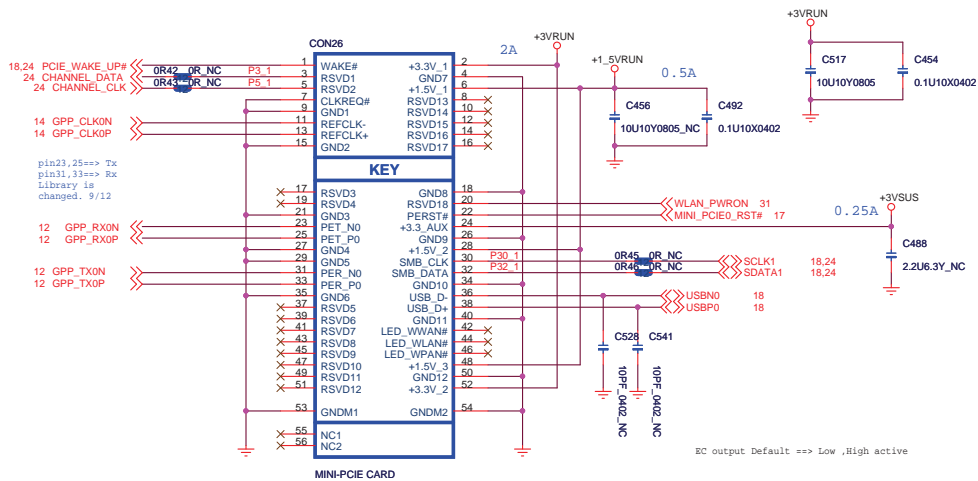


 MICRO-STAR INT'L CO.,LTD.	
Title HDD_ODD	
Size B	Document Number MS-171A1
Date: Thursday, October 04, 2007	Rev 10
Sheet 28 of 48	

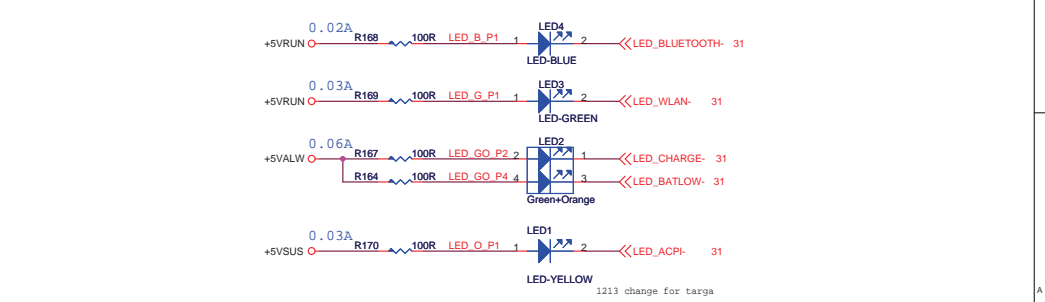
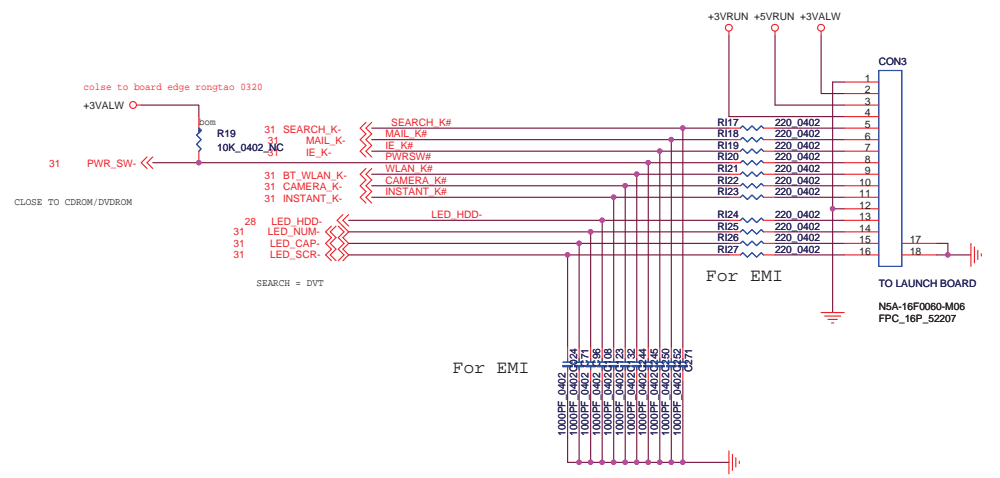
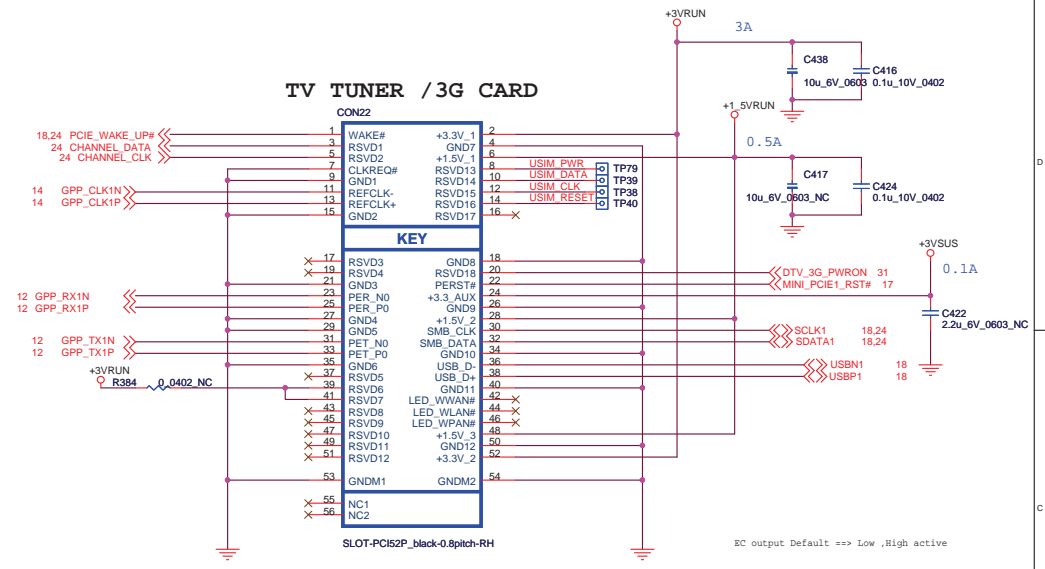


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		MICRO-STAR INT'L CO.,LTD.	
Title			
SATA HDD/PATA CDROM CONN			
Size	Document Number		Rev
Custpm	MS-171A1		10
Date:	Thursday, October 04, 2007		Sheet 29 of 48



Wireless LAN

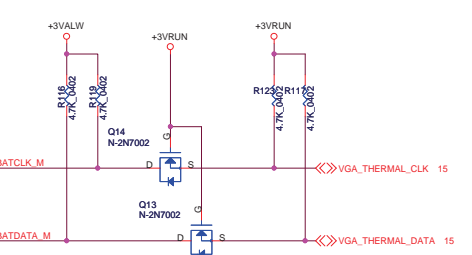
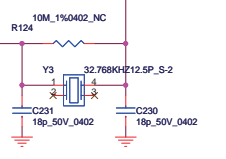
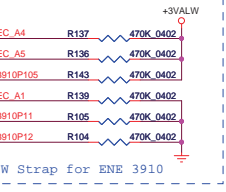
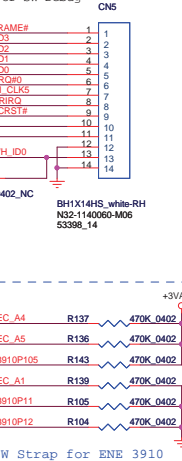
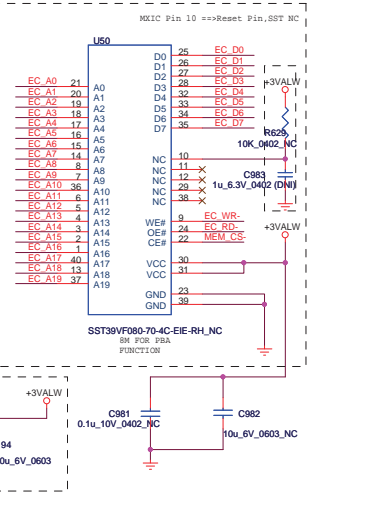
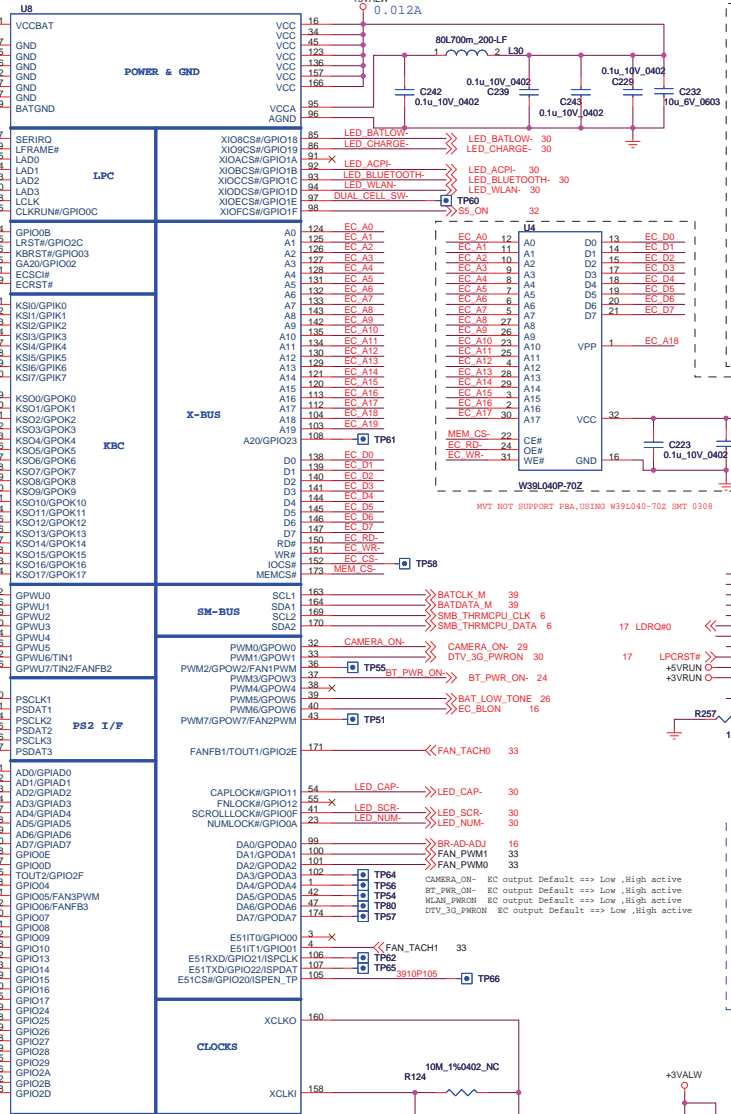
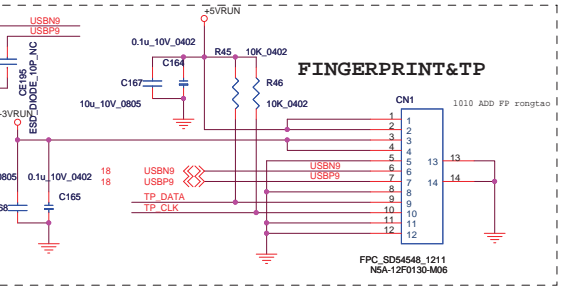
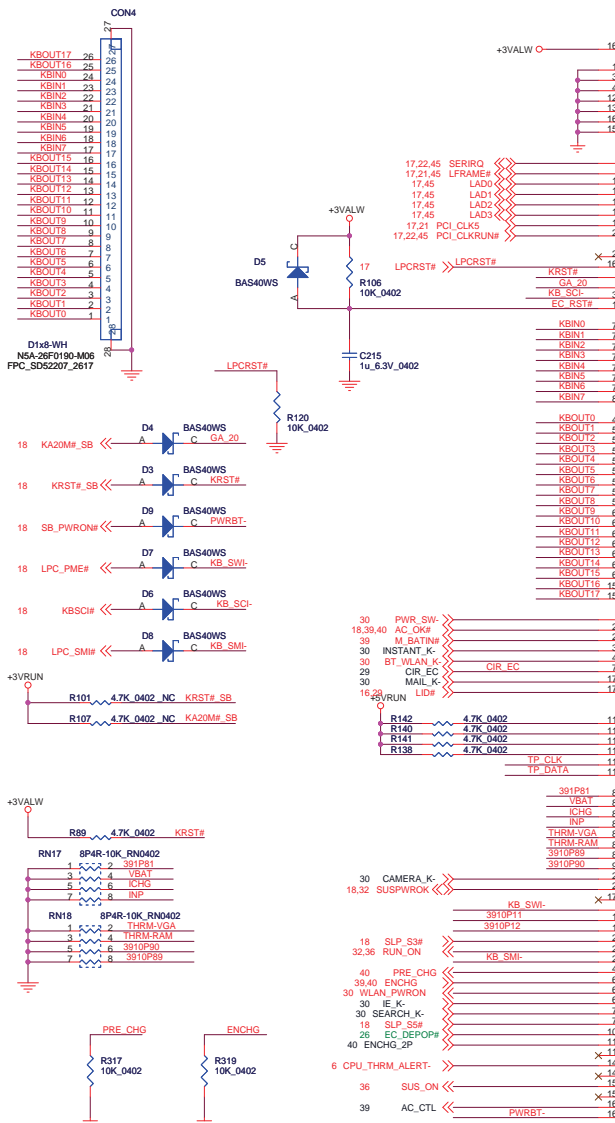


MSI MICRO-STAR INT'L CO.,LTD.

File: **MINI-PCIE X2& LED & SW**

Size: Custom Document Number: **MS-171A1** Rev: 10

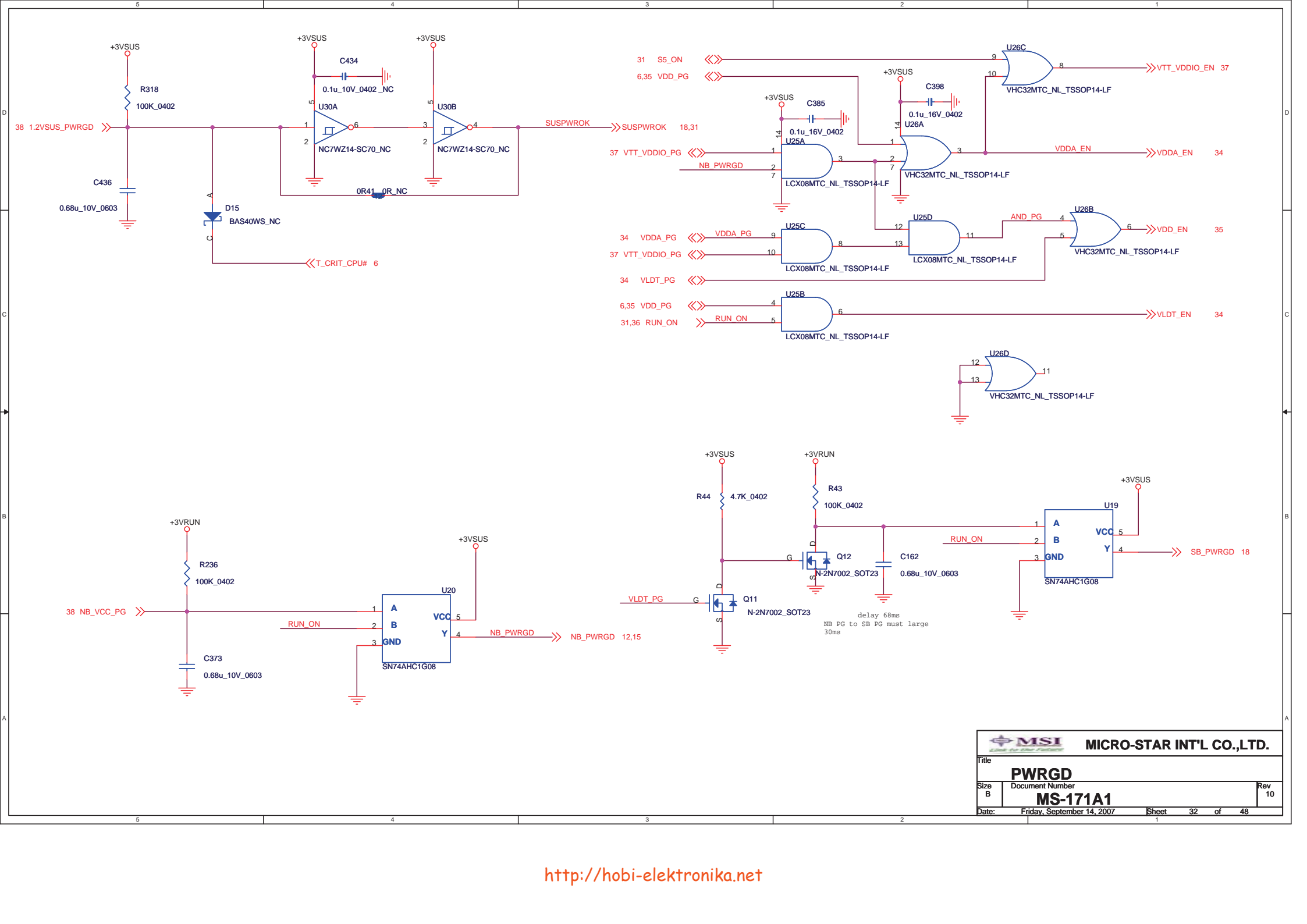
Date: Friday, September 14, 2007 Sheet: 30 of 48




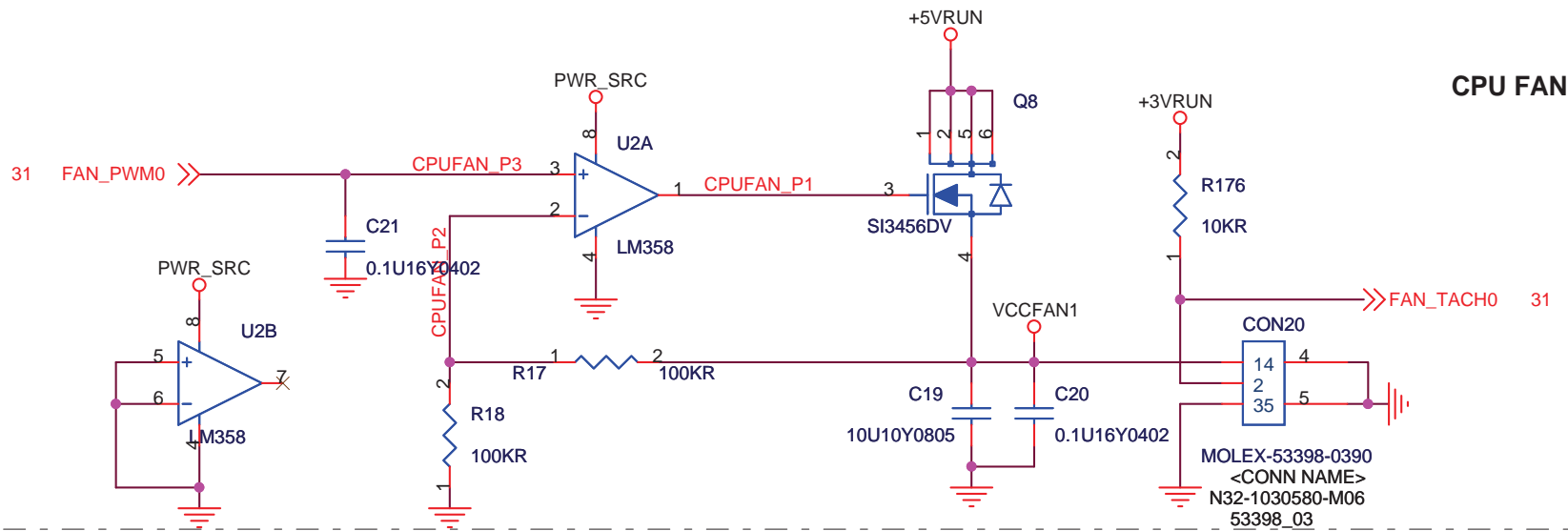
MSI MICRO-STAR INT'L CO.,LTD.

File		KBC (ENE3910) & ISA BIOS	
Size	Document Number	MS-171A1	
Date:	Friday, September 14, 2007	Sheet	31 of 48

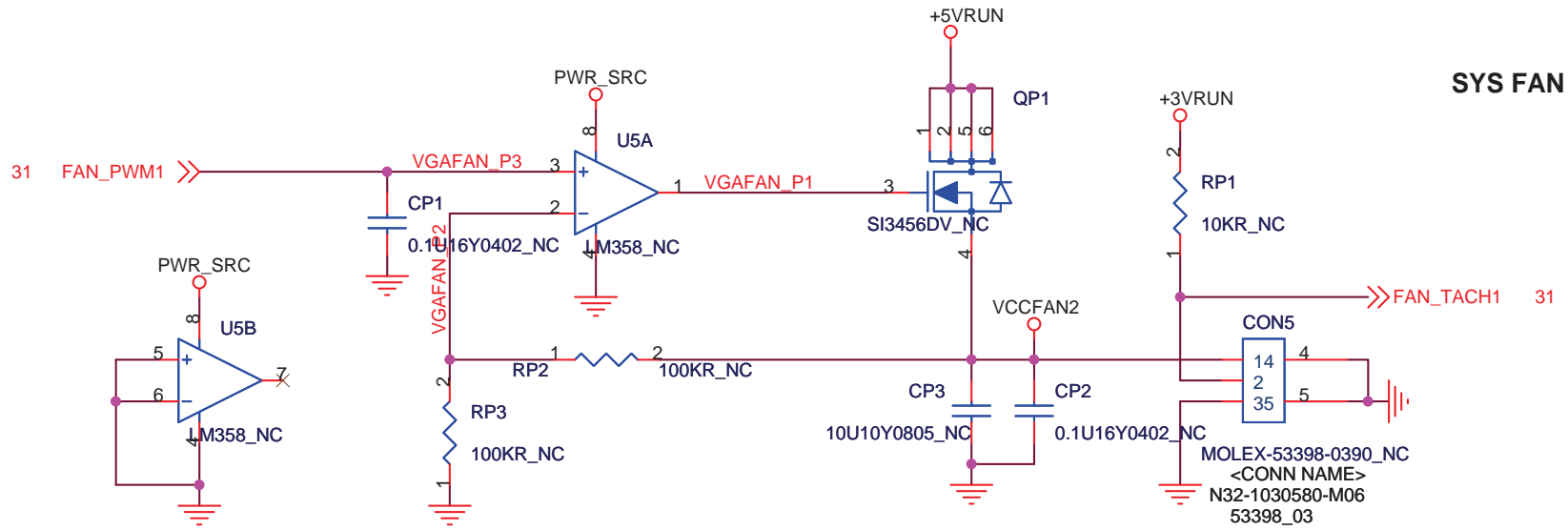
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 MICRO-STAR INT'L CO.,LTD.	
Title	
PWRGD	
Size	Document Number
B	MS-171A1
Date:	Friday, September 14, 2007
Sheet	32 of 48
Rev	10




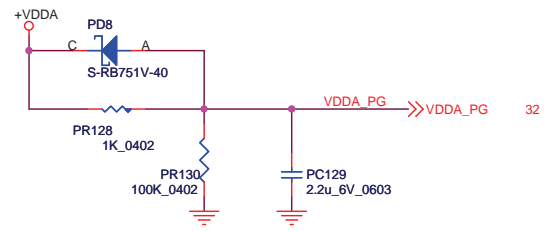
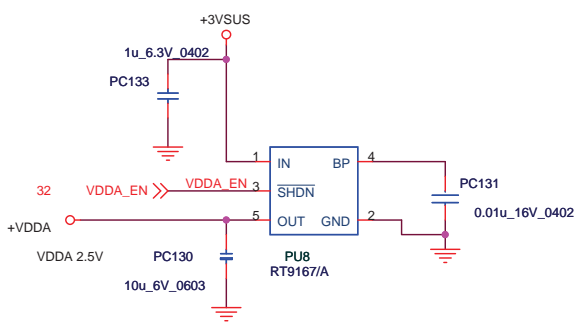
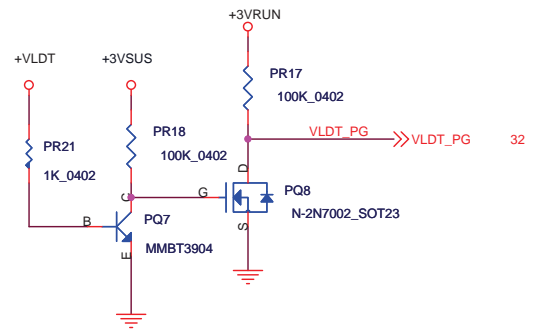
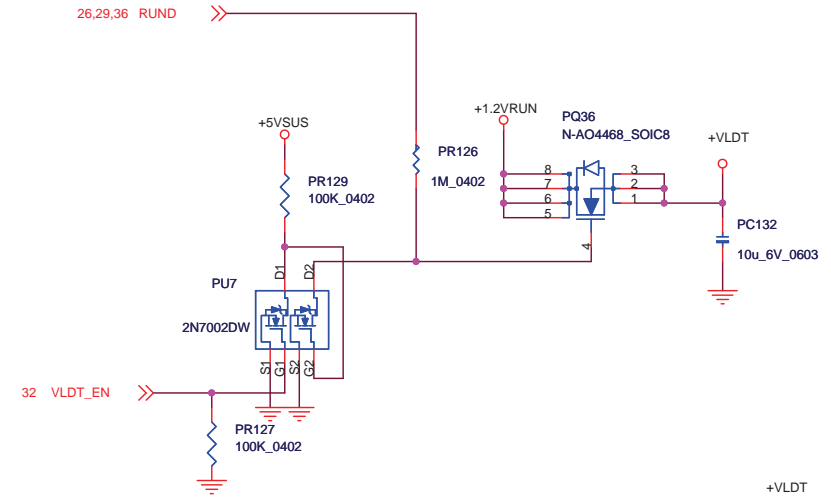
CPU FAN




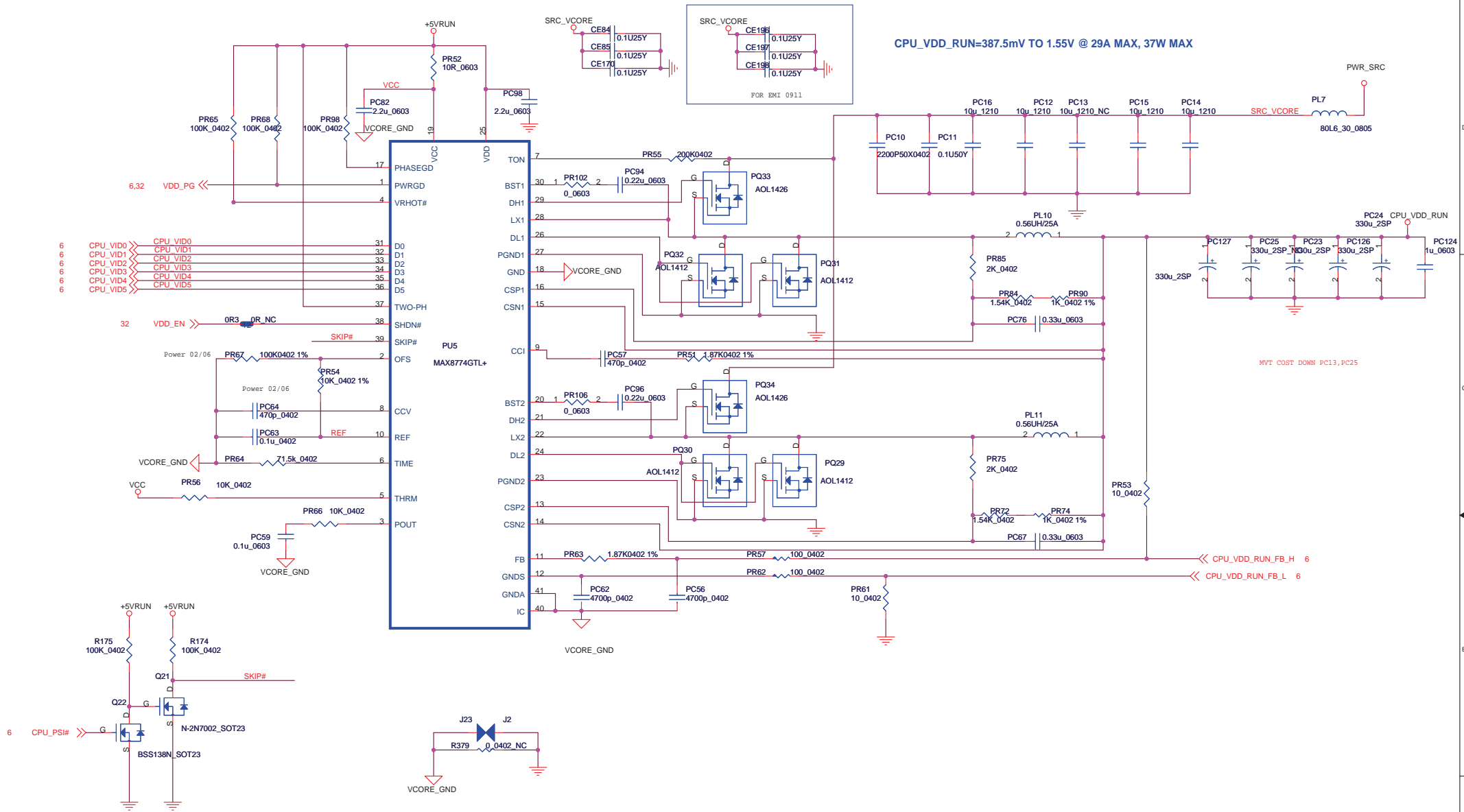
SYS FAN

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 MICRO-STAR INT'L CO.,LTD.	
Title	
FAN	
Size	Document Number
A	MS-171A1
Date:	Rev 10
Friday, September 14, 2007	10
Sheet	of
33	48




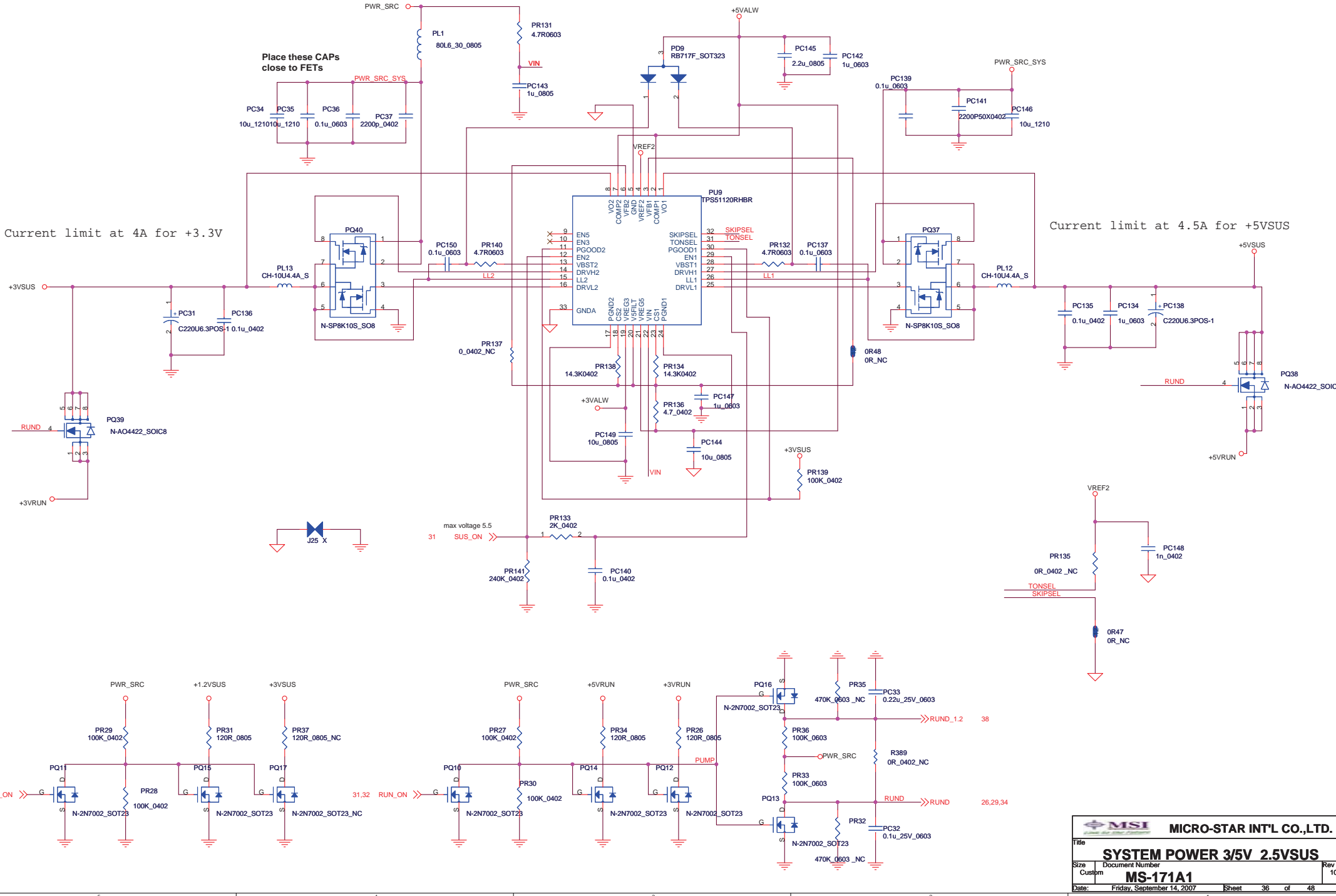
		MICRO-STAR INT'L CO.,LTD.	
Title			
M 1.2V VDDA 2.5V VLDT			
Size	Document Number		Rev
B	MS-171A1		10
Date:	Friday, September 14, 2007	Sheet	34 of 48



CPU_VDD_RUN=387.5mV TO 1.55V @ 29A MAX, 37W MAX

<http://hobi-elektronika.net>

 MICRO-STAR INT'L CO.,LTD.	
Title	
VCORE	
Size	Document Number
Custom	MS-171A1
Date:	Friday, September 14, 2007
Sheet	35 of 48
Rev	10




Current limit at 4A for +3.3V

Current limit at 4.5A for +5VSUS

Place these CAPs close to FETs

max voltage 5.5

 MICRO-STAR INT'L CO.,LTD.			
SYSTEM POWER 3/5V 2.5VSUS			
Size	Document Number		Rev
Custom	MS-171A1		10
Date:	Friday, September 14, 2007	Sheet	36 of 48

Current limit at 3.8A for SMDR_VTERM

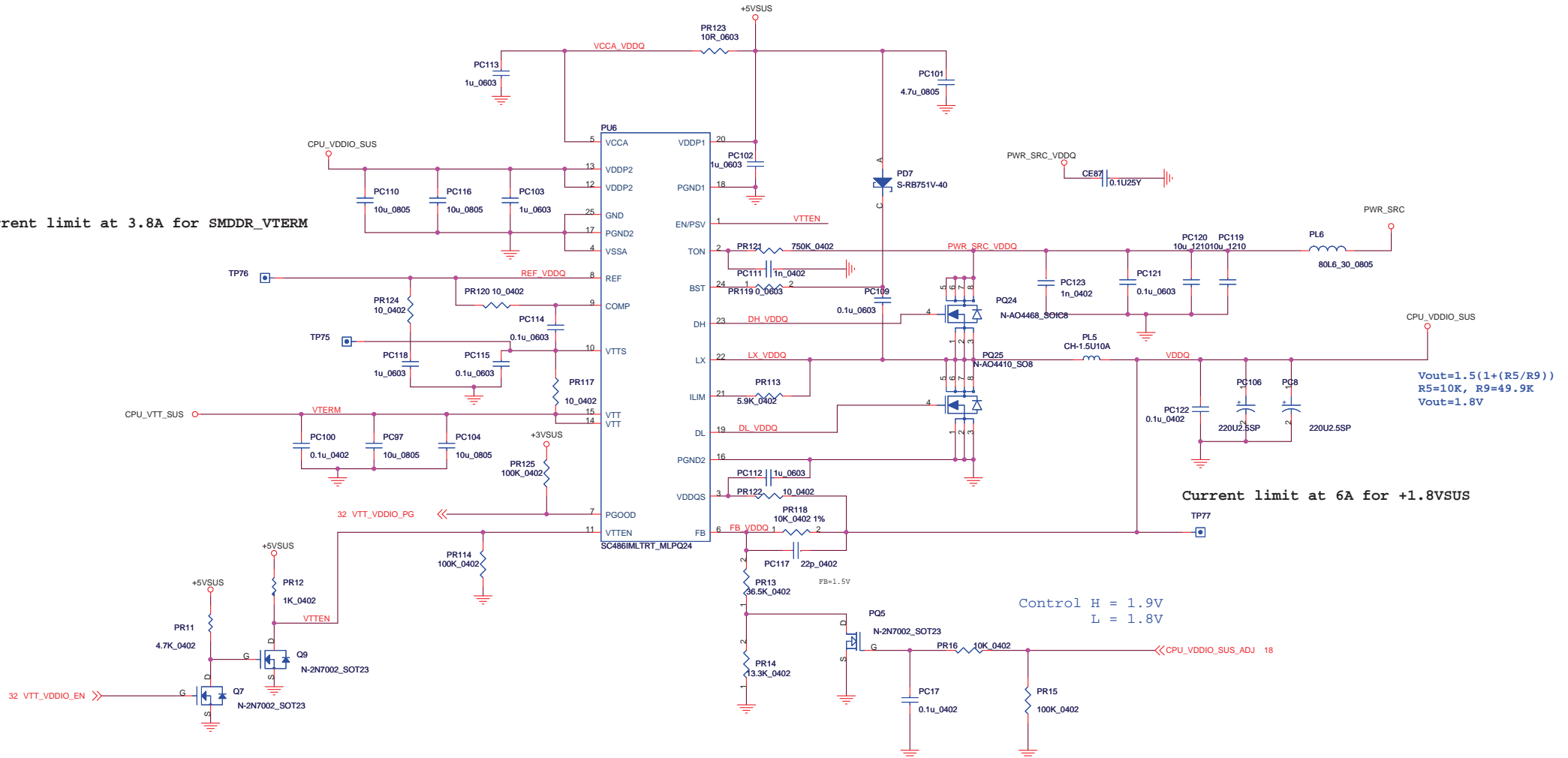
Current limit at 6A for +1.8VSUS


Control H = 1.9V
L = 1.8V

$$V_{out} = 1.5(1 + (R_5/R_9))$$

$$R_5 = 10K, R_9 = 49.9K$$

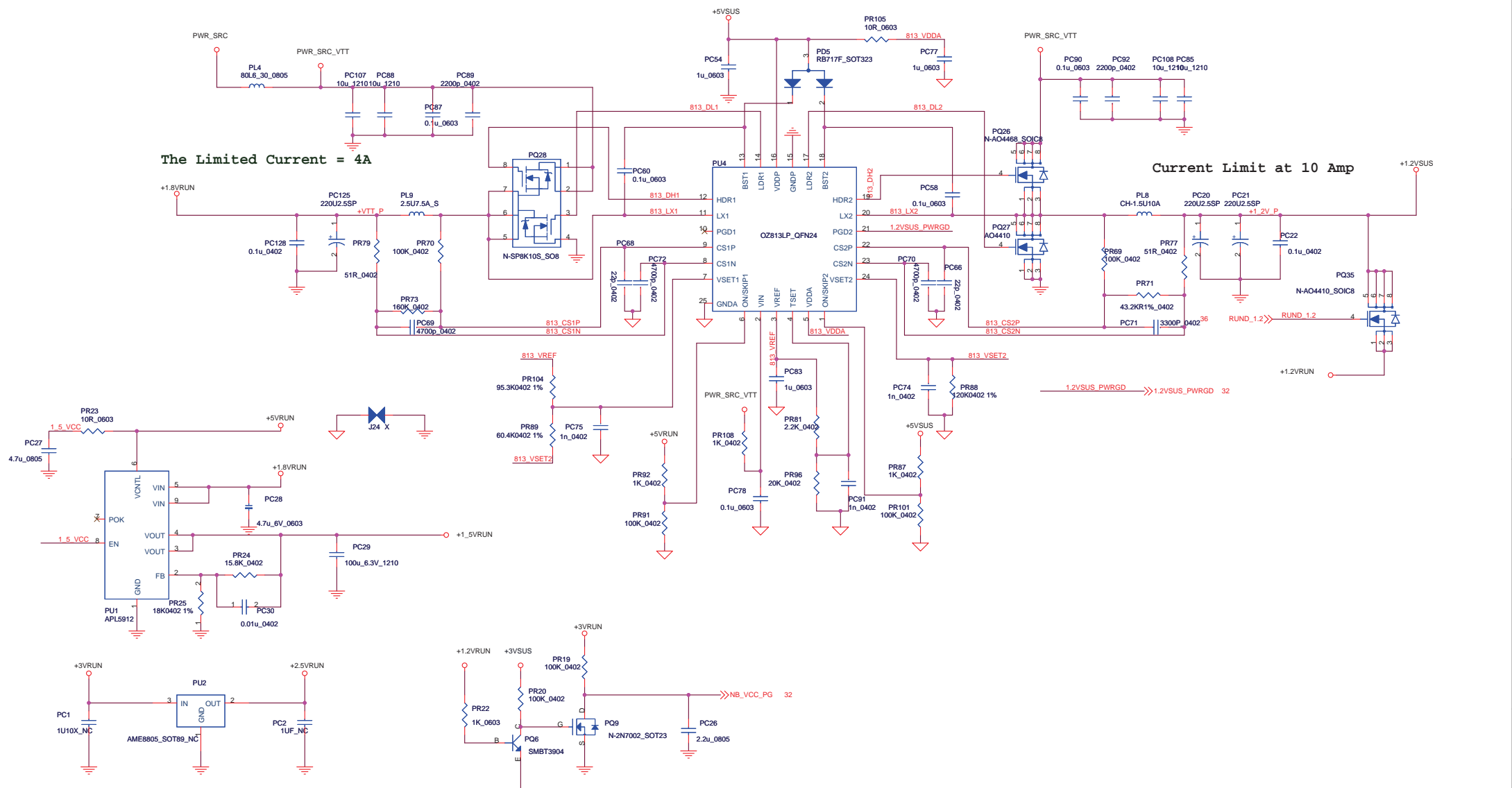
$$V_{out} = 1.8V$$



 MICRO-STAR INT'L CO.,LTD.	
Title DDR 2 1.8V VTT 0.9V	
Size	Document Number
Custom	MS-171A1
Date:	Friday, September 14, 2007
Sheet	37 of 48
Rev	10

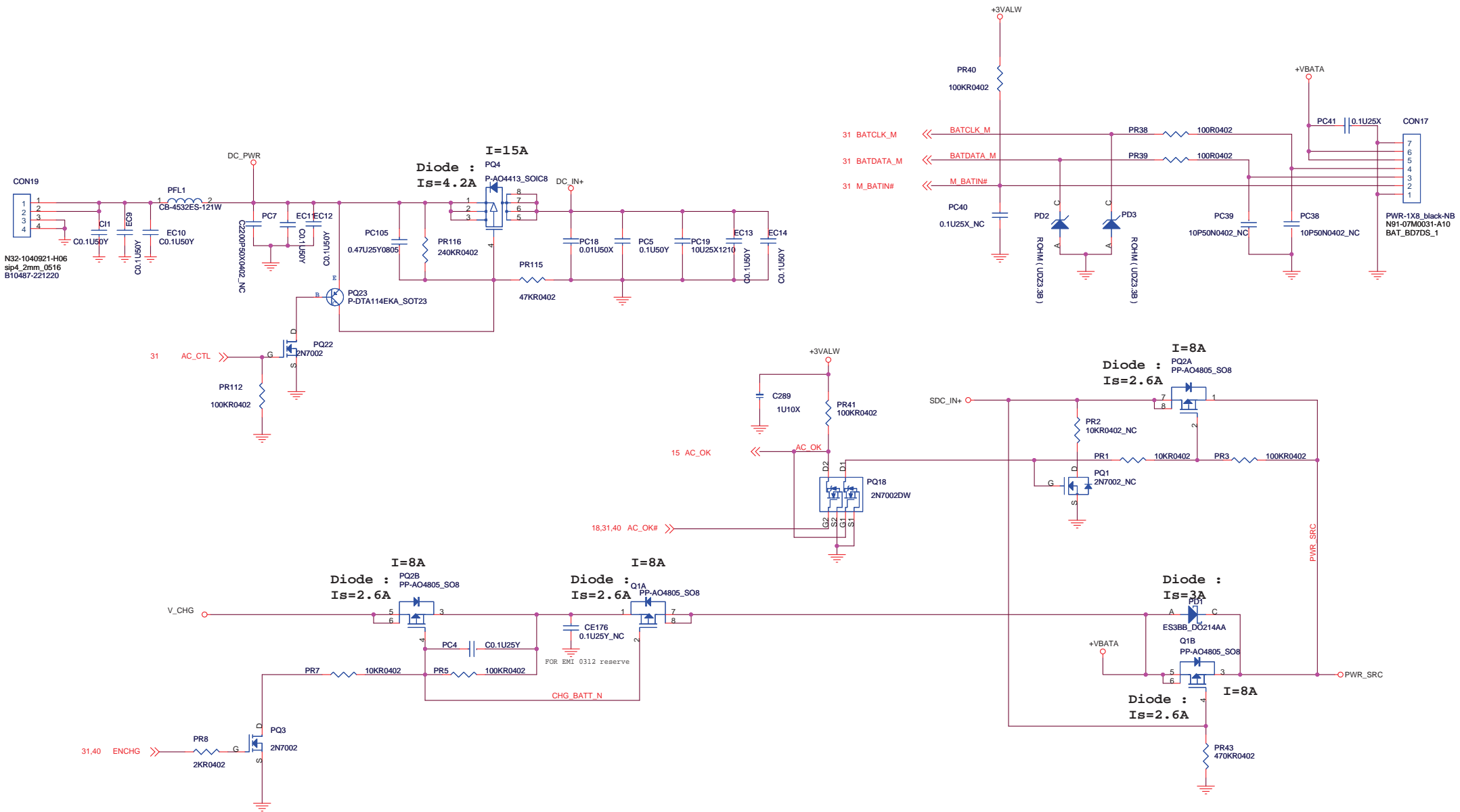
The Limited Current = 4A

Current Limit at 10 Amp



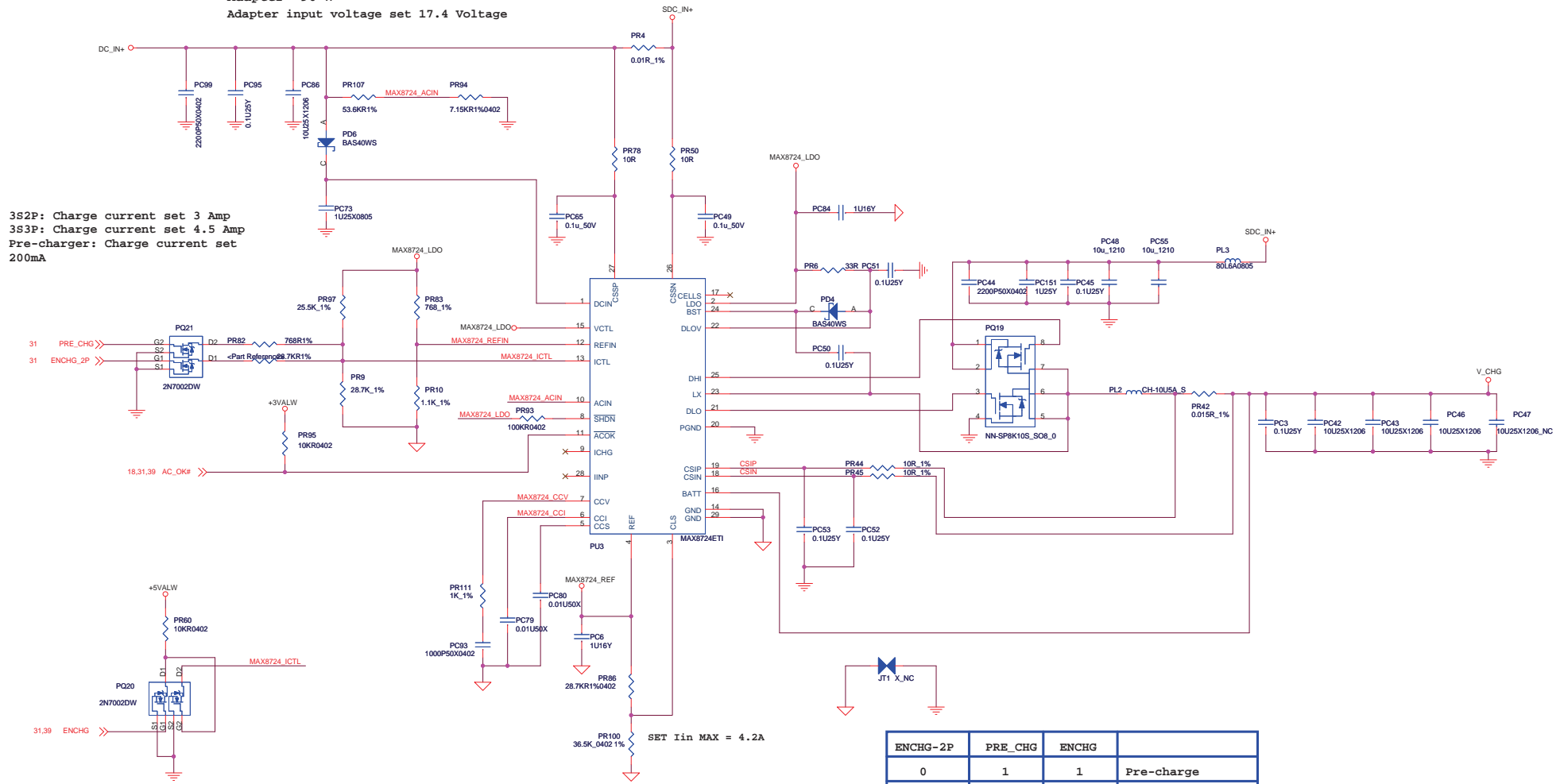
1/23 ADD +2.5VRUN LDO for MXMII
CLOSE TO MXMII CONN
STUFF FOR NVIDIA CARD

		MICRO-STAR INT'L CO.,LTD.	
Title: VCC_NB 1.2VSUS 1.5VRUN 1.8VRUN			
Size	Document Number	Rev	
Custom	MS-171A1	10	
Date:	Friday, September 14, 2007	Sheet	38 of 48



MSI MICRO-STAR INT'L CO.,LTD.	
Title Battery Select	
Size Custom	Document Number MS-171A1
Date: Thursday, October 04, 2007	Sheet 39 of 48
Rev 10	

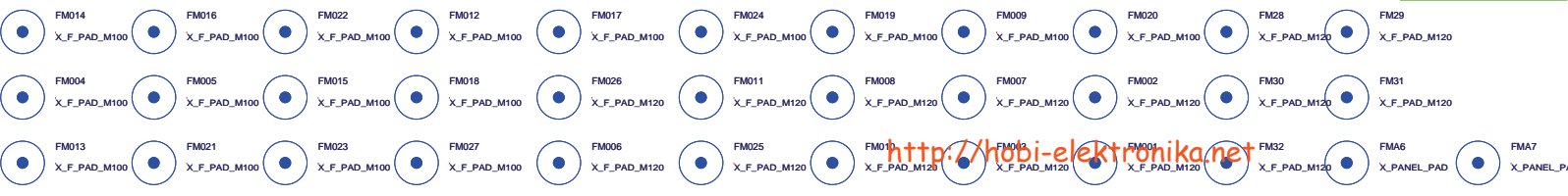
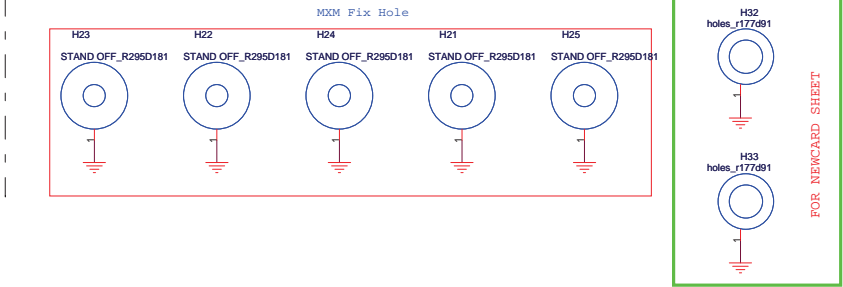
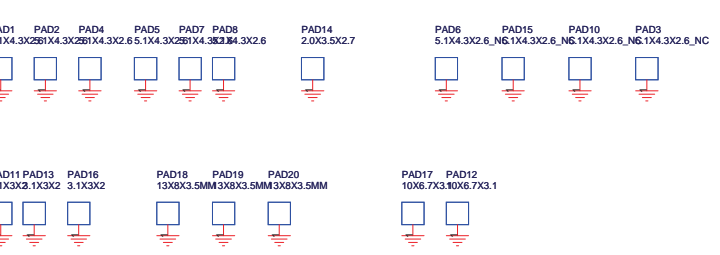
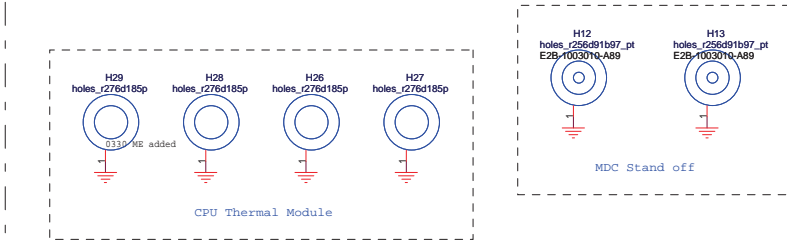
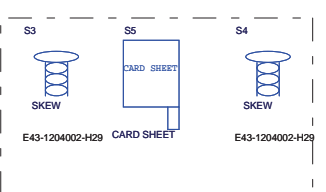
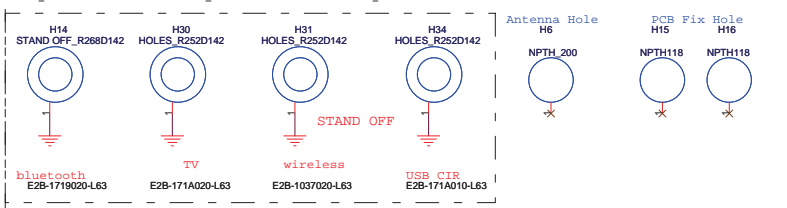
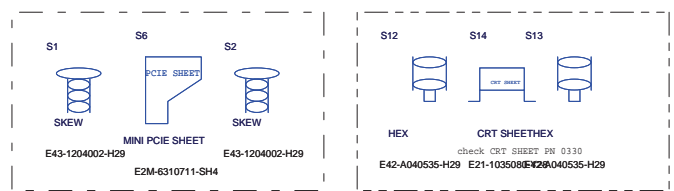
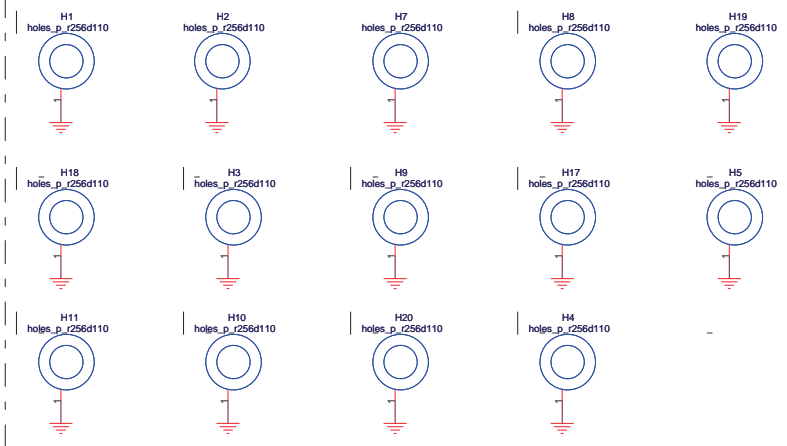
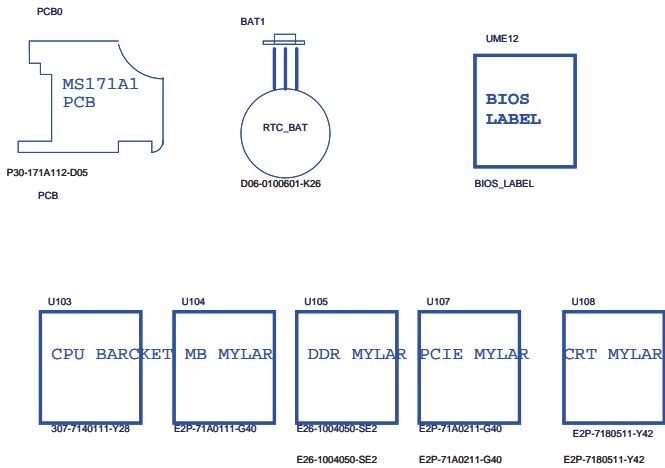
Adapter= 90 W
 Adapter input voltage set 17.4 Voltage



3S2P: Charge current set 3 Amp
 3S3P: Charge current set 4.5 Amp
 Pre-charger: Charge current set 200mA


SET Iin MAX = 4.2A

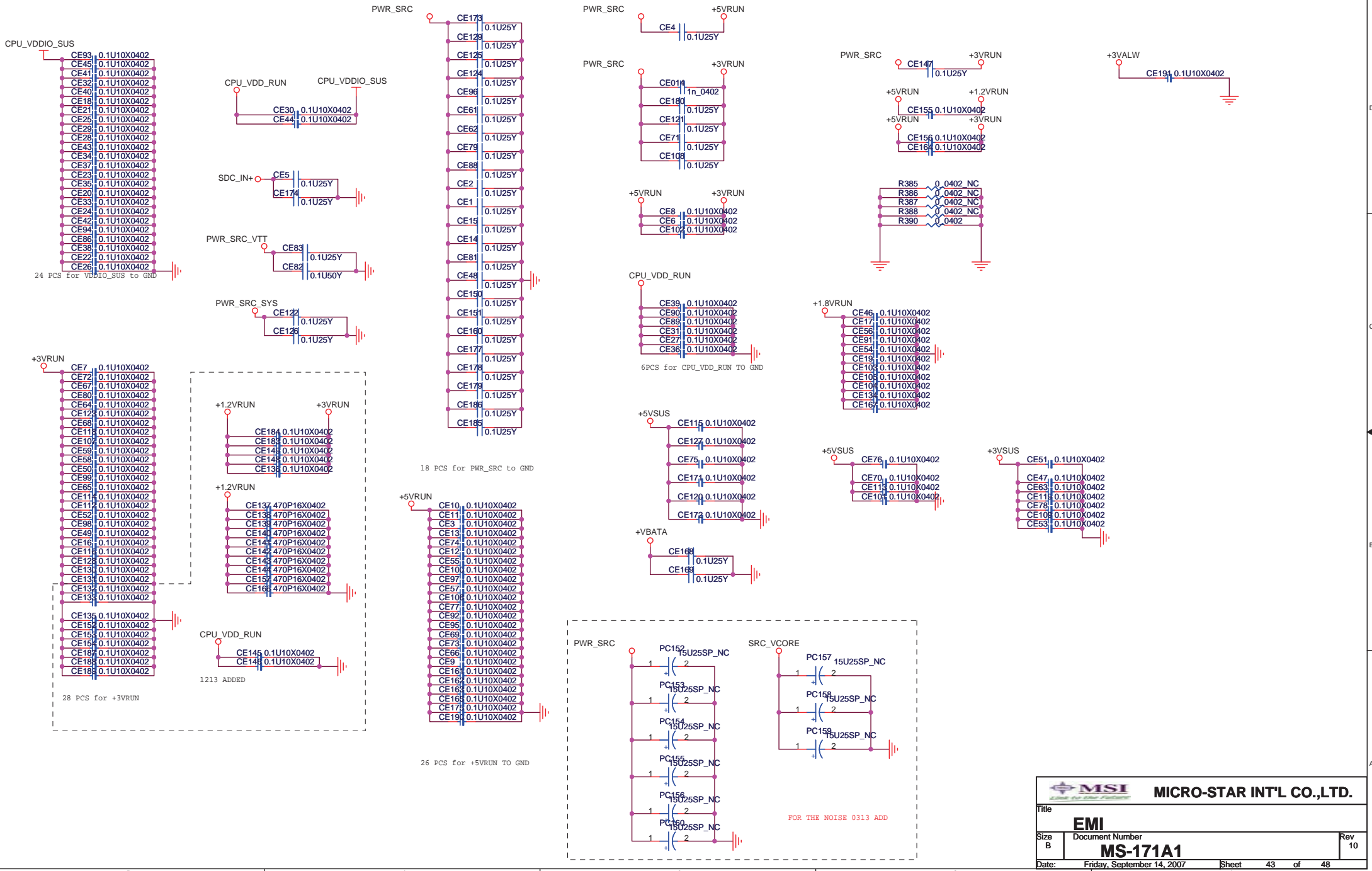
ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE




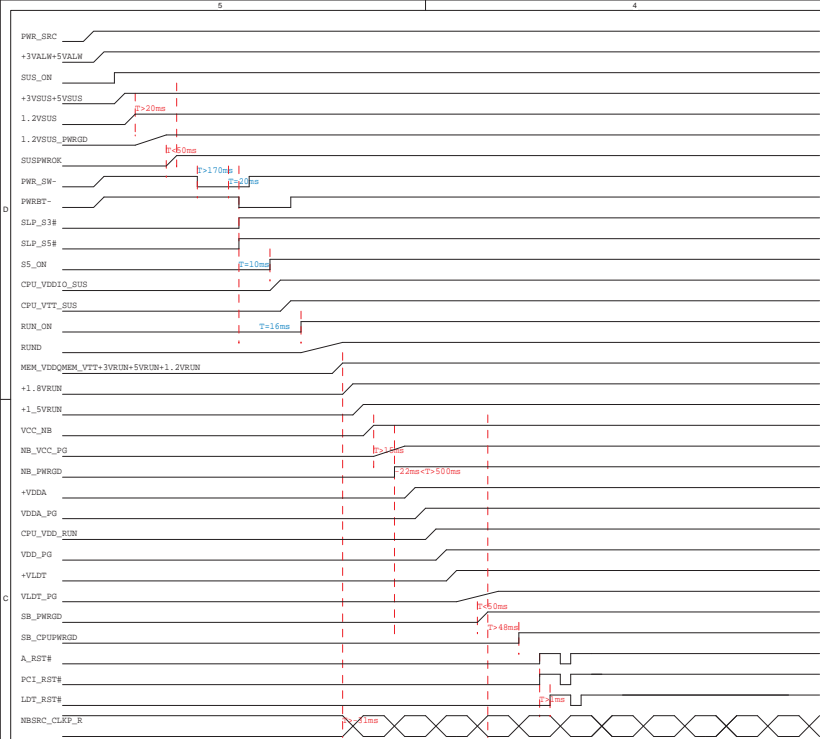
<http://hobi-elektronika.net>



 MICRO-STAR INT'L CO.,LTD.	
Title	
IMPEDANCE	
Size	Document Number
B	MS-171A1
Date:	Rev
Friday, September 14, 2007	10
Sheet	of
42	48

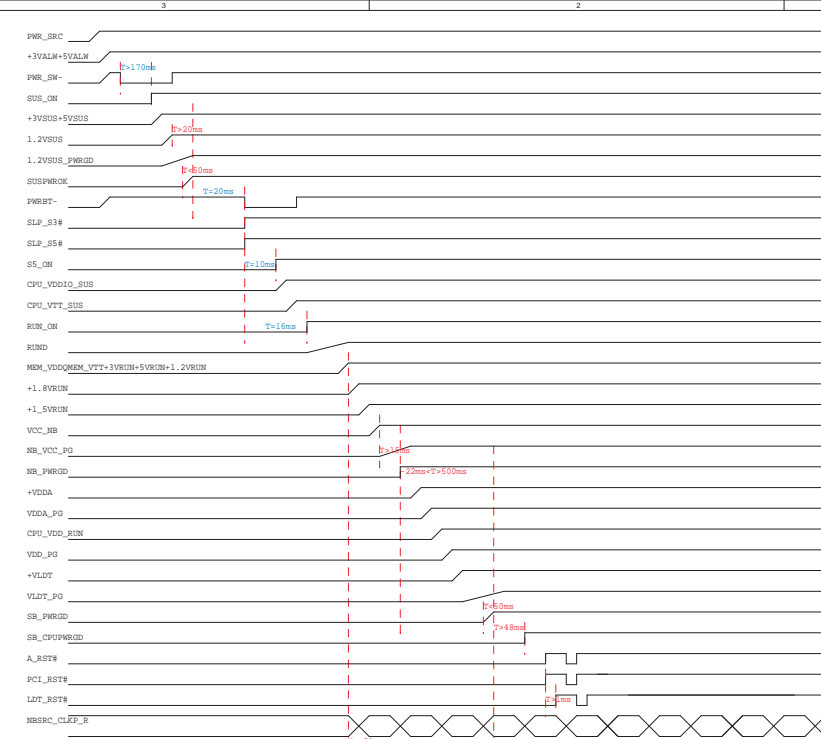


		MICRO-STAR INT'L CO.,LTD.	
Title			
EMI			
Size	Document Number		Rev
B	MS-171A1		10
Date:	Friday, September 14, 2007	Sheet	43 of 48

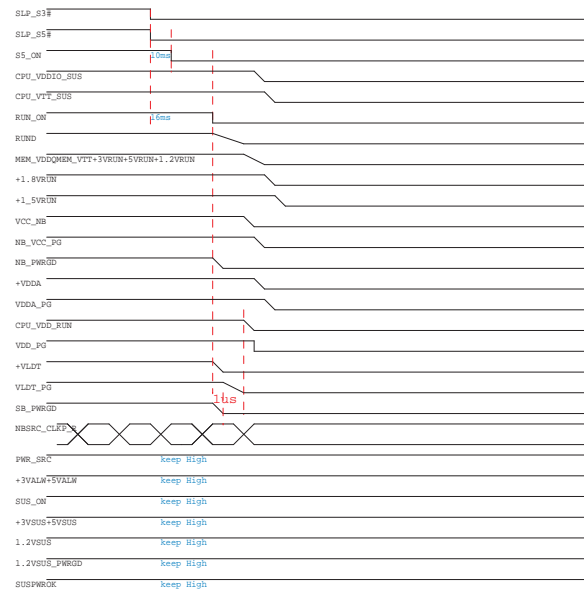


AC MODE S5----->S0

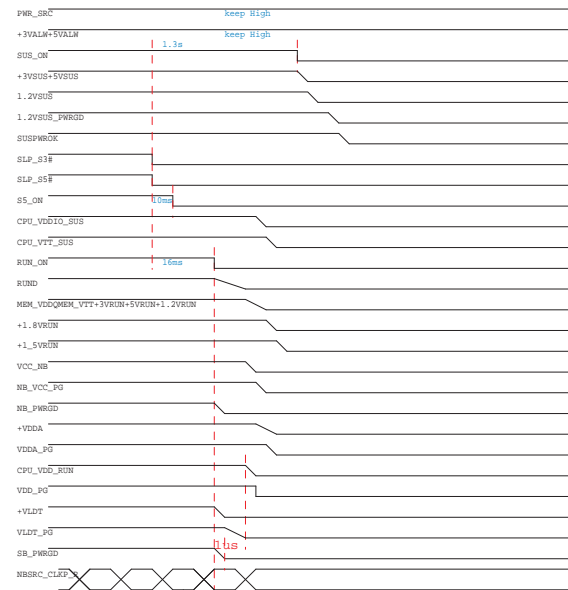
SUS_ON timing need by EC programming
690+600 timing SPEC



DC MODE S5----->S0

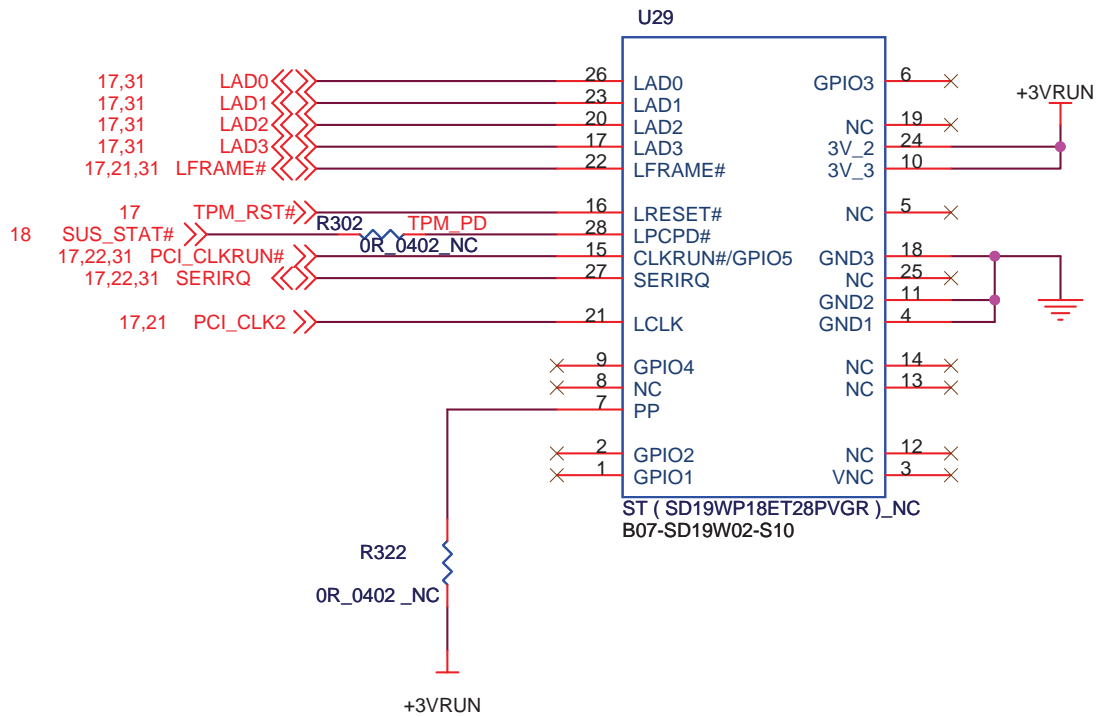


AC MODE S0----->S5




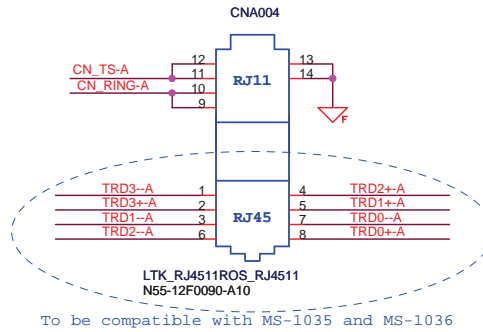
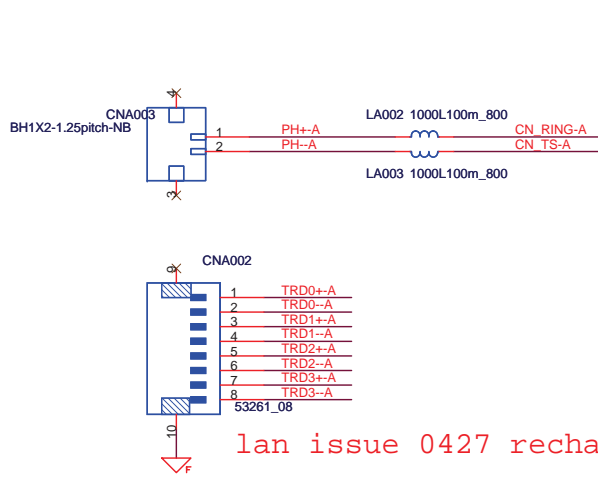
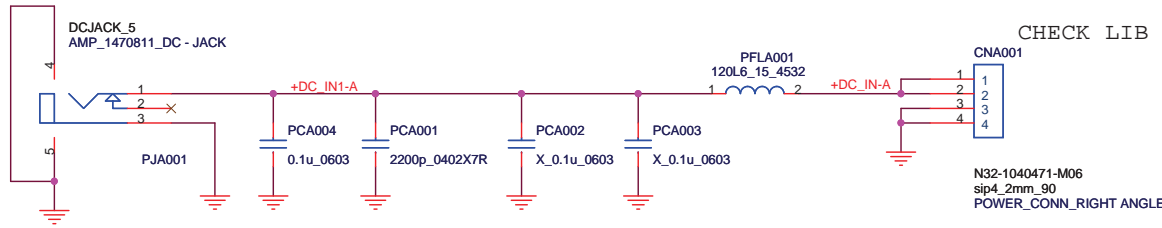
DC MODE S0----->S5

<http://hobi-elektronika.net>



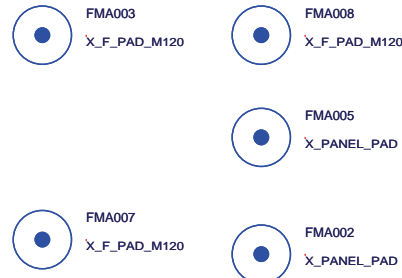
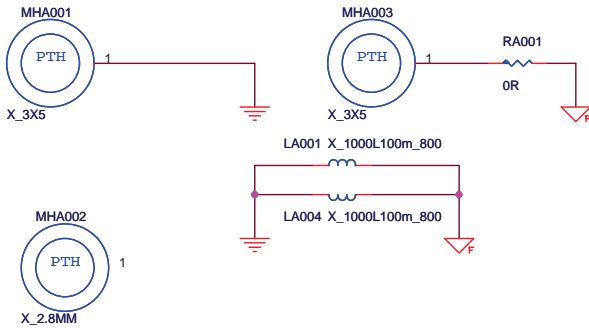
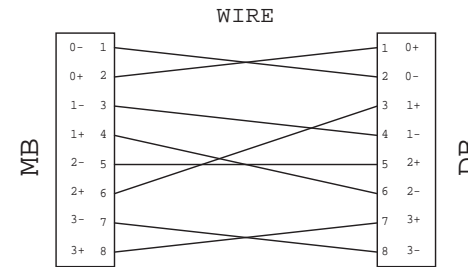
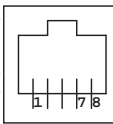
<http://hobi-elektronika.net>

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Title	
TPM (ST19WP18-TPM-C)	
Size	Document Number
A	MS-171A1
Date:	Rev
Friday, September 14, 2007	10
Sheet	of
45	48

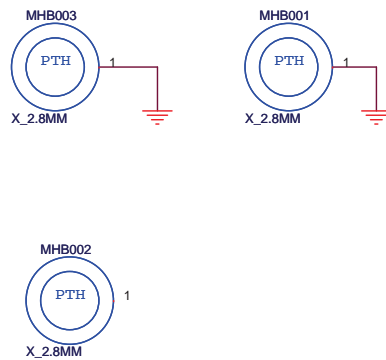
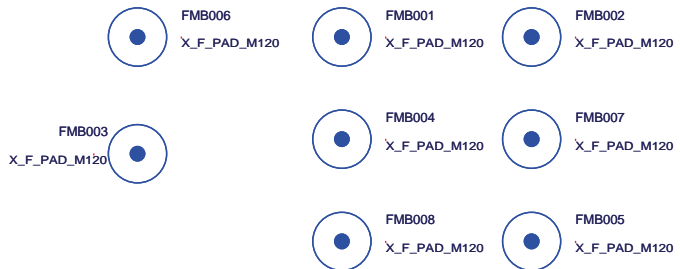
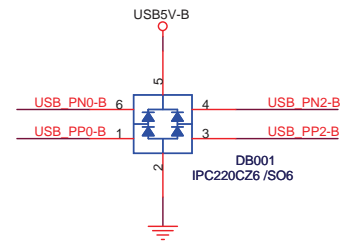
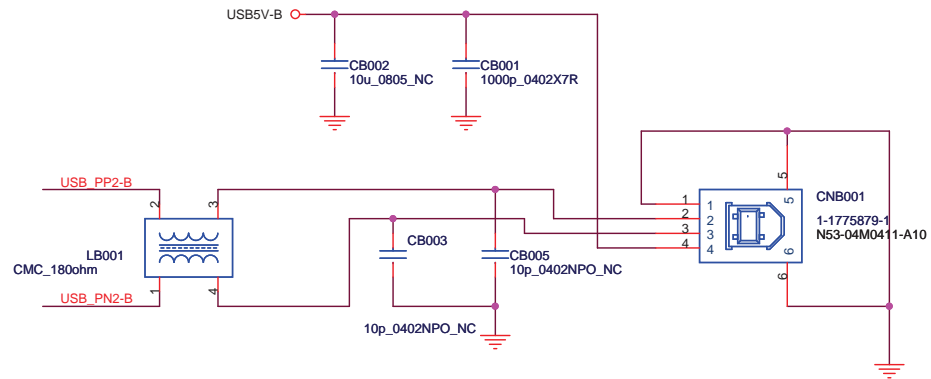
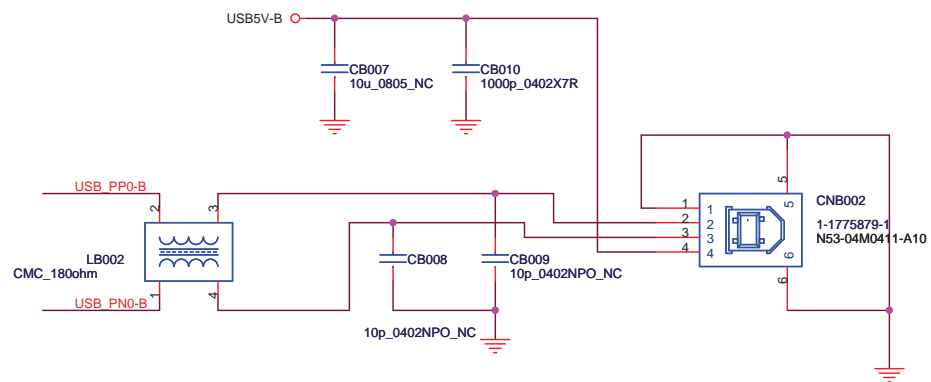
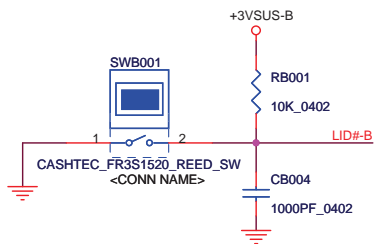
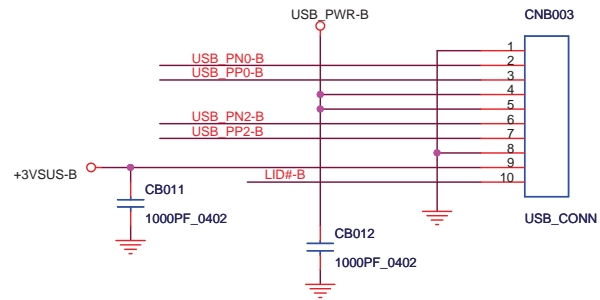
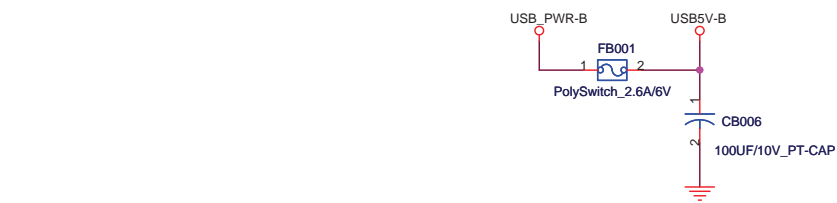



RJ45 Pin define

- 1 TRD3-
- 2 TRD3+
- 3 TRD1-
- 4 TRD2-
- 5 TRD2+
- 6 TRD1+
- 7 TRD0-
- 8 TRD0+



		MICRO-STAR INT'L CO.,LTD.	
Title			
DC-IN Daughterboard			
Size	Document Number		Rev
B	MS-171AA		10
Date:	Friday, September 14, 2007	Sheet	46 of 48



 MICRO-STAR INT'L CO.,LTD.	
Title Block diagram	
Size B	Document Number MS-171AB
Date: Friday, September 14, 2007	Rev 10
Sheet 47	of 48

1203/2006 0B begin ,copy from 171A1 0A 1115

1203/2006

change CN3 footprint to 53398_08

change c60 to 0.1uf 0402

REMOVE Q27,Q28,Q29,Q30,R265,R338 for MINI PCIE +3V connect to +3VRUN straightly.

change R295 to 22ohm 0402

change OR JUMPER footprint to NC_0402_6

add 8M ROM for support PBA function

1206/2006

stuff R121 for PCIE express Card GIGA LAN can't detect but scan the device manager can find and using.

1208/2006

delete NB CRT signal for RX690 have no internal graphic.

Add USB CIR decoder connector circuit.

1211/2006

delete VID pull high resistor

0301/2007

change A_RST# buffer to +3VSUS.

delete CODEC +3v power filter ,connect to +3VRUN by 0 ohm

using new jump for SMT jointing,G1G2,G3,G3,G5,G6 need paste.G7 needn't

AVDD change to +3.3V

DELETE PC13,PC25,C71,C121,C122 CPU POWER.for cost down

on audio page ,add all EMI bypass capacitor,and one resistor instead of bead.

0514/2007

1.0 begian.copy from 171A10C0329

modify D13 power source to USB5V_A


add HDMI I2C switch circuit for HDMI 5V tolerance

5V HDMI power change to a fuse delivery instead of diode

delete EC1,EC2 for HDMI DATA/CLK DUT off fail

0709/2007

ADD EMI solution

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Title	
IMPEDANCE	
Size	Document Number
B	MS-171A1
Date:	Friday, September 14, 2007
Sheet	48 of 48
Rev	10