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SUZHOU-D

CPU : AMD Caspin
Chip Set : AMD RX881+SB710
Remarks : Tigris Platform

Model Name : Suzhou-D
PBA Name : MAIN
PCB Code : GCE :
 NAN :
 HAN :
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.11.10

Design	CHECK	APPROVAL
XIE BIN	GUO LEI	BC LEE

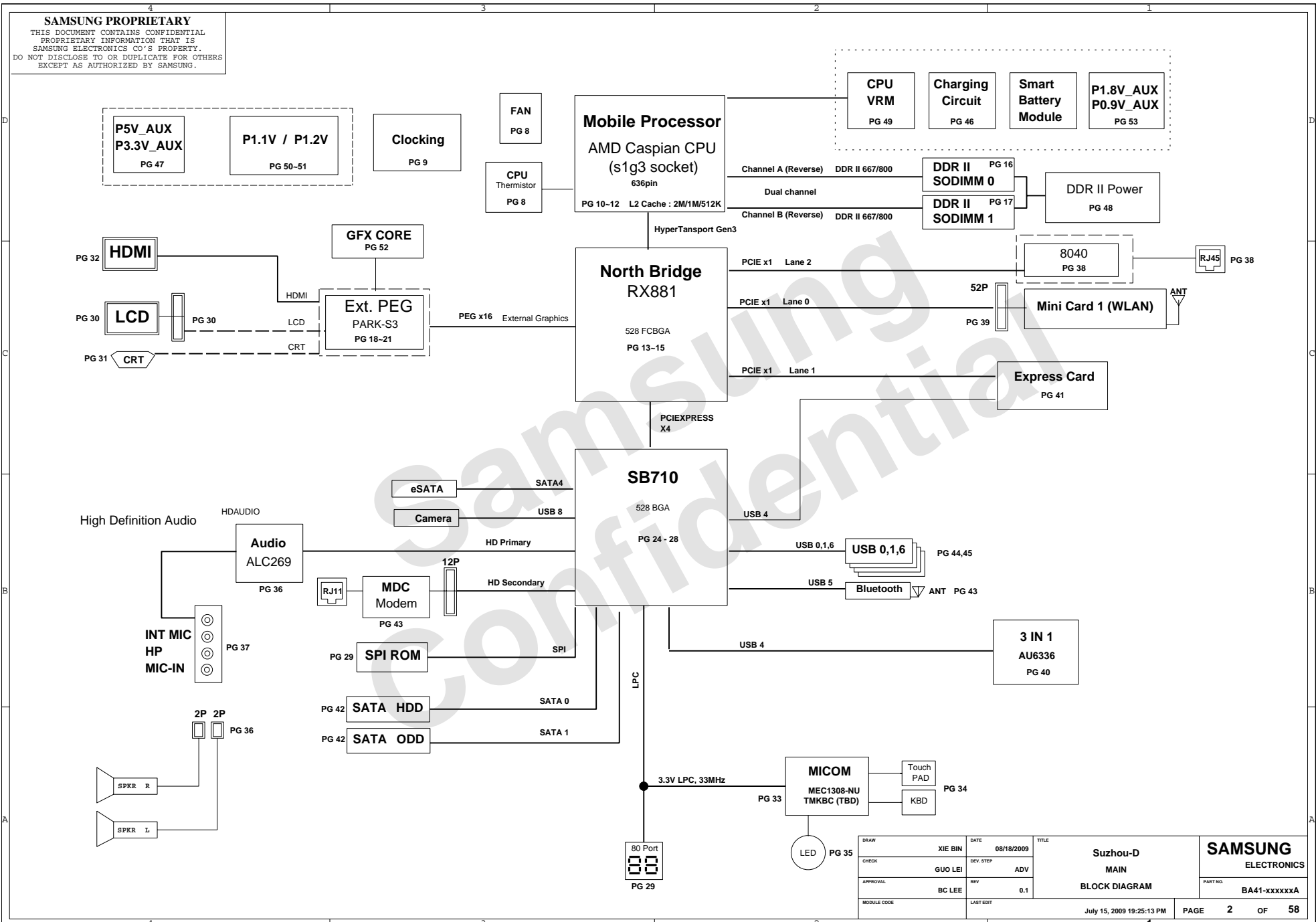
Owner : SEC Mobile R & D Signature : X

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DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV.STEP	ADV	MAIN		
APPROVAL	BC LEE	REV	0.1	COVER	PART NO.	
MODULE CODE		LAST EXT			BA41-xxxxxxA	
				July 15, 2009 19:25:13 PM	PAGE	1 OF 58

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DRAW	XIE BIN	DATE	TITLE	Suzhou-D MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS	
CHECK	GUO LEI	DEV. STEP	ADV			PART NO.
APPROVAL	BC LEE	REV	0.1			BA41-xxxxxA
MODULE CODE		LAST EXT				
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE0	Core Voltage for CPU
CPU_CORE1	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.1V	VTT for M92_RX881
P1.2V	Core Voltage for SB710
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V_AUX	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_STB	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB710	Real Time Clock
Crystal	10MHz	MICOM	MEC1308-NU
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	88E8040
Crystal	25MHz	SATA	SB710

I²C / SMB Address

Devices	Address	Hex	Bus
SB710	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	NC
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	EXPRESS CARD

PCI Express Assign

PORT #	ASSIGNED TO
0	Mini Card (WLAN)
1	EXPRESS CARD
2	LOM
3	NC
4	NC
5	NC

LCD Panel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0(strap0)

REVISION HISTORY

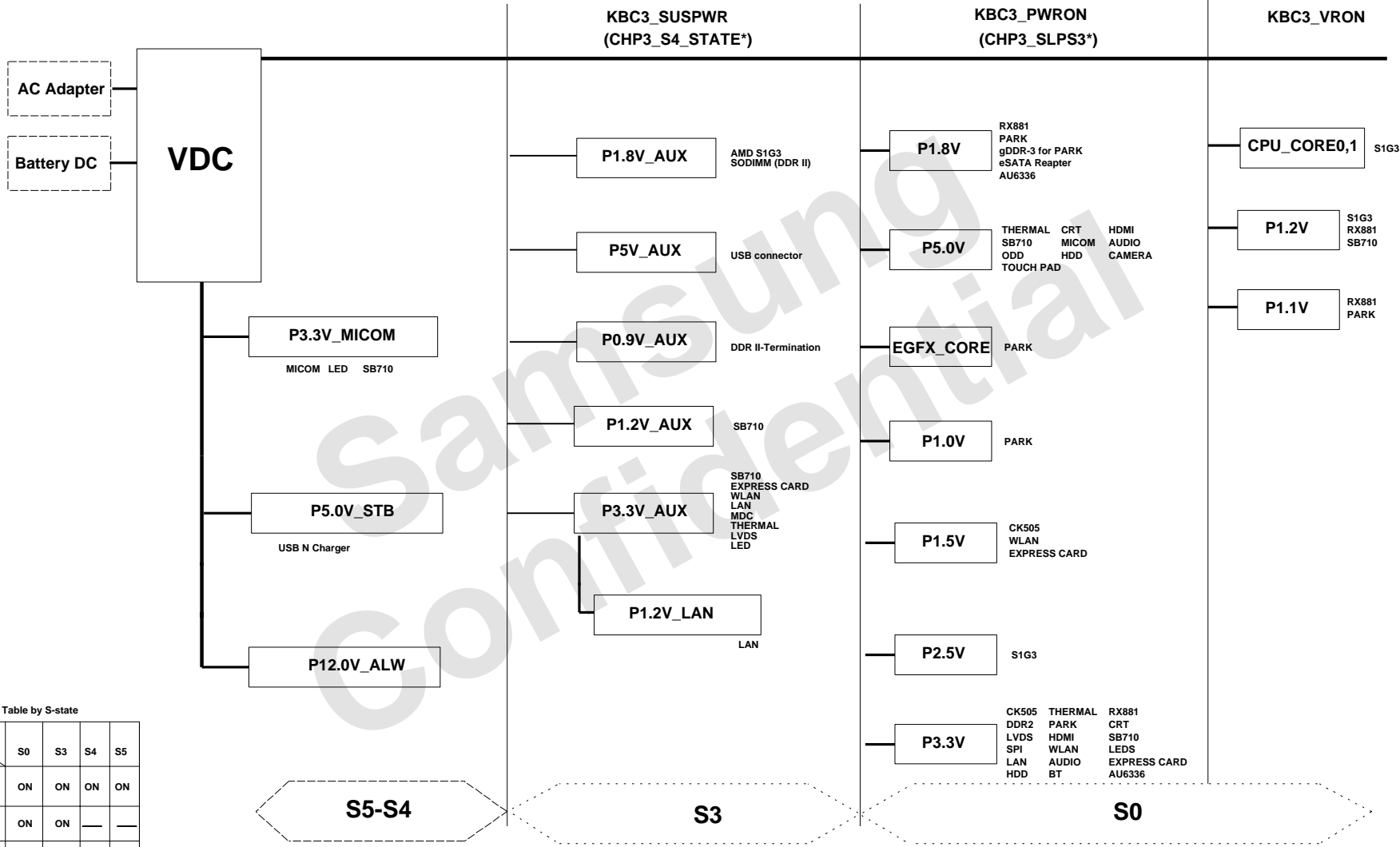
See rev notes for more information.

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CHECK	GUO LEI	DEV. STEP	ADV	MAIN		
APPROVAL	BC LEE	REV	0.1	BOARD INFORMATION	PART NO.	BA41-xxxxxA
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POWER DIAGRAM

Rev 0.1

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Power On/Off Table by S-state

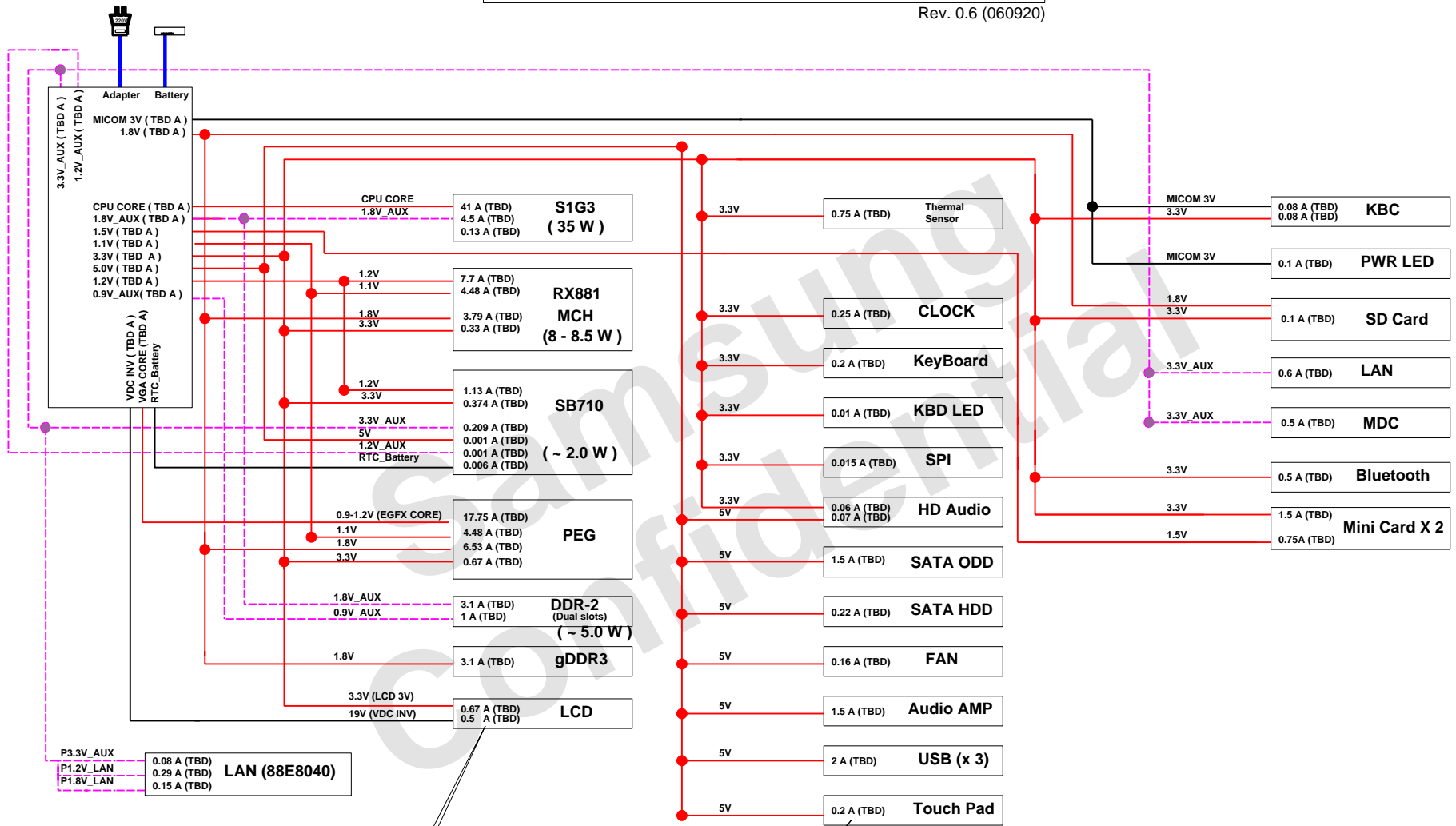
Rail \ State	S0	S3	S4	S5
+V*(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	---	---
+1.8V_AUX	ON	ON	---	---
+0.9V_AUX	ON	ON	---	---
+V*AUX	ON	ON	---	---
+V	ON	---	---	---
+V* (CORE)	ON	---	---	---

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D MAIN	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	POWER DIAGRAM	PART NO. BA41-xxxxxA	
APPROVAL	BC LEE	REV	0.1	July 15, 2009 19:25:13 PM	PAGE	4 OF 58
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POWER RAILS ANALYSIS

Rev. 0.6 (060920)

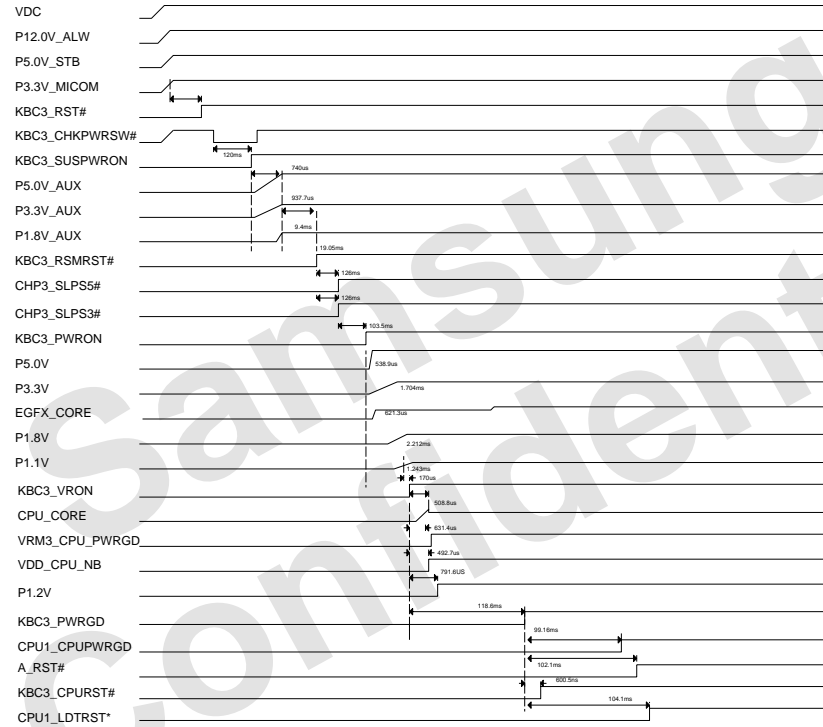


Value by Datasheet/Application notes (Value by measurement)

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MAIN		
APPROVAL	BC LEE	REV	0.1	POWER RAILS ANALYSIS	PART NO.	BA41-xxxxxA
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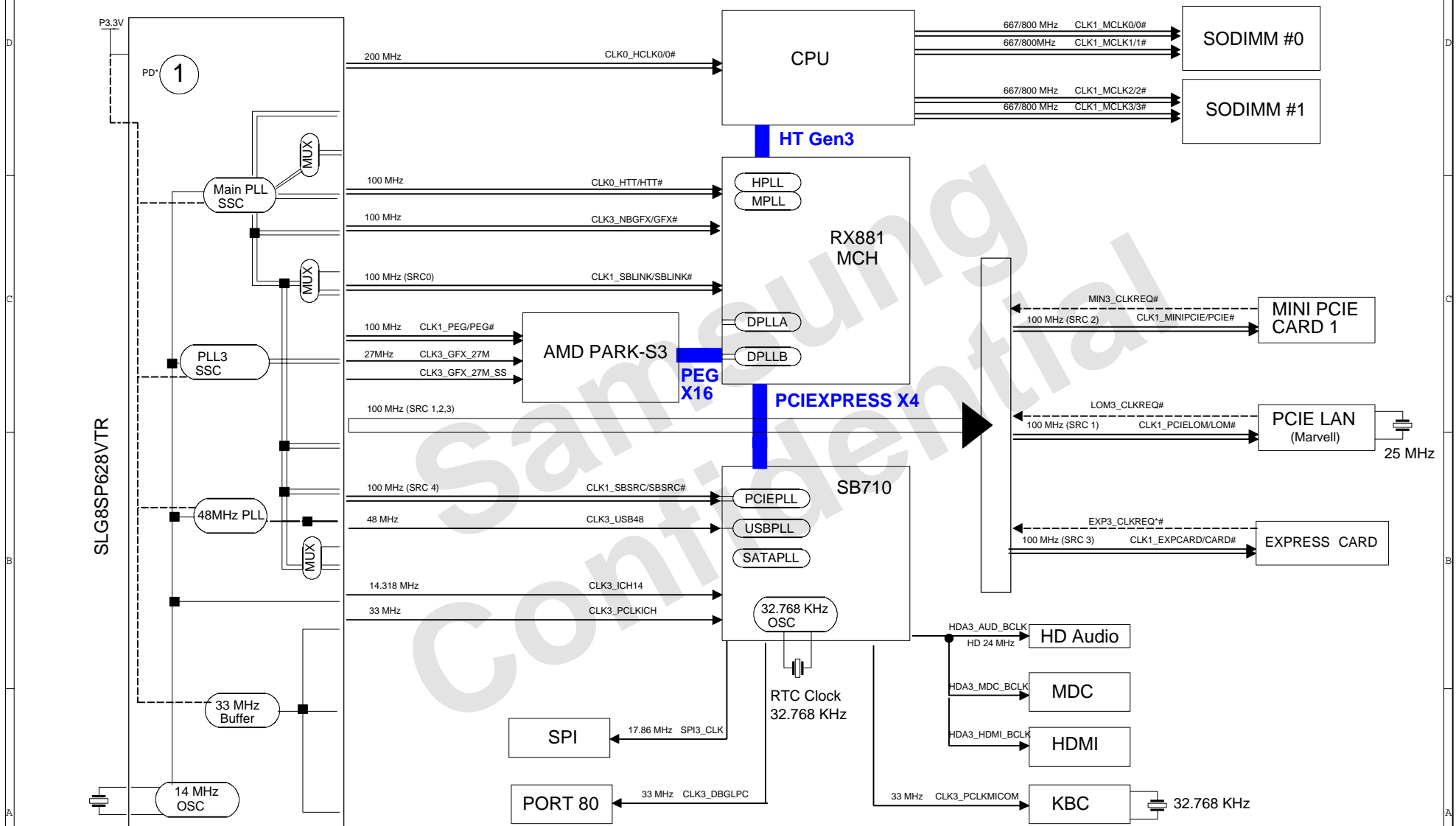
Timing Diagram, Power ON Rev..1.0 2009-08-27



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APPROVAL	BC LEE	REV	0.1	TIMING DIAGRAM	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	6	OF 58

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CLOCK DISTRIBUTION



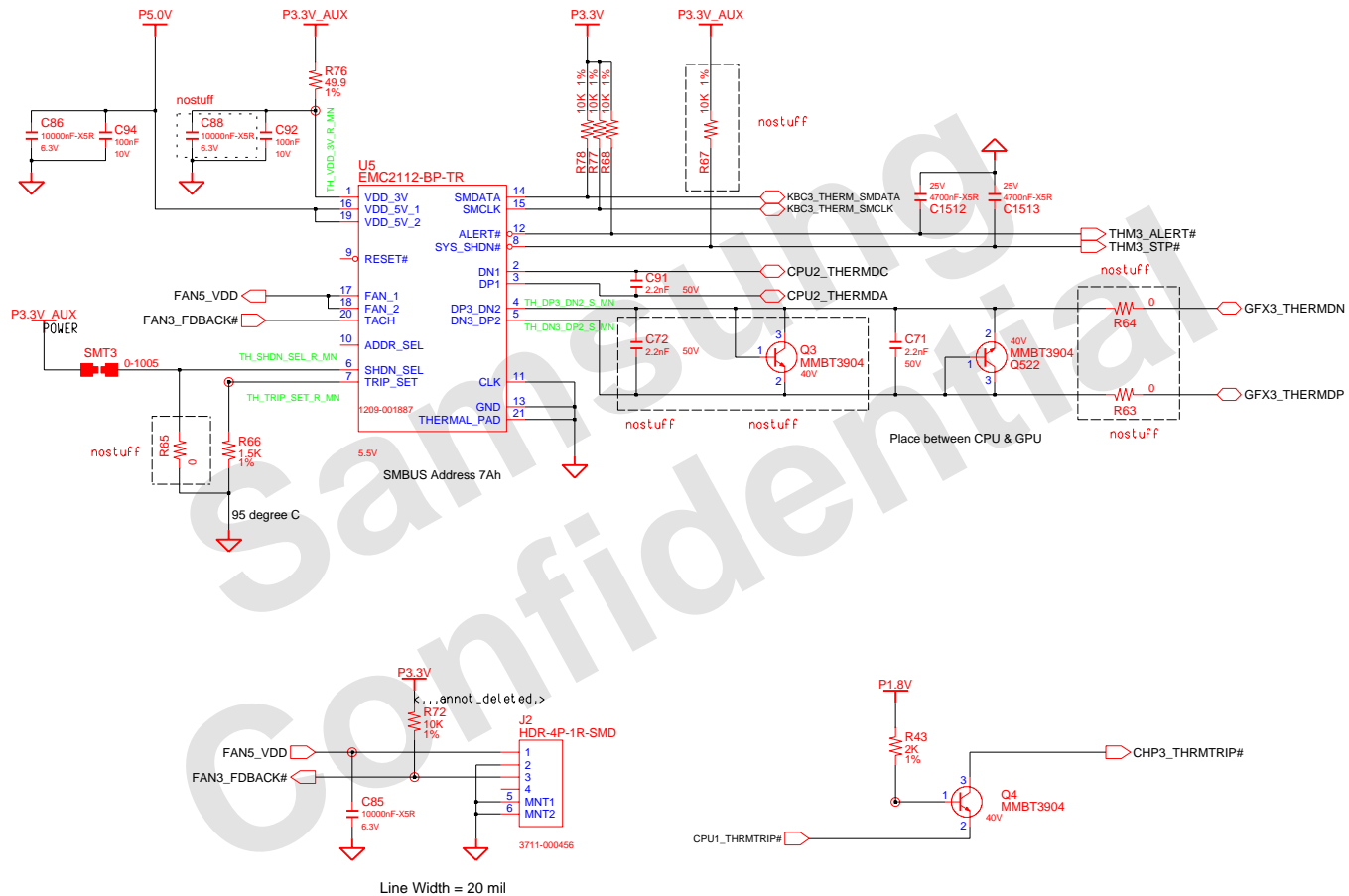
14.318 MHz

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MAIN	MAIN	
APPROVAL	BC LEE	REV	0.1	CLOCK DISTRIBUTION	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EXT		July 15, 2009 19:25:13 PM	PAGE	7 OF 58

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THERMAL SENSOR & FAN CONTROL



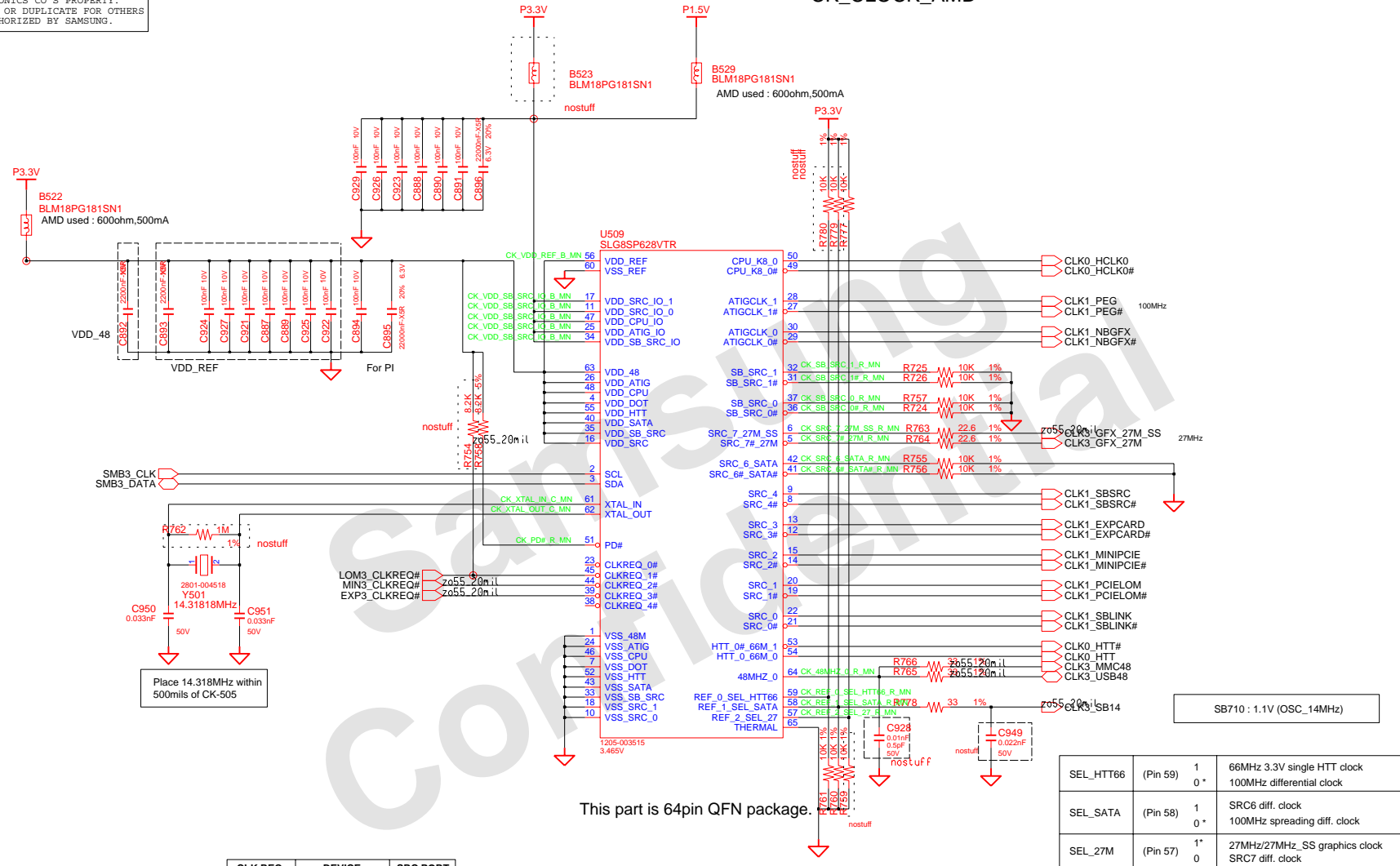
SHDN_SEL MODE	
0	CH1(CPU MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	THERMAL SENSOR		
APPROVAL	BC LEE	REV	0.1	EMC2112	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	8	OF 58

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CK_CLOCK_AMD



This part is 64pin QFN package.

CLK REQ	DEVICE	SRC PORT
CLK REQ 0	-	SB Link
CLK REQ 1	LOM3_CLKREQ#	LOM
CLK REQ 2	MIN3_CLKREQ#	MINI CARD
CLK REQ 3	EXP3_CLKREQ#	EXP CARD
CLK REQ 4	-	SB_SRC

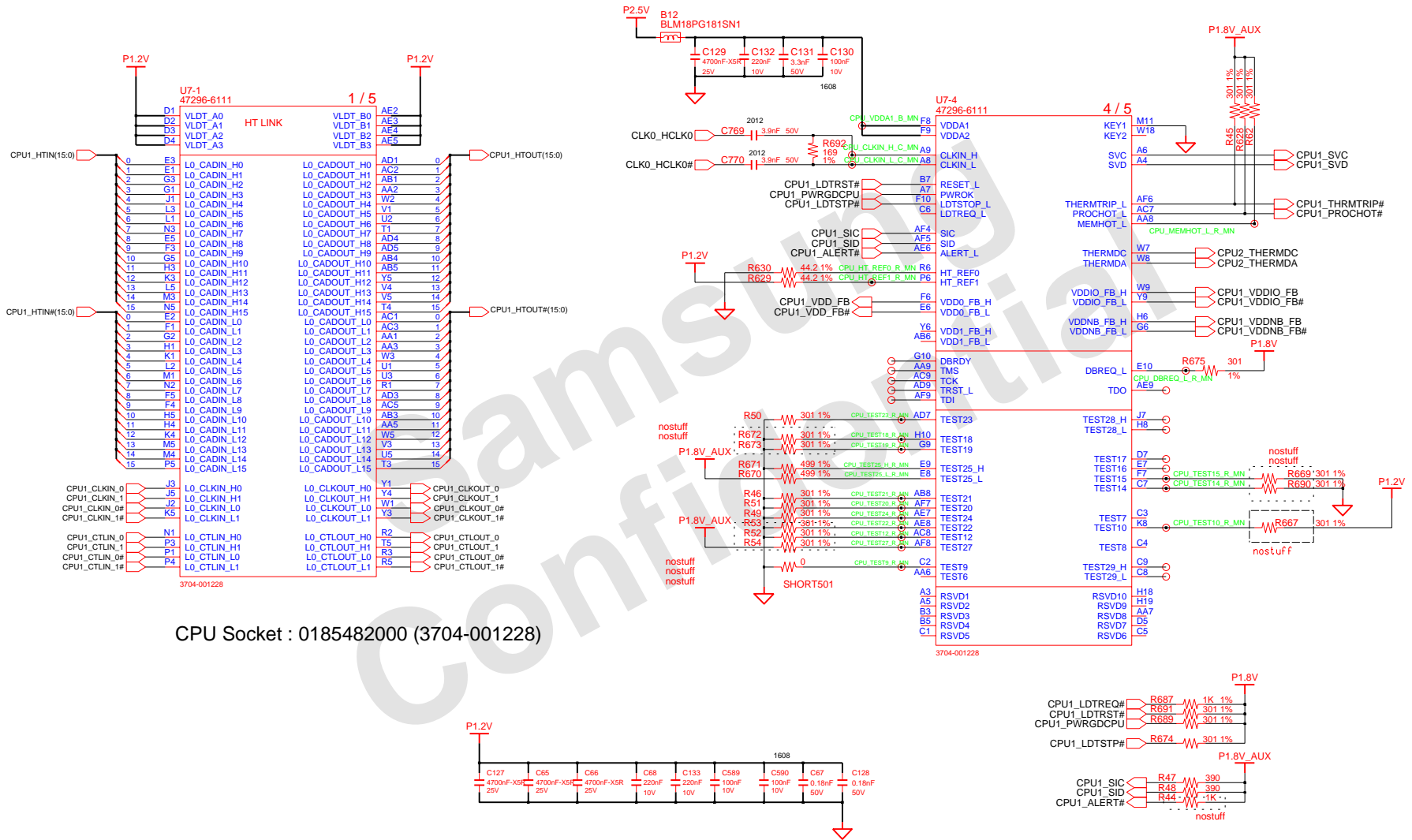
SEL_HTT66	(Pin 59)	1 0 *	66MHz 3.3V single HTT clock 100MHz differential clock
SEL_SATA	(Pin 58)	1 0 *	SRC6 diff. clock 100MHz spreading diff. clock
SEL_27M	(Pin 57)	1* 0	27MHz/27MHz_SS graphics clock SRC7 diff. clock

DRAW	XIE BIN	DATE	TITLE	Suzhou-D Main_Clock_Circuit CK for AMD CPU	SAMSUNG ELECTRONICS
CHECK	GUO LEI	08/18/2009	ADV		
APPROVAL	BC LEE	REV	0.1	July 15, 2009 19:25:13 PM	PAGE 9 OF 58
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CPU_Caspian

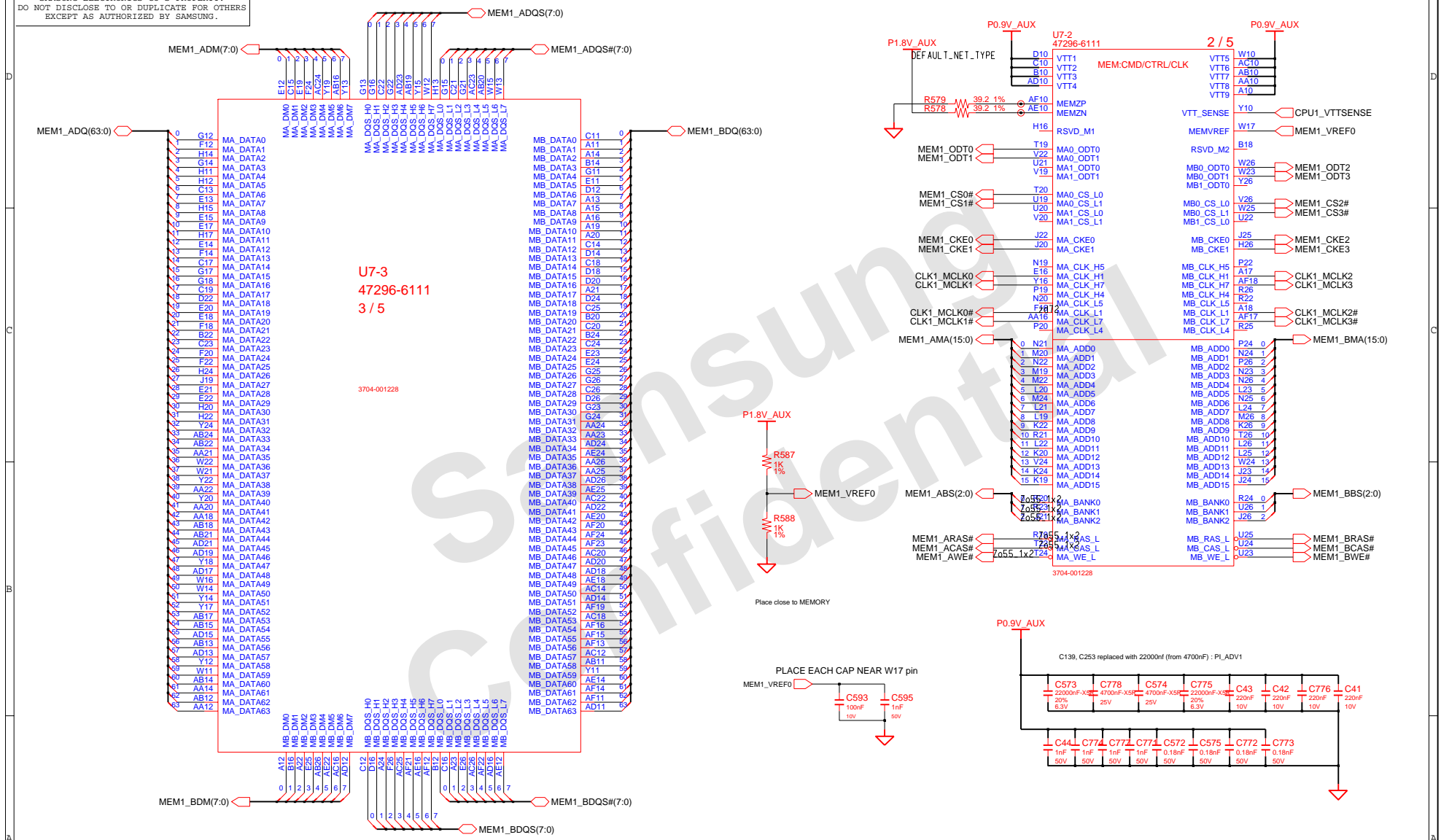


CPU Socket : 0185482000 (3704-001228)

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D
CHECK	GUO LEI	DEV.STEP	ADV		Caspian CPU
APPROVAL	BC LEE	REV	0.1		S1G3 CPU (1/3)
MODULE CODE		LAST EDIT			
					July 15, 2009 19:25:13 PM
					PAGE 10 OF 58

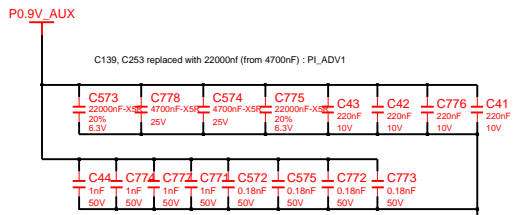
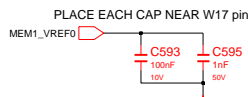
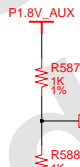
SAMSUNG
ELECTRONICS
PART NO.
BA41-xxxxxA

CPU_Caspian



U7-3
 47296-6111
 3 / 5
 3704-001228

3704-001228

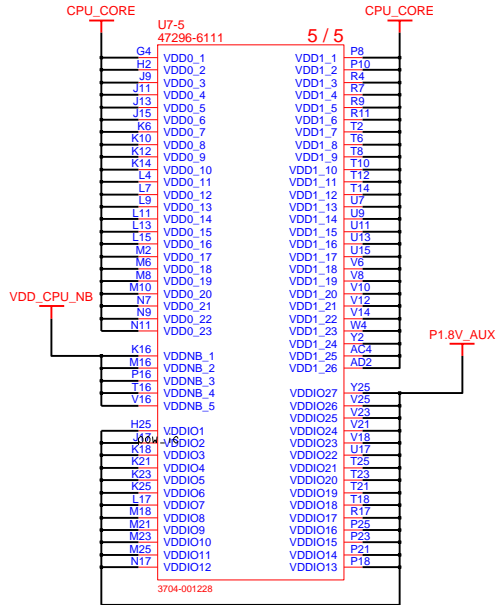


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CHECK	GUO LEI	DEV. STEP	ADV		Caspian CPU		ELECTRONICS	
APPROVAL	BC LEE	REV	0.1		S1G3 CPU (2/3)		PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDT			July 15, 2009 19:25:13 PM	PAGE	11	OF 58

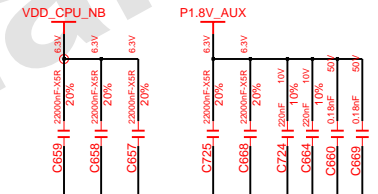
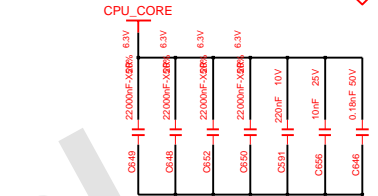
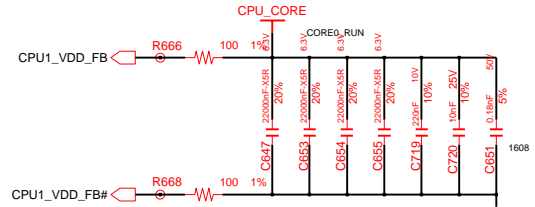
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CPU_Caspian

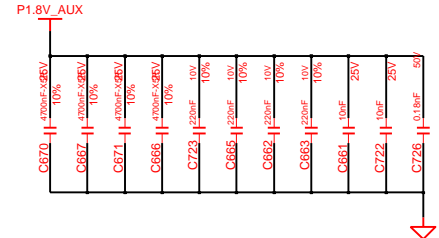


AA4	VSS1	VSS66	J6
AA11	VSS2	VSS67	J10
AA13	VSS3	VSS68	J12
AA15	VSS4	VSS69	J14
AA17	VSS5	VSS70	J16
AA19	VSS6	VSS71	J18
AB2	VSS7	VSS72	J2
AB7	VSS8	VSS73	K7
AB9	VSS9	VSS74	K9
AB23	VSS10	VSS75	K11
AB25	VSS11	VSS76	K13
AC11	VSS12	VSS77	K15
AC13	VSS13	VSS78	K17
AC15	VSS14	VSS79	K19
AC17	VSS15	VSS80	L6
AC19	VSS16	VSS81	L8
AD6	VSS17	VSS82	L12
AD8	VSS18	VSS83	L14
AD25	VSS19	VSS84	L16
AE11	VSS20	VSS85	L18
AE13	VSS21	VSS86	M7
AE15	VSS22	VSS87	M9
AE17	VSS23	VSS88	AC6
AE19	VSS24	VSS89	AM7
AE21	VSS25	VSS90	M17
AE23	VSS26	VSS91	N8
B4	VSS27	VSS92	N10
B6	VSS28	VSS93	N16
B8	VSS29	VSS94	N18
B9	VSS30	VSS95	P2
B11	VSS31	VSS96	P7
B13	VSS32	VSS97	P17
B15	VSS33	VSS98	P11
B17	VSS34	VSS99	R8
B19	VSS35	VSS100	R9
B21	VSS36	VSS101	R10
B23	VSS37	VSS102	R16
B25	VSS38	VSS103	R18
D6	VSS39	VSS104	T7
D8	VSS40	VSS105	T9
D9	VSS41	VSS106	T11
D11	VSS42	VSS107	T13
D13	VSS43	VSS108	T15
D15	VSS44	VSS109	T17
D17	VSS45	VSS110	U4
D19	VSS46	VSS111	U6
D21	VSS47	VSS112	U8
D23	VSS48	VSS113	U10
D25	VSS49	VSS114	U12
E4	VSS50	VSS115	U14
F1	VSS51	VSS116	U16
F2	VSS52	VSS117	U18
F11	VSS53	VSS118	V2
F15	VSS54	VSS119	V7
F17	VSS55	VSS120	V9
F19	VSS56	VSS121	V11
F21	VSS57	VSS122	V13
F23	VSS58	VSS123	V15
F25	VSS59	VSS124	V17
H7	VSS60	VSS125	W6
H9	VSS61	VSS126	W6
H21	VSS62	VSS127	Y21
H23	VSS63	VSS128	Y23
J4	VSS64	VSS129	N6
	VSS65		



Bottom side decoupling

Decoupling between processor and Memory
Place close to processor as possible

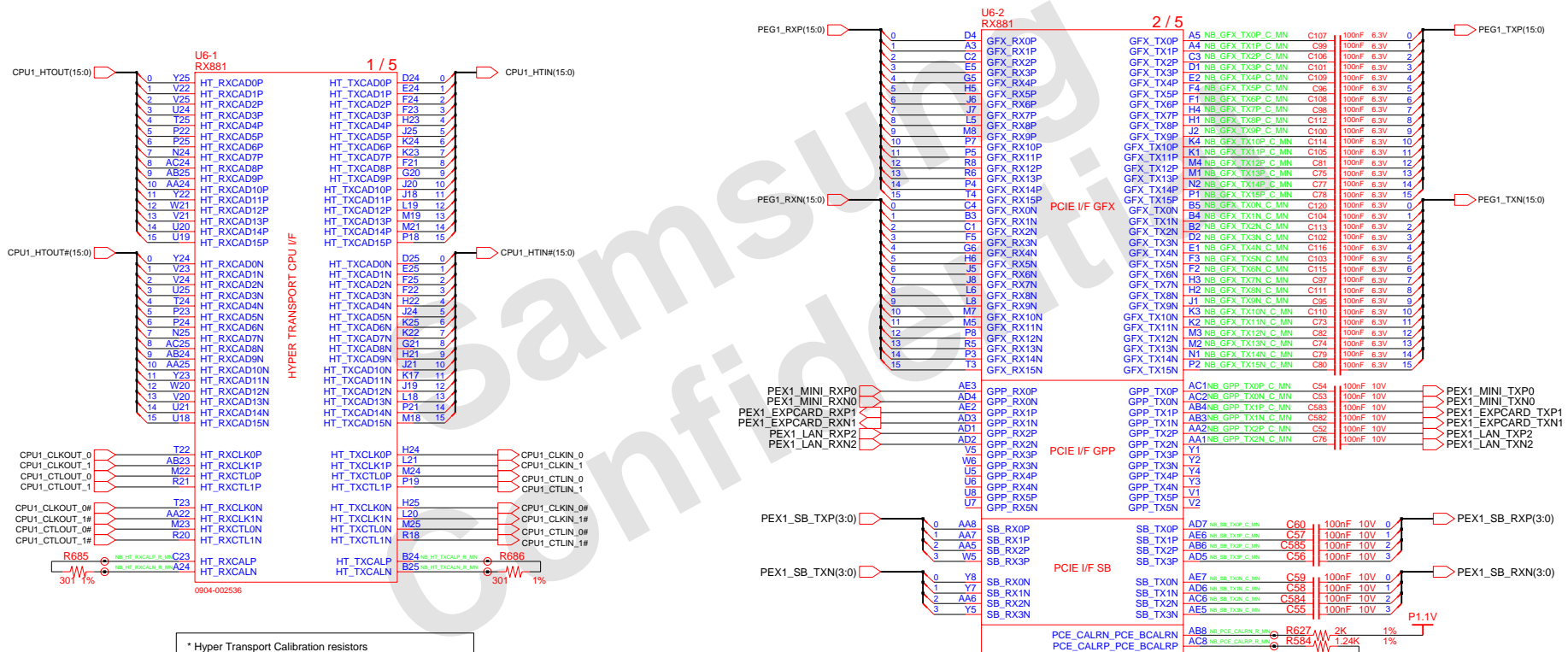


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CHECK	GUO LEI	DEV. STEP	ADV	Caspian CPU	PART NO.	
APPROVAL	BC LEE	REV	0.1	S1G3 CPU (3/3)	BA41-xxxxxA	
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	12 OF 58

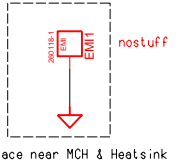
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NB_RX881_AMD



* Hyper Transport Calibration resistors
 RS780M / RX781 : 301 ohm
 RX780 / RD780 : 1.21K ohm (for S3 issue in D/T chipset)

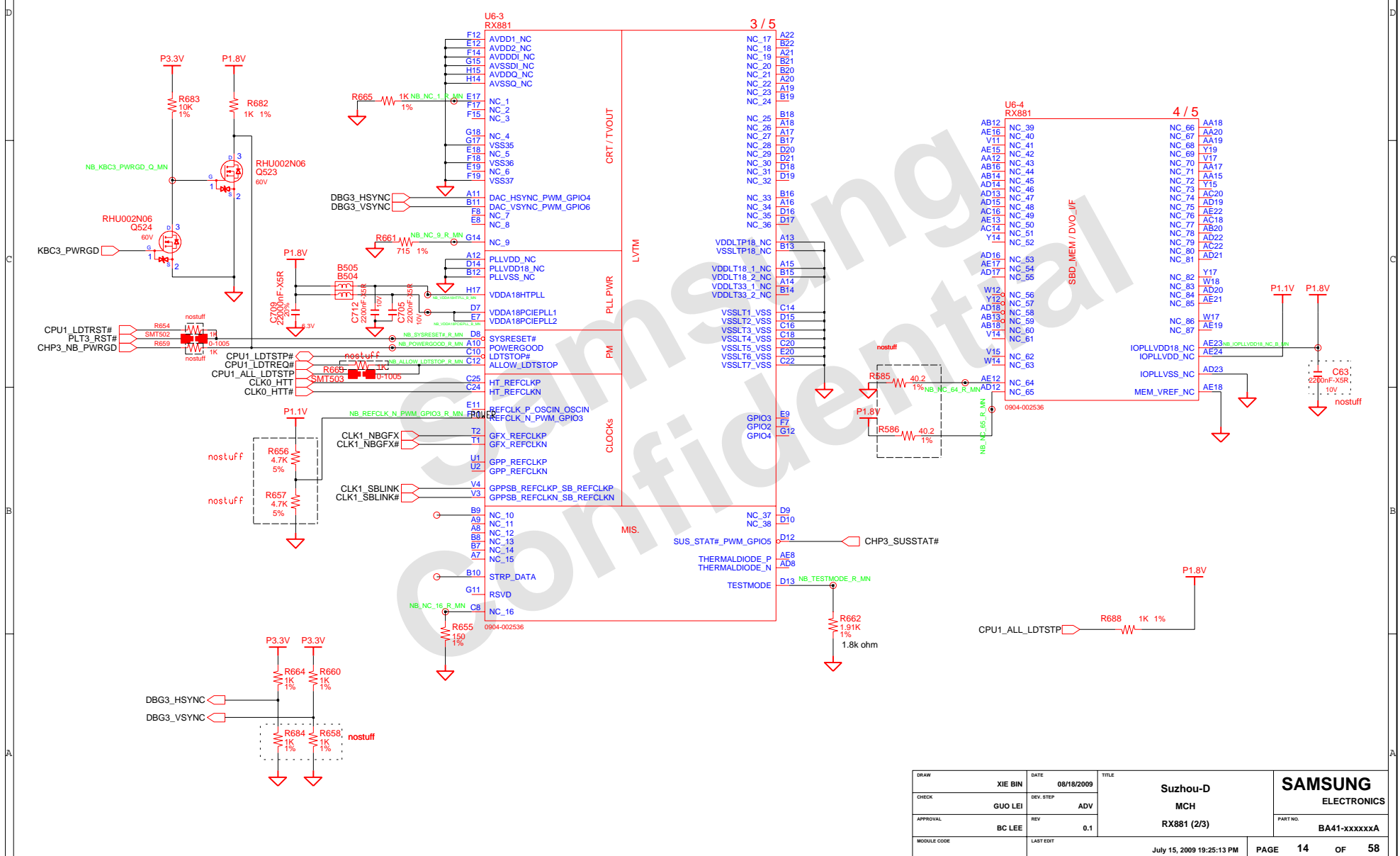


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CHECK	GUO LEI	DEV. STEP	ADV	MCH		
APPROVAL	BC LEE	REV	0.1	RX881 (1/3)		
MODULE CODE		LAST EDT			July 15, 2009 19:25:13 PM	PAGE 13 OF 58

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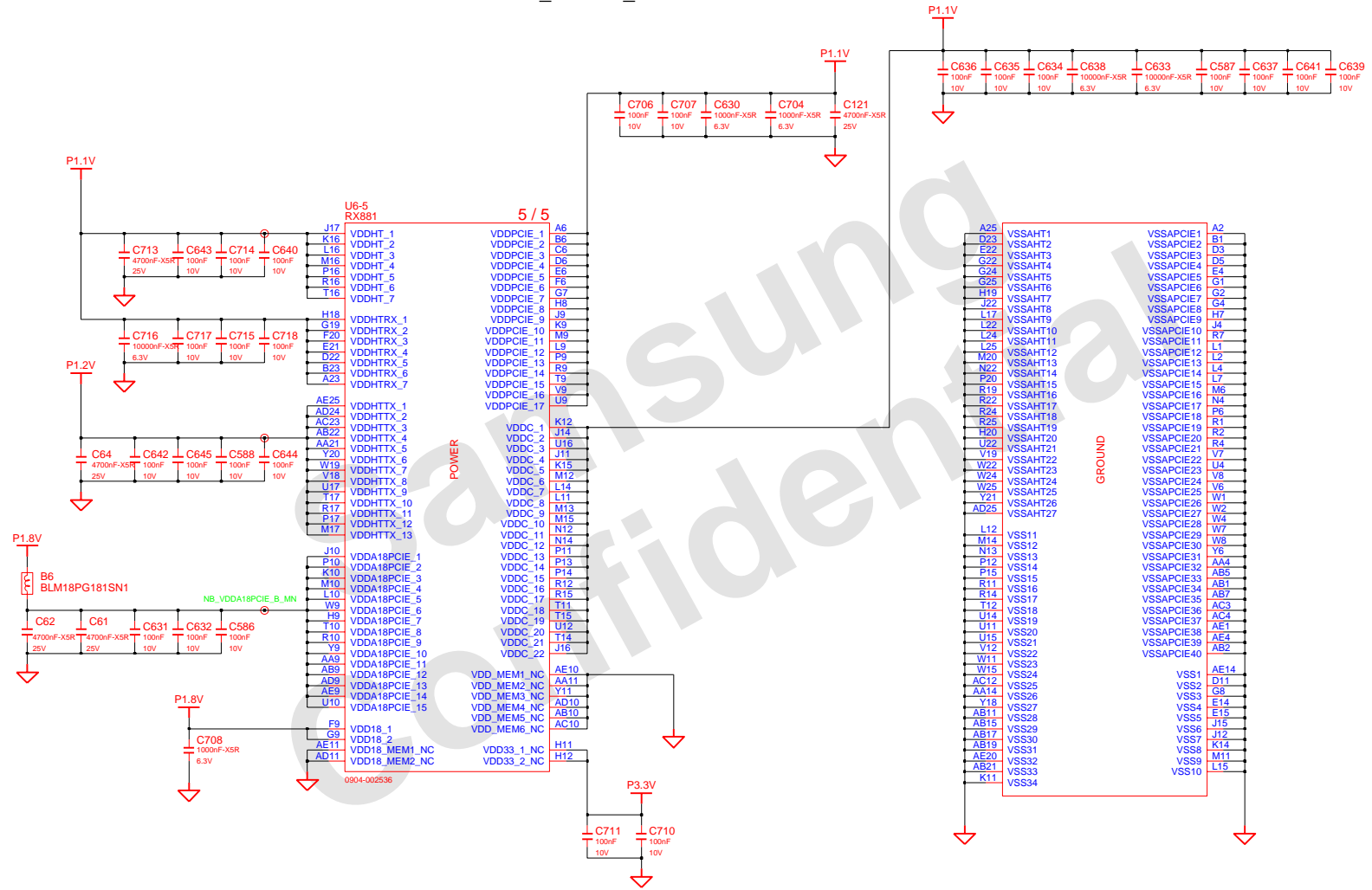
NB_RX881_AMD



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MCH		
APPROVAL	BC LEE	REV	0.1	RX881 (2/3)	PART NO. BA41-xxxxxA	
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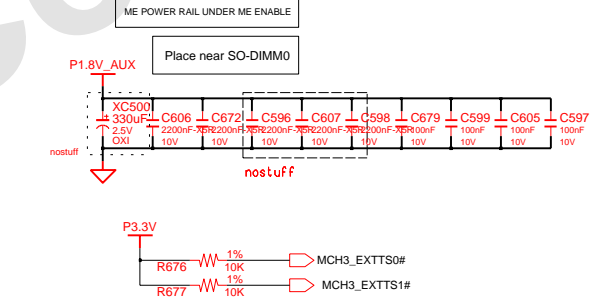
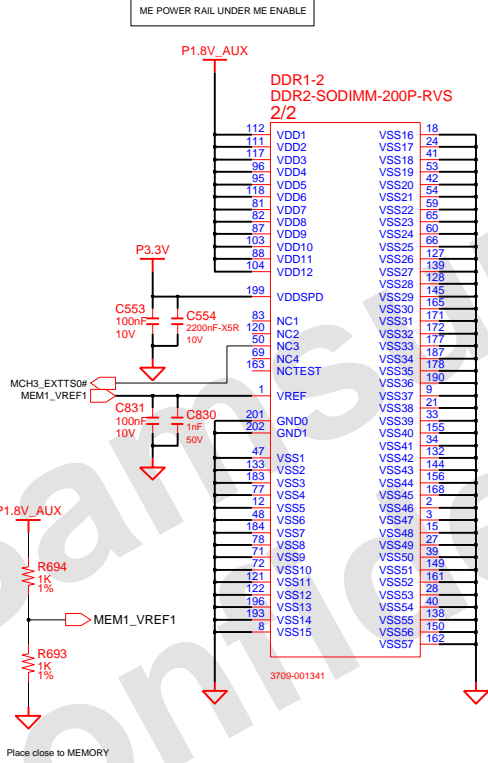
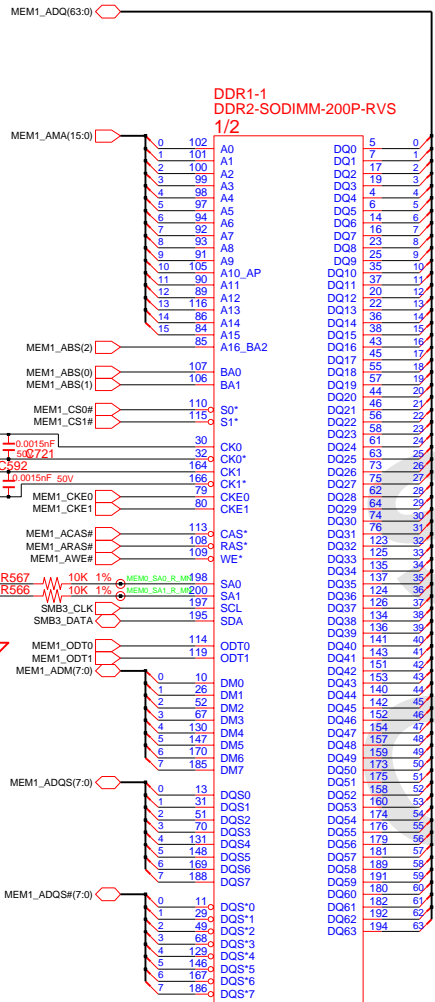
NB_RX881_AMD



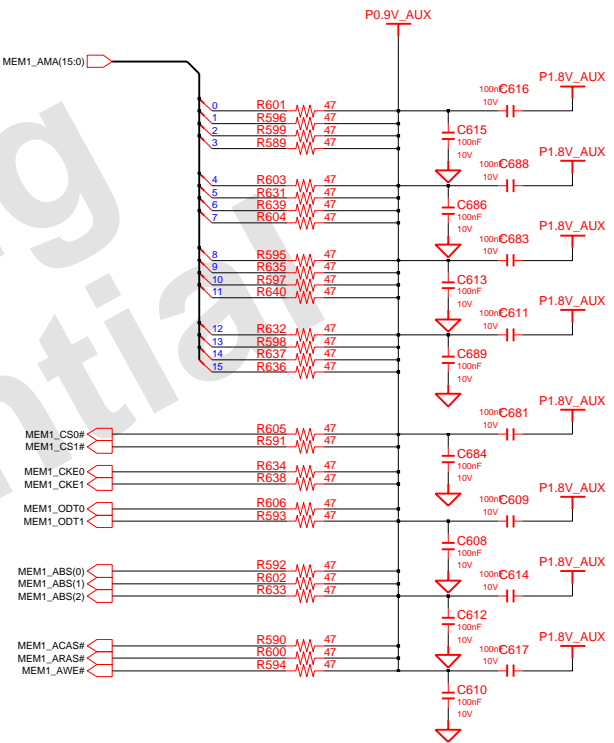
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MCH	MCH	
APPROVAL	BC LEE	REV	0.1	RX881 (3/3)	RX881 (3/3)	PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	15 OF 58

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DDR SO-DIMM #0



Array resistors & Single resistors used to improve layout & routing.

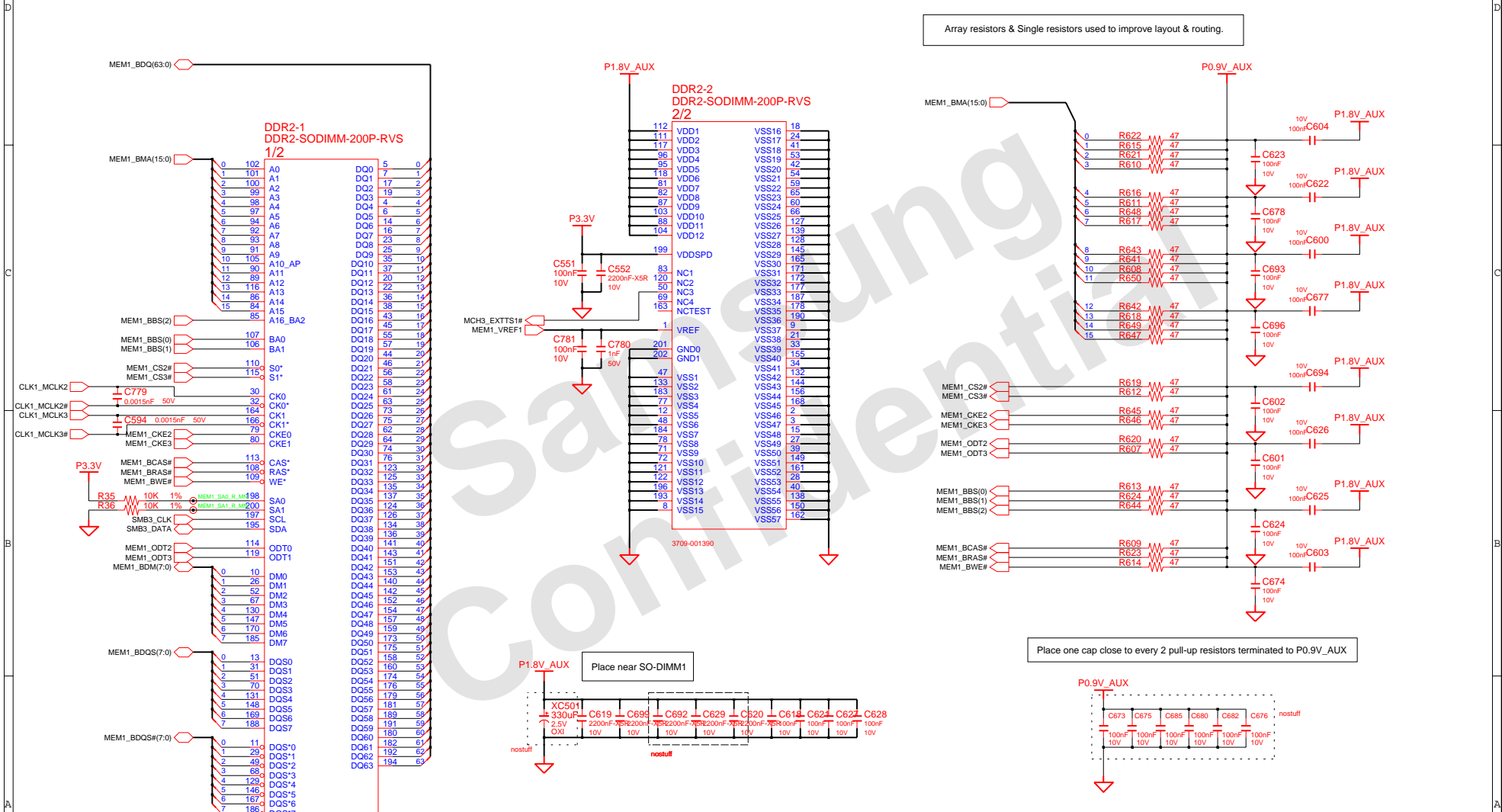


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	SODIMM_DDR2		
APPROVAL	BC LEE	REV	0.1	SODIMM_DDR2 (1/2)		PART NO. BA41-xxxxxxA
MODULE CODE	LAST EXT		July 15, 2009 19:25:13 PM		PAGE	16 OF 58

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DDR SO-DIMM #1

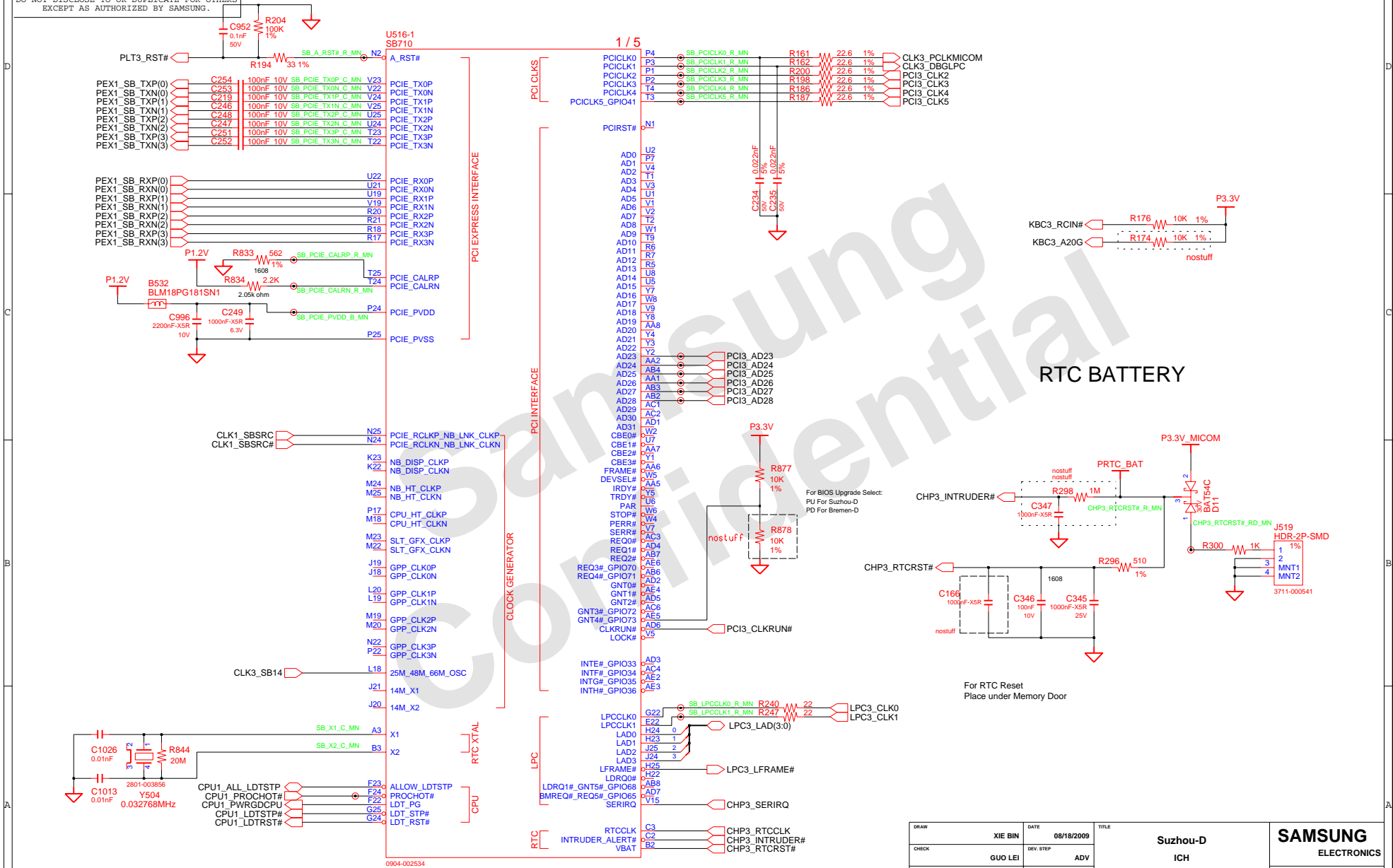


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CHECK	GUO LEI	DEV. STEP	ADV	SODIMM_DDR2	BA41-xxxxxA	
APPROVAL	BC LEE	REV	0.1	SODIMM_DDR2 (2/2)	PART NO.	BA41-xxxxxA
MODULE CODE		LAST ENT			July 15, 2009 19:25:13 PM	PAGE 17 OF 58

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SB_710_AMD



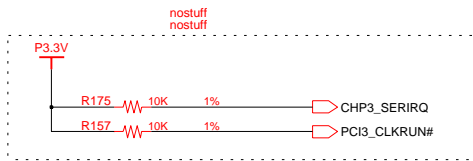
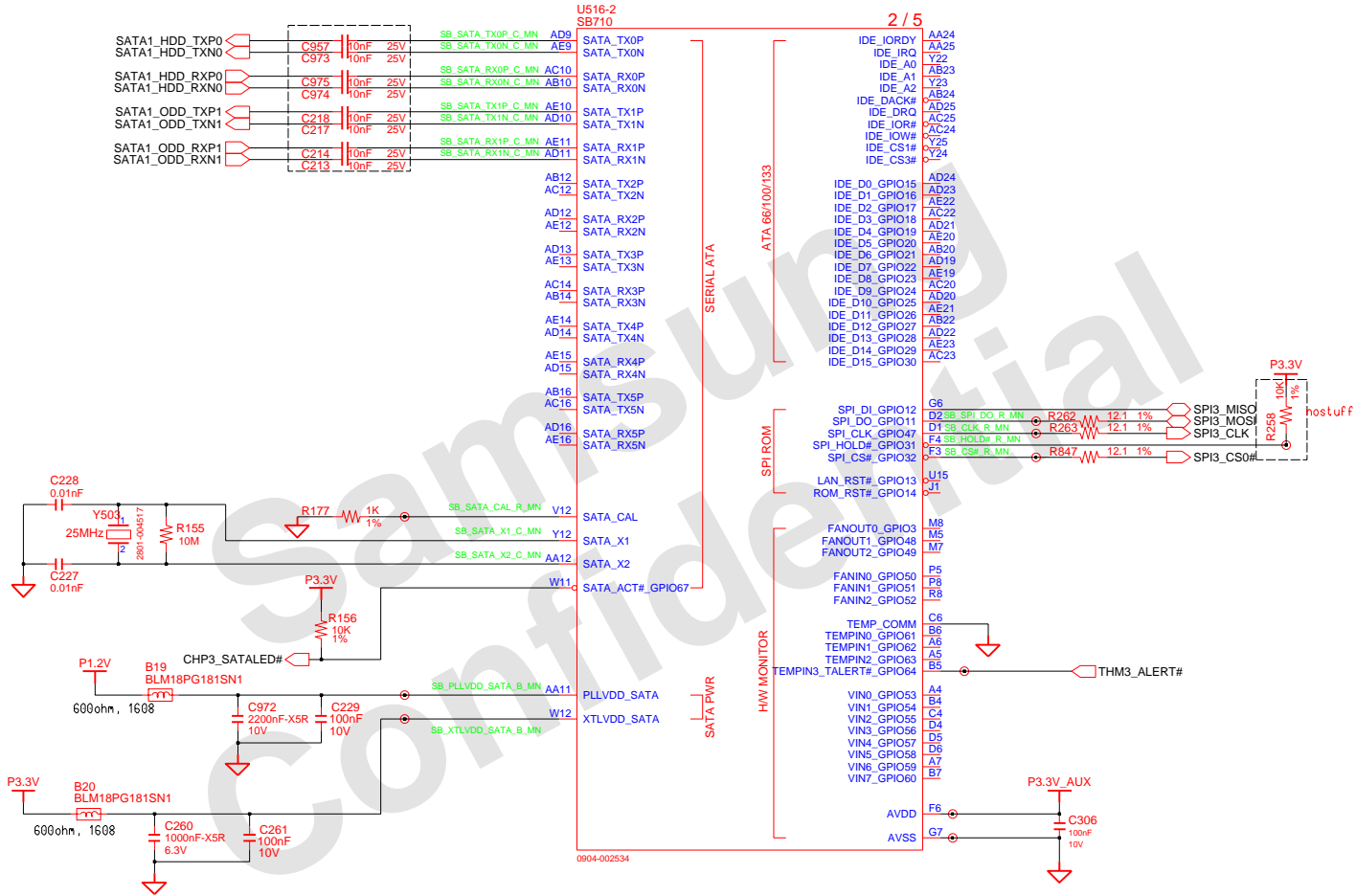
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CHECK	GUO LEI	DEV.STEP	ADV	ICH		
APPROVAL	BC LEE	REV	0.1	SB710 (1/5)		BA41-xxxxxA
MODULE CODE	LAST ENT		July 15, 2009 19:25:13 PM		PAGE	18 OF 58

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SB_710_AMD

Route to connector side closely



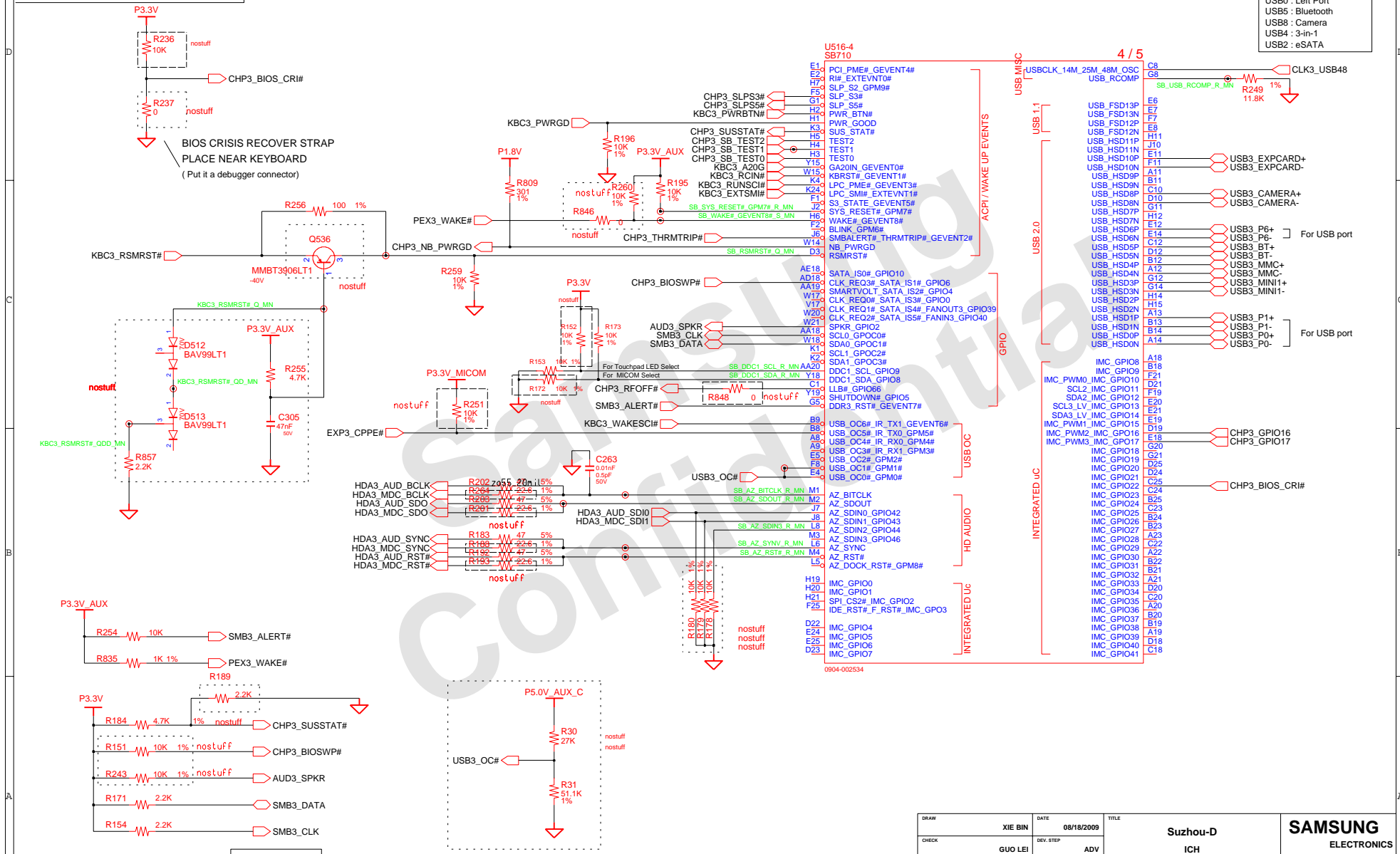
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CHECK	GUO LEI	DEV. STEP	ADV	ICH	PART NO.	
APPROVAL	BC LEE	REV	0.1	SB710 (2/5)	BA41-xxxxxA	
MODULE CODE		LAST EXT		July 15, 2009 19:25:13 PM	PAGE	19 OF 58

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SB_710_AMD

USB1, 6 : Right Port
 USB0 : Left Port
 USB5 : Bluetooth
 USB8 : Camera
 USB4 : 3-in-1
 USB2 : eSATA

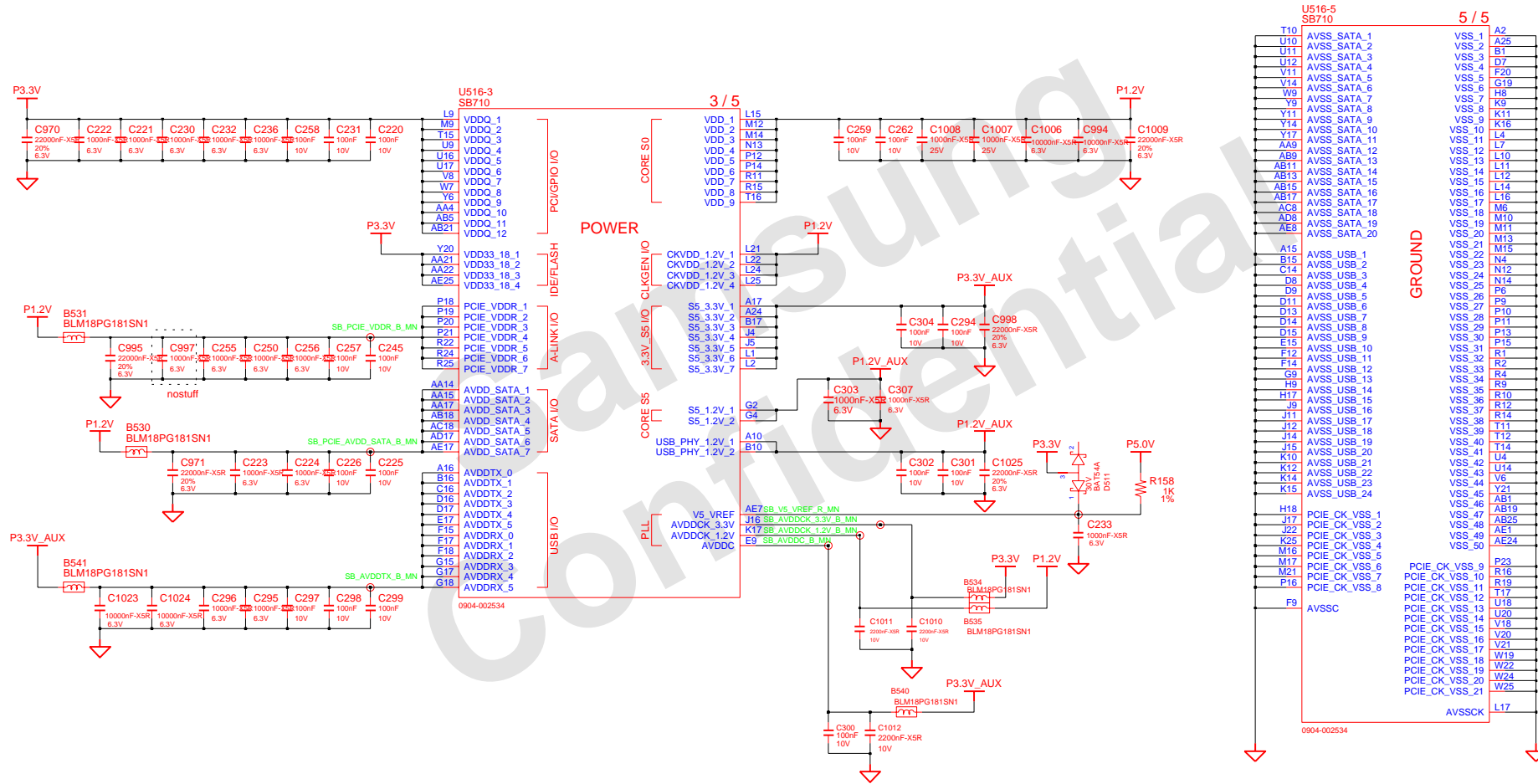


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV_STEP	ADV	ICH	ICH	
APPROVAL	BC LEE	REV	0.1	SB710 (3/5)	SB710 (3/5)	PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	20 OF 58

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SB_710_AMD



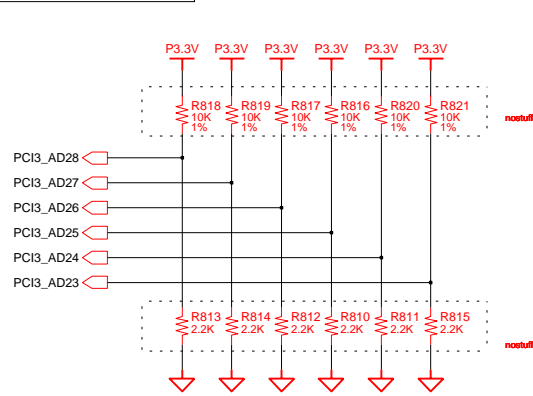
U516-5 SB710		5 / 5	
T10	AVSS_SATA_1	VSS_1	A25
U10	AVSS_SATA_2	VSS_2	B1
U11	AVSS_SATA_3	VSS_3	D7
U12	AVSS_SATA_4	VSS_4	F20
V11	AVSS_SATA_5	VSS_5	G19
V14	AVSS_SATA_6	VSS_6	H8
W9	AVSS_SATA_7	VSS_7	K9
Y9	AVSS_SATA_8	VSS_8	K11
Y11	AVSS_SATA_9	VSS_9	K16
Y14	AVSS_SATA_10	VSS_10	L4
Y17	AVSS_SATA_11	VSS_11	L7
AA9	AVSS_SATA_12	VSS_12	L10
AB9	AVSS_SATA_13	VSS_13	L11
AB11	AVSS_SATA_14	VSS_14	L12
AB13	AVSS_SATA_15	VSS_15	L14
AB15	AVSS_SATA_16	VSS_16	L16
AB17	AVSS_SATA_17	VSS_17	M6
AC8	AVSS_SATA_18	VSS_18	M10
AD8	AVSS_SATA_19	VSS_19	M11
AE8	AVSS_SATA_20	VSS_20	M13
A15	AVSS_USB_1	VSS_21	M15
B15	AVSS_USB_2	VSS_22	N4
C14	AVSS_USB_3	VSS_23	N12
D8	AVSS_USB_4	VSS_24	N14
D9	AVSS_USB_5	VSS_25	P6
D11	AVSS_USB_6	VSS_26	P9
D13	AVSS_USB_7	VSS_27	P10
D14	AVSS_USB_8	VSS_28	P11
E15	AVSS_USB_9	VSS_29	P15
F12	AVSS_USB_10	VSS_30	R1
F14	AVSS_USB_11	VSS_31	R2
G9	AVSS_USB_12	VSS_32	R4
H9	AVSS_USB_13	VSS_33	R9
H17	AVSS_USB_14	VSS_34	R10
J9	AVSS_USB_15	VSS_35	R12
J11	AVSS_USB_16	VSS_36	R12
J12	AVSS_USB_17	VSS_37	R14
J14	AVSS_USB_18	VSS_38	R12
J15	AVSS_USB_19	VSS_39	R12
K10	AVSS_USB_20	VSS_40	T14
K12	AVSS_USB_21	VSS_41	U4
K14	AVSS_USB_22	VSS_42	U14
K15	AVSS_USB_23	VSS_43	V6
K15	AVSS_USB_24	VSS_44	Y21
H18	AVSSCK	VSS_45	AB1
J17	PCIE_CK_VSS_1	VSS_46	AB19
J22	PCIE_CK_VSS_2	VSS_47	AB25
K25	PCIE_CK_VSS_3	VSS_48	AE1
M16	PCIE_CK_VSS_4	VSS_49	AE24
M17	PCIE_CK_VSS_5	VSS_50	
M21	PCIE_CK_VSS_6		P23
P16	PCIE_CK_VSS_7		R16
	PCIE_CK_VSS_8		R19
			R17
			U18
			U20
			V15
			V20
			V21
			V19
			W22
			W24
			W25
			L17

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	ICH		
APPROVAL	BC LEE	REV	0.1	SB710 (4/5)		PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT			July 15, 2009 19:25:13 PM	PAGE 21 OF 58

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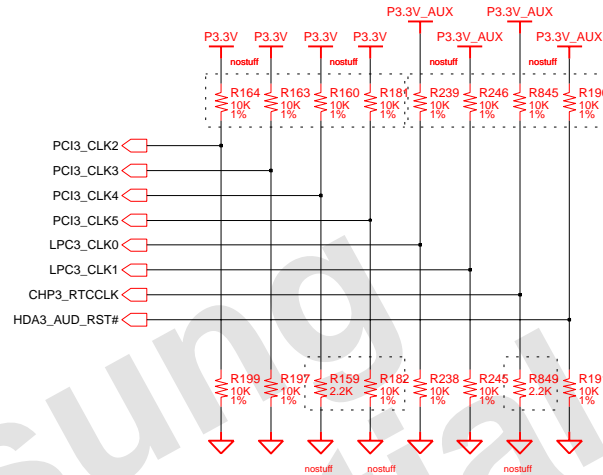
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Strap

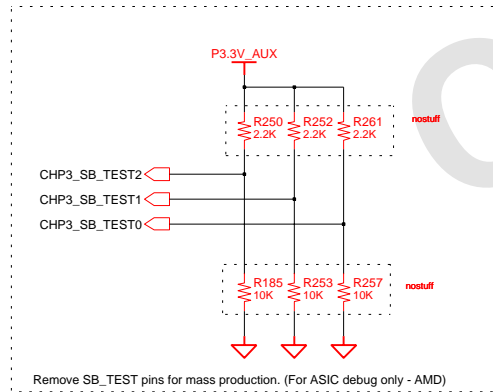


DEBUG STRAPS

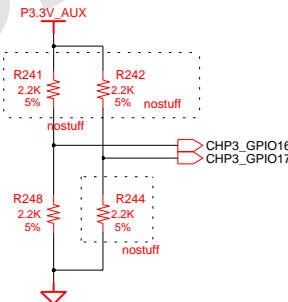
	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
STRAP HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT



Remove SB_TEST pins for mass production. (For ASIC debug only - AMD)



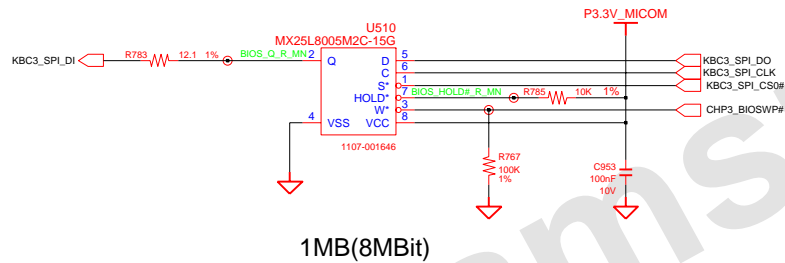
GPIO17	GPIO16
ROM TYPE	
NC, NC = RSVD	
NC, L = SPI ROM	
L, NC = LPC ROM	
L, L = FW ROM	

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	ICH		
APPROVAL	BC LEE	REV	0.1	SB710 Strap(5/5)	PART NO.	BA41-xxxxxA
MODULE CODE		LAST ENT		July 15, 2009 19:25:13 PM	PAGE	22 OF 58

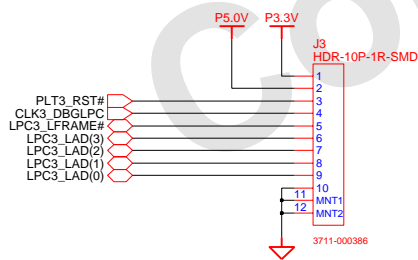
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SPI_BIOS_ROM

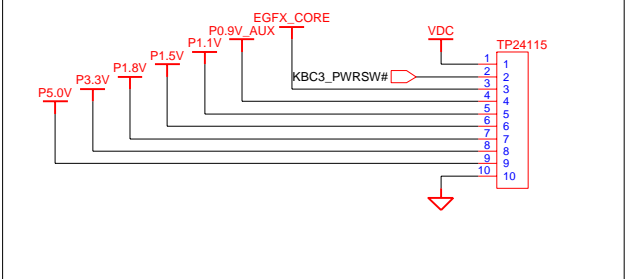


80H DECODER CONNECTOR

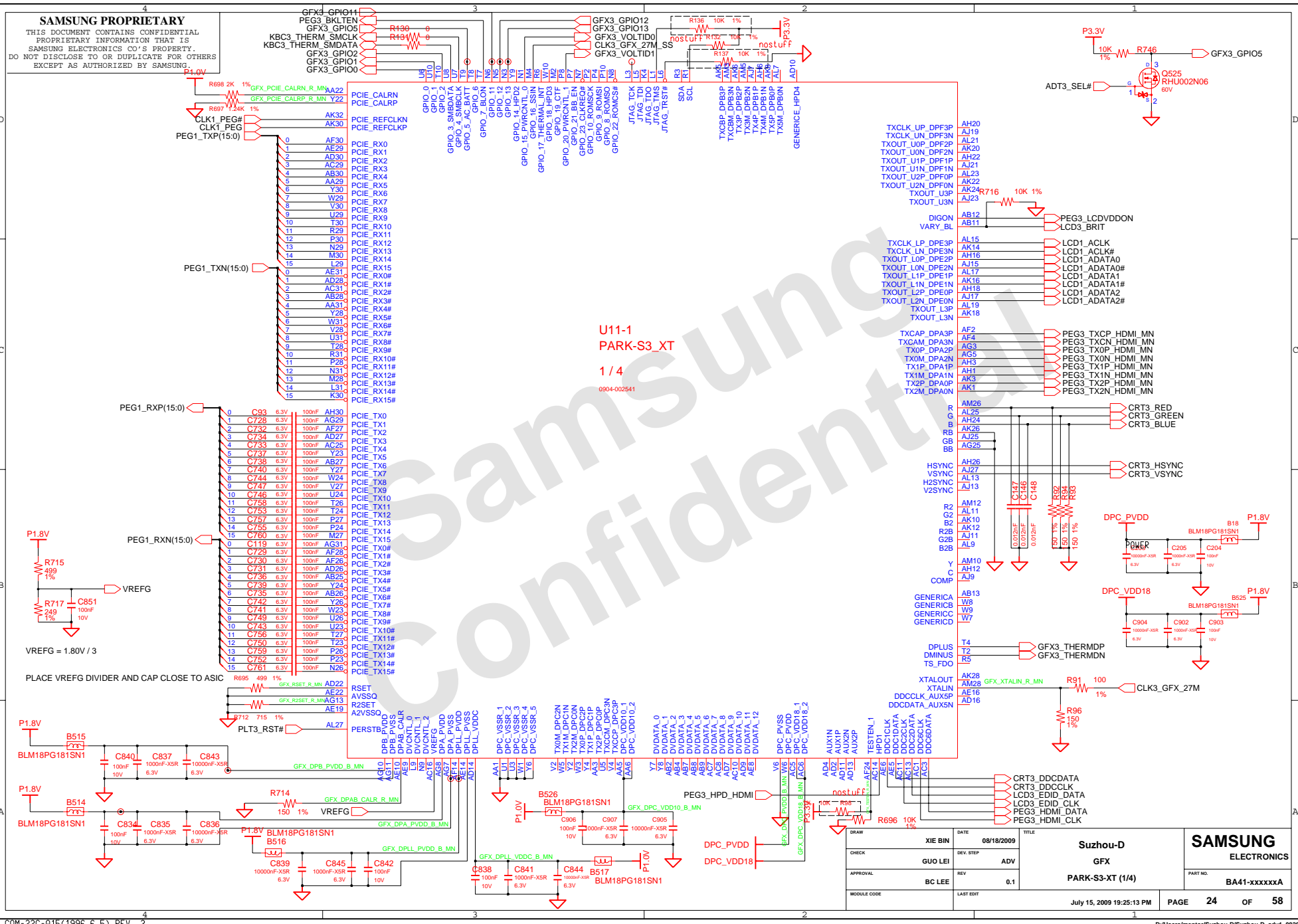


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT. RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT. PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
14	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
16	INIT. KEYBOARD CONTROLLER	8A	INIT. EXTENDED BIOS DATA AREA
18	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
1A	8254 TIMER INIT.	8E	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	90	SETUP POWER MANAGEMENT
1E	TEST DRAM REFRESH	92	ENABLE H/W INTERRUPT
20	TEST 8742 KEYBOARD CONTROLLER	94	SET TIME OF DAY
22	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
24	AUTO SIZING DRAM	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	COMPUTE THE CPU SPEED	AC	ENTER SETUP
2A	TEST CMOS RAM	AE	CLEAR IN POST FLAG
2C	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
2E	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
30	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
32	LOAD ALTERNATE REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
34	INIT. INTERRUPT VECTOR	B8	ACPI INIT.
36	INIT. BIOS INTERRUPT	BA	DMI INIT.
38	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
3A	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
3C	CHECK VIDEO CONFIGURE AGAINST CMOS	C2	INTERUPT HANDLER ERROR
3E	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
40	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
42	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
44	DISPLAY CPU TYPE AND SPEED	DA	SHUTDOWN ERROR
46	TEST KEYBOARD	DC	EXTENDED BLOCK MOVE
48	SET KEYCLICK IF ENABLED	89	SHUTDOWN 10
4A	ENABLE KEYBOARD	90	ENABLE NMI
4C	TEST FOR UNEXPECTED INTERRUPTS	92	INIT. HDD CONTROLLER
4E	DISPLAY "PRESS... SETUP"	94	INIT. LOCAL BUS HDD CONTROLLER
50	TEST RAM BETWEEN 512K AND 640K	96	JUMP TO USER PATCH 2
52	TEST EXTENDED MEMORY	98	DISABLE A20 ADDRESS LINE
54	TEST EXTENDED MEMORY ADDRESS LINE		CLEAR HUGE ES SEGMENT REG.
56	JUMP TO USER PATCH 1		SEARCH FOR OPTION ROMS

ICT FREE



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	SPI_BIOS_ROM	PART NO.	
APPROVAL	BC LEE	REV	0.1	SPI_BIOS_ROM	BA41-xxxxxA	
MODULE CODE		LAST ENT		July 15, 2009 19:25:13 PM	PAGE	23 OF 58



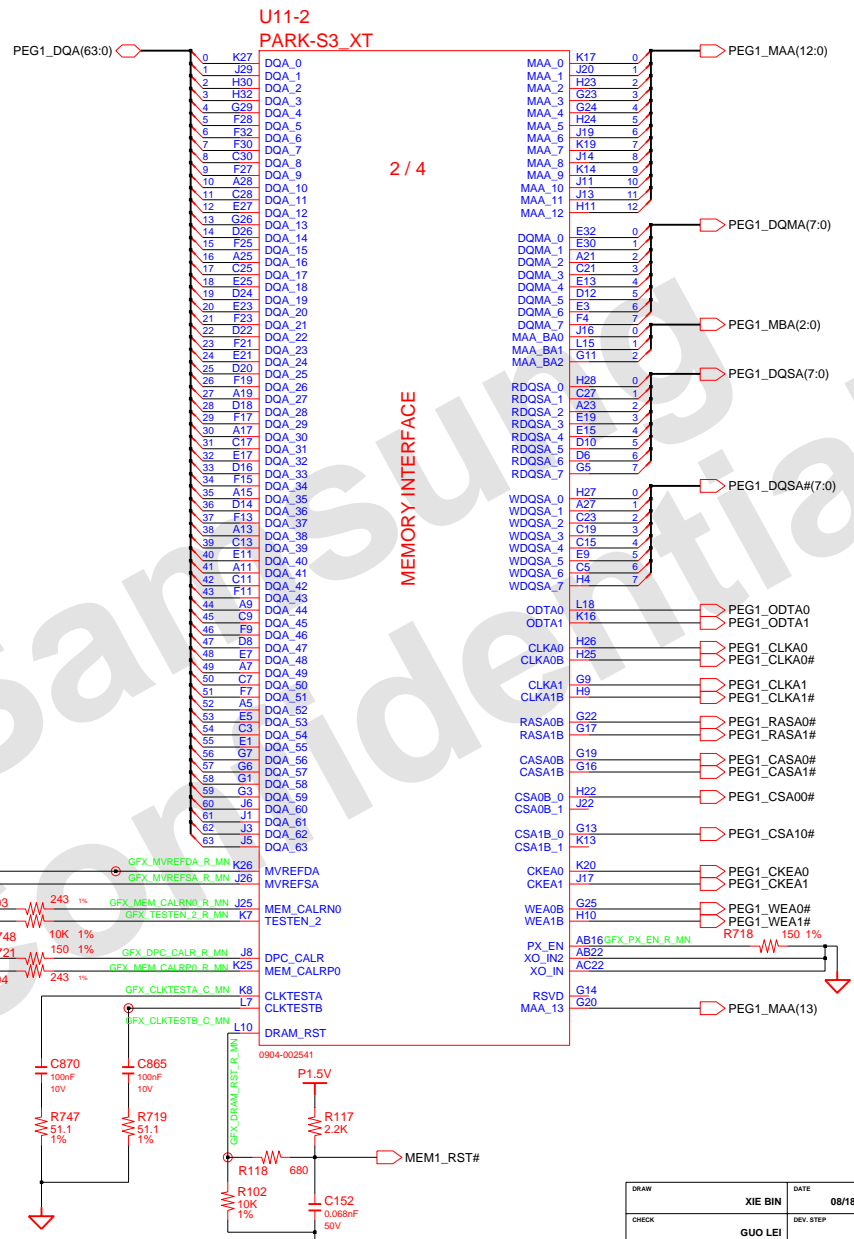
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U11-1
 PARK-S3_XT
 1 / 4
 0004-002541

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

DRW	XIE BIN	DATE	TITLE
		08/18/2009	Suzhou-D GFX
CHECK	GUO LEI	DEV STEP	ADV
APPROVAL	BC LEE	REV	0.1
MODULE CODE		LAST EDIT	

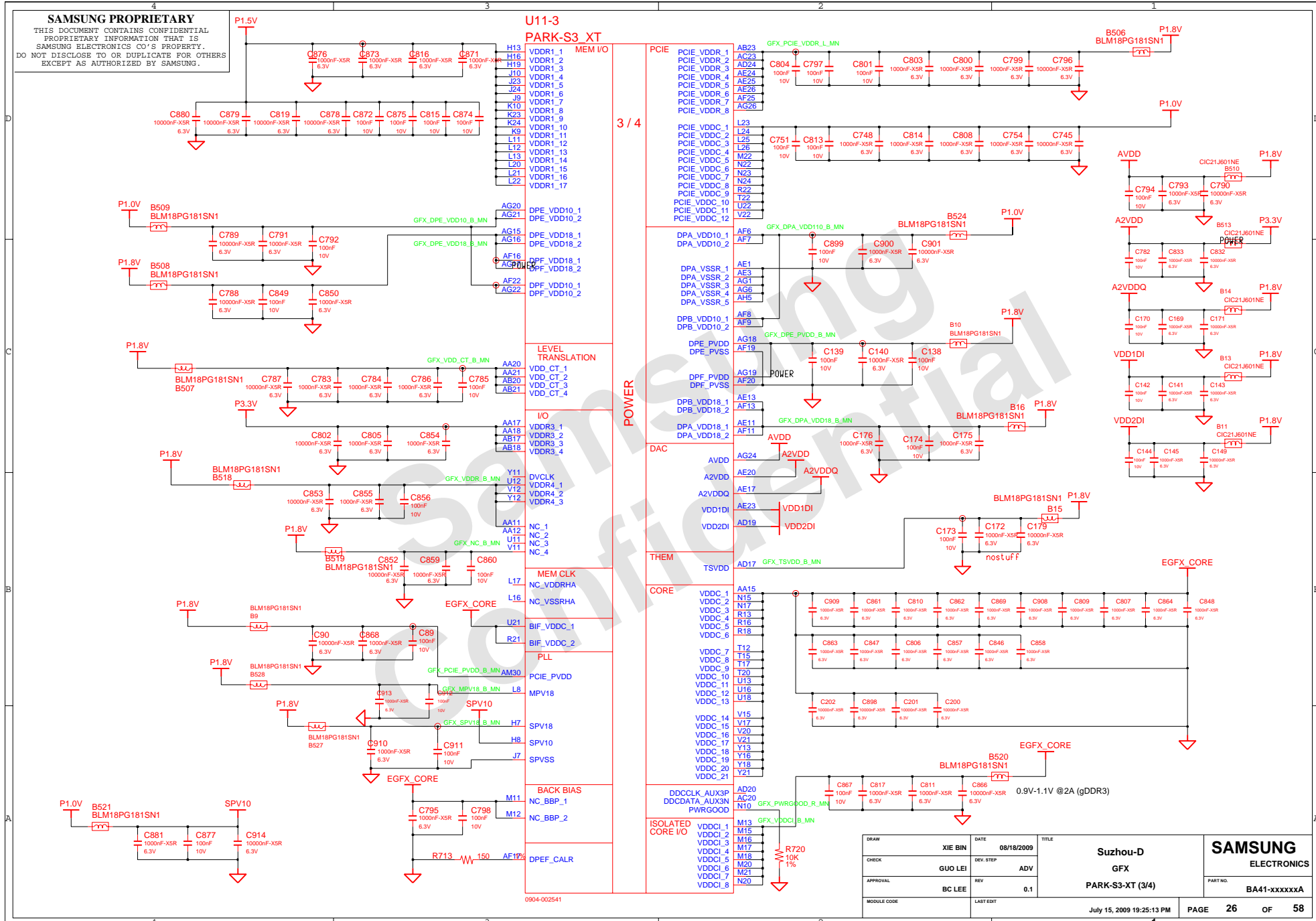
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DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	GFXX	GFXX	
APPROVAL	BC LEE	REV	0.1	PARK-S3-XT (2/4)	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	25 OF 58

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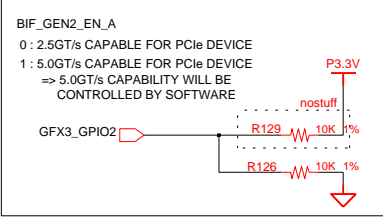
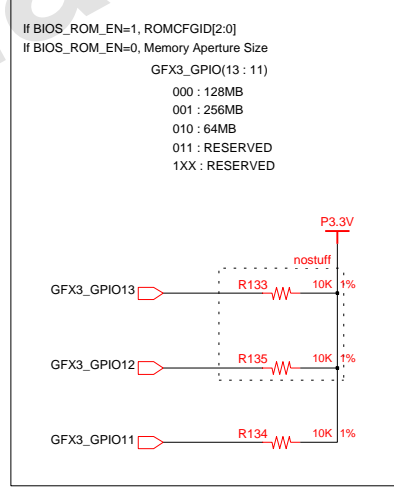
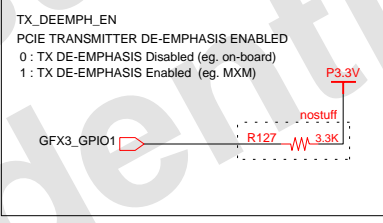
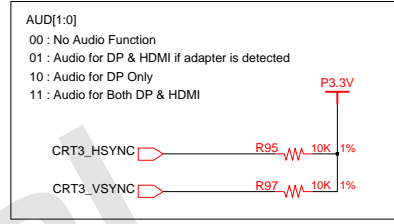
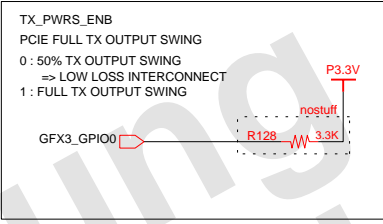
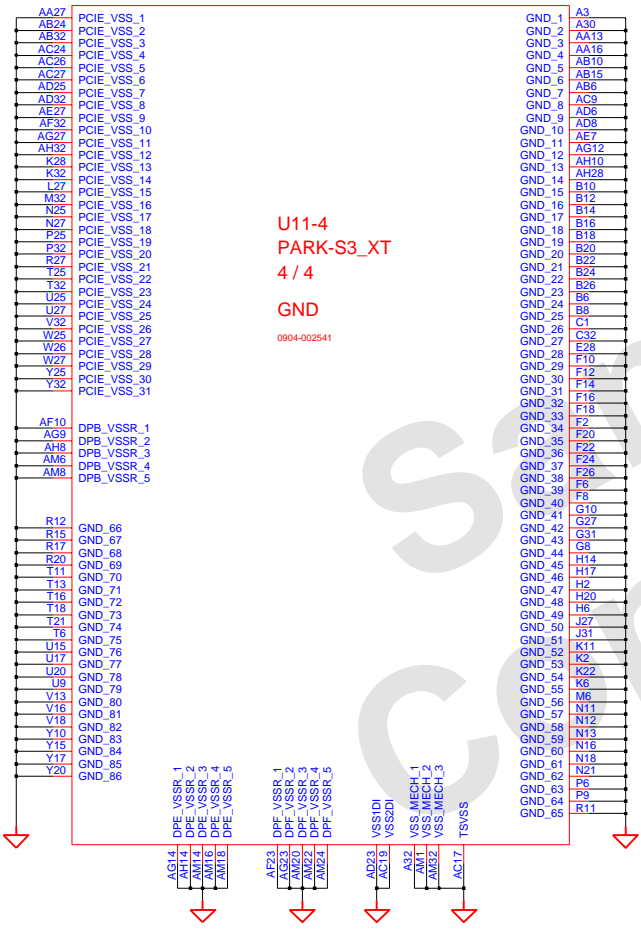


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D GFX	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV		PART NO.	
APPROVAL	BC LEE	REV	0.1		BA41-xxxxxA	
MODULE CODE		LAST ENT				
			July 15, 2009 19:25:13 PM	PAGE	26 OF 58	

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PARK Straps

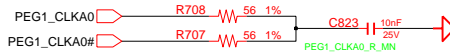
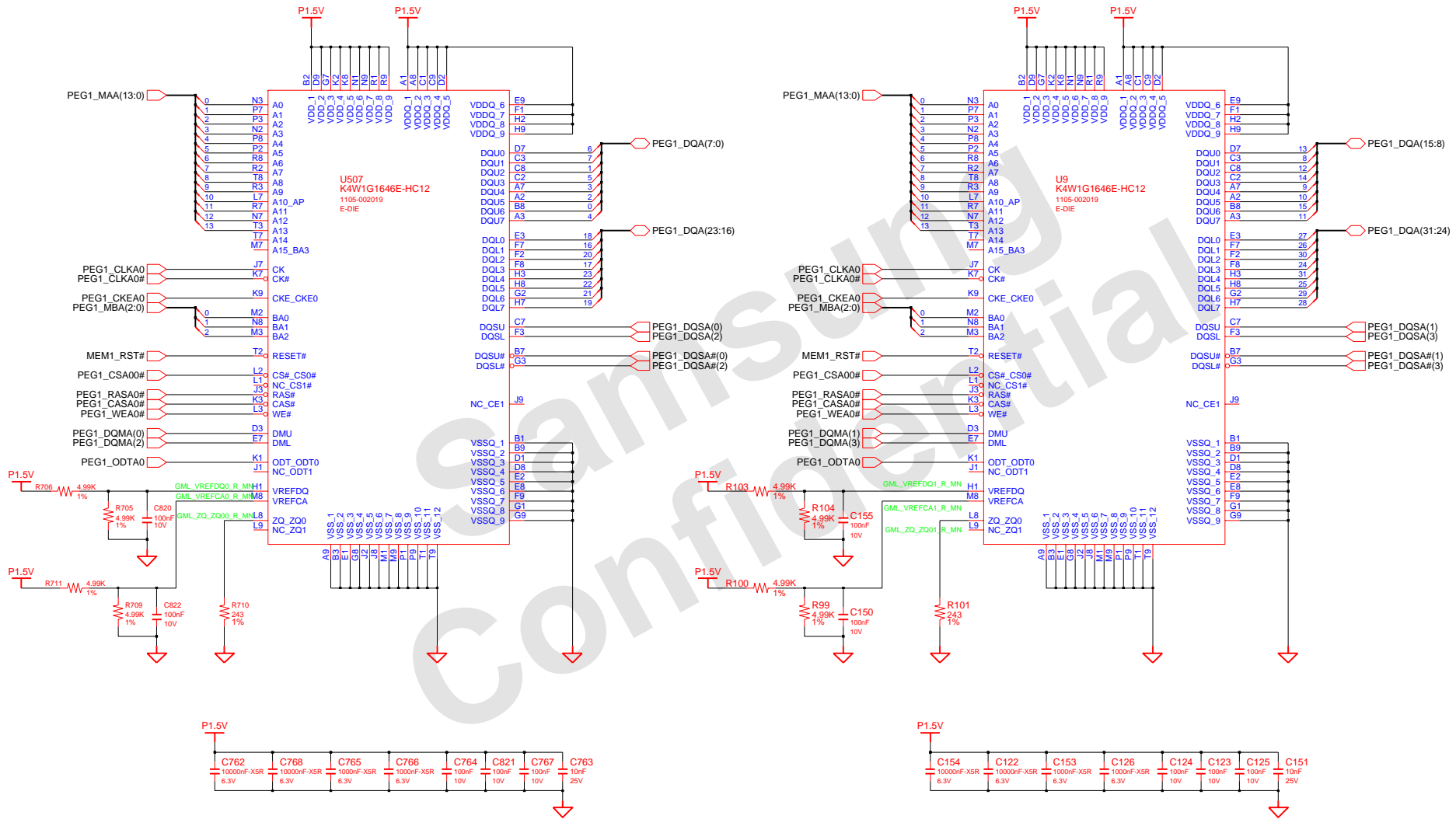


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	GFX	GFX	
APPROVAL	BC LEE	REV	0.1	PARK-S3-XT (4/4)	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	27	OF 58

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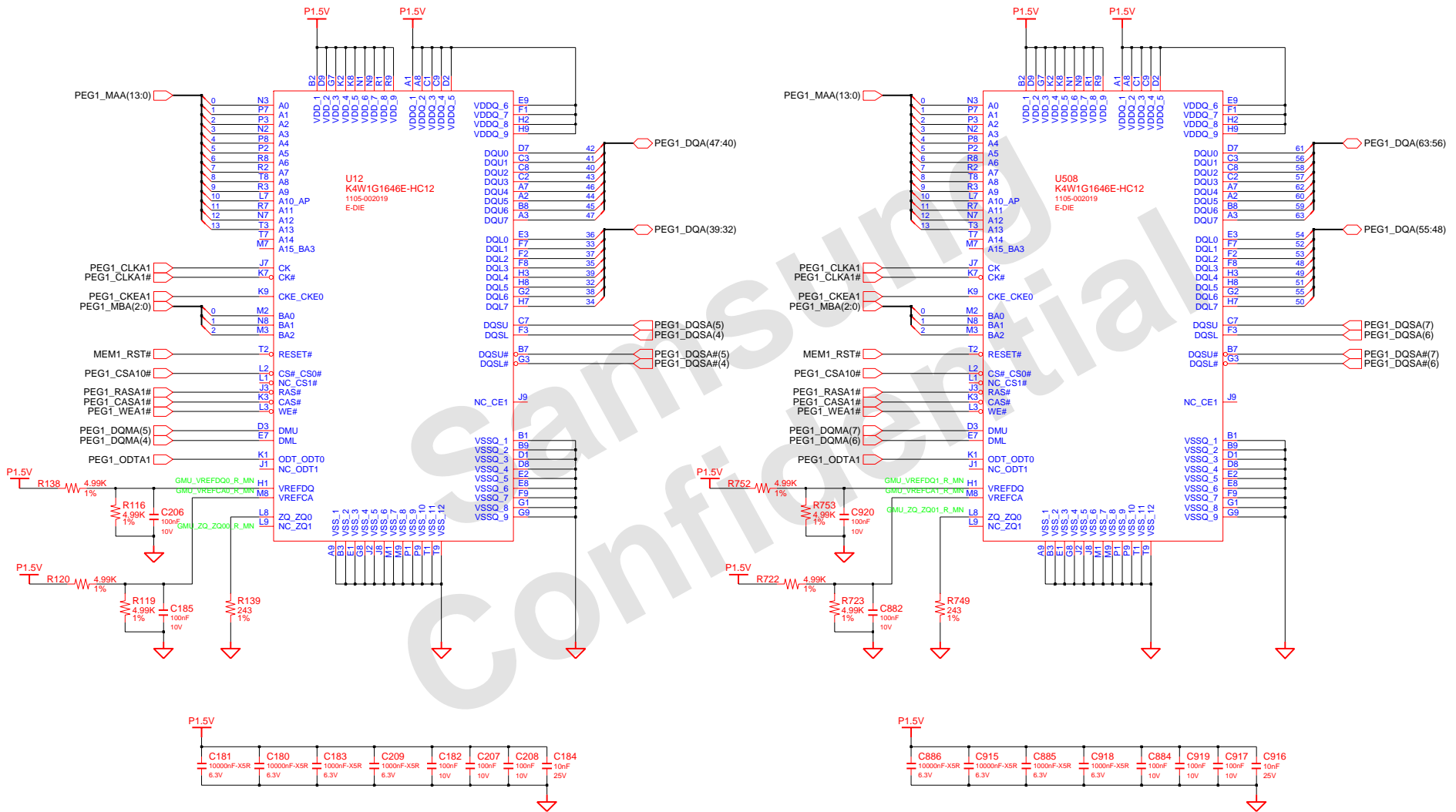
A-channel Lower Data



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D
CHECK	GUO LEI	DEV. STEP	ADV	GRAPHICS_MEMORY	SAMSUNG ELECTRONICS
APPROVAL	BC LEE	REV	0.1	gDDR3 (1/2)	PART NO. BA41-xxxxxA
MODULE CODE		LAST ENT		July 15, 2009 19:25:13 PM	PAGE 28 OF 58

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A-channel Upper Data



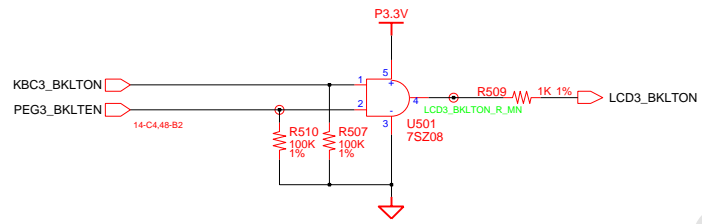
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D
CHECK	GUO LEI	DEV.STEP	ADV		GRAPHICS_MEMORY
APPROVAL	BC LEE	REV	0.1		gDDR3 (Z2)
MODULE CODE		LAST EDT			
				July 15, 2009 19:25:13 PM	PAGE 29 OF 58

SAMSUNG
 ELECTRONICS
 PART NO. BA41-xxxxxA

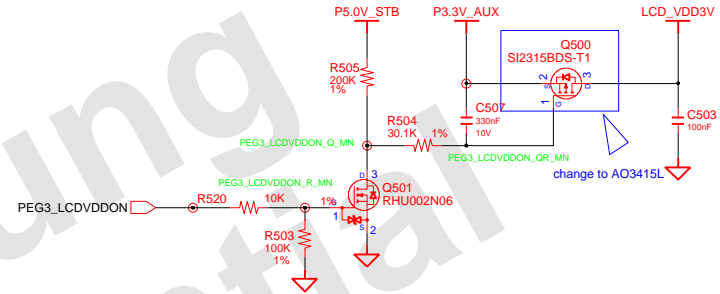
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LVDS

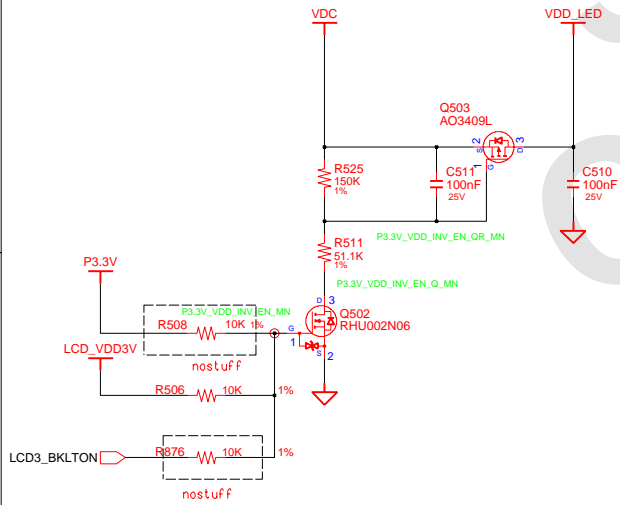
Backlight On



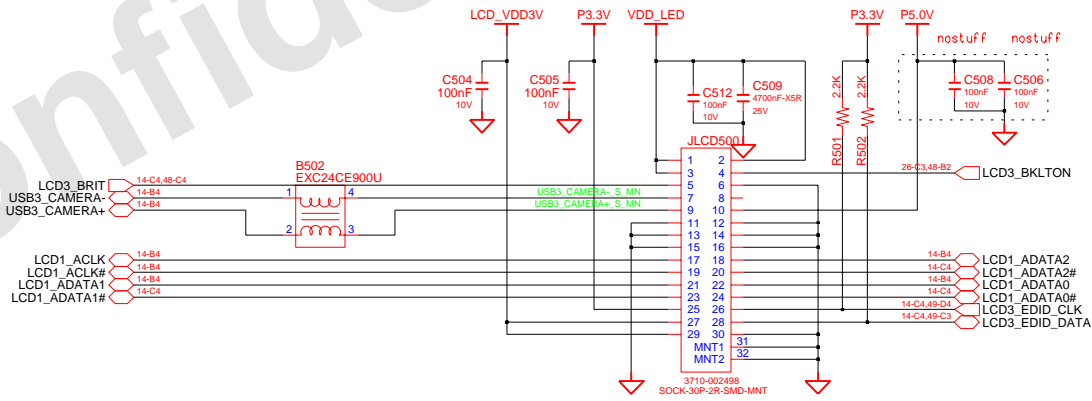
LCD Power EBL Purpose



Converter Power



Camera + LCD Connector



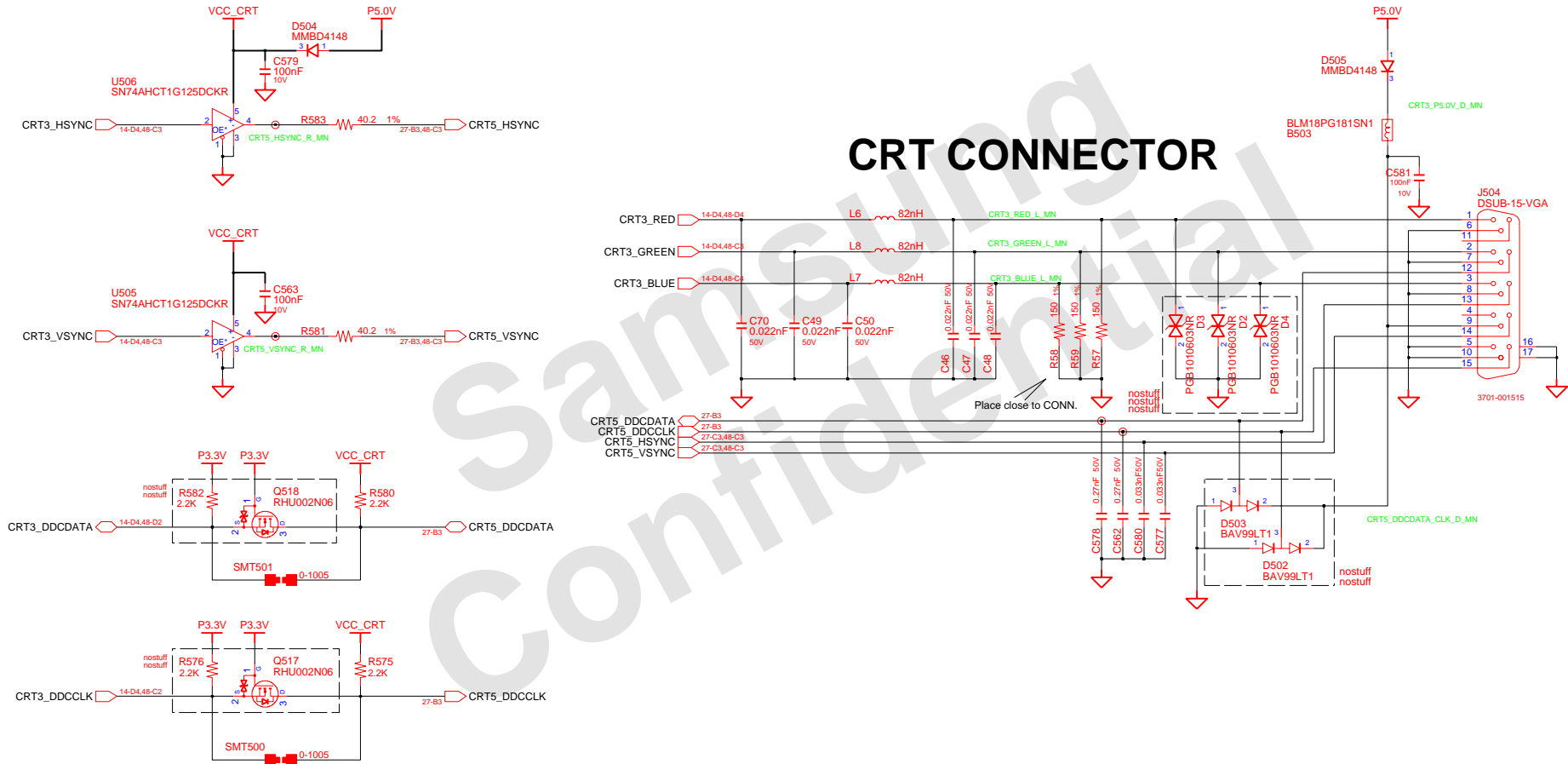
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV.STEP	ADV	GRAPHICS_IF (1/2)	PART NO.	
APPROVAL	BC LEE	REV	0.1	July 15, 2009 19:25:13 PM	PAGE	BA41-xxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	OF	58

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CRT

CRT CONNECTOR



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

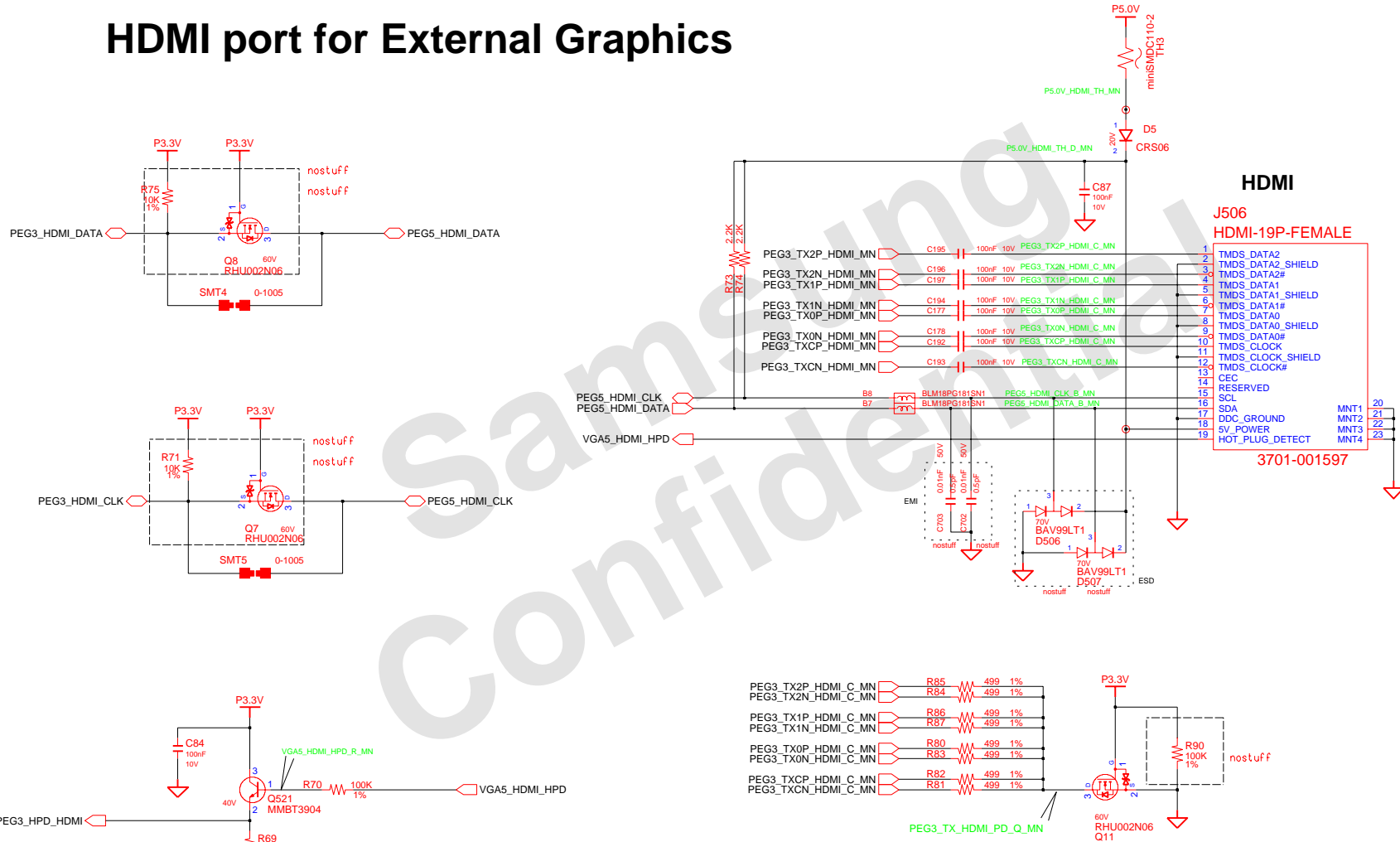
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	GRAPHICS_IF (2/2)	PART NO.	
APPROVAL	BC LEE	REV	0.1	July 15, 2009 19:25:13 PM	PAGE	31 OF 58
MODULE CODE	LAST EXT					

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HDMI

HDMI port for External Graphics

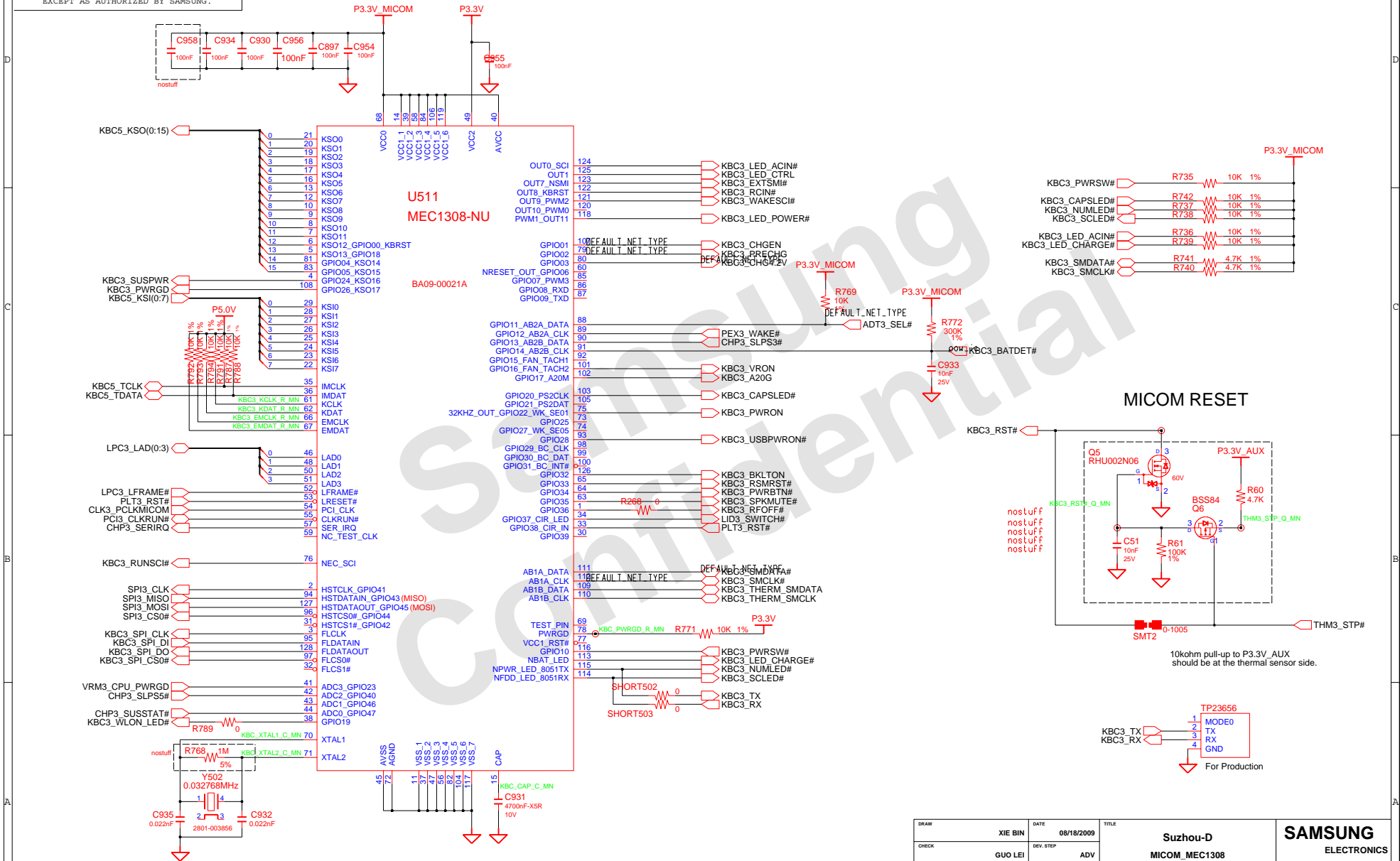


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	GRAPHICS_IF	PART NO.	
APPROVAL	BC LEE	REV	0.1	HDMI	BA41-xxxxxA	
MODULE CODE		LAST EXT		July 15, 2009 19:25:13 PM	PAGE 32 OF 58	

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MICOM_MEC1308-NU

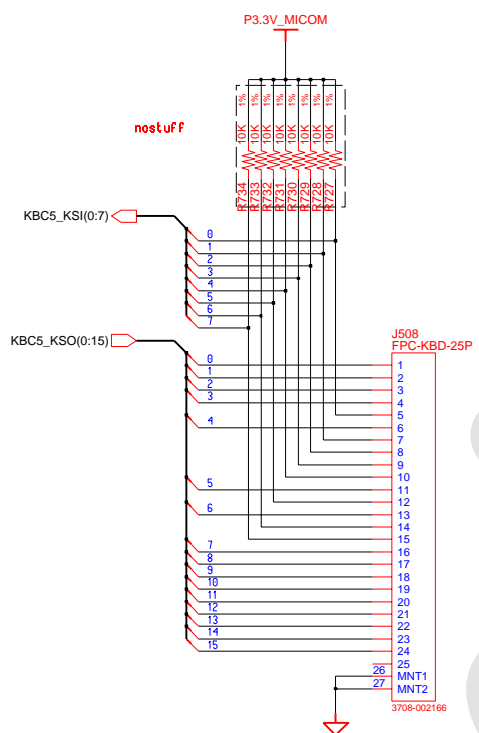


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MICOM_MEC1308	MICOM_MEC1308	
APPROVAL	BC LEE	REV	0.1	MICOM_MEC1308	PART NO.	BA41-xxxxxA
MODULE CODE		LAST ENT			July 15, 2009 19:25:13 PM	PAGE 33 OF 58

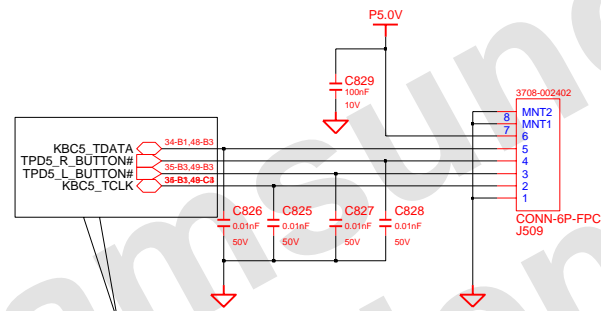
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Micom Glue Logic

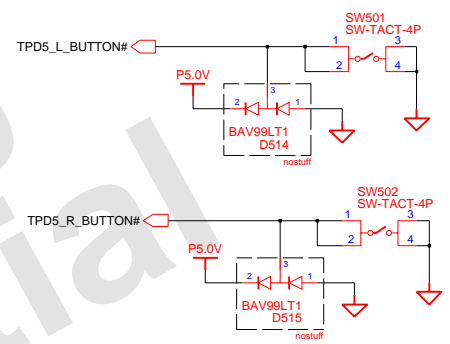
KEYBOARD



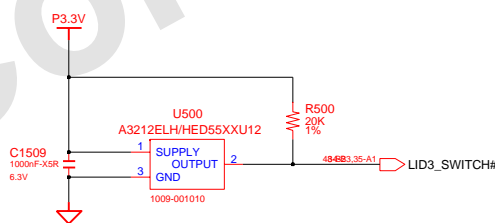
TOUCHPAD



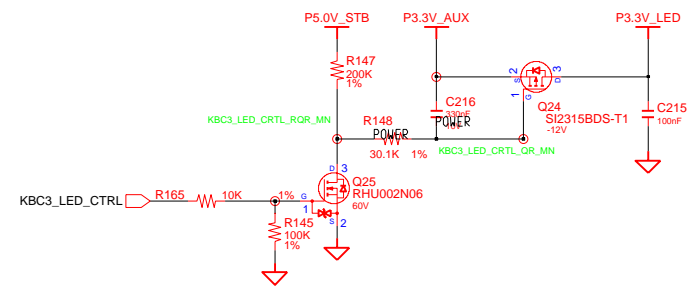
TOUCHPAD BUTTON



LID SWITCH



TOUCHPAD LED POWER

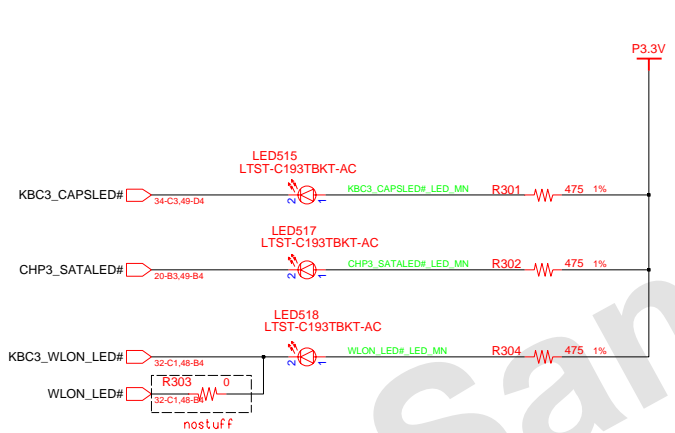


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MICOM_GLUE	PART NO.	
APPROVAL	BC LEE	REV	0.1	July 15, 2009 19:25:13 PM	PAGE	34 OF 58
MODULE CODE		LAST ENT				BA41-xxxxxA

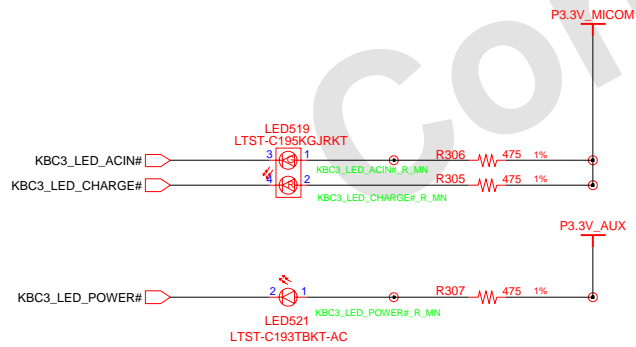
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LEDs

FUNCTION KEY LED



ADAPTERIN/CHARGING LED



Resistor	Value	Tolerance	LED	LED Type
R781	475	1%	LED501	LTST-C193TBKT-AC
R782	475	1%	LED502	LTST-C193TBKT-AC
R784	475	1%	LED503	LTST-C193TBKT-AC
R786	475	1%	LED504	LTST-C193TBKT-AC
R790	475	1%	LED505	LTST-C193TBKT-AC
R795	475	1%	LED506	LTST-C193TBKT-AC
R808	475	1%	LED507	LTST-C193TBKT-AC
R822	475	1%	LED508	LTST-C193TBKT-AC
R841	475	1%	LED509	LTST-C193TBKT-AC
R850	475	1%	LED510	LTST-C193TBKT-AC
R856	475	1%	LED511	LTST-C193TBKT-AC
R858	475	1%	LED512	LTST-C193TBKT-AC
R859	475	1%	LED513	LTST-C193TBKT-AC
R860	475	1%	LED514	LTST-C193TBKT-AC
R861	475	1%	LED516	LTST-C193TBKT-AC
R862	475	1%	LED520	LTST-C193TBKT-AC
R863	475	1%	LED522	LTST-C193TBKT-AC
R864	475	1%	LED523	LTST-C193TBKT-AC
R872	475	1%	LED524	LTST-C193TBKT-AC
R873	475	1%	LED525	LTST-C193TBKT-AC

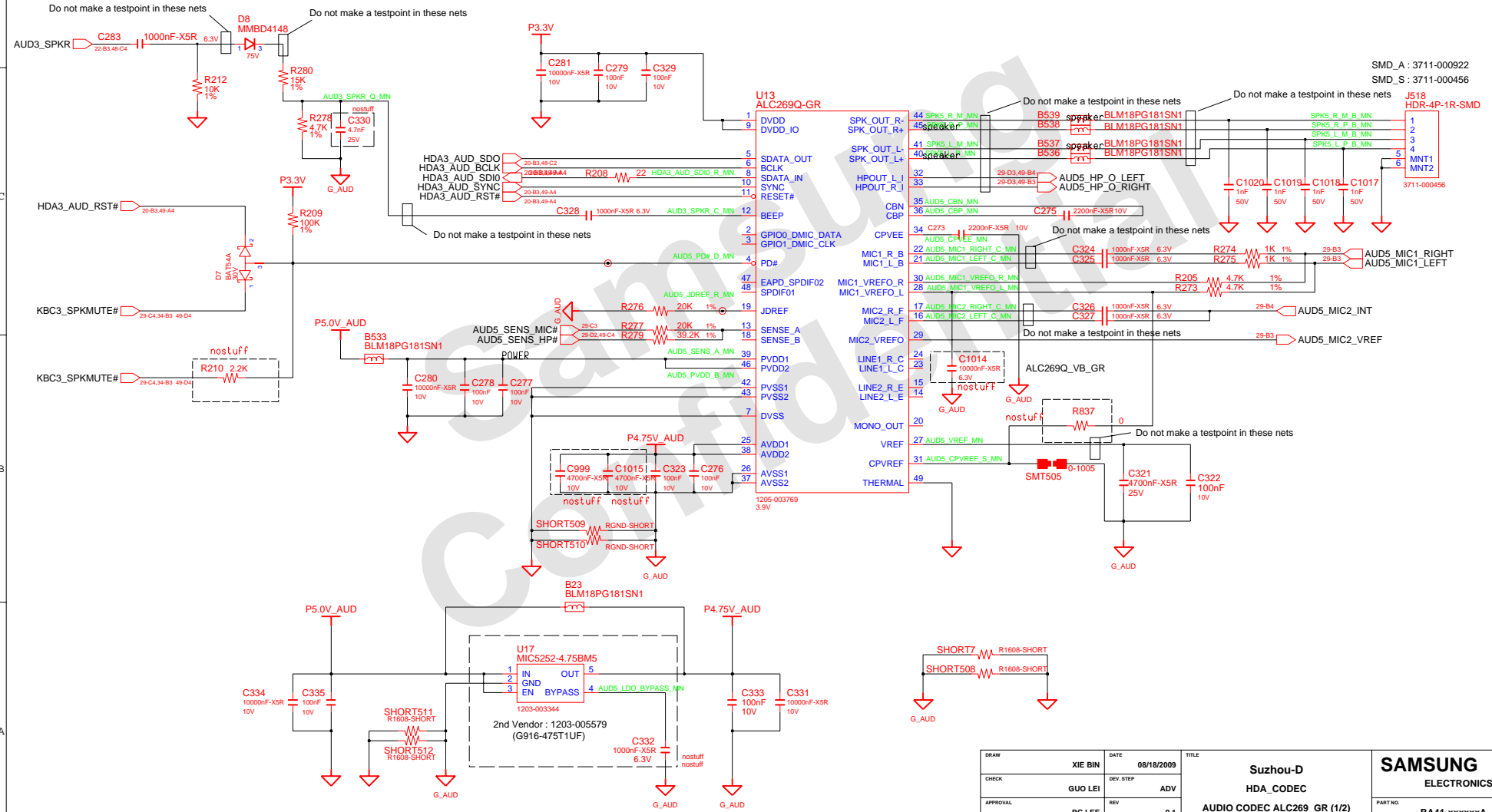
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D LED_SWITCH	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV		LED_SWITCH	
APPROVAL	BC LEE	REV	0.1		LED_SWITCH	PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM		PAGE 35 OF 58

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AUDIO CODEC (ALC269)

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



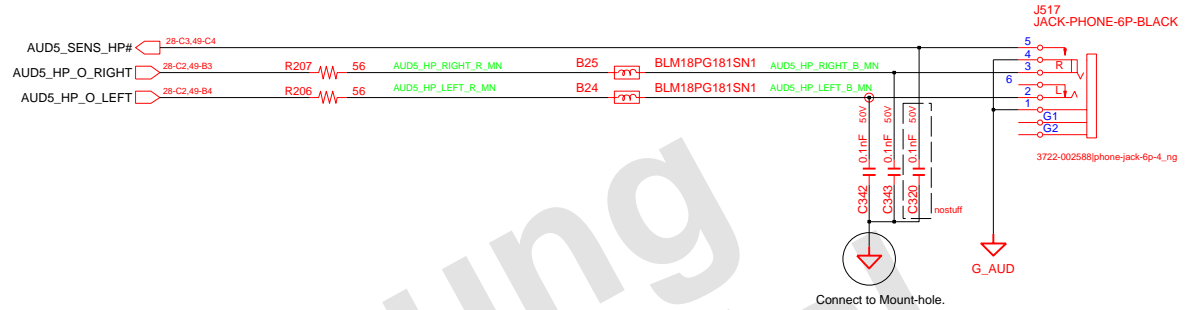
SMD_A : 3711-000922
SMD_S : 3711-000456

DRAW	XIE BIN	DATE	TITLE	Suzhou-D		SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV.STEP	ADV	HDA_CODEC		
APPROVAL	BC LEE	REV	0.1	AUDIO CODEC ALC269_GR (1/2)		PART NO. BA41-xxxxxA
MODULE CODE		LAST EXT		July 15, 2009 19:25:13 PM	PAGE	36 OF 58

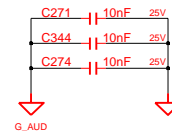
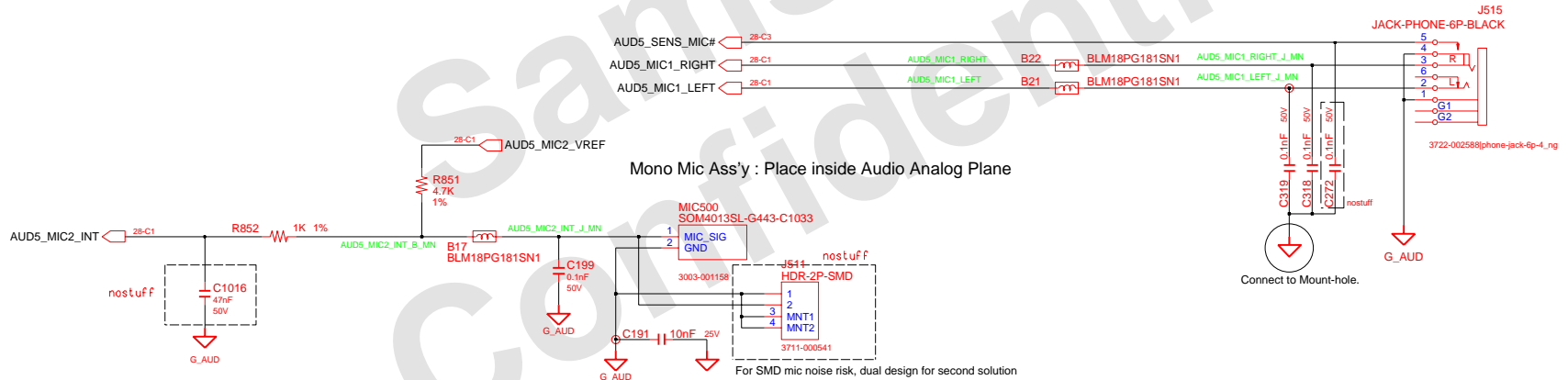
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HEADPHONE



MIC JACK

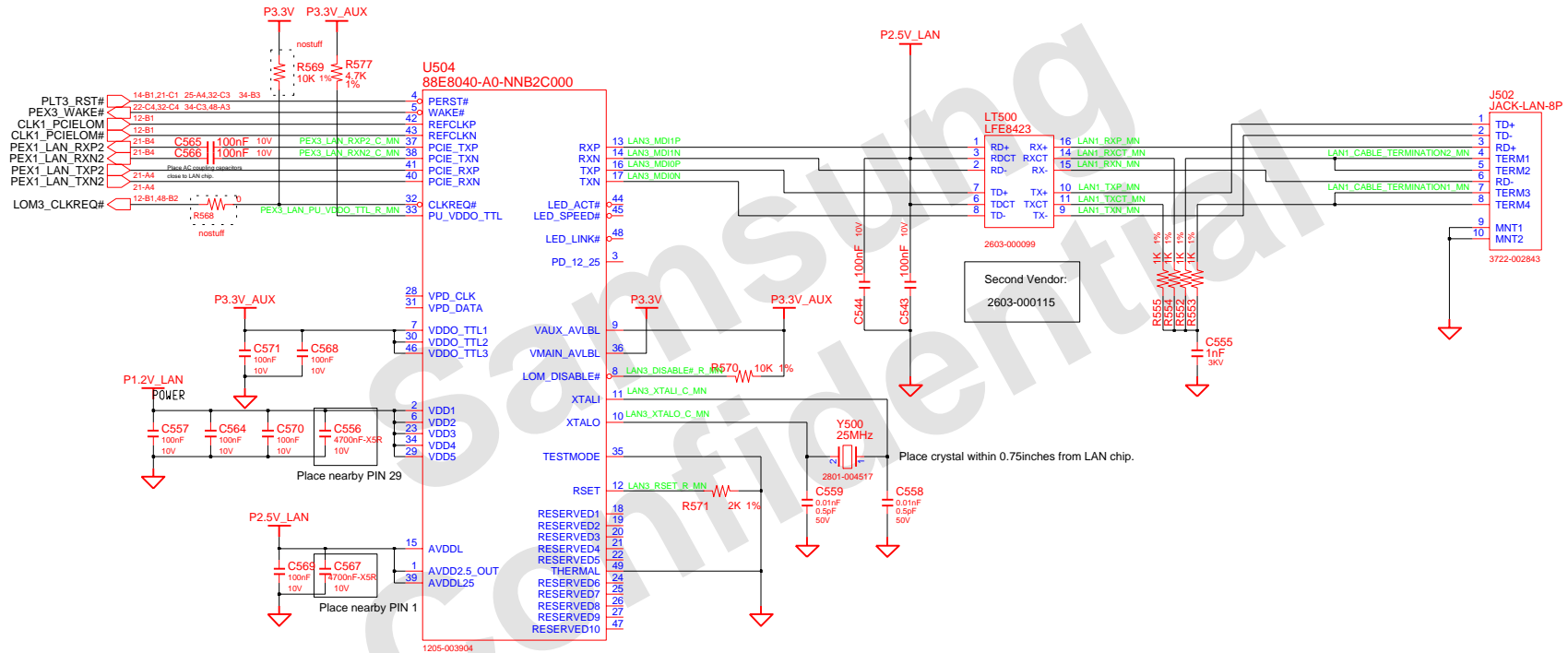


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CHECK	GUO LEI	DEV. STEP	ADV	HDA_CODEC	PART NO.	
APPROVAL	BC LEE	REV	0.1	AUDIO CODEC ALC269_GR (2/2)	BA41-xxxxxA	
MODULE CODE		LAST ENT		July 15, 2009 19:25:13 PM	PAGE 37 OF 58	

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LAN Controller (Marvell 88E8040)



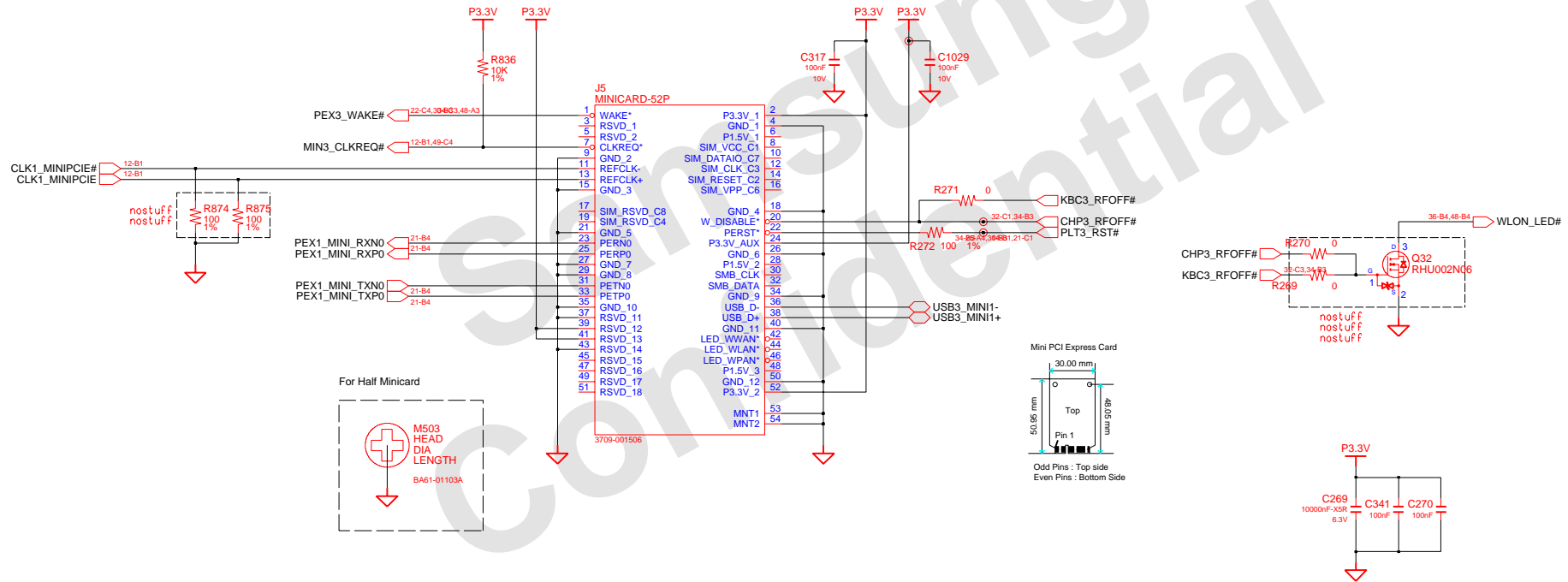
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	LAN	LAN	
APPROVAL	BC LEE	REV	0.1	LAN_Marvell 88E8040	LAN_Marvell 88E8040	PART NO. BA41-xxxxxA
MODULE CODE		LAST ENT		July 15, 2009 19:25:13 PM	PAGE	38 OF 58

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Wireless LAN

WLAN, 4mm

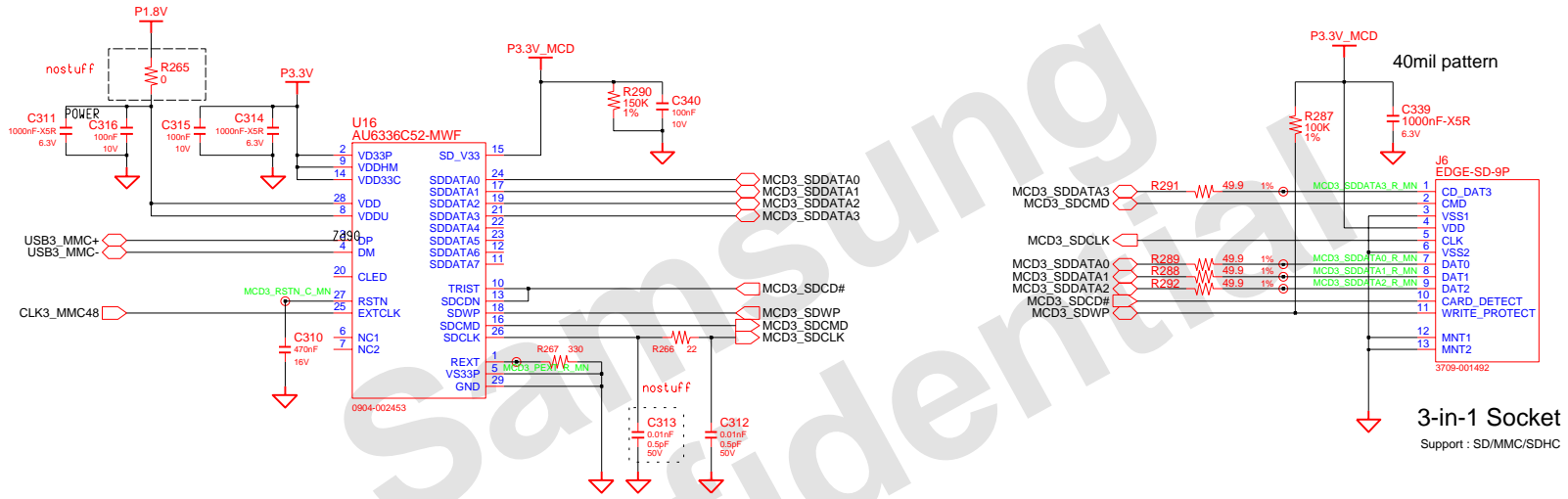


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MINI_PCIE_CONN		
APPROVAL	BC LEE	REV	0.1	Wireless LAN	PART NO.	BA41-xxxxxA
MODULE CODE		LAST ENT		July 15, 2009 19:25:13 PM	PAGE	39 OF 58

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Card Reader (AU6336)

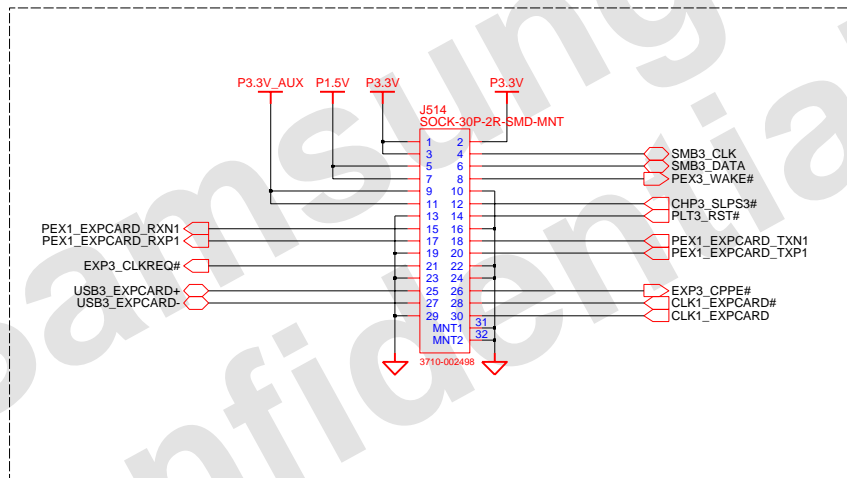


MCD3_SD_SPD	SD v1.0 Clock Option
PU / PD : No Stuff	24 MHz (default)
PU : Stuff, PD : No Stuff	15 MHz
MCD3_CLK_IN	827S Clock Source option
PU : X, PD : X	12MHz, fixed S/N
PU : No Stuff, PD : Stuff	12MHz, no S/N
PU : Stuff, PD : No Stuff	48MHz

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MULTICARD	MULTICARD	
APPROVAL	BC LEE	REV	0.1	3 IN 1 CARD	3 IN 1 CARD	
MODULE CODE		LAST ENT			July 15, 2009 19:25:13 PM	PAGE 40 OF 58

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Express Card Connector



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	EXPRESS CARD	PART NO.	
APPROVAL	BC LEE	REV	0.1		BA41-xxxxxxA	
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 41 OF 58	

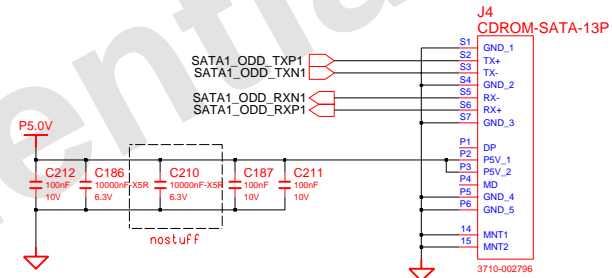
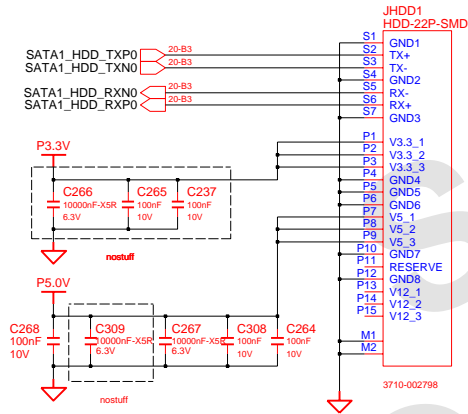
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SATA I/F CONN

SATA HDD CONN

ODD CONN



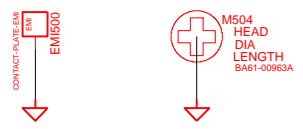
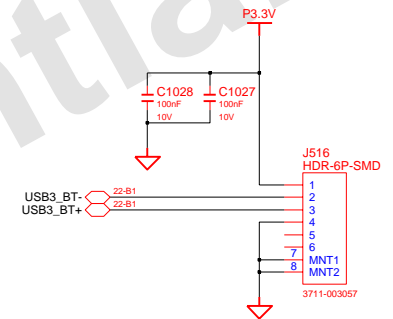
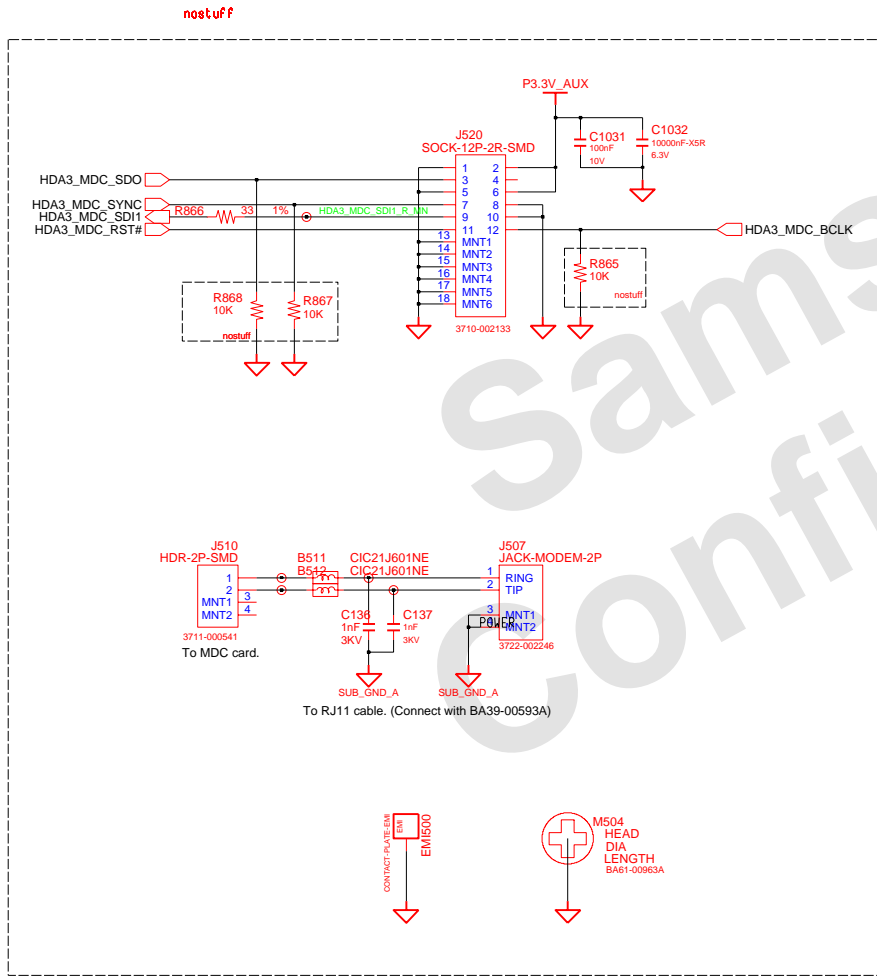
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D SATA_DEVICES	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	HDD & ODD SUB BONNECTOR	PART NO. BA41-xxxxxxA	
APPROVAL	BC LEE	REV	0.1	July 15, 2009 19:25:13 PM		PAGE 42 OF 58
MODULE CODE	LAST EDIT					

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MDC Connector

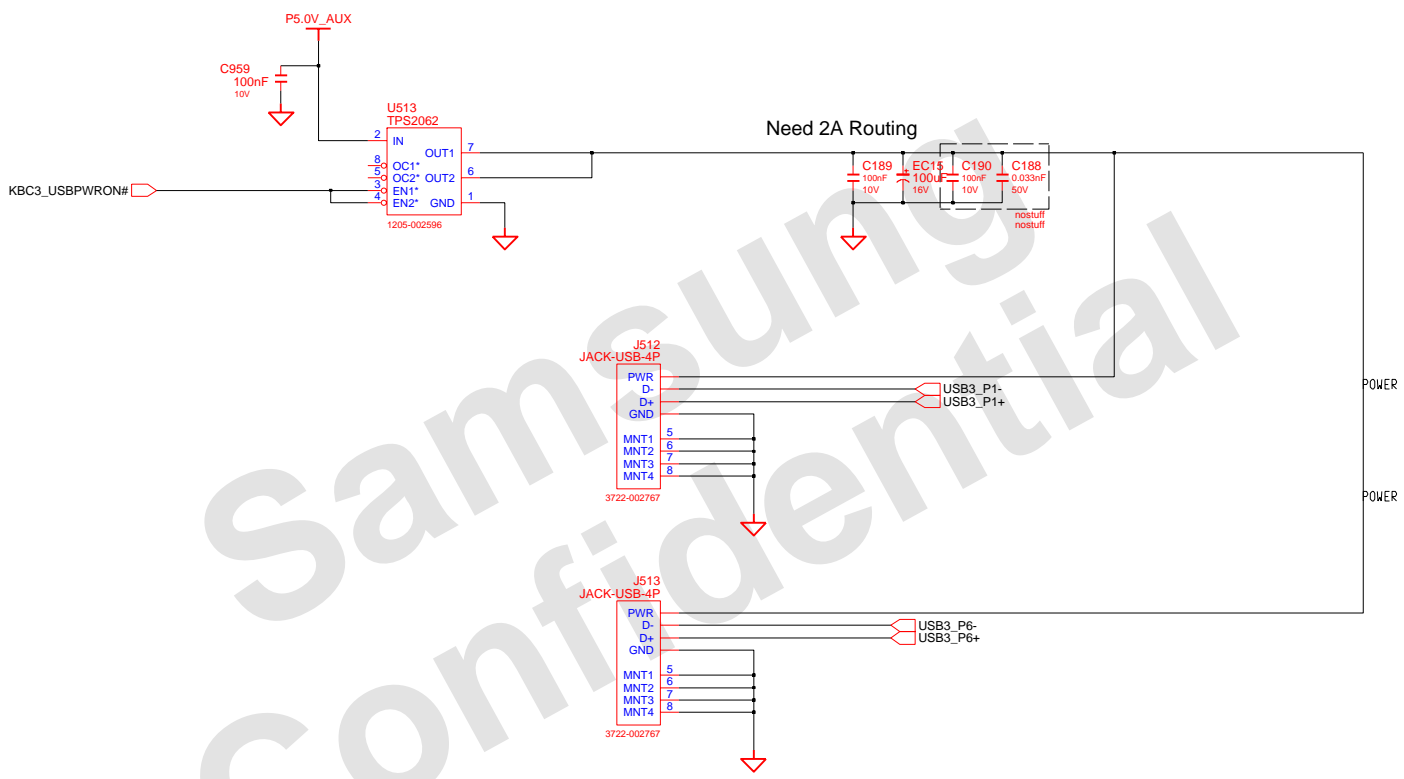
BLUETOOTH



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	HDA_MODEM & BLUETOOTH		
APPROVAL	BC LEE	REV	0.1	MODEM & BLUETOOTH		PART NO. BA41-xxxxxA
MODULE CODE	LAST EXT		July 15, 2009 19:25:13 PM		PAGE	43 OF 58

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LEFT USB PORT



Samsung
Confidential

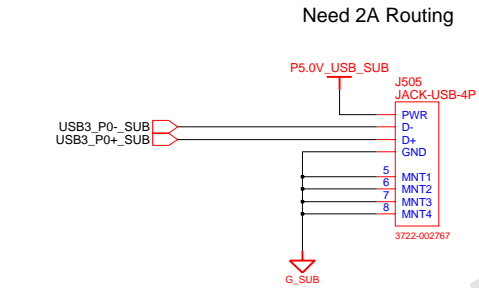
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	USB_CONNECTOR	PART NO.	
APPROVAL	BC LEE	REV	0.1	USB_CONNECTOR (1/2)	BA41-xxxxxA	
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	44	OF 58

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USB PORT & POWER S/W SUB B'D

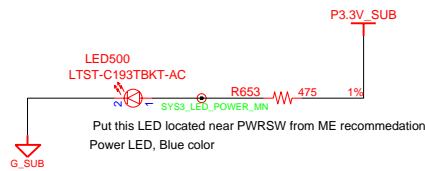
TOP RIGHT USB PORT



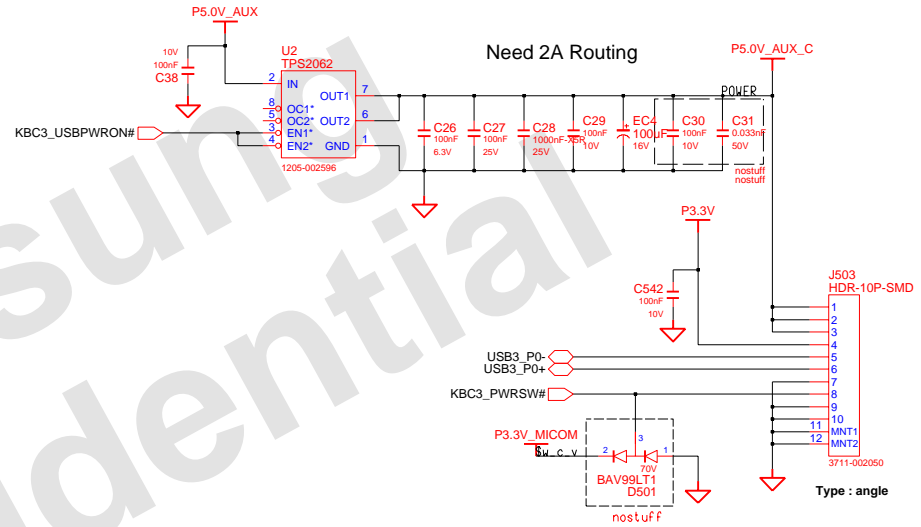
Power Button



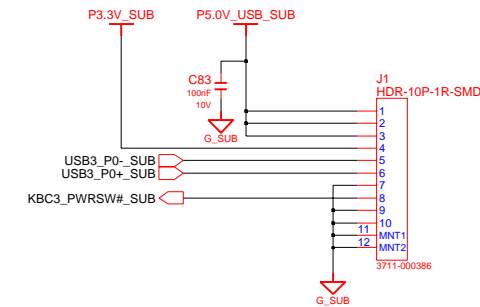
Power ON LED



MAIN TO SUB USB CONN



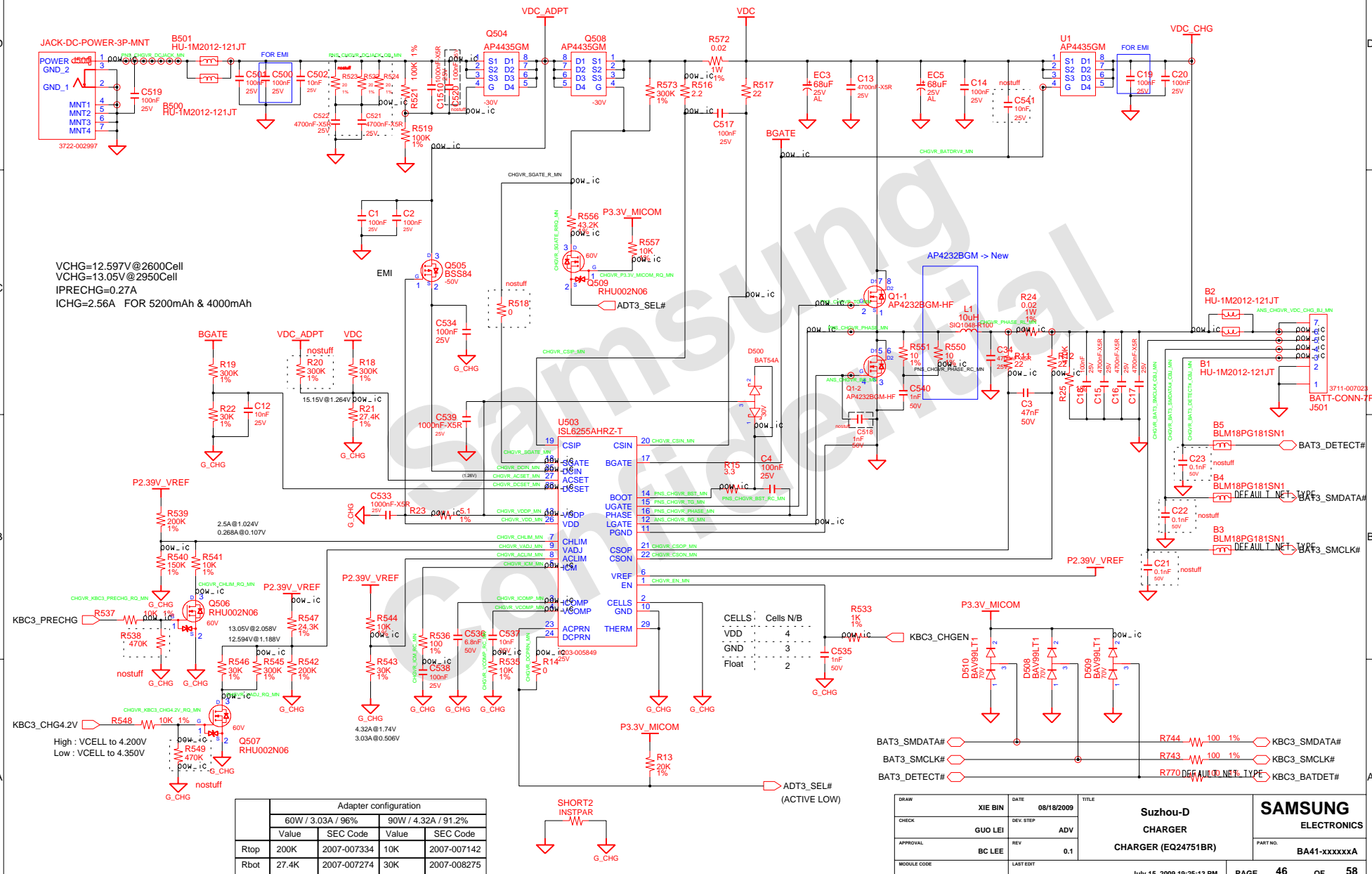
SUB TO MAIN USB CONN



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	USB_CONNECTOR	PART NO.	
APPROVAL	BC LEE	REV	0.1	USB_CONNECTOR (2/2)	BA41-xxxxxA	
MODULE CODE	LAST ENT	July 15, 2009 19:25:13 PM		PAGE	45	OF 58

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CHARGER & POWER MANAGEMENT

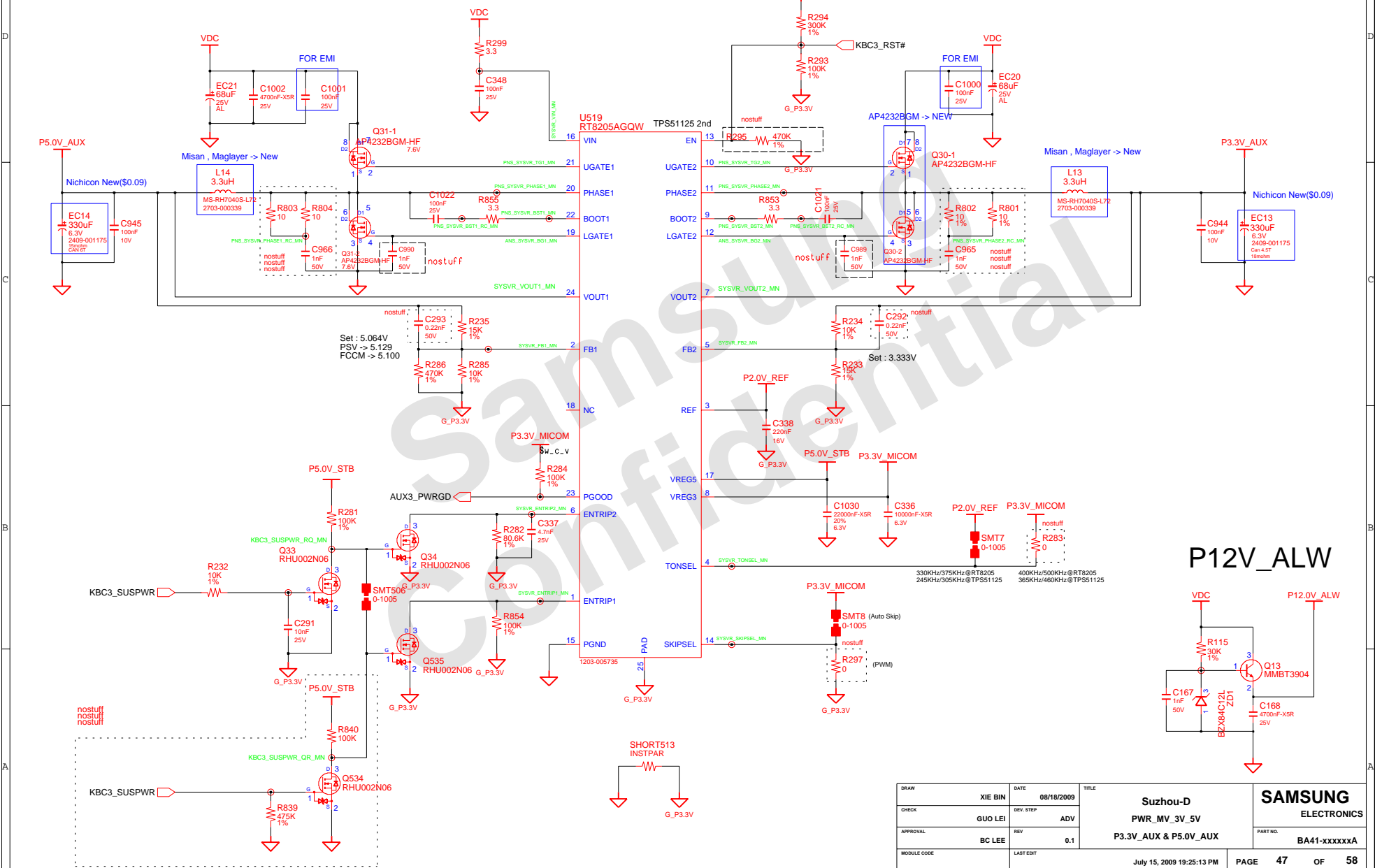


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D CHARGER	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV STEP	ADV	CHARGER (EQ24751BR)		
APPROVAL	BC LEE	REV	0.1			PART NO. BA41-xxxxxA
MODULE CODE	LAST ENT		July 15, 2009 19:25:13 PM	PAGE	46	OF 58

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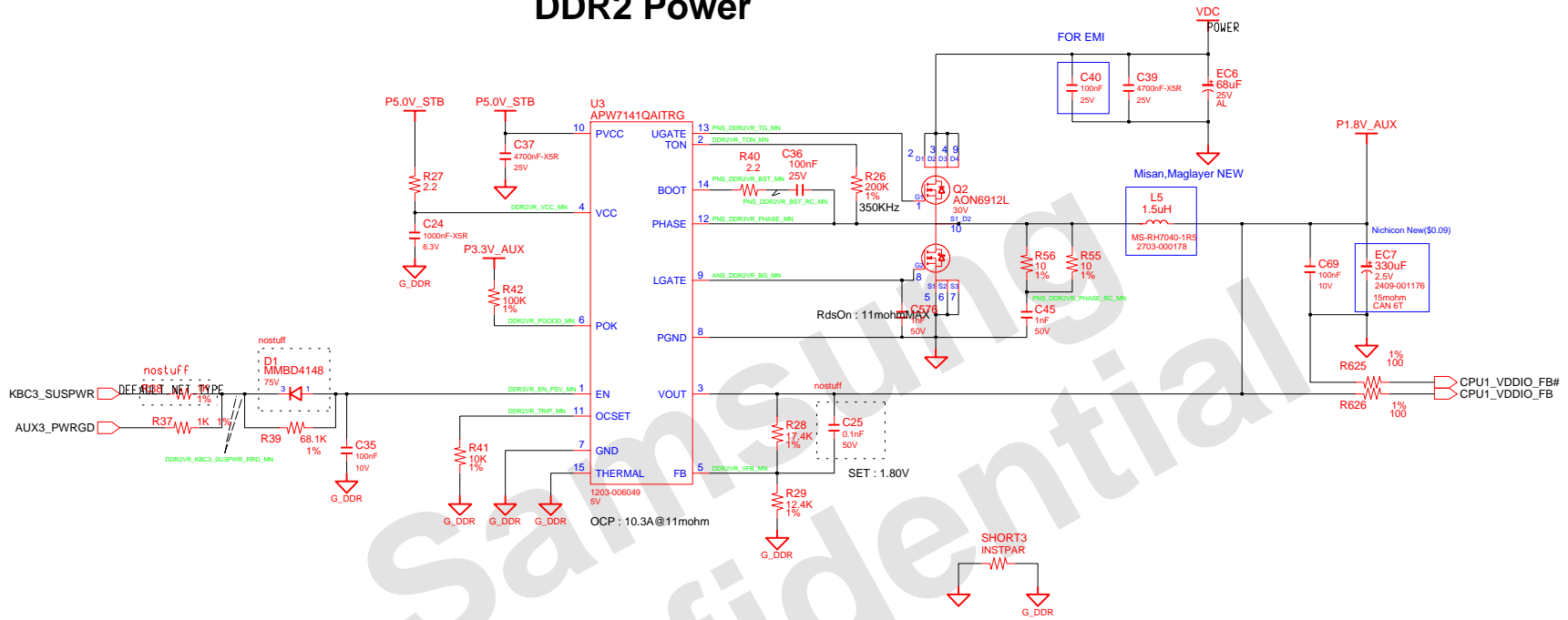
P3.3V_AUX & P5.0V_AUX



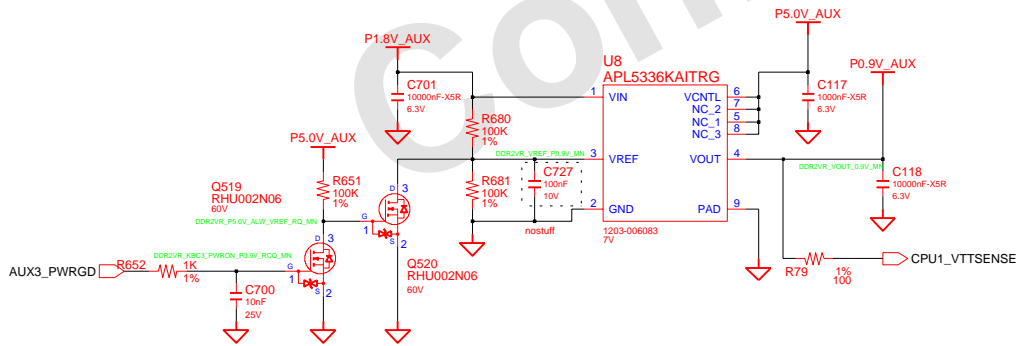
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D PWR_MV_3V_5V P3.3V_AUX & P5.0V_AUX	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1			
MODULE CODE		LAST ENT				
July 15, 2009 19:25:13 PM						PAGE 47 OF 58

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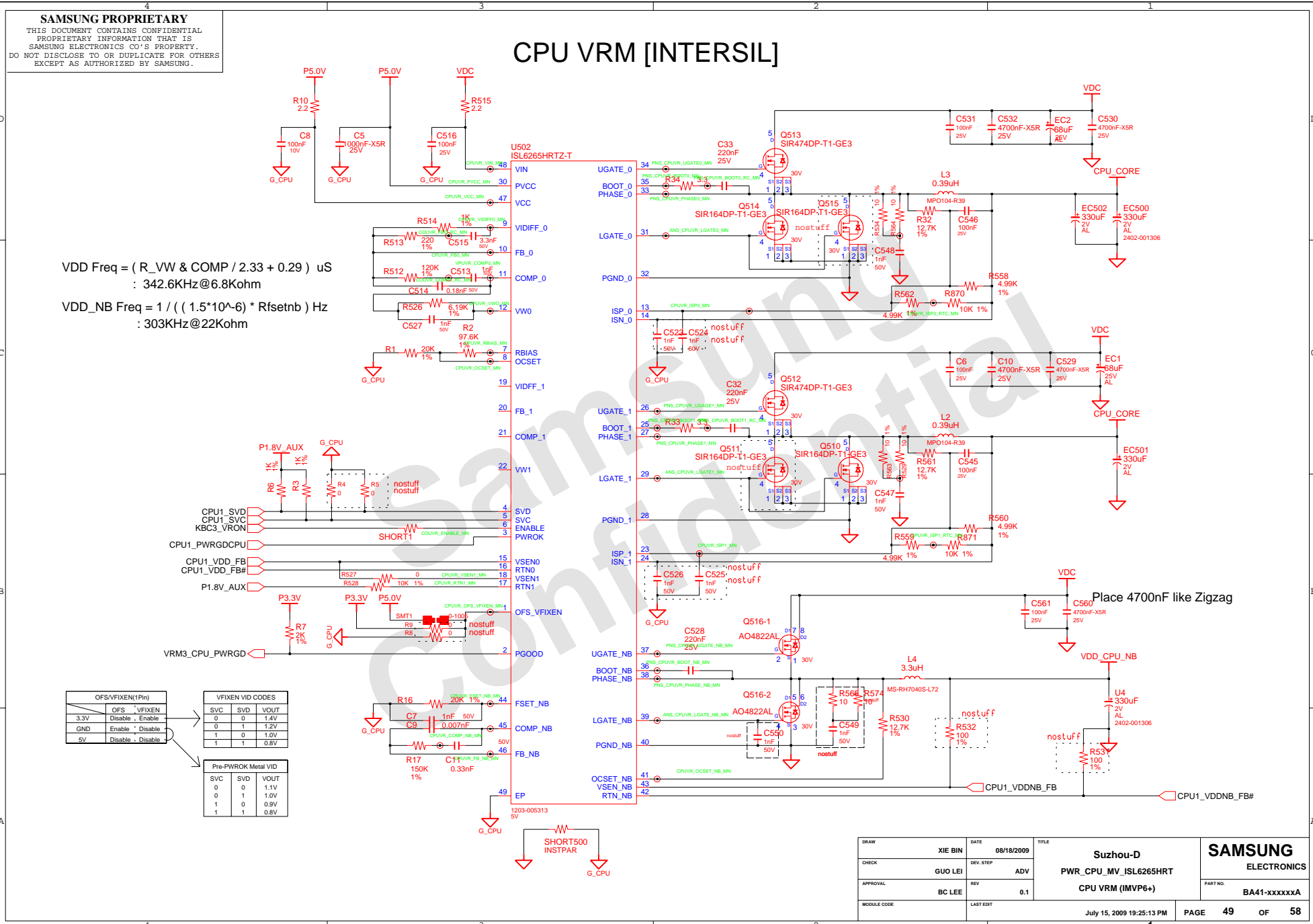
DDR2 Power



DDR2 VTT(P0.9V_AUX)



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV		PWR_MEMORY	
APPROVAL	BC LEE	REV	0.1		DDR2 POWER	PART NO. BA41-xxxxxA
MODULE CODE		LAST EXT			July 15, 2009 19:25:13 PM	PAGE 48 OF 58



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CPU VRM [INTERSIL]

$$VDD \text{ Freq} = (R_{VW} \& \text{COMP} / 2.33 + 0.29) \text{ uS}$$

$$: 342.6\text{KHz}@6.8\text{Kohm}$$

$$VDD_{NB} \text{ Freq} = 1 / ((1.5 \times 10^{-6}) * R_{fsetnb}) \text{ Hz}$$

$$: 303\text{KHz}@22\text{Kohm}$$

OFS_VFIXEN(1Pin)		VFIXEN VID CODES		
OFS_VFIXEN	VFIXEN	SVC	SVD	VOUT
3.3V	Disable, Enable	0	0	1.4V
GND	Enable, Disable	0	1	1.2V
5V	Disable, Disable	1	0	1.0V
		1	1	0.8V

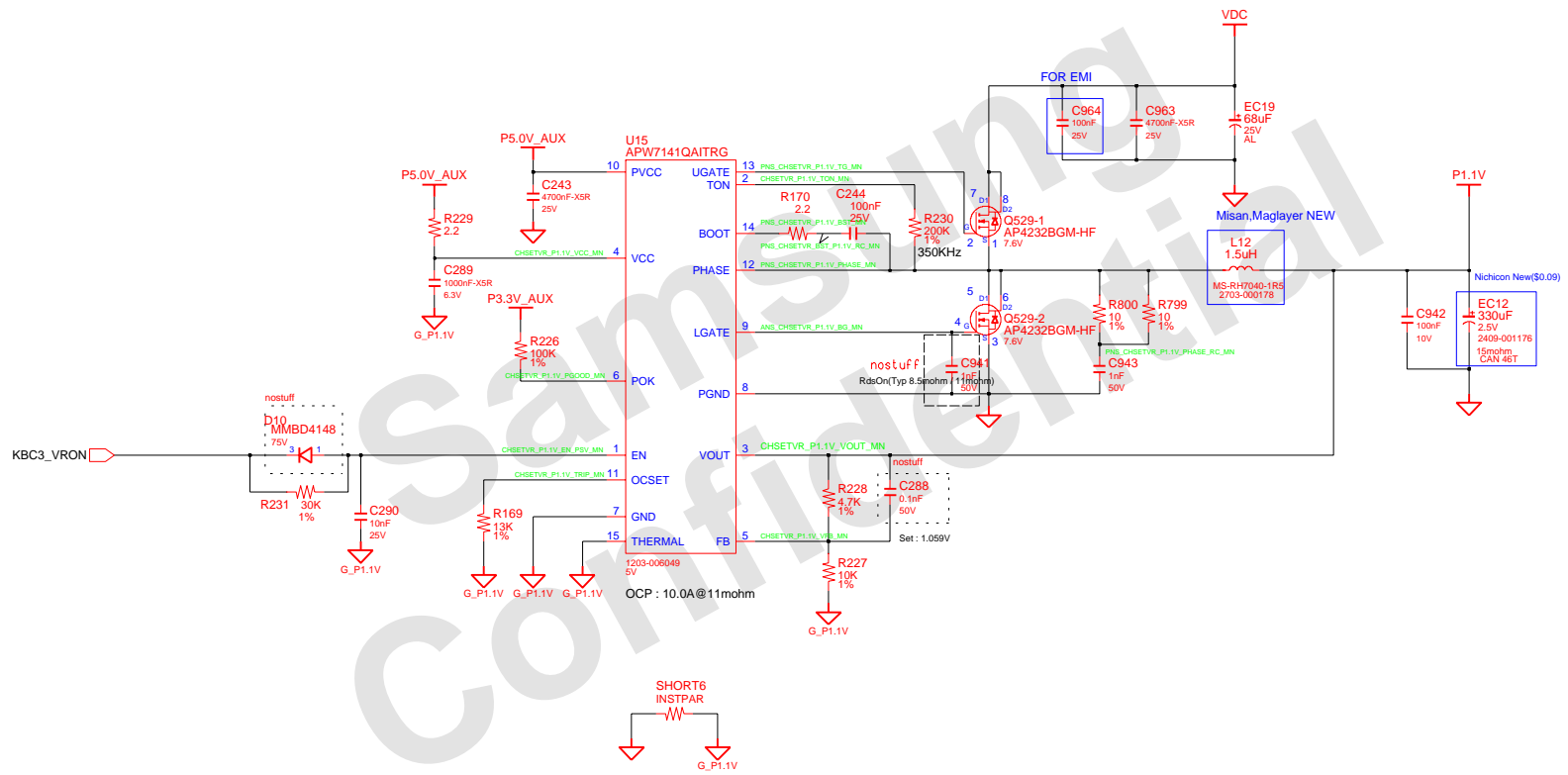
Pre-PWROK Metal VID			
SVC	SVD	VOUT	
0	0	1.1V	
0	1	1.0V	
1	0	0.9V	
1	1	0.8V	

Place 470nF like Zigzag

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	PWR_CPU_MV_ISL6265HRT		
APPROVAL	BC LEE	REV	0.1	CPU VRM (IMVP6+)		
MODULE CODE		LAST ENT		July 15, 2009 19:25:13 PM		
				PAGE	49 OF 58	

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CHIPSET POWER(P1.1V)

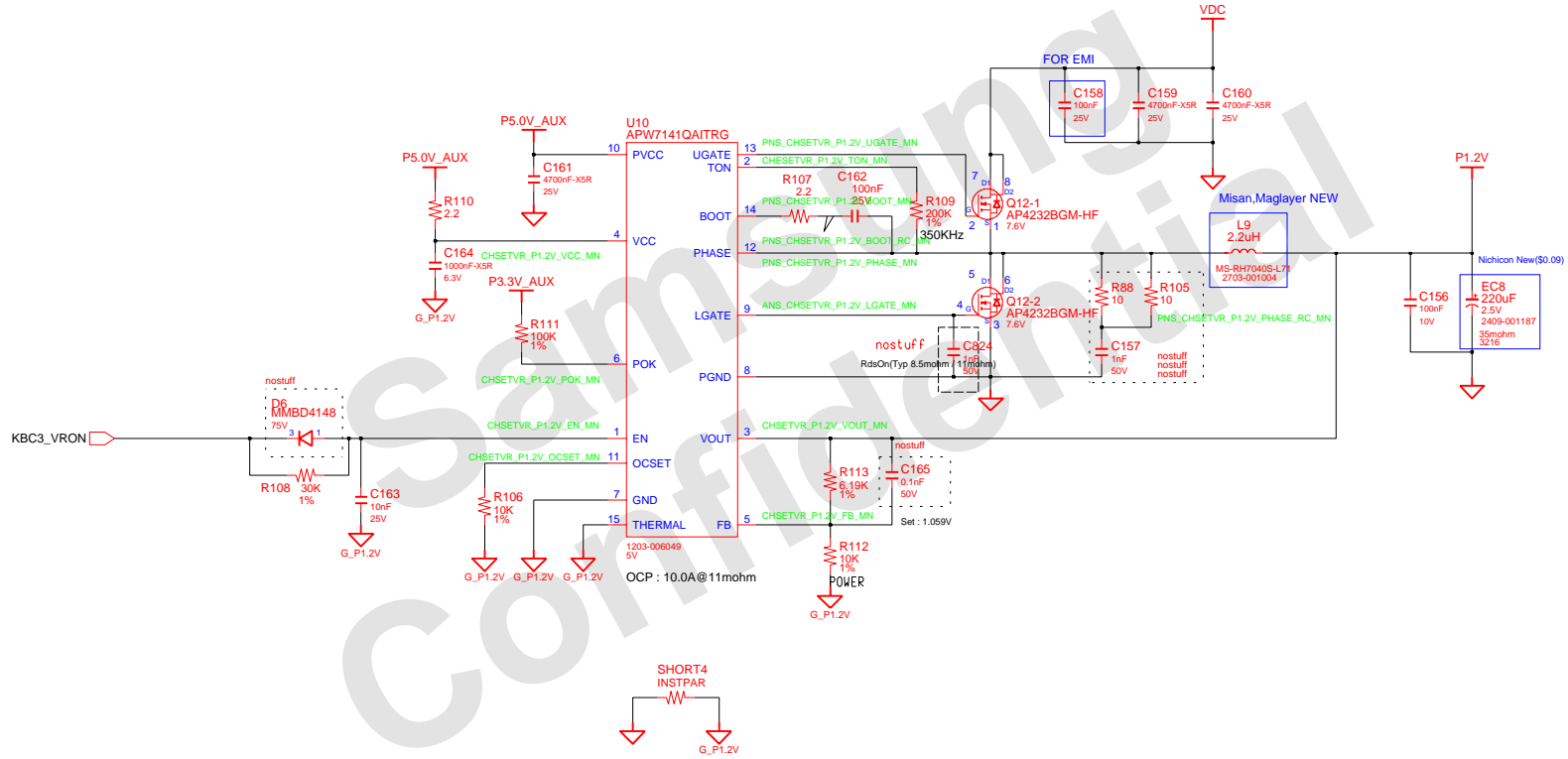


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MV_RX881	P1.1V	ELECTRONICS
APPROVAL	BC LEE	REV	0.1			PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	50	OF 58

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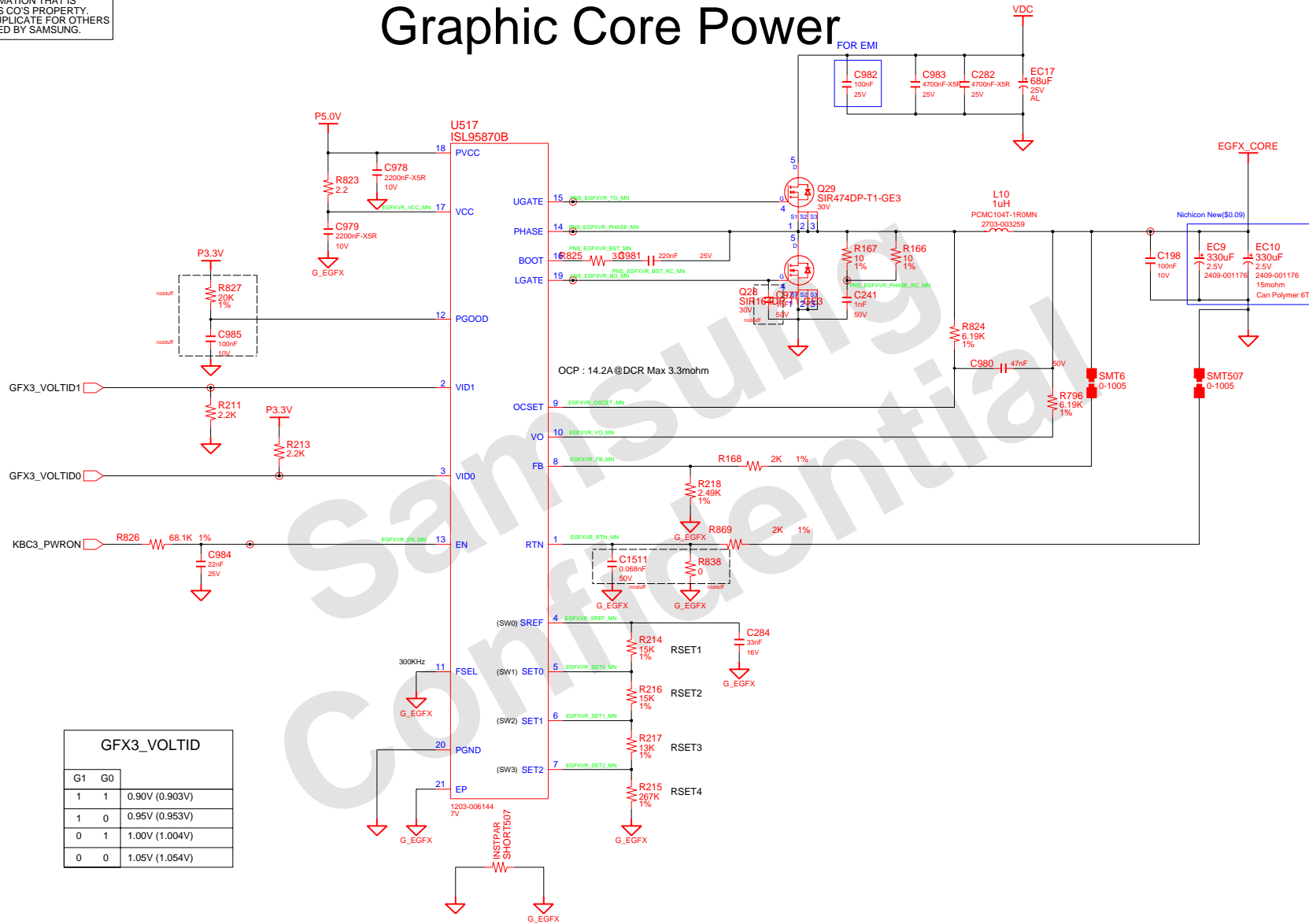
CHIPSET POWER(P1.2V)



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MV_RX881		
APPROVAL	BC LEE	REV	0.1	P1.2V		
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE 51 OF 58		

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Graphic Core Power

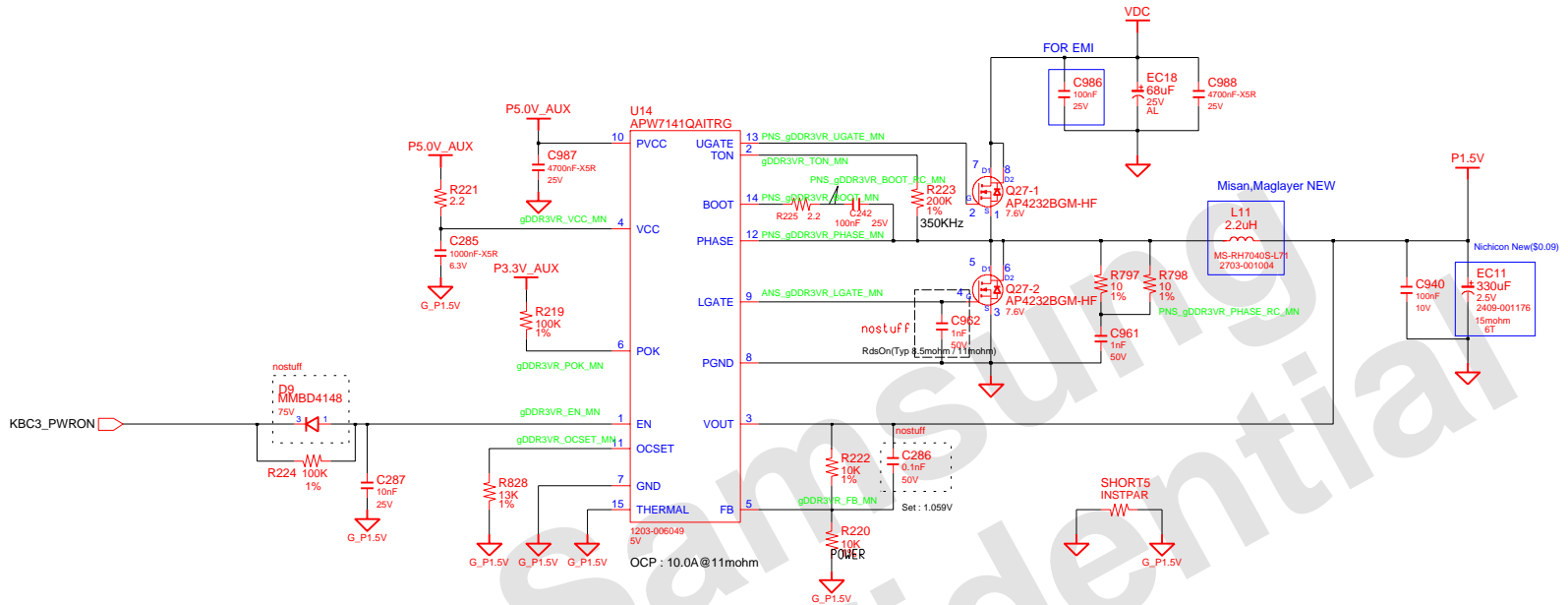


GFX3_VOLTID		
G1	G0	
1	1	0.90V (0.903V)
1	0	0.95V (0.953V)
0	1	1.00V (1.004V)
0	0	1.05V (1.054V)

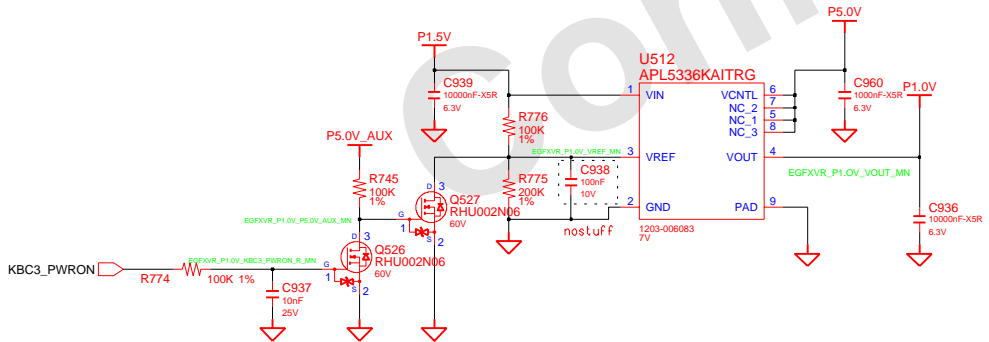
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	PWR_GFX	PWR_GFX	
APPROVAL	BC LEE	REV	0.1	GFX POWER	GFX POWER	PART NO. BA41-xxxxxA
MODULE CODE		LAST ENT			July 15, 2009 19:25:13 PM	PAGE 52 OF 58

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gDDR3 POWER(P1.5V)



P1.0V



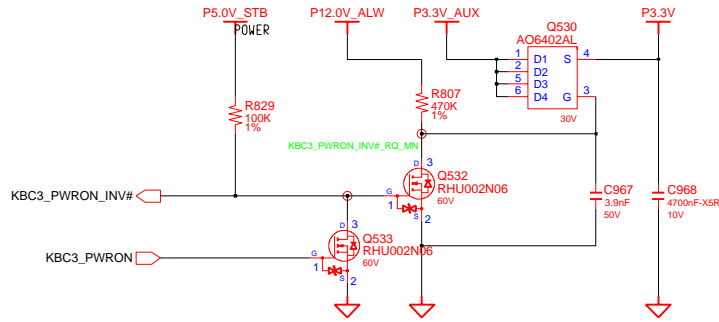
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CHECK	GUO LEI	DEV. STEP	ADV	PWR GFX MEMORY	PART NO.	
APPROVAL	BC LEE	REV	0.1	gDDR3 POWER	BA41-xxxxxA	
MODULE CODE	LAST EXT	July 15, 2009 19:25:13 PM		PAGE	53	OF 58

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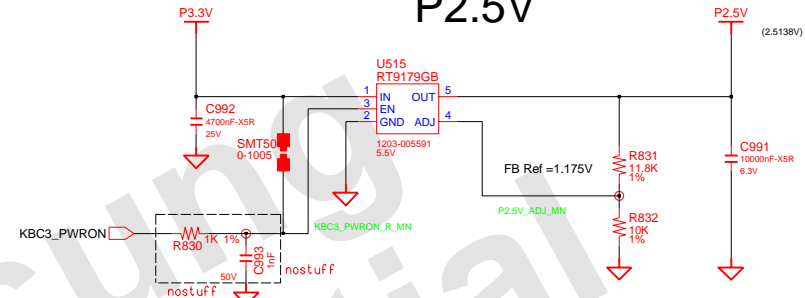
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Switched Power

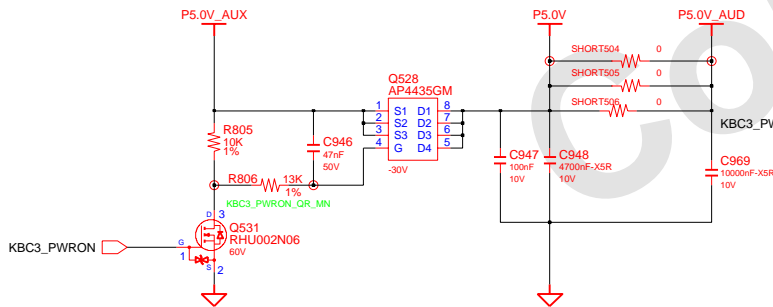
Switched Power On (P3.3V)



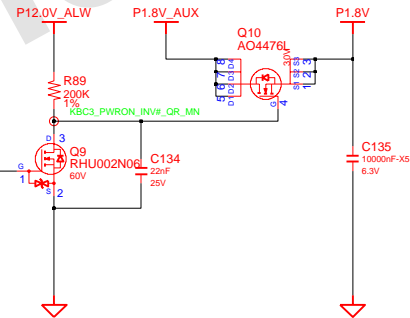
P2.5V



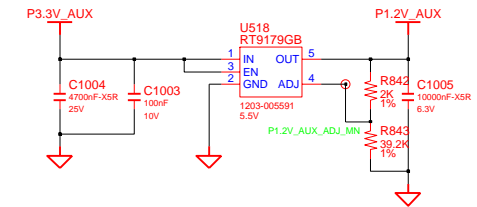
Switched Power On (P5.0V)



Switched Power On (P1.8V)



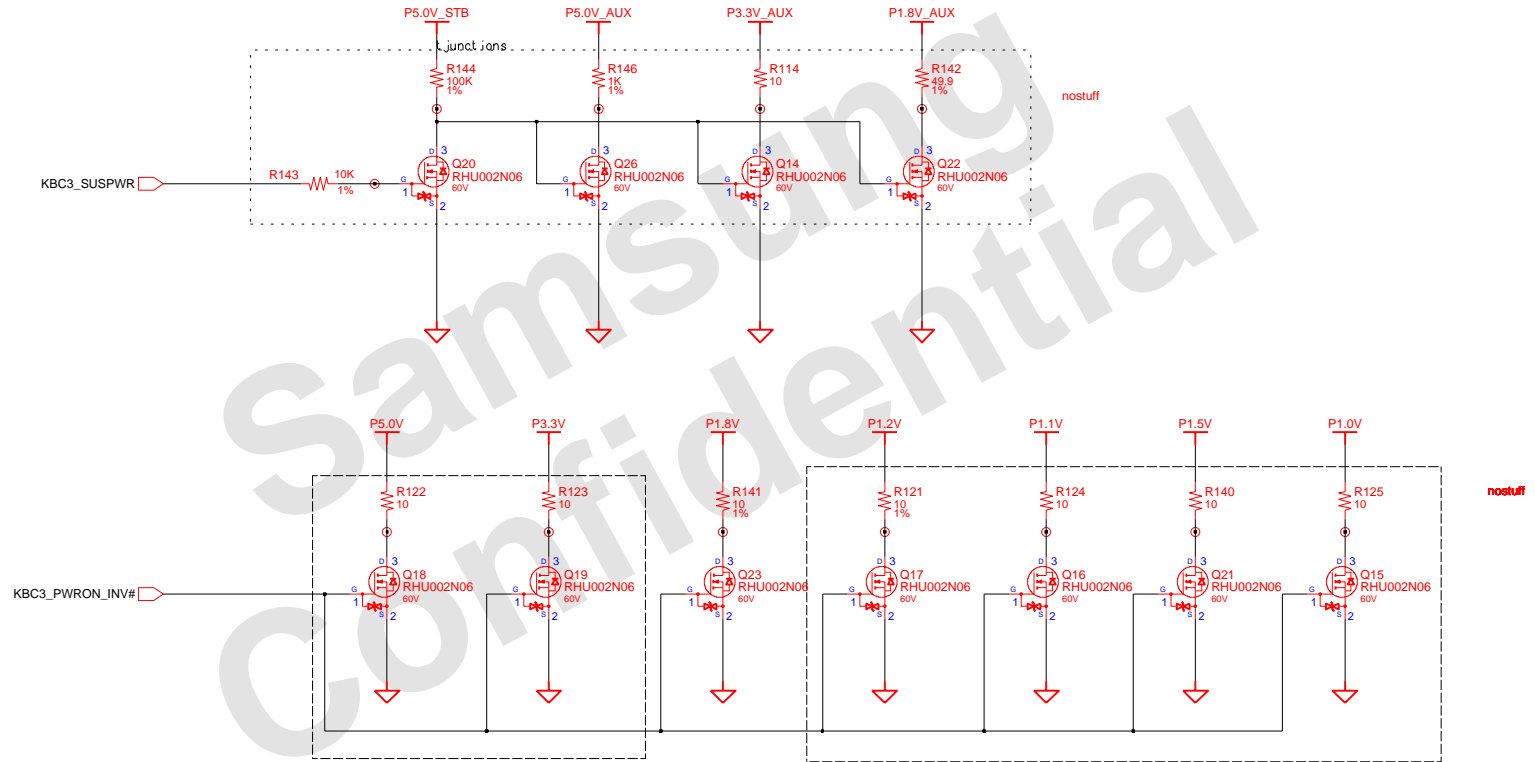
P1.2V_AUX



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	PWR_SWITCH	PAGE 54 OF 58	
APPROVAL	BC LEE	REV	0.1	SWITCH POWER	July 15, 2009 19:25:13 PM	PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT				

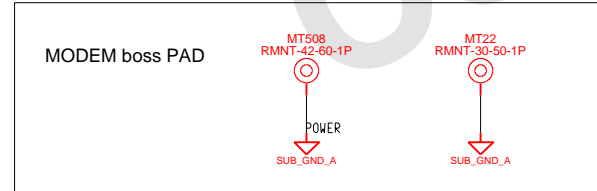
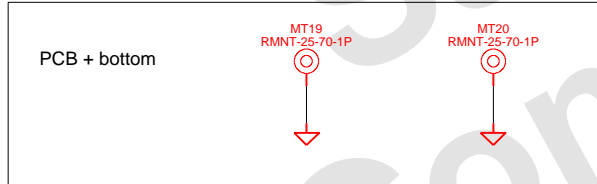
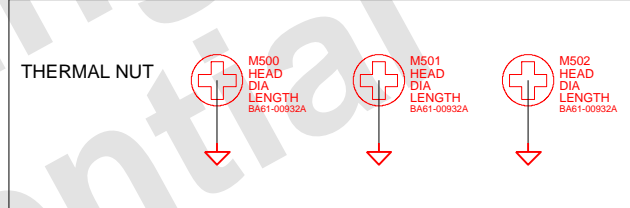
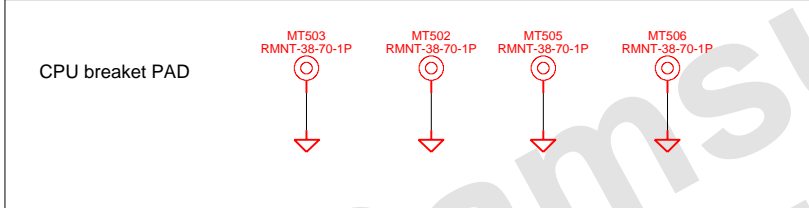
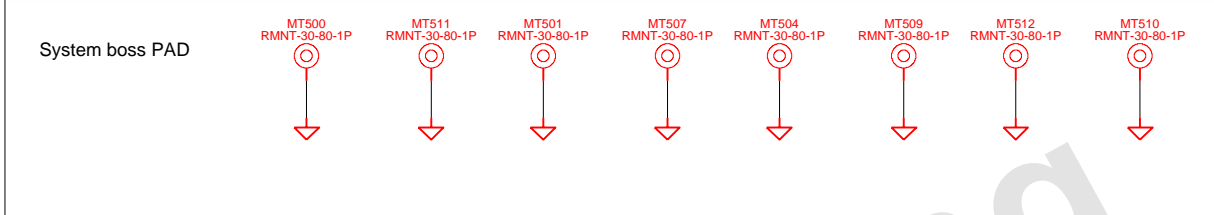
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POWER DISCHARGER



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	PWR_CPU_MV_IDISCHARGER	PART NO.	
APPROVAL	BC LEE	REV	0.1	DISCHARGER LOGIC	BA41-xxxxxA	
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 55 OF 58	

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DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D MAIN MOUNT HOLE	SAMSUNG ELECTRONICS	
CHECK	GUO LEI	DEV. STEP	ADV	PART NO.			BA41-xxxxxA
APPROVAL	BC LEE	REV	0.1	PAGE			56 OF 58
MODULE CODE	LAST EDIT		July 15, 2009 19:25:13 PM				

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○CPU1_SID
○CPU1_SVC
○CPU1_SVD
○CRT3_RED
○SMB3_CLK
○SPI3_CLK
○ADT3_SEL#
○CRT3_BLUE
○KBC3_A20G
○KBC3_VRON
○KBC3_TCLK
○LCD1_ACLK
○LCD3_BRIT
○LPC3_CLK0
○LPC3_CLK1
○MCD3_SDWP
○SMB3_DATA
○SPI3_CS0#
○SPI3_MISO
○SPI3_MOSI
○THM3_STP#
○WLON_LED#
○CRT3_GREEN
○CRT3_HSYNC
○CRT3_VSYNC
○CRT5_HSYNC
○CRT5_VSYNC
○DBG3_HSYNC
○DBG3_VSYNC
○GFX3_GPIO0
○GFX3_GPIO1
○GFX3_GPIO2
○KBC3_CHGEN
○KBC3_PWRGD
○KBC3_PWRON
○KBC3_RCIN#
○KBC3_TDATA
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○MCD3_SDCMD
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○MEM1_VREF1
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○SB_X2_C_MN
○CHGVR_EN_MN
○CHP3_GPIO16
○CHP3_GPIO17
○CHP3_RTCCCLK
○CHP3_SERIRQ
○CHP3_SLPS3#
○CHP3_SLPS5#
○CK_PDF_R_MN
○CPU1_ALERT#
○CRT3_DDCCLK
○GFX_NC_B_MN
○KBC3_BKLTON
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○KBC3_PRECHG
○KBC3_PWR3W#
○KBC3_RFOFF#
○KBC3_SCLEDF#
○KBC3_SMLCF#
○KBC3_SPI_DI
○KBC3_SPI_DO
○KBC5_KS10
○KBC5_KS11
○KBC5_KS12
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○KBC5_KS30
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○LPC3_LAD(1)
○LPC3_LAD(2)
○LPC3_LAD(3)
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○BAT3_DETECT#
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○CHGVR_VDD_MN
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○CPU1_LDTSTP#
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○EGFXVR_VO_MN
○EXP3_CLKREQ#
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○KBC3_CHG4.2V
○KBC3_EXTSMI#
○KBC3_NUMLED#
○KBC3_PWRBTN#
○KBC3_RSMRST#
○KBC3_RUNSDF#
○KBC3_SMDATA#
○KBC3_SPI_CLK
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○KBC5_KS0(11)
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○KBC5_KS0(13)
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○CHGVR_CSIP_MN
○CHGVR_CSON_MN
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○CHGVR_DCIN_MN
○CHGVR_VADJ_MN
○CHGVR_VDDP_MN
○CHP3_NB_PWRGD
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○CHP3_SB_TEST0
○CHP3_SB_TEST2
○CHP3_SUSTAT#
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○CPU1_VDONS_FB
○CPU1_VTTSENSE
○CRT3_RED_L_MN
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○DDR2VR_VCC_MN
○DDR2VR_VFB_MN
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○EGFXVR_VCC_MN

- GDDR3VR_EN_MN
○GDDR3VR_FB_MN
○GFX_RSET_R_MN
○KBC3_CAPSLED#
○KBC3_LED_CTRL
○KBC3_SPI_CS0#
○KBC3_SPMUTE#
○KBC3_WAKESDF#
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○PEG5_HDMI_CLK
○VGA5_HDMI_HPD
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○CHGVR_ACSET_MN
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○CHGVR_OCSET_MN
○CHGVR_ICOMP_MN
○CHGVR_SGATE_MN
○CHGVR_VCOMP_MN
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○CHP3_INTRUDER#
○CHP3_THRMTRIP#
○CPU1_THRMTRIP#
○CPU1_VDDIO_FB#
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○EGFXVR_SETO_MN
○EGFXVR_SET1_MN
○EGFXVR_SET2_MN
○EGFXVR_SREF_MN
○KBC3_POK_MN
○GDDR3VR_TON_MN
○GDDR3VR_VCC_MN
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○KBC3_USBPWRON#
○KBC3_WLON_LED#
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○PEG3_HDMI_DATA
○PEG5_HDMI_DATA
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○TPDS_R_BUTTON#
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○KBC3_EMDAT_R_MN
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○KBC3_PWR3W#_SUB
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○ANS_SYSVR_BG2_MN
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○GFX_DPC_CALR_R_MN
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○PEG5_HDMI_CLK_B_MN
○VGA5_HDMI_HPD_R_MN
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○CHSETVR_P1.2V_FB_MN
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○GFX_PWRGOOD_R_MN
○PNS_DDR2VR_PHASE_RC_MN
○PNS_GDDR3VR_BOOT_RC_MN
○PNS_SYSVR_PHASE2_RC_MN

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○NB_REFCLK_N_PWM_GPIO3_R_MN
○PNS_CHSETVR_P1.1V_PHASE_MN
○PNS_CHSETVR_P1.2V_PHASE_MN
○PNS_CHSETVR_P1.2V_LGATE_MN
○DDR2VR_P5.0V_ALW_VREF_RO_MN
○PNS_CHSETVR_BST_P1.1V_RC_MN
○EGFXVR_P1.0V_KBC3_PWRON_R_MN
○PNS_CHSETVR_P1.2V_BOOT_RC_MN
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○PNS_CHSETVR_P1.2V_PHASE_RC_MN
○DDR2VR_KBC3_PWRON_P0.9V_RCQ_MN
○AVDD
○A2VDD
○A2VDDQ
○CPU_CORE
○CPU_CORE
○DPC_PVDD
○DPC_VDD18
○G_CHG
○G_CPU
○G_DDR
○G_SUB
○G_EGFX
○G_P1.1V
○G_P1.2V
○G_P1.5V
○G_P3.3V
○LCD_VDD3V
○P1.0V
○P2.5V
○P0.9V_AUX
○P1.2V_AUX
○P1.2V_LAN
○P1.8V_AUX
○P2.0V_REF
○P2.5V_LAN
○P3.3V_LED
○P3.3V_LED
○VDD_LED
○P3.3V_MCD
○P3.3V_MCD
○P3.3V_SUB
○P5.0V_AUX
○P5.0V_AUX
○P5.0V_STB
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○P12.0V_ALW
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○SPW10
○SUB_GND_A
○VDC
○GFX_PWRGOOD_R_MN
○VDD1D1
○VDD2D1
○VCC_CRT

○VCC_CRT
○VDD_LED

Table with columns: DRAW, CHECK, APPROVAL, MODULE CODE, XIE BIN, GUO LEI, BC LEE, DATE, DEV_STEP, REV, 08/18/2009, ADV, 0.1, TITLE, Suzhou-D Test Point, SAMSUNG ELECTRONICS, PART NO. BA41-xxxxxA, July 15, 2009 19:25:13 PM, PAGE 57 OF 58