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BONN-INT

CPU : Intel Penryn
 Chip Set : Intel Cantiga & ICH9M
 Remarks : Montevina Platform

Model Name : BONN-INT
 PBA Name : MAIN
 PCB Code : GCE : BA41-01039A
 NAN : BA41-01040A
 HAN : BA41-01041A
 Dev. Step : PR
 Revision : 1.0
 T.R. Date : 2009.02.03

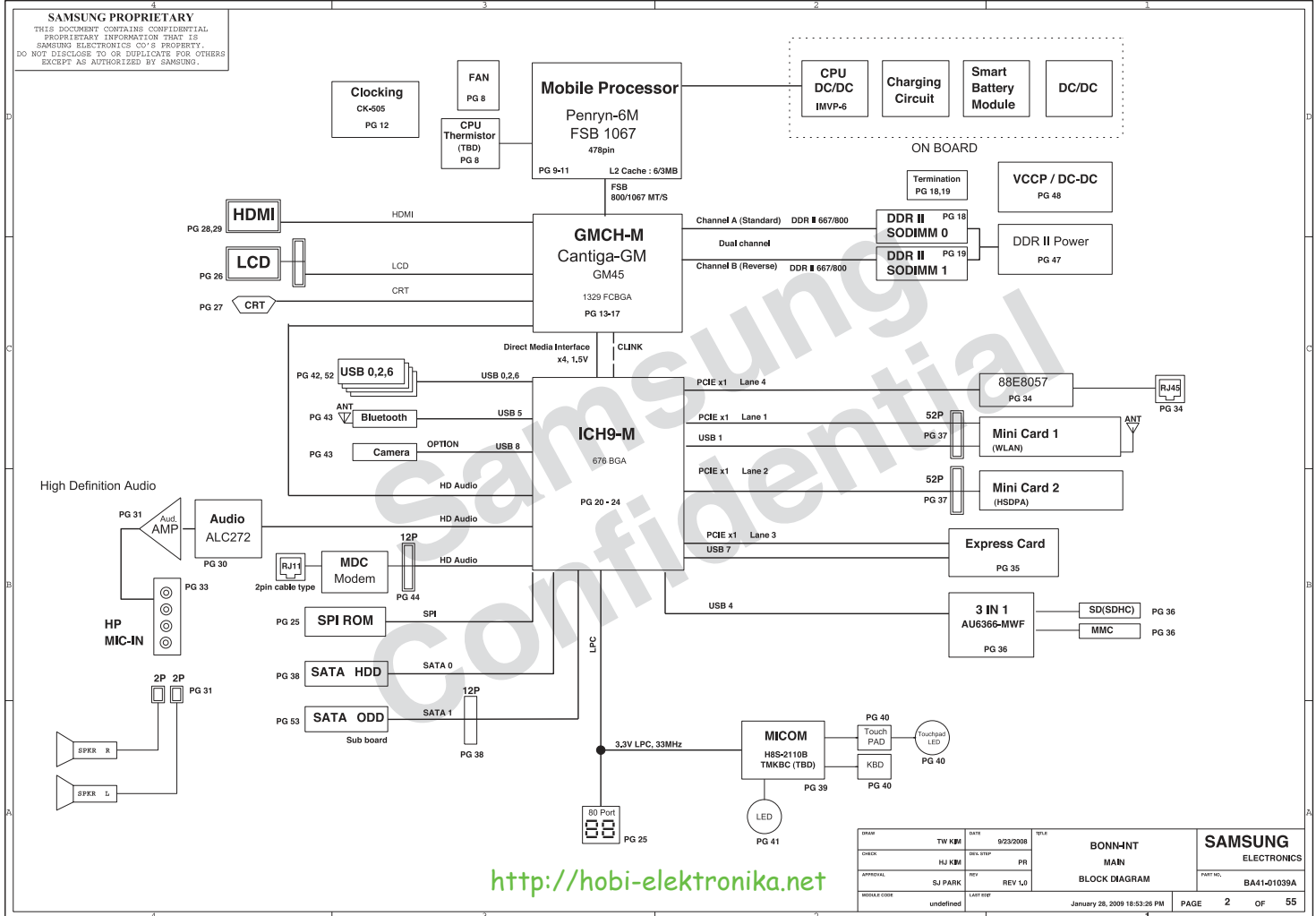
Design	CHECK	APPROVAL

■ Owner : SEC Mobile R & D

Signature : <http://kobi-elektronika.net>

DRAW	TW KIM	DATE	10/10/2008	TITLE	BONN-INT MAIN COVER	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	PR			
APPROVAL	SJ PARK	REV	REV 1.0		PART NO.	BA41-01039A
MODULE CODE		LAST EDIT		January 28, 2009 18:53:26 PM	PAGE	1 OF 55

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DESIGN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEL. STMP	PR	MAIN		
APPROVAL	SJ PARK	REV	REV 1.0	BLOCK DIAGRAM		PART NO. BA41-01039A
MODEL CODE	undefined	LAST EDIT		January 28, 2009 18:53:26 PM	PAGE	2 OF 55

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A, B, C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHC1) : H
Hub to PCI LPC bridge/IDE/AC97/SMBUS	AD30(internal) AD31(internal)	- -	B B
Internal MAC AC Link GLAN	AD24(internal) - -	- - -	HE B F

Voltage Rails

VDC_CORE	Primary DC system power supply (7 to 21V)
GFX_CORE	Core Voltage for CPU
P1.0V (VCCP)	Core Voltage for GPU
P3.3V_MICOM	VTT for CPU, Crestina & ICH8-M 3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 001x	7Ah	Thermal Sensor
SODIMM0	1010 000x	60h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	50h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	NC
1	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
2	SYSTEM PORT 2	2	NC
3	NC	3	NC
4	NC	4	LDM
5	Bluetooth	5	Mini Card 2 (ROBSON or DVB-T)
6	Mini PCI Express 2		
7	Camera		
8	NC		
9	NC		

REVISION HISTORY

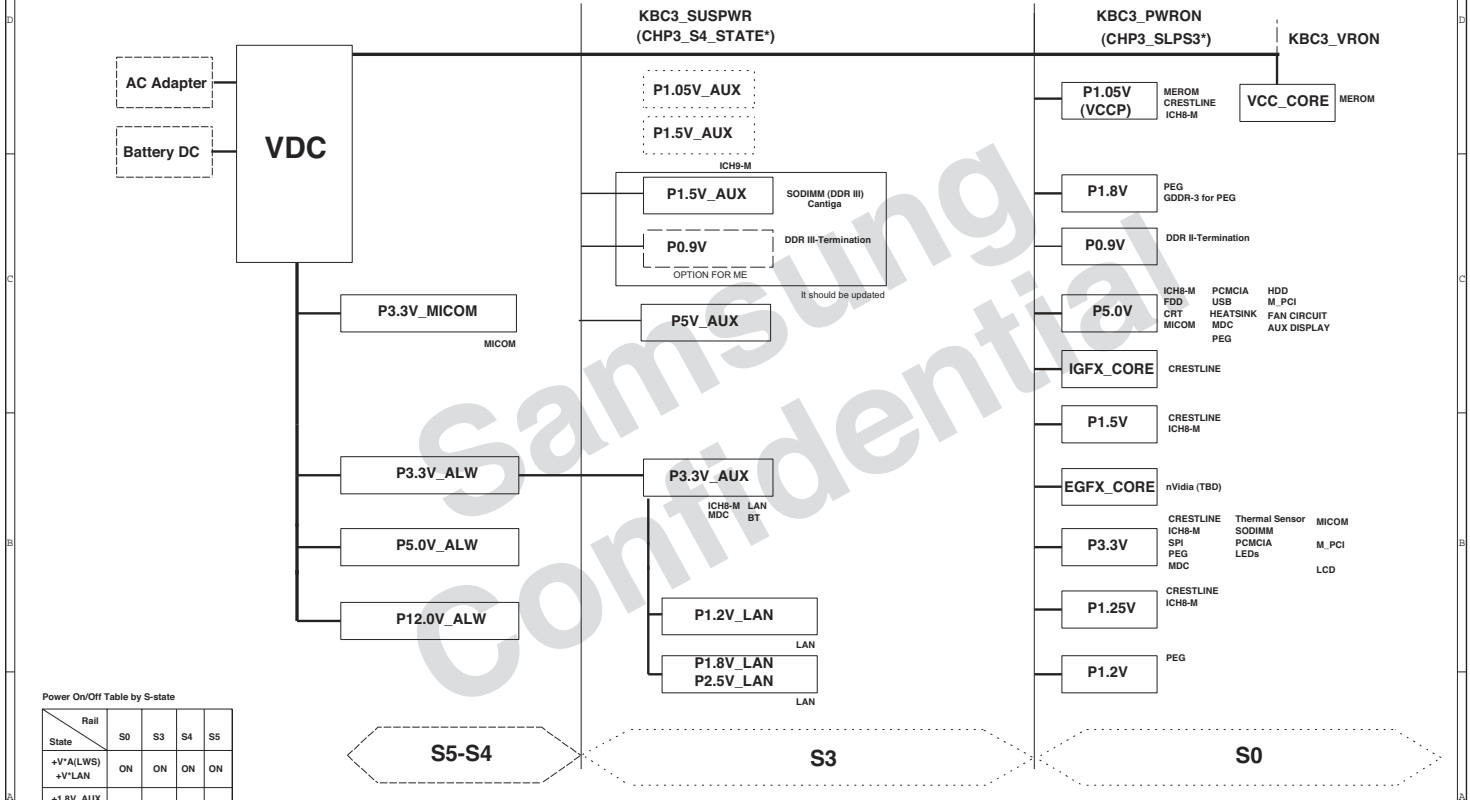
See rev notes for more information.

DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT MAIN BOARD INFO		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR				PART NO.
APPROVAL	SJ PARK	REV	REV 1.0				BA41-01039A
MODULE CODE	undefined	LAST EDIT		January 28, 2009 18:53:26 PM	PAGE	3	OF 55

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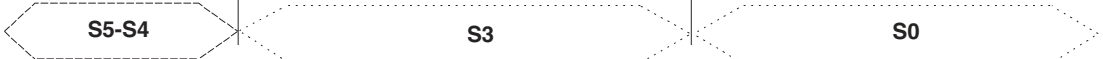
POWER DIAGRAM

Rev 0.1



Power On/Off Table by S-state

State \ Rail	S-state				
	S0	S3	S4	S5	
+V*(LWS)	ON	ON	ON	ON	
+V*LAN	ON	ON	ON	ON	
+1.8V_AUX +0.9V	ON	ON	---	---	
+V*AUX	ON	ON	---	---	
+V	ON	---	---	---	
+V* (CORE)	ON	---	---	---	



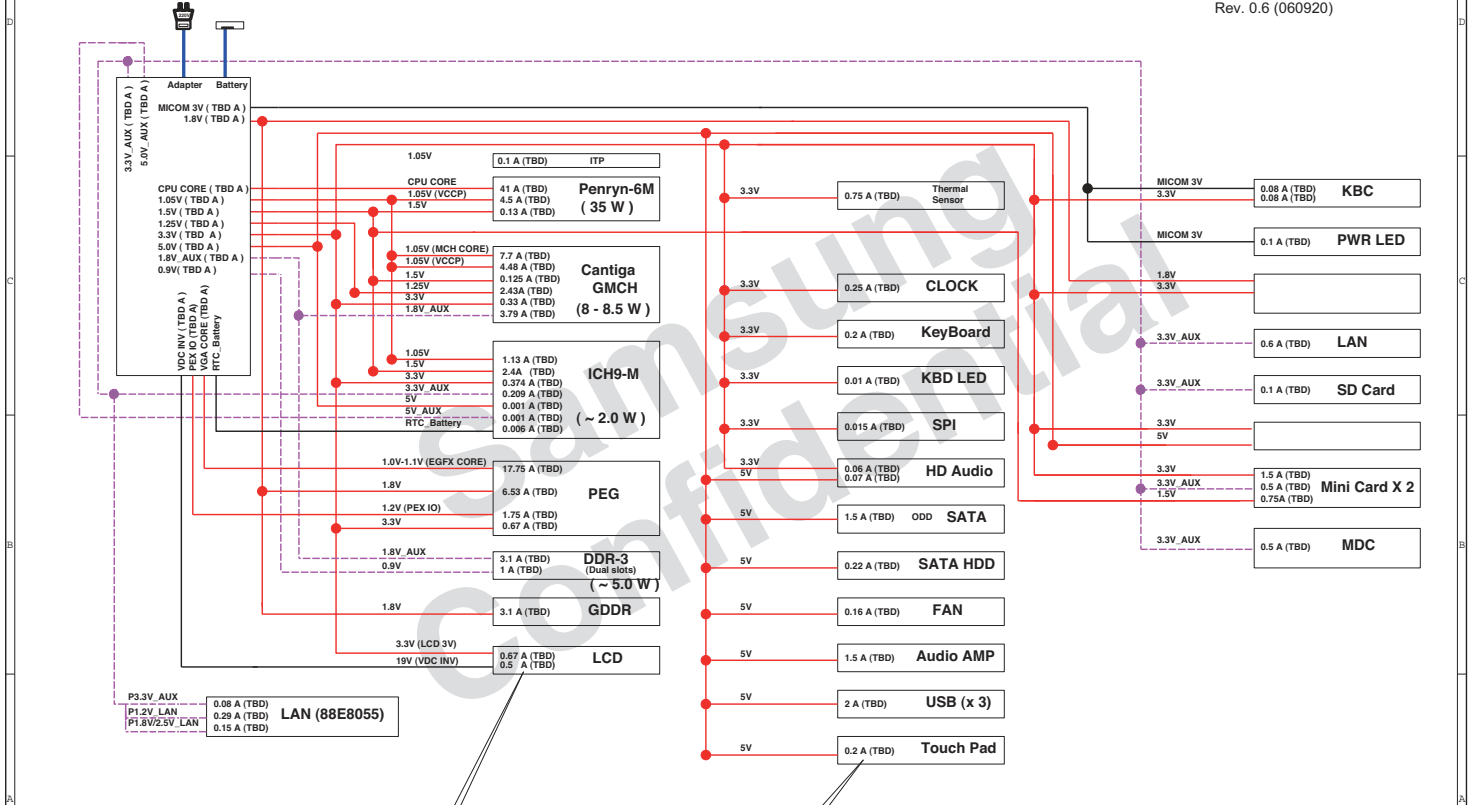
<http://hobi-elektronika.net>

DRAWN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT MAIN POWER DIAGRAM		SAMSUNG ELECTRONICS PART NO. BA41-01038A
CHECKED	HJ KIM	REV. 0/00	PR	REV.	REV 1.0	PAGE	
APPROVAL	SJ PARK	LAST DATE		REV.	REV 1.0	PAGE	4
MODEL CODE	undefined	LAST DATE		REV.	REV 1.0	OF	55
				DATE	January 28, 2009 18:53:26 PM		

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POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT MAIN		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV.	STEP	PR	POWER RAILS		
APPROVAL	SJ PARK	REV.	REV 1.0	REV 1.0	PART NO.		BA41-01039A
MODULE CODE	undefined	LAST EDIT	January 28, 2009 18:53:26 PM		PAGE	5	OF 55

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Host Boot / ME Off

(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
 M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
 M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot

(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot

(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

POWER S/W

KBC

8) CHP3_SLPS5#/4#/3#

7) KBC3_RSMRST#

17) KBC3_PWRGD

15) VRM3_CPU_PWRGD

5) KBC3_SUSPWR

9) KBC3_PWRON

13) KBC3_VRON

110ms Delay

4) POWER_SW*

8) KBC3_SUSPWR

9) KBC3_PWRON

8) KBC3_SUSPWR

9) KBC3_PWRON

9-1) KBC3_PWRON_INV#

9-1) KBC3_PWRON_INV#

2-1) P12.0V_ALW

3) P3.3V_MICOM

2) VDC

3) P3.3V_MICOM

2-1) P12.0V_ALW

3) P3.3V_MICOM

6) P5.0V_AUX

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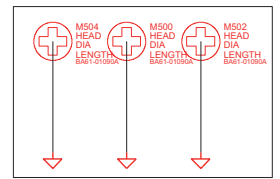
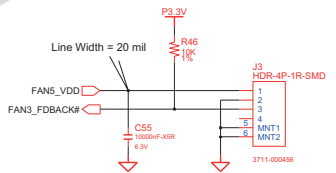
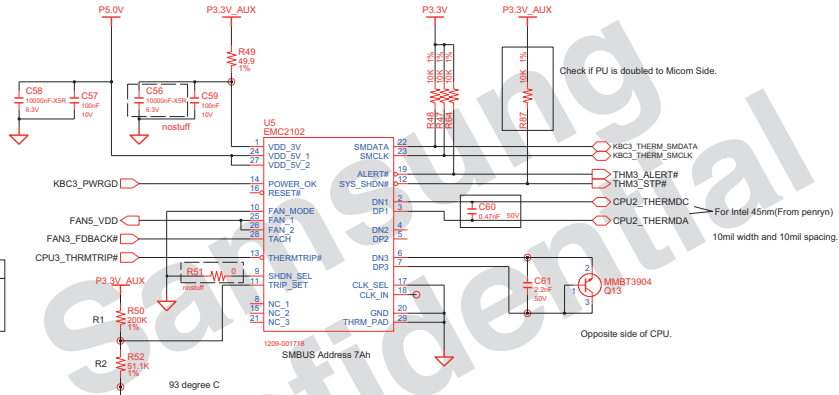
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THERMAL SENSOR & FAN CONTROL

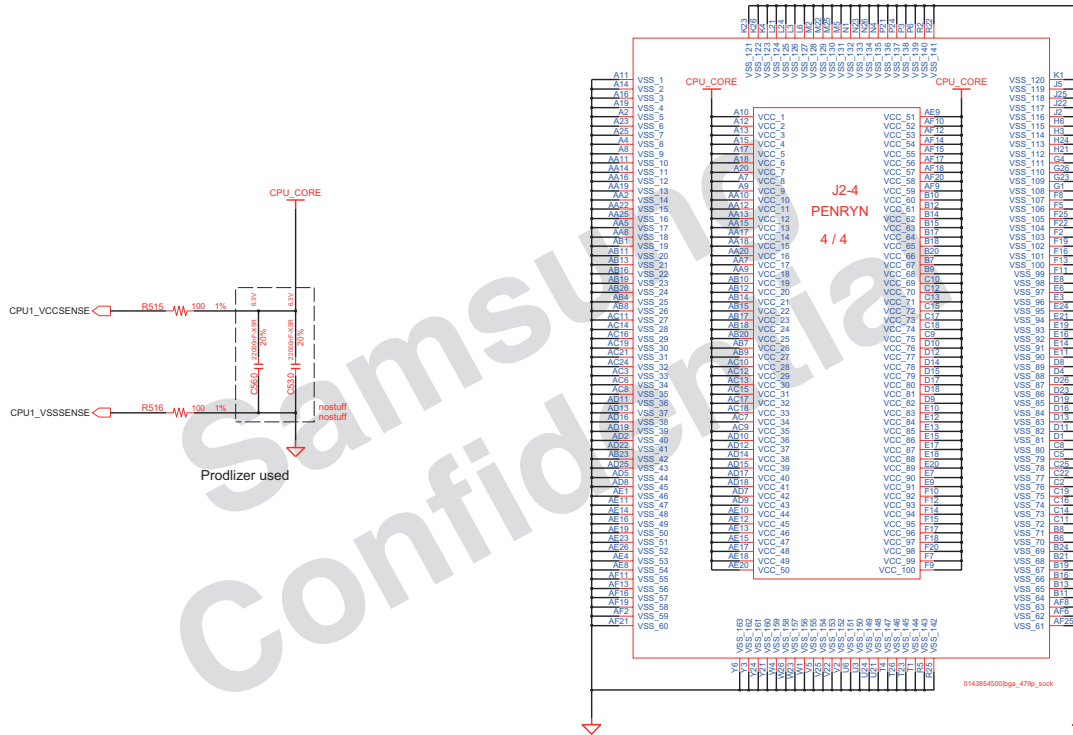


To support heatsink

DESIGN	TW KM	DATE	9/23/2008	TITLE	BONN-INT THERMAL SENSOR		SAMSUNG ELECTRONICS
CHECK	HJ KM	REV/STEP	PR	THERMAL SENSOR EMC2102		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0	THERMAL SENSOR EMC2102		BA41-01039A	
MODEL CODE		LAST EDIT		DESIGN	January 28, 2009 18:53:26 PM	PAGE	8 OF 55

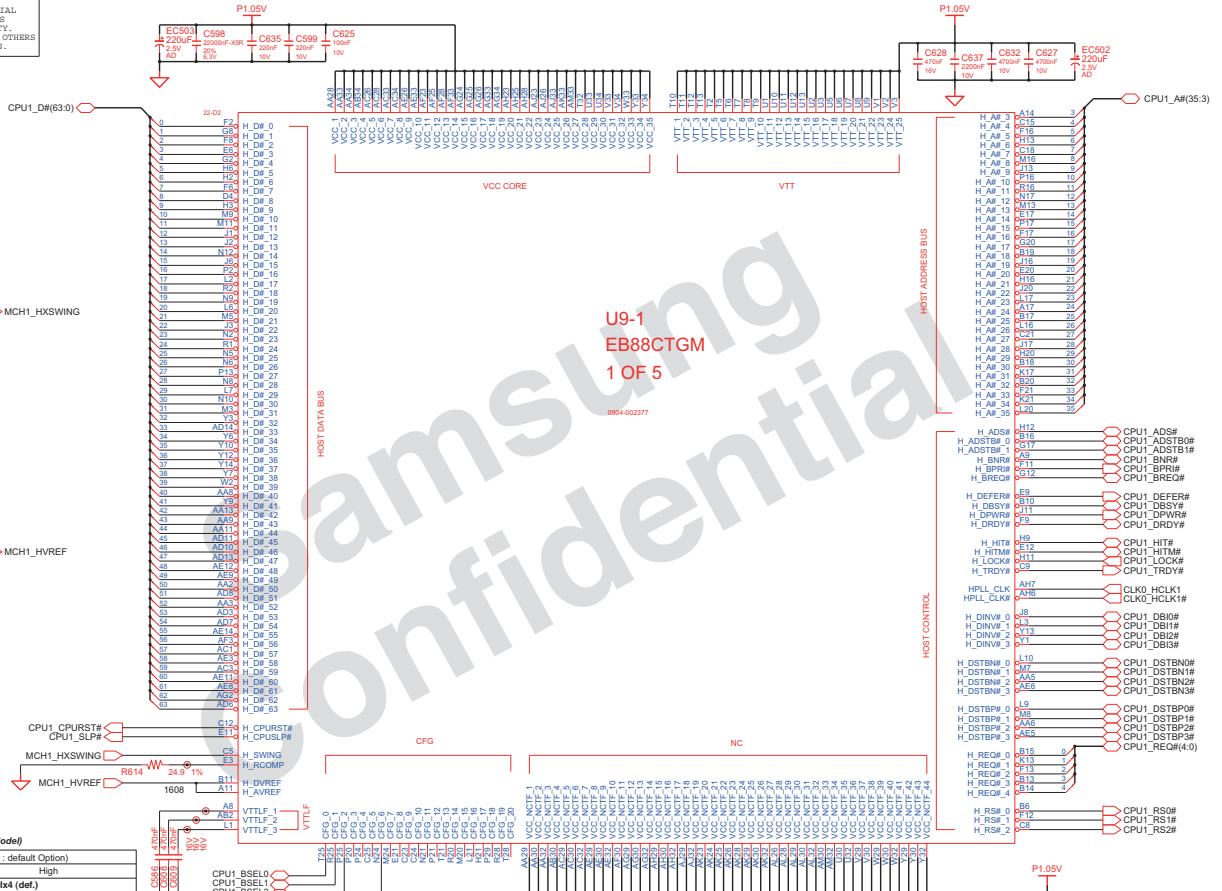
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DRAW	TW KM	DATE	9/23/2008	TITLE	BONN-INT		SAMSUNG ELECTRONICS
CHECK	HJ KM	REV. STEP	PR	CPU		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0	PENRYN (3/3)		BA11-01039A	
MODEL CODE	undefined	LAST DESI	January 28, 2009 18:53:26 PM	PAGE	11	OF	55

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U9-1
 EB88CTGM
 1 OF 5

0954-003277

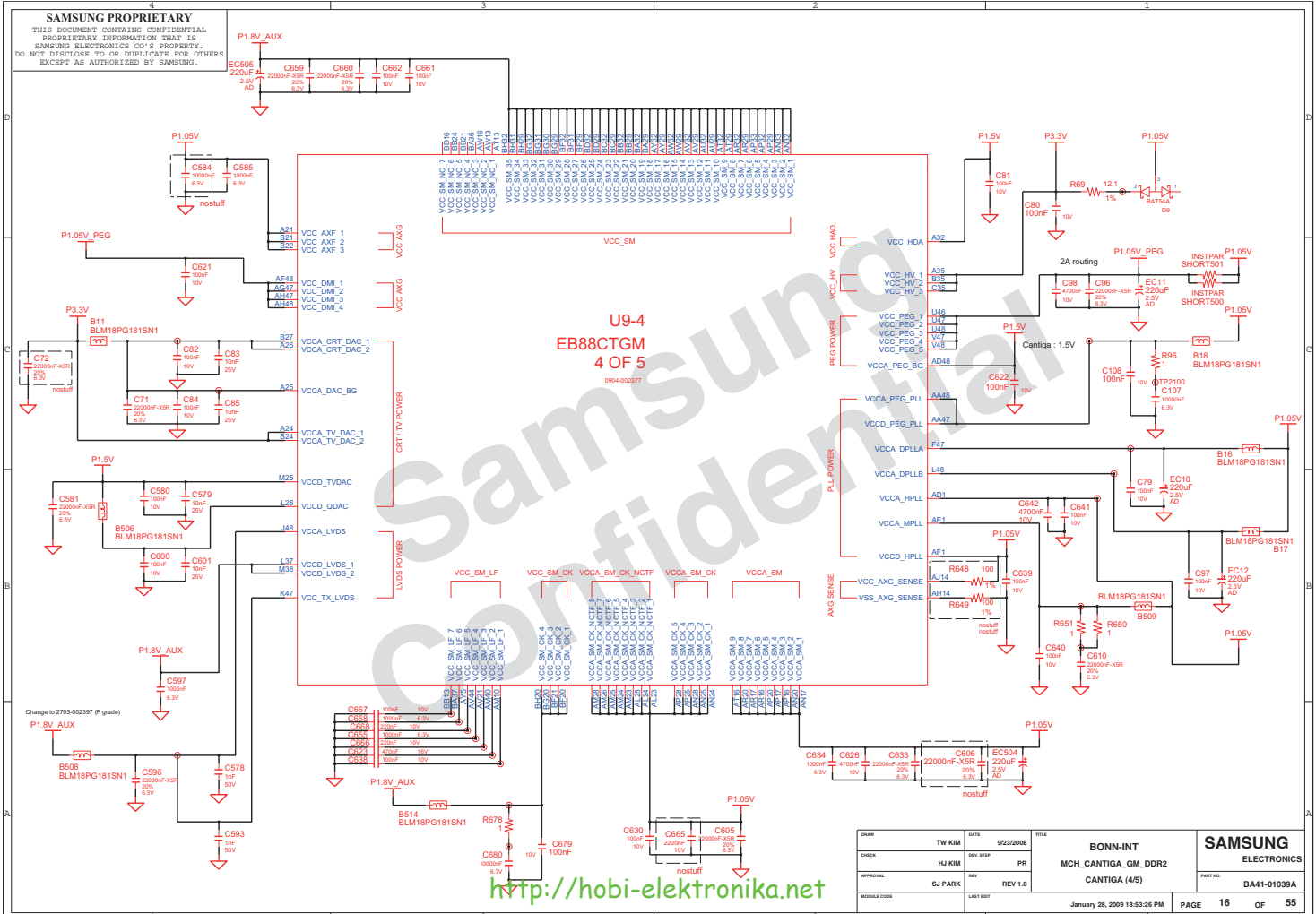
"POCAFE8-12 Only (Remove in MP Mode)"

CFG#	Current Setting (def.: default Option)	Low	High
CFG(5)	DmX2		DmX4 (def.)
CFG(6)	ITPM Host Interface Enable		ITPM Host Interface Disable (def.)
CFG(7)	ME Crypto non confidentiality		ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)		Normal
CFG(10)	PCIe Loop Back Enable		PCIe Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled		Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)		DMI Lane Reversal
CFG(20)	SDVO or PCIe X1 Only(def.)		SDVO and PCIe X1 Simultaneously



DRAWN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT
CHECK	HJ KIM	REV	STEP	PR	MCH_CANTIGA_GM_DDR2
APPROVAL	SJ PARK	REV	VER	1.0	CANTIGA (1/5)
MODEL CODE	undefined	LAST EDIT			January 28, 2009 18:53:26 PM

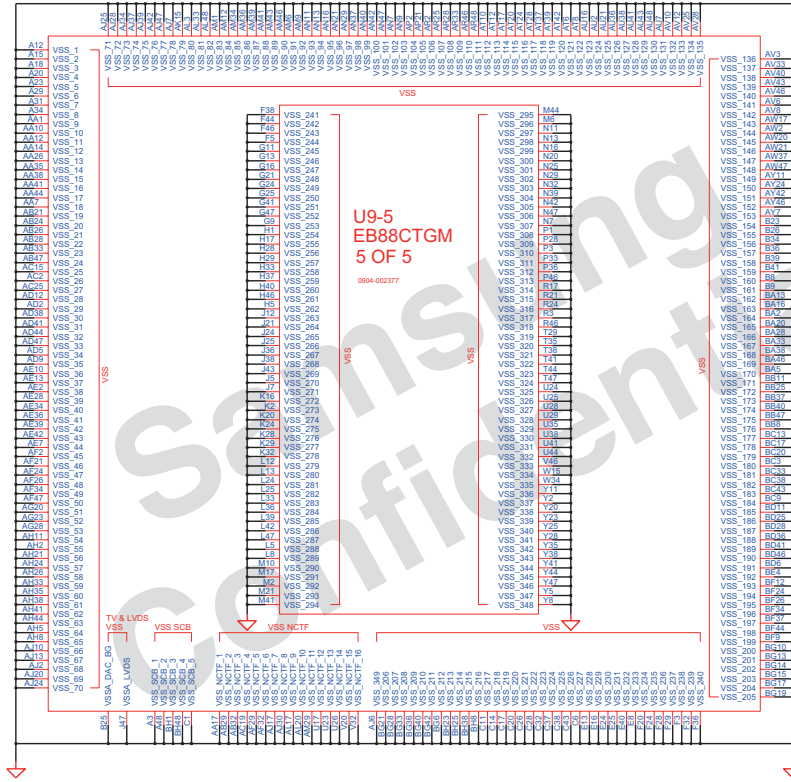
SAMSUNG	
ELECTRONICS	
PART NO.	BA41-01039A
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DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT	SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV/STEP	PR	MCH, CANTIGA, GM, DDR2	CANTIGA (4/5)	
APPROVAL	SJ PARK	REV	1.0			BA11-01039A
MODEL CODE		LAST DATE		January 28, 2009 18:53:26 PM	PAGE	16 OF 55

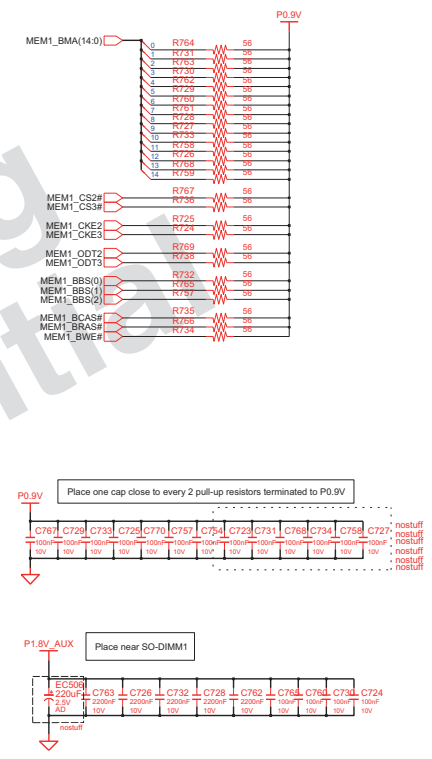
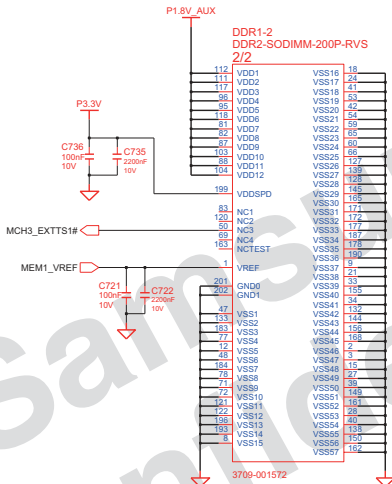
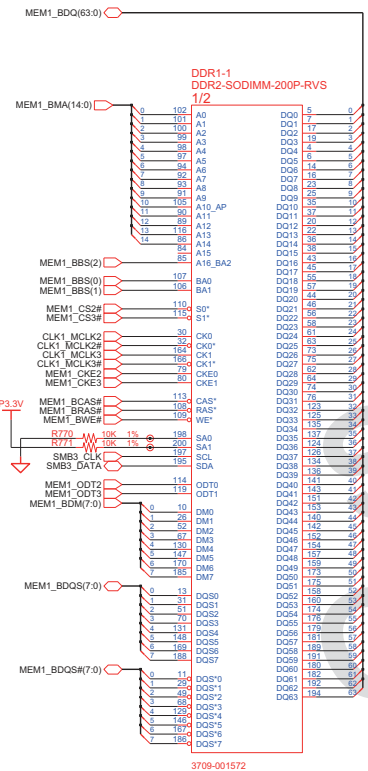
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DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-IN T	SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV	STEP	PR	MCH_CANTIGA_GM_DDR2	
APPROVAL	SJ PARK	REV	REV 1.0		CANTIGA (5/5)	PART NO.
MODEL CODE		LAST DESI				BA11-01039A
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DDR SO-DIMM #1

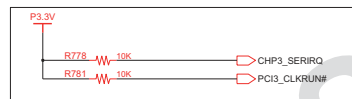
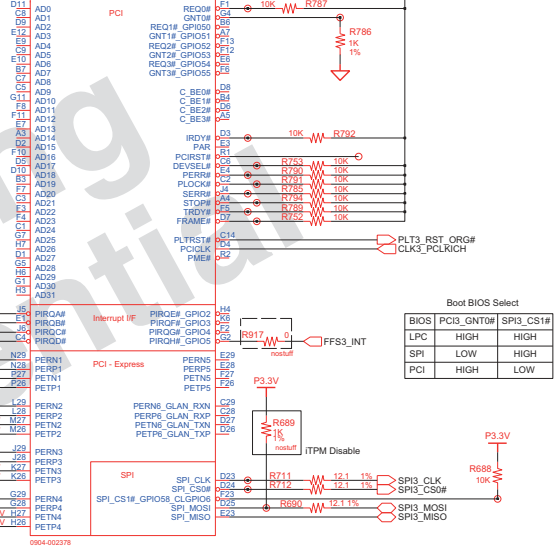


DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT SODIMM_DDR2		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR	SODIMM_DDR2 #2		PART NO.	
APPROVAL	SJ PARK	REV	VER 1.0	SODIMM_DDR2 #2		BA11-01039A	
MODEL CODE	LAST EDIT	January 28, 2009 18:53:26 PM		PAGE	19	OF	55

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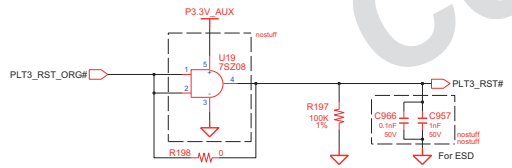
**U18-2
NH828011BM
2/5**



Boot BIOS Select

	BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH	HIGH
SPI	LOW	HIGH	HIGH
PCI	HIGH	LOW	LOW

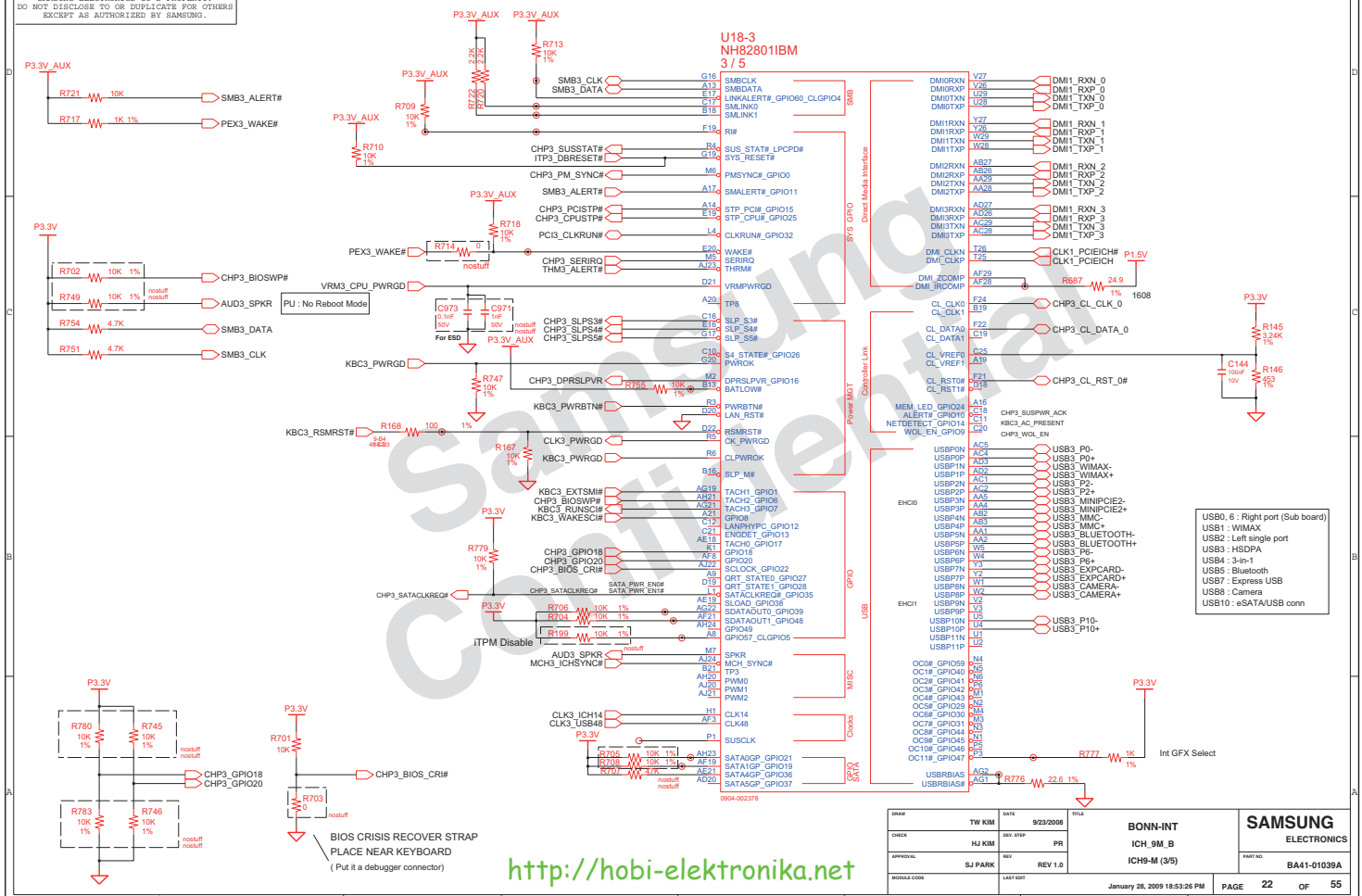
AC caps : PCIe need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs



DRAWN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT ICH_9M_B		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR	ICH9-M (2/5)		PART NO.	
APPROVAL	SJ PARK	REV	V1.0	ICH9-M (2/5)		BA11-01039A	
MODEL CODE	undefined	LAST DESI		January 28, 2009 18:53:26 PM	PAGE	21	OF 55

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USB0_6 : Right port (Sub board)
 USB1 : WIMAX
 USB2 : Left single port
 USB3 : HSDPA
 USB4 : 3-in-1
 USB5 : Bluetooth
 USB7 : Express USB
 USB8 : Camera
 USB10 : eSATA/USB conn

BIOS CRISIS RECOVER STRAP
 PLACE NEAR KEYBOARD
 (Put it a debugger connector)

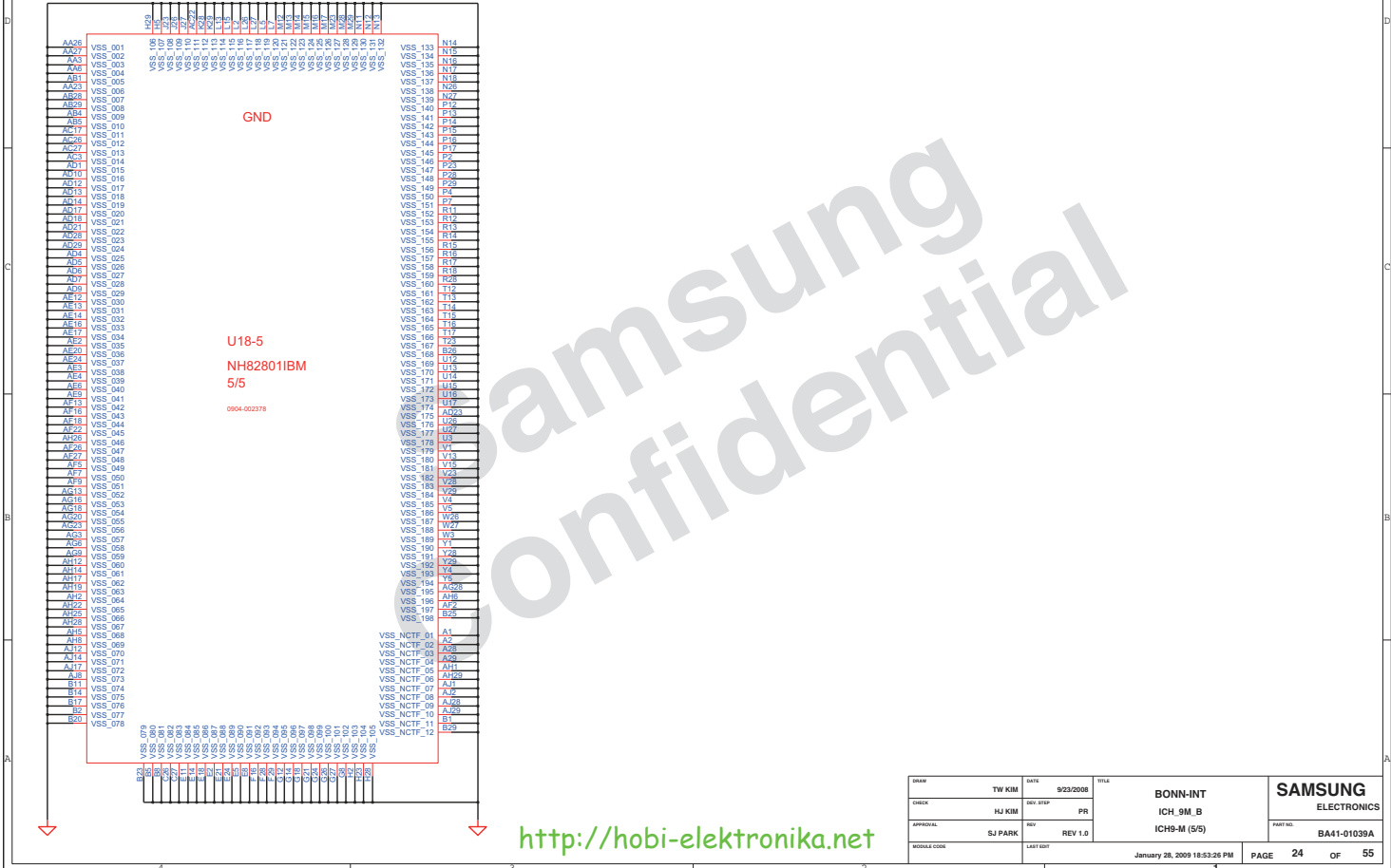
<http://hobi-elektronika.net>

DATE	9/23/2008	TITLE	BONN-INT	SAMSUNG ELECTRONICS
DESIGNER	TW KIM	REV. REV	ICH_9M_B	
APPROVAL	HJ KIM	REV. REV	PR	PART NO.
DESIGNER	SJ PARK	REV. REV	1.0	
MODEL CODE		LAST MOD		PAGE
				OF
				55

January 28, 2009 18:53:26 PM

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GND

U18-5
 NH82801BM
 5/5

0004-002378

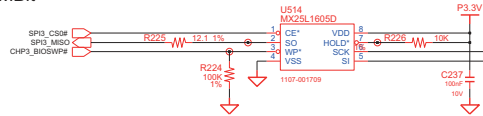
<http://hobi-elektronika.net>

DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT ICH_9M_B	SAMSUNG ELECTRONICS PART NO. BA41-01039A
CHECK	HJ KIM	REV./STEP	PR	REV	ICH9-M (5/5)	
APPROVAL	SJ PARK	REV	REV 1.0	PAGE 24 OF 55		
MODEL CODE	LAST EDIT		January 28, 2009 18:53:26 PM		PAGE 24 OF 55	

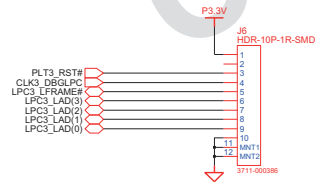
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SPI_BIOS_ROM

16MBit



80H DECODER CONNECTOR



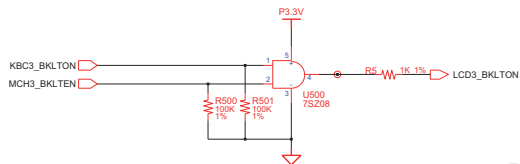
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	SET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM F/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	SET REAL TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT IO VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
14	WITH INITIAL POST VALUE	8A	INIT. EXTENDED BIOS DATA AREA
16	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	9A	SHADOW OPTION ROMS
16	256 TIMER INIT.	9C	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT.	9E	ENABLE HW INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AC	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
28	COMPUTE THE CPU SPEED	AE	CHECK FOR ERRORS
34	TEST CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	BA	ACPI INIT
42	INIT. INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I2O SUPPORT IF INSTALLED	D0	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
48	INIT. PCI BIOS AND PCI	D6	SHUTDOWN ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	INIT. HDD CONTROLLER
52	TEST KEYBOARD	DE	ENABLE NMI
54	SET KEYBOARD IF ENABLED	DE	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 2
5A	DISPLAY ADDRESS LINE	94	DISABLE ADDRESS LINE
5C	TEST RAM BETWEEN 512K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		

DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP		PR	SPI_BIOS_ROM		
APPROVAL	SJ PARK	REV	REV 1.0		SPI_BIOS_ROM		PART NO. BA41-01039A
MODEL CODE		LAST EDIT			January 28, 2009 18:53:26 PM		PAGE 25 OF 55

LVDS

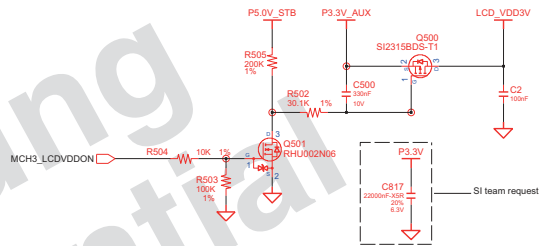
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Backlight On

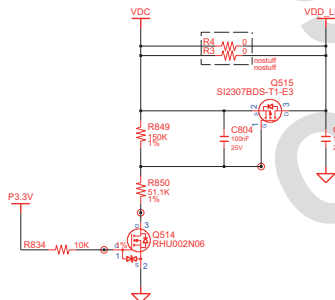


LCD Power

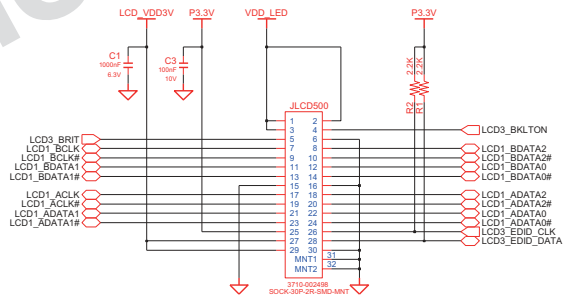
EBL Purpose



LED Power



2Ch. LCD Connector



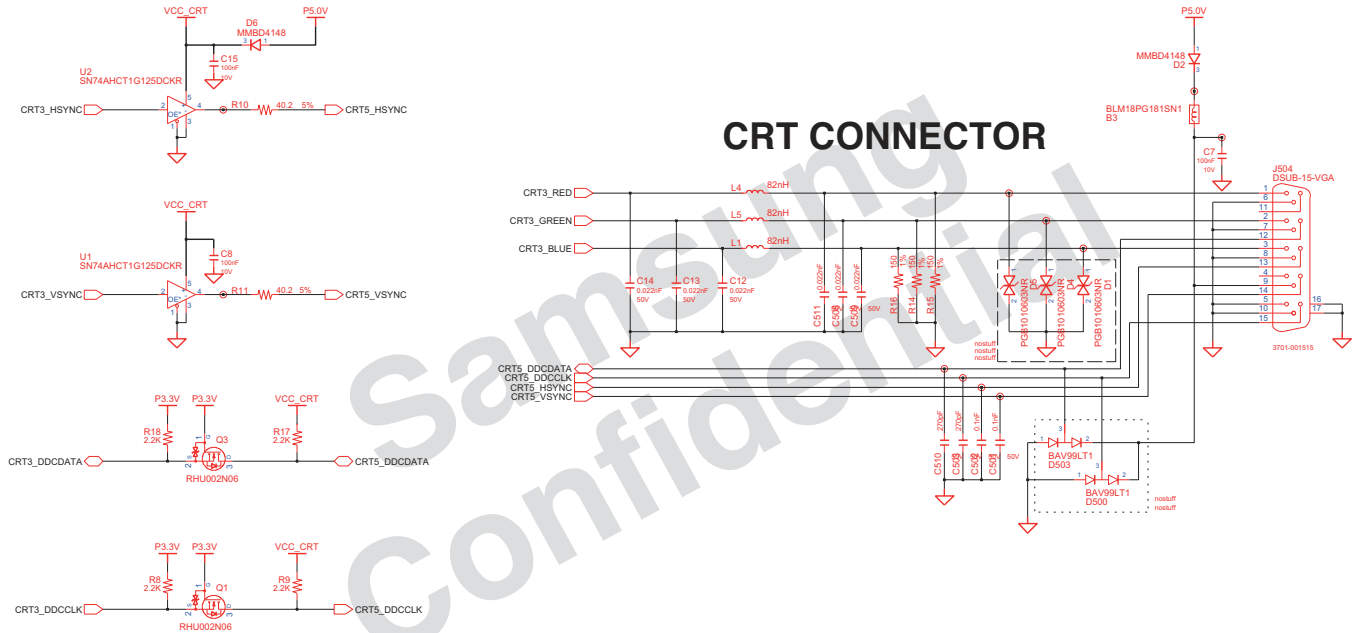
<http://hobi-elektronika.net>

DESIGN	TW KM	DATE	9/23/2008	TITLE	BONN-INT		SAMSUNG ELECTRONICS
CHECK	HJ KM	REV/STEP	PR	GRAPHICS_IF		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0	LVDS		BA1-01039A	
MODEL CODE	LAST MOD	January 28, 2009 18:53:26 PM		PAGE	26	OF	55

CRT

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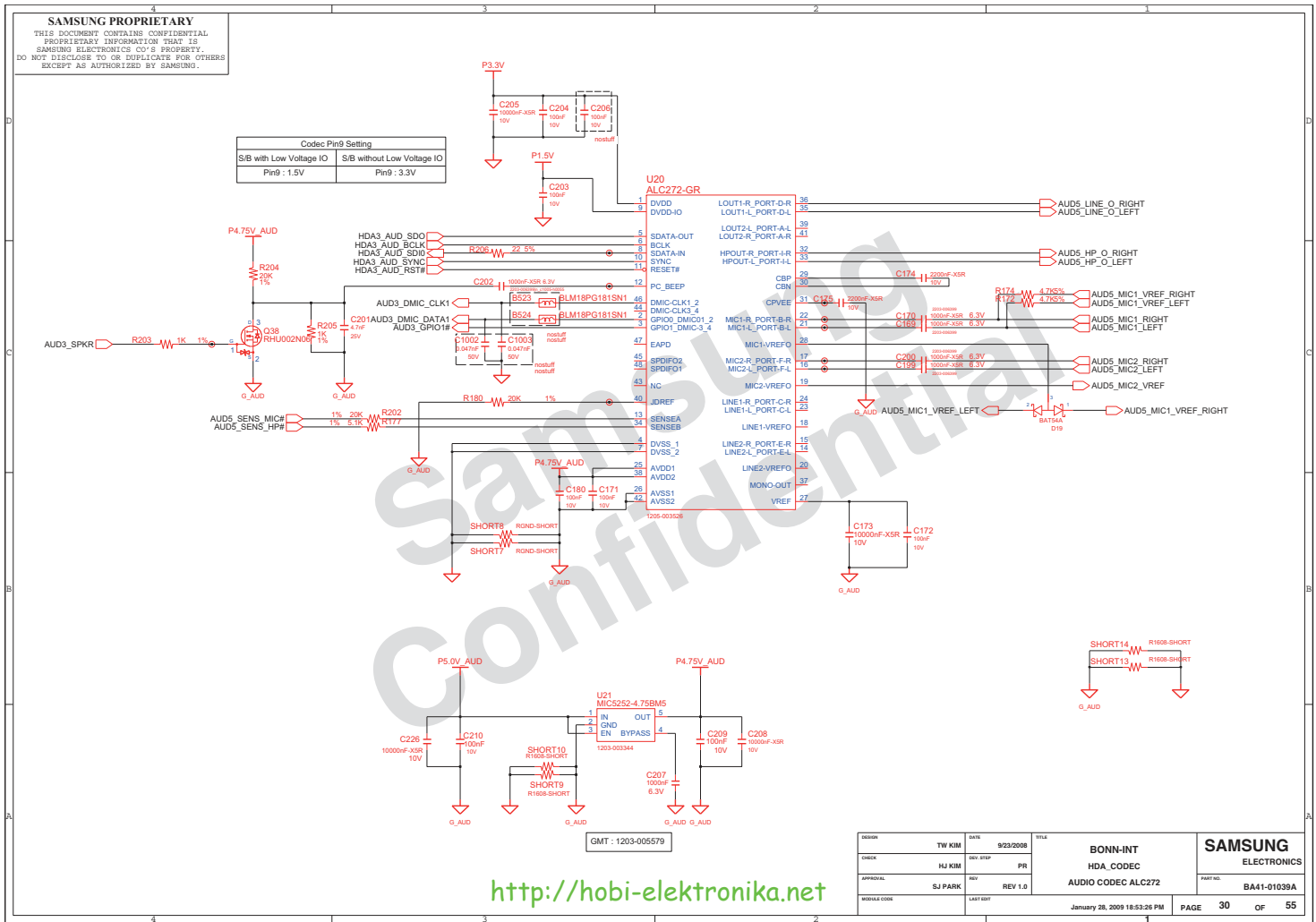
Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DESIGN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT GRAPHICS_IF		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR	CRT		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0			BA41-01039A	
MODULE CODE	LAST EDIT		January 28, 2009 18:53:26 PM		PAGE	27	OF 55

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Codec Pin# Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



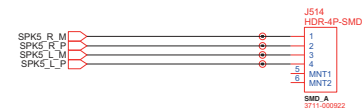
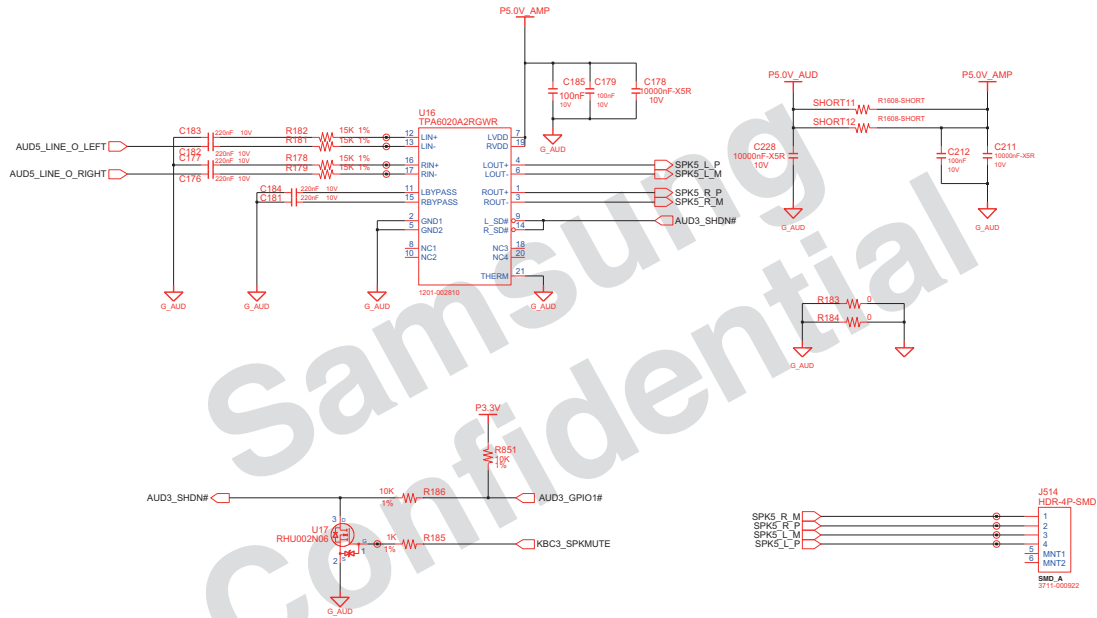
GMT : 1203-005579

<http://hobi-elektronika.net>

DESIGN	TW KM	DATE	TITLE	SAMSUNG ELECTRONICS	
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APPROVAL	SJ PARK	REV	REV 1.0	BA41-01038A	
MODEL CODE	LAST EDIT	January 28, 2009 18:53:26 PM		PAGE	30 OF 55

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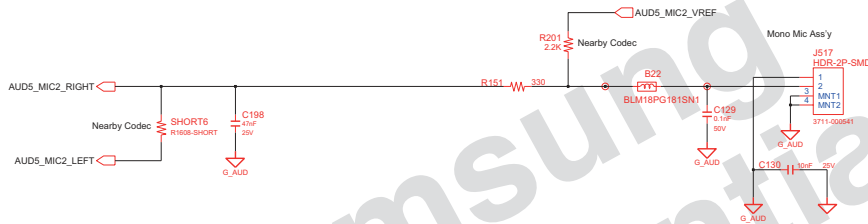
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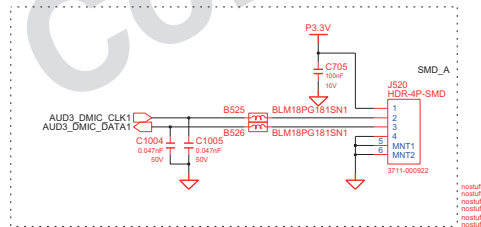
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CHECK	HJ KM	REV. STEP	PR	SPK AMP TPA6017	PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0		BA41-01039A	
MODULE CODE		LAST EDIT		January 28, 2009 18:53:26 PM	PAGE	31 OF 55

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Digital MIC CONNECTOR



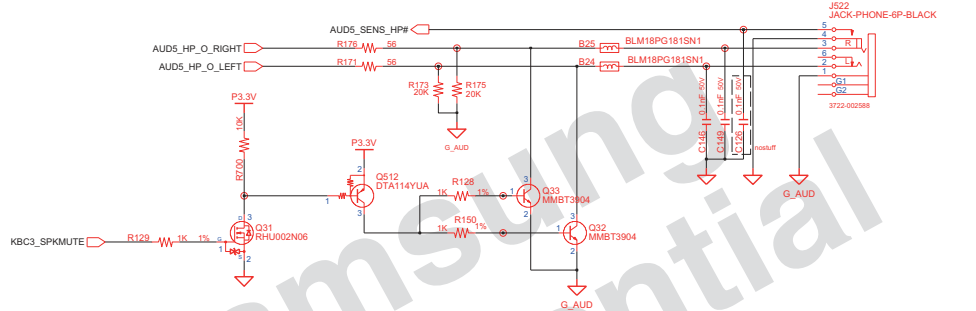
<http://hobi-elektronika.net>

DESIGN	TW KM	DATE	9/23/2008	TITLE	BONN-INT HDA_CODEC	SAMSUNG ELECTRONICS
CHECK	HJ KM	REV. STEP	PR			
APPROVAL	SJ PARK	REV.	REV 1.0		MIC AMP LMV358	PART NO.
MODEL CODE		LAST EDIT		January 28, 2009 18:53:26 PM		BA41-01039A
					PAGE	32 OF 55

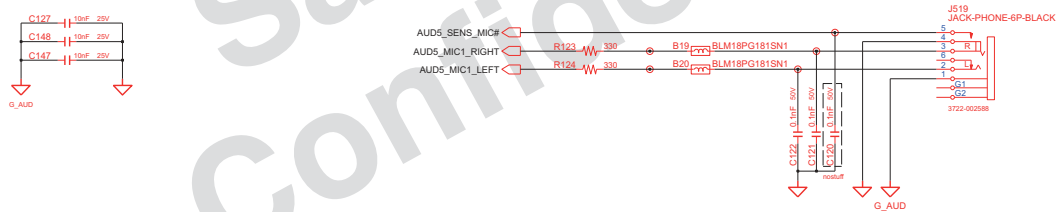
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HEADPHONE(BLACK)



MIC JACK(BLACK)

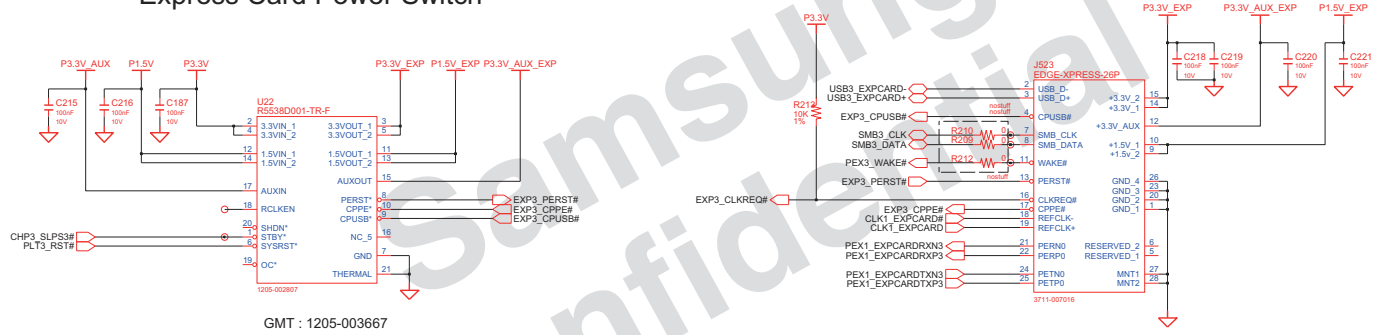


DESIGN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT HDA_CODEC		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR	H/P JACK AND MIC JACK		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0	January 28, 2009 18:53:26 PM		BA41-01039A	PAGE 33 OF 55
MODULE CODE	LAST EDIT						

Express Card

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Express Card Power Switch



TYPE - II

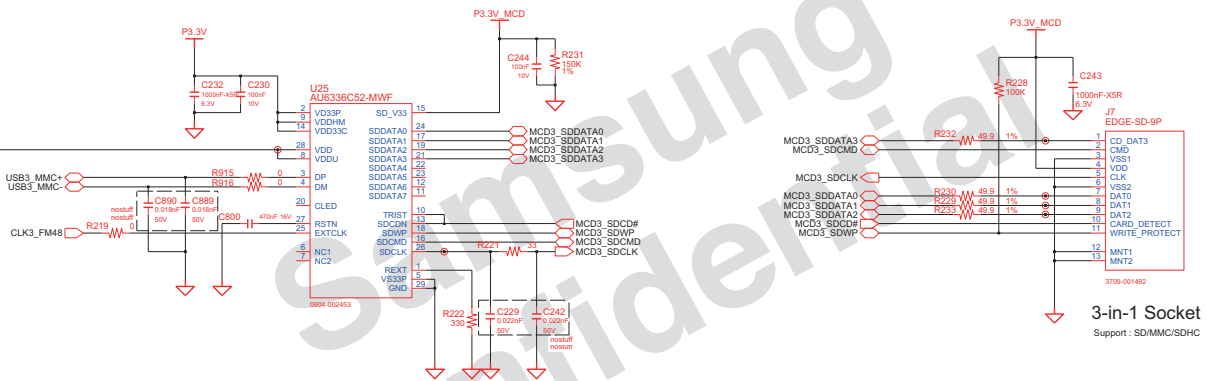


DESIGN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT EXPRESS CARD		SAMSUNG ELECTRONICS PART NO. BA41-01039A
CHECK	HJ KIM	REV. STEP	PR	EXPRESS CARD			
APPROVAL	SJ PARK	REV	REV 1.0			PAGE	35 OF 55
MODEL CODE		LAST EDIT	January 28, 2009 18:53:26 PM				

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3 IN 1 CARD (AU6336)



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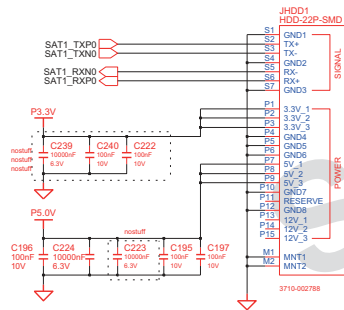
DESIGN	TW KM	DATE	9/23/2008	TITLE	BONN-INT MULTICARD		SAMSUNG ELECTRONICS
CHECK	HJ KM	REV./STEP	PR	2 IN 1 CARD		PART NO. BA41-01039A	
APPROVAL	SJ PARK	REV.	REV 1.0	January 28, 2009 18:53:26 PM		PAGE	36 OF 55
MODEL CODE	LAST EDIT						

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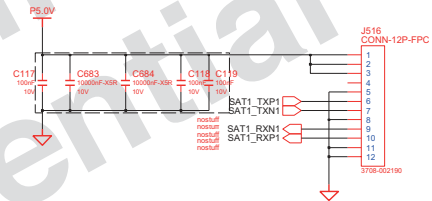
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SATA I/F CONN

SATA HDD CONN



MAIN TO SUB SATA ODD CONN



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DESIGN	TW KM	DATE	9/23/2008	TITLE	BONN-INT SATA DEVICES		SAMSUNG ELECTRONICS
CHECK	HJ KM	REV. SHEET	PR	HDD & ODD SUB CONNECTOR		PART NO.	
APPROVAL	SJ PARK	REV.	REV 1.0			BA41-01039A	
MODEL CODE	LAST EDIT	January 28, 2009 18:53:26 PM		PAGE	38	OF	55

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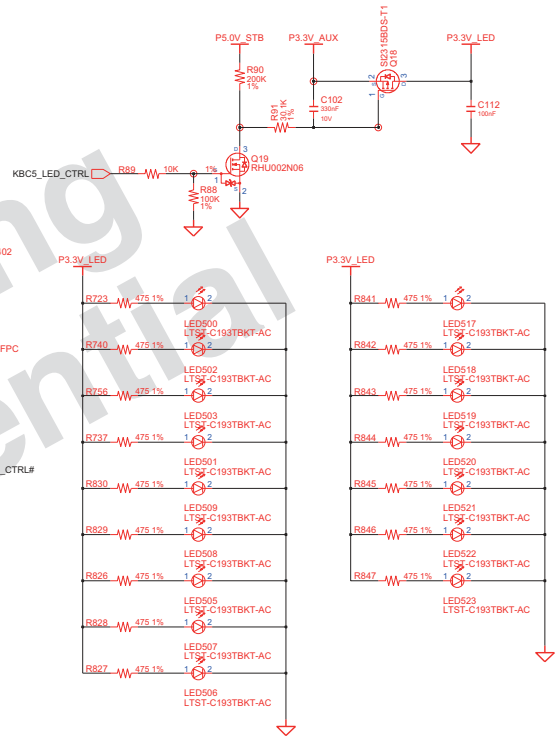
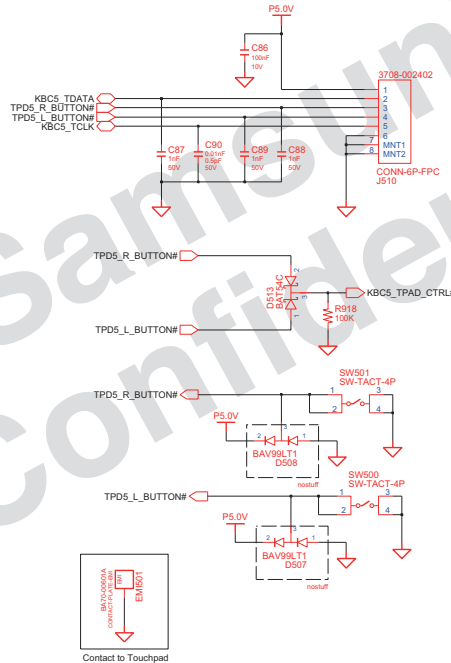
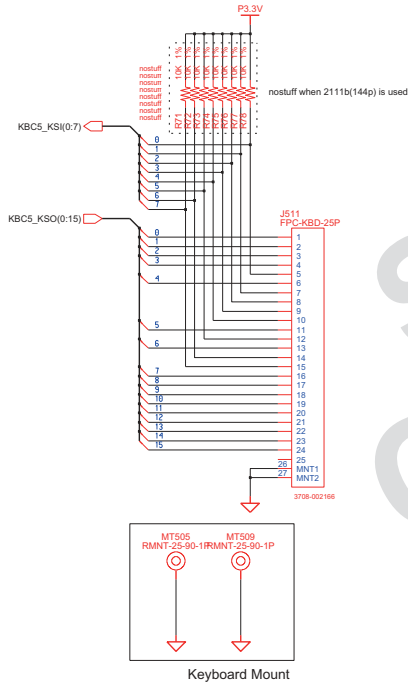
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Micom Glue Logic

TOUCHPAD LED

KEYBOARD

TOUCHPAD

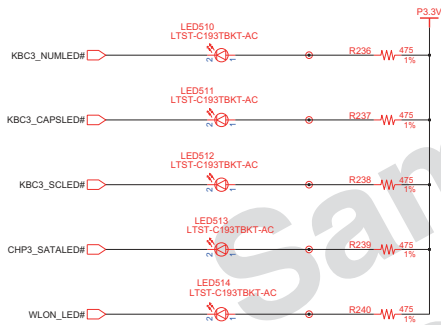


<http://hobi-elektronika.net>

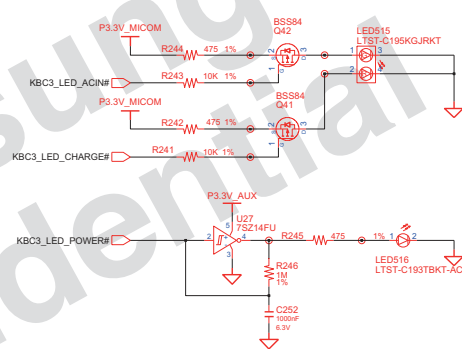
DESIGN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT MICOM GLUE LOGIC		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV/STEP	PR	KEYBOARD & TOUCHPAD		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0				BA1-01039A
MODEL CODE		LAST EDIT		January 28, 2009 18:53:26 PM		PAGE	40 OF 55

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FUNCTION KEY LED



ADAPTERIN/CHARGING LED

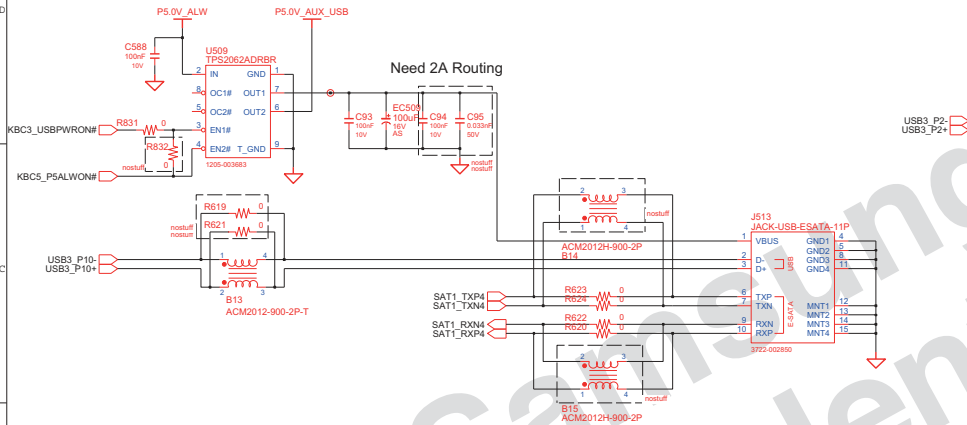


DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT LED_SWITCH		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR	LED_SWITCH		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0			BA41-01039A	
MODULE CODE		LAST EDIT	January 28, 2009 18:53:26 PM		PAGE	41	OF 55

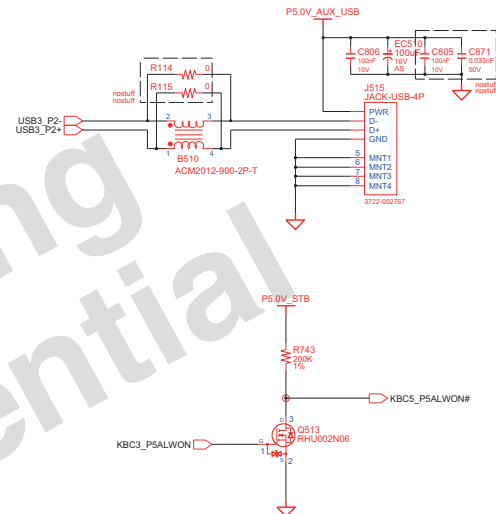
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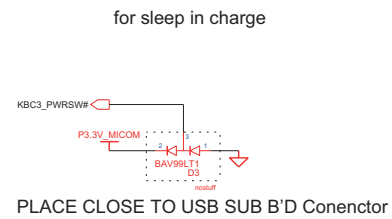
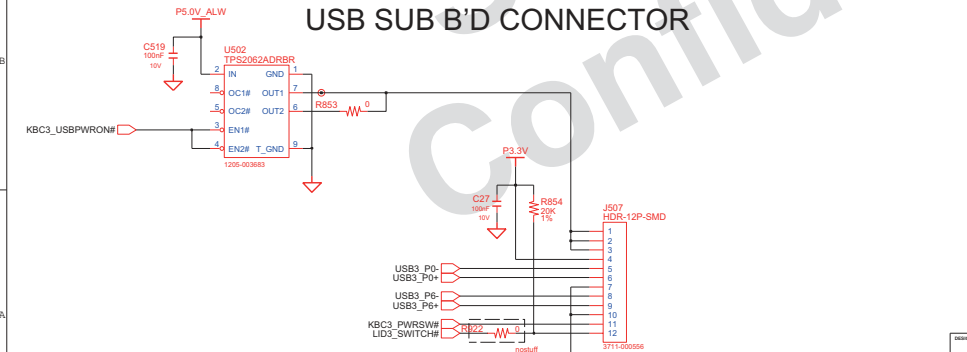
USB + eSATA CONNECTOR



USB Single connector



USB SUB B'D CONNECTOR



DESIGN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT USB_CONN		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV./STEP	PR	USB & eSATA		PART NO.	
APPROVAL	SJ PARK	REV.	REV 1.0			BA1-01039A	
MODEL CODE	LAST DATE	January 28, 2009 18:53:26 PM		PAGE	42	OF	55

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USB I/F Devices

Bluetooth Interface

CAMERA



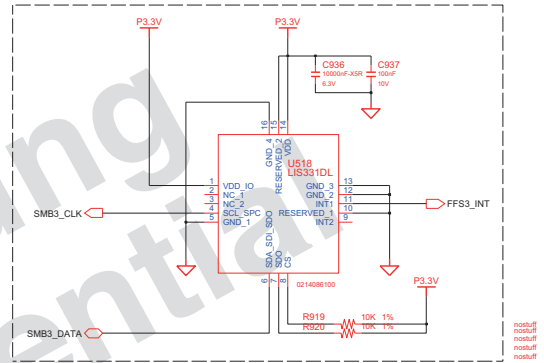
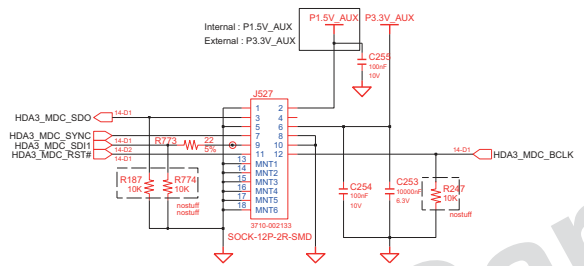
DESIGN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT USB_DEVICES BLUETOOTH & CAMERA	SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR	PART NO.		
APPROVAL	SJ PARK	REV	REV 1.0	January 28, 2009 18:53:26 PM		PAGE 43 OF 55
MODULE CODE	LAST EDIT					

SAMSUNG PROPRIETARY

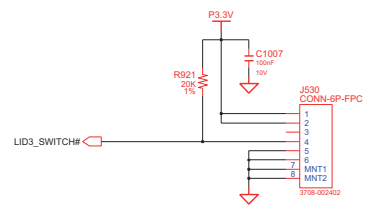
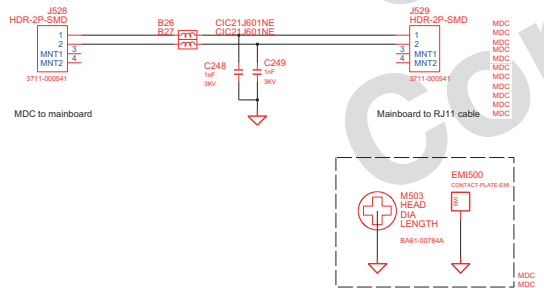
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Freelfall sensor

MDC connector



LID SWITCH

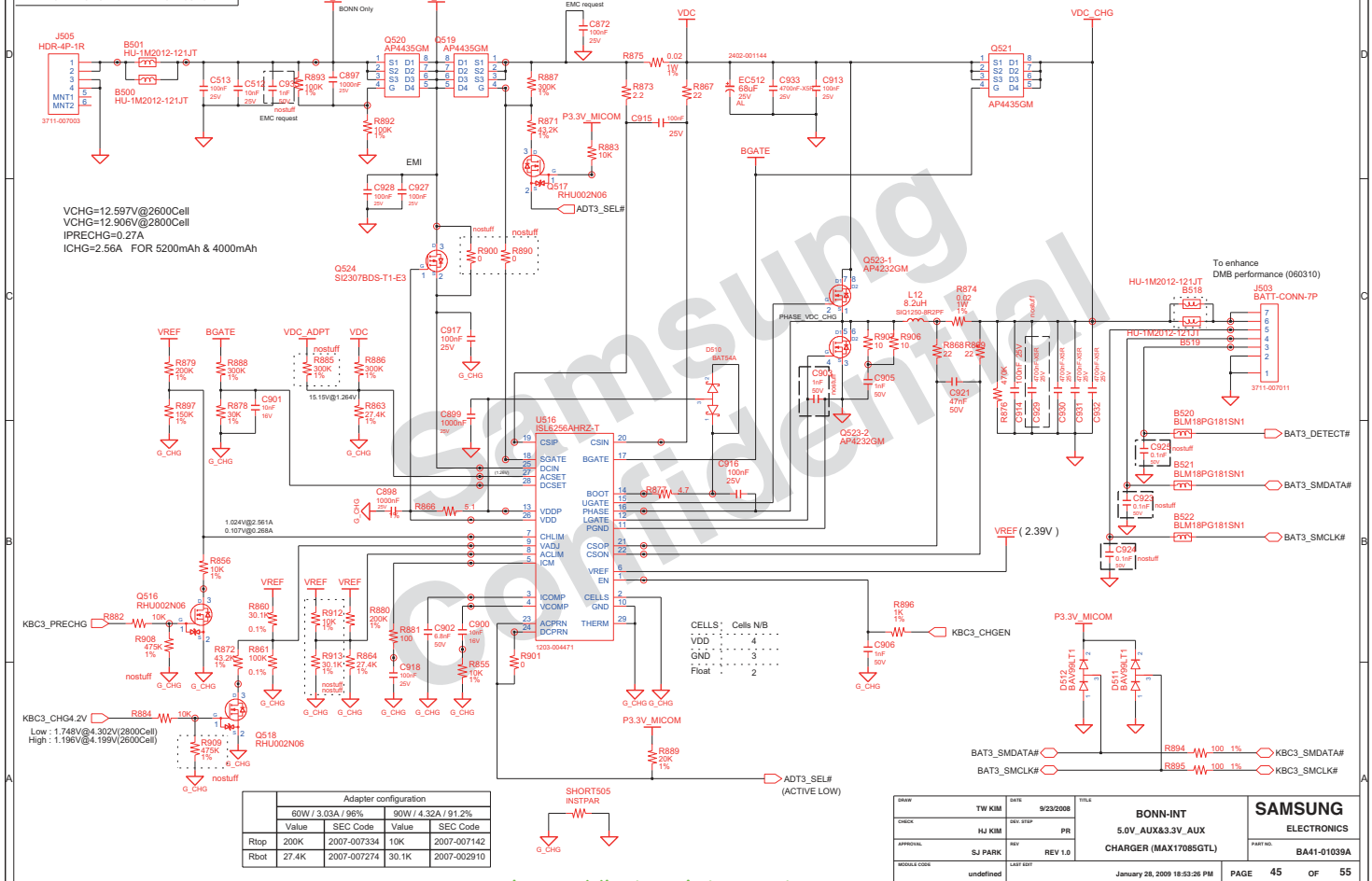


<http://hobi-elektronika.net>

DRAW	TW KM	DATE	9/23/2008	TITLE	BONN-INT MDC CONNECTOR		SAMSUNG ELECTRONICS
CHECK	HJ KM	REV/STEP	PR	MDC CONNECTOR		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0	MDC CONNECTOR		BA41-01039A	
MODEL CODE	undefined	LAST EDIT	January 28, 2009 18:53:26 PM	PAGE	44	OF	55

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CHARGER & POWER MANAGEMENT



VCHG=12.597V@2600Cell
 VCHG=12.906V@2800Cell
 IPRECHG=0.27A
 ICHG=2.56A FOR 5200mAh & 4000mAh

To enhance
 DNB performance (060310)

CELLS: Cells N/B
 VDD 4
 GND 3
 Float 2

Adapter configuration			
60W / 3.03A / 96%	90W / 4.32A / 91.2%	Value	SEC Code
Risp	200K	2007-00733A	10K 2007-007142
Rbot	27.4K	2007-00727A	30.1K 2007-002910

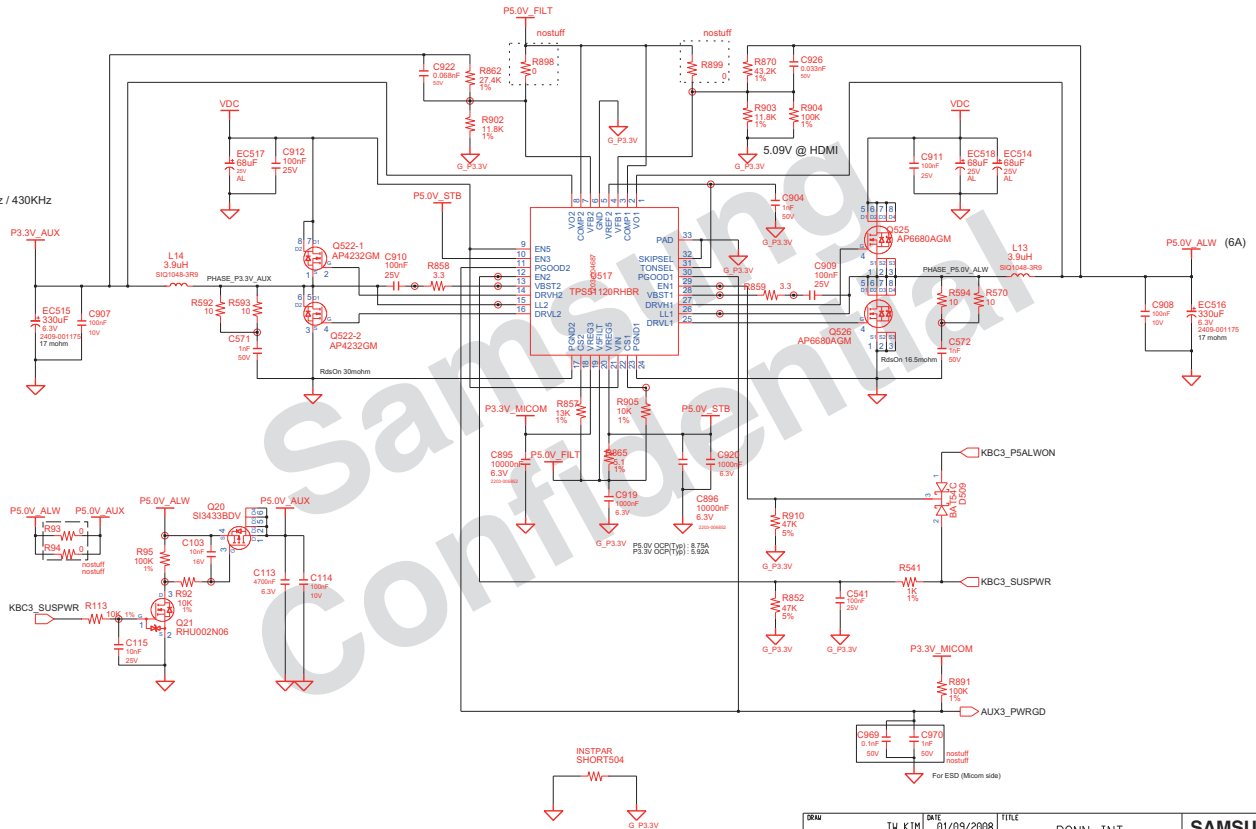
DRAWN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT 5.0V_AUX&3.3V_AUX CHARGER (MAX17085GTL)		SAMSUNG ELECTRONICS PART NO. BA41-01039A
CHECK	HJ KIM	REV	STEP	PR			
APPROVAL	SJ PARK	REV	VER	1.0			
MODEL CODE	undefined	LAST ESD			January 28, 2009 18:53:26 PM PAGE 45 OF 55		

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P3.3V_AUX & P5.0V_AUX

TONSEL VREF2
 5V / 3.3V : 280KHz / 430KHz
 (4A)

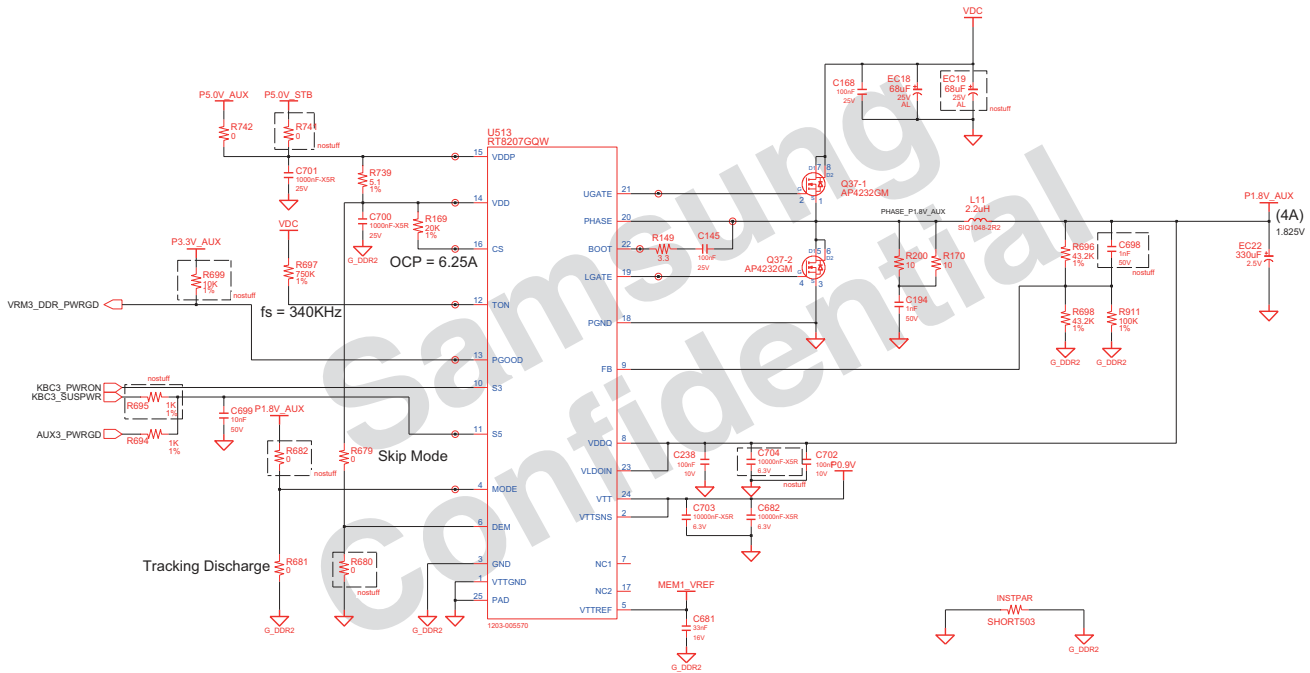


<http://hobi-elektronika.net>

DATE	TW KIM	DATE	01/09/2008	TITLE	BONN-INT	SAMSUNG ELECTRONICS
DESIGN	HJ KIM	REV. STEP	PR		PMR_MW_3V_5V	
APPROVAL	SJ PARK	REV	REV 1.0		P3.3V_AUX / P5.0V_AUX	PART NO.
MODULE CODE		LAST EDIT	undef ined			BA11-01039A
				January 28, 2009 18:53:26 PM	PAGE	46 OF 55

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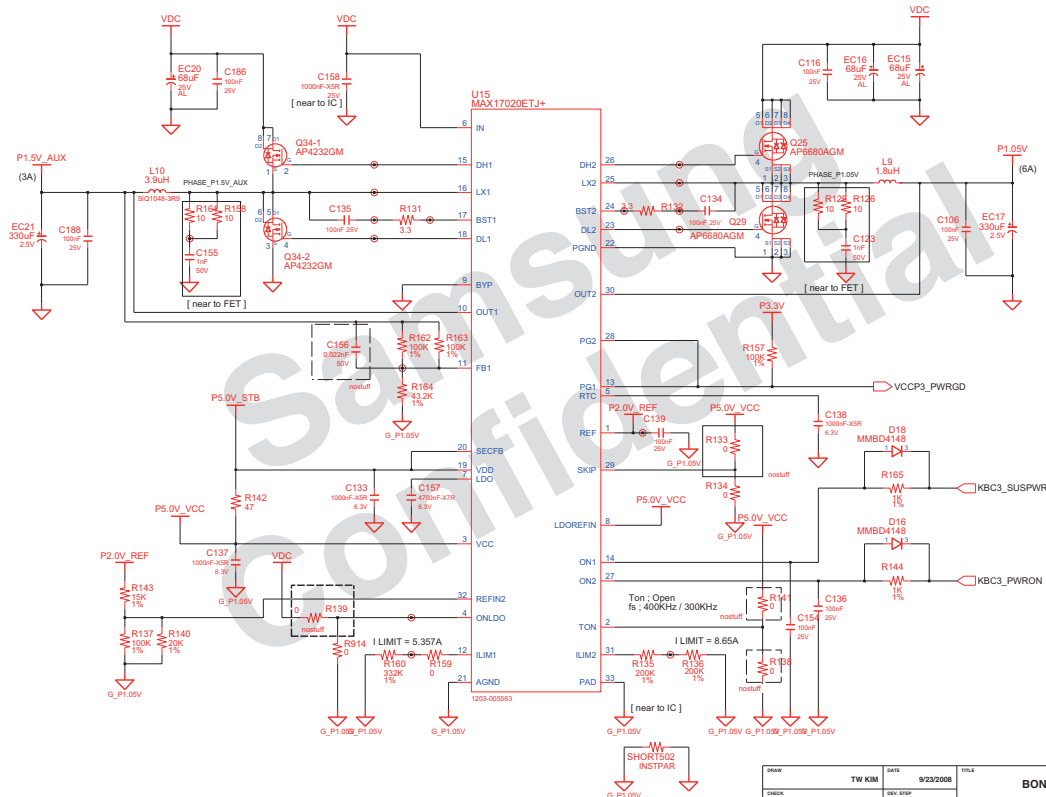
DDR2 Power



DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT PWR_MEMORY		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV	STEP	PR	DDR2 POWER		
APPROVAL	SJ PARK	REV	REV	REV	REV	REV	PART NO. BA41-01039A
MODULE CODE	undefined	LAST DESG					PAGE 47 OF 55

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CHIPSET POWER(P1.5V_AUX & P1.05V)

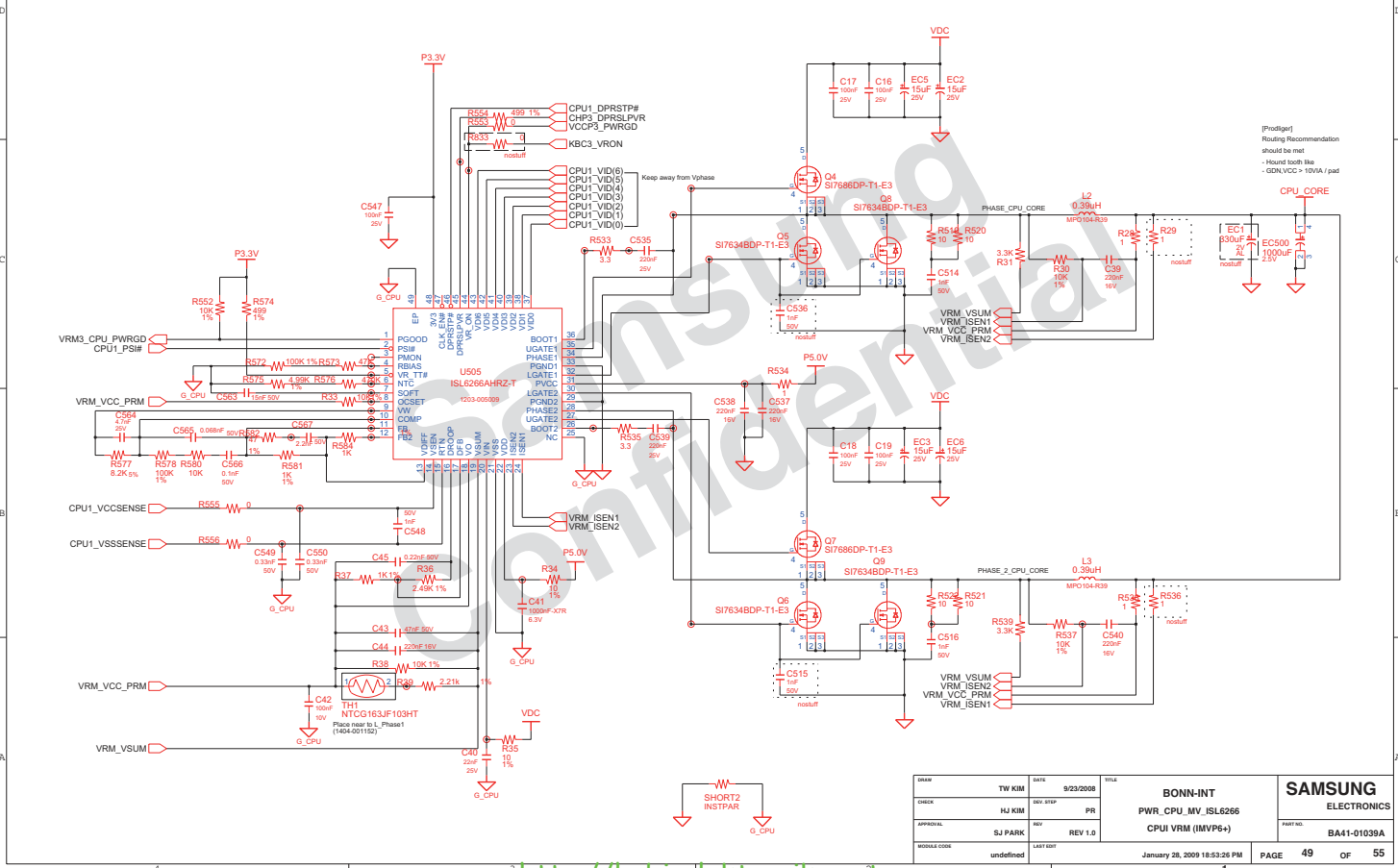


<http://hobi-elektronika.net>

DATE	TW KIM	DATE	9/23/2008	TITLE	BONN-INT PWR_MV_Cantiga		SAMSUNG ELECTRONICS
DRAWN	HJ KIM	REV. DATE		PR			
CHECKED	SJ PARK	REV	REV 1.0		P1.5V_AUX, P1.05V		PART NO. BA41-01039A
APPROVAL		LAST EDIT			January 28, 2009 18:53:26 PM		PAGE 48 OF 55
MODEL CODE							

CPU VRM [INTERSIL]

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[Footnote]
 Routing Recommendation
 should be met
 - Mount both the
 - GDN VCC > 10V/A / pad

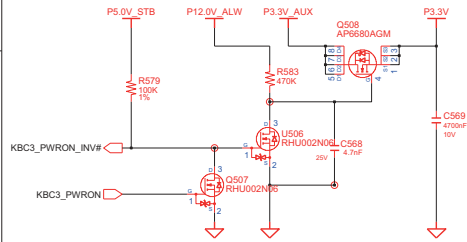
DESIGN	TW KIM	DATE	9/23/2008	TITLE	BONN-INT PWR_CPU_MV_ISL6266		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV	STEP	PR	CPU1 VRM (MVP6+)		
APPROVAL	SJ PARK	REV	VER	1.0			PART NO. BA41-01039A
MODULE CODE	undefined	LAST DESG	January 28, 2009 18:53:26 PM		PAGE	49	OF 55

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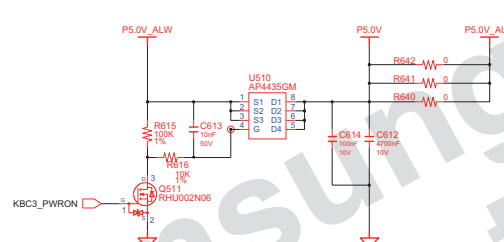
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Switched Power

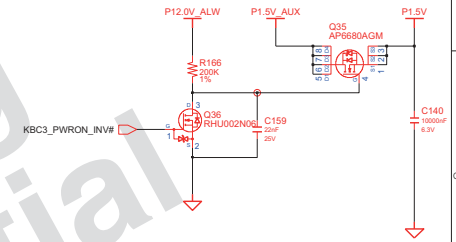
Switched Power On (P3.3V)



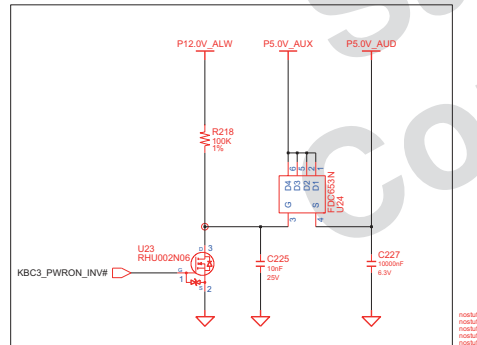
Switched Power On (P5.0V)



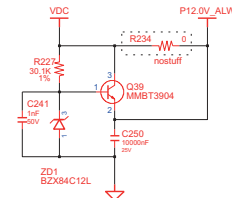
Switched Power On (P1.5V)



Audio Power (nostuff)



P12.0V_ALW



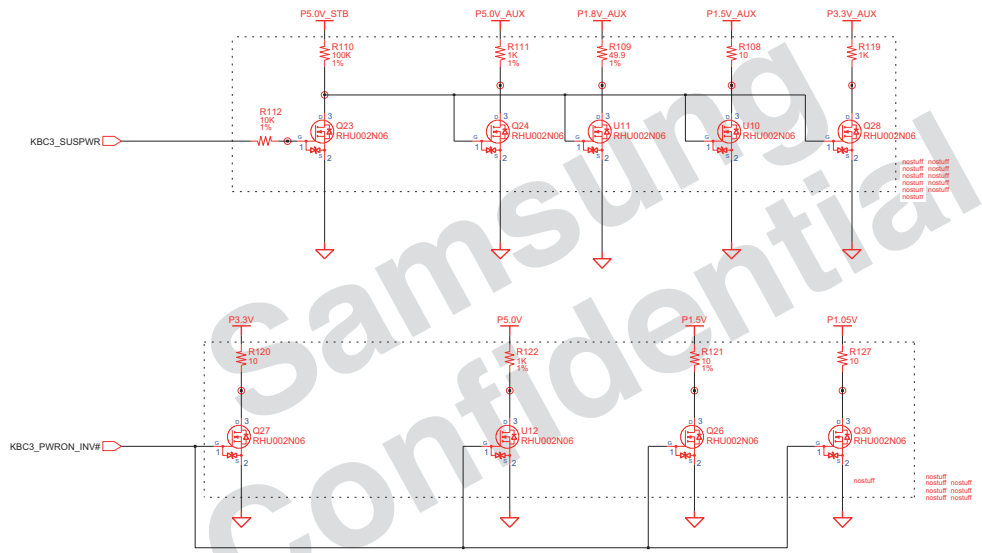
nostuff
nostuff
nostuff
nostuff

<http://hobi-elektronika.net>

DRAW	TW KM	DATE	9/23/2008	TITLE	BONN-INT PWR_MV_SWITCHED		SAMSUNG ELECTRONICS	
CHECK	HJ KM	REV./STEP	PR	APPROVAL	SWITCHED POWER		PART NO. BA41-01039A	
APPROVAL	SJ PARK	REV.	REV 1.0	MODEL CODE	LAST EDIT		PAGE 50 OF 55	
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POWER DISCHARGER



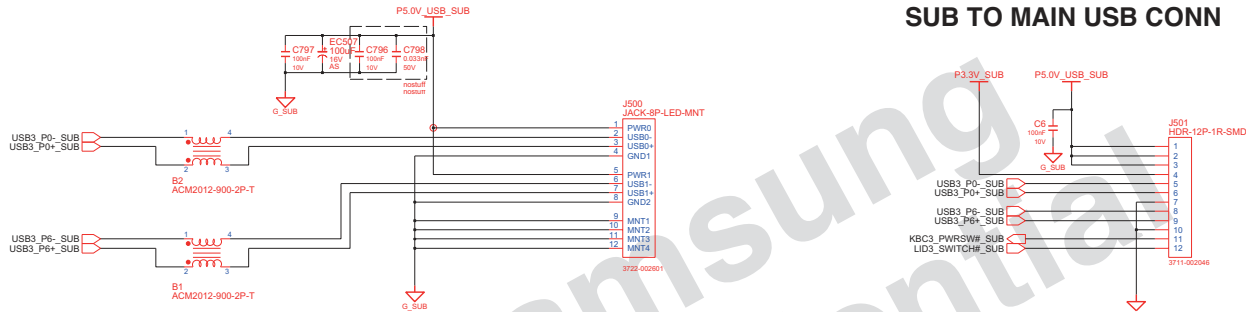
DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT PWR_MV_DISCHARGER		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR	DISCHARGING LOGIC		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0	January 28, 2009 18:53:26 PM		BA41-01039A	PAGE 51 OF 55
MODULE CODE	undefined	LAST EDIT					

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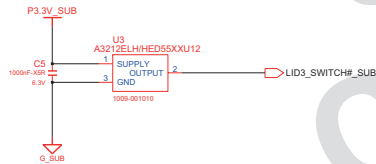
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2 USB PORT & POWER S/W SUB B'D

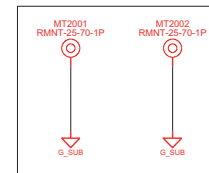
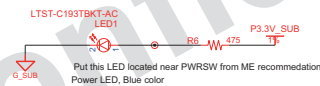
SUB TO MAIN USB CONN



LID_SWITCH

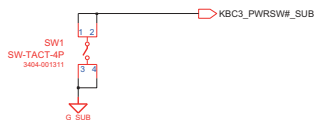


Power ON LED



USB sub board mount hole

Power Switch Button



<http://hobi-elektronika.net>

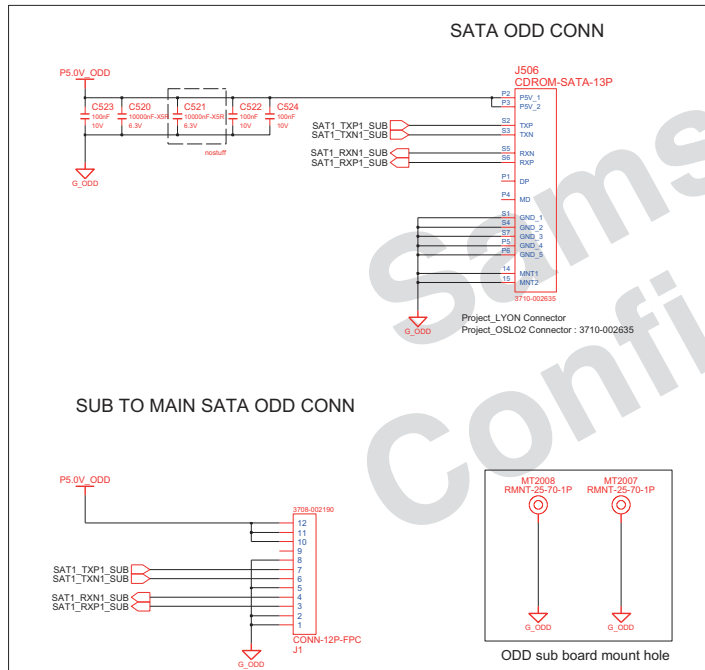
DESIGN	TW KM	DATE	9/23/2008	TITLE	BONN-INT SUB BOARD1		SAMSUNG ELECTRONICS
CHECK	HJ KM	REV./STEP	PR	2 USB & POWER SW		PART NO. BA41-01039A	
APPROVAL	SJ PARK	REV.	REV 1.0				
MODEL CODE		LAST EDIT		January 28, 2009 18:53:26 PM		PAGE	52 OF 55

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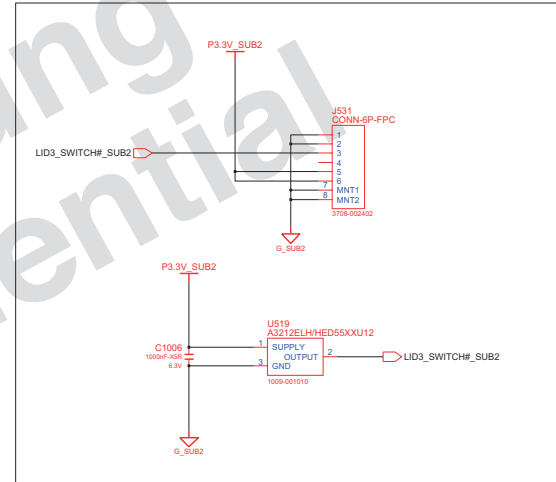
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SATA ODD & LID SW SUB BOARD

SATA ODD SUB BOARD



LID SWITCH SUB BOARD

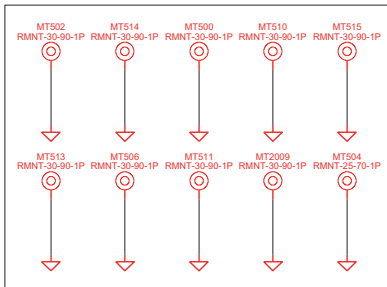


DRAW	TW KIM	DATE	9/23/2008	TITLE	BONN-INT SUB BOARD2		SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	PR	SATA ODD SUB BOARD		PART NO.	
APPROVAL	SJ PARK	REV	REV 1.0			BA41-01039A	
MODULE CODE	undefined	LAST EDIT	January 28, 2009 18:53:26 PM		PAGE	53 OF 55	

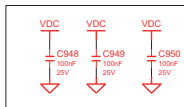
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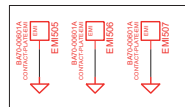
Mainboard Mount ((30,80)x9), (30,90)x9), (25,70)x1))



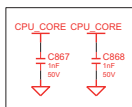
Top : (30,80) x 9
Bot : (30,90) x 9



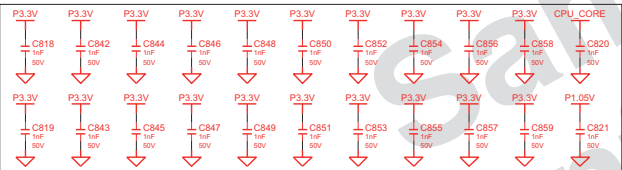
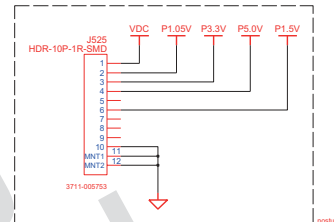
Add for EMC (LAN), 2008.11.19



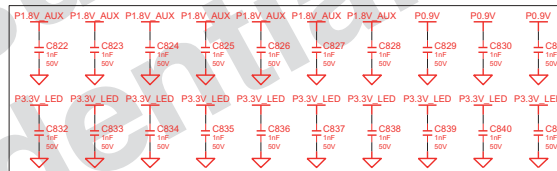
Add for ESD(top), 2009.01.14



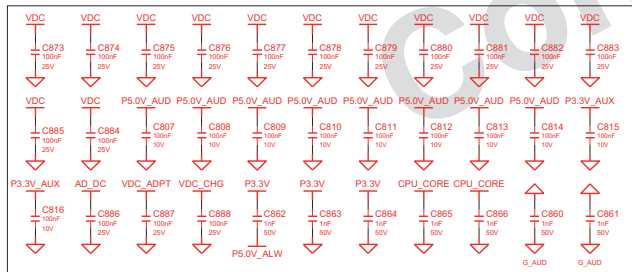
Add for EMC (Top), 2008.11.19



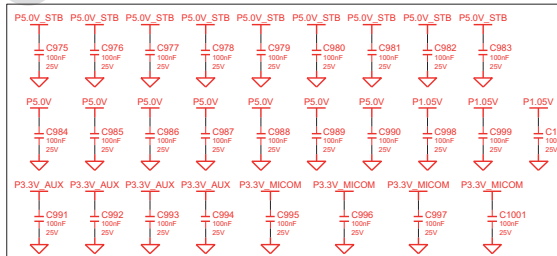
Add for EMC (5th Layer), 2008.11.19



Add for EMC (Bottom), 2008.11.19



Add for EMC (Bottom), 2008.11.19



Add for EMC (Bottom), 2009.01.28

ICT PORT

<http://hobi-elektronika.net>

DRAW	TW KIM	DATE	9/23/2008	TITLE		
CHECK	HJ KIM	REV. STEP	PR	BONN-INT		SAMSUNG ELECTRONICS
APPROVAL	SJ PARK	REV.	REV 1.0	ICT PORT		
MODEL CODE		LAST DATE		ICT PORT		PART NO. BA1-01039A
				January 28, 2009 18:53:26 PM		PAGE 54 OF 55

