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CANNES-L / BONN-L NVIDIA(N-10M-GE)

CPU : Intel Pentium
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : R719 / R519
PBA Name : MAIN
PCB Code : GCE BA41-01146A
 NANYA BA41-01147A
 HST BA41-01148A
Dev. Step : PR
Revision : 1.0
T.R. Date : 2009.08.07

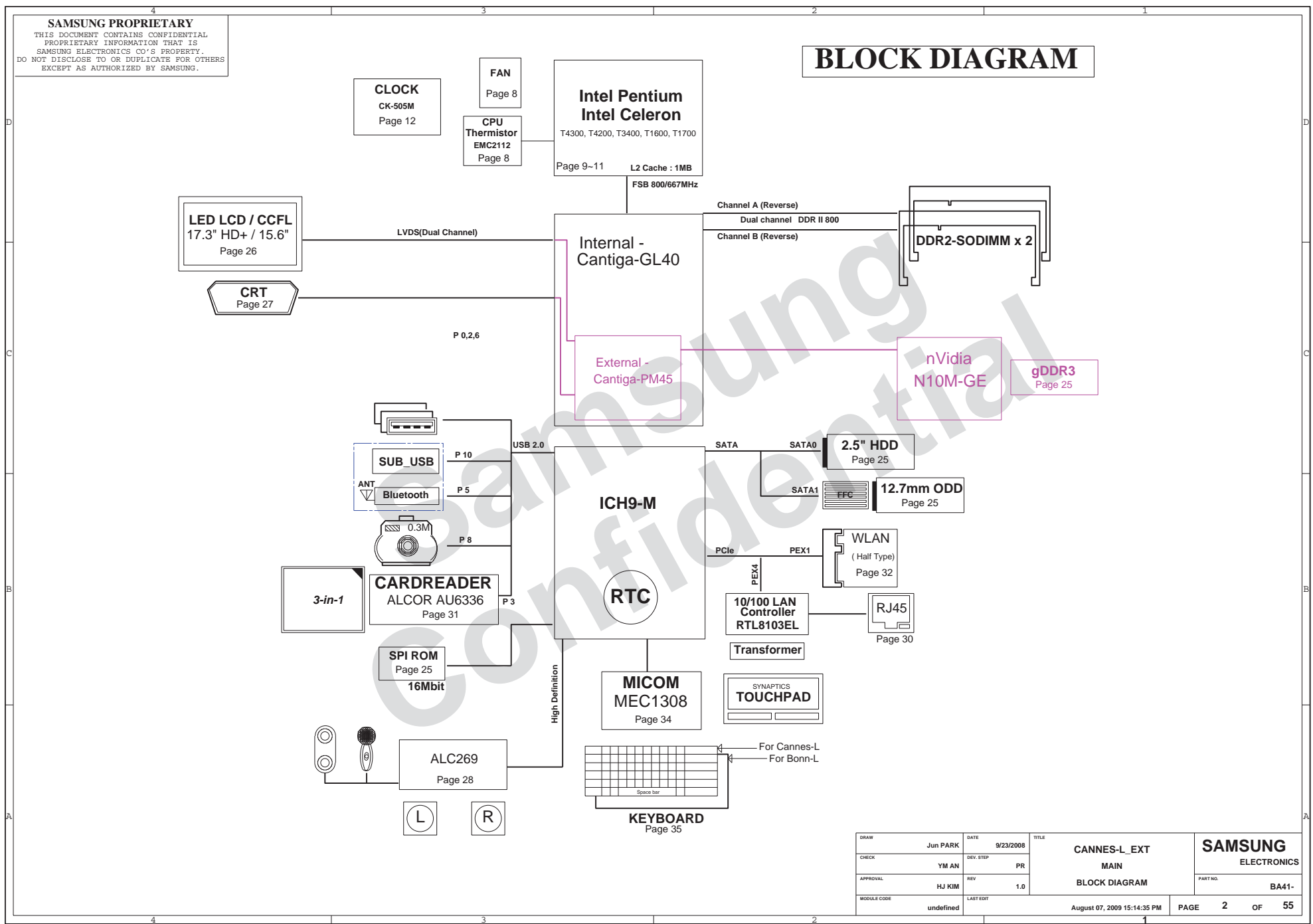
Design	CHECK	APPROVAL

■ Owner : SEC Mobile R & D Signature : X

DRAW	Jun PARK	DATE	10/10/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MAIN	COVER	
APPROVAL	HJ KIM	REV	1.0			PART NO. BA41-
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 1 OF 55	

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BLOCK DIAGRAM



DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT MAIN	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR			
APPROVAL	HJ KIM	REV	1.0		BLOCK DIAGRAM	PART NO. BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	2	OF 55

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9M	Master		SMBUS Master
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 001X	A4h	-
MICOM	Master		
BATTERY	0001 011X	16h	
EMC2102	0111 101X	7Ah	

USB PORT Assignation

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCl_0	0 USB PORT (LEFT, BOTTOM)	UHCl_3	6 USB PORT (LEFT, TOP)
UHCl_1	2 USB PORT (LEFT,CENTER)	UHCl_4	8 CAMERA
UHCl_2	3 CARD READER(AU6336)	UHCl_5	10 SUB_USB(TBD)
	4 BLUETOOTH		11

SATA Assignation

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA2	-	SATA3	-

PCI EXPRESS Assignation

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCle1	WLAN	PCle2	Wired LAN
PCle3	-	PCle4	-

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	
Crystal	10MHz	MICOM	
Crystal	14.318MHz	CLOCK-Generator	
Crystal	25MHz	LAN	

Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
VDC_ADPPT	Primary DC system power supply (9 to 19V)	P1.05V_PEG	P1.05V (Direct Media Interface Compensation)
VDC	Charger Reference Voltage Source	P5.0V	5.0V Power Rail (off in S3-S5)
VDC_CHG	3.3V supply for the RTC well.	P3.3V	3.3V Power Rail (off in S3-S5)
PRTC_BAT	5.0V always power well	P1.05	1.05V Power Rail (off in S3-S5)
P5.0V_ALW	12.0V always power well	P0.9V	DDR2 Termination
P12.0V_ALW	Power Chip Reference	P5.0V_AUX	5.0V Power Rail (off in S4-S5)
P1.7V_VREF	Power Chip Reference	P3.3V_AUX	3.3V Power Rail (off in S4-S5)
P2.0V_VREF	Power Chip Reference	P1.8_AUX	1.8V Power Rail (off in S4-S5)
P5.0V_VREF_FILT	Power Chip Reference	CPU_CORE	Core Voltage for CPU
P3.3V_MICOM	Output voltage of TPS51125 (if VDC is removed, it will be off)	AUD_P5V	5.0V supply for Audio
LCD_VDD3V	3.3V (LED LCD)	P4.75V_AUD	Audio Analog Voltage
KBC3_CHG4.2V	To charge battery	P5.0V_STB	To charge USB device at sleep status
P1.2V_LAN	Internal Regulator's Power of LAN Controller	P5.0V_ODD	5.0V supply at SUB_ODD Board
P3.3V_MCD	3.3V (3-in-1 Socket)	EGFX_CORE	nVidia Graphic Chip power
		P1.5V	1.5V Power Rail (off in S3-S5)
		P1.5_AUX	1.5V Power Rail (off in S4-S5)
		P1.8V	1.8V Power Rail (off in S3-S5)

Power source of External

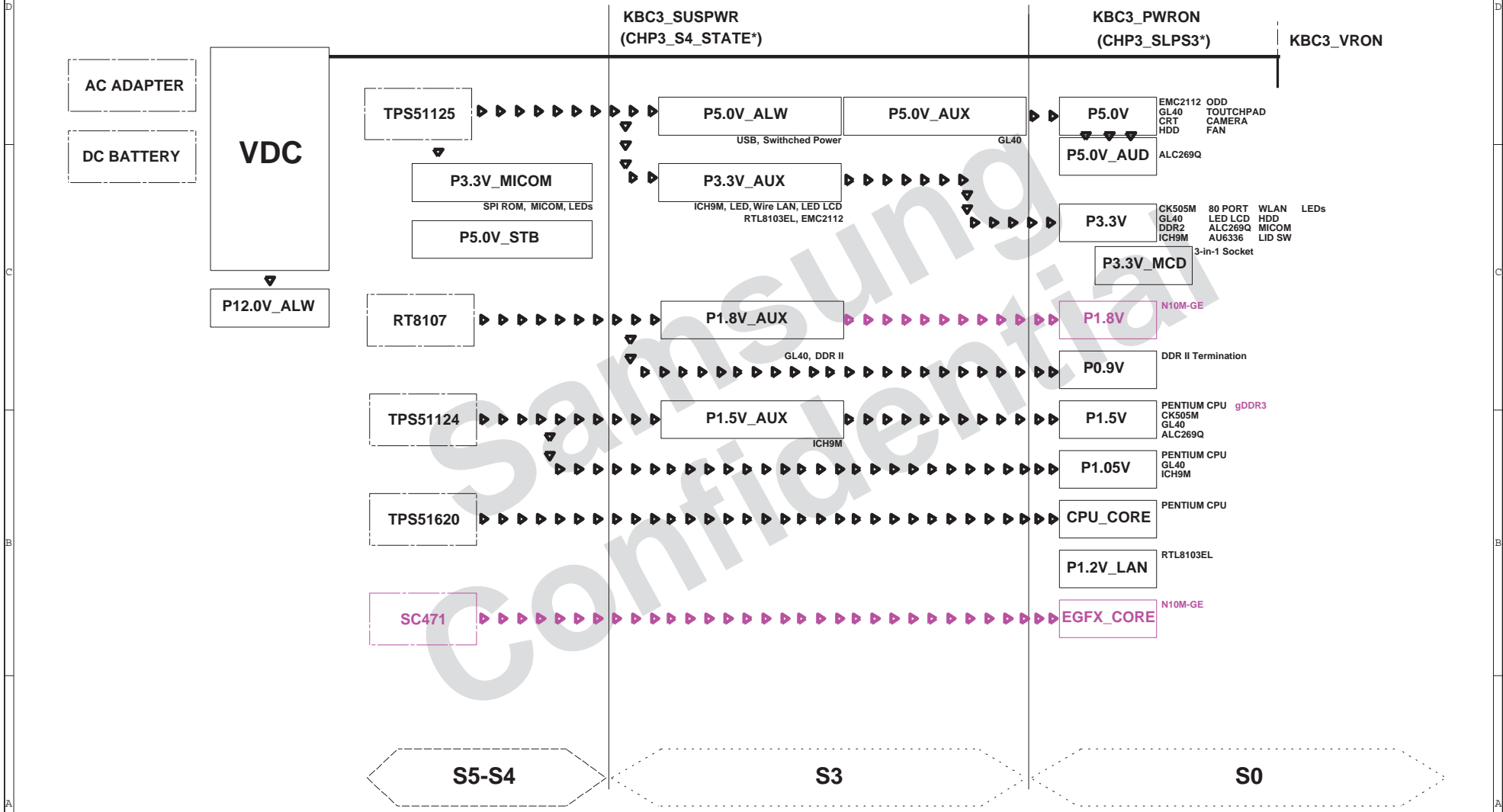
REVISION HISTORY

See rev notes for more information.

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	MAIN		
APPROVAL	HJ KIM	REV	1.0	BOARD INFO	PART NO.	BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	3	OF 55

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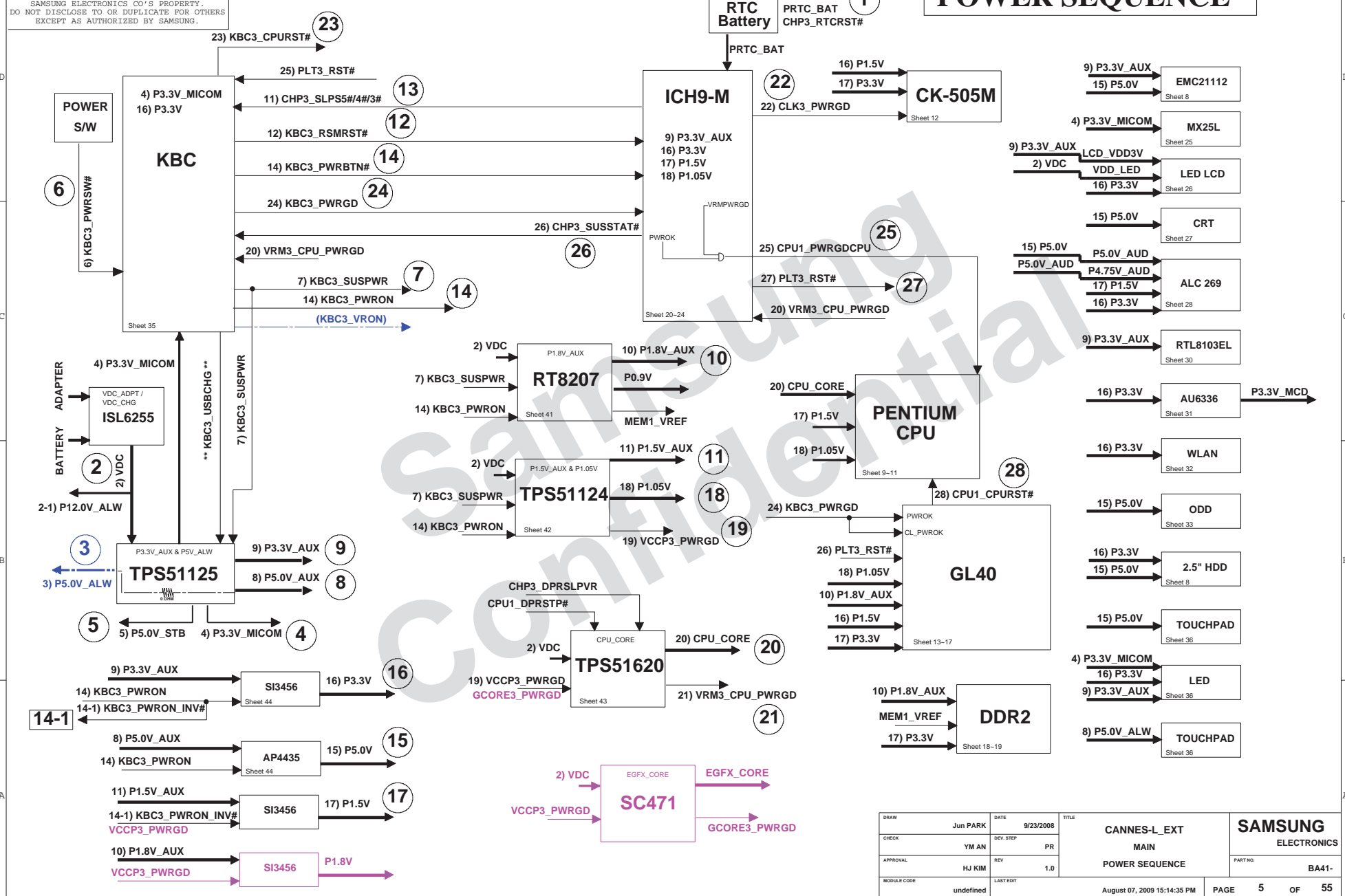
POWER DIAGRAM



DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MAIN	MAIN	
APPROVAL	HJ KIM	REV	1.0	POWER DIAGRAM		PART NO. BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	4	OF 55

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POWER SEQUENCE

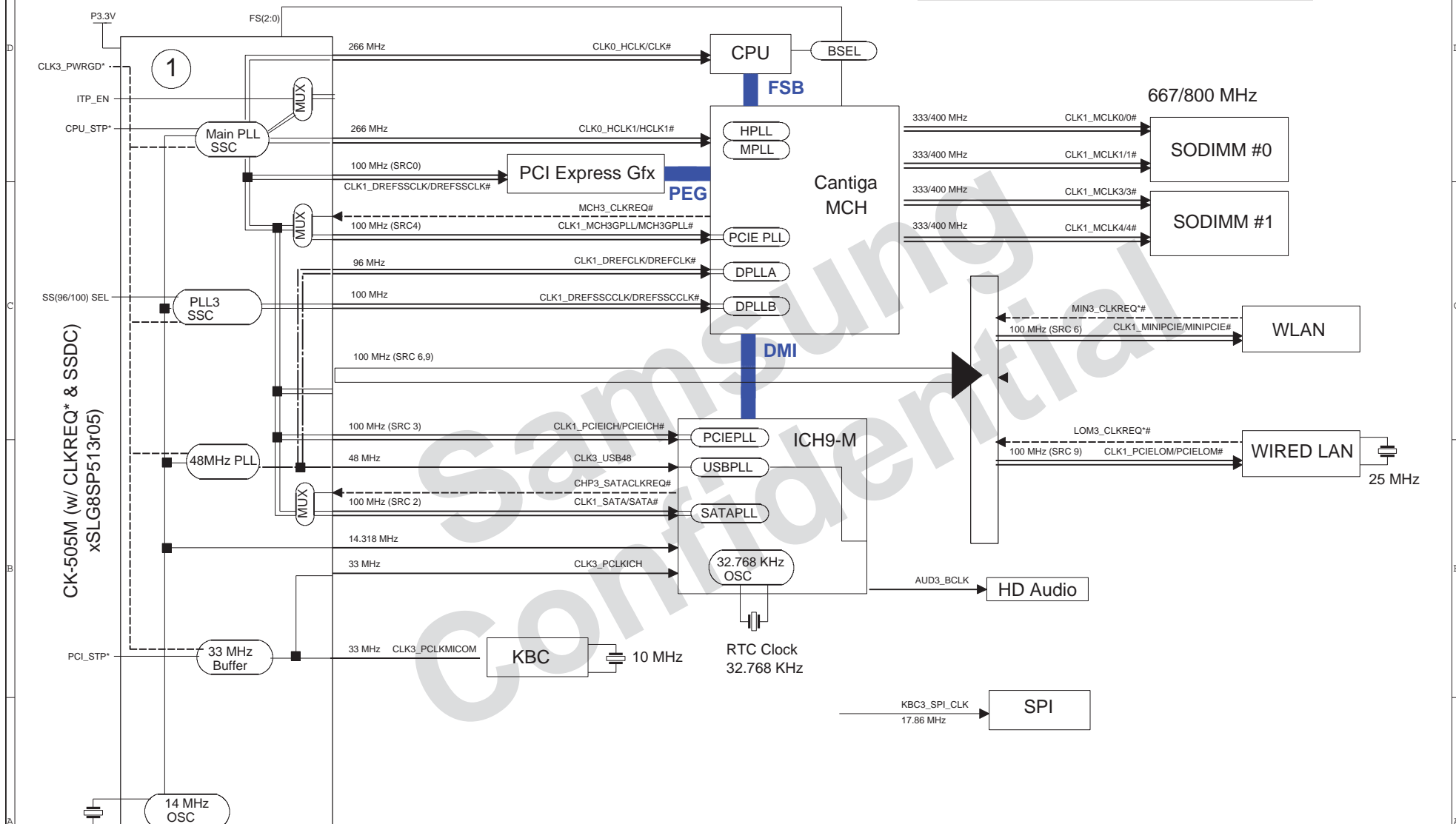


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CHECK	YM AN	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	HJ KIM	REV	1.0	POWER SEQUENCE	BA41-	
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	5	OF 55

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CLOCK DISTRIBUTION



CK-505M (w/ CLKREQ* & SSDC)
xSLG8SP513r05

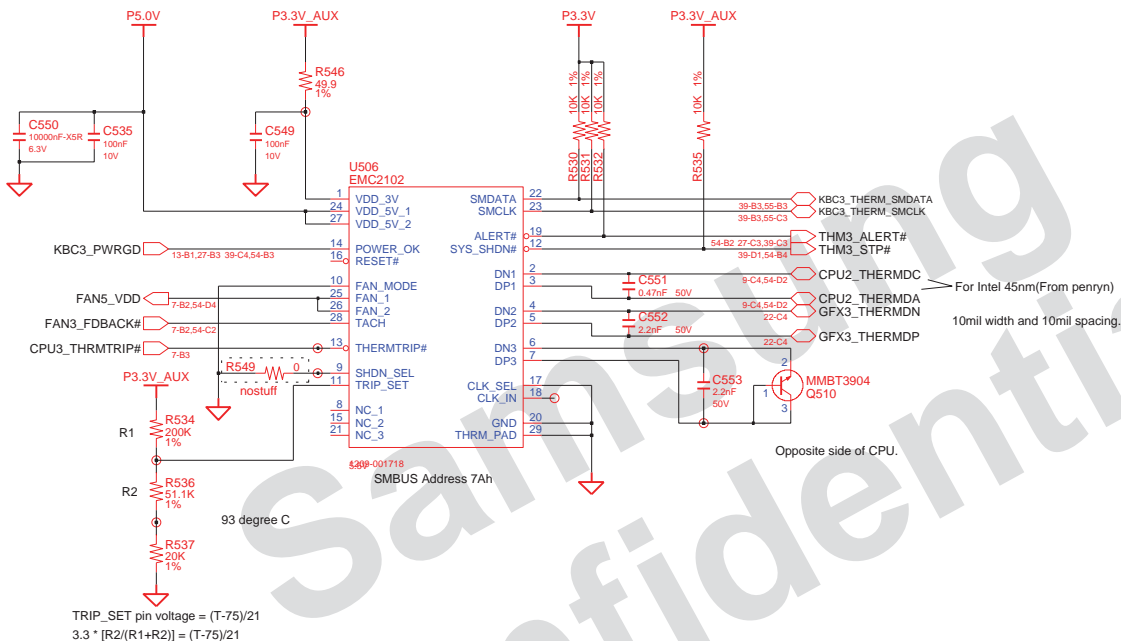
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DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MAIN		
APPROVAL	HJ KIM	REV	1.0	CLOCK DIAGRAM	PART NO.	BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	6	OF 55

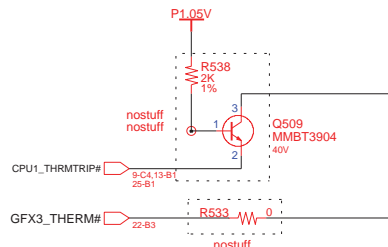
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THERMAL SENSOR & FAN CONTROL

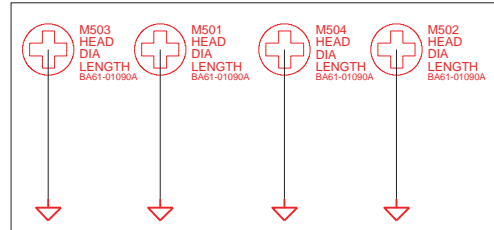
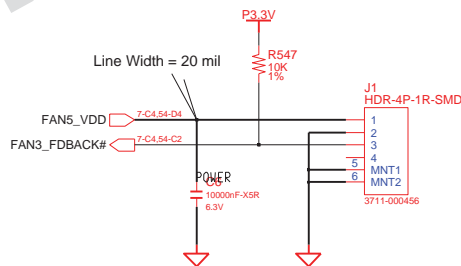


TRIP_SET pin voltage = $(T-75)/21$
 $3.3 * [R2/(R1+R2)] = (T-75)/21$



SHDN_SEL MODE	
0	INTEL TR MODE
<input checked="" type="checkbox"/>	HIGH Z
1	AMD CPU/DIODE MODE
	EXT.DIODE 2 MODE

ADDRESSSEL MODE	
0	0101 111xb
<input checked="" type="checkbox"/>	HIGH Z
	0111 101xb (7A)
1	0101 110xb

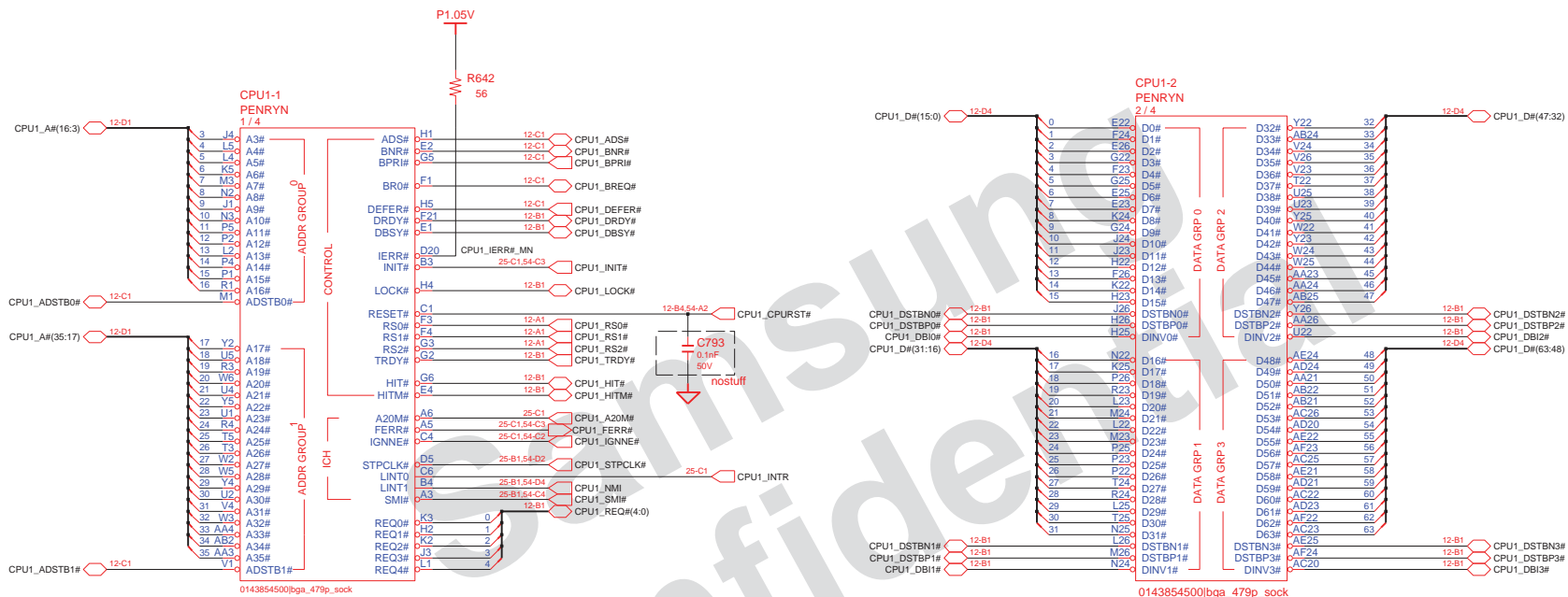


To support heatsink

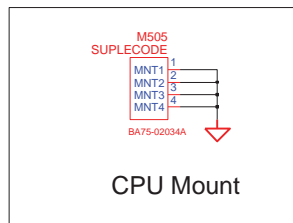
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS	
CHECK	YM AN	DEV.STEP	PR		THERMAL SENSOR		
APPROVAL	HJ KIM	REV	1.0		THERMAL SENSOR EMC2112	PART NO.	
MODULE CODE		LAST EDIT				BA41-	
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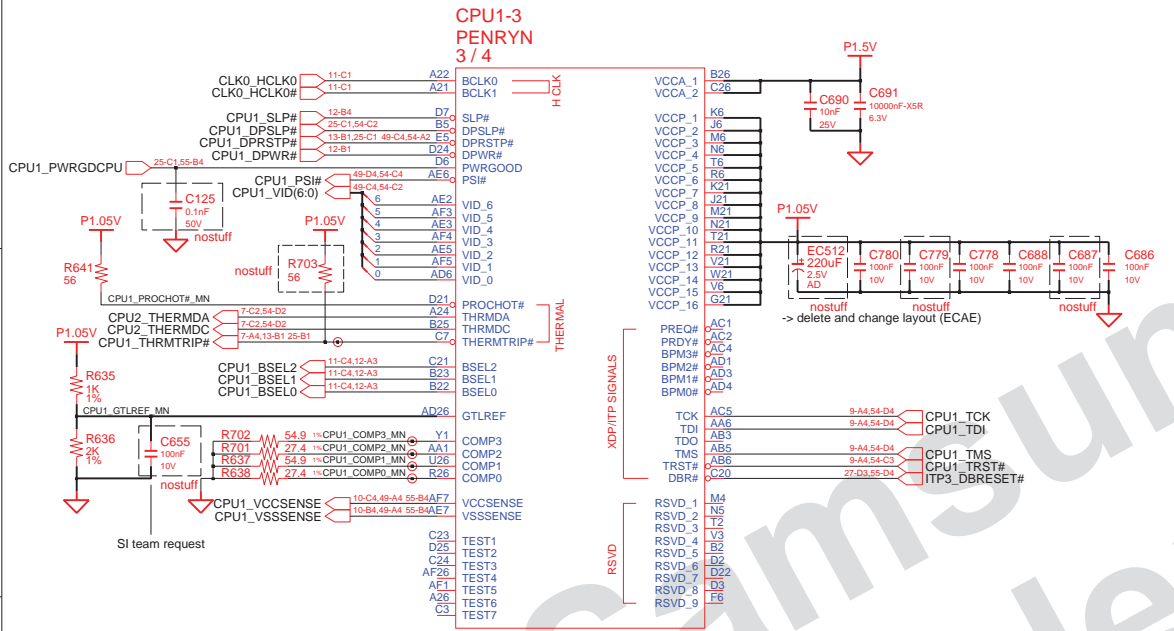


CPU Socket : 3704-001153



DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT CPU	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR			
APPROVAL	HJ KIM	REV	1.0		PENRYN (1/3)	PART NO. BA41-
MODULE CODE	undefined	LAST EDIT		August 07, 2009 15:14:35 PM	PAGE	8 OF 55

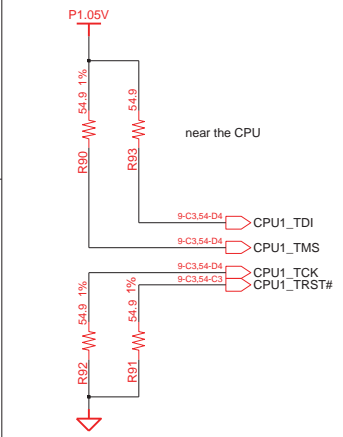
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0143854500bga_479p_sock

CPU Socket : 3704-001153

FSC	FSB	FSA	FRQ
0	0	0	266M
0	1	0	200M
0	1	1	166M



BSEL

FSB	Pull-down
FSB 1067 MHz	BSEL0, BSEL1, BSEL2
FSB 800 MHz	BSEL0, BSEL2

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 1 0 0	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 1	0.9625 V	1 0 1 1 0 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 1 0 1 0	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 1 1 0 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 1 1 1 0	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 1 1 1	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 1 0	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 1	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 1 0 0 0 0 0	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 1	1.1000 V	1 0 0 0 1 1 1	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 1 0	1.0875 V	1 0 0 1 0 0 0	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 1	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 1 0 0	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 1	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 1 0	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 1	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 1 0 0 0	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 1 0 0 1	1.0000 V	1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
0 1 0 1 0 1 0	0.9875 V	1 0 0 1 1 1 1	0.4875 V	1 1 1 1 0 1 0	0.0000 V
0 1 0 1 0 1 1	0.9750 V	1 0 0 1 1 1 1	0.4750 V	1 1 1 1 0 1 1	0.0000 V
0 1 0 1 1 0 0	0.9625 V	1 0 0 1 1 1 1	0.4625 V	1 1 1 1 1 0 0	0.0000 V
0 1 0 1 1 0 1	0.9500 V	1 0 0 1 1 1 1	0.4500 V	1 1 1 1 1 0 1	0.0000 V
0 1 0 1 1 1 0	0.9375 V	1 0 0 1 1 1 1	0.4375 V	1 1 1 1 1 1 0	0.0000 V
0 1 0 1 1 1 1	0.9250 V	1 0 0 1 1 1 1	0.4250 V	1 1 1 1 1 1 1	0.0000 V

GTLREF : Keep the Voltage divider within 0.5° of the first GTLREF0 pin with Zo=50ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(50ohm) trace shorter than 1/2" to their respective Banias socket pins.

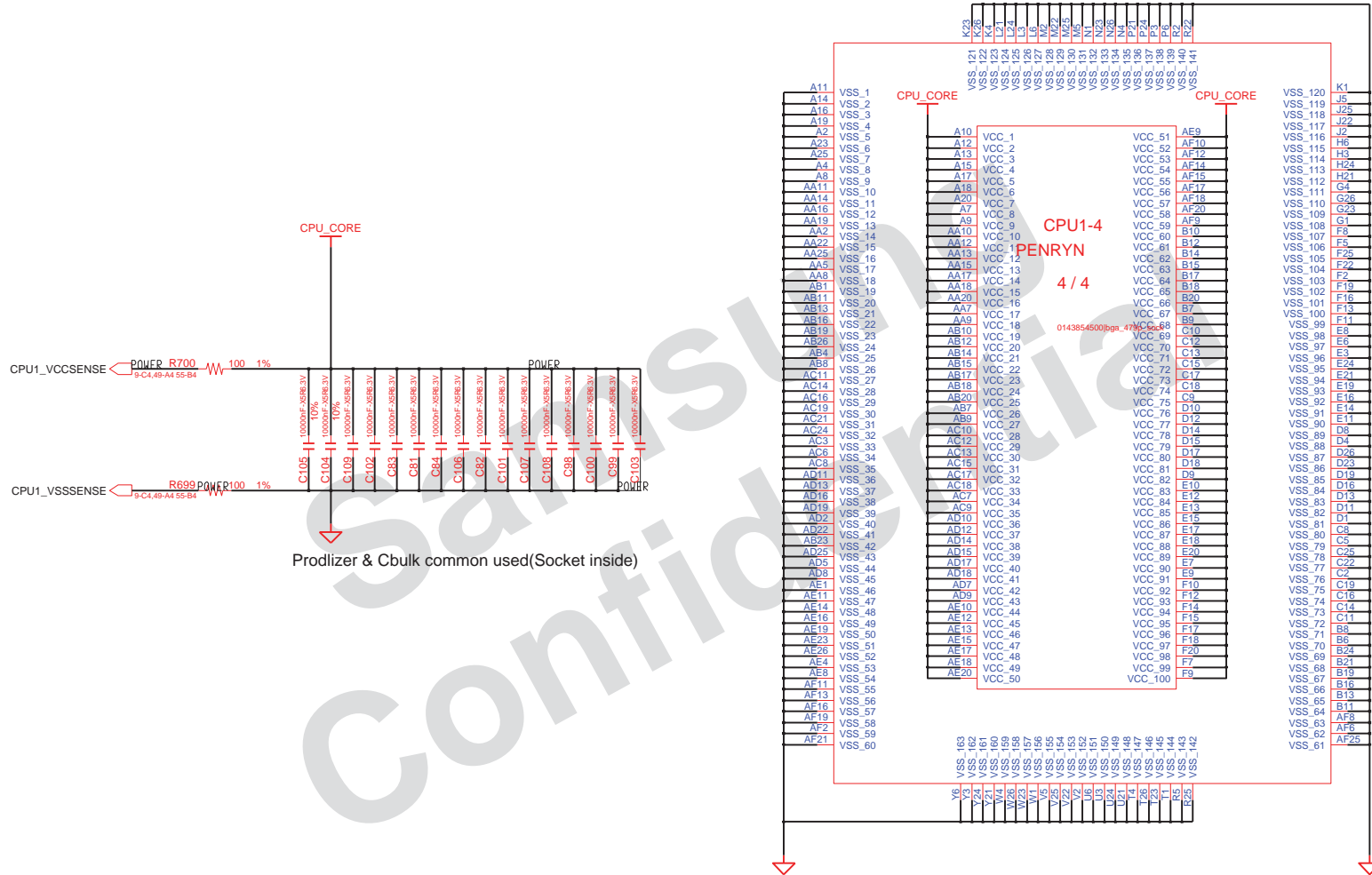
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=50ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	CPU	PENRYN (2/3)	
APPROVAL	HJ KIM	REV	1.0			PART NO. BA41-
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Prodizer & Cbulk common used(Socket inside)

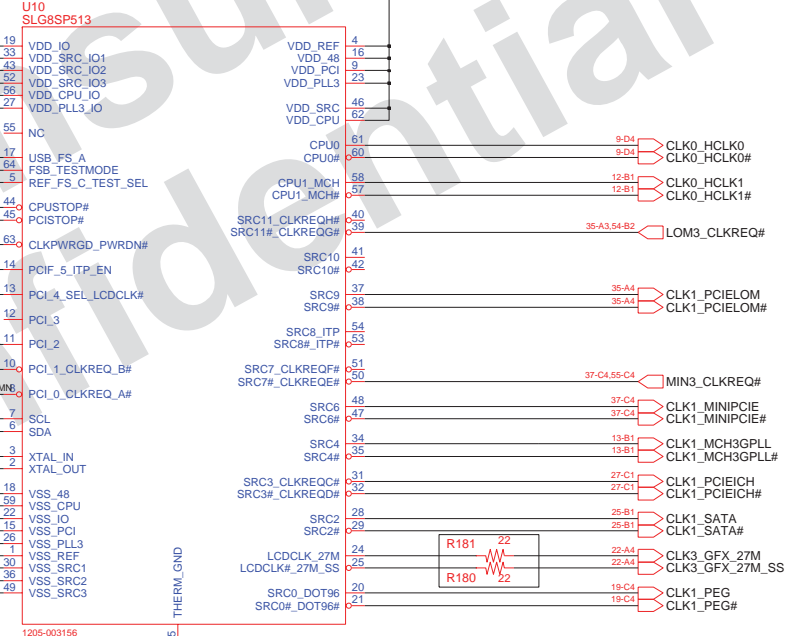
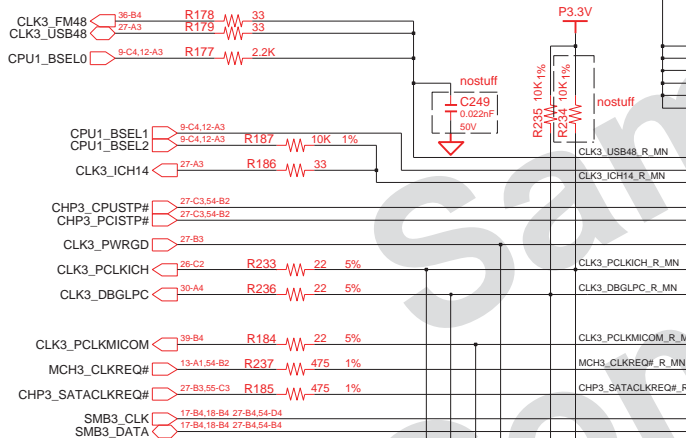
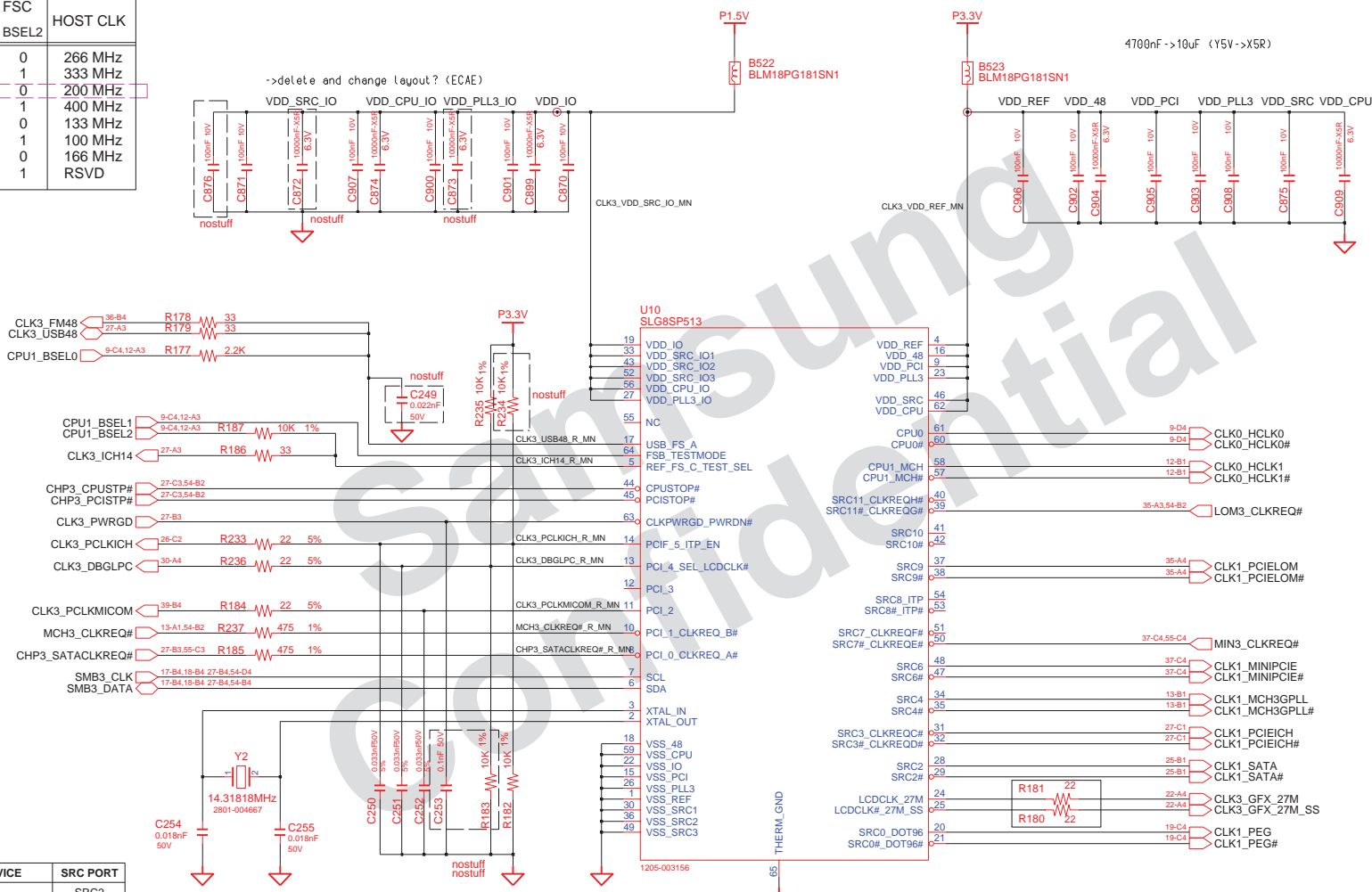
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR		CPU	
APPROVAL	HJ KIM	REV	1.0		PENRYN (3/3)	PART NO. BA41-
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CK505M

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

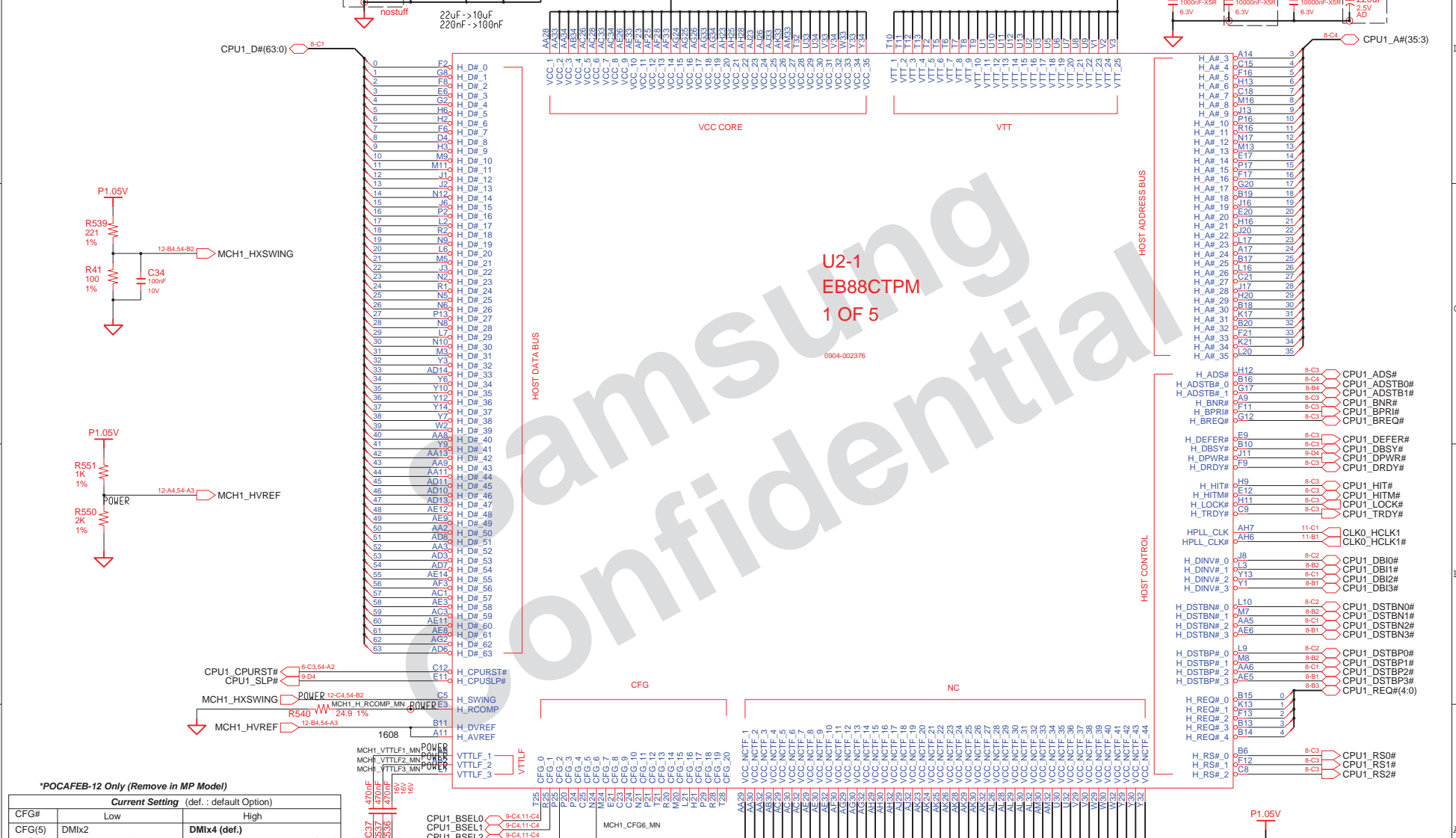
Place 14.318MHz within 500mils of CK-505

This part is 64pin QFN package.

IDT : 1205-003159
SL : 1205-003533

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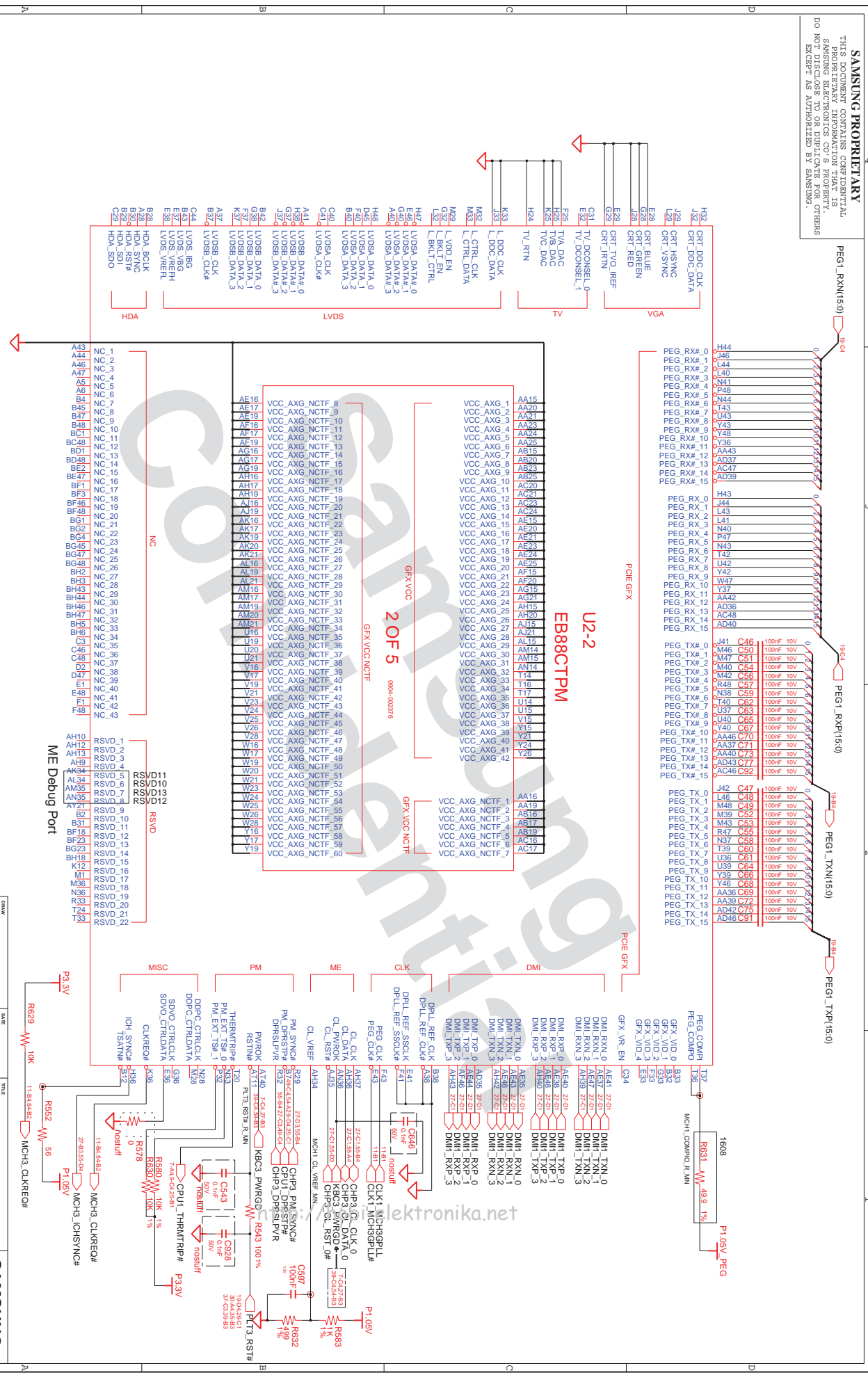
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***POCAFEB-12 Only (Remove in MP Model)**

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	iTPM Host Interface Enable	iTPM Host Interface Disable (def.)
CFG(7)	ME Crypto no confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIe Loop Back Enable	PCIe Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIe X1 Only(def.)	SDVO and PCIe X1 Simultaneously

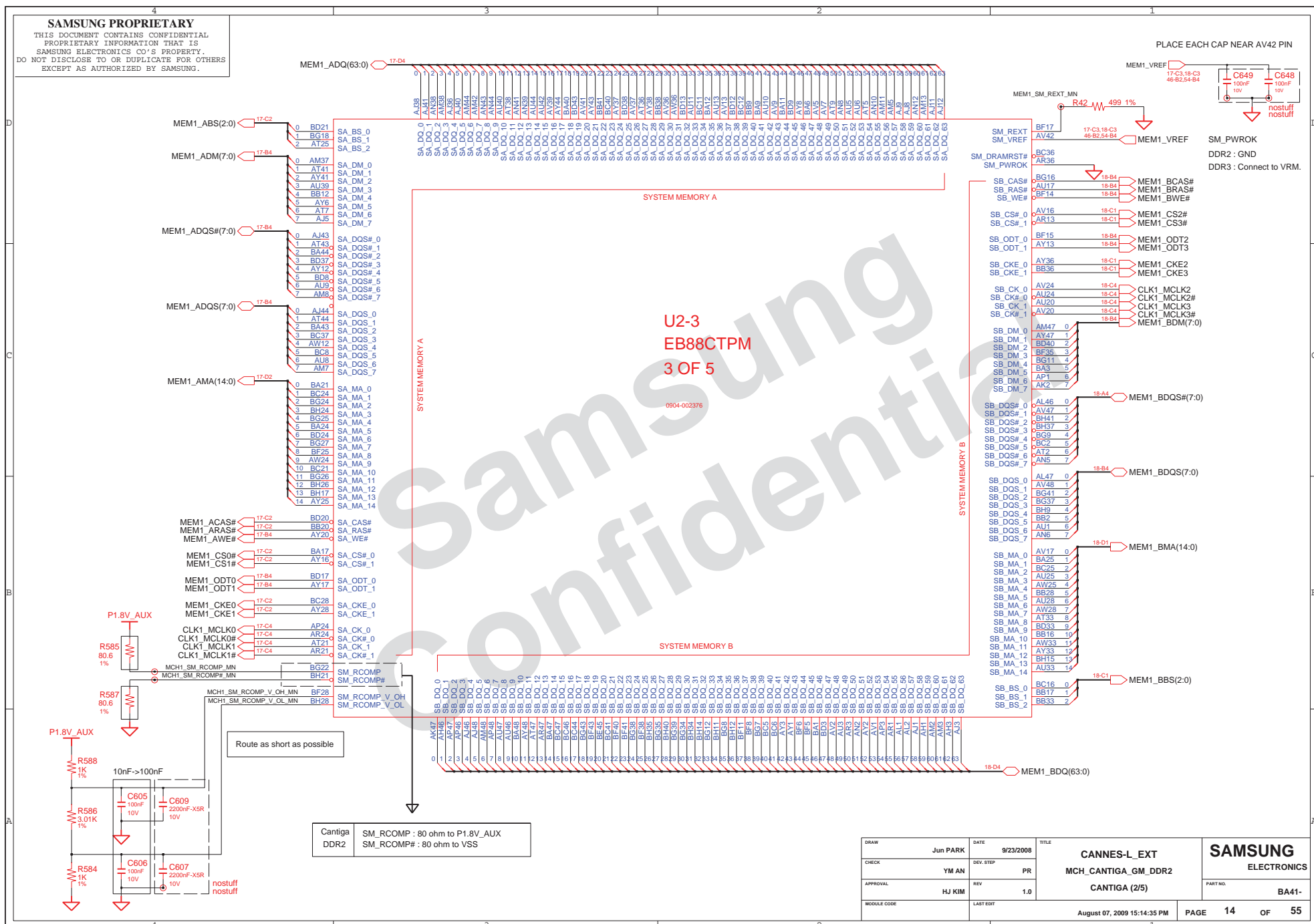
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CHECK	YM AN	DEV. STEP	PR	MCH_CANTIGA_GM_DDR2	PART NO.	
APPROVAL	HJ KIM	REV	1.0	CANTIGA (1/5)	BA41-	
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	12	OF 55



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PLACE EACH CAP NEAR AV42 PIN



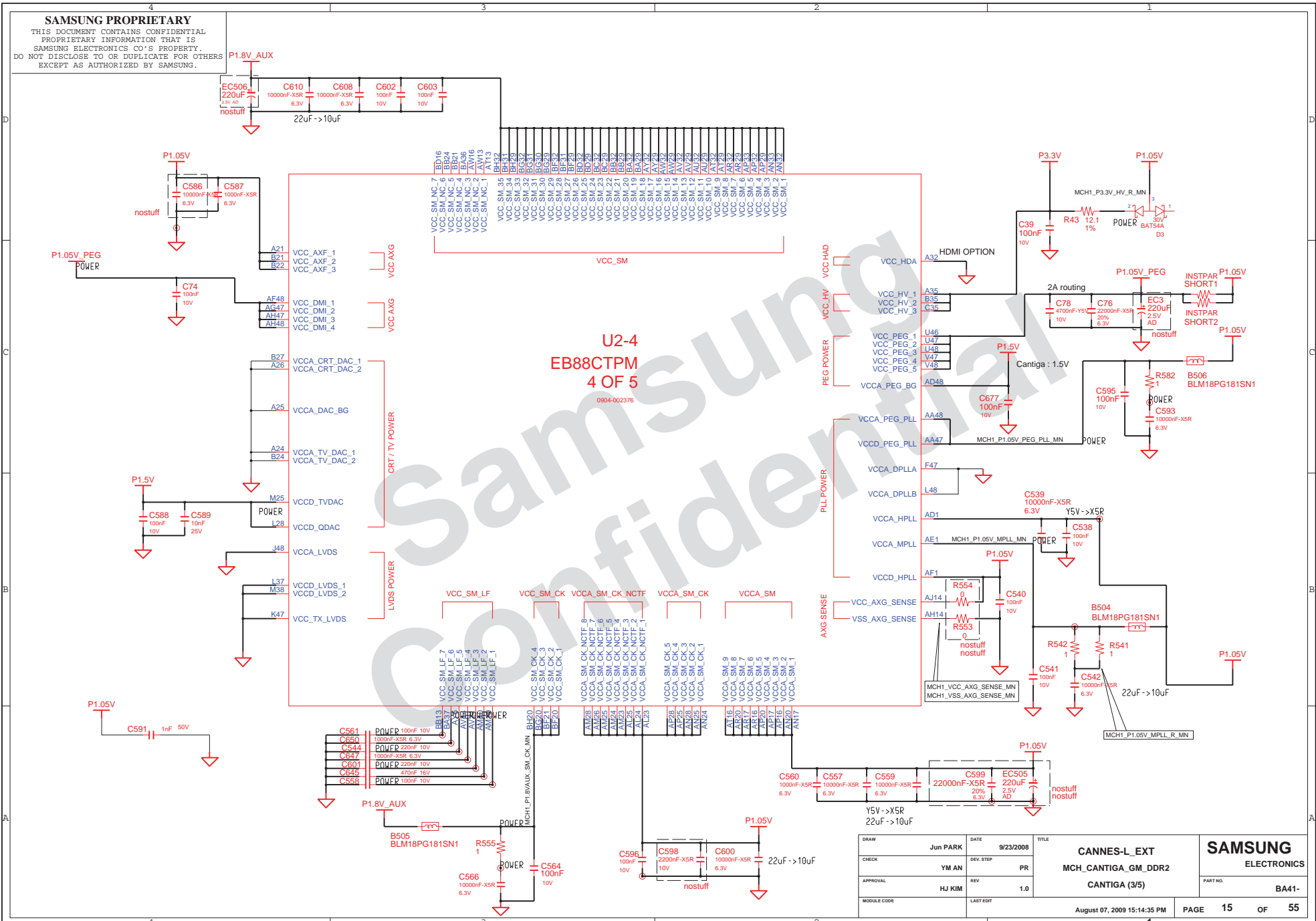
MEM1_ADQ(63:0)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63							
MEM1_ABS(2:0)	0	1	2																																																																				
MEM1_ADM(7:0)	0	1	2	3	4	5	6	7																																																															
MEM1_ADQS(7:0)	0	1	2	3	4	5	6	7																																																															
MEM1_ADQS(7:0)	0	1	2	3	4	5	6	7																																																															
MEM1_ADQS(7:0)	0	1	2	3	4	5	6	7																																																															
MEM1_AMA(14:0)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14																																																								
MEM1_ACAS#	0																																																																						
MEM1_ARAS#	0																																																																						
MEM1_AWE#	0																																																																						
MEM1_CS0#	0																																																																						
MEM1_CS1#	0																																																																						
MEM1_ODT0	0																																																																						
MEM1_ODT1	0																																																																						
MEM1_CKE0	0																																																																						
MEM1_CKE1	0																																																																						
CLK1_MCLK0	0																																																																						
CLK1_MCLK0#	0																																																																						
CLK1_MCLK1	0																																																																						
CLK1_MCLK1#	0																																																																						
MCH1_SM_RCAMP#_MN	0																																																																						
MCH1_SM_RCAMP#_V_OH_MN	0																																																																						
MCH1_SM_RCAMP#_V_OL_MN	0																																																																						
MCH1_SM_RCAMP#_MN	0																																																																						
MCH1_SM_RCAMP#_V_OH	0																																																																						
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SM_RCAMP#_MN	0																																																																						
SM_RCAMP#_V_OH	0																																																																						
SM_RCAMP#_V_OL	0																																																																						
SM_REXT	0																																																																						
SM_VREF	0																																																																						
SM_DRAMRST#	0																																																																						
SM_PWROK	0																																																																						
SB_CAS#	0																																																																						
SB_RAS#	0																																																																						
SB_WE#	0																																																																						
SB_CS#_0	0																																																																						
SB_CS#_1	0																																																																						
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SB_DQS#_3	0																																																																						
SB_DQS#_4	0																																																																						
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SB_DQS#_6	0																																																																						
SB_DQS#_7	0																																																																						
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SB_MA_11	0																																																																						
SB_MA_12	0																																																																						
SB_MA_13	0																																																																						
SB_MA_14	0																																																																						
SB_BS_0	0																																																																						
SB_BS_1	0																																																																						
SB_BS_2	0																																																																						
SB_DS_0	0																																																																						
SB_DS_1	0																																																																						
SB_DS_2	0																																																																						

Cantiga	SM_RCAMP# : 80 ohm to P1.8V_AUX
DDR2	SM_RCAMP# : 80 ohm to VSS

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	MCH_CANTIGA_GM_DDR2	PART NO.	
APPROVAL	HJ KIM	REV	1.0	CANTIGA (2/5)	BA41-	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE	14 OF 55

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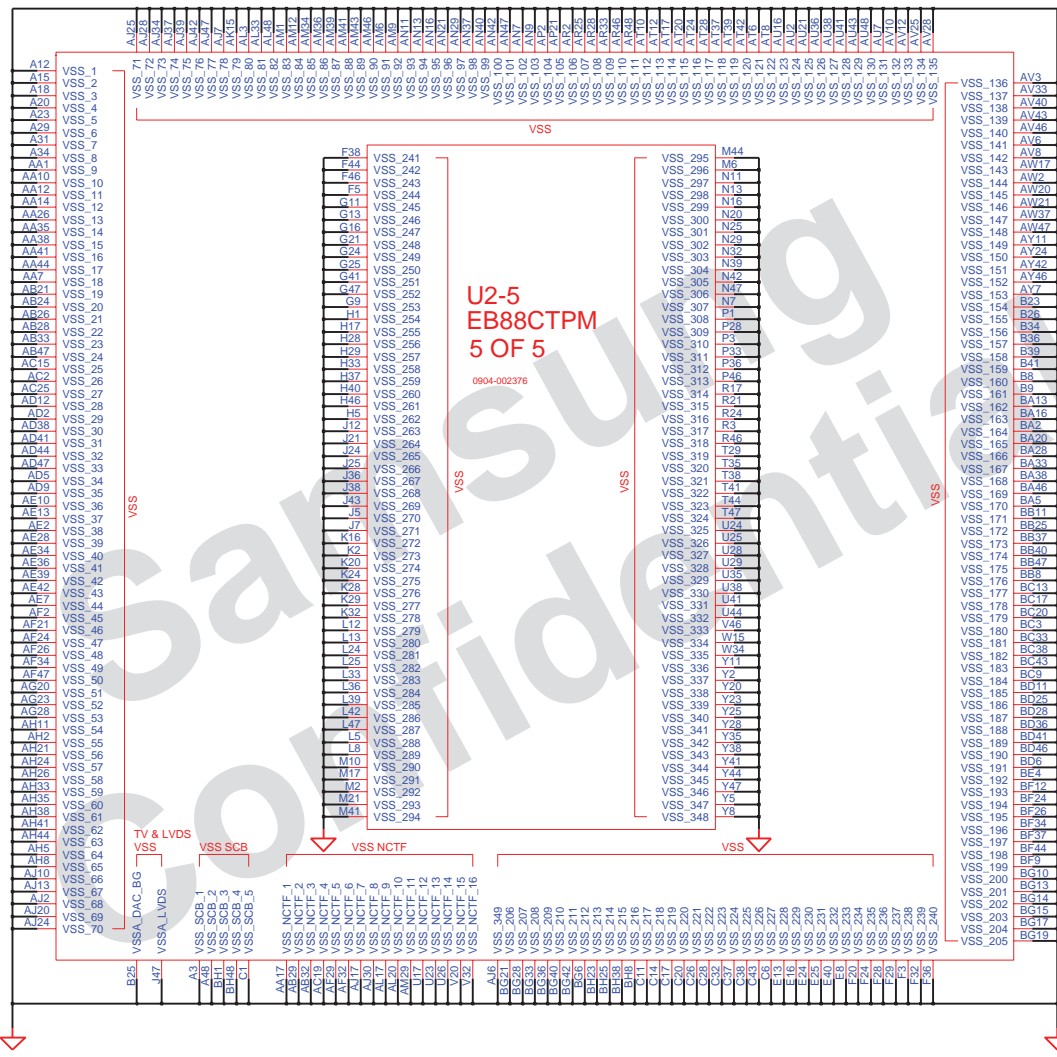
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U2-4
EB88CTPM
4 OF 5
0904-002376

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MCH_CANTIGA_GM_DDR2	PART NO.	
APPROVAL	HJ KIM	REV	1.0	CANTIGA (3/5)	August 07, 2009 15:14:35 PM	PAGE 15 OF 55
MODULE CODE		LAST EDIT				

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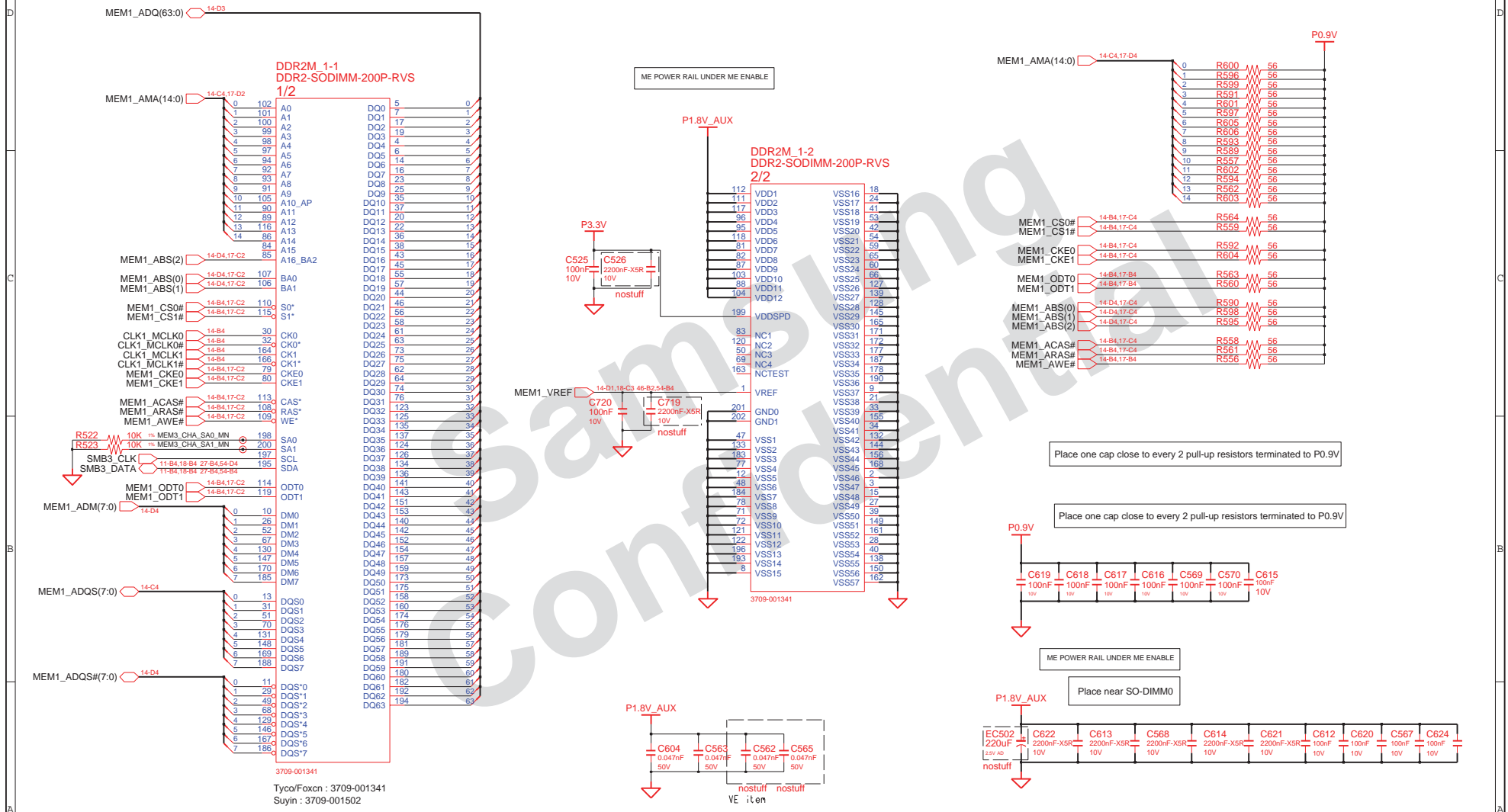
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MCH_CANTIGA_GM_DDR2	PART NO.	
APPROVAL	HJ KIM	REV	1.0	CANTIGA (4/5)	BA41-	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE	16 OF 55

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DDR SO-DIMM #0

Height : 5.2mm (Reverse)



Place one cap close to every 2 pull-up resistors terminated to P0.9V

Place one cap close to every 2 pull-up resistors terminated to P0.9V

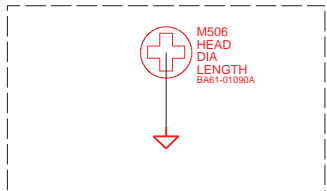
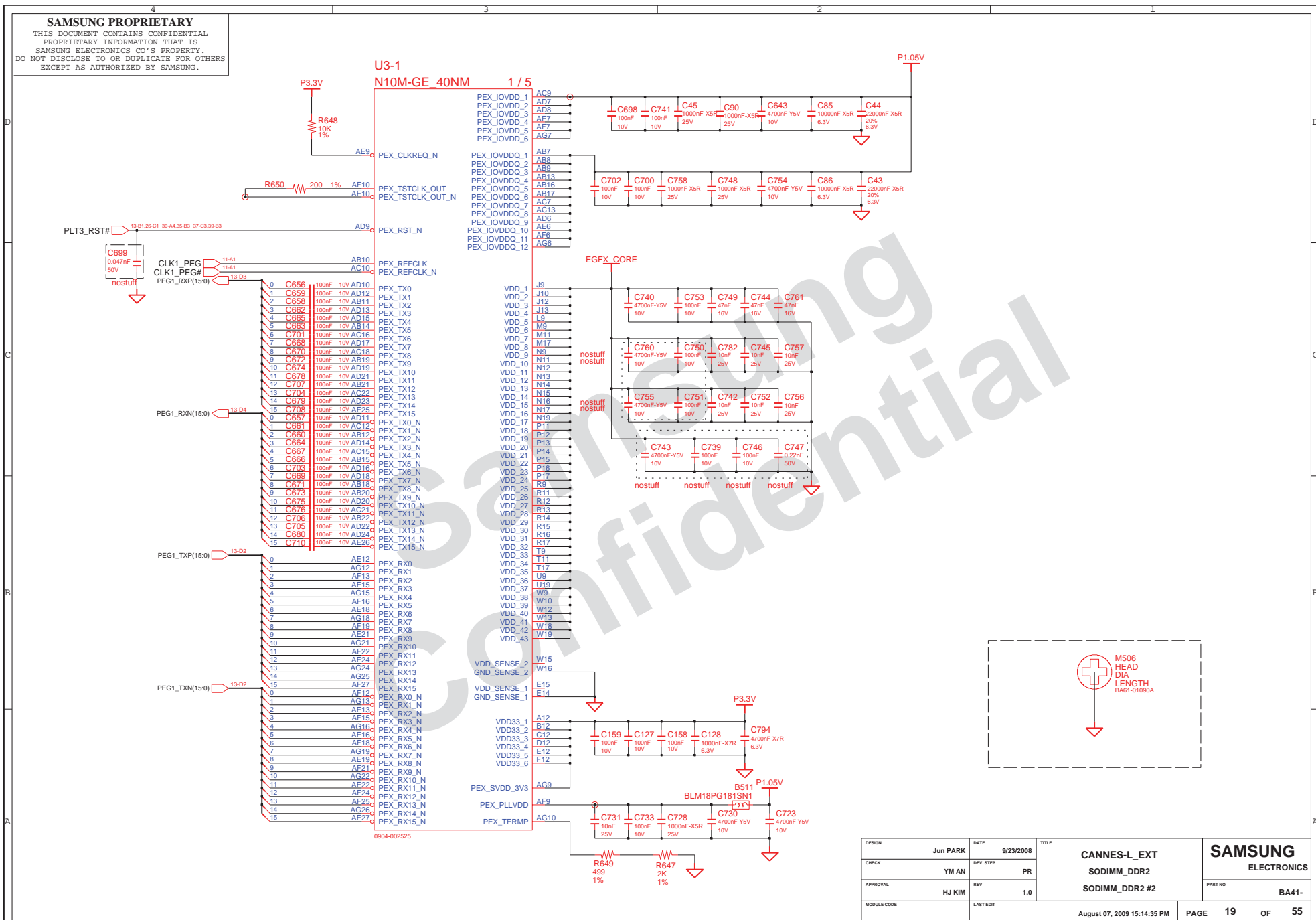
Place near SO-DIMMO

TycoFoxen : 3709-001341
Suyin : 3709-001502

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		MCH_CANTIGA_GM_DDR2	
APPROVAL	HJ KIM	REV	1.0		CANTIGA (5/5)	PART NO. BA41-
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 17 OF 55

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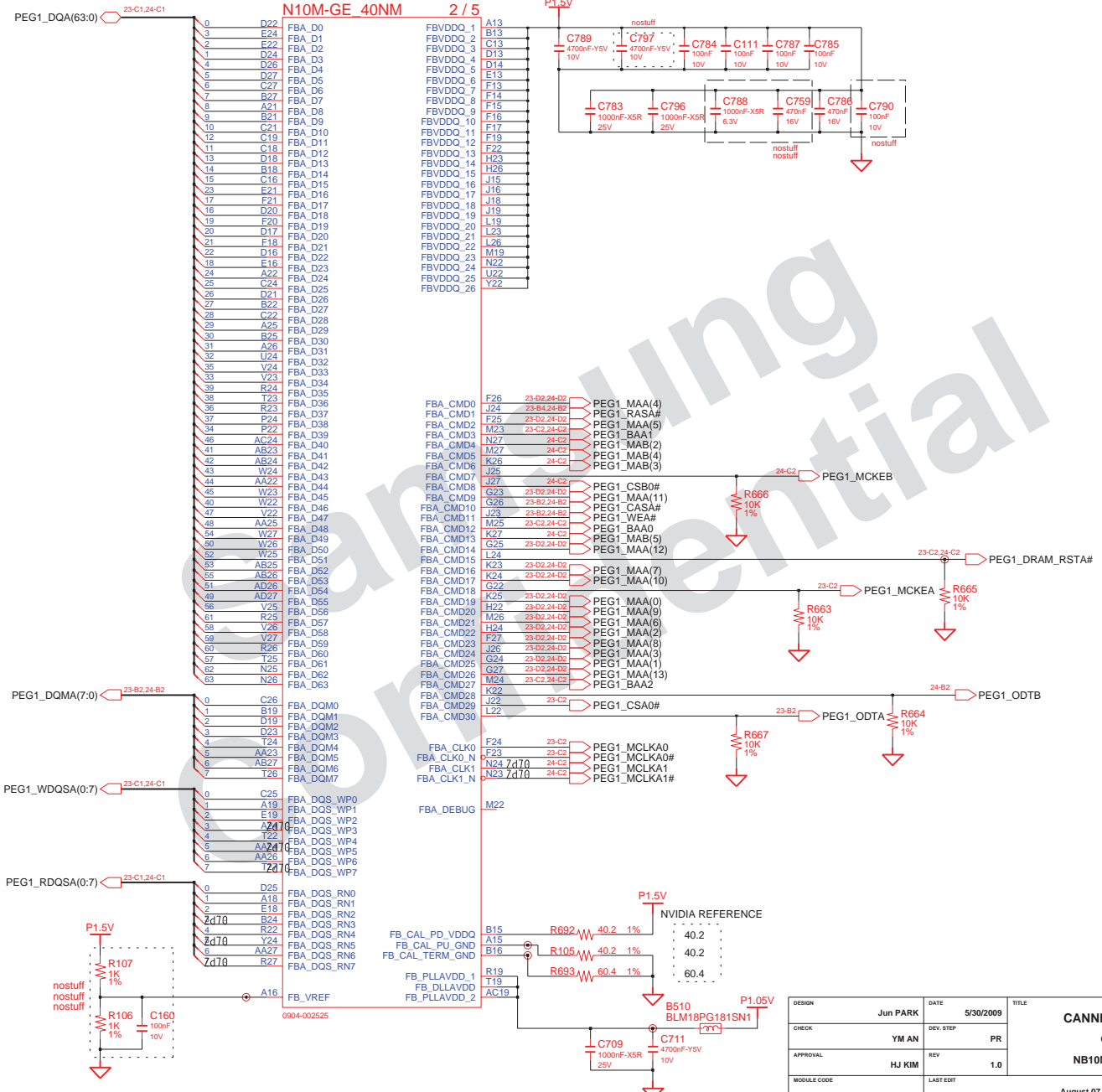
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DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR		SODIMM_DDR2	
APPROVAL	HJ KIM	REV	1.0		SODIMM_DDR2 #2	
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE	19 OF 55

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U3-2
N10M-GE 40NM
2 / 5

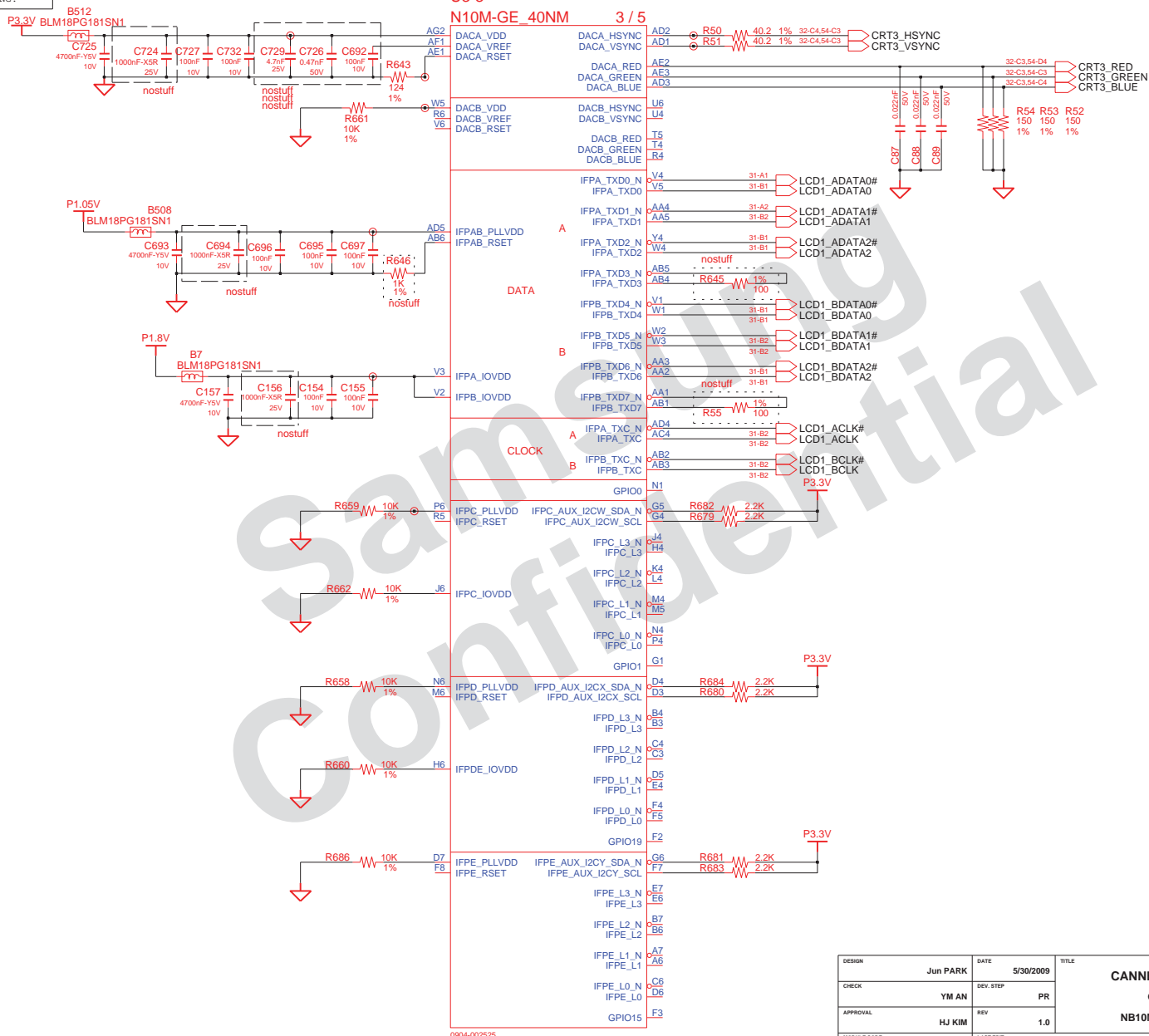


DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		GFY	
APPROVAL	HJ KIM	REV	1.0		NB10M-LP (1/4)	
MODULE CODE		LAST EDIT				
					August 07, 2009 15:14:35 PM	PAGE 20 OF 55

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**U3-3
N10M-GE 40NM 3 / 5**



DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT GFX	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR			
APPROVAL	HJ KIM	REV	1.0		NB10M-LP (2/4)	PART NO. BA41-
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 21 OF 55

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Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCD0_BL_PWM	High
GPIO(3)	LCD0_VDD	High
GPIO(4)	LCD0_BL_EN	High
GPIO(5)	GPU VID0	00 0.8V
GPIO(6)	GPU VID1	10 0.85V
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

Resistor value	PU to VDD	PD to GND	XCLK417 = 0.27MHz
5K ohm	1000	0000	RAM CFG (SEC)
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit
15K ohm	1010	0010	USER[3:0]=1111 for EDID
20K ohm	1011	0011	PADCFG[3:0]=0110 for NB
25K ohm	1100	0100	N10M-GS:0x0A74
30K ohm	1101	0101	N10M-GE:0x0A68
35K ohm	1110	0110	N10M-LP:0x0A69
45K ohm	1111	0111	N10M-NS:0x0A6C
			N10M-NE:0x0A6A
			N10M-GLM:0x0A7C

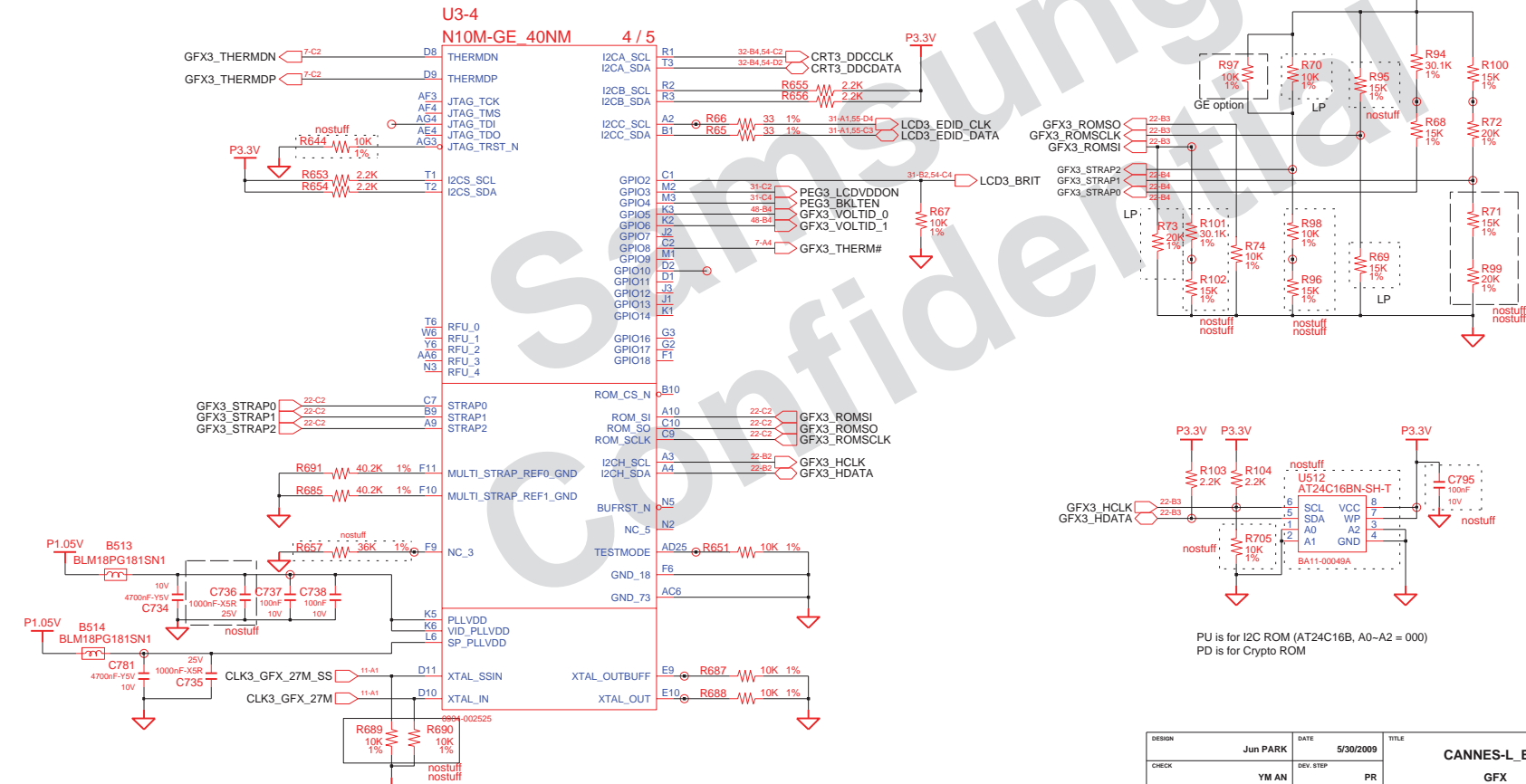
	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	GFX TPYE
SI	0	1	1	1	1Gb

Strap2	1	0	0	1	N10M-LP	DEVICE ID
Strap1	1	0	0	0	N10M-GE	
Strap0	1	1	1	0	For NB	
	1	1	1	1	EDID_EN	

U3-5
N10M-GE_40NM

5 / 5

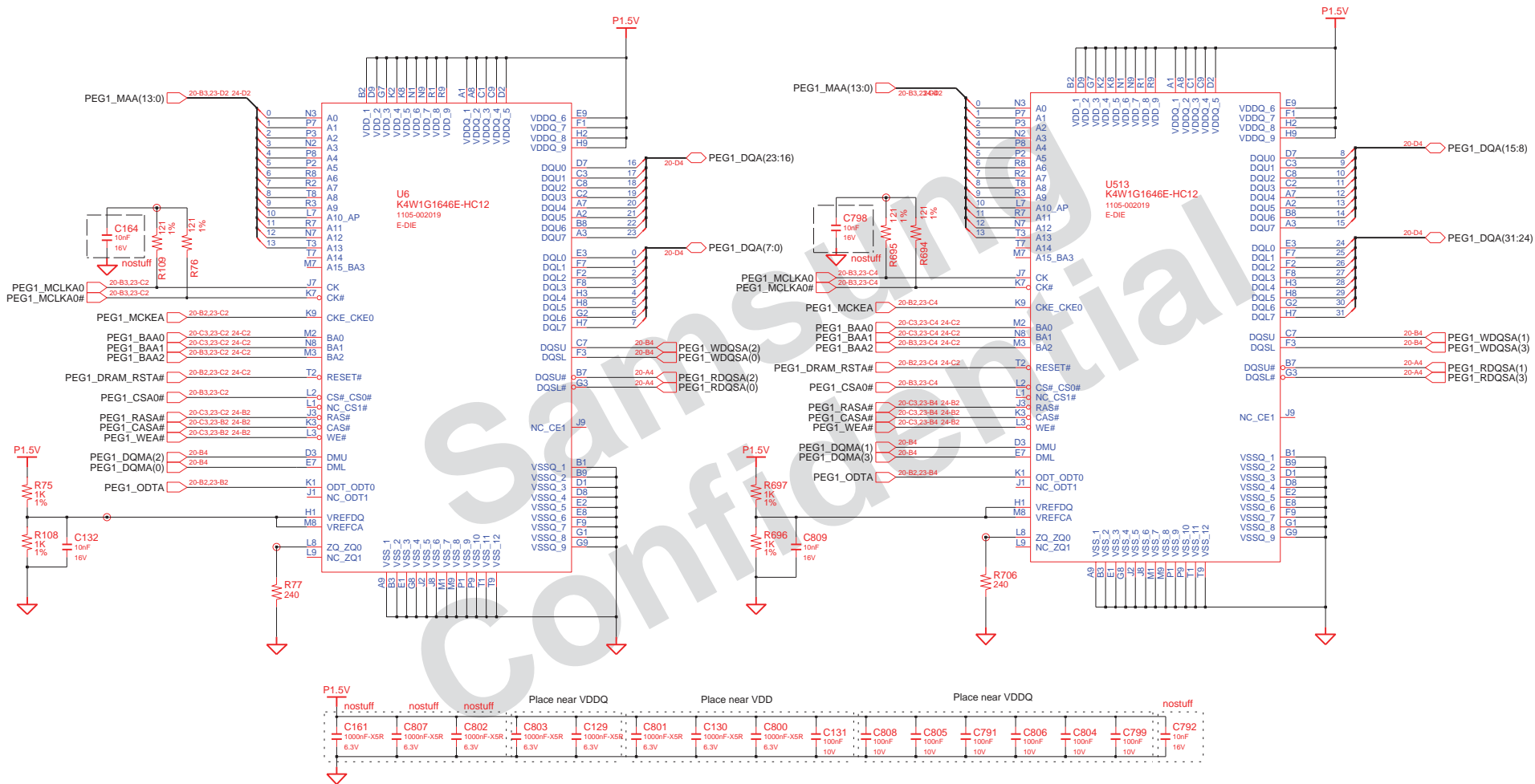
- B3 GND_1
- B5 GND_2
- B8 GND_3
- B11 GND_4
- B14 GND_5
- B17 GND_6
- B20 GND_7
- B23 GND_8
- B26 GND_9
- E2 GND_10
- E5 GND_11
- E23 GND_12
- E26 GND_13
- H2 GND_14
- H5 GND_15
- J11 GND_16
- J14 GND_17
- J17 GND_18
- K9 GND_19
- K15 GND_20
- L2 GND_21
- L5 GND_22
- L11 GND_23
- L12 GND_24
- L13 GND_25
- L14 GND_26
- L15 GND_27
- L16 GND_28
- L17 GND_29
- M12 GND_30
- M13 GND_31
- M14 GND_32
- M15 GND_33
- M16 GND_34
- P2 GND_35
- P5 GND_36
- P9 GND_37
- P18 GND_38
- P23 GND_39
- P26 GND_40
- P28 GND_41
- P33 GND_42
- P38 GND_43
- P44 GND_44
- P45 GND_45
- T12 GND_46
- T13 GND_47
- T14 GND_48
- T15 GND_49
- T16 GND_50
- U2 GND_51
- U11 GND_52
- U12 GND_53
- U13 GND_54
- U14 GND_55
- U15 GND_56
- U16 GND_57
- U17 GND_58
- U23 GND_59
- U26 GND_60
- V9 GND_61
- V19 GND_62
- W11 GND_63
- W14 GND_64
- W17 GND_65
- Y2 GND_66
- Y5 GND_67
- Y26 GND_68
- Y28 GND_69
- Y29 GND_70
- AC2 GND_71
- AC5 GND_72
- AC8 GND_73
- AC11 GND_74
- AC14 GND_75
- AC17 GND_76
- AC20 GND_77
- AC23 GND_78
- AC26 GND_79
- AF2 GND_80
- AF5 GND_81
- AF8 GND_82
- AF12 GND_83
- AF14 GND_84
- AF17 GND_85
- AF20 GND_86
- AF23 GND_87
- AF26 GND_88
- GND_89



DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT
CHECK	YM AN	DEV. STEP	PR	GFX	
APPROVAL	HJ KIM	REV	1.0	NB10M-LP (3/4)	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 22 OF 55

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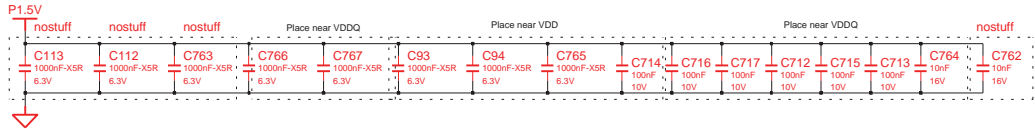
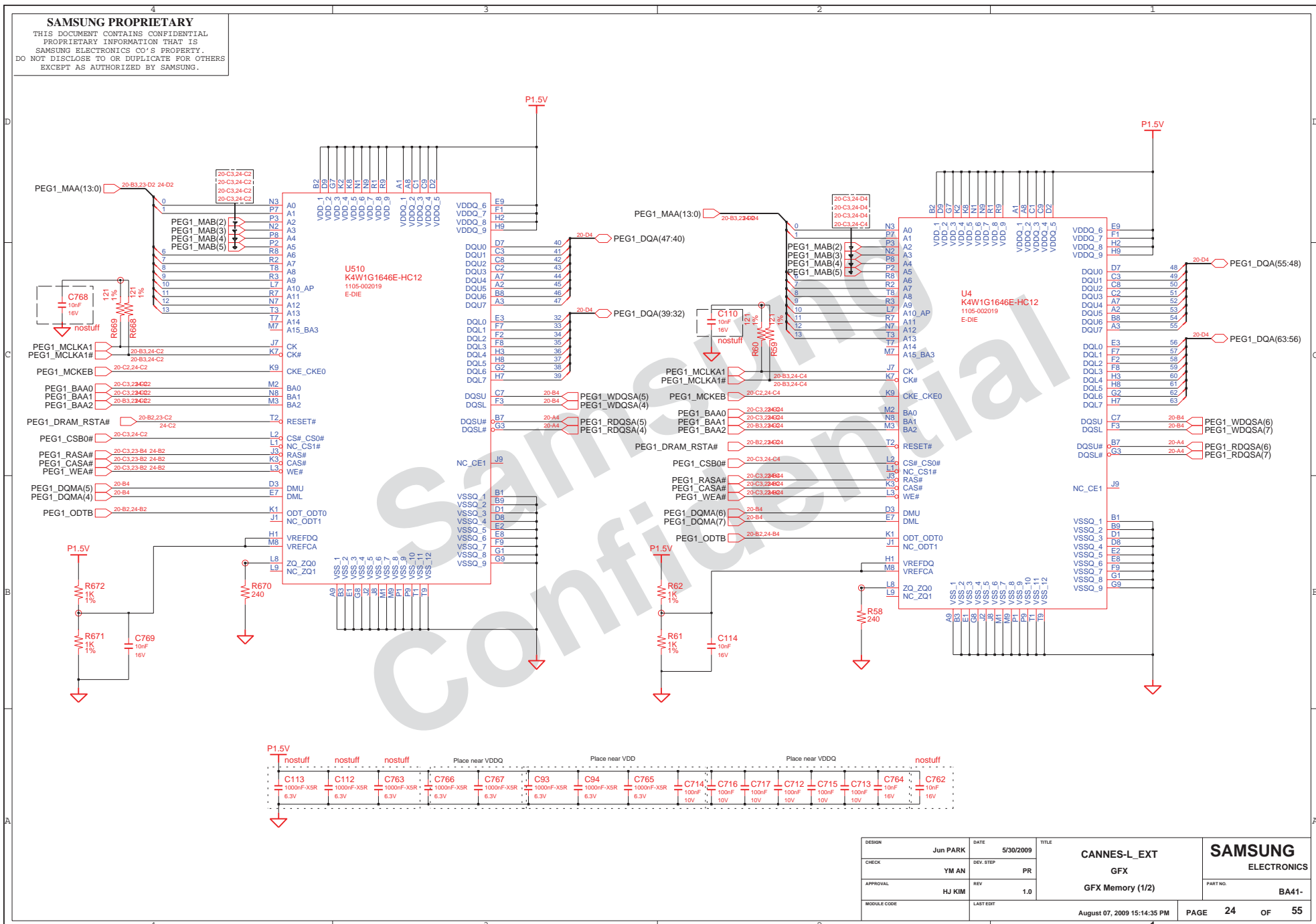
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DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		GFY	
APPROVAL	HJ KIM	REV	1.0		NB10M-LP (4/4)	PART NO. BA41-
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 23 OF 55

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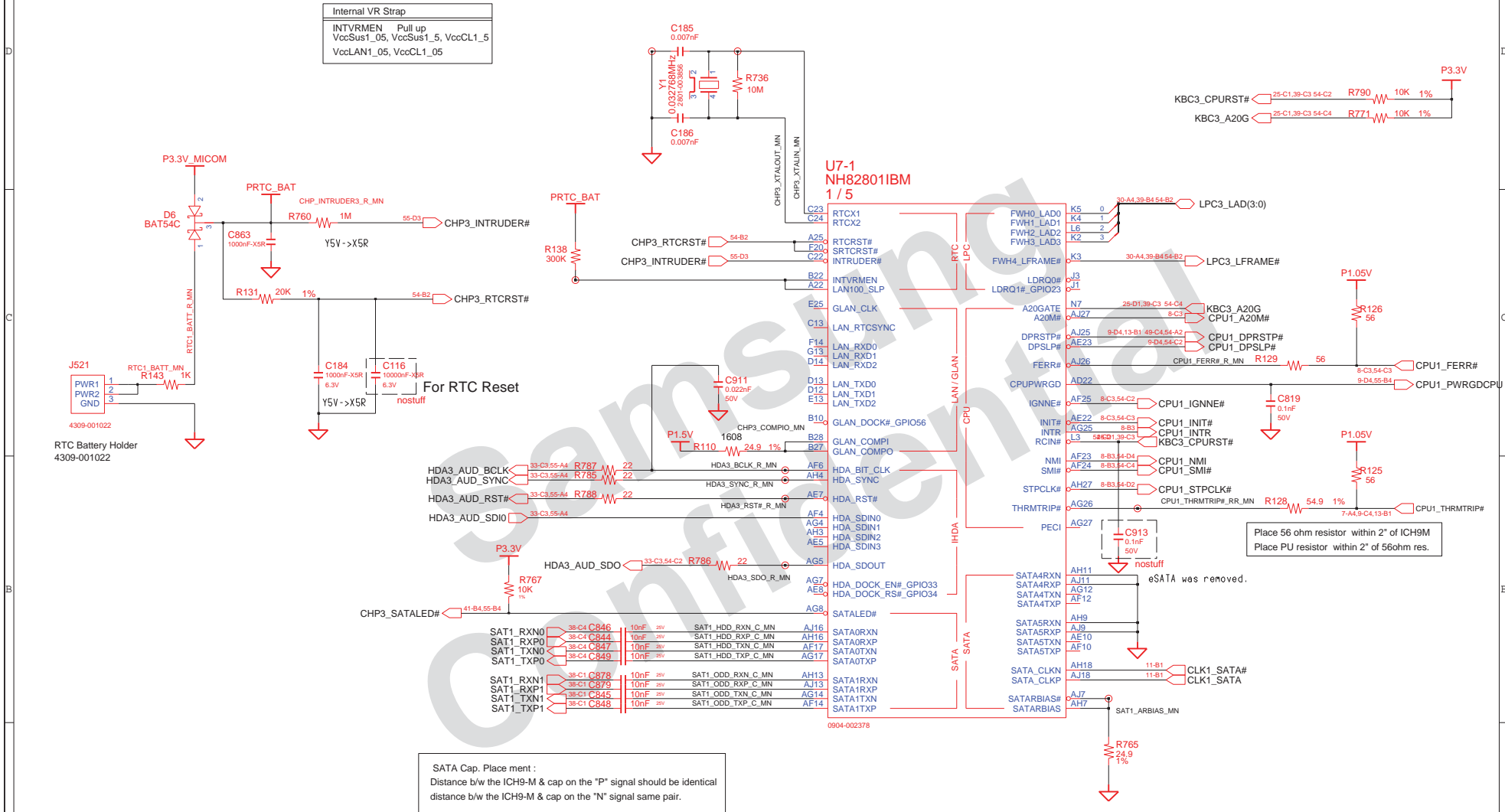


DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR		GFX	
APPROVAL	HJ KIM	REV	1.0		GFX Memory (1/2)	PART NO. BA41-
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 24 OF 55

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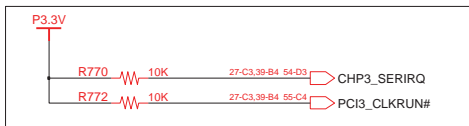
Internal VR Strap	
INTVRMEN	Pull up
VccSus1_05, VccSus1_5, VccCL1_5	
VccLAN1_05, VccCL1_05	



DRAW	DATE	TITLE	SAMSUNG ELECTRONICS	
Jun PARK	5/30/2009	CANNES-L_EXT GFX	PART NO. BA41-	
Y.M AN	DEV. STEP PR	GFX Memory (2/2)	August 07, 2009 15:14:35 PM	
HJ KIM	REV 1.0		PAGE 25	OF 55
MODULE CODE	LAST EDIT			

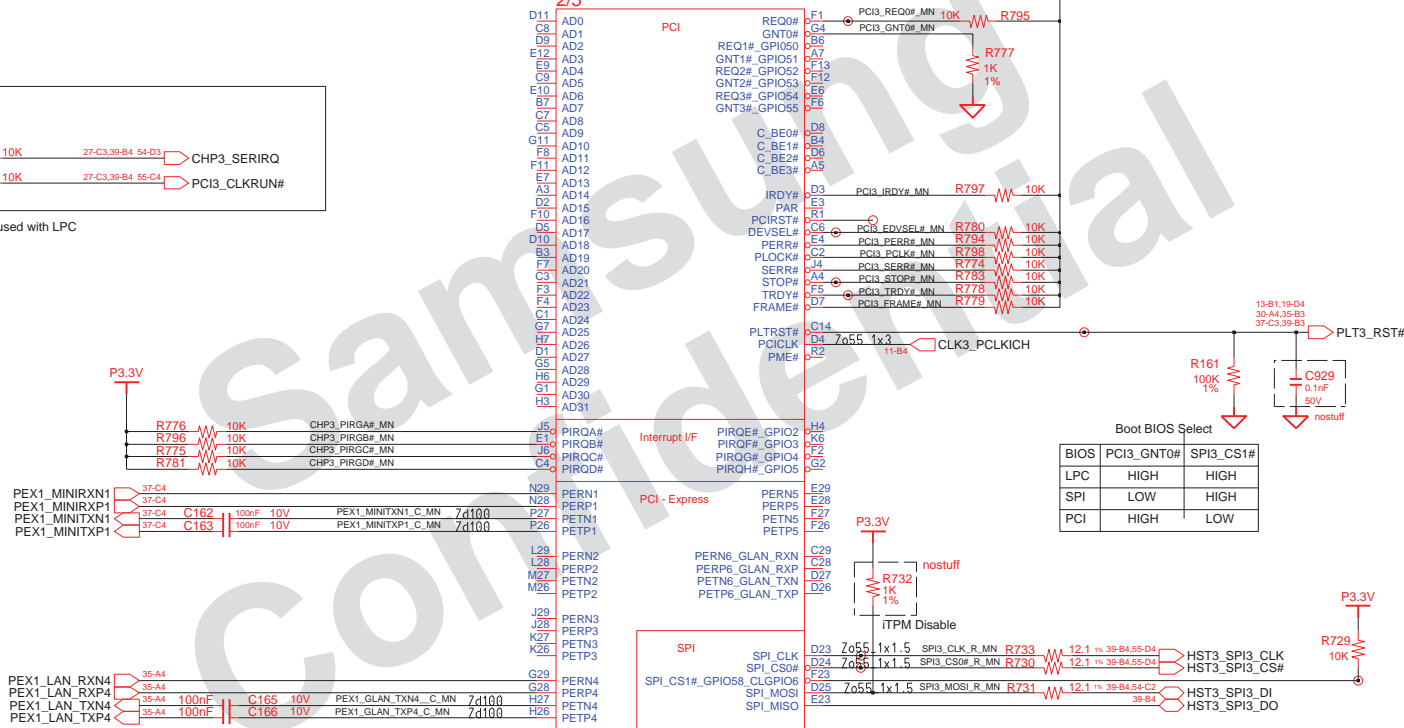
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LPC option ; These are used with LPC

**U7-2
NH82801IBM
2/5**

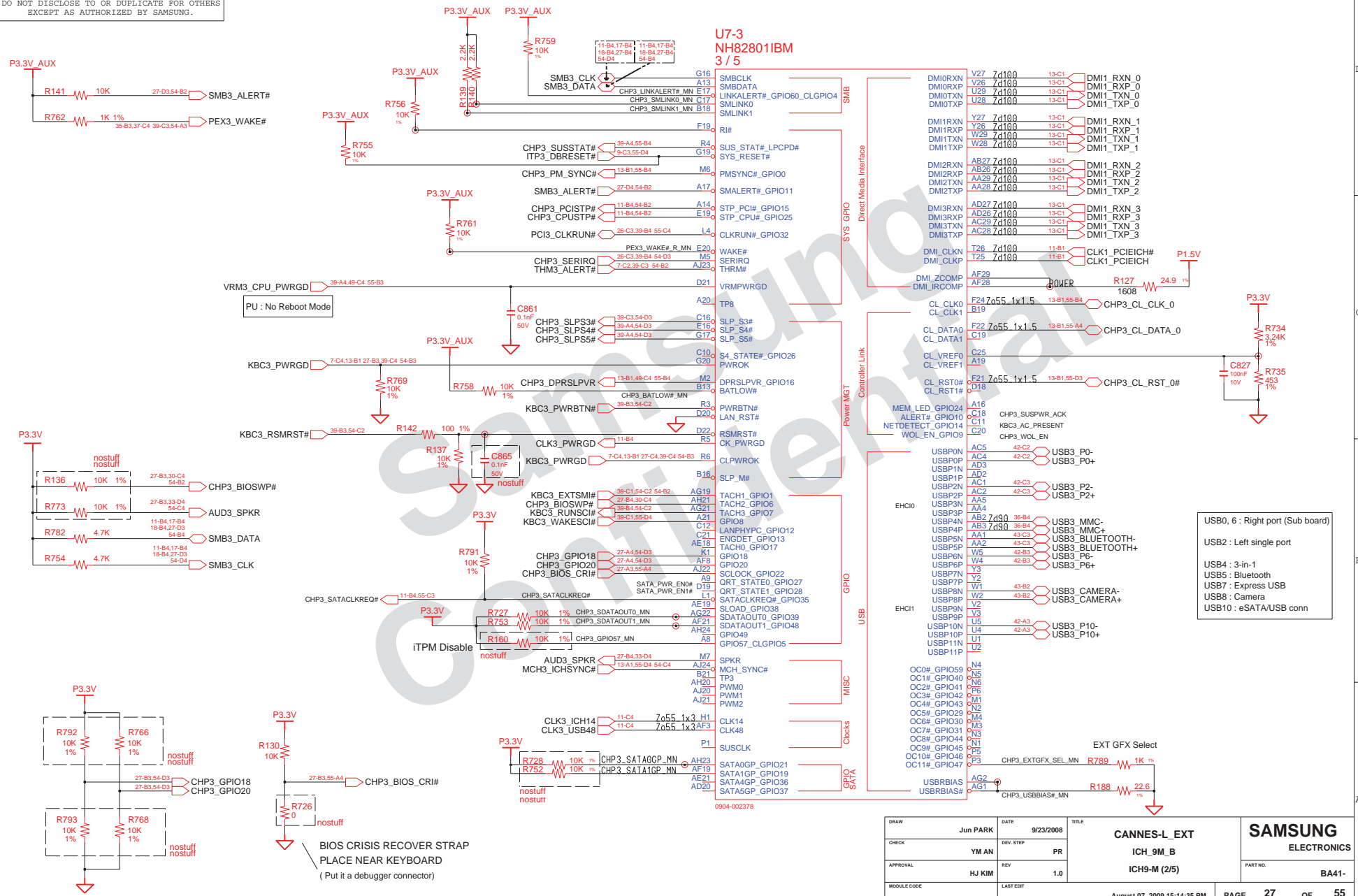


AC caps : PCIe need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		ICH_9M_B	
APPROVAL	HJ KIM	REV	1.0		ICH9-M (1/5)	PART NO. BA41-
MODULE CODE	undefined	LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 26 OF 55

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USB0, 6 : Right port (Sub board)
 USB2 : Left single port
 USB4 : 3-in-1
 USB5 : Bluetooth
 USB7 : Express USB
 USB8 : Camera
 USB10 : eSATA/USB conn

BIOS CRISIS RECOVER STRAP
 PLACE NEAR KEYBOARD
 (Put it a debugger connector)

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR		ICH9_M_B	
APPROVAL	HJ KIM	REV	1.0		ICH9-M (2/5)	
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE	27 OF 55

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AA26	VSS_001	H29	VSS_106	H5	VSS_133	N14
AA27	VSS_002	H6	VSS_107	H6	VSS_134	N15
AA3	VSS_003	J23	VSS_108	J23	VSS_135	N16
AA6	VSS_004	K29	VSS_109	K29	VSS_136	N17
AB1	VSS_005	L22	VSS_110	L22	VSS_137	N18
AA23	VSS_006	M22	VSS_111	M22	VSS_138	N26
AB28	VSS_007	N29	VSS_112	N29	VSS_139	N27
AB29	VSS_008	O28	VSS_113	O28	VSS_140	P12
AB4	VSS_009	P28	VSS_114	P28	VSS_141	P13
AB5	VSS_010	Q28	VSS_115	Q28	VSS_142	P14
AC17	VSS_011	R28	VSS_116	R28	VSS_143	P15
AC26	VSS_012	S28	VSS_117	S28	VSS_144	P16
AC27	VSS_013	T28	VSS_118	T28	VSS_145	P17
AC3	VSS_014	U28	VSS_119	U28	VSS_146	P2
AD1	VSS_015	V28	VSS_120	V28	VSS_147	P28
AD10	VSS_016	W28	VSS_121	W28	VSS_148	P29
AD12	VSS_017	X28	VSS_122	X28	VSS_149	P4
AD13	VSS_018	Y28	VSS_123	Y28	VSS_151	R11
AD14	VSS_019	Z28	VSS_124	Z28	VSS_152	R12
AD17	VSS_020	AA29	VSS_125	AA29	VSS_153	R13
AD18	VSS_021	AB29	VSS_126	AB29	VSS_154	R14
AD21	VSS_022	AC29	VSS_127	AC29	VSS_155	R15
AD28	VSS_023	AD29	VSS_128	AD29	VSS_156	R16
AD29	VSS_024	AE29	VSS_129	AE29	VSS_157	R17
AD4	VSS_025	AF29	VSS_130	AF29	VSS_158	R18
AD5	VSS_026	AG29	VSS_131	AG29	VSS_160	R28
AD6	VSS_027	AH29	VSS_132	AH29	VSS_161	T12
AD7	VSS_028	AI29	VSS_133	AI29	VSS_162	T13
AD9	VSS_029	AJ29	VSS_134	AJ29	VSS_163	T14
AE12	VSS_030	AK29	VSS_135	AK29	VSS_164	T15
AE13	VSS_031	AL29	VSS_136	AL29	VSS_165	T16
AE14	VSS_032	AM29	VSS_137	AM29	VSS_166	T23
AE16	VSS_033	AN29	VSS_138	AN29	VSS_167	T26
AE17	VSS_034	AO29	VSS_139	AO29	VSS_168	B26
AE2	VSS_035	AP29	VSS_140	AP29	VSS_169	U12
AE20	VSS_036	AQ29	VSS_141	AQ29	VSS_170	U13
AE24	VSS_037	AR29	VSS_142	AR29	VSS_171	U14
AE3	VSS_038	AS29	VSS_143	AS29	VSS_172	U15
AE4	VSS_039	AT29	VSS_144	AT29	VSS_173	U16
AE6	VSS_040	AV29	VSS_145	AV29	VSS_174	U17
AE9	VSS_041	AW29	VSS_146	AW29	VSS_175	AD23
AF13	VSS_042	AX29	VSS_147	AX29	VSS_176	U26
AF16	VSS_043	AY29	VSS_148	AY29	VSS_177	U27
AF18	VSS_044	AZ29	VSS_149	AZ29	VSS_178	U3
AF22	VSS_045	BA30	VSS_150	BA30	VSS_179	V1
AH26	VSS_046	BB30	VSS_151	BB30	VSS_179	V13
AF26	VSS_047	BC30	VSS_152	BC30	VSS_180	V15
AF27	VSS_048	BD30	VSS_153	BD30	VSS_181	V23
AF5	VSS_049	BE30	VSS_154	BE30	VSS_182	V26
AF7	VSS_050	BF30	VSS_155	BF30	VSS_183	V28
AF9	VSS_051	BG30	VSS_156	BG30	VSS_184	V4
AG13	VSS_052	BH30	VSS_157	BH30	VSS_185	V5
AG16	VSS_053	BI30	VSS_158	BI30	VSS_186	W26
AG18	VSS_054	BJ30	VSS_159	BJ30	VSS_187	W27
AG20	VSS_055	BK30	VSS_160	BK30	VSS_188	W3
AG23	VSS_056	BL30	VSS_161	BL30	VSS_189	Y1
AG3	VSS_057	BM30	VSS_162	BM30	VSS_190	Y2
AG6	VSS_058	BN30	VSS_163	BN30	VSS_191	Y29
AG9	VSS_059	BO30	VSS_164	BO30	VSS_192	Y4
AH12	VSS_060	BP30	VSS_165	BP30	VSS_193	Y5
AH14	VSS_061	BQ30	VSS_166	BQ30	VSS_194	AG28
AH17	VSS_062	BR30	VSS_167	BR30	VSS_195	AH6
AH19	VSS_063	BS30	VSS_168	BS30	VSS_196	AF2
AH2	VSS_064	BT30	VSS_169	BT30	VSS_197	B25
AH22	VSS_065	BV30	VSS_170	BV30	VSS_198	
AH25	VSS_066	BW30	VSS_171	BW30	VSS_NCTF_01	A1
AH28	VSS_067	BX30	VSS_172	BX30	VSS_NCTF_02	A2
AH5	VSS_068	BY30	VSS_173	BY30	VSS_NCTF_03	A28
AH8	VSS_069	BZ30	VSS_174	BZ30	VSS_NCTF_04	A29
AJ12	VSS_070	CA31	VSS_175	CA31	VSS_NCTF_05	AH1
AJ14	VSS_071	CB31	VSS_176	CA31	VSS_NCTF_06	AH29
AJ17	VSS_072	CC31	VSS_177	CB31	VSS_NCTF_07	AJ1
AJ8	VSS_073	CD31	VSS_178	CD31	VSS_NCTF_08	AJ2
B11	VSS_074	CE31	VSS_179	CE31	VSS_NCTF_09	AJ28
B14	VSS_075	CF31	VSS_180	CF31	VSS_NCTF_10	AJ29
B17	VSS_076	CG31	VSS_181	CG31	VSS_NCTF_11	B1
B2	VSS_077	CH31	VSS_182	CH31	VSS_NCTF_12	B29
B17	VSS_078	CI31	VSS_183	CI31		
B20	VSS_079	CK31	VSS_184	CK31		
	VSS_080	CL31	VSS_185	CL31		
	VSS_081	CM31	VSS_186	CM31		
	VSS_082	CN31	VSS_187	CN31		
	VSS_083	CO31	VSS_188	CO31		
	VSS_084	CP31	VSS_189	CP31		
	VSS_085	CQ31	VSS_190	CQ31		
	VSS_086	CR31	VSS_191	CR31		
	VSS_087	CS31	VSS_192	CS31		
	VSS_088	CT31	VSS_193	CT31		
	VSS_089	CU31	VSS_194	CU31		
	VSS_090	CV31	VSS_195	CV31		
	VSS_091	CW31	VSS_196	CW31		
	VSS_092	CX31	VSS_197	CX31		
	VSS_093	CY31	VSS_198	CY31		
	VSS_094	CA32	VSS_199	CA32		
	VSS_095	CB32	VSS_200	CB32		
	VSS_096	CC32	VSS_101	CC32		
	VSS_097	CD32	VSS_102	CD32		
	VSS_098	CE32	VSS_103	CE32		
	VSS_099	CF32	VSS_104	CF32		
	VSS_100	CG32	VSS_105	CG32		
	VSS_101	CH32				
	VSS_102	CI32				
	VSS_103	CK32				
	VSS_104	CL32				
	VSS_105	CM32				

GND

U7-5

NH82801IBM
5/5

0904-002378



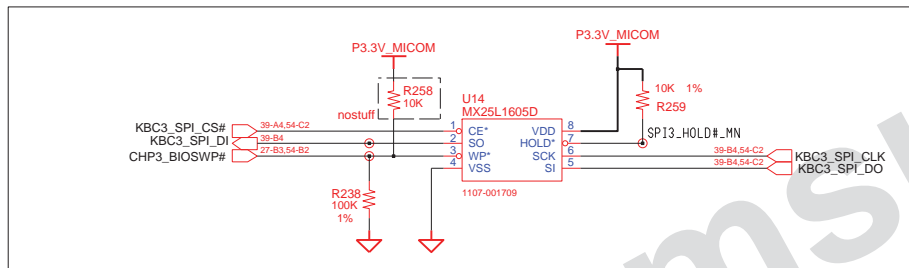
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CHECK	YM AN	DEV.STEP	PR		ICH_9M_B	
APPROVAL	HJ KIM	REV	1.0		ICH9-M (4/5)	PART NO. BA41-
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 29	OF 55

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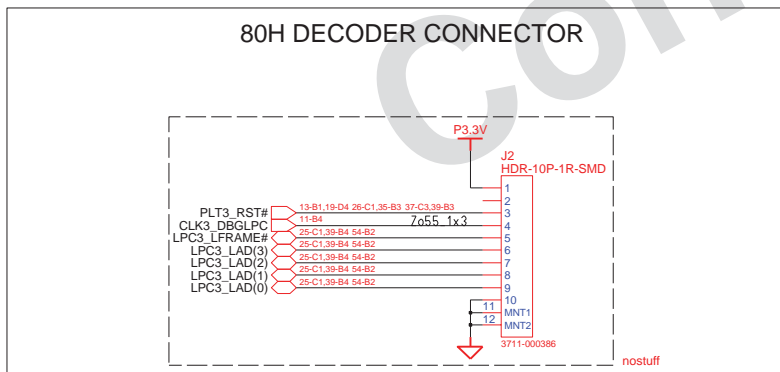
SPI_BIOS_ROM

16MBit



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	9E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
	WITH INITIAL POST VALUE	8A	INIT. EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	9A	SHADOW OPTION ROMS
18	8254 TIMER INIT	9C	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT.	9E	ENABLE H/W INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
32	COMPUTE THE CPU SPEED	B0	CHECK FOR ERRORS
34	TEST CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
38	SHADOW SYSTEM BIOS ROM	B4	ONE BEEP
3A	AUTO SIZING CACHE	B6	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B7	ACPI INIT
3D	LOAD ALTER REG. WITH CMOS VALUE	BA	DMI INIT
42	INIT. INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I20 SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	SHUTDOWN 5
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	89	ENABLE NMI
54	SET KEYCLICK IF ENABLED	90	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 2
5A	DISPLAY PRESS SETUP	94	DISABLE A20 ADDRESS LINE
5C	TEST RAM BETWEEN 812K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		

80H DECODER CONNECTOR



80port will be removed in MP stage.

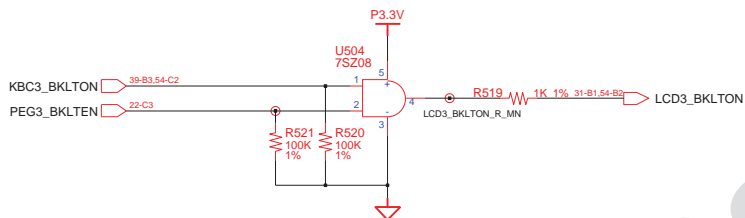
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	ICH9_M_B	PART NO.	
APPROVAL	HJ KIM	REV	1.0	ICH9-M (5/5)	BA41-	
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE	30 OF 55

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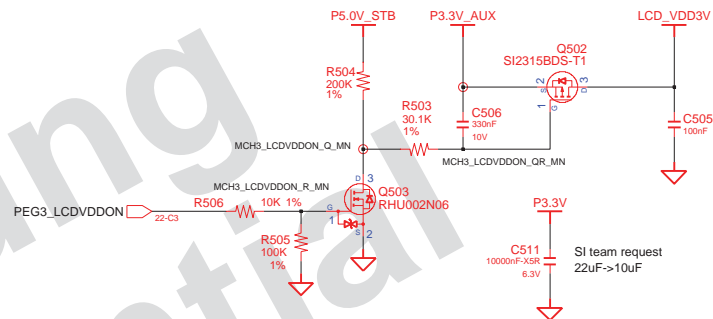
LVDS

Backlight On

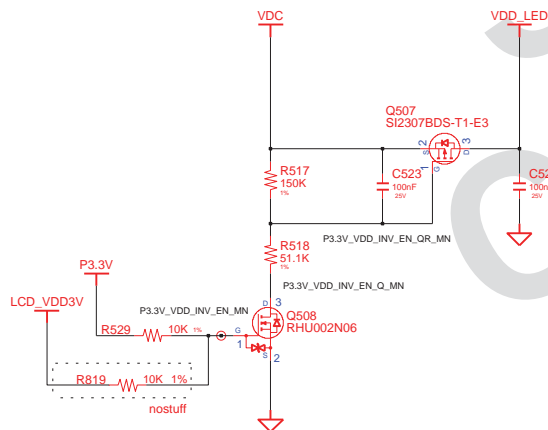


LCD Power

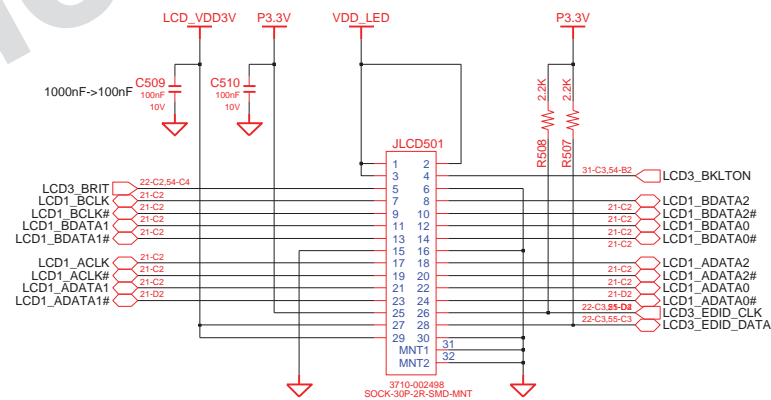
EBL Purpose



LED Power



2Ch. LCD Connector



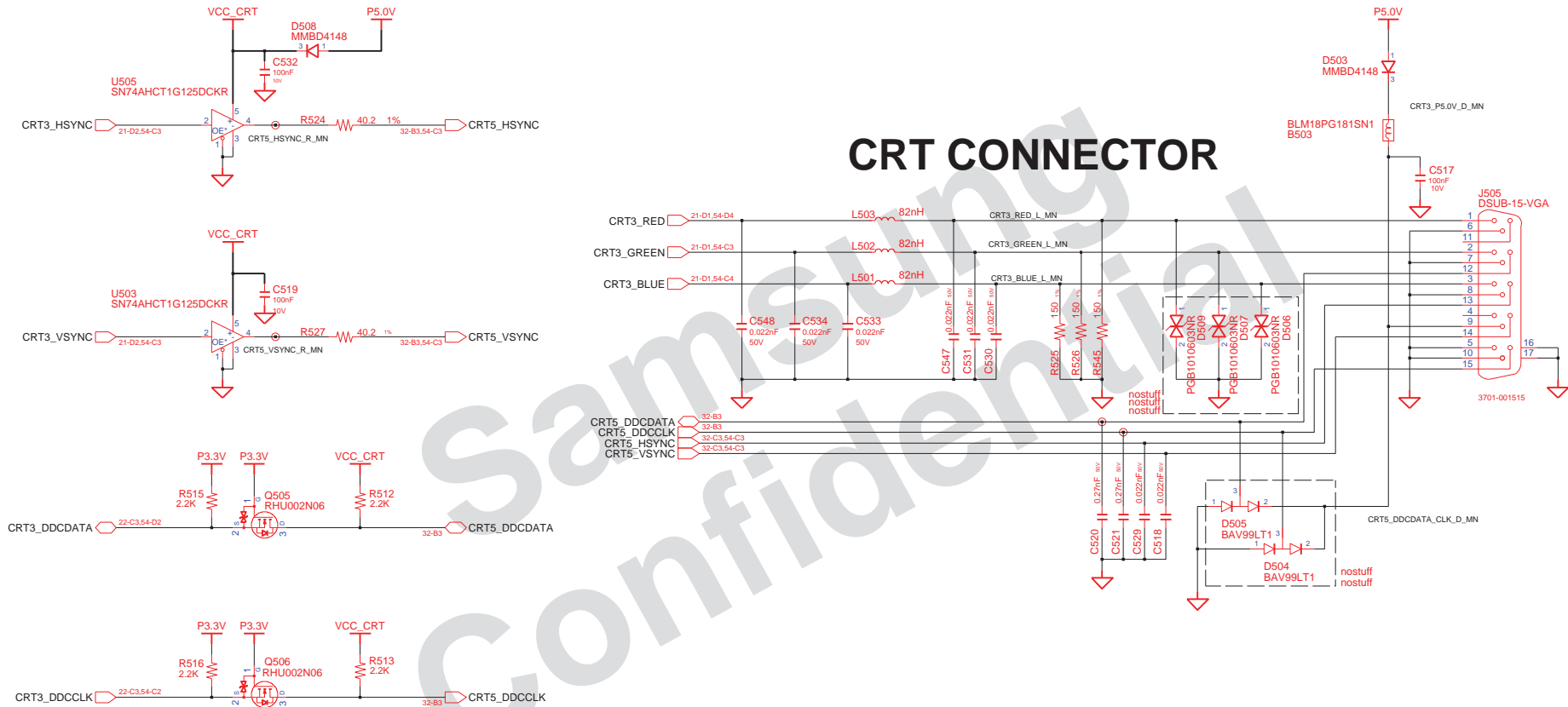
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR		SPI_BIOS_ROM	
APPROVAL	HJ KIM	REV	1.0		SPI_BIOS_ROM	PART NO.
MODULE CODE		LAST EDIT				BA41-
				August 07, 2009 15:14:35 PM	PAGE	31 OF 55

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CRT

CRT CONNECTOR



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

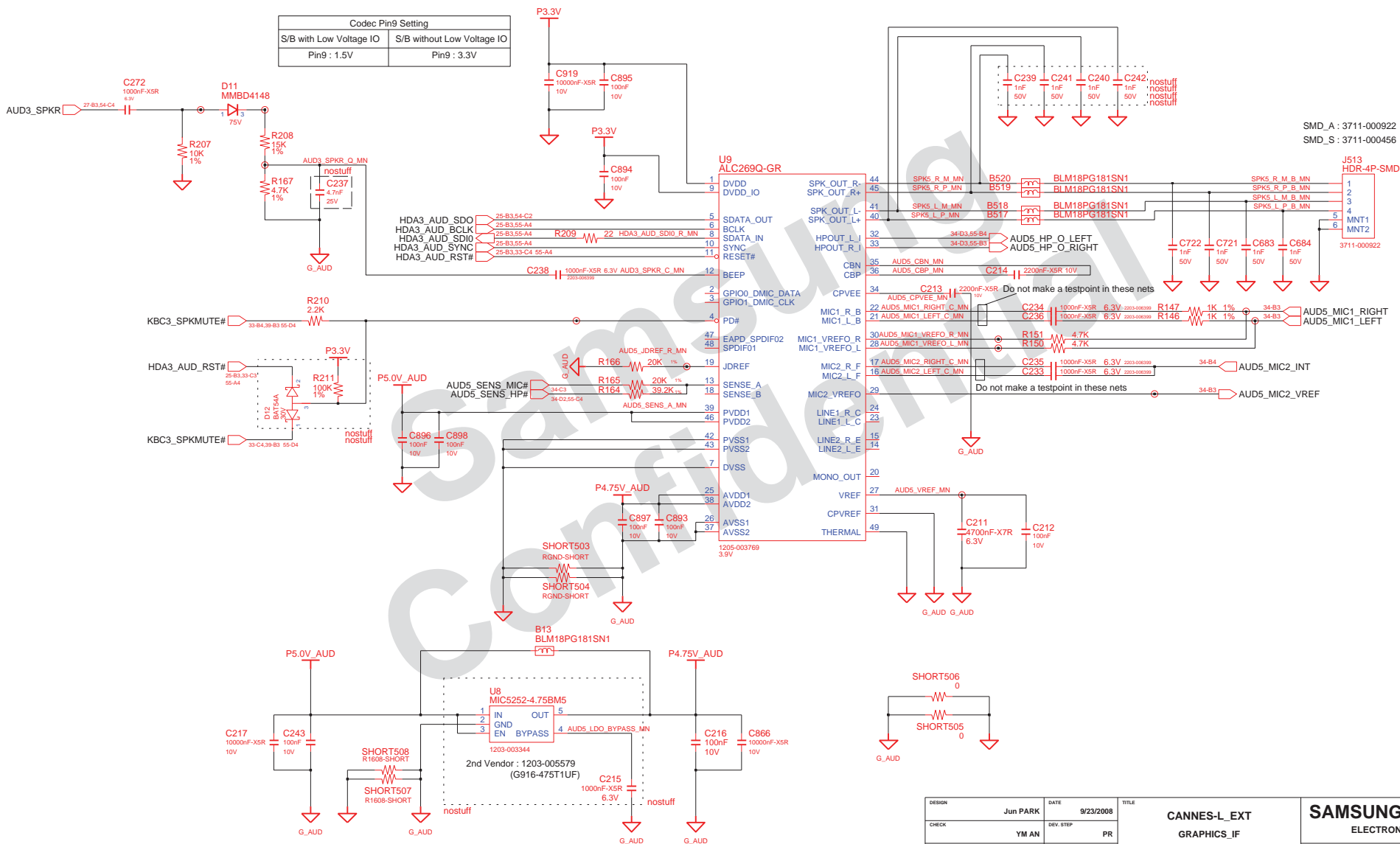
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR		GRAPHICS_IF	
APPROVAL	HJ KIM	REV	1.0		LVDS	PART NO. BA41-
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE	32 OF 55

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AUdio Codec (ALC269)

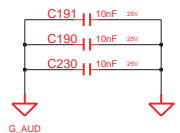
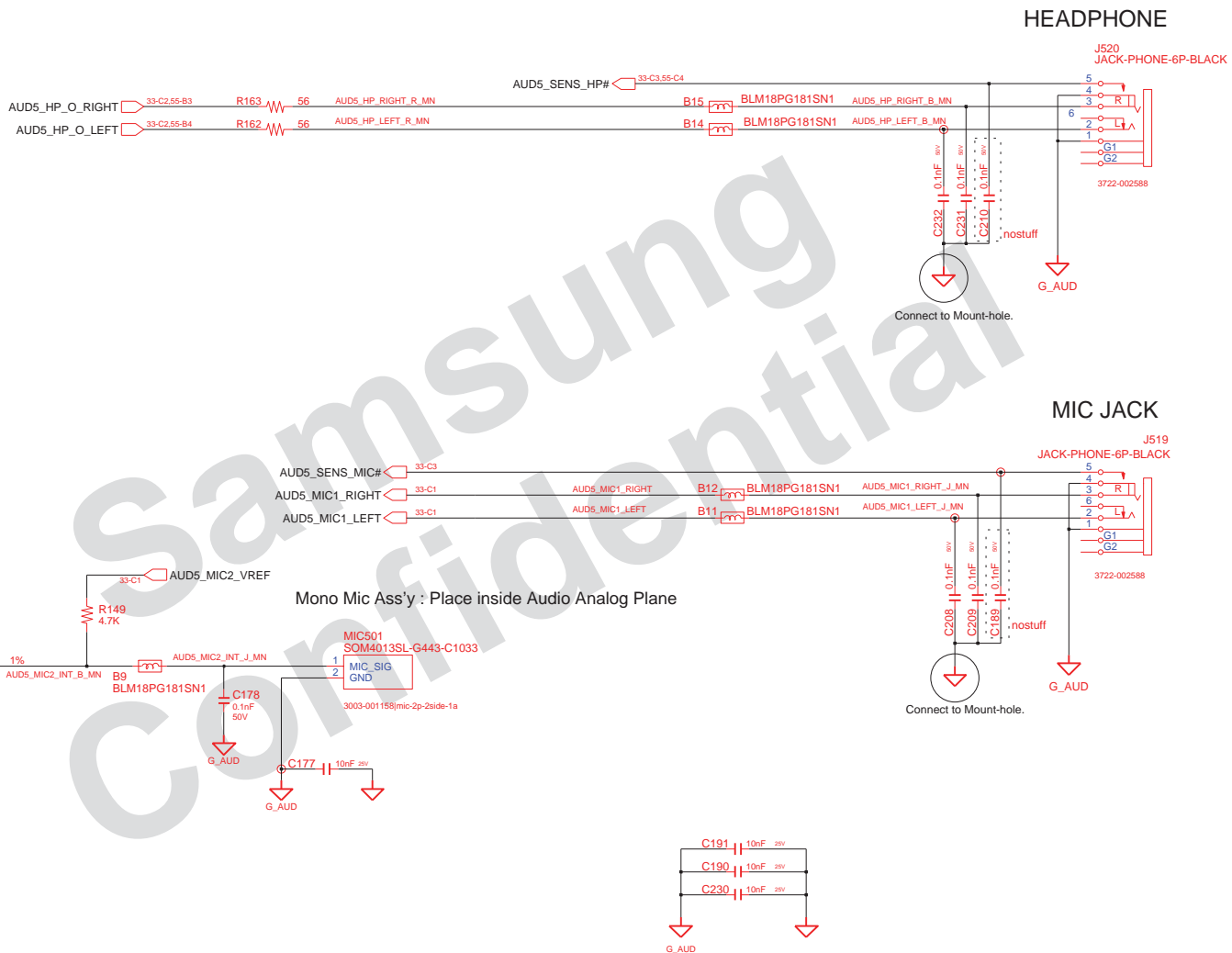
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	GRAPHICS_IF	PART NO.	
APPROVAL	HJ KIM	REV	1.0	CRT		
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 33 OF 55

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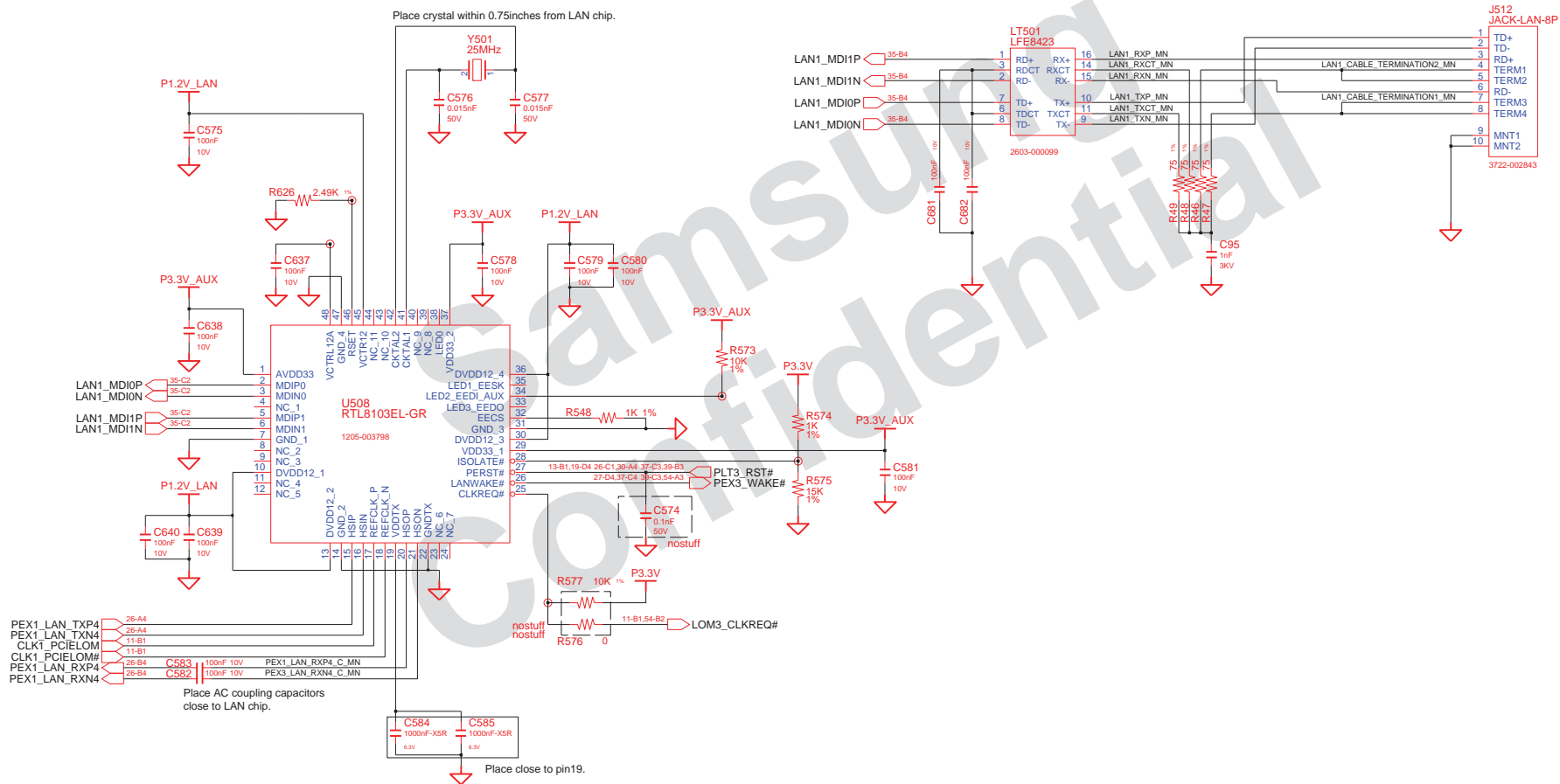


DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	HDA_CODEC	PART NO.	
APPROVAL	HJ KIM	REV	1.0	AUDIO CODEC ALC269_GR	BA41-	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 34 OF 55	

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LAN Controller (RTL8103EL)

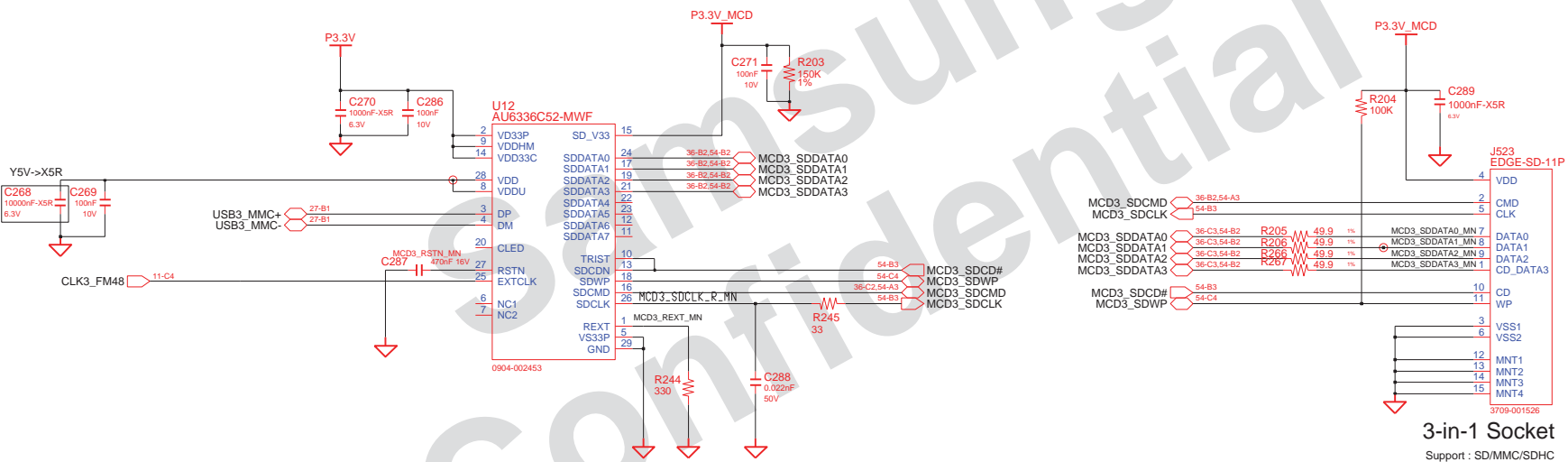


DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		HDA_CODEC	
APPROVAL	HJ KIM	REV	1.0		AUDIO INPUT/OUTPUT	PART NO.
MODULE CODE		LAST EDIT				BA41-
				August 07, 2009 15:14:35 PM	PAGE	35 OF 55

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3 IN 1 CARD (AU6336)



3-in-1 Socket
Support : SD/MMC/SDHC

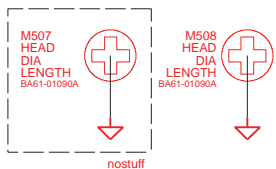
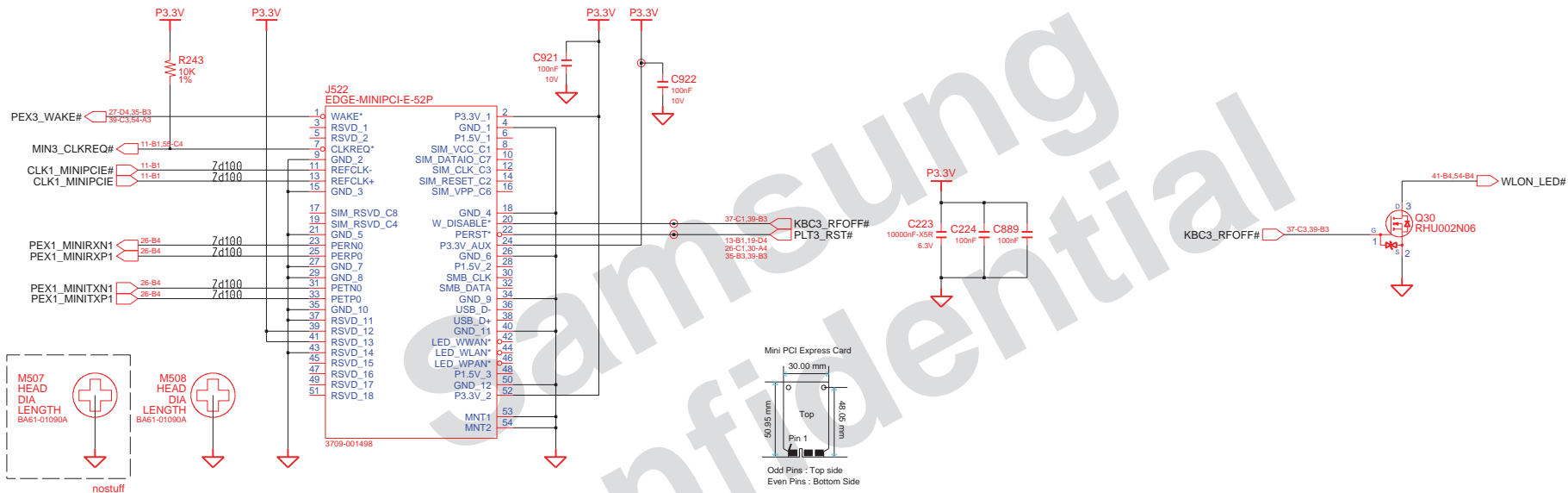
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV.STEP	PR		LAN	
APPROVAL	HJ KIM	REV	1.0		LAN_MARVELL_8057	
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 36 OF 55

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Wireless LAN

WLAN, 4mm



PEM : WLAN minicard + Half minicard

DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR		MULTICARD	
APPROVAL	HJ KIM	REV	1.0		2 IN 1 CARD	PART NO. BA41-
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE	37 OF 55

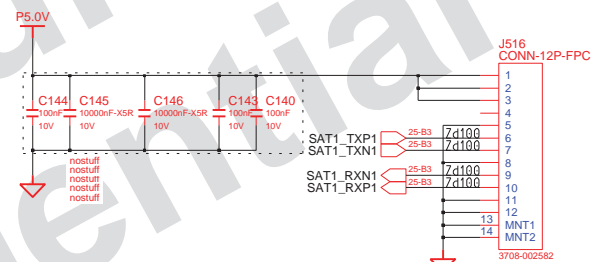
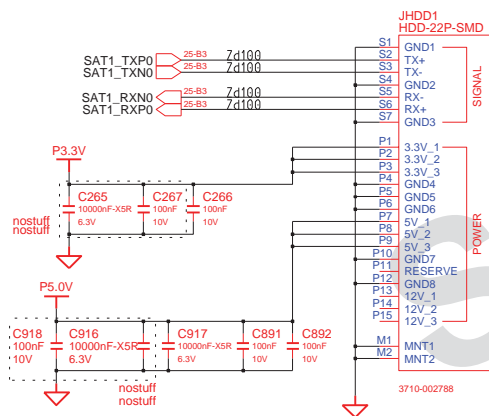
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SATA I/F CONN

SATA HDD CONN

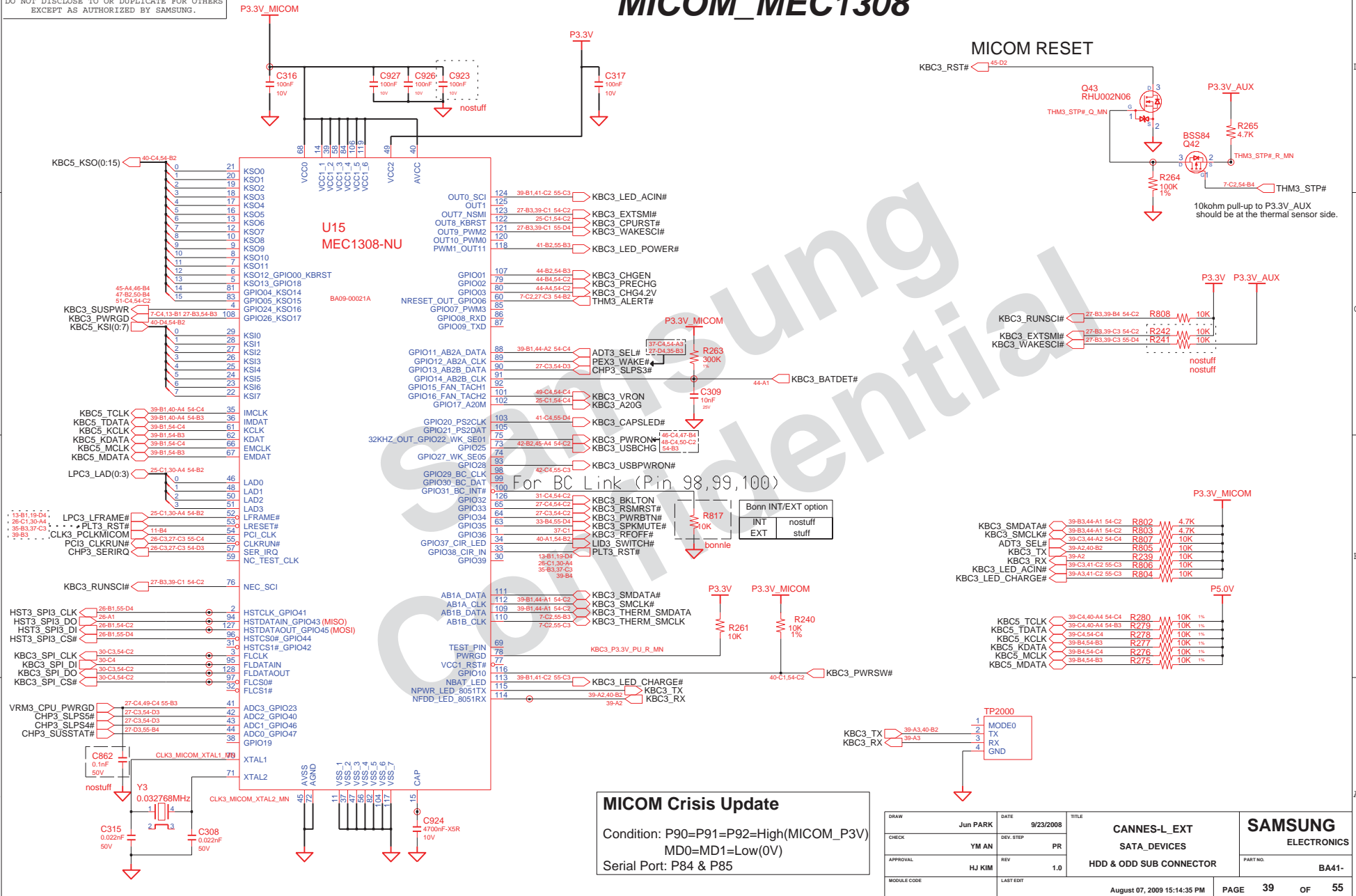
MAIN TO SUB SATA ODD CONN



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	MINI_PCIE_CONN	PART NO.	
APPROVAL	HJ KIM	REV	1.0	WLAN & HSDPA & SIM CARD	BA41-	
MODULE CODE		LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	38	OF 55

MICOM_MEC1308

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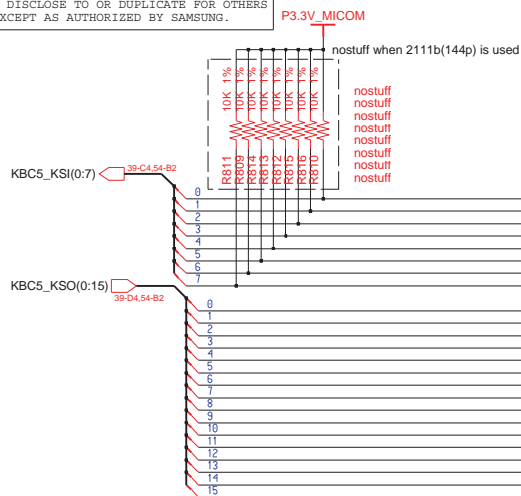
MICOM Crisis Update
 Condition: P90=P91=P92=High(MICOM_P3V)
 MD0=MD1=Low(0V)
 Serial Port: P84 & P85

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS	
CHECK	YM AN	DEV. STEP	PR		SATA_DEVICES		
APPROVAL	HJ KIM	REV	1.0		HDD & ODD SUB CONNECTOR	PART NO.	
MODULE CODE		LAST EDIT				BA41-	
					August 07, 2009 15:14:35 PM	PAGE	39 OF 55

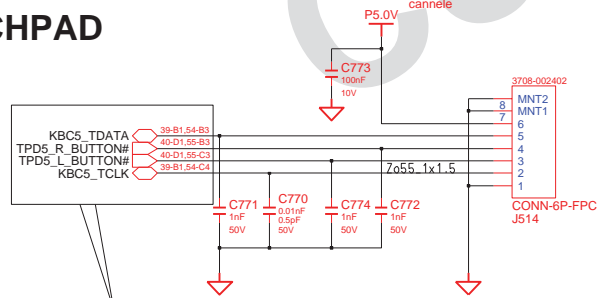
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Micom Glue Logic

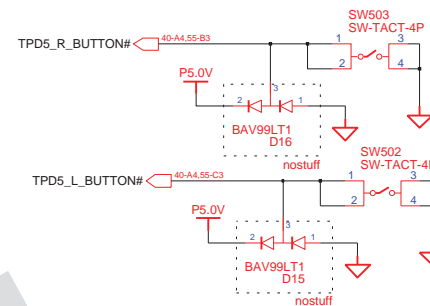
KEYBOARD



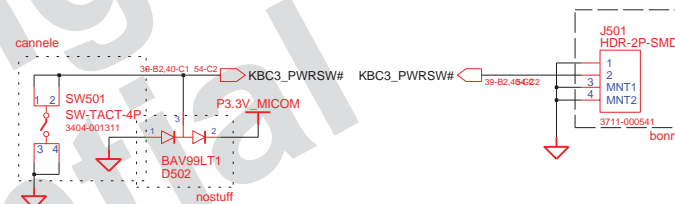
TOUCHPAD



Confirm that there are PU on Touch PAD moduel side or micom.

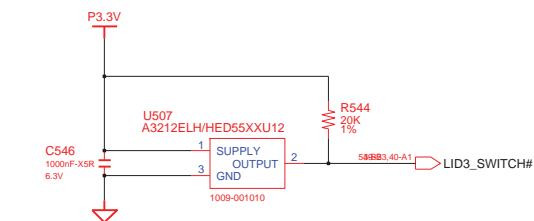


Power Switch Button

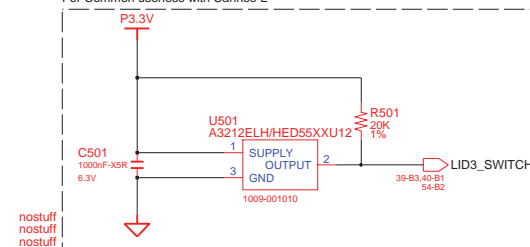


BONN-L PWRSW CONN

LID SWITCH



For Common useness with Cannes-L



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR		MICOM	
APPROVAL	HJ KIM	REV	1.0		MICOM_SMSC MEC1308	PART NO.
MODULE CODE		LAST EDIT				BA41-
				August 07, 2009 15:14:35 PM	PAGE	40 OF 55

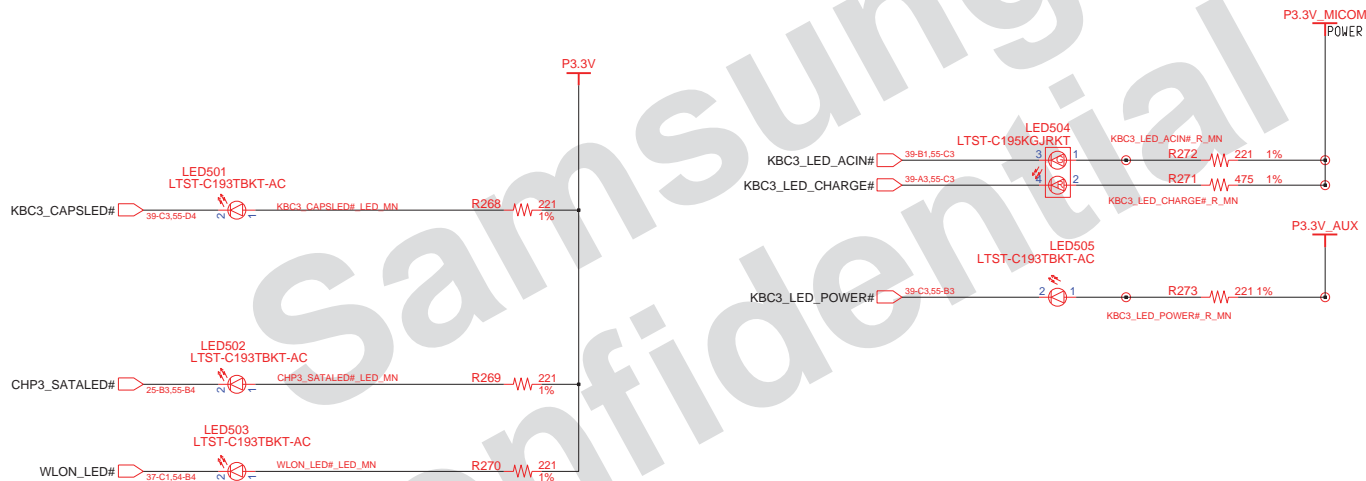
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LEDs

FUNCTION KEY LED

ADAPTERIN/CHARGING LED



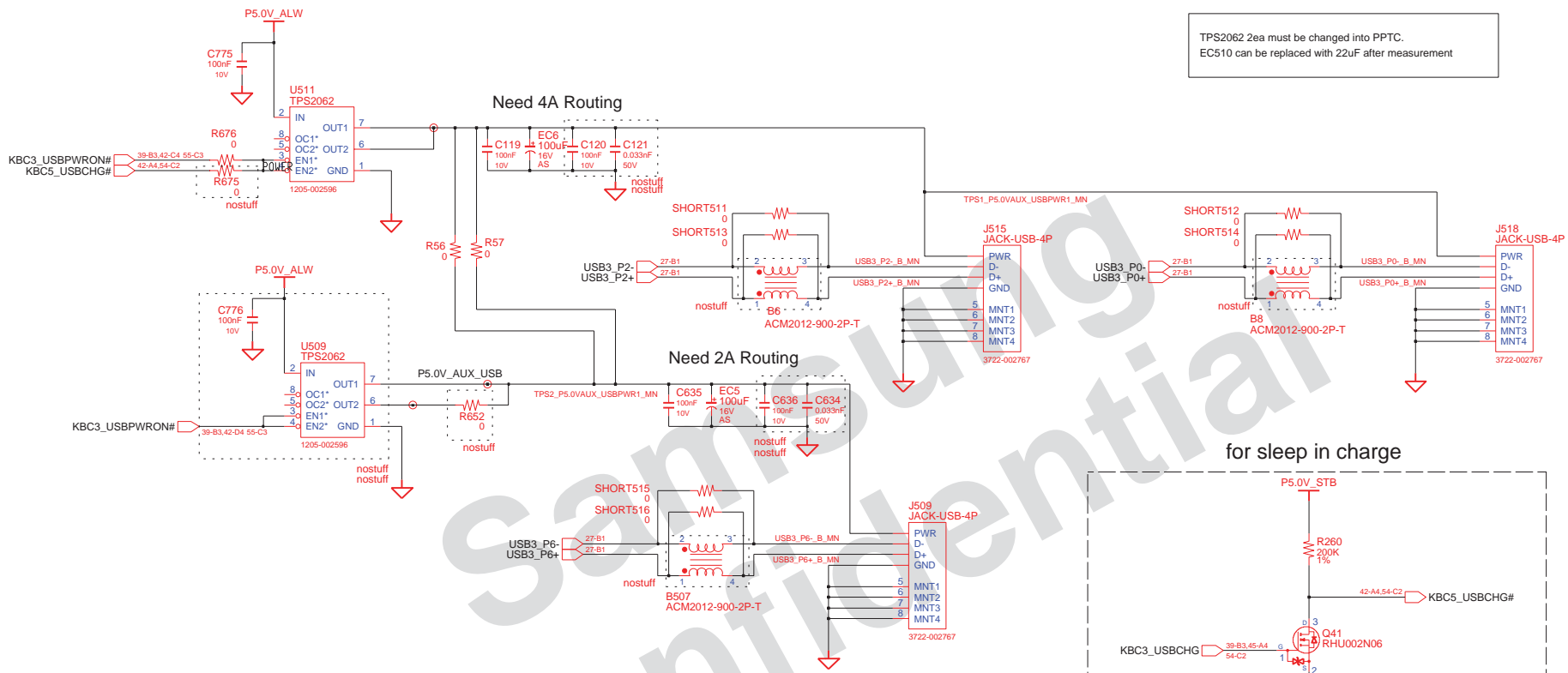
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT MICOM GLUE LOGIC KEYBOARD & TOUCHPAD	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	PART NO.		
APPROVAL	HJ KIM	REV	1.0		BA41-	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 41 OF 55	

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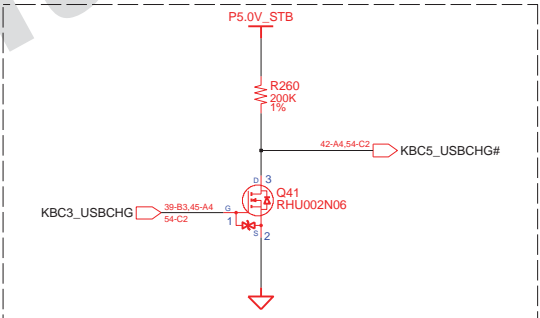
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USB Single connector X 3 (Left)

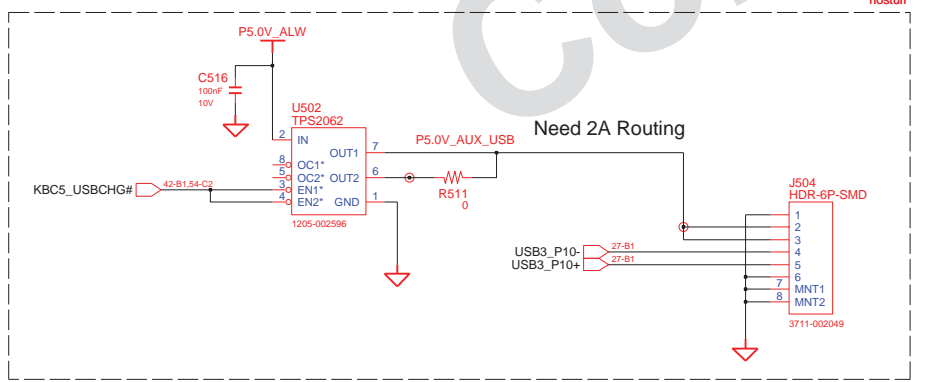
TPS2062 2ea must be changed into PPTC.
EC510 can be replaced with 22uF after measurement



for sleep in charge



USB SUB B'D CONNECTOR



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR		LED_SWITCH	
APPROVAL	HJ KIM	REV	1.0		LED_SWITCH	
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE 42	OF 55

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USB I/F Devices

Bluetooth Interface

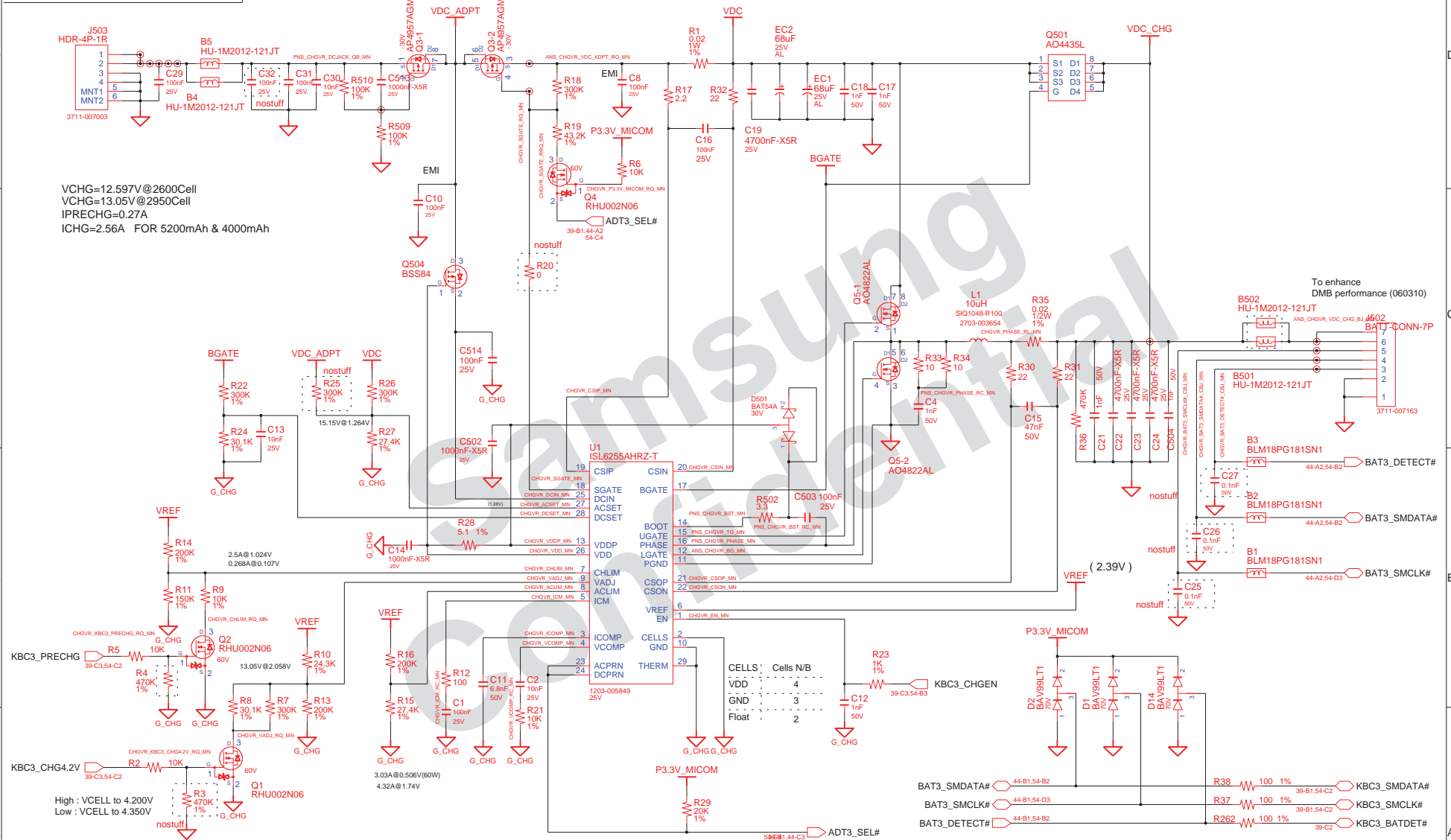
CAMERA



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	USB_CONN		
APPROVAL	HJ KIM	REV	1.0	USB & eSATA	PART NO.	BA41-
MODULE CODE		LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	43	OF 55

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CHARGE & POWER MANAGEMENT



VCHG=12.597V @2600Cell
 VCHG=13.05V @2950Cell
 IPRECHG=0.27A
 ICHG=2.56A FOR 5200mAh & 4000mAh

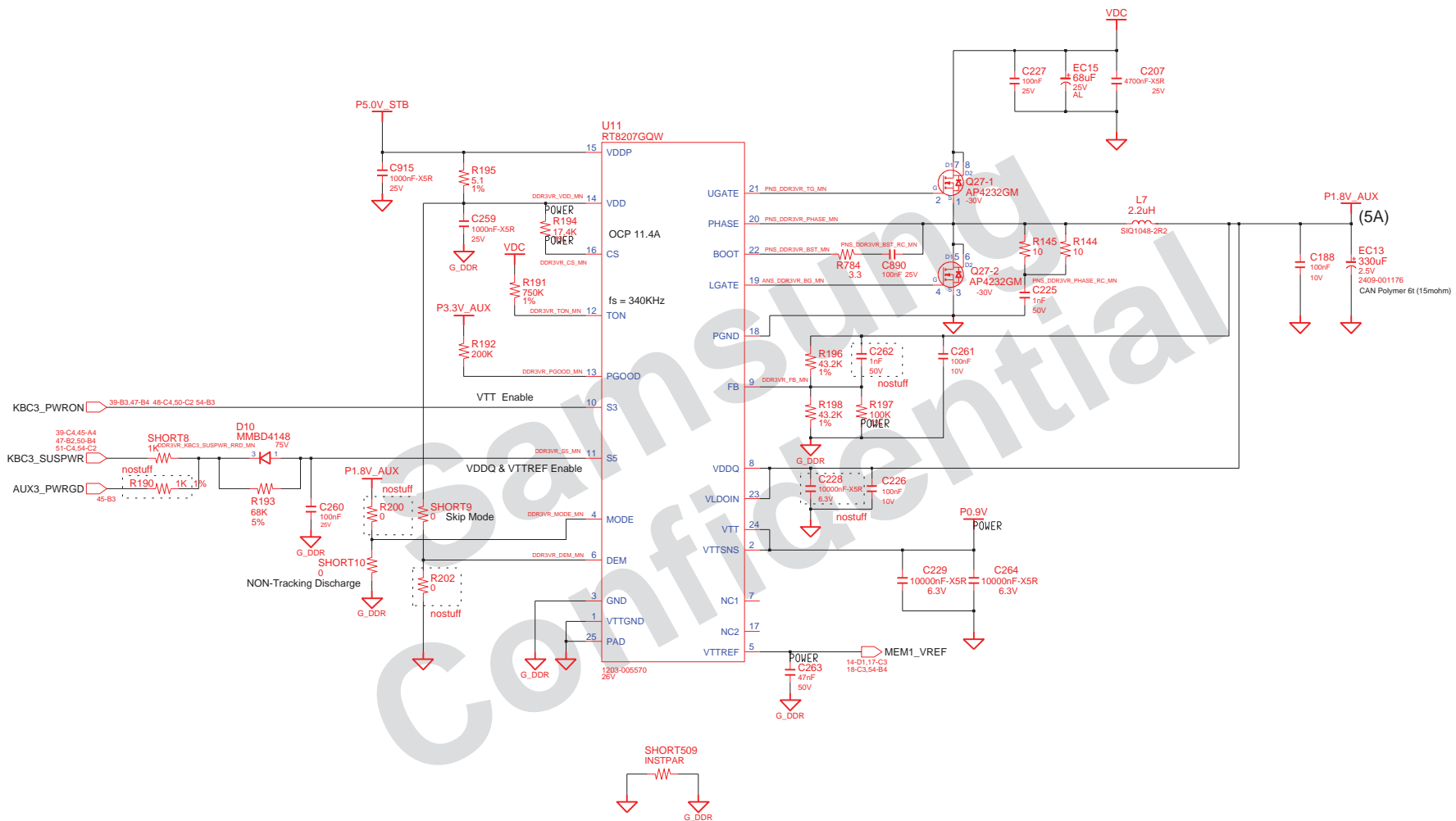
Adapter configuration				
60W / 3.03A / 96%		90W / 4.32A / 91.2%		
Value	SEC Code	Value	SEC Code	
Rtop	200K	2007-007334	10K	2007-007142
Rbot	27.4K	2007-007274	30.1K	2007-002910

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		USB_DEVICES	
APPROVAL	HJ KIM	REV	1.0		BLUETOOTH & CAMERA	PART NO. BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	44	OF 55

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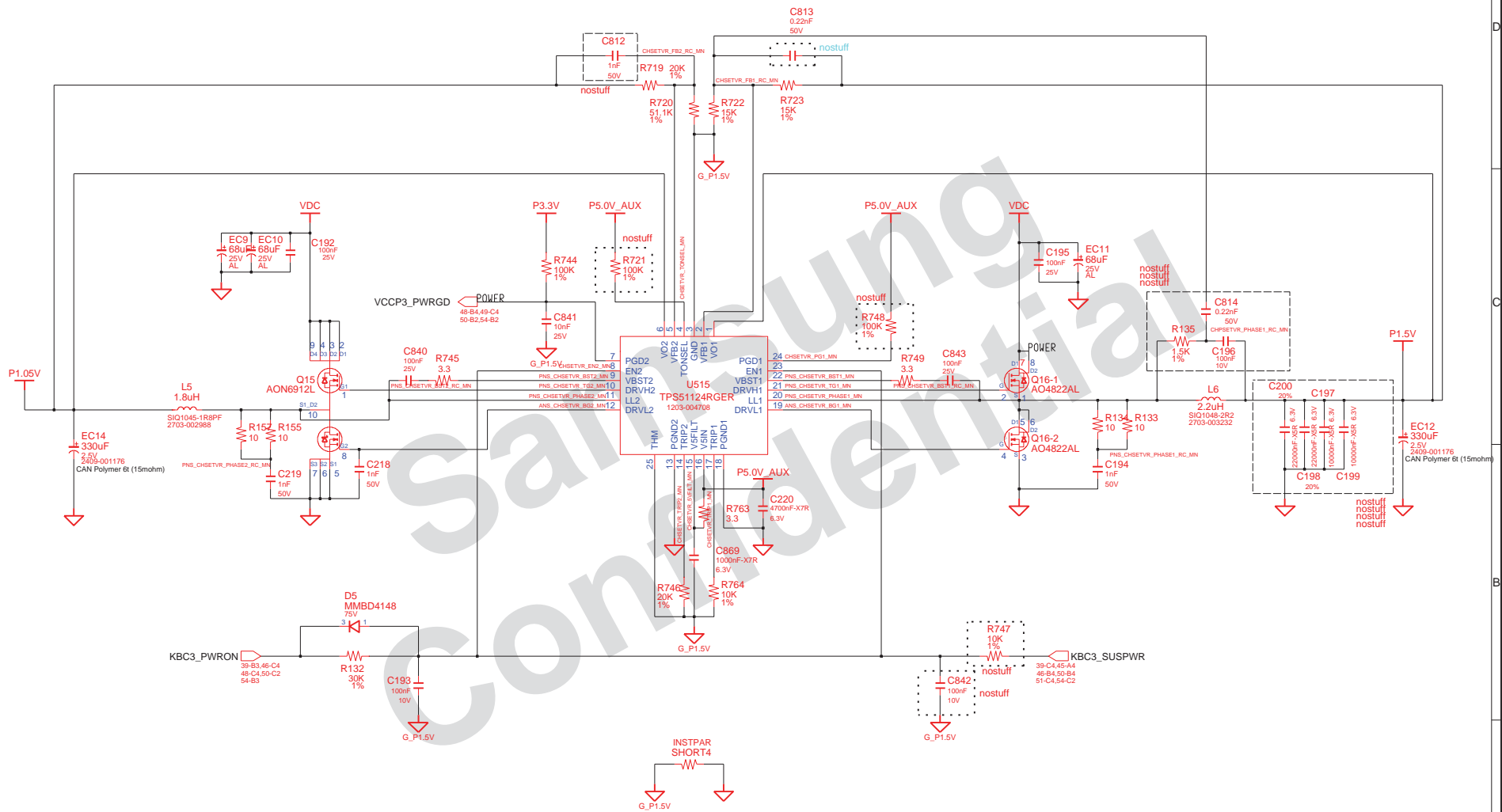
DDR2 Power



DRAW	Jun PARK	DATE	01/09/2008	TITLE	CANNES-L_EXT PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	PART NO.		
APPROVAL	HJ KIM	REV	1.0	MODULE CODE	August 07, 2009 15:14:35 PM	PAGE 46 OF 55

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CHIPSET POWER(P1.5V_AUX & P1.05V)



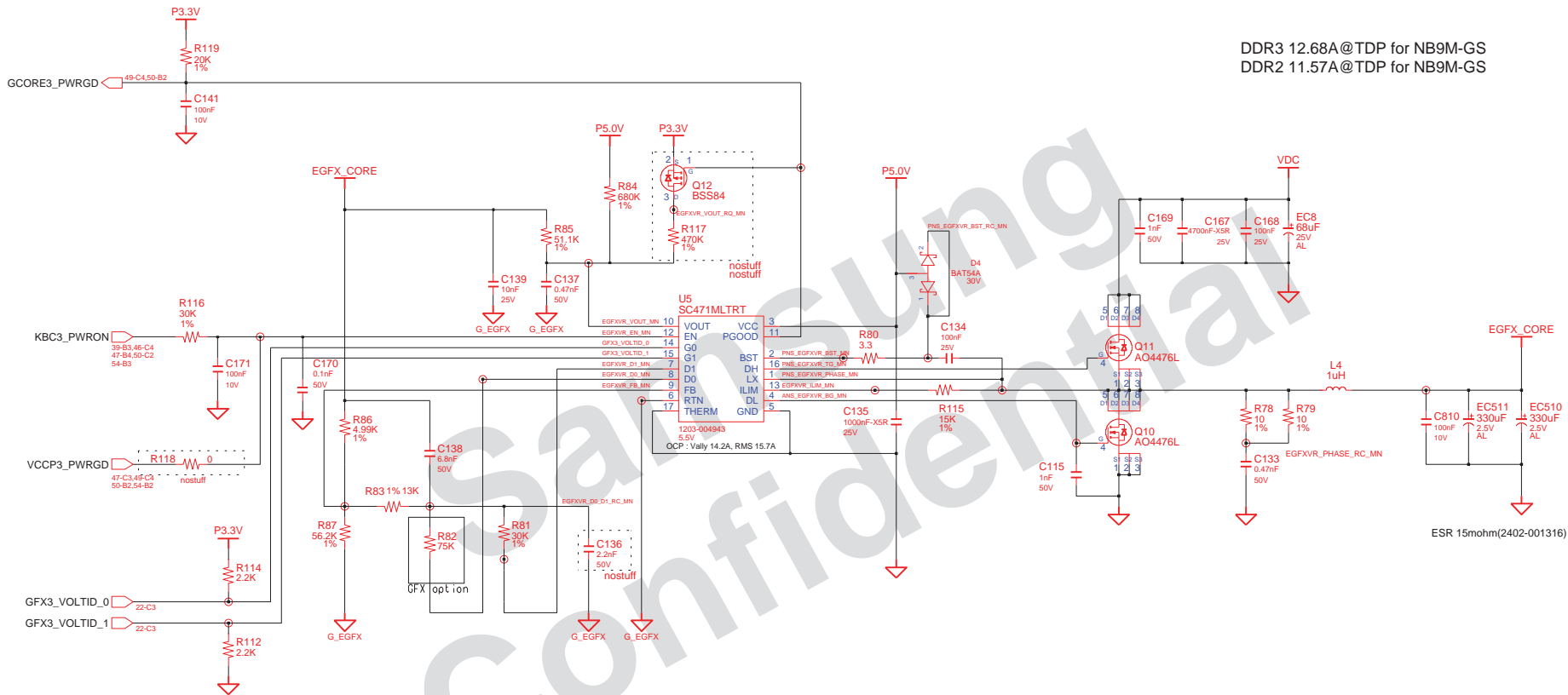
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	PWR_MEMORY	PART NO.	
APPROVAL	HJ KIM	REV	1.0	DDR2 POWER	BA41-	
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	47	OF 55

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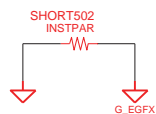
Graphic Core Power

DDR3 12.68A@TDP for NB9M-GS
DDR2 11.57A@TDP for NB9M-GS



GFX3_VOLTID		
G0	G1	
0	0	0.8V(0.8166V)
1	0	0.85V(0.8591V)
0	1	0.90V(0.9036V)
1	1	RESERVED

R845 GFX option		
LP	GE	
75K		(2007-001161)
30.1K		(2007-002910)



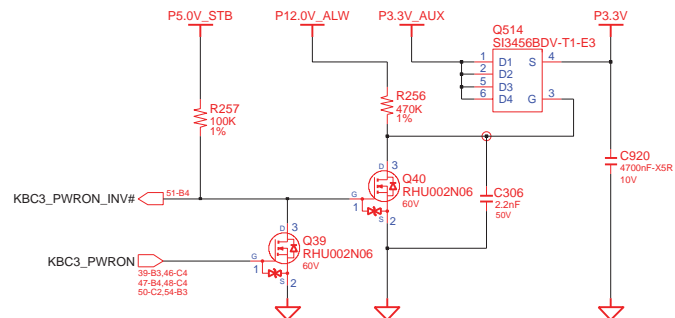
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT PWR_MV_Cantiga P1.5V_AUX, P1.05V	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR			PART NO. BA41-
APPROVAL	HJ KIM	REV	1.0			BA41-
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 48 OF 55	

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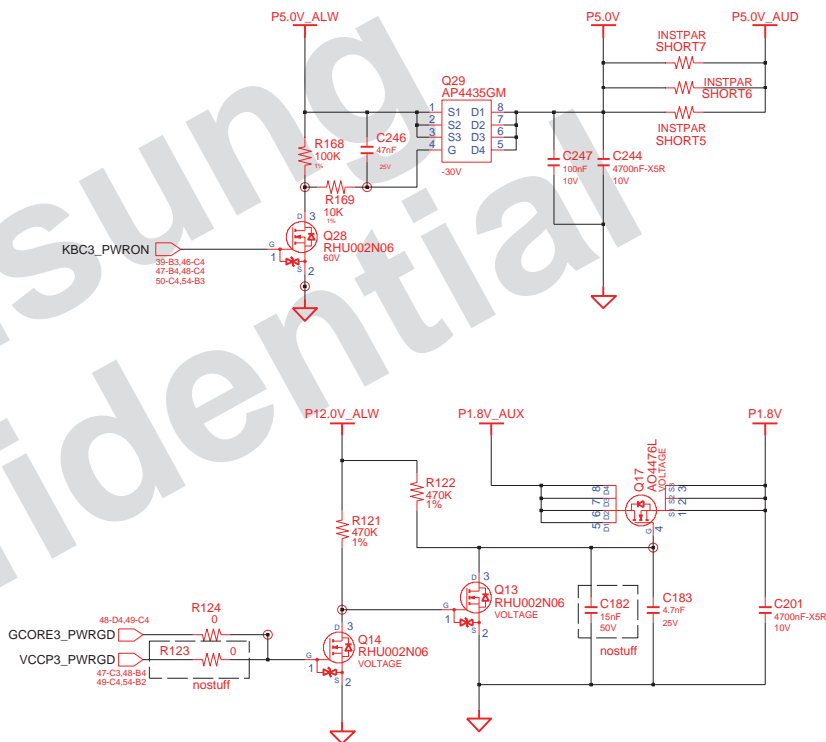
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Switched Power

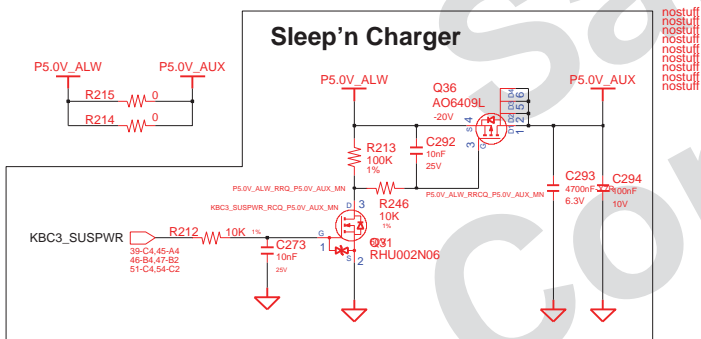
Switched Power On (P3.3V)



Switched Power On (P5.0V)



Sleep'n Charger



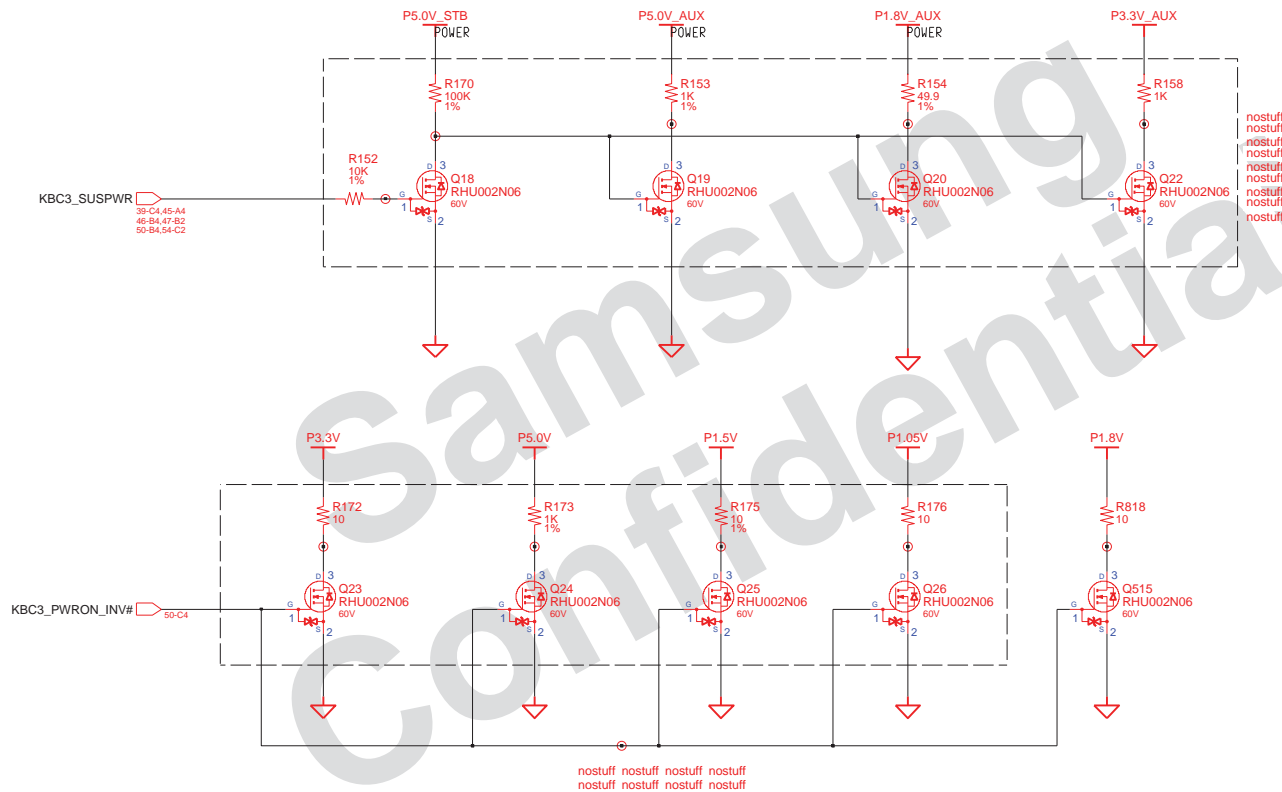
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR		PWR_CPU_MV_TPS51620	
APPROVAL	HJ KIM	REV	1.0		CPUI VRM (IMVP6+)	
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE 50 OF 55	

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POWER DISCHARGER

This page will be deleted in PV stage.



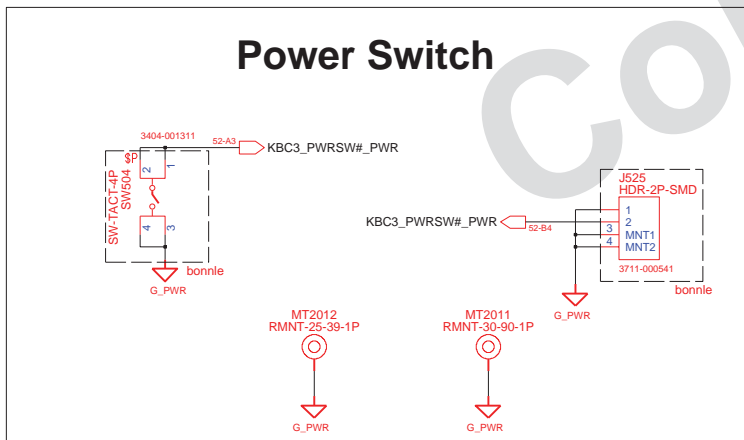
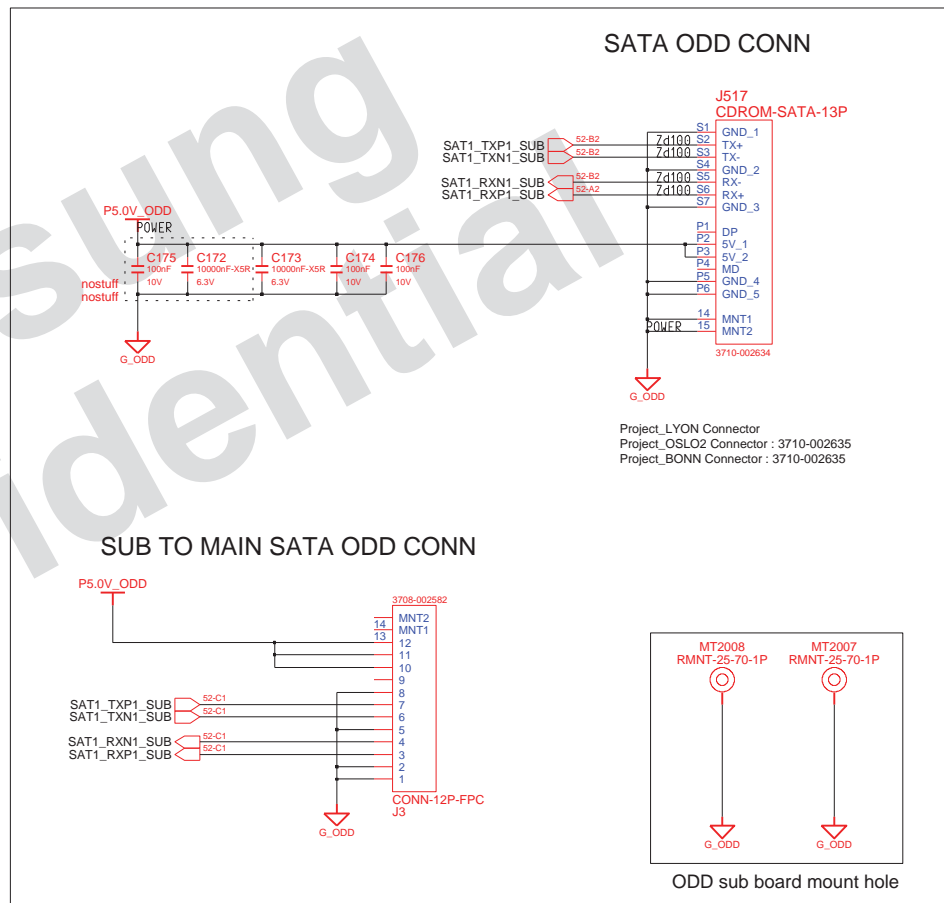
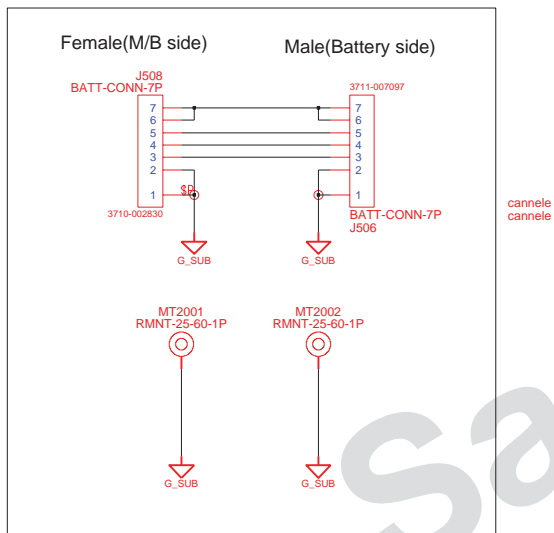
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		PWR_MV_SWITCHED	
APPROVAL	HJ KIM	REV	1.0		SWITCHED POWER	PART NO.
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM			BA41-
				PAGE	51	OF 55

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Battery & SATA ODD SUBBOARD

SATA ODD SUB BOARD

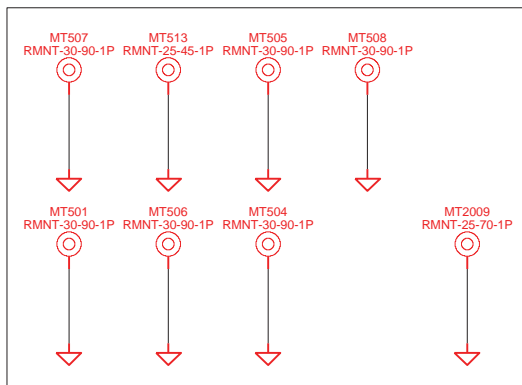


DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	PWR_MV_DISCHARGER	PART NO.	
APPROVAL	HJ KIM	REV	1.0	DISCHARGING LOGIC	BA41-	
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	52	OF 55

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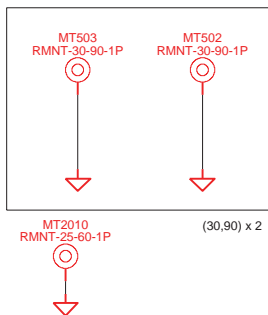
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Mainboard Mount



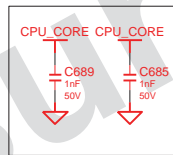
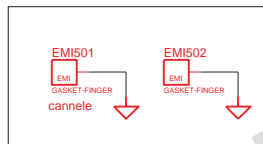
(30.90) x 7, (25.70) x 1

Keyboard Mount

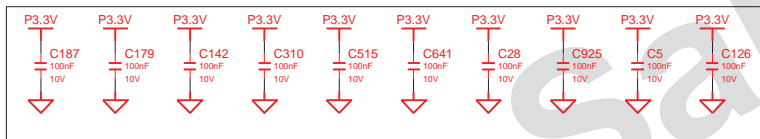


(30.90) x 2

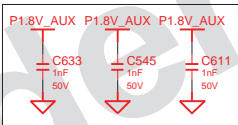
EMI FINGER



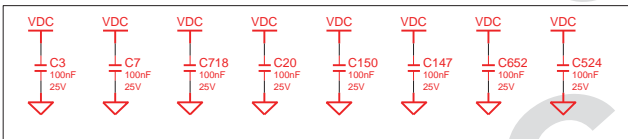
Add for EMC (Top), 2008.11.19



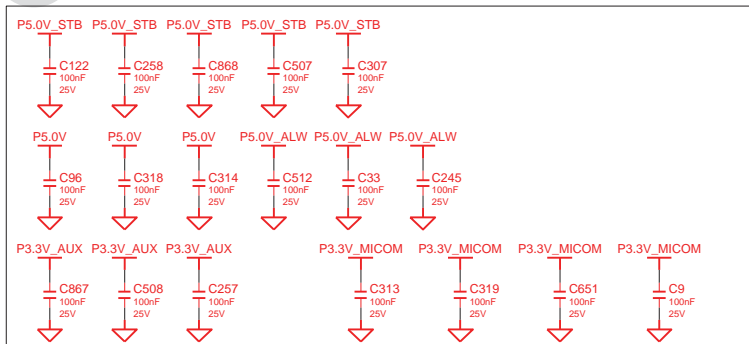
Add for EMC (5th Layer), 2008.11.19



Add for EMC (Bottom), 2008.11.19



Add for EMC (Bottom), 2008.11.19

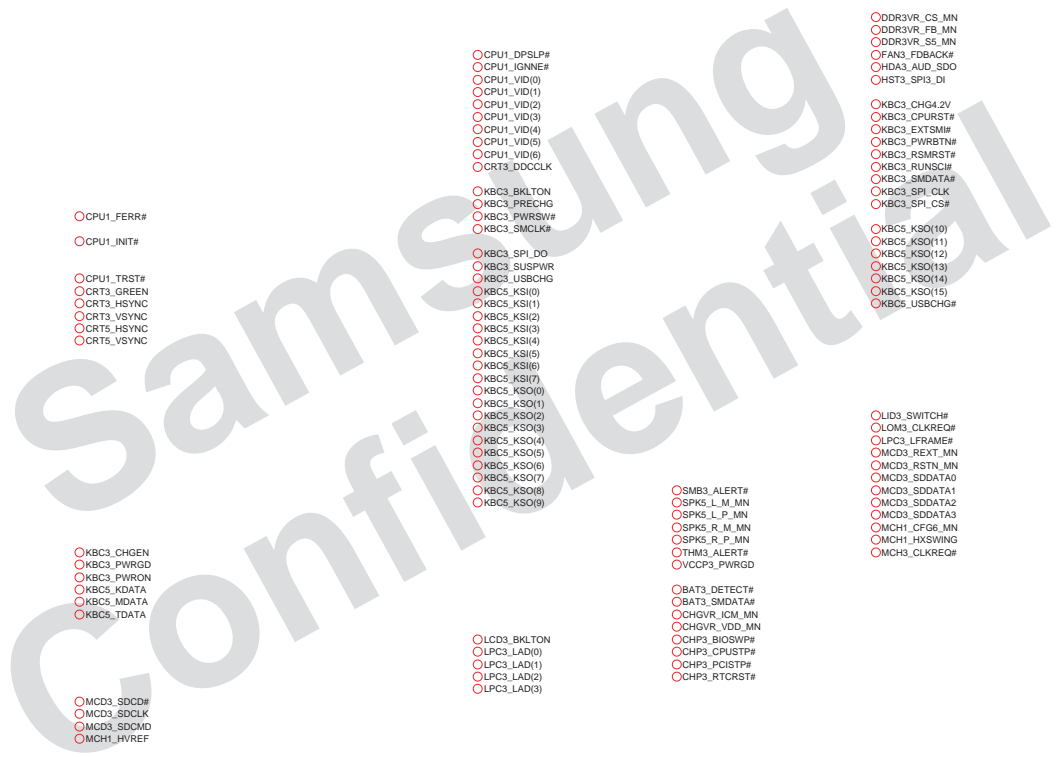


Add for EMC (Bottom), 2009.01.28

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT SUB BOARD2	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR			
APPROVAL	HJ KIM	REV	1.0		SATA ODD SUB BOARD	PART NO. BA41-
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 53	OF 55

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- CPU1_NMI
- CPU1_TCK
- CPU1_TDI
- CPU1_TMS
- CRT3_RED
- FAN5_VDD
- SMB3_CLK
- ADT3_SEL#
- AUD3_SPKR
- CPU1_PSI#
- CPU1_SMI#
- CRT3_BLUE
- KBC3_A20G
- KBC3_VRON
- KBC5_KCLK
- KBC5_MCLK
- KBC5_TCLK
- LCD3_BRIT
- MCD3_SDWP
- MEM1_VREF
- SMB3_DATA
- THM3_STP#
- W1ON_LED#
- PEX3_WAKE#
- CPU1_FERR#
- CPU1_INIT#
- CPU1_TRST#
- CRT3_GREEN
- CRT3_HSYNC
- CRT3_VSYNC
- CRT5_HSYNC
- CRT5_VSYNC
- KBC3_CHGEN
- KBC3_PWRGD
- KBC3_PWRON
- KBC5_KDATA
- KBC5_MDATA
- KBC5_TDATA
- MCD3_SDCD#
- MCD3_SDCLK
- MCD3_SDCMD
- MCH1_HVREF
- AUD5_CBP_MN
- BAT3_SMCLK#
- CHGVR_EN_MN
- CHP3_GPIO18
- CHP3_GPIO20
- CHP3_SERIRQ
- CHP3_SLPS3#
- CHP3_SLPS4#
- CHP3_SLPS5#
- CPU1_DPSLP#
- CPU1_IJNNE#
- CPU1_VID(0)
- CPU1_VID(1)
- CPU1_VID(2)
- CPU1_VID(3)
- CPU1_VID(4)
- CPU1_VID(5)
- CPU1_VID(6)
- CRT3_DCCCLK
- KBC3_BKLTON
- KBC3_PRECHG
- KBC3_PWRSW#
- KBC3_SMCLK#
- KBC3_SPI_DO
- KBC3_SUSPWR
- KBC3_USBCHG
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)
- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)
- KBC5_KSO(2)
- KBC5_KSO(3)
- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)
- LCD3_BKLTON
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- CPU1_CPURST#
- CPU1_DPRST#
- CPU1_STPCLK#
- CPU2_THERMDA
- CPU2_THERMDC
- CRT3_DCCDATA
- DDR3V3R_CS_MN
- DDR3V3R_FB_MN
- DDR3V3R_S5_MN
- FAN3_FDBACK#
- HDA3_AUD_SDO
- HST3_SPI3_DI
- KBC3_CHG4.2V
- KBC3_CPURST#
- KBC3_EXTSMI#
- KBC3_PWRBTN#
- KBC3_RSMRST#
- KBC3_RUNSCI#
- KBC3_SMDATA#
- KBC3_SPL_CLK
- KBC3_SPL_CS#
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
- KBC5_KSO(13)
- KBC5_KSO(14)
- KBC5_KSO(15)
- KBC5_USBCHG#
- LID3_SWITCH#
- LOM3_CLKREG#
- LPC3_LFRAME#
- MCD3_REXT_MN
- MCD3_RSTN_MN
- MCD3_SSDATA0
- MCD3_SSDATA1
- MCD3_SSDATA2
- MCD3_SSDATA3
- MCH1_CFG6_MN
- MCH1_HKSWING
- MCH3_CLKREG#
- BAT3_DETECT#
- BAT3_SMDATA#
- CHGVR_ICM_MN
- CHGVR_VDD_MN
- CHP3_BIOSWPP#
- CHP3_CPURST#
- CHP3_PCISTP#
- CHP3_RTRCRST#



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		ICT PORT	
APPROVAL	HJ KIM	REV	1.0		ICT PORT	PART NO. BA41-
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 54 OF 55

