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# CYGNUS C

CPU : Intel Dothan533 / Yonah(TBD)  
 Chip Set : Intel Alviso & ICH6-M  
 Remarks : Mobility Platform

Model Name : CYGNUS C  
 PBA Name : MAIN  
 PCB Code : BA41-00451A  
 Dev. Step : MP  
 Revision : 1.0  
 T.R. Date : NOV 29 2004

DRAW	CHECK	APPROVAL

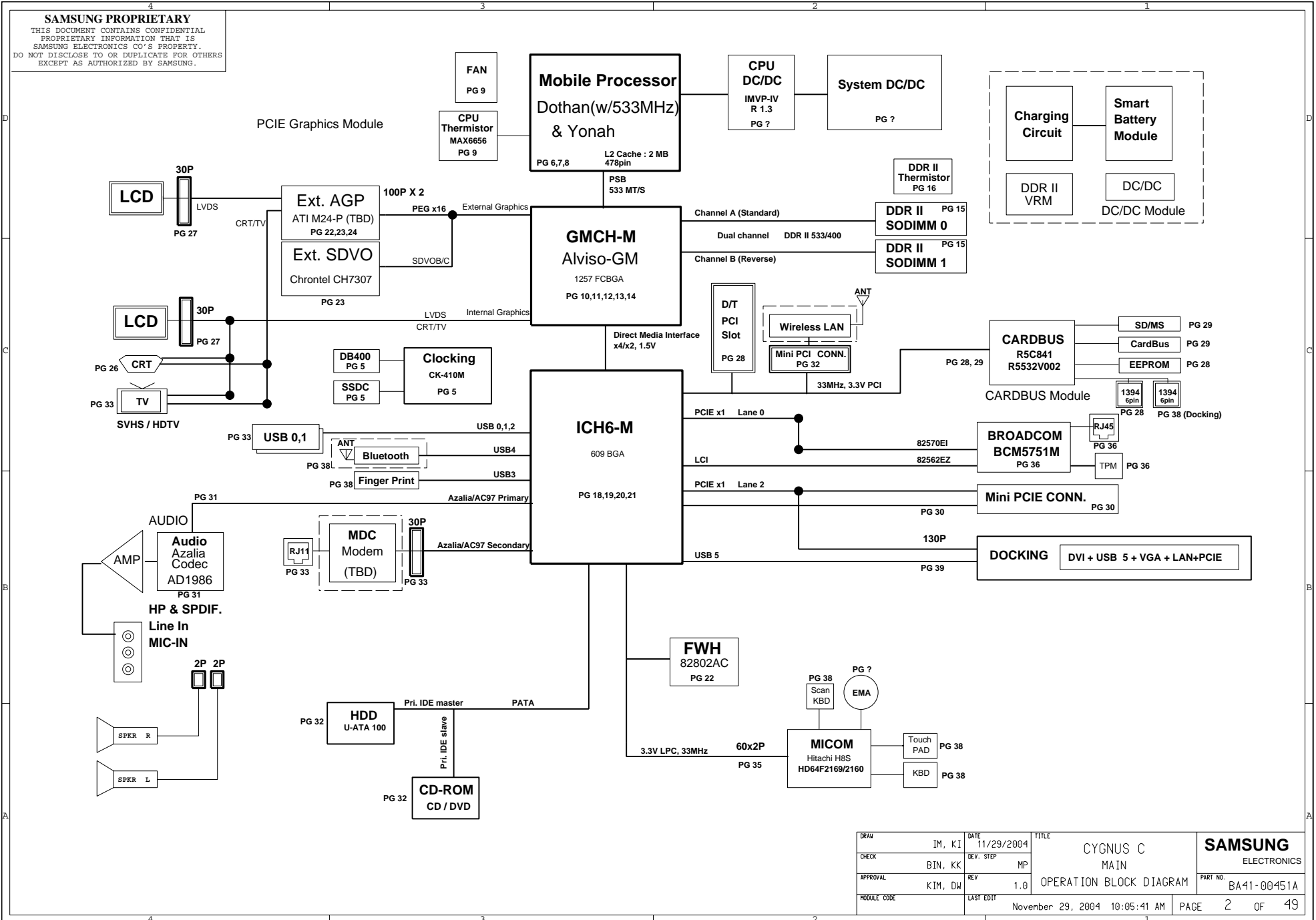
Owner : SEC Mobile R & D      Signature :      X

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MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	1	OF 49

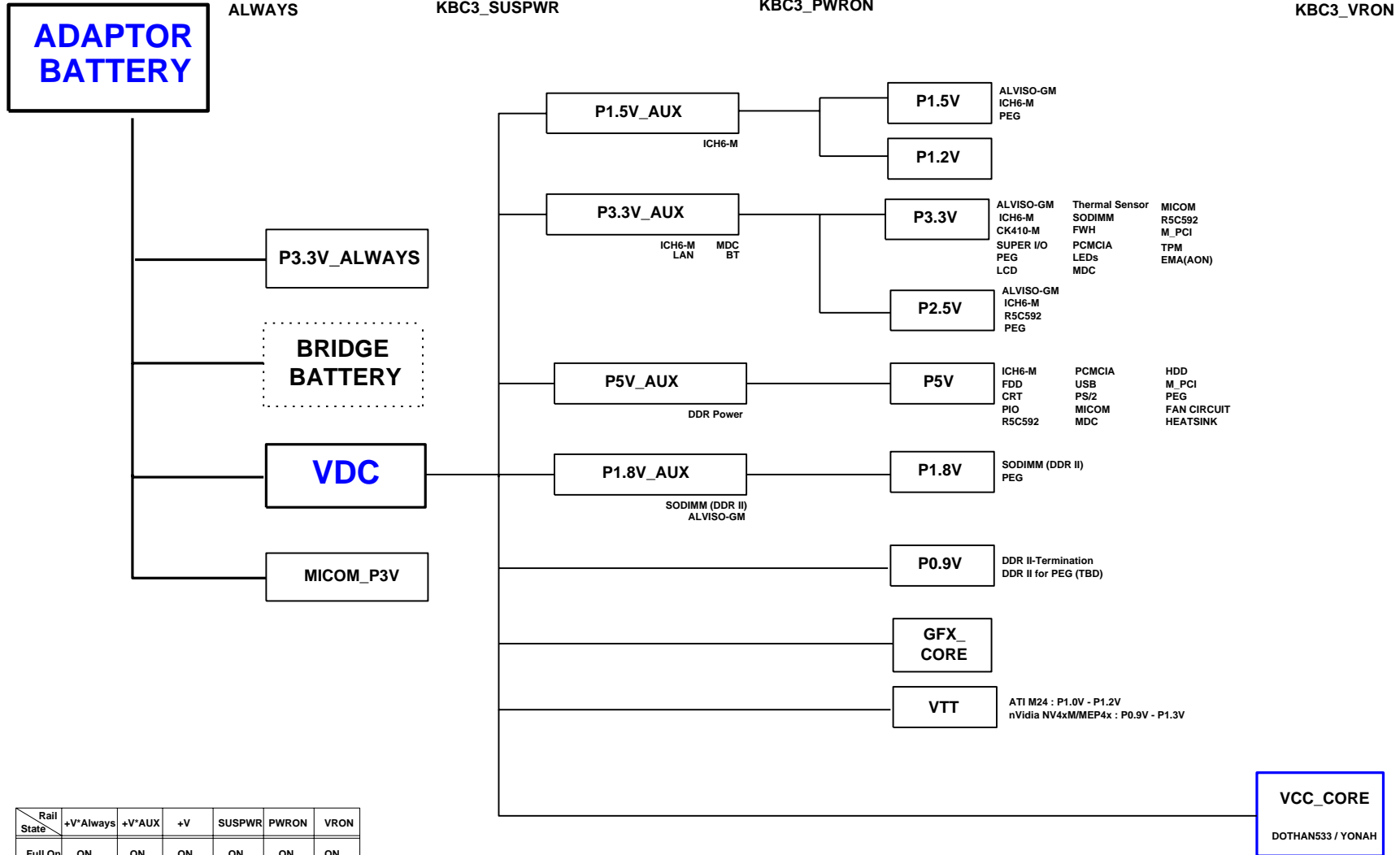
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# Power Diagram



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF	OFF
S4	ON	ON	OFF	ON	OFF	OFF
S5	ON	OFF	OFF	OFF	OFF	OFF

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# SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

## PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
	AD21	3	
MiniPCI SLOT1	AD23	2	D,E
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
		-	A,B
Internal MAC	AD24(internal)	-	E
AC Link		-	B

## Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308-1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

## CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	Northwood-B (Interposer B'd)
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	1	1	0	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	1	1	1	1	1.596 V	1	0	1	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
Highest Freq.	0	1	0	1	1	1.356 V	1	1	0	1	1	0	0.844 V	Lowest Freq.
	0	1	0	1	1	1.340 V	1	1	0	1	1	1	0.828 V	
	0	1	1	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
	0	1	1	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
	0	1	1	0	1	1.292 V	1	1	1	0	1	0	0.780 V	
	0	1	1	0	1	1.276 V	1	1	1	0	1	1	0.764 V	
	0	1	1	1	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
	0	1	1	1	0	1.244 V	1	1	1	0	1	0	0.732 V	
	0	1	1	1	1	1.228 V	1	1	1	1	1	0	0.716 V	
	0	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

## IC / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable

## USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	BLUETOOTH
4	FINGER PRINT
	OPTION
	OPTION

## System Power States

- CHP3\_SLP51\* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3\_SLP3\* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3\_SLP4\* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3\_SLP5\* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

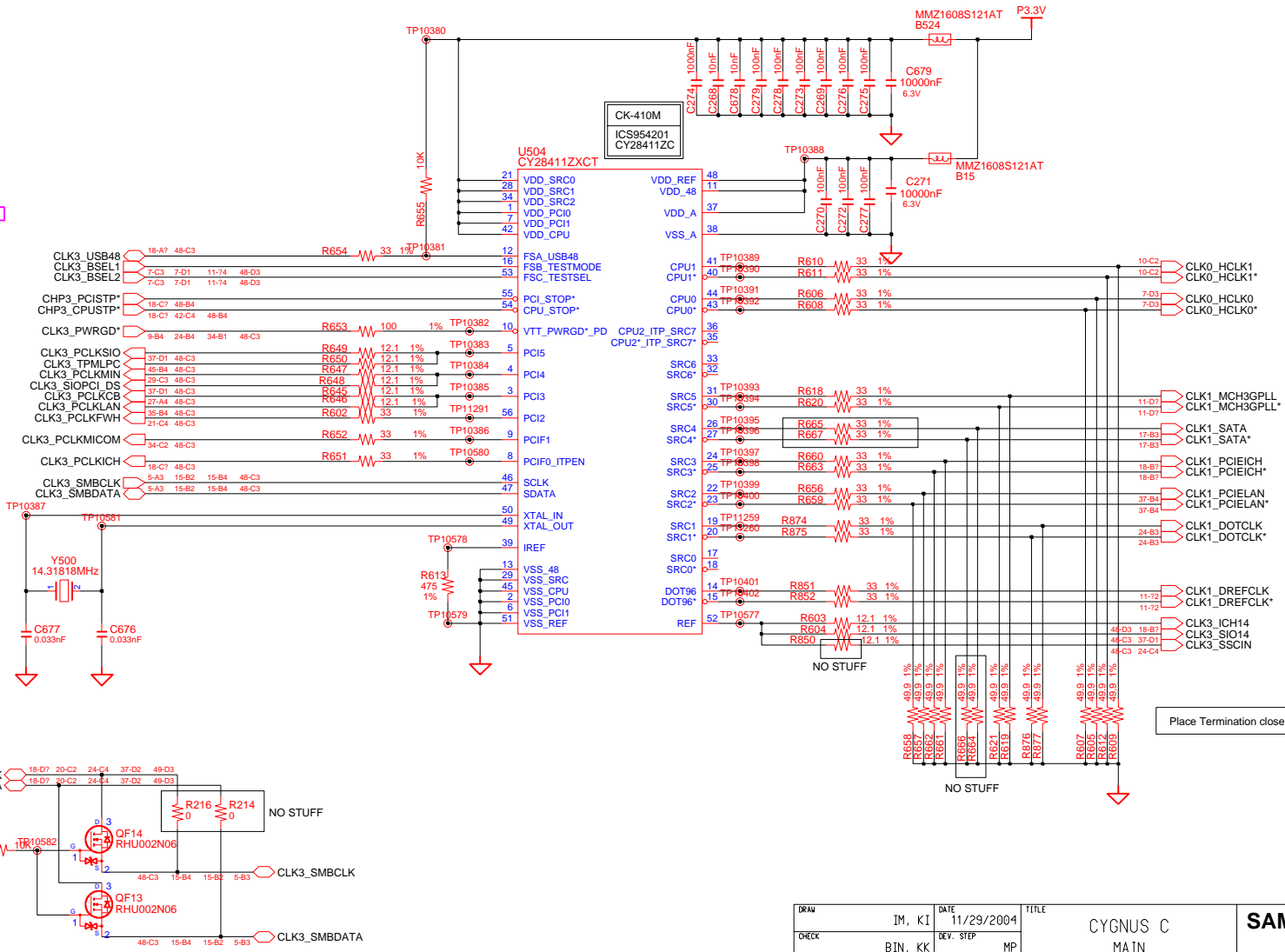
## REVISION HISTORY

See rev notes in the changes file for more information.

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APPROVAL	KIM, DW	REV	1.0		PART NO.	BA41-00451A
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FSA	FSB	FSC	HOST CLK
BSEL2	BSEL1	BSEL0	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

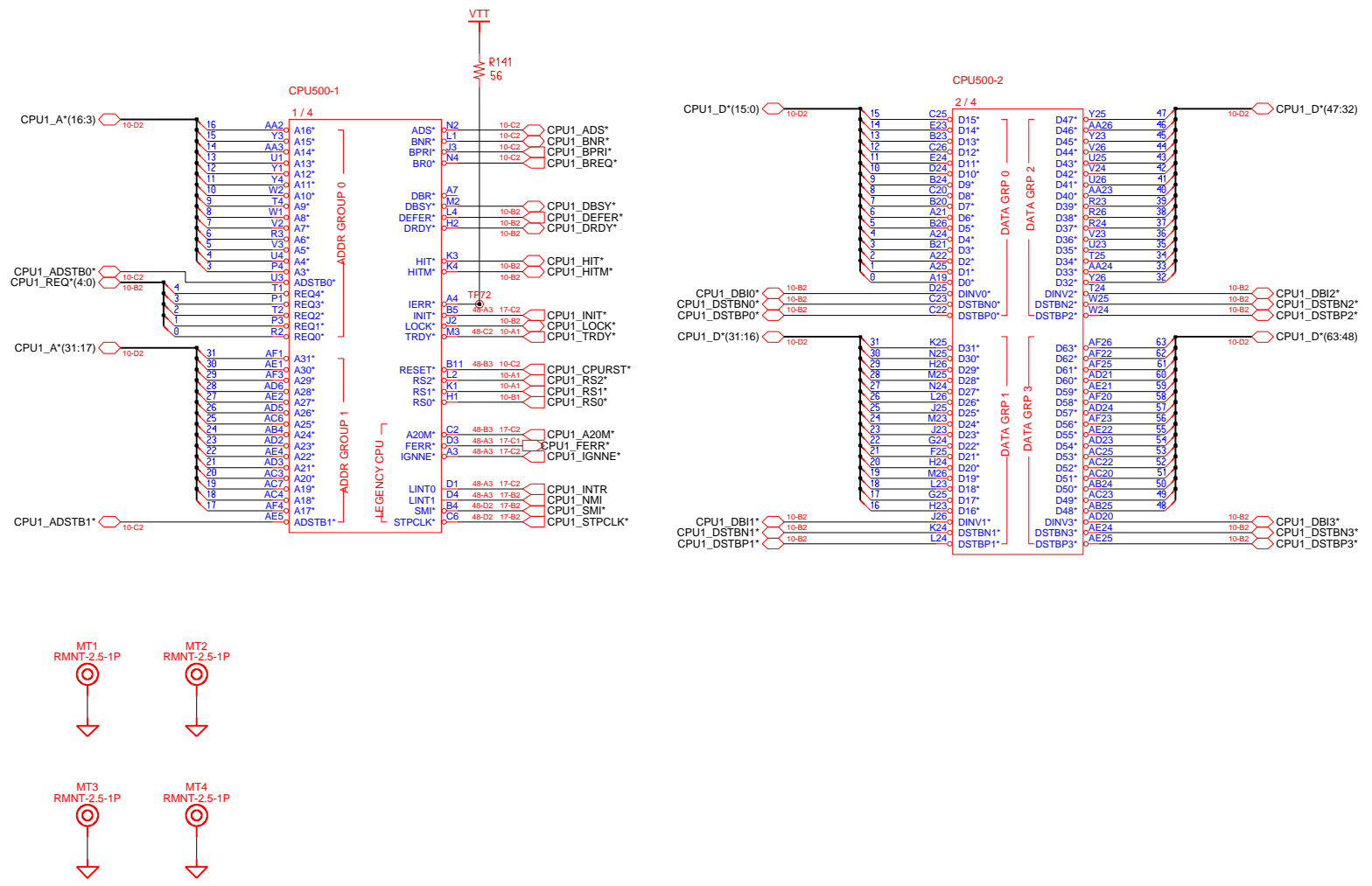


Place 14.318MHz within 500mils of CK-410M

Place Termination close to CK-410M

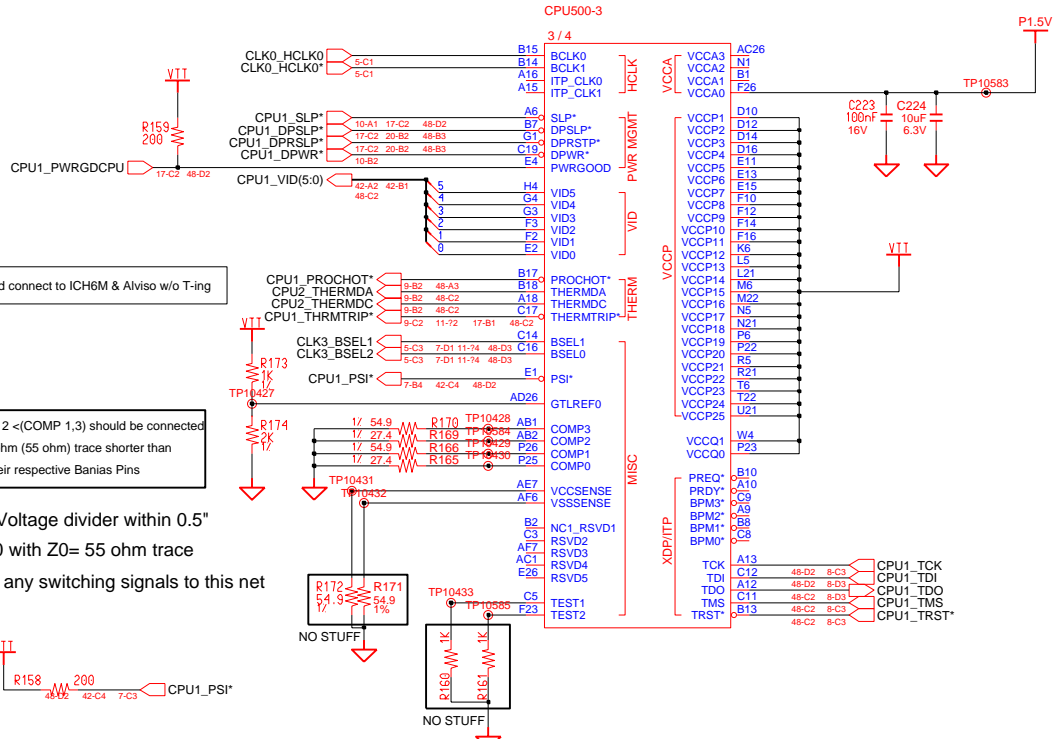
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APPROVAL	KIM, DW	REV	1.0	CLOCK GENERATOR		PART NO. BA41-00451A
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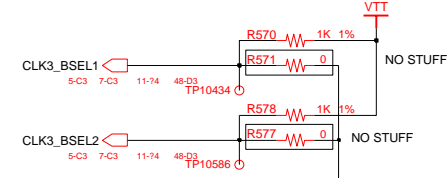
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THERTRIP\* should connect to ICH6M & Alviso w/o T-ing

COMP 0, 2 <(COMP 1,3) should be connected  
 ZO=27.4 ohm (55 ohm) trace shorter than  
 1/2" to their respective Banias Pins

GTLREF : Keep the Voltage divider within 0.5"  
 of the First GTLREF0 with ZO= 55 ohm trace  
 Minimize coupling of any switching signals to this net



### CPU Core Voltage Table

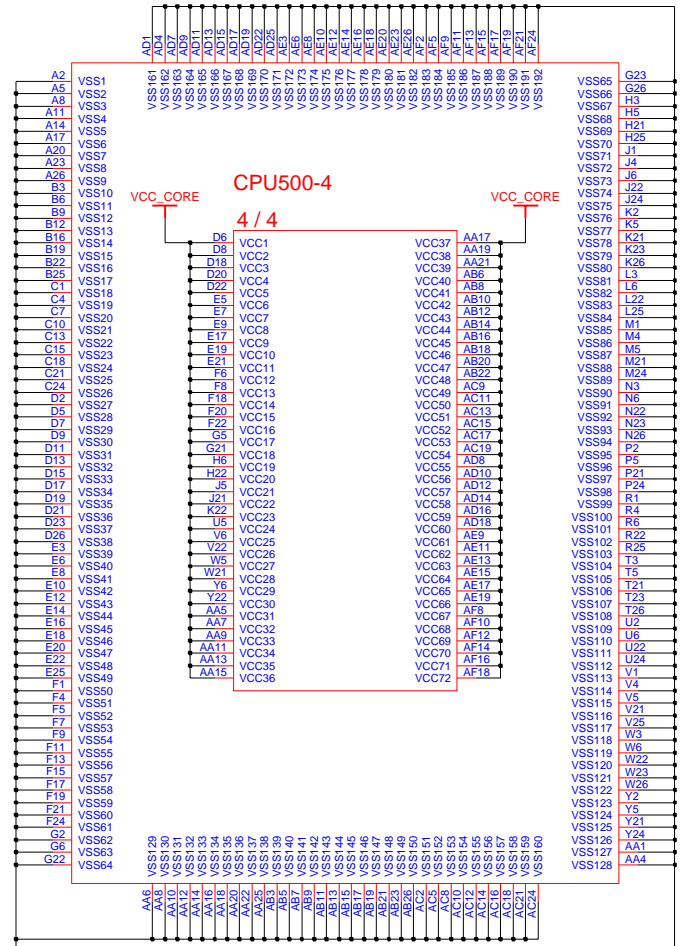
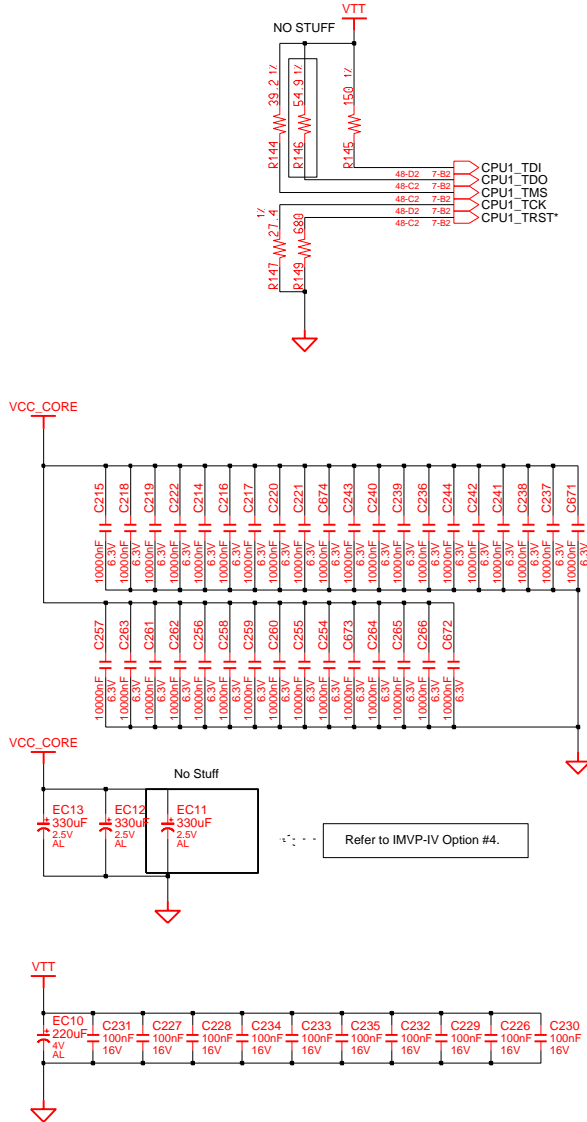
VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0	1.708 V	1 0 0 0 0	1.196 V
0 0 0 0 0	1.692 V	1 0 0 0 0	1.180 V
0 0 0 0 1	1.676 V	1 0 0 0 0	1.164 V
0 0 0 0 1	1.660 V	1 0 0 0 1	1.148 V
0 0 0 1 0	1.644 V	1 0 0 1 0	1.132 V
0 0 0 1 0	1.628 V	1 0 0 1 0	1.116 V
0 0 0 1 1	1.612 V	1 0 0 1 1	1.100 V
0 0 0 1 1	1.596 V	1 0 0 1 1	1.084 V
0 0 1 0 0	1.580 V	1 0 1 0 0	1.068 V
0 0 1 0 0	1.564 V	1 0 1 0 0	1.052 V
0 0 1 0 1	1.548 V	1 0 1 0 1	1.036 V
0 0 1 0 1	1.532 V	1 0 1 0 1	1.020 V
0 0 1 1 0	1.516 V	1 0 1 1 0	1.004 V
0 0 1 1 0	1.500 V	1 0 1 1 0	0.988 V
0 0 1 1 1	1.484 V	1 0 1 1 1	0.972 V
0 0 1 1 1	1.468 V	1 0 1 1 1	0.956 V
0 1 0 0 0	1.452 V	1 1 0 0 0	0.940 V
0 1 0 0 0	1.436 V	1 1 0 0 0	0.924 V
0 1 0 0 1	1.420 V	1 1 0 0 1	0.908 V
0 1 0 0 1	1.404 V	1 1 0 0 1	0.892 V
0 1 0 1 0	1.388 V	1 1 0 1 0	0.876 V
0 1 0 1 0	1.372 V	1 1 0 1 0	0.860 V
0 1 0 1 1	1.356 V	1 1 0 1 1	0.844 V
0 1 0 1 1	1.340 V	1 1 0 1 1	0.828 V
0 1 1 0 0	1.324 V	1 1 1 0 0	0.812 V
0 1 1 0 0	1.308 V	1 1 1 0 0	0.796 V
0 1 1 0 1	1.292 V	1 1 1 0 1	0.780 V
0 1 1 0 1	1.276 V	1 1 1 0 1	0.764 V
0 1 1 1 0	1.260 V	1 1 1 1 0	0.748 V
0 1 1 1 0	1.244 V	1 1 1 1 0	0.732 V
0 1 1 1 1	1.228 V	1 1 1 1 1	0.716 V
0 1 1 1 1	1.212 V	1 1 1 1 1	0.700 V

Highest Freq. of Dothan400(1.8GHz)  
 \* Highest Freq. of Dothan533( ?? GHz : TBD)

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Refer to Sonoma Platform Design Guide(4.6.1.4)



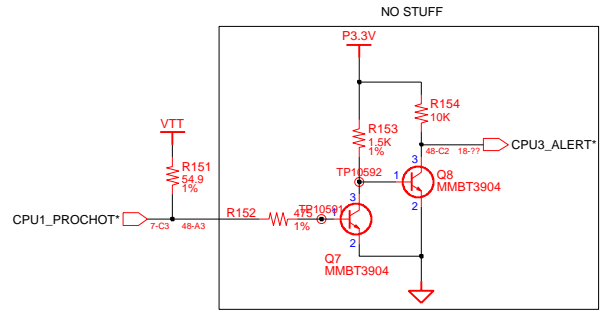
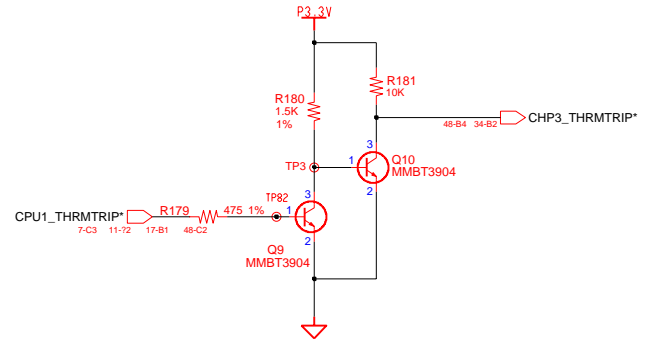
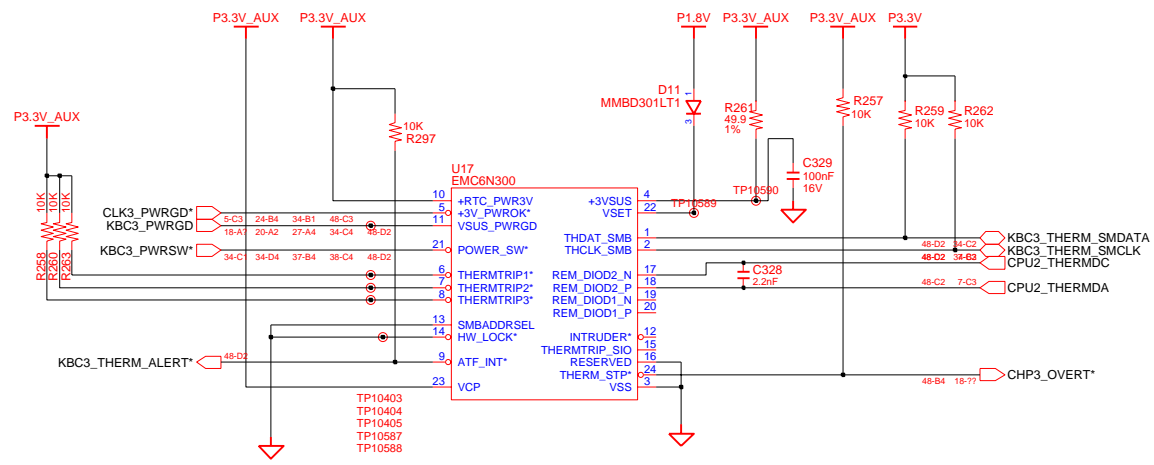
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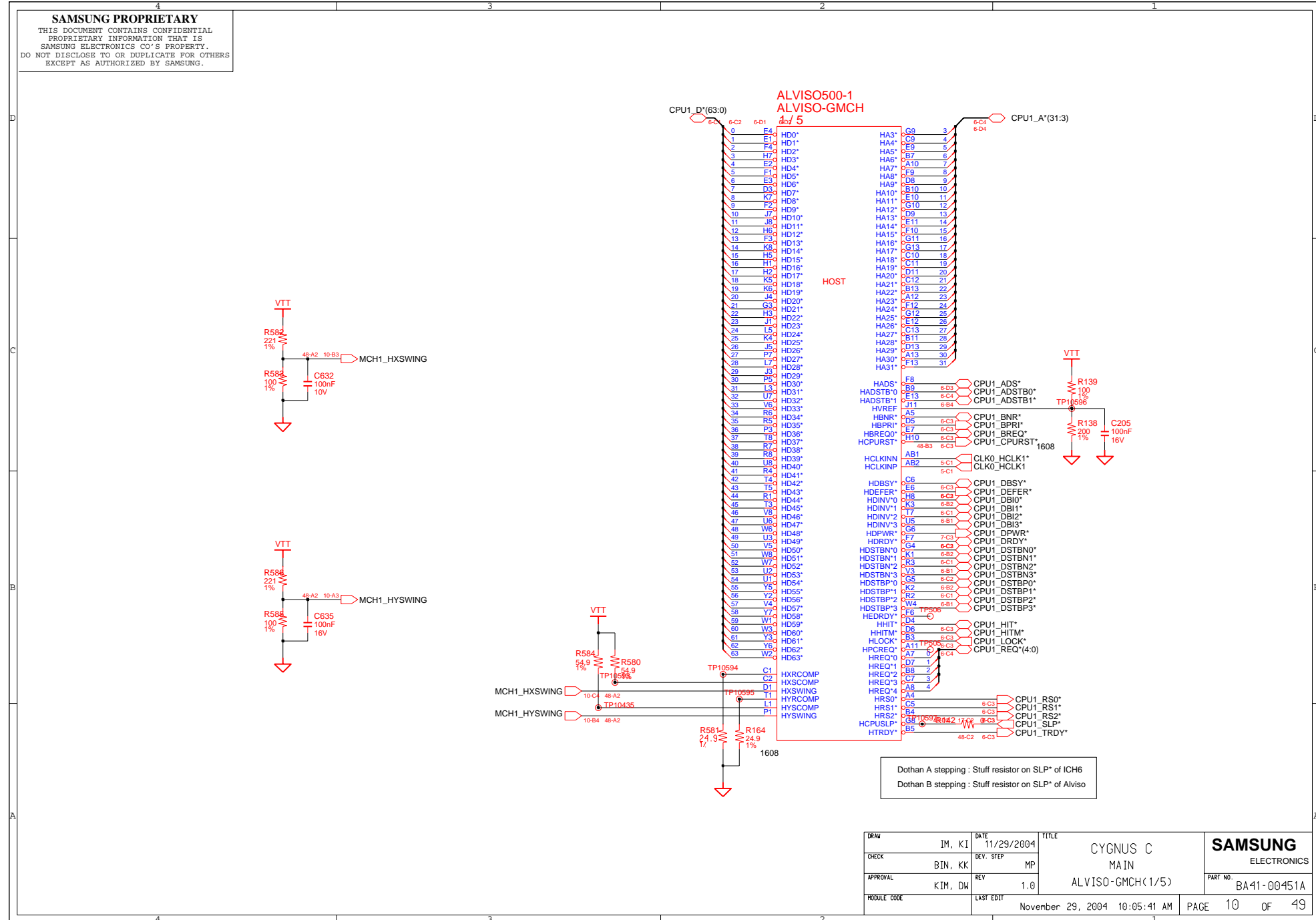
- Refer To Thermal Sensor Layout Guidelines.**
- Place the Thermal Sensor close to a remote diode.
  - Keep traces away from high voltage (+12V bus)
  - Keep traces away from fast data buses and CRT signal.
  - Use recommended trace widths and spacings (10mil)
  - Place a ground plane under the traces.
  - Use guard traces flanking DXP and DXN and connecting to GND

### CPU / DDR Thermal Sensor



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MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	9	OF 49

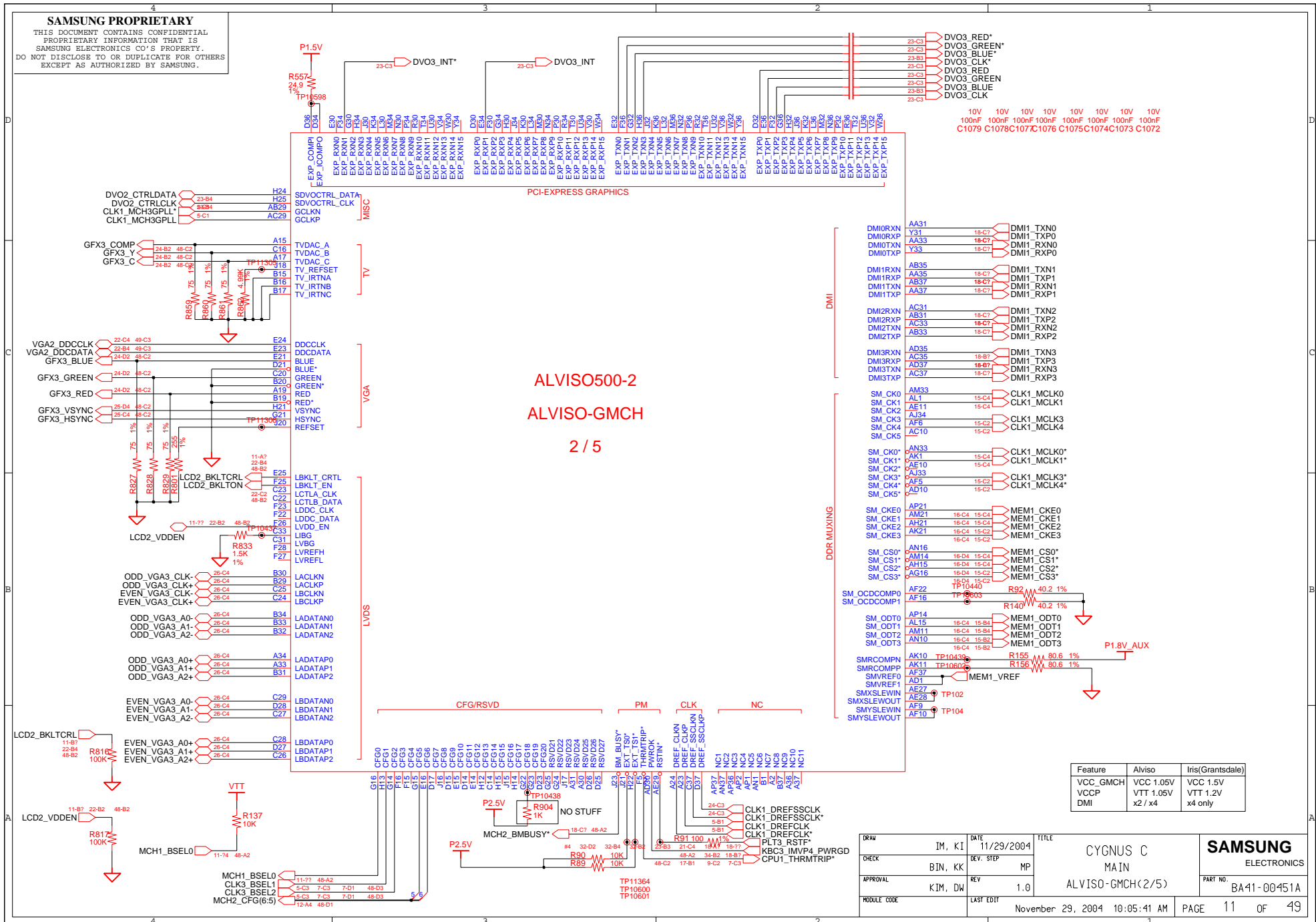
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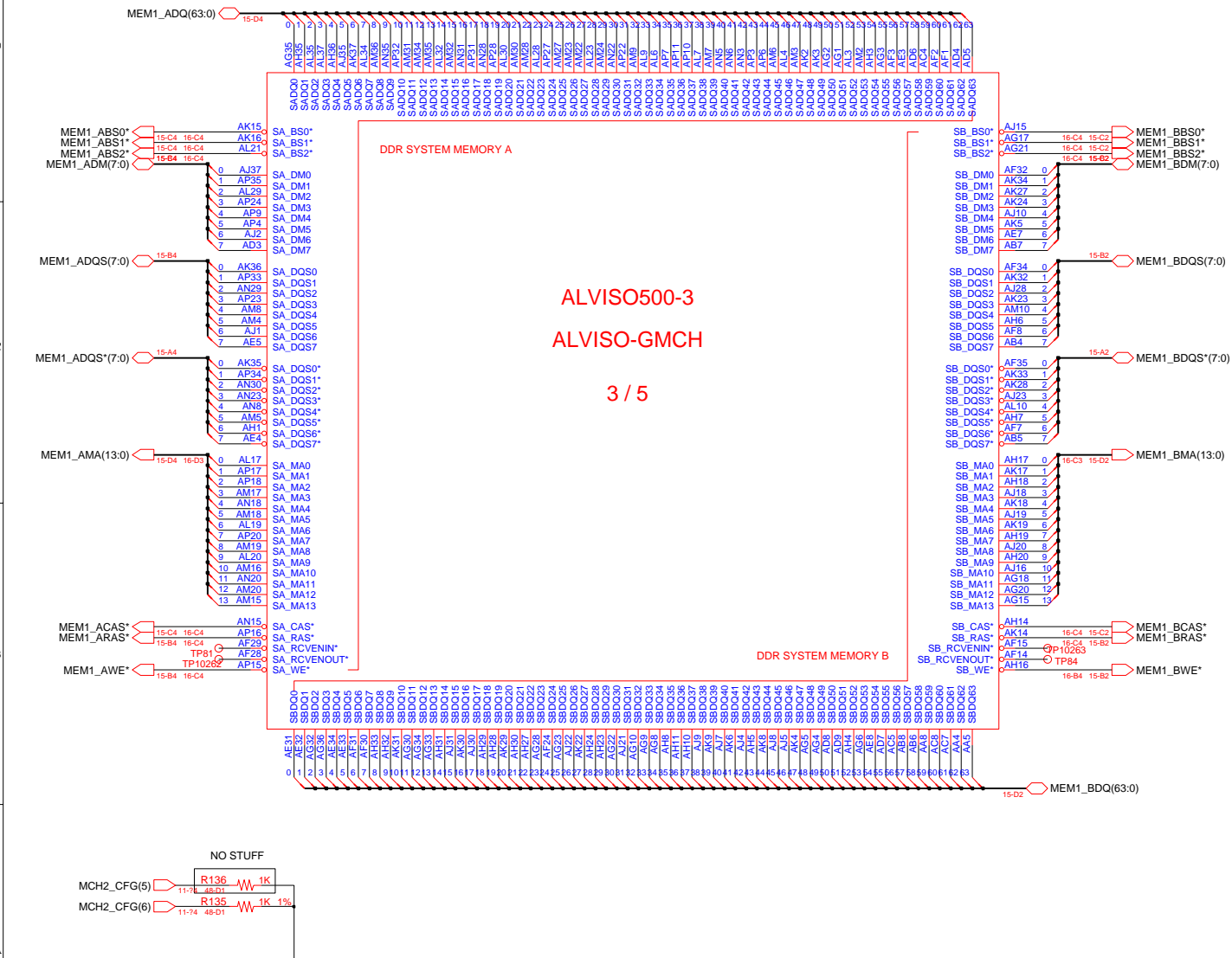
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Feature	Alviso	Iris(Grantsdale)
VCC_GMCH	VCC 1.05V	VCC 1.5V
VCCP	VTT 1.05V	VTT 1.2V
DMI	x2 / x4	x4 only

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APPROVAL	KIM, DW	REV	1.0		ALVISO-GMCH(2/5)	PART NO. BA41-00451A
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DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_ODT*(1:0)	SA_ODT*(1:0)	N/A
SM_SKE(3:2)	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

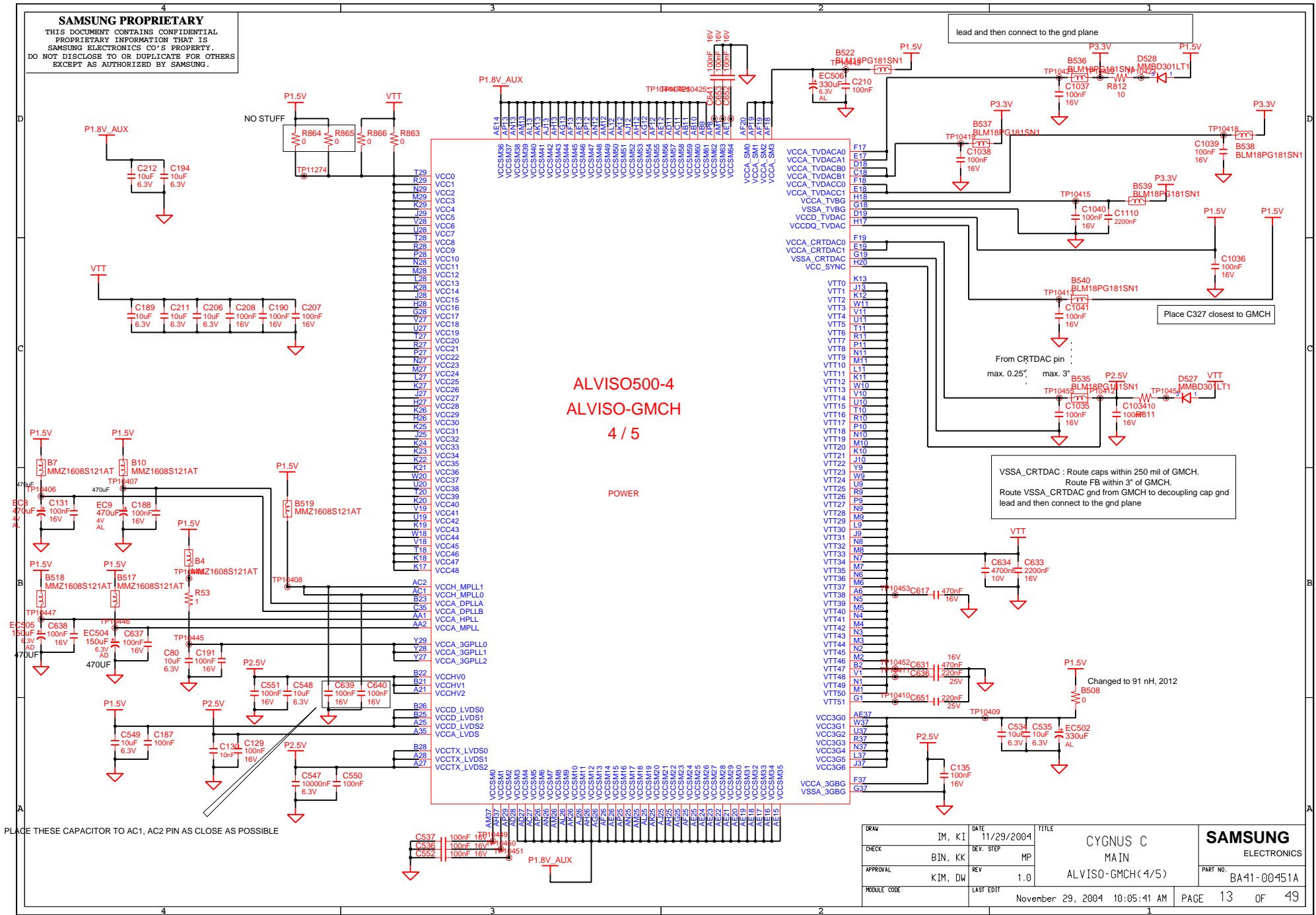
SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXN_5
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	EXP_TXN_6
SDVOC_GREEN*	EXP_TXN_7
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_8
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_9
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

def. : default Option

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN	BA41-00451A	
APPROVAL	KIM, DW	REV	1.0	ALVISO-GMCH(3/5)		
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	12	OF 49

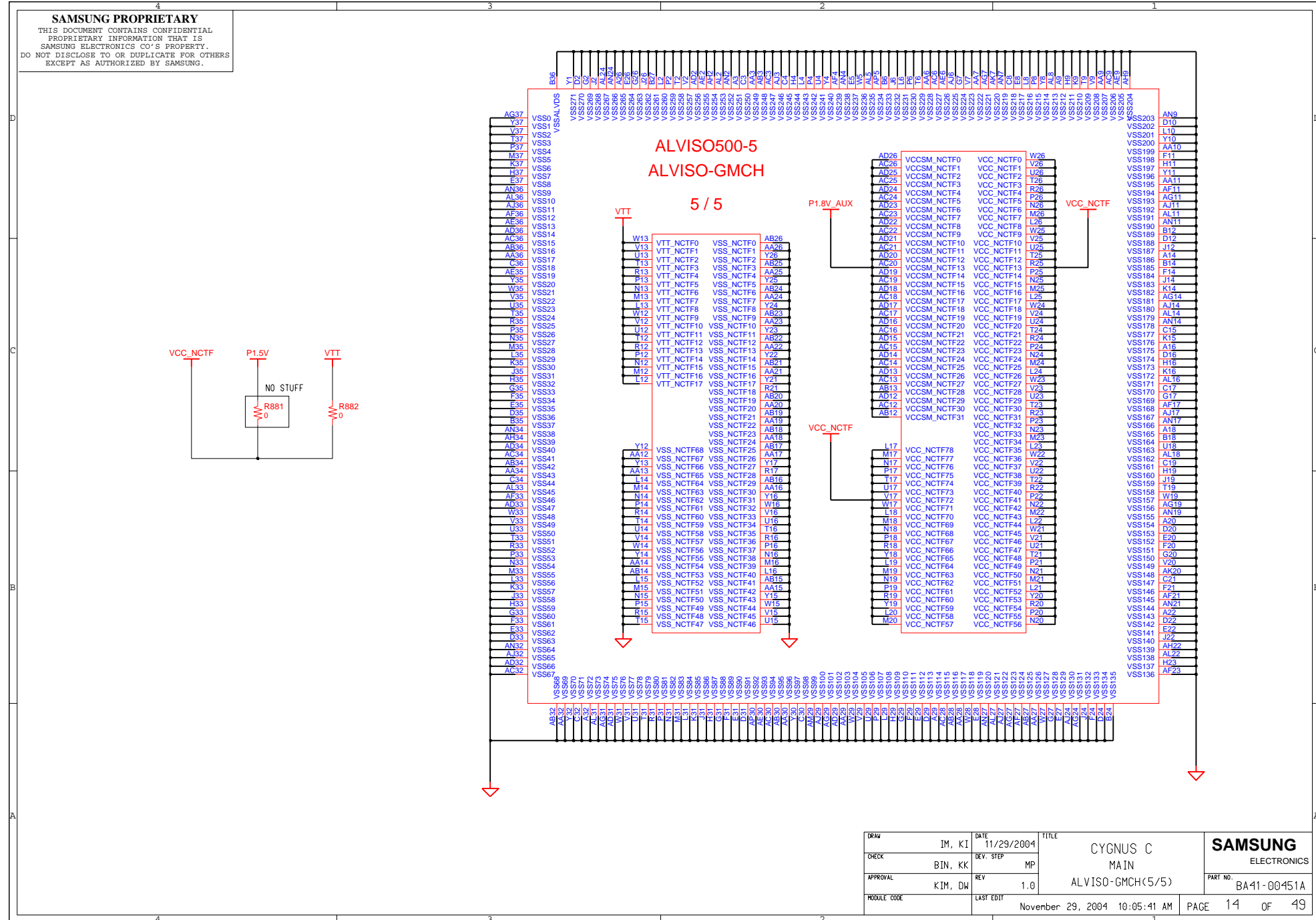
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**ALVISO500-4  
 ALVISO-GMCH  
 4 / 5  
 POWER**

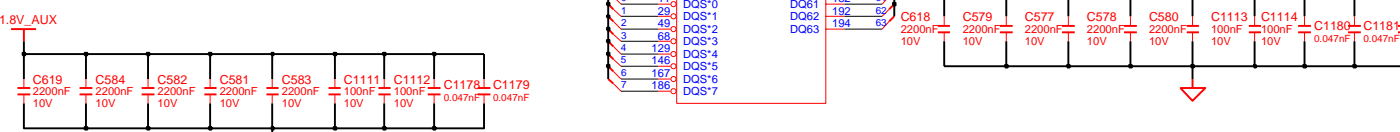
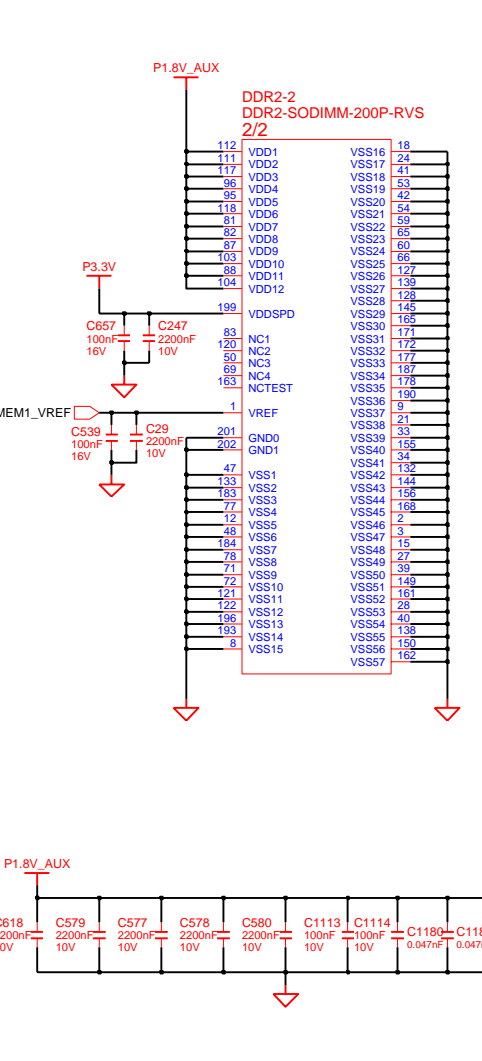
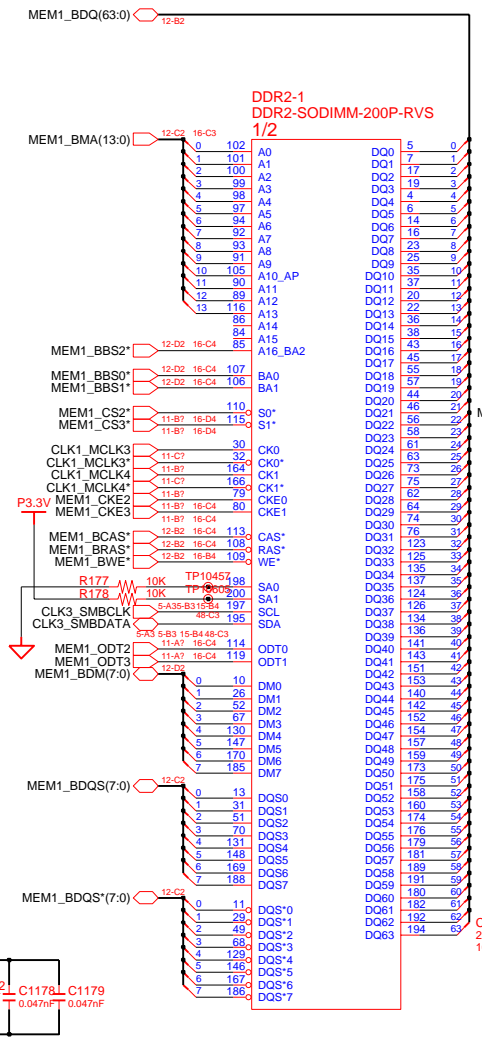
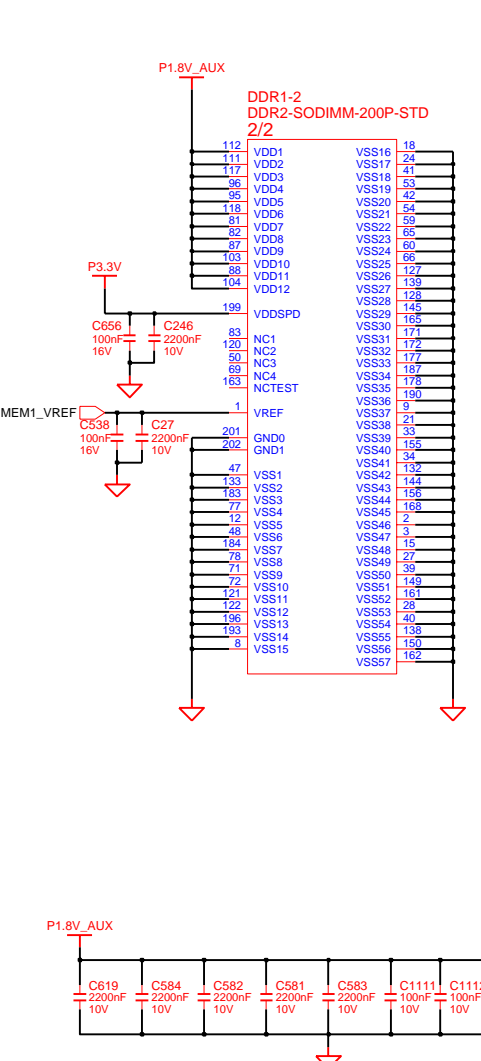
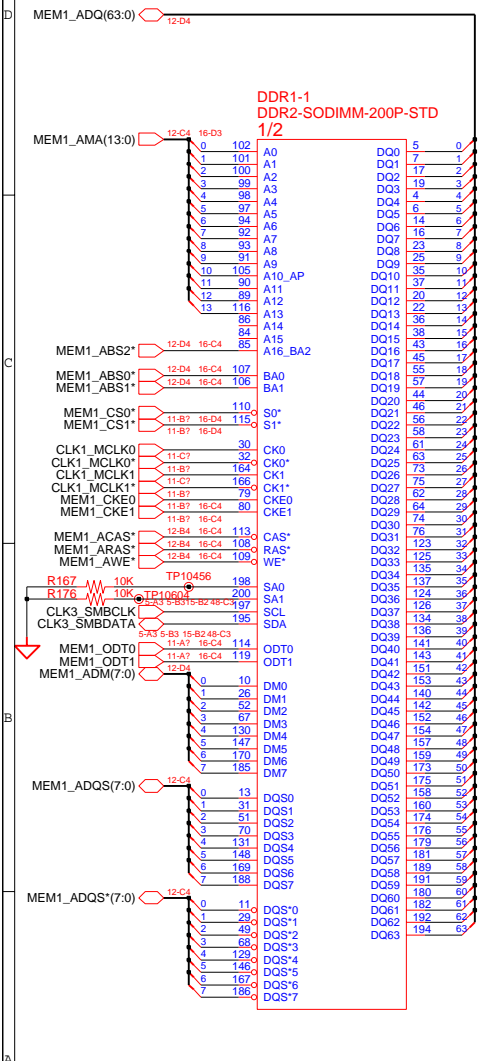
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CHECK	BIN, KK	DEV. STEP	MP	ALVISO-GMCH(4/5)		
APPROVAL	KIM, DW	REV	1.0			PART NO. BA41-00451A
MODULE CODE	LAST EDIT		November 29, 2004 10:05:41 AM		PAGE	13 OF 49

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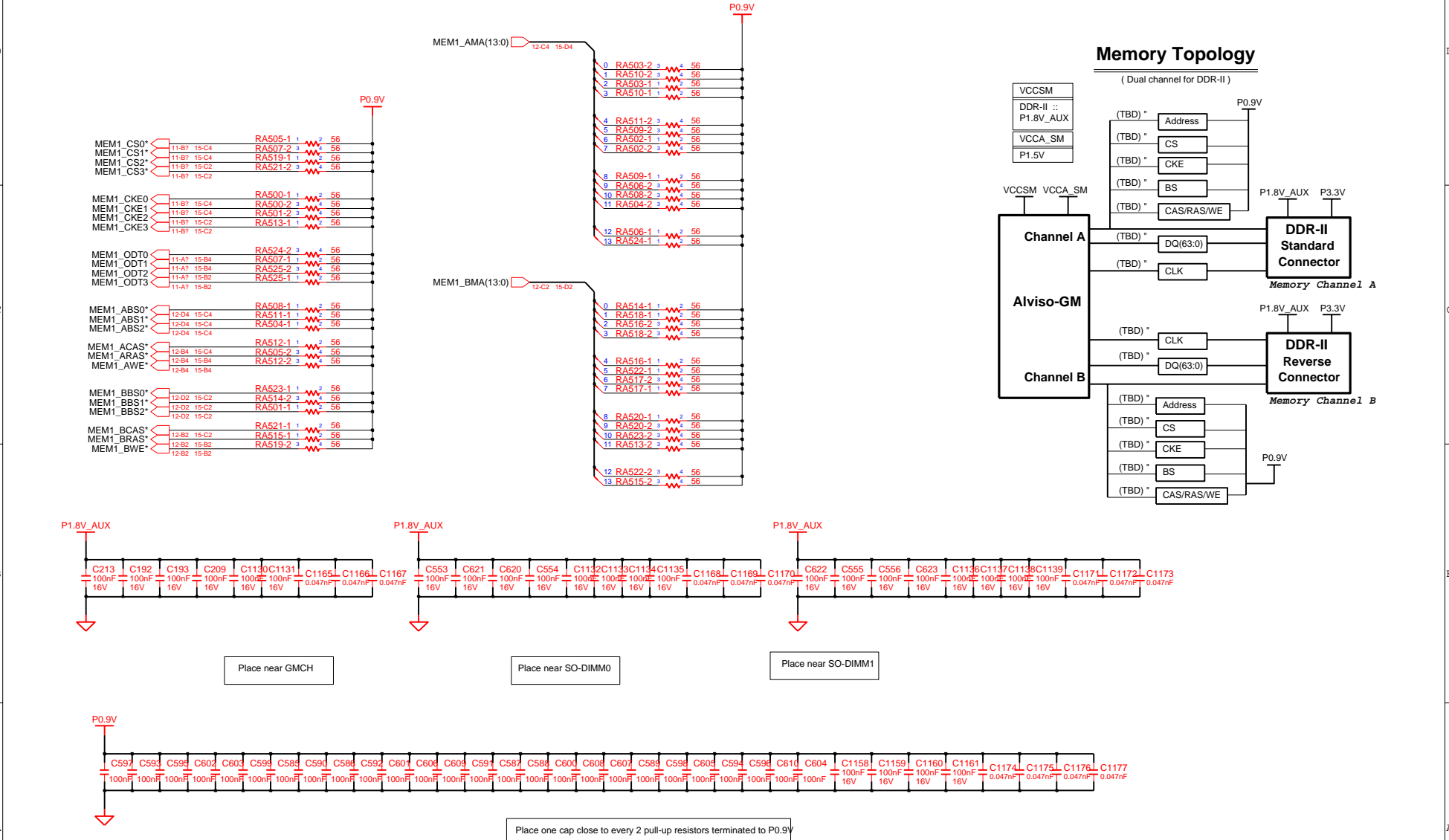
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CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	ALVISO-GMCH(5/5)		PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	14	OF 49

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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	DDR - SODIMM		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	15	OF 49

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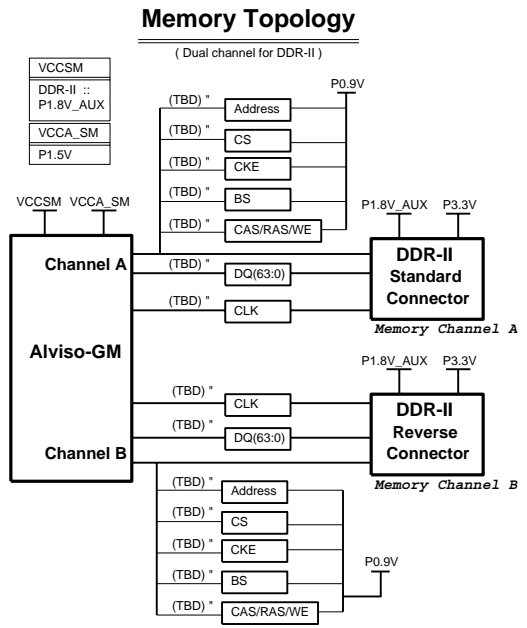


Place near GMCH

Place near SO-DIMM0

Place near SO-DIMM1

Place one cap close to every 2 pull-up resistors terminated to P0.9V



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CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		DDR - TERMINATION	PART NO.
MODULE CODE		LAST EDIT				BA41-00451A
				November 29, 2004 10:05:41 AM	PAGE	16 OF 49

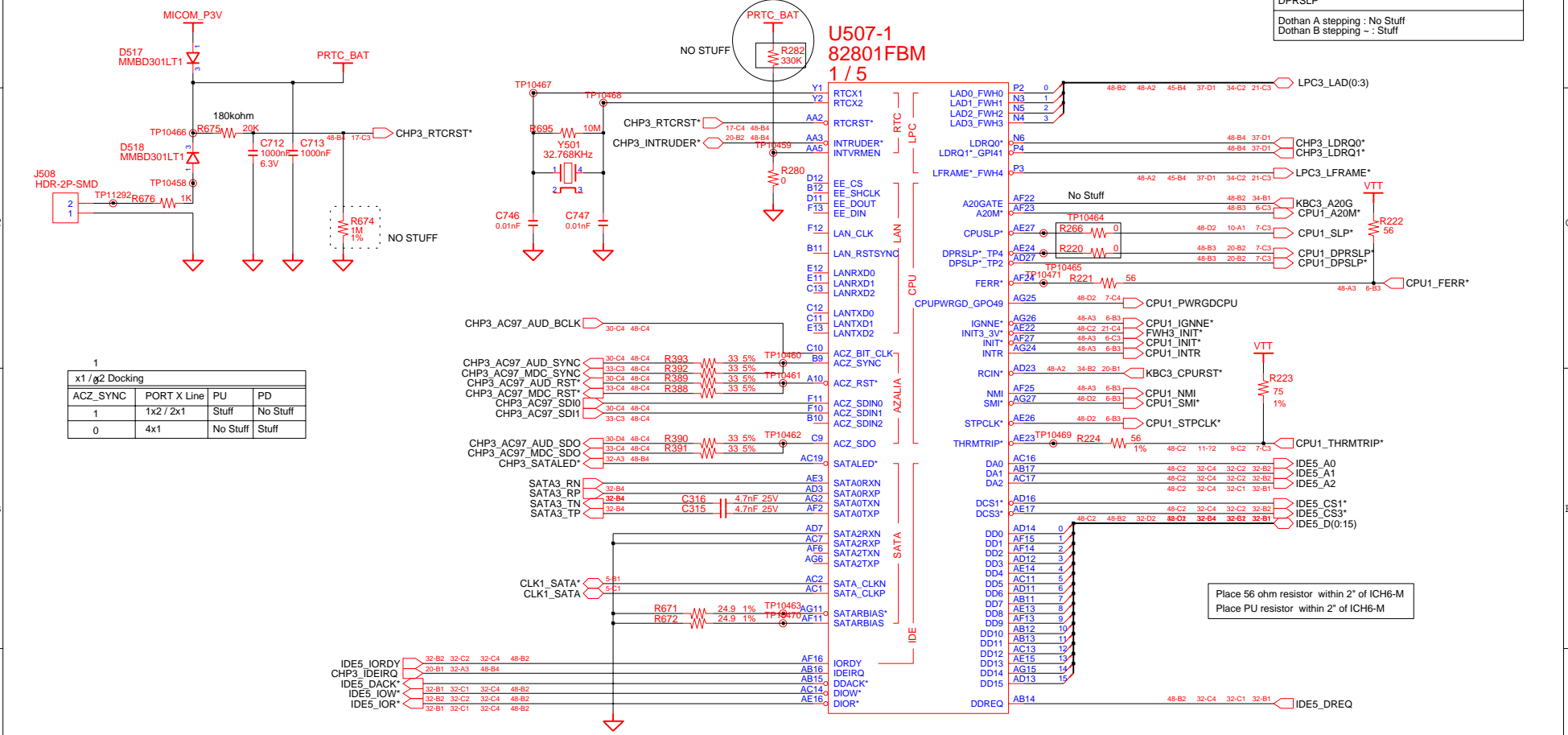


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**CPUSLP\***  
 Dothan A stepping : Stuff resistor on SLP\* of ICH6  
 Dothan B stepping - : Stuff resistor on SLP\* of Alviso

**DPRS LP\***  
 Dothan A stepping : No Stuff  
 Dothan B stepping - : Stuff

Enable intergated P1.5V\_AUX VRM

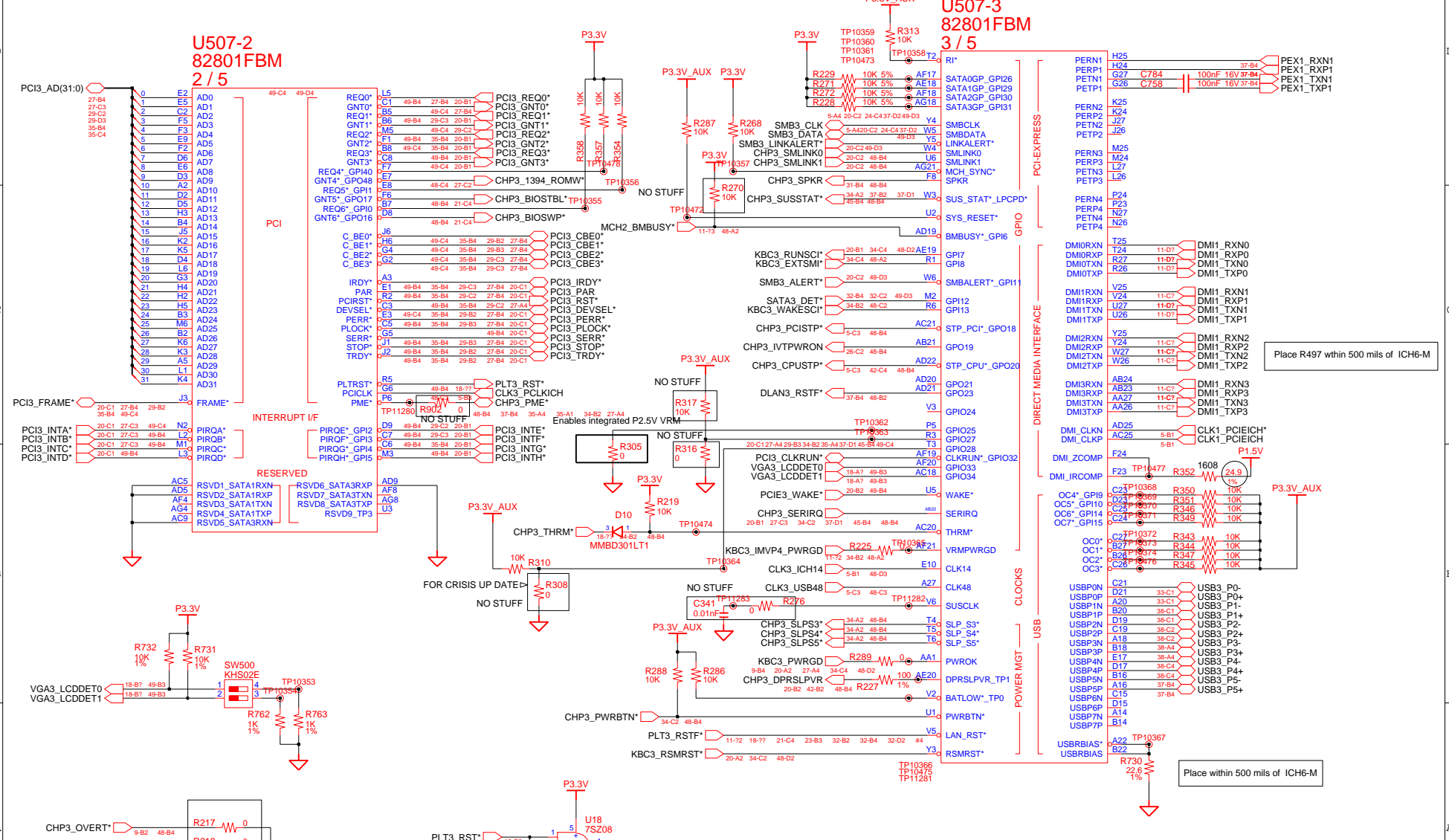


x1 / g2 Docking

ACZ_SYNC	PORT X Line	PU	PD
1	1x2 / 2x1	Stuff	No Stuff
0	4x1	No Stuff	Stuff

DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS	
CHECK	BIN, KK	DEV. STEP	MP		MAIN		
APPROVAL	KIM, DW	REV	1.0		ICH6 - M(1/4)	PART NO.	
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	17	OF	49

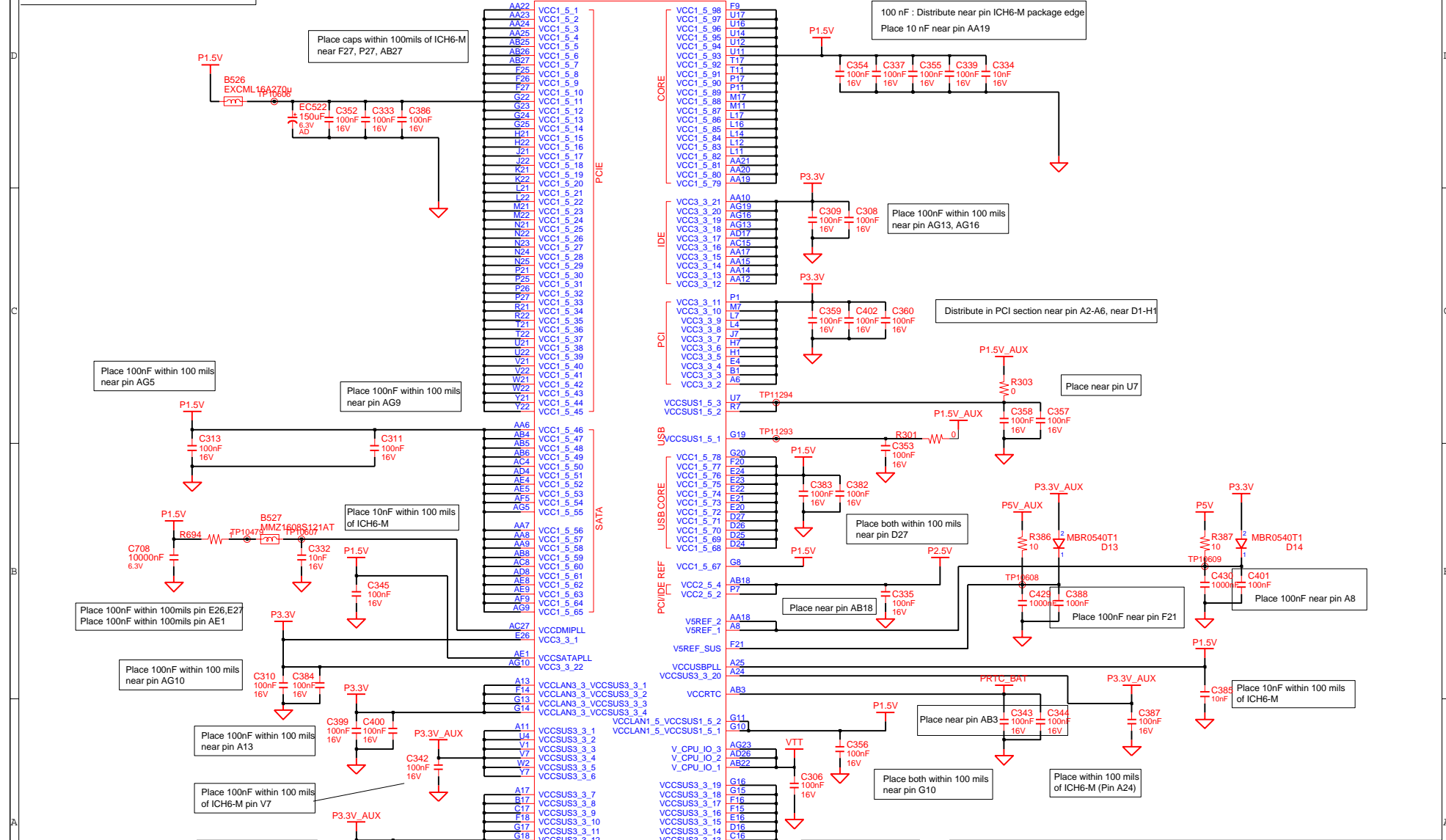
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CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	ICHG - M(2/4)		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			PAGE 18 OF 49

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**U507-4  
 82801FBM  
 4 / 5**



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN ICH6 - M(3/4)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	19	OF 49

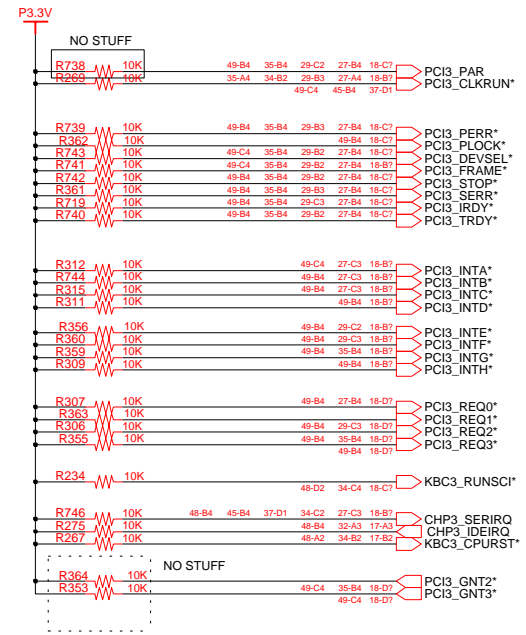
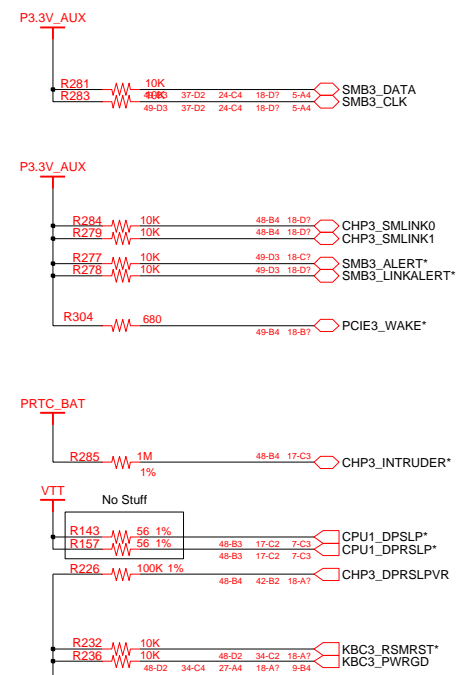
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### ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EPP_DOUT		TBD

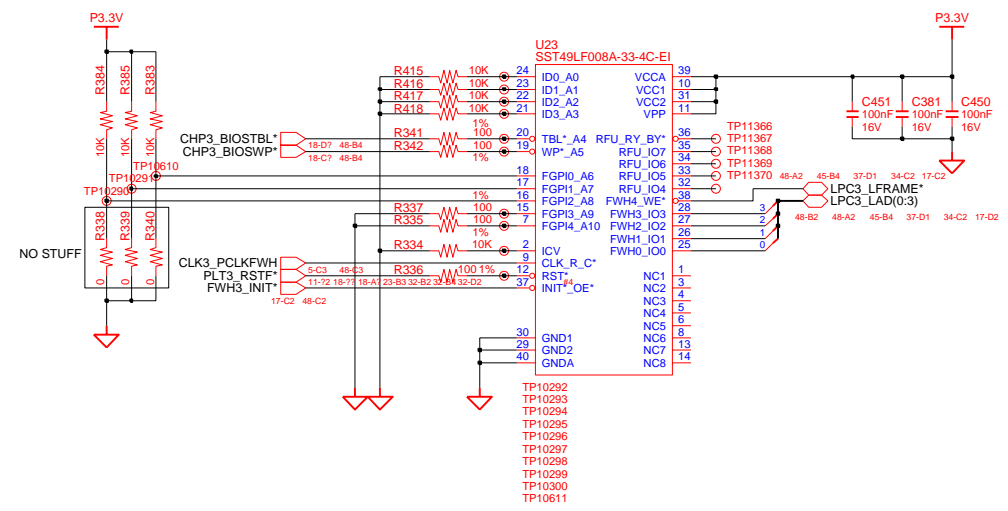
### U507-5 82801FBM 5 / 5

AG22	VSS_172	P22
AG20	VSS_171	P16
AG17	VSS_170	P15
AG14	VSS_169	P14
AG12	VSS_168	P13
AG7	VSS_167	P12
AG3	VSS_166	N17
AG1	VSS_165	N16
AF26	VSS_164	N15
AF12	VSS_163	N14
AF10	VSS_162	N13
AF7	VSS_161	N12
AF3	VSS_160	N11
AF1	VSS_159	N7
AE25	VSS_158	N1
AE21	VSS_157	M27
AE12	VSS_156	M26
AE11	VSS_155	M23
AE10	VSS_154	M15
AE7	VSS_153	M18
AE6	VSS_152	M14
AE2	VSS_151	M13
AD24	VSS_150	M12
AD18	VSS_149	M4
AD15	VSS_148	L25
AD10	VSS_147	L24
AD6	VSS_146	L23
AD2	VSS_145	L15
AD1	VSS_144	L13
AC26	VSS_143	K27
AC23	VSS_142	K26
AC22	VSS_141	K7
AC12	VSS_139	K1
AC10	VSS_138	J25
AC6	VSS_137	J23
AC3	VSS_136	J4
AB19	VSS_135	H27
AB9	VSS_134	H23
AB7	VSS_133	H25
AB2	VSS_132	G21
AB1	VSS_131	G12
AA16	VSS_129	G9
AA13	VSS_128	G7
AA11	VSS_127	G1
AA4	VSS_126	F22
Y27	VSS_125	F19
Y26	VSS_124	F17
Y23	VSS_123	F4
Y6	VSS_122	E27
W25	VSS_121	E25
W24	VSS_120	E18
W23	VSS_119	E15
W1	VSS_117	E14
V27	VSS_116	D22
V26	VSS_115	D20
V23	VSS_114	D19
V4	VSS_113	D14
U24	VSS_112	D13
U23	VSS_111	D10
U15	VSS_110	D1
U13	VSS_108	C22
T27	VSS_107	C20
T26	VSS_106	C18
T23	VSS_105	C14
T16	VSS_104	C4
T15	VSS_103	B25
T14	VSS_102	B24
T13	VSS_101	B23
T12	VSS_100	B21
T7	VSS_99	B19
T1	VSS_98	B15
R25	VSS_97	B13
R24	VSS_96	A26
R23	VSS_95	A23
R17	VSS_94	A21
R16	VSS_93	A19
R15	VSS_92	A15
R14	VSS_91	A12
R13	VSS_90	A9
R12	VSS_89	A7
R11	VSS_88	A4
R4	VSS_87	A1



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		ICH6 - M(4/4)	PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			BA41-00451A
						PAGE 20 OF 49

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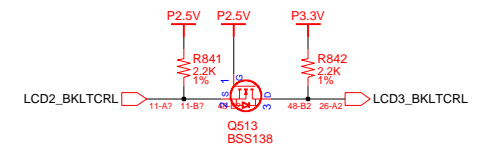
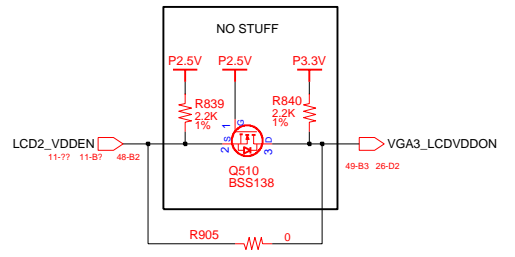
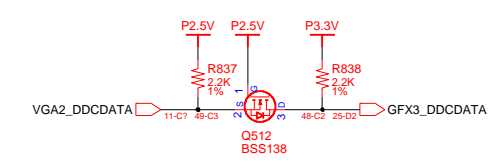
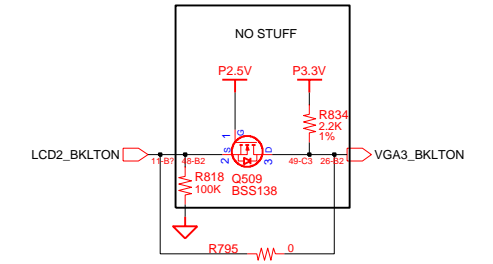
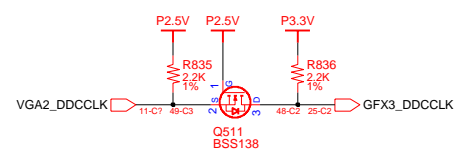


- |    |  |    |                                 |
|----|--|----|---------------------------------|
| 02 | VERIFY REAL MODE                             | 66 | CONFIGURE ADVANCE CACHE REG.    |
| 03 | DISABLE NMI                                  | 6A | DISPLAY EXTERNAL CACHE SIZE     |
| 04 | GET CPU TYPE                                 | 6C | DISPLAY SHADOW MESSAGE          |
| 06 | INIT. SYSTEM H/W                             | 6E | DISPLAY NON-DISPOSABLE SEGMENT  |
| 08 | INIT. CHIPSET REG.                           | 70 | DISPLAY ERROR MESSAGE           |
| 09 | SET IN POST FLAG                             | 72 | CHECK FOR CONFIGURATION ERROR   |
| 0A | INIT CPU.REG                                 | 74 | TEST REAL-TIME CLOCK            |
| 0B | CPU CACHE ON                                 | 76 | CHECK FOR KEYBOARD ERROR        |
| 0C | INIT.CACHE TO POST                           | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE                              | 7E | TEST COPROCESSER IF PRESENT     |
| 0F | ENABLE THE L-BUS IDE                         | 80 | DISABLE ON-BOARD I/O PORT       |
| 10 | INIT. POWER MANAGER                          | 82 | DETECT AND INSTALL EXT.RS232C   |
| 11 | LOAD ALTERNATE REG.                          | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT      |
| 14 | INIT. KEYBOARD CONTROLLER                    | 88 | INIT. BIOS DATA ROM             |
| 16 | CHECK CHECKSUM                               | 8A | INIT.EXTENDED BIOS DATA AREA    |
| 18 | 8254 TIMER INIT.                             | 8C | INIT. FDD CONTROLLER            |
| 1A | 8237 DMA CONTROLLER INIT.                    | 9A | SHADOW OPTION ROMS              |
| 1C | RESET INTERRUPT CONTROLLER                   | 9C | SETUP POWER MANAGEMENT          |
| 20 | TEST DRAM REFRESH                            | 9E | ENABLE H/W INTERRUPT            |
| 22 | TEST 8742 KEYBOARD CONTROLLER                | A0 | SET TIME OF DAY                 |
| 24 | SET ES SEGMENT REG. TO 4GB                   | A4 | INIT. TYPOMATIC RATE            |
| 26 | ENABLE A20                                   | A8 | ERASE F2 PROMPT                 |
| 28 | AUTO SIZING DRAM                             | AA | SCAN FOR F2 KEY STROKE          |
| 32 | COMPUTE THE CPU SPEED                        | AC | ENTER SETUP                     |
| 34 | TEST CMOS RAM                                | AE | CLEAR IN POST FLAG              |
| 38 | SHADOW SYSTEM BIOS ROM                       | B0 | CHECK FOR ERRORS                |
| 3A | AUTO SIZING CACHE                            | B2 | POST DONE-PREPARE TO BOOT O/S   |
| 3C | CONFIGURE ADVANCED CHIPSET REG.              | B4 | ONE BEEP                        |
| 3D | LOAD ALTER REG. WITH CMOS VALUE              | B6 | CHECK PASSWORD (OPTION)         |
| 42 | INIT. INTERRUPT VECTOR                       | B7 | ACPI INIT                       |
| 44 | INIT. BIOS INTERRUPT                         | BA | DMI INIT                        |
| 46 | CHECK ROM COPYRIGHT NOTICE                   | BE | CLEAR SCREEN                    |
| 47 | INIT. I20 SUPPORT IF INSTALLED               | C0 | TRY BOOT WITH INT19             |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS           | D0 | INTERRUPT HANDLER ERROR         |
| 49 | INIT. PCI BUS AND DEVICE                     | D2 | UNKNOWN INTERRUPT ERROR         |
| 4A | INIT. ALL VIDEO BIOS ROM                     | D4 | PENDING INTERRUPT ERROR         |
| 4C | SHADOW VIDEO BIOS ROM                        | D6 | SHUTDOWN 5                      |
| 50 | DISPLAY CPU TYPE AND SPEED                   | D8 | SHUTDOWN ERROR                  |
| 52 | TEST KEYBOARD                                | DA | EXTENDED BLOCK MOVE             |
| 54 | SET KEYCLICK IF ENABLED                      | DC | SHUTDOWN 10                     |
| 56 | ENABLE KEYBOARD                              | 89 | ENABLE NMI                      |
| 58 | TEST FOR UNEXPECTED INTERRUPTS               | 90 | INIT. HDD CONTROLLER            |
| 5A | DISPLAY ' PRESS ..... SETUP'                 | 91 | INIT. LOCAL BUS HDD CONTROLLER  |
| 5C | TEST RAM BETWEEN 512K AND 640K               | 92 | JUMP TO USER PATCH 2            |
| 60 | TEST EXTENDED MEMORY                         | 94 | DISABLE A20 ADDRESS LINE        |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE            | 96 | CLEAR HUGE ES SEGMENT REG.      |
| 64 | JUMP TO USER PATCH 1                         | 98 | SEARCH FOR OPTION ROMS          |

DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN FIRMWARE HUB	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	21	OF 49

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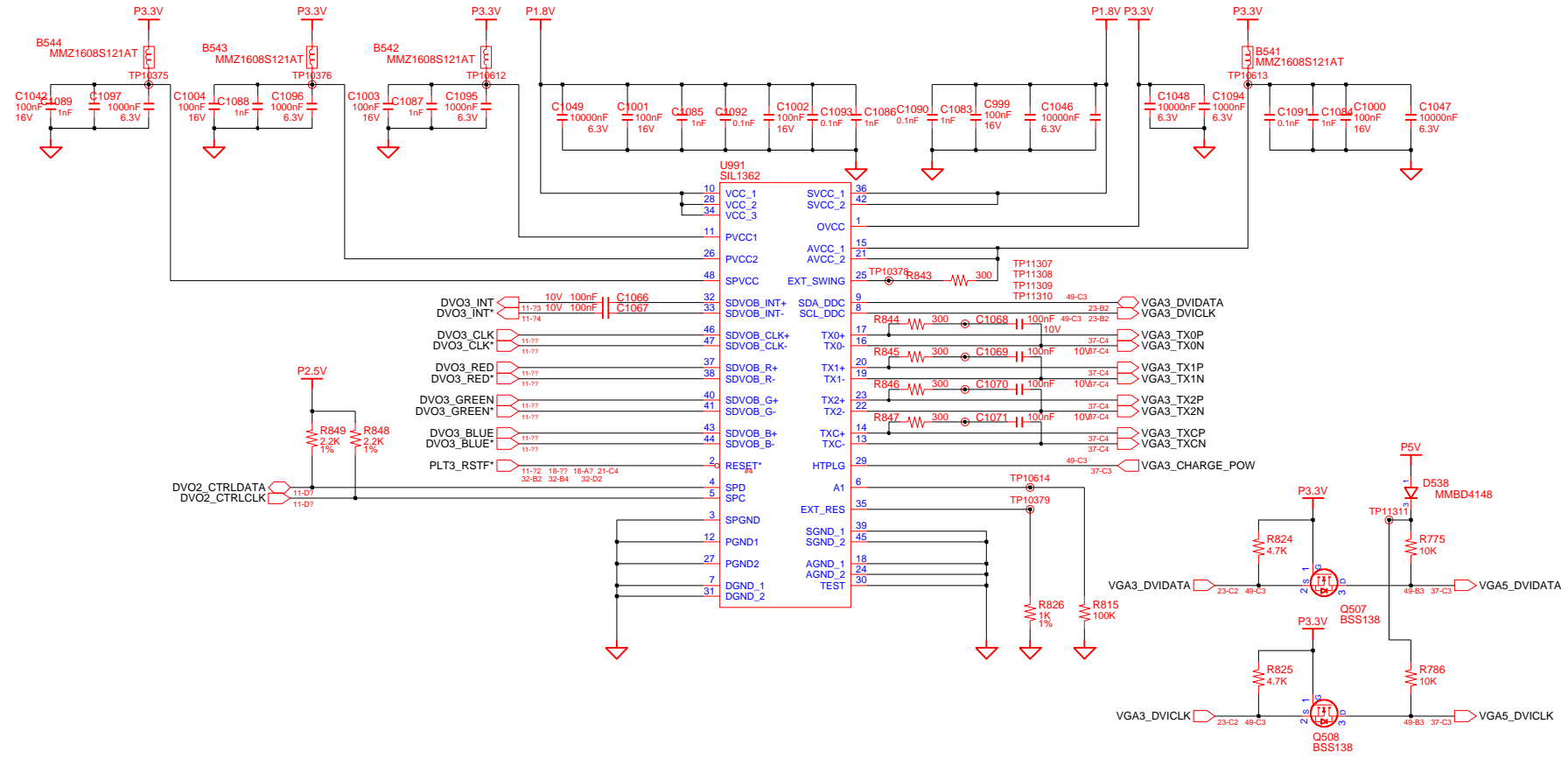
### LVDS Voltage Translation Logic (2.5V -> 3.3V)



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	ATI M24 GRAPHIC CONTROL1/4		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	22	OF 49

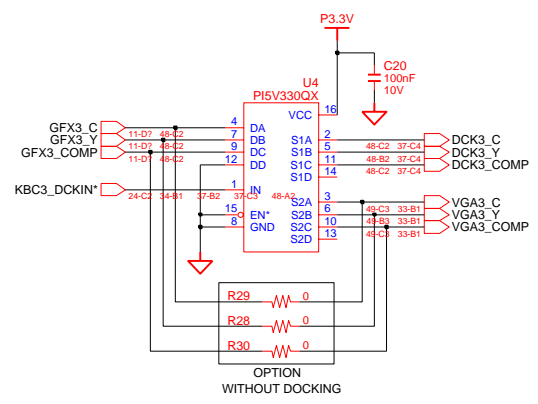
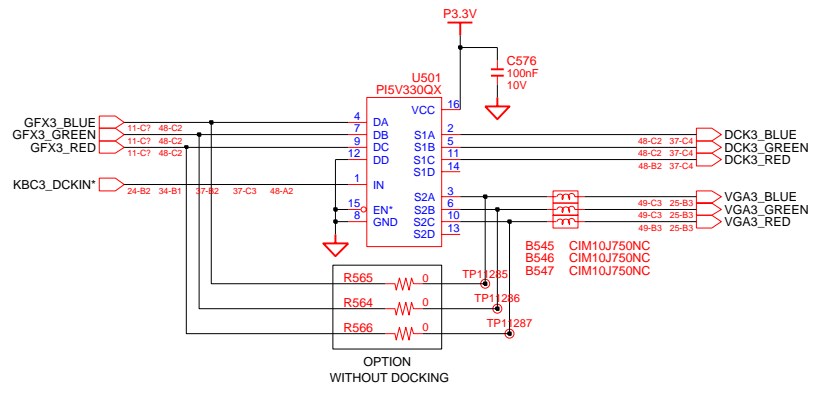
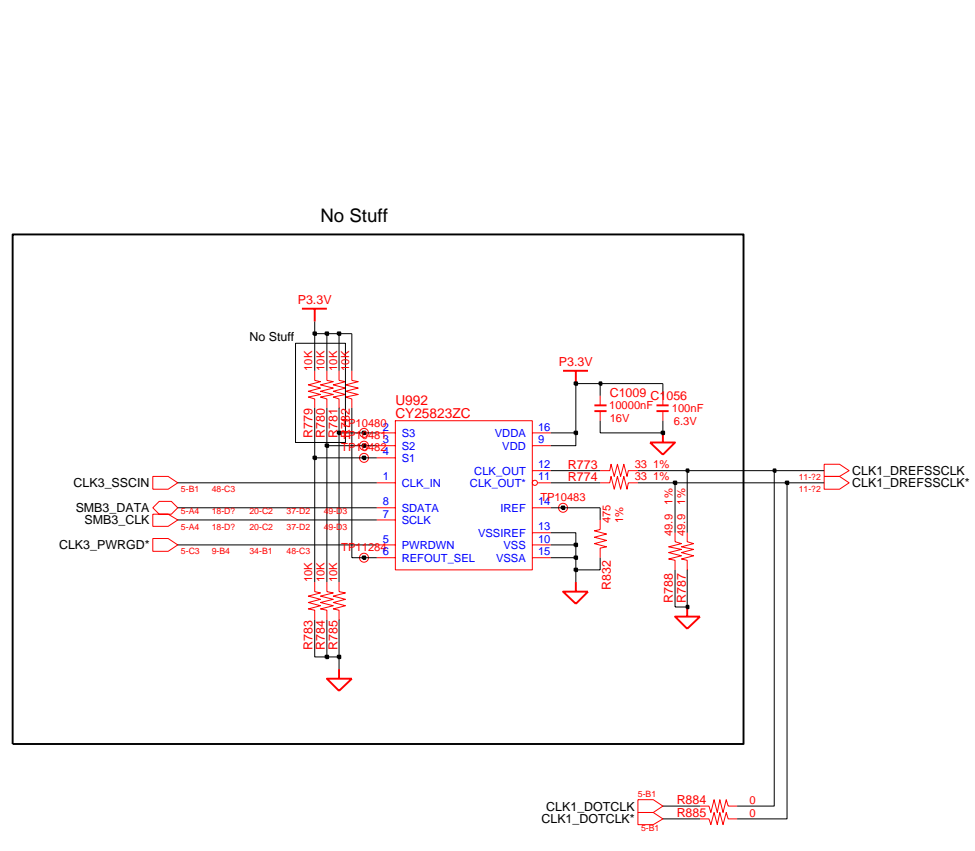
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CHECK	BIN, KK	DEV. STEP	MP	REV	1.0	
APPROVAL	KIM, DW	LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	23	OF 49
MODULE CODE						PART NO. BA41-00451A

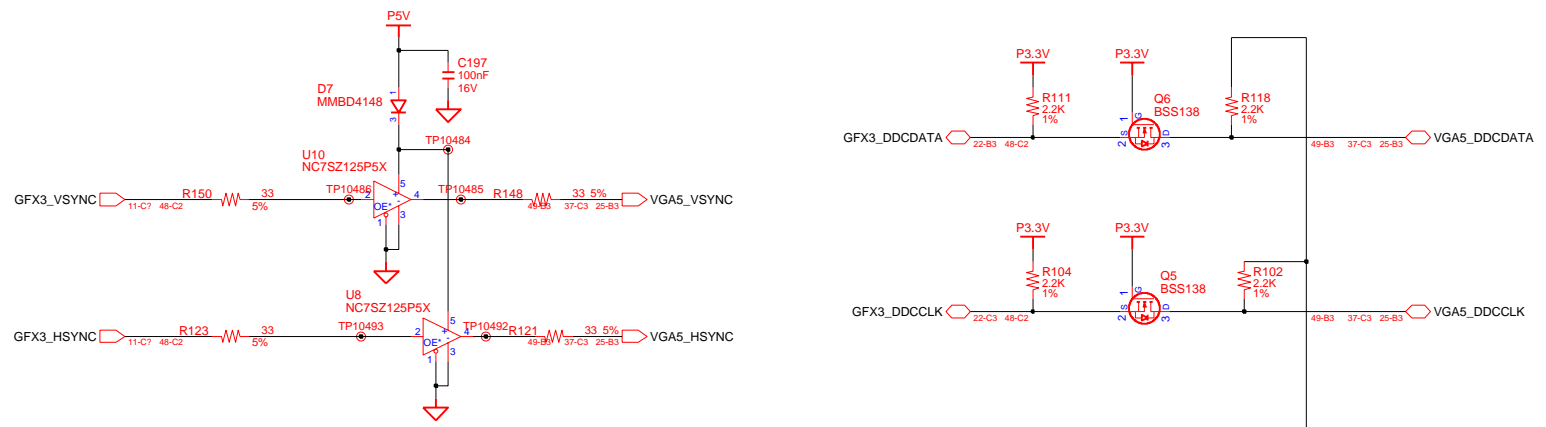
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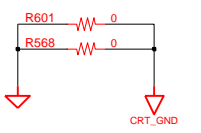
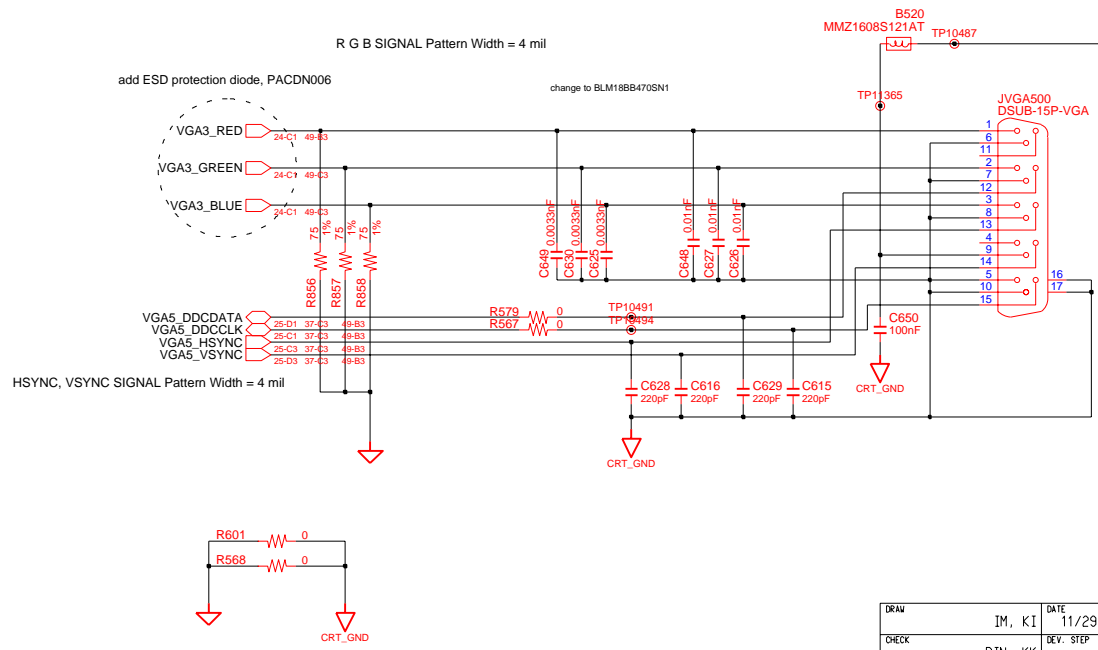
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CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0	ATI M24 GRAPHIC CONTROL3/4		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			PAGE 24 OF 49



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**CRT**

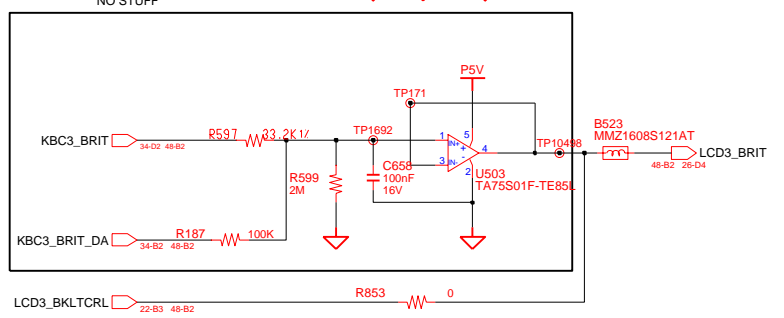
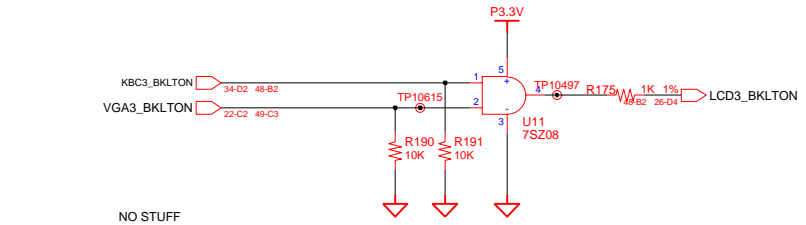
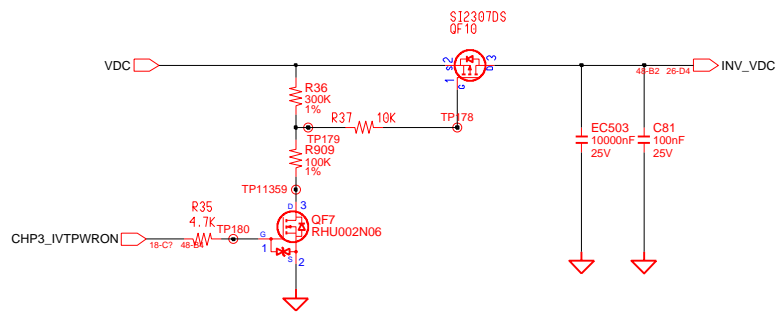
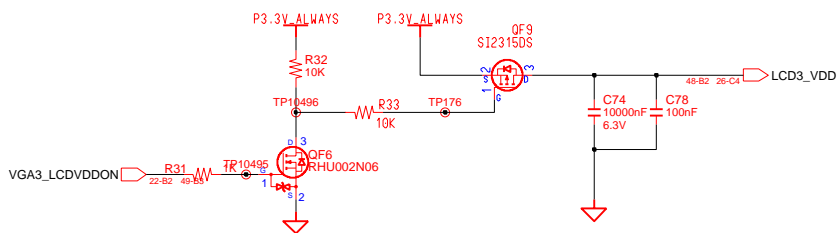
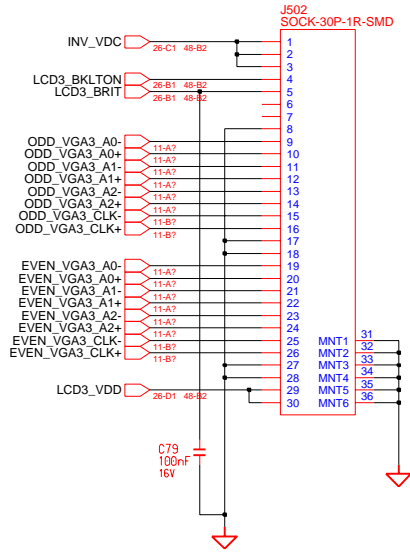


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	CRT PORT/SPREAD SPECTRUM		
APPROVAL	KIM, DW	REV	1.0	PART NO. BA41-00451A		PAGE 25 OF 49
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			

Optional External Thermal Sensor

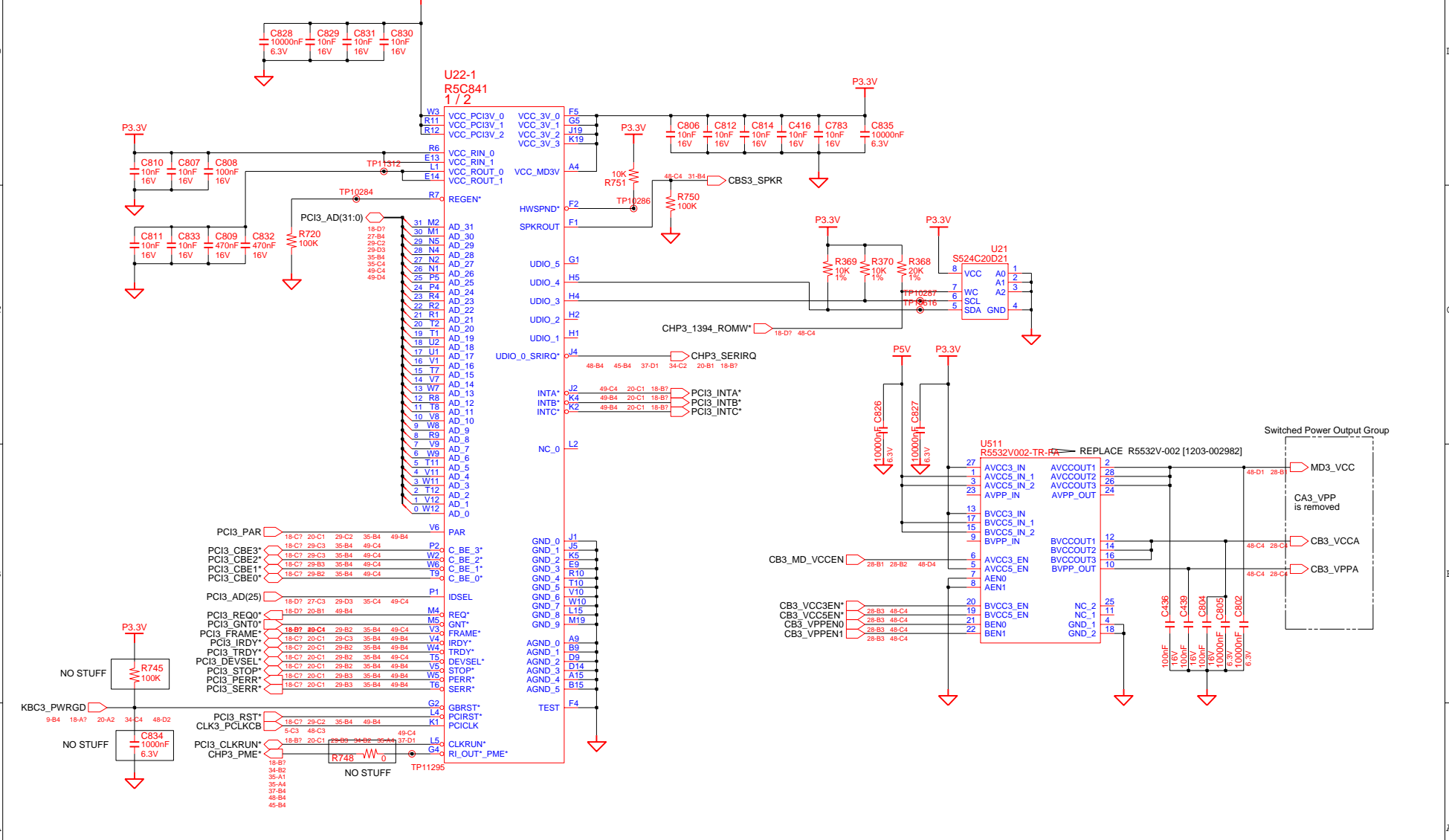
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### LCD CONNECTOR



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	LCD_CONNECTOR / BKLT		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	26	OF 49

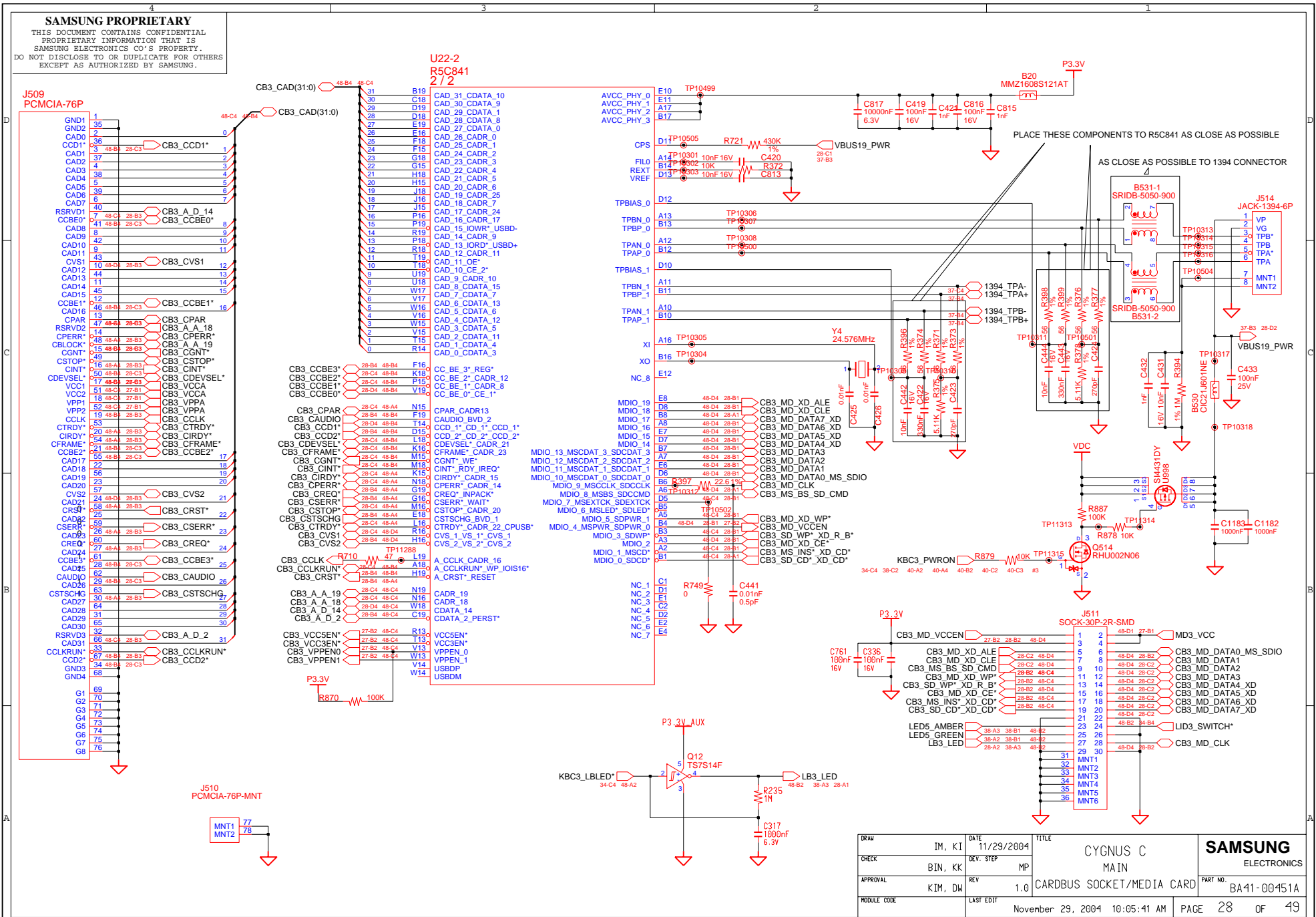
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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		CARDBUS / 1394	PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	27	OF 49

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**U22-2 R5C841 2/2**

31	B19	CAD_31_CDATA_10
30	C18	CAD_30_CDATA_9
29	D18	CAD_29_CDATA_1
28	D18	CAD_27_CDATA_0
27	E19	CAD_28_CDATA_8
26	E16	CAD_26_CADR_0
25	F18	CAD_25_CADR_1
24	F15	CAD_24_CADR_2
23	G18	CAD_23_CADR_3
22	G15	CAD_22_CADR_4
21	H18	CAD_21_CADR_5
20	H15	CAD_20_CADR_6
19	J18	CAD_19_CADR_25
18	J16	CAD_18_CADR_2
17	J15	CAD_17_CADR_24
16	P18	CAD_16_CADR_17
15	P19	CAD_15_IOWR*_USBD+
14	R19	CAD_14_CADR_9
13	P18	CAD_13_IORD*_USBD+
12	R18	CAD_12_CADR_11
11	T19	CAD_11_OE*
10	T16	CAD_10_CE_2*
9	U19	CAD_9_CADR_10
8	U18	CAD_8_CDATA_15
7	V17	CAD_7_CDATA_7
6	V17	CAD_6_CDATA_13
5	W16	CAD_5_CDATA_6
4	W16	CAD_4_CDATA_12
3	W15	CAD_3_CDATA_2
2	W15	CAD_2_CDATA_11
1	T15	CAD_1_CDATA_4
0	R14	CAD_0_CDATA_3

28-B4 48-B4	F16	CC_BE_3*_REG*
28-C4 48-B4	P15	CC_BE_2*_CADR_12
28-D4 48-B4	V19	CC_BE_1*_CADR_8
28-E4 48-B4	V19	CC_BE_0*_CE_1*

28-C4 48-A4	N15	CPAR_CADR13
28-B4 48-B4	F19	CAUDIO_BVD_2
28-D4 48-B4	T14	CCD_1*_CD_1*_CCD_2*
28-C4 48-B4	L18	CCD_2*_CD_1*_CCD_2*
28-C4 48-B4	K18	CDEVSEL*_CADR_21
28-D4 48-B4	M15	CFRAME*_CADR_23
28-C4 48-B4	M15	CGNT*_WE*
28-C4 48-B4	M18	CGNT*_ROY_IREQ*
28-C4 48-A4	K15	CIRDY*_CADR_15
28-C4 48-A4	G15	CPERR*_CADR_14
28-C4 48-A4	G15	CREQ*_INPACK*
28-C4 48-A4	G16	CSERR*_WAIT*
28-C4 48-A4	M18	CSTOP*_CADR_20
28-C4 48-A4	E18	CSTSCHG_BVD_1
28-C4 48-A4	L16	CTRDY*_CADR_22_CPUSB*
28-C4 48-D4	R16	CVS_1_VS_1*_CVS_1
28-B4 48-D4	H16	CVS_2_VS_2*_CVS_2

28-C4 48-A4	L19	A_CCLK_CADR_16
28-B4 48-B4	A18	A_CCLKRUN*_WP_IOIS16*
28-B4 48-B4	H19	A_CRST*_RESET

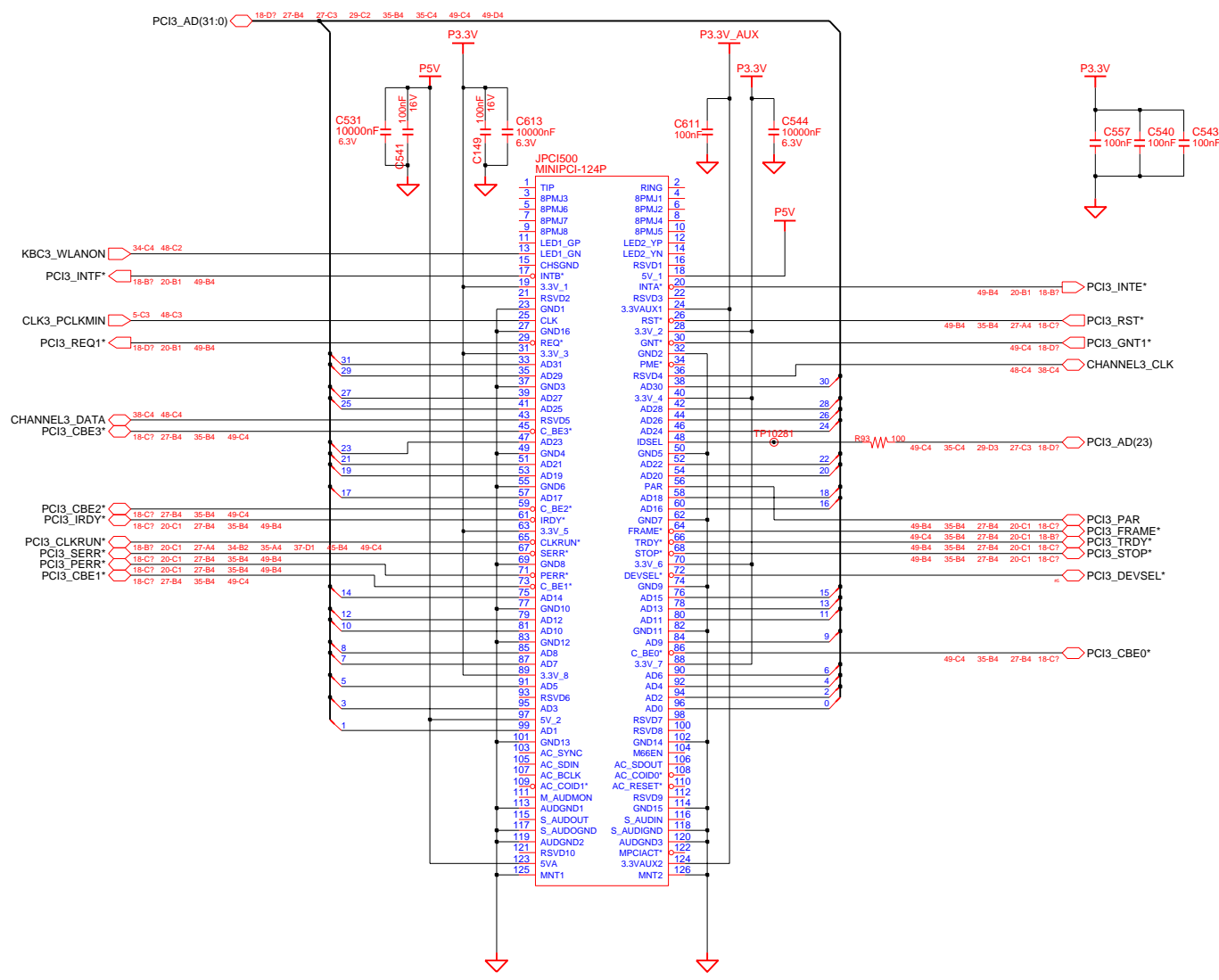
28-C4 48-C4	R13	VCCSEN*_R13
28-B4 48-C4	T13	VCCSEN*_T13
28-B4 48-C4	V13	VPPEN_0
28-B4 48-C4	V13	VPPEN_1
28-B4 48-A4	V14	USBDP
28-B4 48-A4	V14	USBDM

28-C4 48-C4	R13	CADR_19
28-C4 48-C4	R13	CADR_18
28-D4 48-C4	W18	CDATA_14
28-B4 48-C4	C19	CDATA_2_PERST*

DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN	PART NO.	BA1-00451A
CHECK	BIN, KK	DEV. STEP	MP				
APPROVAL	KIM, DW	REV	1.0				
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	28	OF	49

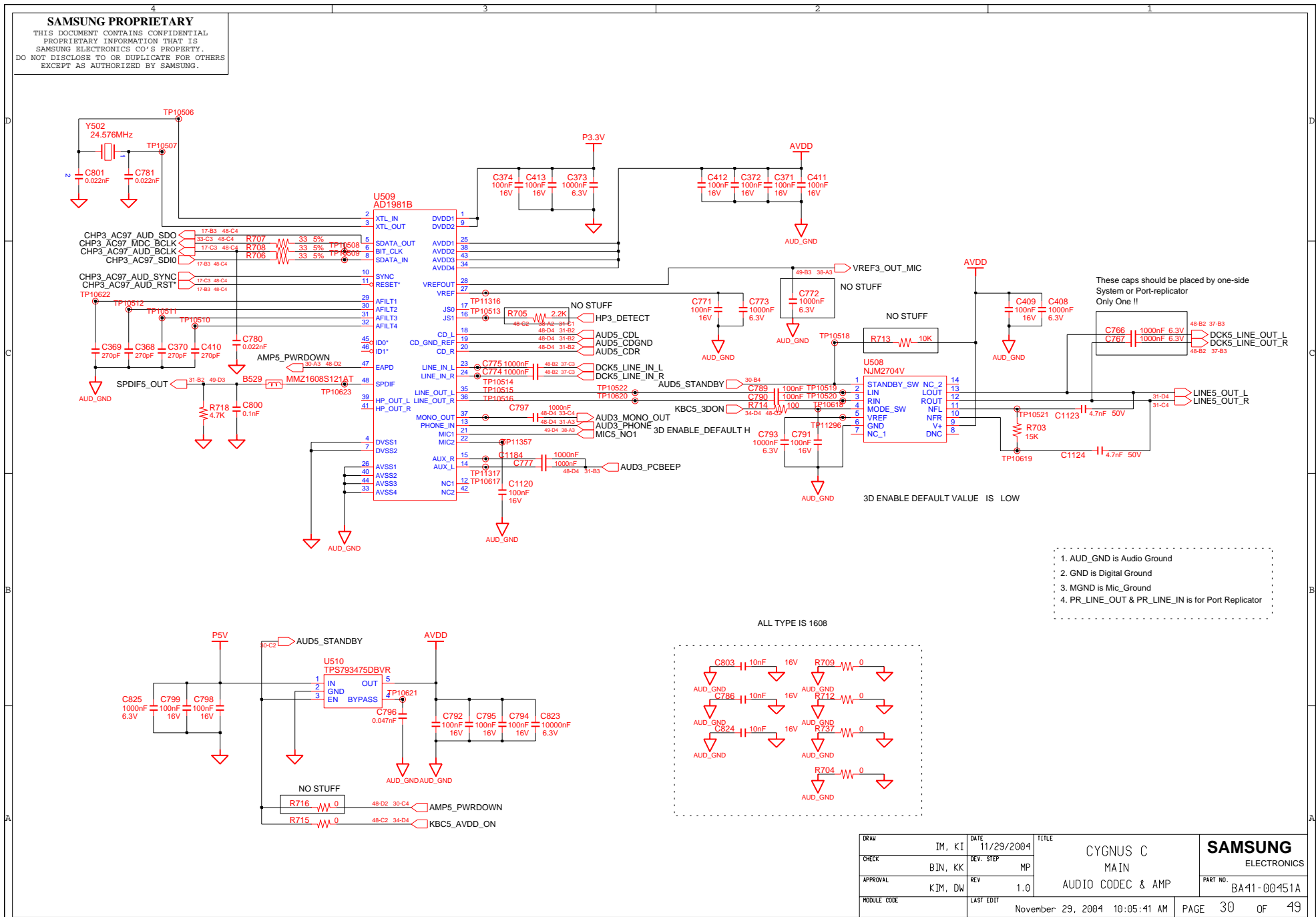
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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN MINI PCI	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	29	OF 49

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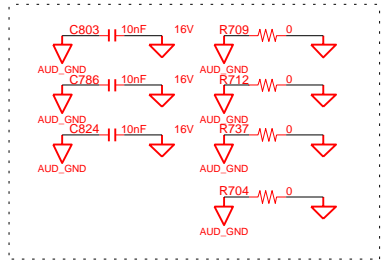
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These caps should be placed by one-side System or Port-replicator Only One !!

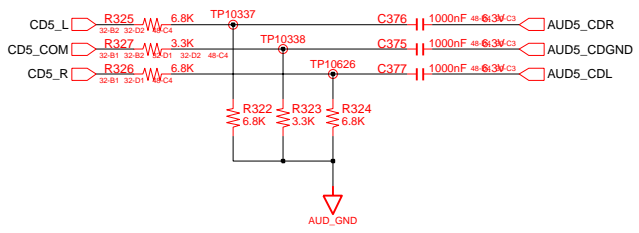
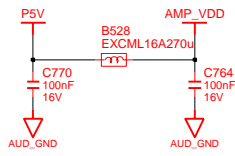
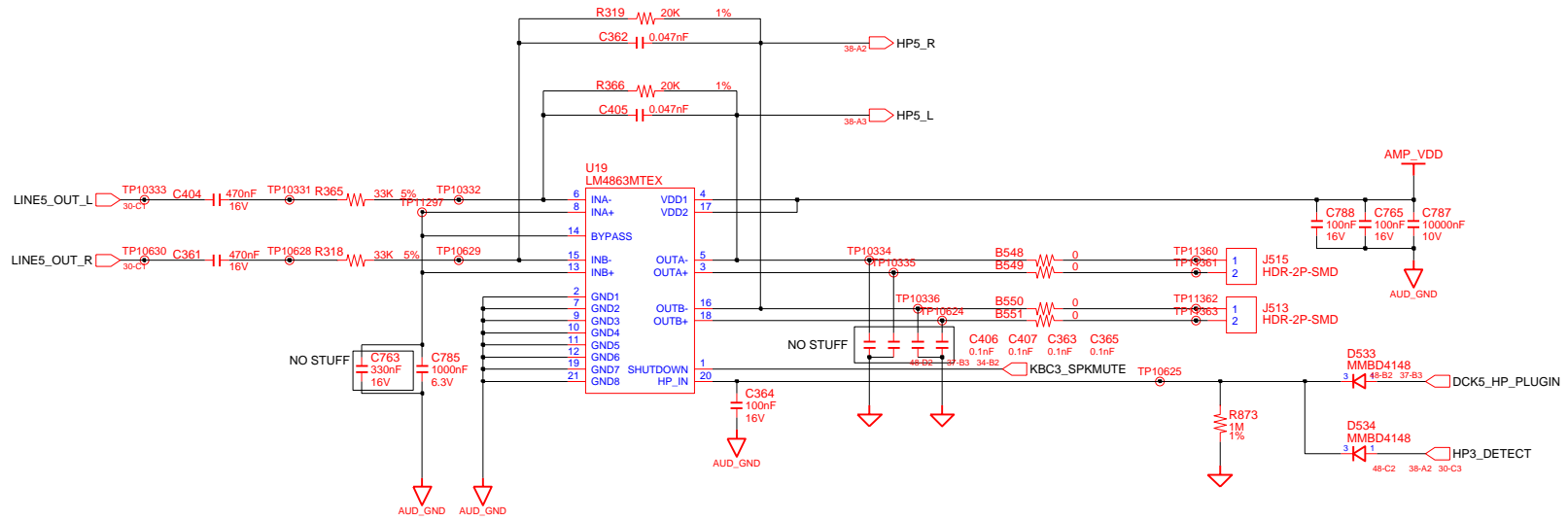
- 1. AUD\_GND is Audio Ground
- 2. GND is Digital Ground
- 3. MGN is Mic\_Ground
- 4. PR\_LINE\_OUT & PR\_LINE\_IN is for Port Replicator

ALL TYPE IS 1608

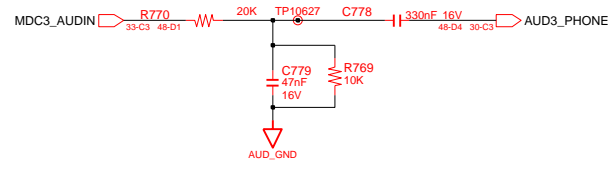
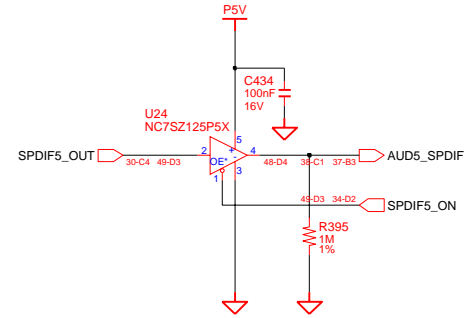
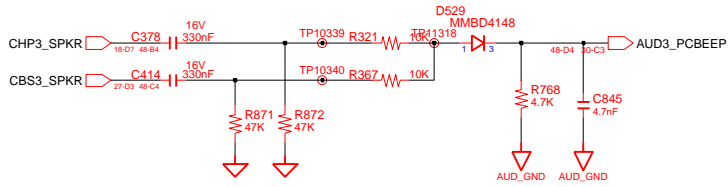


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	AUDIO CODEC & AMP		PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	30	OF 49

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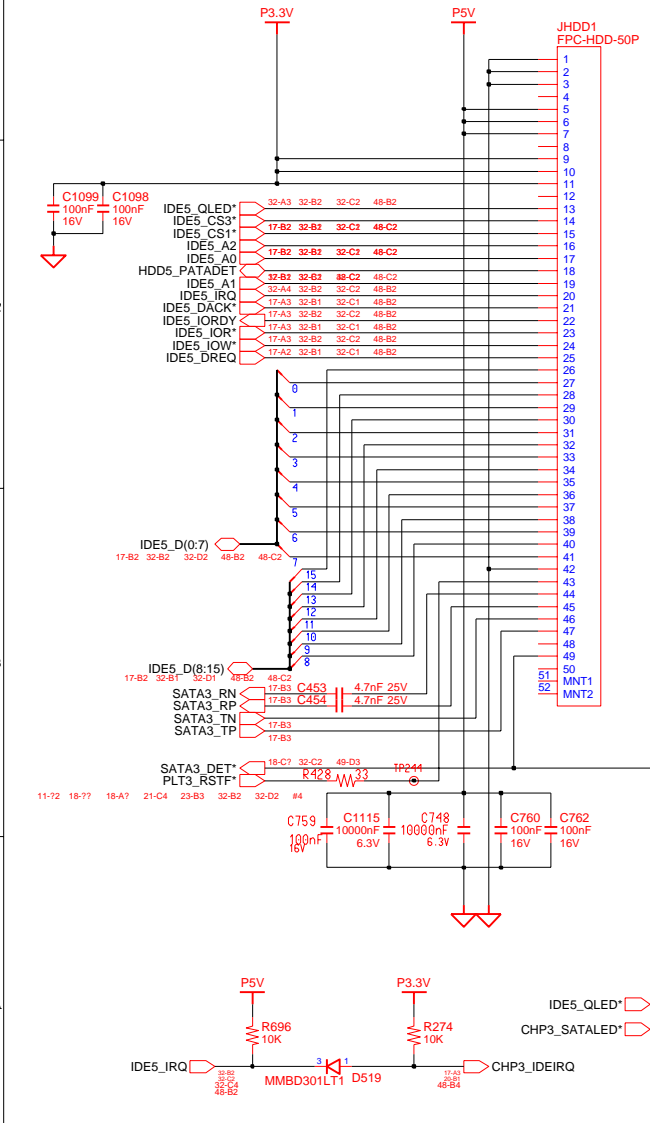
1. HP\_IN SHOULD BE USED FOR PORT\_REPLICATOR JACK SENSE AND SPDIF\_JACK SENSE  
 2. PR\_JS SHOULD BE IN MAIN B'D  
 PR\_JS SHOULD HAVE 100kohm RESISTOR WITH Pull\_Down  
 3. PORT\_REPLICATOR SHOULD HAVE 10Kohm with Pull\_up



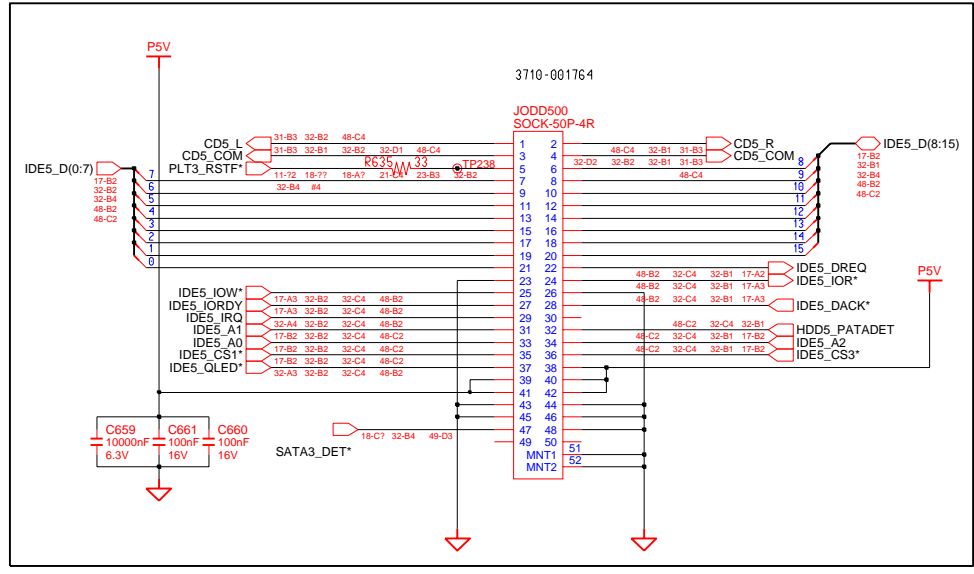
DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	AUDIO CODEC & AMP		PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	31	OF 49

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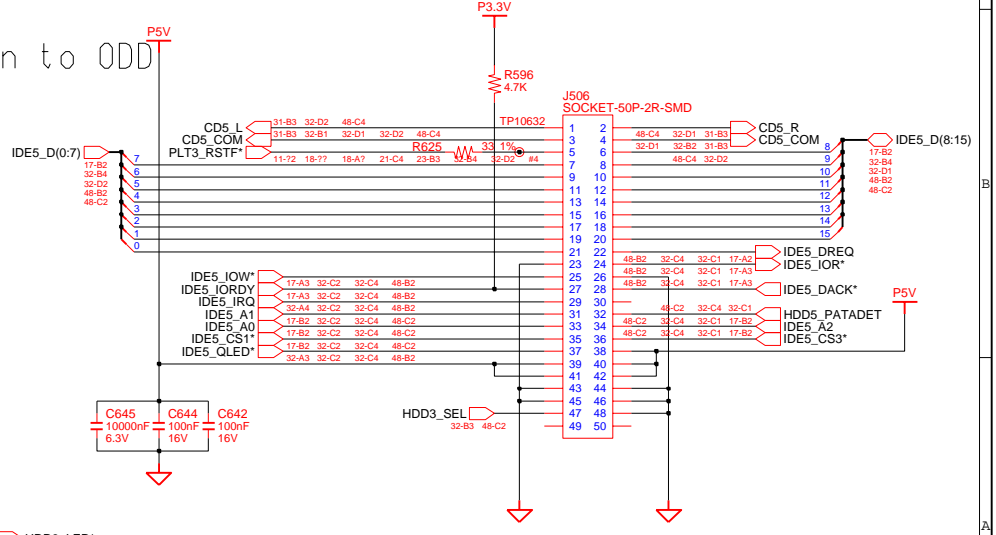
Main to HDD



NO STUFF



Main to ODD

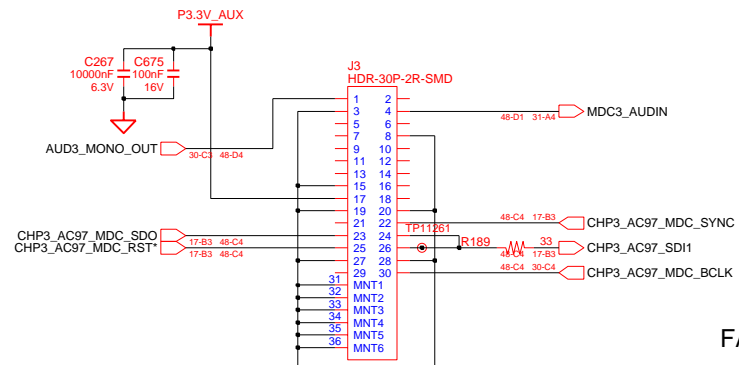


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	HDD & ODD CONNECTOR		PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	32	OF 49

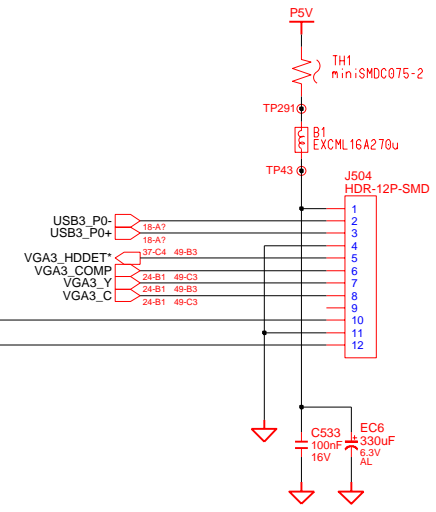


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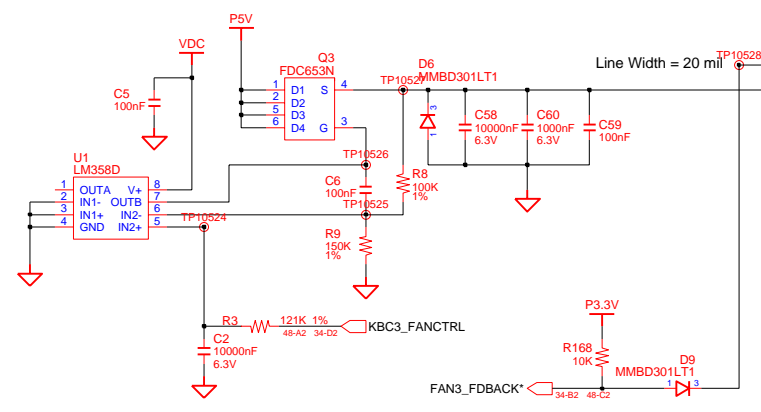
## MDC Connector



## TV-OUT(S-VHS)



## FAN Control Logic

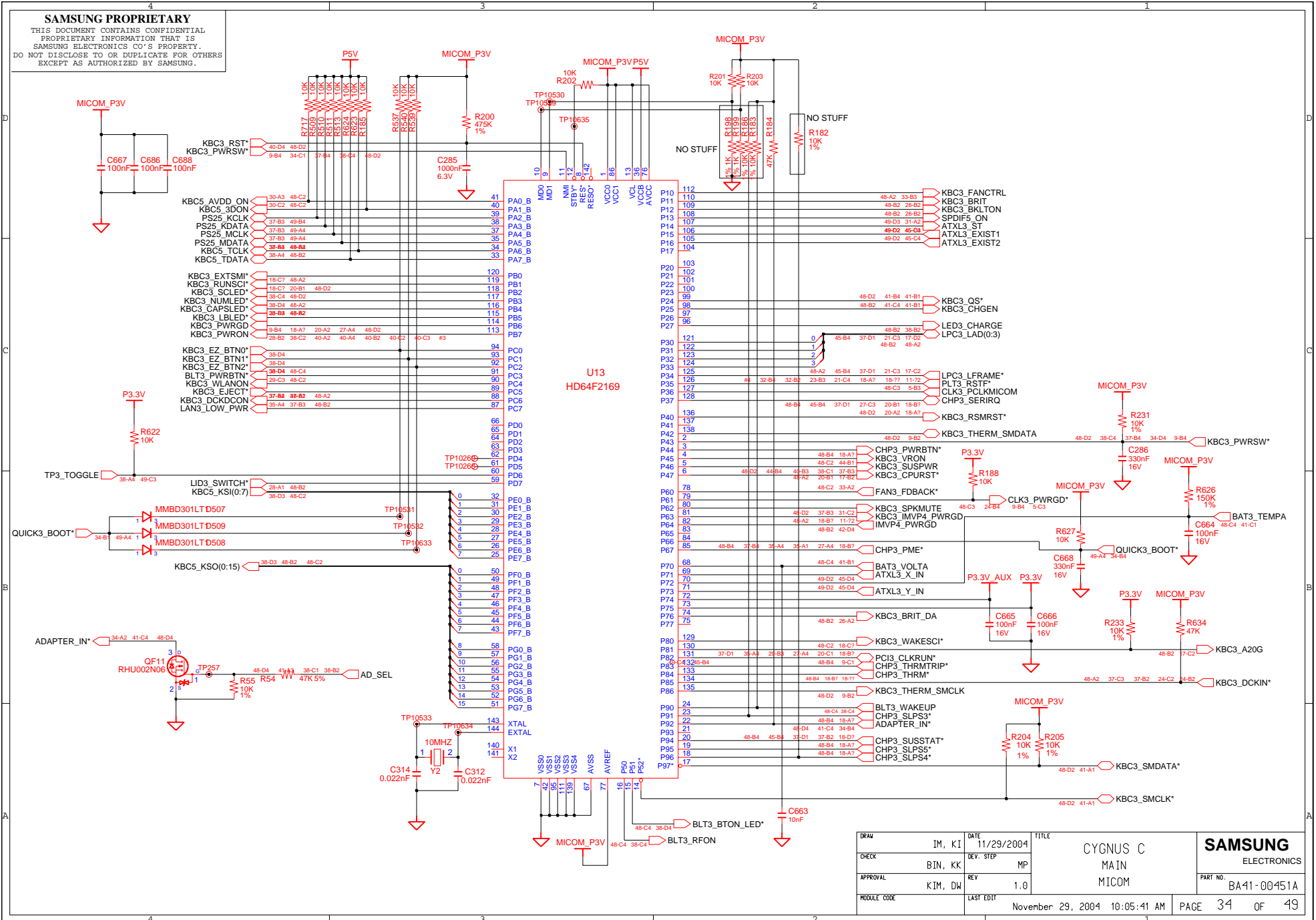


M1 HEAD DIA LENGTH

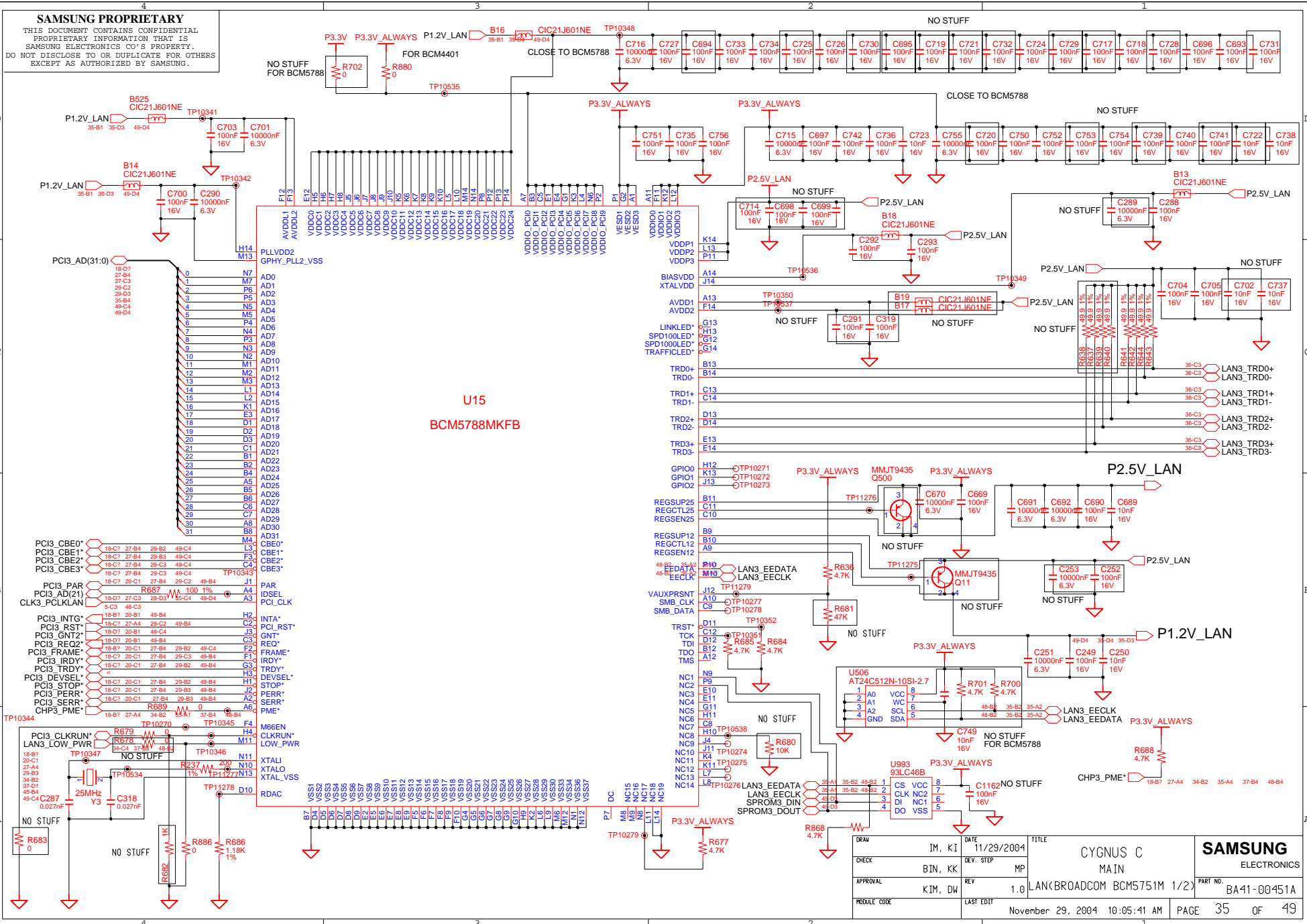
DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	MDC MODEM / TV-OUT(SVHS)		PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	33	OF 49

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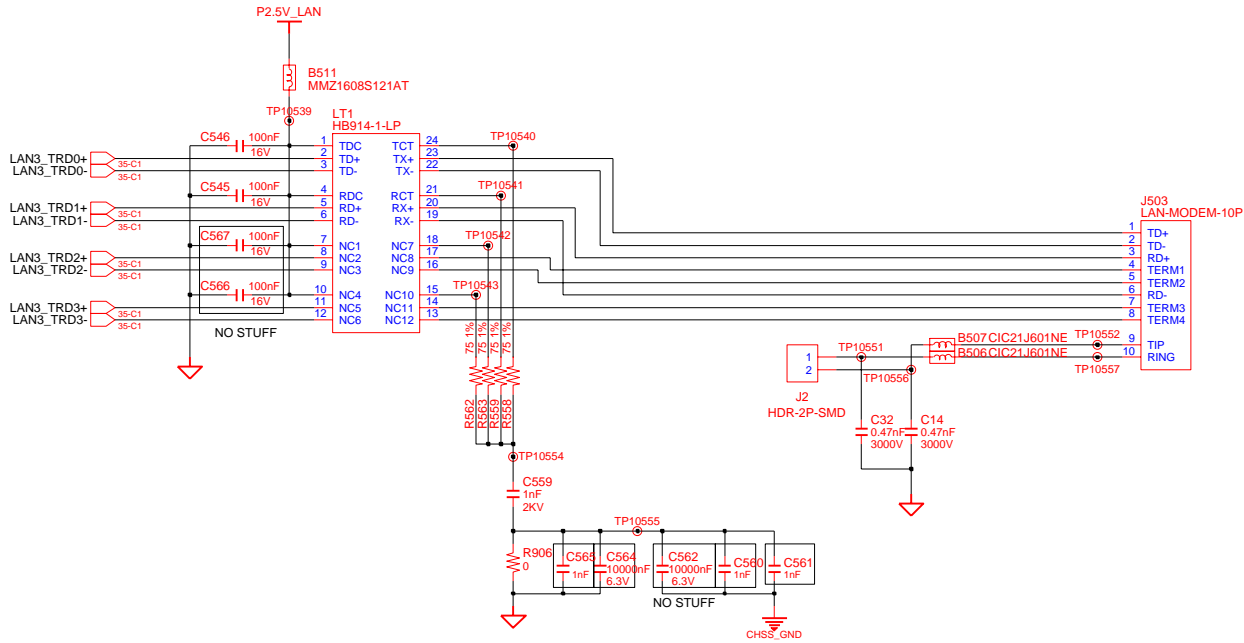


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		MICOM	
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	34 OF 49	



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	LAN(BROADCOM BCM5751M 1/2)		PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	35	OF 49

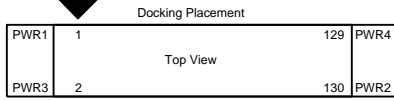
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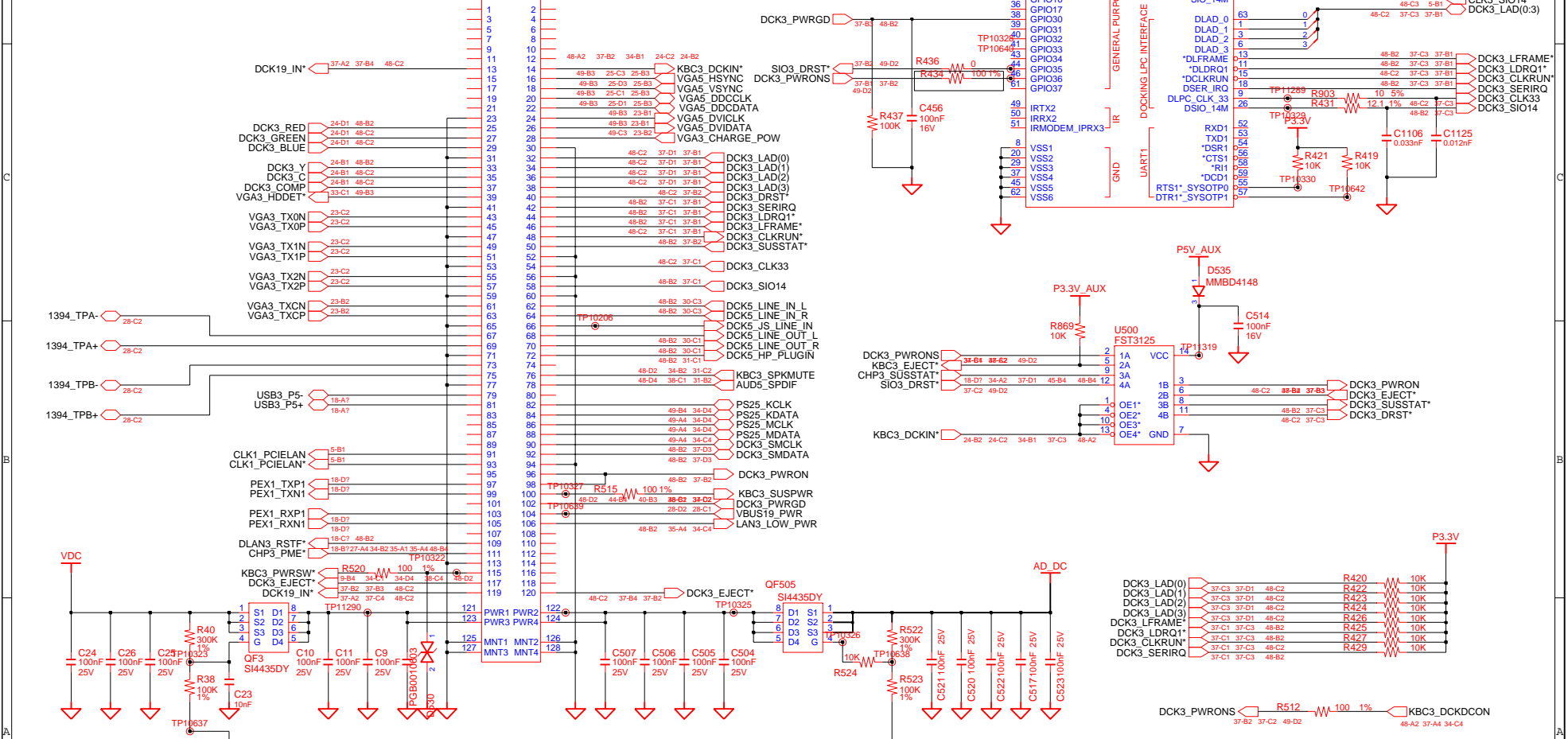
DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	PART NO.	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN	LAN(BROADCOM BCM5751M 2/2)		
APPROVAL	KIM, DW	REV	1.0			BA41-00451A	
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	36	OF	49

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# DOCKING CONNECTOR (130PIN)



## J1 SOCK-DOCKING-120P



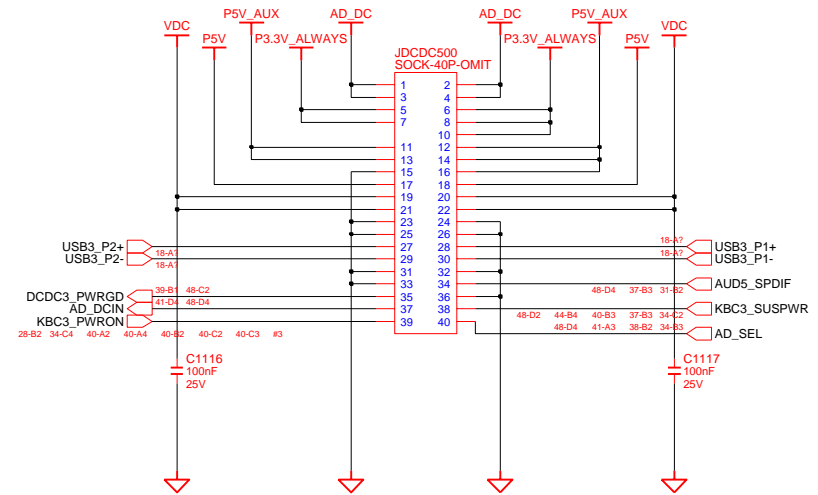
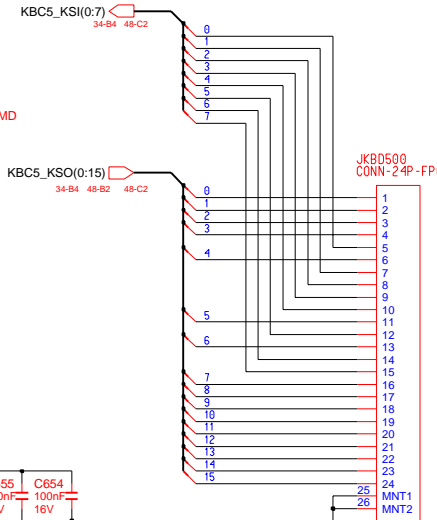
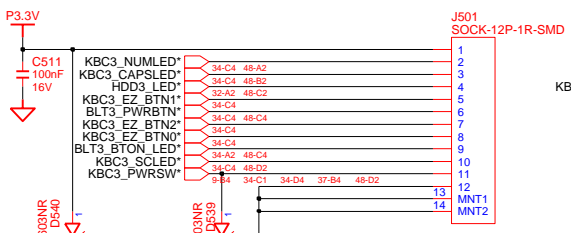
DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	DOCKING CONNECTOR		PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	37	OF 49

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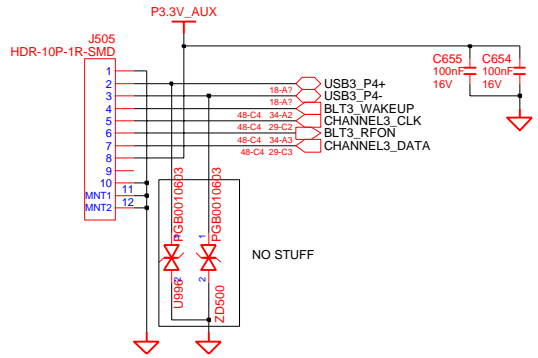
KEYBOARD

Main to DC/DC BOARD

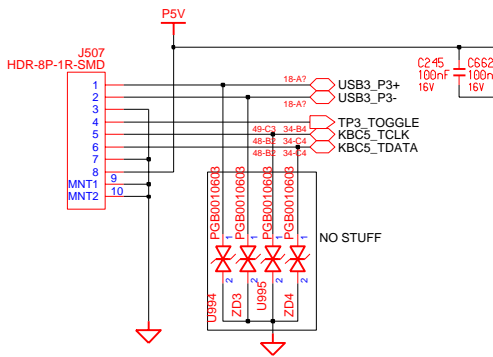
MAIN TO ON-TOP



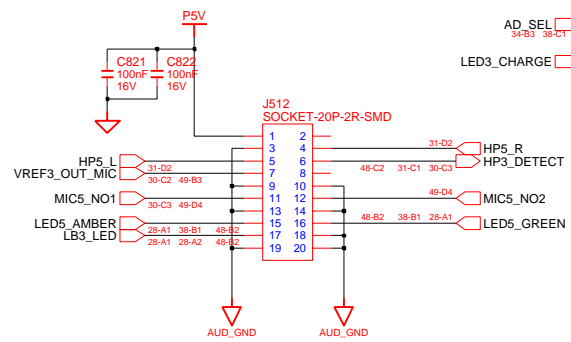
BLUETOOTH CONNECTOR



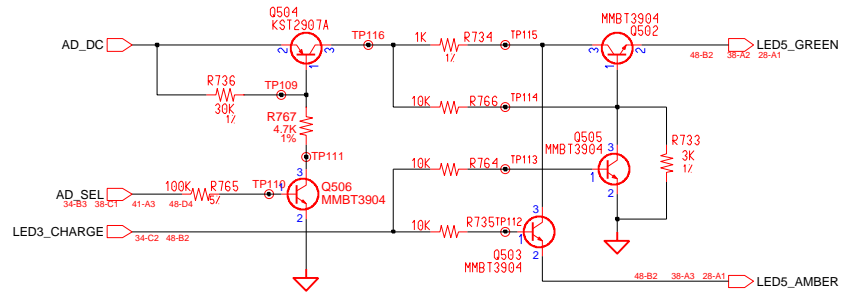
TOUCHPAD CONNECTOR



AUDIO CONNECTOR



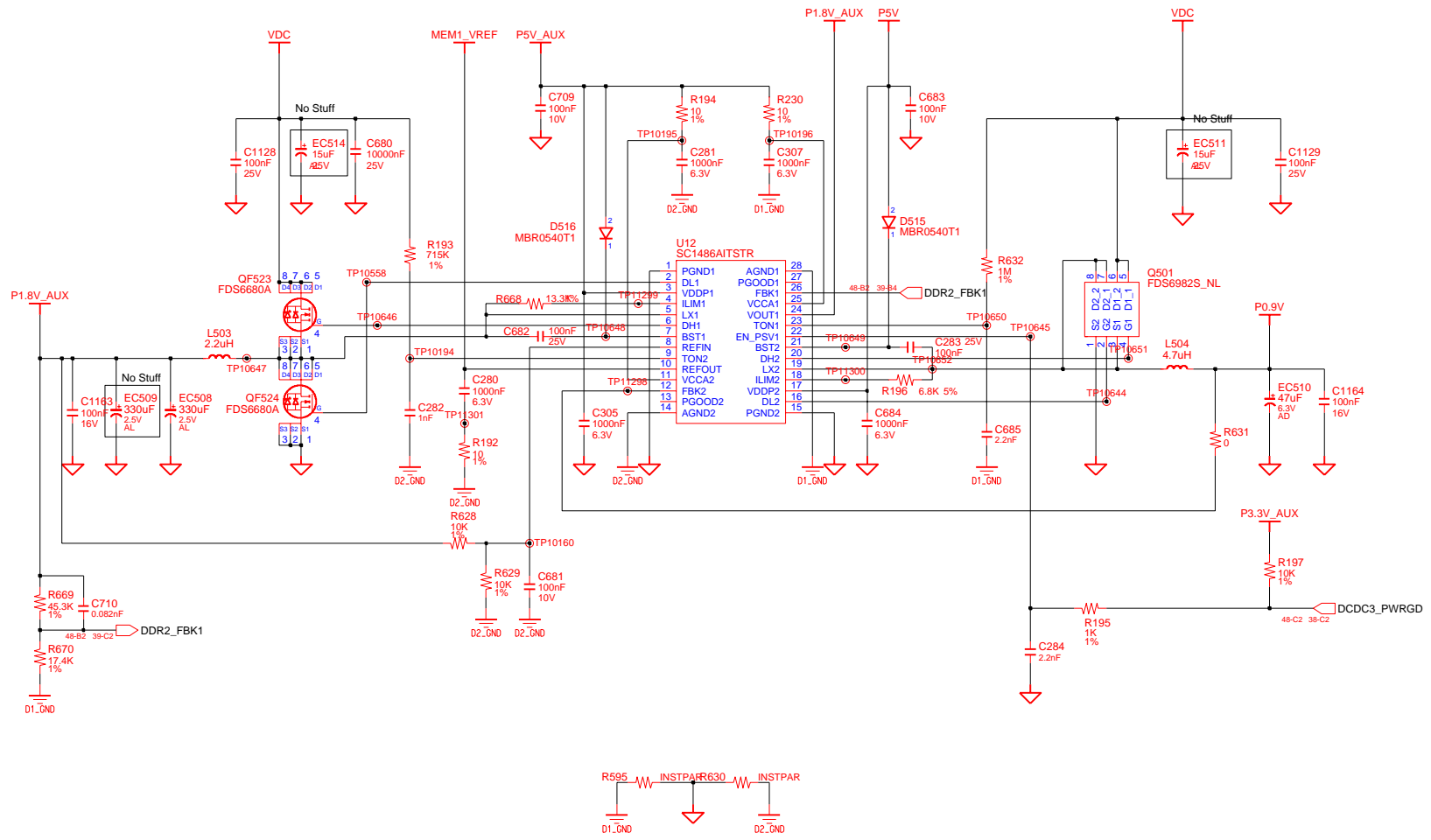
ADAPTER IN/CHARGING LED



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN B'D TO B'D CONNECTOR	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	38 OF 49	

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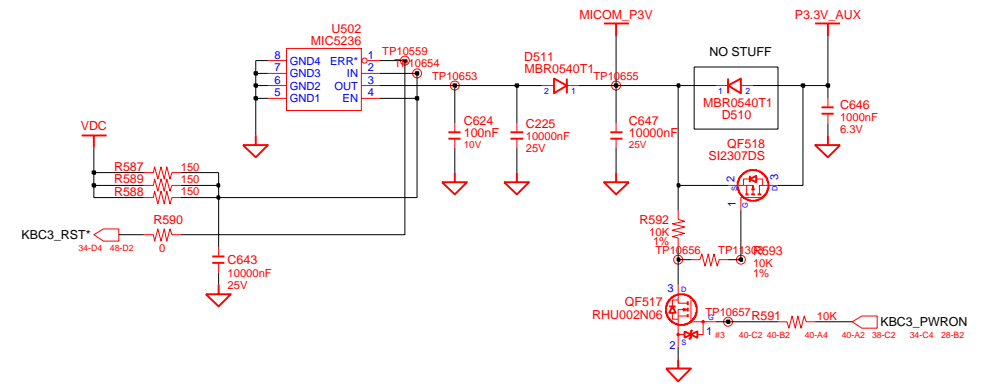
# DDR Power



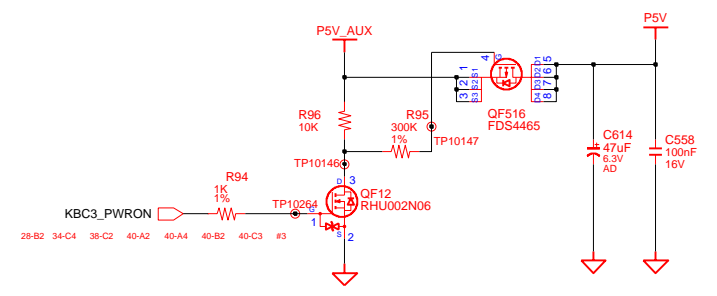
DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN DDR POWER	<b>SAMSUNG</b> ELECTRONICS	
CHECK	BIN, KK	DEV. STEP	MP	PART NO.			BA41-00451A
APPROVAL	KIM, DW	REV	1.0	LAST EDIT			November 29, 2004 10:05:41 AM
MODULE CODE				PAGE			39 OF 49

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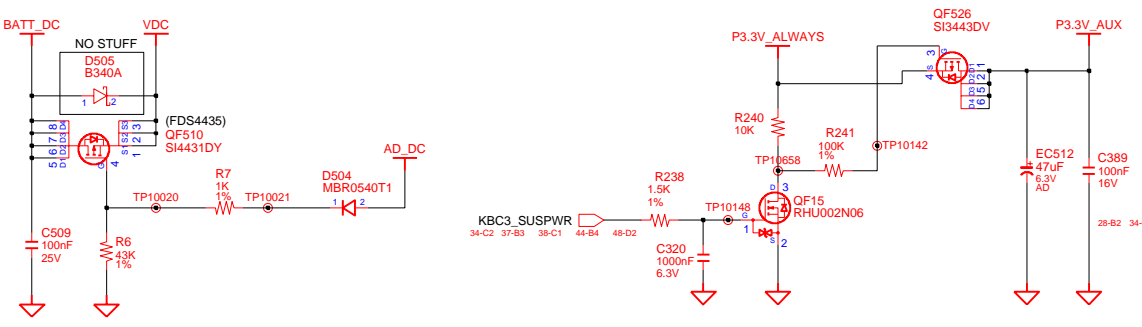
### MICOM\_P3V Power



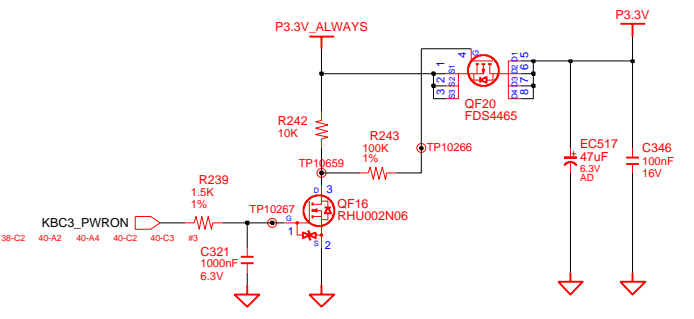
### Switched Power On (P5V)



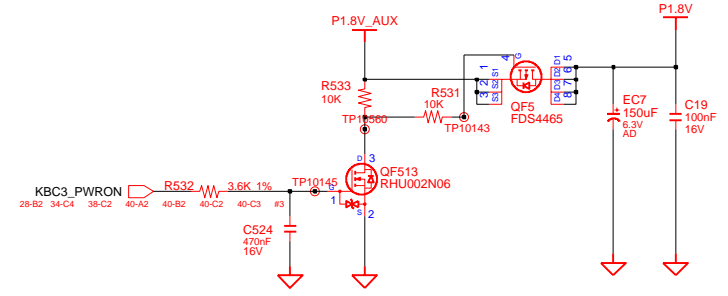
### Switched Power On (P3.3V\_AUX)



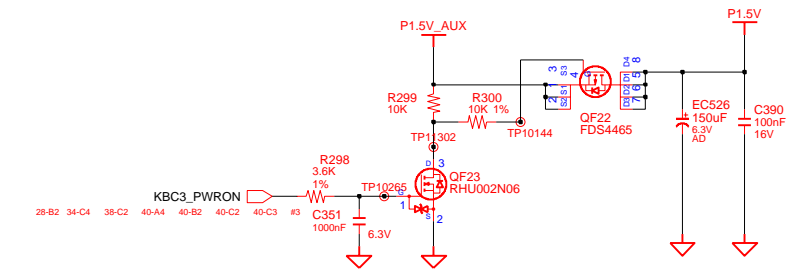
### Switched Power On (P3.3V)



### Switched Power On (P1.8V)



### Switched Power On (P1.5V)

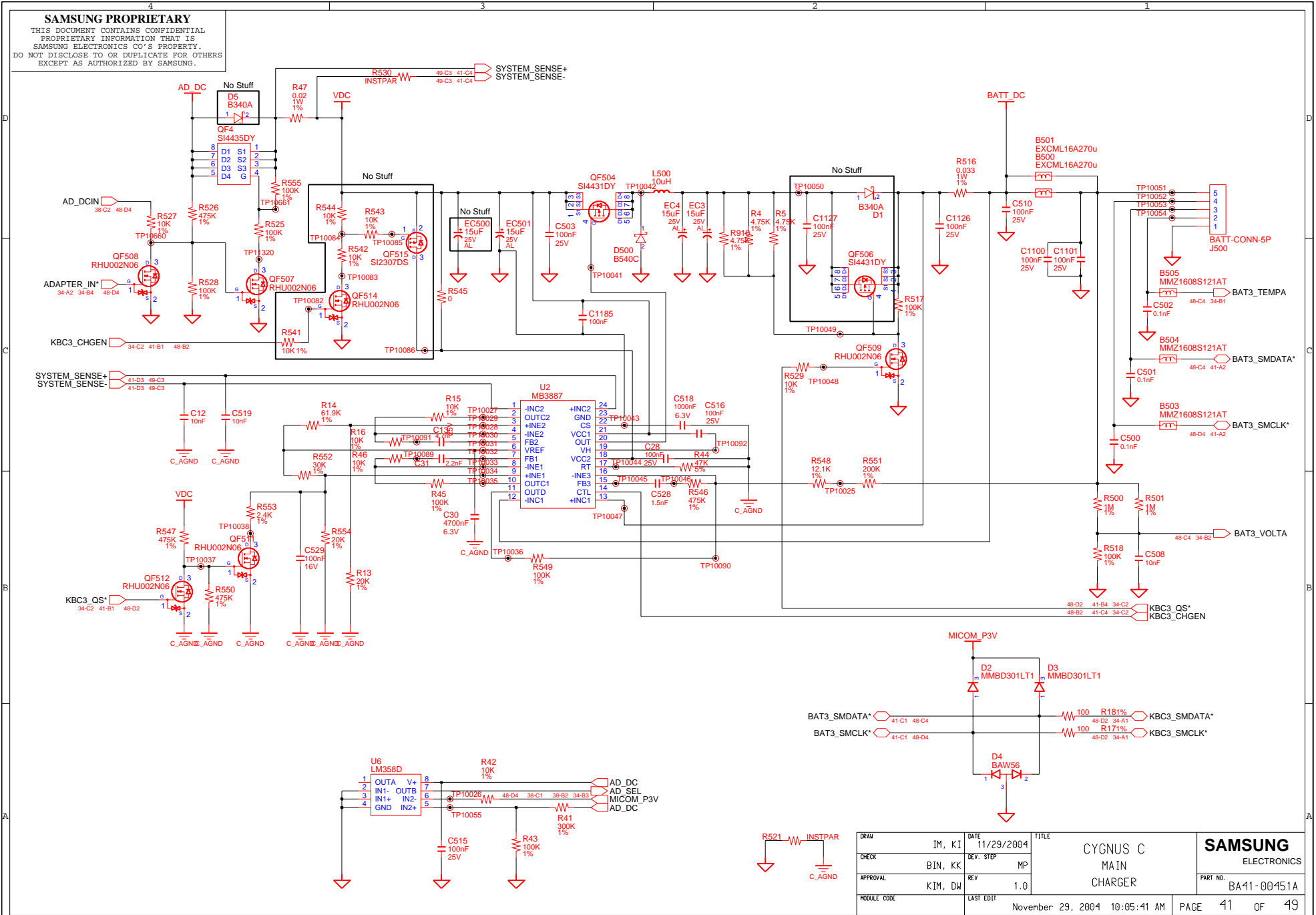


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	MICOM & SWITCHED POWER		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	40	OF 49



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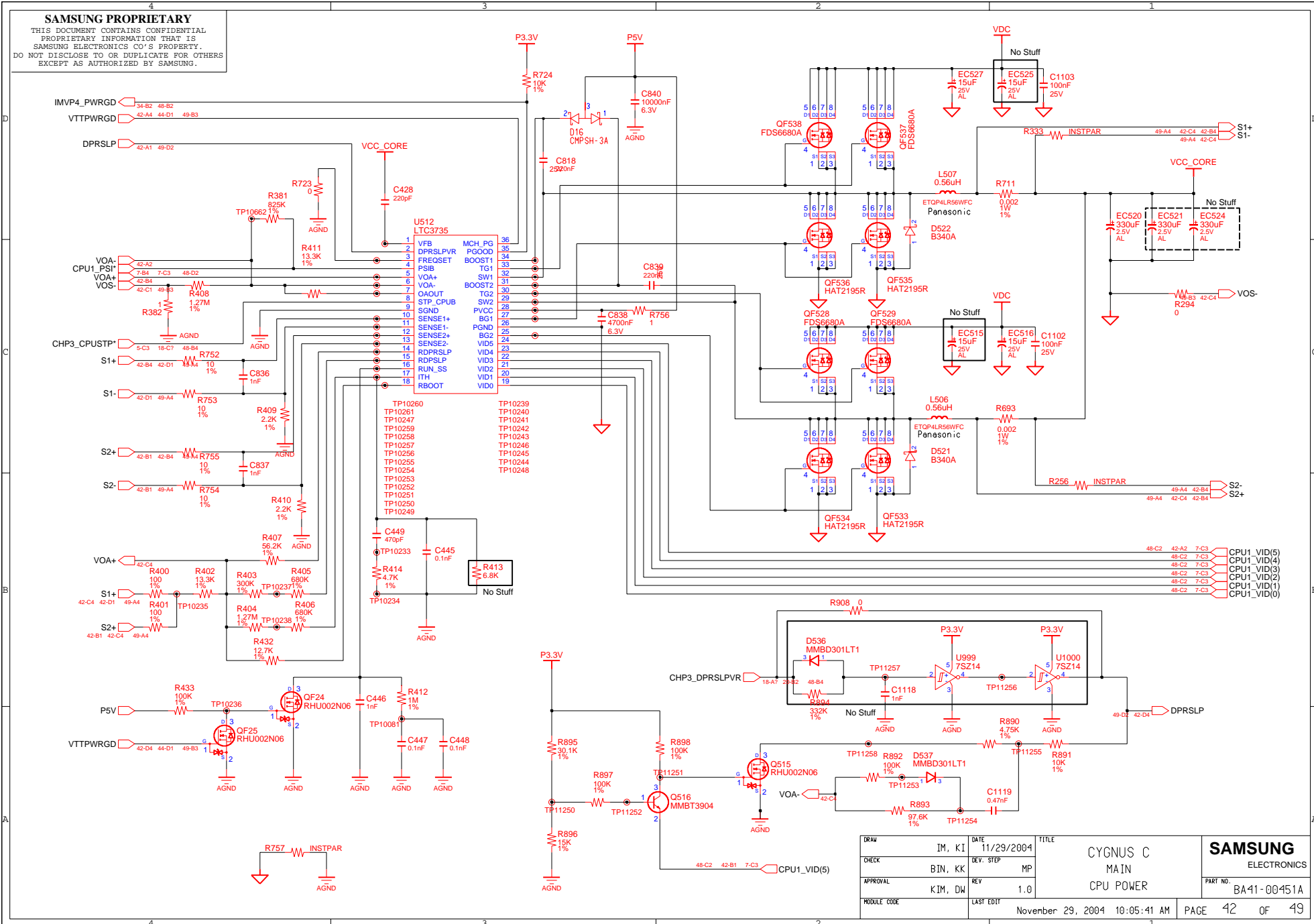
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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN CHARGER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	41 OF 49	

**SAMSUNG PROPRIETARY**

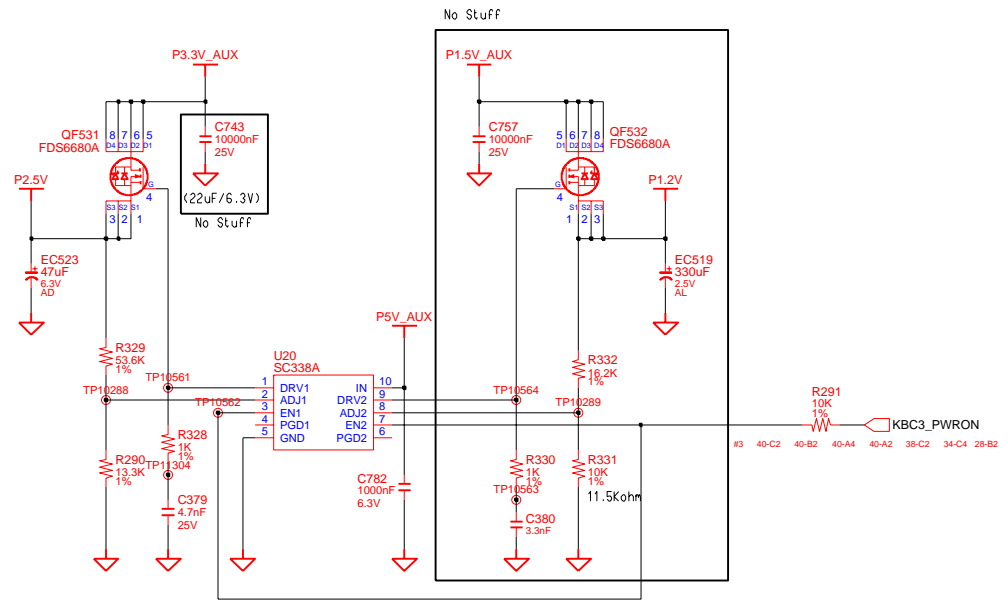
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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN CPU POWER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	MP	REV	1.0	
APPROVAL	KIM, DW	LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	42	OF 49

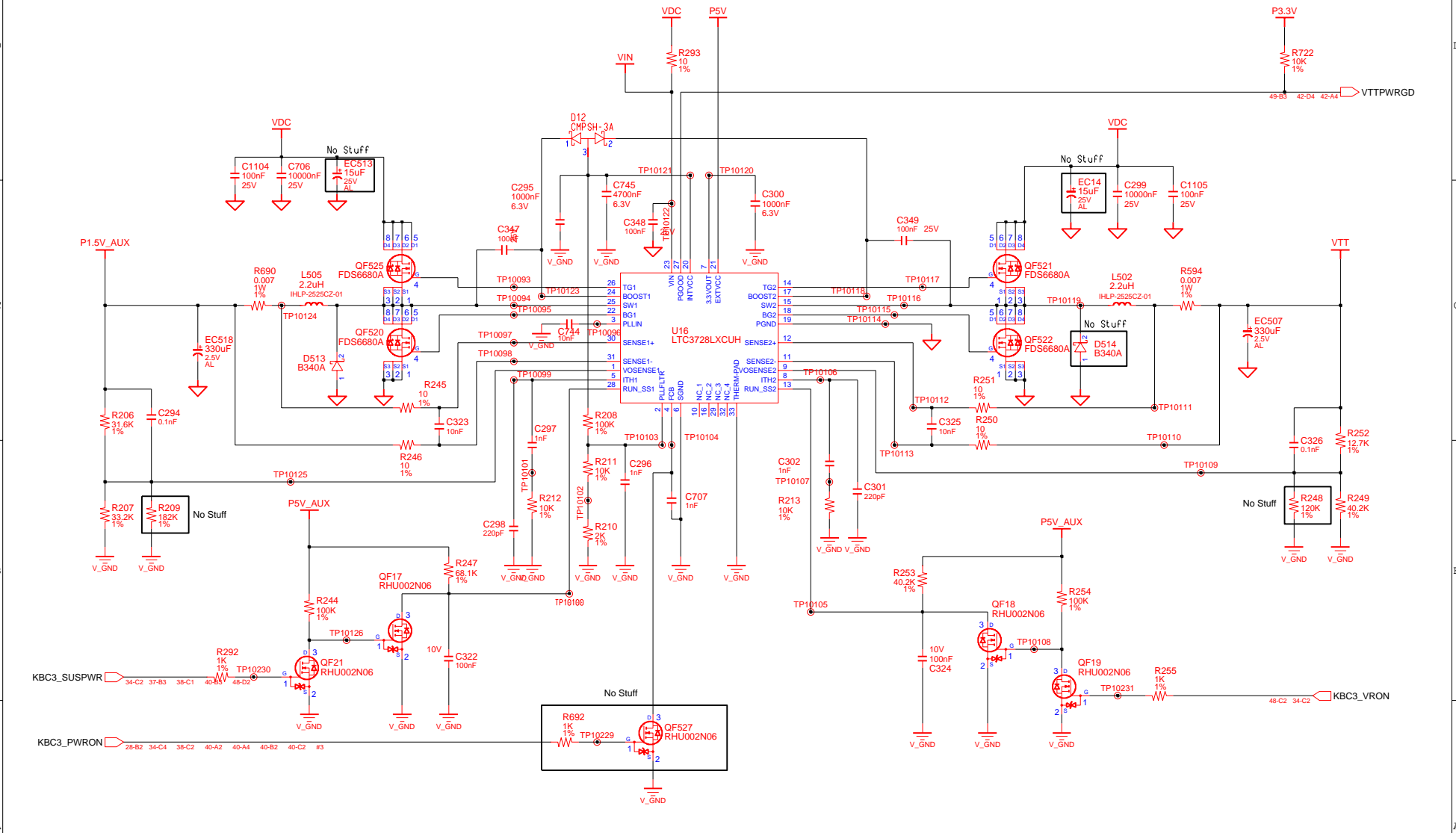
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## P2.5V&P1.2V



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN P2.5V & P1.2V	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0		PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	43	OF 49

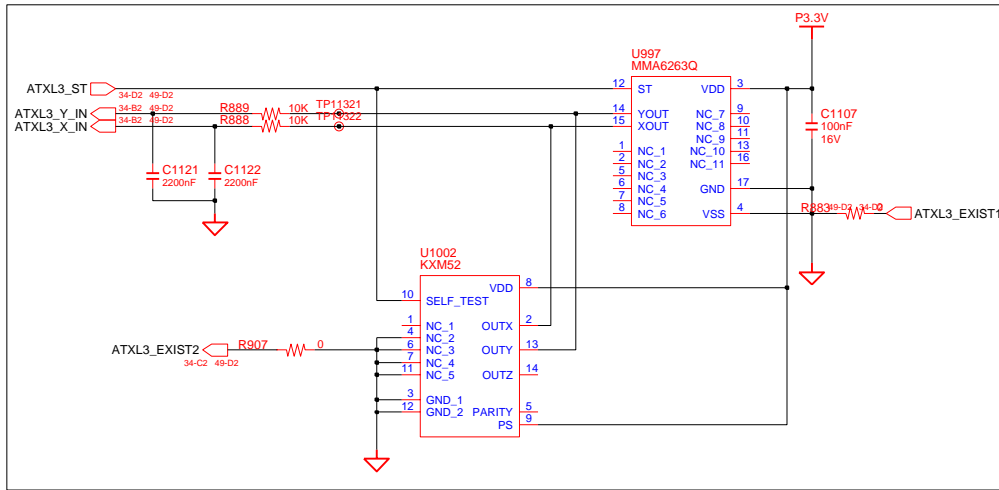
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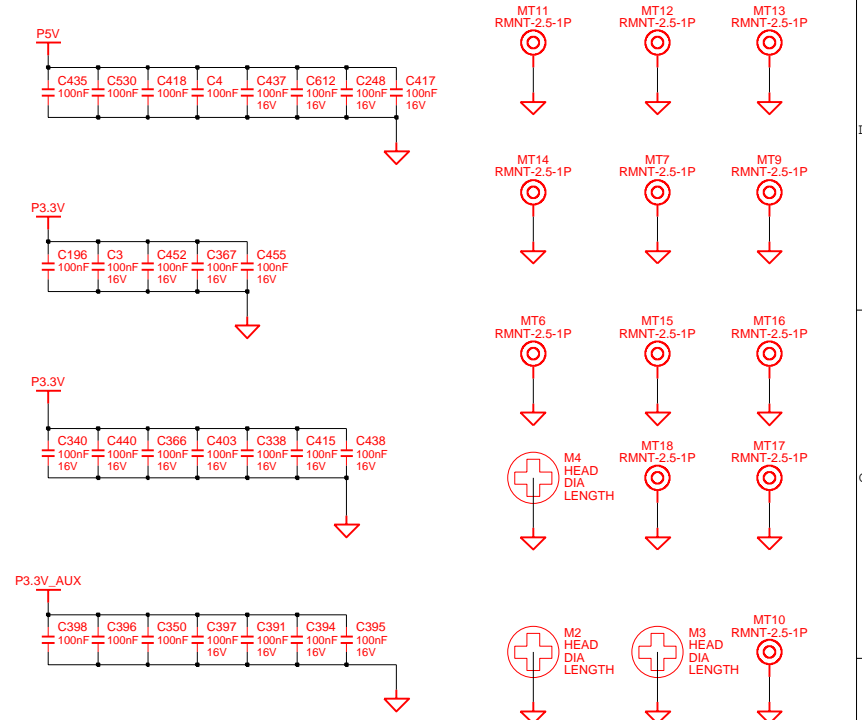
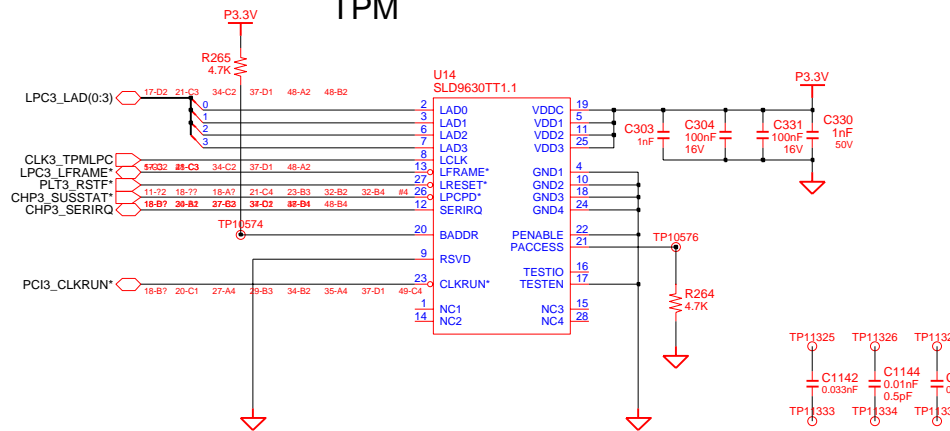
DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN P1.5V_AUX & VTT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	44 OF 49	

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# AIRBAG



# TPM



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

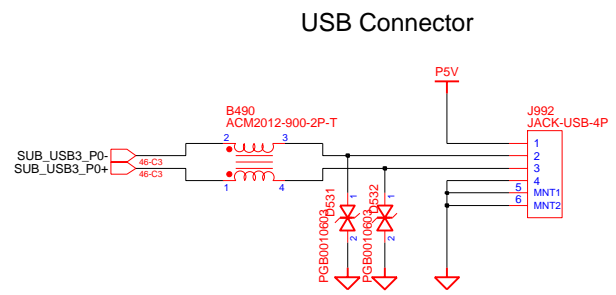


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAINBD AIRBAG & TPM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	45 OF 49	

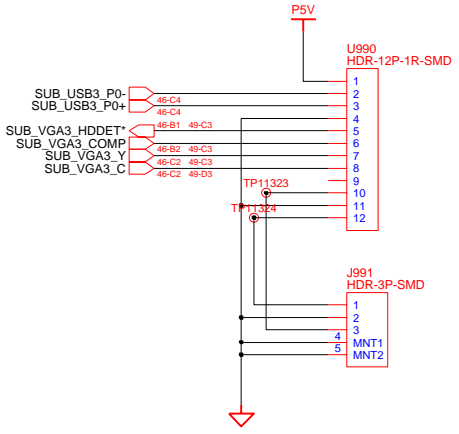
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# < USB BOARD >

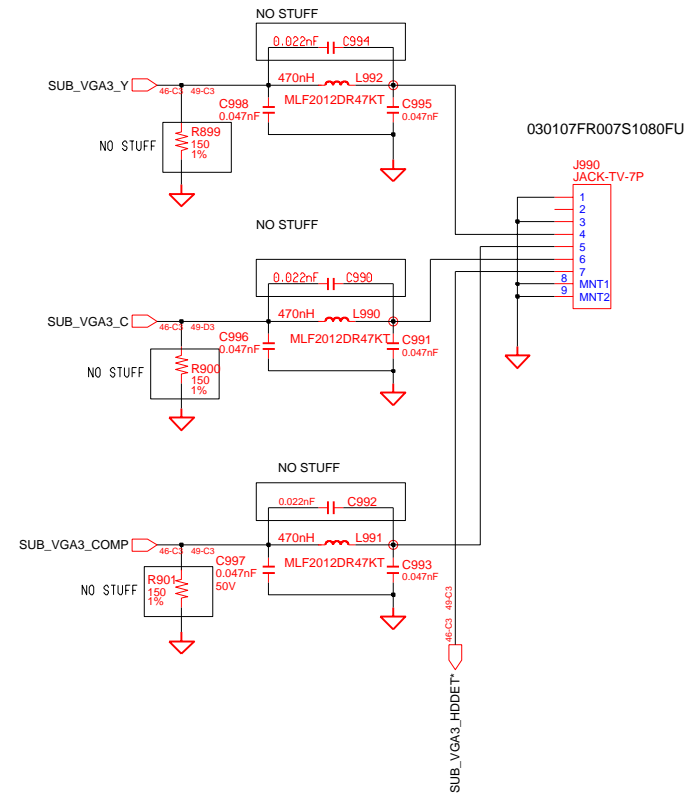
## USB Connector



## Mother Board I/F



## TV OUT JACK



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN MOUNT HOLE	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT				
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# Revision History

Page No.	Cause And Actions (Revised Items)	Page No.	Cause And Actions (Revised Items)

DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN REV. HISTORY	<b>SAMSUNG</b> ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			
			PAGE	47	OF	49

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TP11002O ADAPTER\_IN\*  
TP11003O AD\_DGIN  
TP11004O AD\_SEL  
TP11005O AUD3\_MONO\_OUT  
TP11006O AUD3\_PCBEFP  
TP11007O AUD3\_PHONE  
TP11008O AUD5\_SPDIF  
TP11009O AUD5\_CDND  
TP11010O AUD5\_CDL  
TP11011O AUD5\_CDR  
TP11012O BAT3\_LS\_K\*  
TP11013O BAT3\_SMDATA\*  
TP11014O BAT3\_TEMP\*  
TP11015O BAT3\_VOLTA  
TP11016O BL13\_BTN\_LED\*  
TP11017O BL13\_CURRTIN\*  
TP11018O BL13\_RFON  
TP11019O BL13\_WAKEUP  
TP11020O CB3\_AA\_18  
TP11021O CB3\_AA\_19  
TP11022O CB3\_A\_D\_14  
TP11023O CB3\_A\_D\_2  
TP11024O CB3\_CAD(0)  
TP11025O CB3\_CAD(1)  
TP11026O CB3\_CAD(10)  
TP11027O CB3\_CAD(11)  
TP11028O CB3\_CAD(12)  
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TP11054O CB3\_CAD(8)  
TP11055O CB3\_CAD(9)  
TP11056O CB3\_CAUDIO  
TP11057O CB3\_CCBE1\*  
TP11058O CB3\_CCBE2\*  
TP11059O CB3\_CCBE3\*  
TP11060O CB3\_CCLK  
TP11061O CB3\_CCLKRUN\*  
TP11062O CB3\_CFMSEL\*  
TP11063O CB3\_CFRAME\*  
TP11064O CB3\_CNTI\*  
TP11065O CB3\_CINI\*  
TP11066O CB3\_CPHY\*  
TP11067O CB3\_CPHR\*  
TP11068O CB3\_CPER\*  
TP11069O CB3\_CREQ\*  
TP11070O CB3\_CRS1\*  
TP11071O CB3\_CRS2\*  
TP11072O CB3\_CSTOP\*  
TP11073O CB3\_CS1SCHG  
TP11074O CB3\_CS1TRD\*

TP10954OCB3\_CVS1  
TP10955OCB3\_CVS2  
TP10956OCB3\_MD\_CLK  
TP10957OCB3\_MD\_DATA0\_MS\_SDI0  
TP10958OCB3\_MD\_DATA1  
TP10959OCB3\_MD\_DATA2  
TP10960OCB3\_MD\_DATA3  
TP10961OCB3\_MD\_DATA4\_XD  
TP10962OCB3\_MD\_DATA5\_XD  
TP10963OCB3\_MD\_DATA6\_XD  
TP10964OCB3\_MD\_DATA7\_XD  
TP10965OCB3\_MD\_VCCEN  
TP10966OCB3\_MD\_XD\_ALE  
TP10967OCB3\_MD\_XD\_CE\*  
TP10968OCB3\_MD\_XD\_CLE  
TP10969OCB3\_MD\_XD\_MP\*  
TP10970OCB3\_MS\_BS\_SD\_CMD  
TP10971OCB3\_MS\_INS\*\_XD\_CD\*  
TP10972OCB3\_SD\_CD\*\_XD\_CD\*  
TP10973OCB3\_SD\_WP\*\_XD\_R\_B\*  
TP10974OCB3\_VCCSEN\*  
TP10975OCB3\_VCCSEN\*  
TP10976OCB3\_VCCA  
TP10977OCB3\_VCPA  
TP10978OCB3\_VPPEN0  
TP10979OCB3\_VPPEN1  
TP10980OCB3\_SPKR  
TP10981OCB3\_SPCOM  
TP10982OCB3\_S  
TP10983OCB3\_CLK  
TP10984OCB3\_DATA  
TP10985OCB3\_S394\_ROMW\*  
TP10986OCB3\_AUD\_BCLK  
TP10987OCB3\_AUD\_RST\*  
TP10988OCB3\_AUD\_SDO  
TP10989OCB3\_AUD\_SYNC  
TP10990OCB3\_MDC\_BCLK  
TP10991OCB3\_MDC\_RST\*  
TP10992OCB3\_MDC\_SDO  
TP10993OCB3\_MDC\_SYNC  
TP10994OCB3\_CS37\_SD16  
TP10995OCB3\_CS37\_SD11  
TP10996OCB3\_BIOS\_TBL\*  
TP10997OCB3\_BIOS\_WP\*  
TP10998OCB3\_DPSL\_PVR  
TP10999OCB3\_IDE\_IRQ\*  
TP11000OCB3\_INTRUDER\*  
TP11001OCB3\_INTPWRON  
TP11002OCB3\_LDR0\*  
TP11003OCB3\_LDR0\*  
TP11004OCB3\_OVERTP\*  
TP11005OCB3\_PC15TP\*  
TP11006OCB3\_PME\*  
TP11007OCB3\_PWRBTN\*  
TP11008OCB3\_RTC\_RST\*  
TP11009OCB3\_SATA\_LED\*  
TP11010OCB3\_SER\_IRQ  
TP11011OCB3\_SLP\_S3\*  
TP11012OCB3\_SLP\_S4\*  
TP11013OCB3\_SLP\_S5\*  
TP11014OCB3\_SMLINK0  
TP11015OCB3\_SMLINK1  
TP11016OCB3\_SUSSTAT\*  
TP11017OCB3\_THRMTRIP\*  
TP11018OCB3\_THRMTRIP\*

TP10868O CLK3\_BSEL1  
TP10869O CLK3\_BSEL2  
TP10870O CLK3\_ICH14  
TP10871O CLK3\_PCLKCB  
TP10872O CLK3\_PCLKFHW  
TP10873O CLK3\_PCLKICH  
TP10874O CLK3\_PCLKLAN  
TP10875O CLK3\_PCLKMCOM  
TP10876O CLK3\_PCLKMIN  
TP10877O CLK3\_PCLKS10  
TP10878O CLK3\_PWRGD\*  
TP10879O CLK3\_S1014  
TP10880O CLK3\_S10PCI\_DS  
TP10881O CLK3\_SMBCLK  
TP10882O CLK3\_SMBDATA  
TP10883O CLK3\_SSCIN  
TP10884O CLK3\_TPLMPC  
TP10885O CLK3\_USB48

TP10867O CPU1\_A20M\*  
TP10856O CPU1\_DPSL\_P\*  
TP10857O CPU1\_DP\_SLP\*  
TP10866O CPU1\_CPURST\*

TP10858O CPU1\_FERR\*  
TP10859O CPU1\_IGNNE\*  
TP10860O CPU1\_INIT\*  
TP10861O CPU1\_INTR\*  
TP10862O CPU1\_NMI\*  
TP10863O CPU1\_PROCH0T\*

TP10832O CPU1\_PS]\*  
TP10833O CPU1\_PWRGD CPU

TP10834O CPU1\_SLP\*  
TP10835O CPU1\_SMI\*  
TP10836O CPU1\_STPCLK\*  
TP10837O CPU1\_TCK  
TP10838O CPU1\_TDI  
TP10839O CPU1\_TRST\*  
TP10840O CPU1\_THRMTRIP\*  
TP10841O CPU1\_TMS  
TP10842O CPU1\_TROY\*  
TP10843O CPU1\_TRST\*  
TP10844O CPU1\_VID(0)  
TP10845O CPU1\_VID(1)  
TP10846O CPU1\_VID(2)  
TP10847O CPU1\_VID(3)  
TP10848O CPU1\_VID(4)  
TP10849O CPU1\_VID(5)  
TP10850O CPU2\_THERM\_DA  
TP10851O CPU2\_THERM\_DC  
TP10852O CPU3\_ALERT\*  
TP10853O DDC3\_PWRGD  
TP10854O DCK19\_IN\*  
TP10855O DCK3\_BLUE  
TP10856O DCK3\_C  
TP10857O DCK3\_CLK33  
TP10858O DCK3\_CLKRUN\*  
TP10859O DCK3\_COMP  
TP10860O DCK3\_DRST\*  
TP10861O DCK3\_EJECT\*  
TP10862O DCK3\_GREEN  
TP10863O DCK3\_LAD(0)  
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TP10867O DCK3\_LDR0\*  
TP10868O DCK3\_LFRAME\*  
TP10869O DCK3\_PWRGD  
TP10870O DCK3\_SER\_IRQ  
TP10871O DCK3\_S1014  
TP10872O DCK3\_SMBCLK  
TP10873O DCK3\_SMDATA  
TP10874O DCK3\_SUSSTAT\*  
TP10875O DCK3\_Y  
TP10876O DCK5\_HP\_PLUGIN  
TP10877O DCK5\_LINE\_IN\_L  
TP10878O DCK5\_LINE\_IN\_R  
TP10879O DCK5\_LINE\_OUT\_L  
TP10880O DCK5\_LINE\_OUT\_R  
TP10881O DDR2\_FBK1\*  
TP10882O DLAN3\_RSTF\*

TP10802O CAMP5\_PWRDOWN

TP10772O CFAN3\_FDBACK\*  
TP10773O CFH3\_INIT\*  
TP10774O CGFX3\_BLUE  
TP10775O CGFX3\_C  
TP10776O CGFX3\_COMP  
TP10777O CGFX3\_DDC\_CLK  
TP10778O CGFX3\_DDCDATA  
TP10779O CGFX3\_GREEN  
TP10780O CGFX3\_HSYNC  
TP10781O CGFX3\_RED  
TP10782O CGFX3\_VSYNC  
TP10783O CGFX3\_Y  
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TP10785O CHD05\_PATADET  
TP10786O CHD03\_SEL  
TP10787O CHP3\_DETECT  
TP10788O IDE5\_A0  
TP10789O IDE5\_A2  
TP10790O IDE5\_A3  
TP10791O IDE5\_CS1\*  
TP10792O IDE5\_CS3\*  
TP10793O IDE5\_D(0)  
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TP10808O IDE5\_D(9)  
TP10809O IDE5\_DACK\*  
TP10810O IDE5\_DREQ\*

TP10700O LAN3\_LOW\_PWR  
TP10701O LB3\_LED  
TP10702O L\_CD2\_BKLTCRL  
TP10703O L\_CD2\_BKLTON  
TP10704O L\_CD2\_VDDEN  
TP10705O L\_CD3\_BKLTCRL  
TP10706O L\_CD3\_BKLTON  
TP10707O L\_CD3\_BRT\*  
TP10708O L\_CD3\_VDD  
TP10709O L\_CD3\_CHARGE  
TP10710O L\_CD5\_AMPBR  
TP10711O L\_CD5\_GREEN  
TP10712O L\_ID3\_SWITCH\*  
TP10713O L\_PC3\_LAD(0)  
TP10714O L\_PC3\_LAD(1)  
TP10715O L\_PC3\_LAD(2)  
TP10716O L\_PC3\_LAD(3)  
TP10717O L\_PC3\_LFRAME\*  
TP10718O LCH1\_BSEL0  
TP10719O LCH1\_HXSWING  
TP10720O LCH1\_HYSWING  
TP10721O LCH2\_BMBUSV\*

TP10708O KBC3\_PWRGD  
TP10709O KBC3\_PWRON  
TP10710O KBC3\_PWRSW\*  
TP10711O KBC3\_QS\*  
TP10712O KBC3\_RSMRST\*  
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TP10715O KBC3\_SLELED\*  
TP10716O KBC3\_SMLCLK\*  
TP10717O KBC3\_SMDATA\*  
TP10718O KBC3\_SPKMUTE  
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TP10720O KBC3\_THERM\_ALERT\*  
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TP10723O KBC3\_VRON  
TP10724O KBC3\_WAKESC1\*  
TP10725O KBC3\_WLANON  
TP10726O KBC5\_3DDON  
TP10727O KBC5\_AVDD\_ON  
TP10728O KBC5\_KSI(0)  
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TP10759O KBC5\_KSI(31)  
TP10760O KBC3\_BRIT\_DA  
TP10761O KBC3\_CAPSLED\*  
TP10762O KBC3\_CHGEN  
TP10763O KBC3\_CPURST\*  
TP10764O KBC3\_DCKDCON  
TP10765O KBC3\_DCKIN\*  
TP10766O KBC3\_EJECT\*  
TP10767O KBC3\_EXTSMT  
TP10768O KBC3\_F\_AWC\_TRL  
TP10769O KBC3\_INVP4\_PWRGD  
TP10770O KBC3\_LBLED\*  
TP10771O KBC3\_NUMLED\*

TP10880O MCH2\_CFG(5)  
TP10881O MCH2\_CFG(6)  
TP10882O MDC3\_AUDIN  
TP10883O MDC3\_VCC  
TP10700O LAN3\_LOW\_PWR  
TP10701O LB3\_LED  
TP10702O L\_CD2\_BKLTCRL  
TP10703O L\_CD2\_BKLTON  
TP10704O L\_CD2\_VDDEN  
TP10705O L\_CD3\_BKLTCRL  
TP10706O L\_CD3\_BKLTON  
TP10707O L\_CD3\_BRT\*  
TP10708O L\_CD3\_VDD  
TP10709O L\_CD3\_CHARGE  
TP10710O L\_CD5\_AMPBR  
TP10711O L\_CD5\_GREEN  
TP10712O L\_ID3\_SWITCH\*  
TP10713O L\_PC3\_LAD(0)  
TP10714O L\_PC3\_LAD(1)  
TP10715O L\_PC3\_LAD(2)  
TP10716O L\_PC3\_LAD(3)  
TP10717O L\_PC3\_LFRAME\*  
TP10718O LCH1\_BSEL0  
TP10719O LCH1\_HXSWING  
TP10720O LCH1\_HYSWING  
TP10721O LCH2\_BMBUSV\*



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<p>TP11030MIC5_N01 TP11031MIC5_N02</p>	<p>TP11032OPIC13_AD(0) TP11033OPIC13_AD(1) TP11034OPIC13_AD(10) TP11035OPIC13_AD(11) TP11036OPIC13_AD(12) TP11037OPIC13_AD(13) TP11038OPIC13_AD(14) TP11039OPIC13_AD(15) TP11040OPIC13_AD(16) TP11041OPIC13_AD(17) TP11042OPIC13_AD(18) TP11043OPIC13_AD(19) TP11044OPIC13_AD(2) TP11045OPIC13_AD(20) TP11046OPIC13_AD(21) TP11047OPIC13_AD(22) TP11048OPIC13_AD(23) TP11049OPIC13_AD(24) TP11050OPIC13_AD(25) TP11051OPIC13_AD(26) TP11052OPIC13_AD(27) TP11053OPIC13_AD(28) TP11054OPIC13_AD(29) TP11055OPIC13_AD(3) TP11056OPIC13_AD(30) TP11057OPIC13_AD(31) TP11058OPIC13_AD(4) TP11059OPIC13_AD(5) TP11060OPIC13_AD(6) TP11061OPIC13_AD(7) TP11062OPIC13_AD(8) TP11063OPIC13_AD(9) TP11064OPIC13_CBE0* TP11065OPIC13_CBE1* TP11066OPIC13_CBE2* TP11067OPIC13_CBE3* TP11068OPIC13_CLKRUN* TP11069OPIC13_DEVSSEL* TP11070OPIC13_FRAME* TP11071OPIC13_GNT0* TP11072OPIC13_GNT1* TP11073OPIC13_GNT2* TP11074OPIC13_GNT3* TP11075OPIC13_INTA* TP11076OPIC13_INTB* TP11077OPIC13_INTC* TP11078OPIC13_INTD* TP11079OPIC13_INTE* TP11080OPIC13_INTF* TP11081OPIC13_INTG* TP11082OPIC13_INTH* TP11083OPIC13_IRDY* TP11084OPIC13_PAR* TP11085OPIC13_PERR* TP11086OPIC13_PLCK* TP11087OPIC13_REQ0* TP11088OPIC13_REQ1* TP11089OPIC13_REQ2* TP11090OPIC13_REQ3* TP11091OPIC13_RS1* TP11092OPIC13_SERR* TP11093OPIC13_STOP* TP11094OPIC13_TRDY* TP11096OPICIE3_WAKE*</p>	<p>TP11108OSATA3_DET* TP11109OSMB3_ALERT* TP11110OSMB3_CLK* TP11111OSMB3_DATA* TP11112OSMB3_LINKALERT* TP11113OSPDIF5_ON* TP11114OSPDIF5_OUT* TP11115OSPROM3_DIN* TP11116OSPROM3_DOUT* TP11117OSUB_VGA3_C* TP11118OSUB_VGA3_COMP* TP11119OSUB_VGA3_HDET* TP11120OSUB_VGA3_Y* TP11121OSYSTEM_SENSE+* TP11122OSYSTEM_SENSE-* TP11123OTP3_TOGGLE* TP11169OC_AGND* TP11170OC_AGND* TP11174OVGA2_DDCCLK* TP11125OVGA2_DDCDATA* TP11126OVGA3_BKLTON* TP11127OVGA3_BLUE* TP11128OVGA3_C* TP11129OVGA3_CHARGE_POW* TP11130OVGA3_COMP* TP11131OVGA3_DV1CLK* TP11132OVGA3_DV1DATA* TP11133OVGA3_GREEN* TP11134OVGA3_HDET* TP11135OVGA3_LCDDDET0* TP11136OVGA3_LCDDDET1* TP11137OVGA3_LCDDVDDON* TP11138OVGA3_RED* TP11139OVGA3_Y* TP11140OVGA5_DDCCLK* TP11141OVGA5_DDCDATA* TP11142OVGA5_DV1CLK* TP11143OVGA5_DV1DATA* TP11144OVGA5_HSYNC* TP11145OVGA5_VSYNC* TP11146OVGS* TP11147OVREF3_OUT_MIC* TP11148OVTTWRGD* TP11149OAD_DC* TP11150OAD_DC* TP11151OAD_DC* TP11152OAD_DC* TP11153OAD_DC* TP11154OAMP_VDD* TP11155OAMP_VDD* TP11156OAUD_GND* TP11157OAUD_GND* TP11158OAUD_GND*</p>	<p>TP11159OAUD_GND* TP11160OAUD_GND* TP11161OAUD_GND* TP11162OAVDD* TP11163OBATT_DC* TP11164OBATT_DC* TP11165OCHSS_GND* TP11166OCHSS_GND* TP11167OCRT_GND* TP11168OCRT_GND* TP11173OD2_GND* TP11174OD2_GND* TP11175OMEM1_VREF* TP11176OP0_9V* TP11177OP0_9V* TP11178OP0_9V* TP11179OP0_9V* TP11180OP0_9V* TP11181OP1_2V* TP11182OP1_2V* TP11183OP1_2V* TP11184OP1_2V* TP11185OP1_2V* TP11186OP1_5V* TP11187OP1_5V* TP11188OP1_5V* TP11189OP1_5V* TP11190OP1_5V* TP11191OP1_5V_AUX* TP11192OP1_5V_AUX* TP11193OP1_5V_AUX* TP11194OP1_5V_AUX* TP11195OP1_5V_AUX* TP11196OP1_8V* TP11197OP1_8V* TP11198OP1_8V* TP11199OP1_8V* TP11200OP1_8V* TP11201OP1_8V_AUX* TP11202OP1_8V_AUX* TP11203OP1_8V_AUX* TP11204OP1_8V_AUX* TP11205OP1_8V_AUX* TP11206OP2_5V_LAN* TP11207OP2_5V_LAN* TP11208OP2_5V_LAN* TP11209OP2_5V_LAN* TP11210OP2_5V_LAN* TP11211OP3_3V_AUX* TP11212OP3_3V_AUX* TP11213OP3_3V_AUX*</p>	<p>TP11214OP3_3V_AUX* TP11215OP3_3V_AUX* TP11216OP5V* TP11217OP5V* TP11218OP5V* TP11219OP5V* TP11220OP5V* TP11221OP5V_AUX* TP11222OP5V_AUX* TP11223OP5V_AUX* TP11224OP5V_AUX* TP11225OP5V_AUX* TP11226OVCC_CORE* TP11227OVCC_CORE* TP11228OVCC_CORE* TP11229OVCC_CORE* TP11230OVCC_CORE* TP11231OVDC* TP11232OVDC* TP11233OVDC* TP11234OVDC* TP11235OVDC* TP11236OV_GND* TP11237OV_GND* TP11238 OGROUND* TP11239 OGROUND* TP11240 OGROUND* TP11241 OGROUND* TP11242 OGROUND* TP11243 OGROUND* TP11244 OGROUND* TP11245 OP3_3V_ALWAYS* TP11246 OP3_3V_ALWAYS* TP11247 OP3_3V_ALWAYS* TP11248 OP3_3V_ALWAYS* TP11249 OP3_3V_ALWAYS*</p>	<p>TP11262OATXL3_EX1ST1* TP11358OATXL3_EX1ST2* TP11263OATXL3_ST* TP11264OATXL3_X_IN* TP11265OATXL3_Y_IN* TP11271ODCK3_PWRONS* TP11272ODPRSLP* TP11273OSI03_DRST* TP11266OVCC_NCTF* TP11267OVCC_NCTF* TP11268OVCC_NCTF* TP11269OVCC_NCTF* TP11270OVCC_NCTF*</p>
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