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8. 블록도 및 회로도

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Madrid-EXT

CPU : Intel Penryn-6M (1067/800) MHz
 Chip Set : Intel Cantiga & ICH9M
 Remarks : Montevina Platform

Model Name : Madrid-EXT
 PBA Name : MAIN
 PCB Code : BA41-#####A
 Dev. Step : PV
 Revision : 1.0
 T.R. Date : 2008.02.29

Design	CHECK	APPROVAL
SE LEE	SE LEE	ES CHO

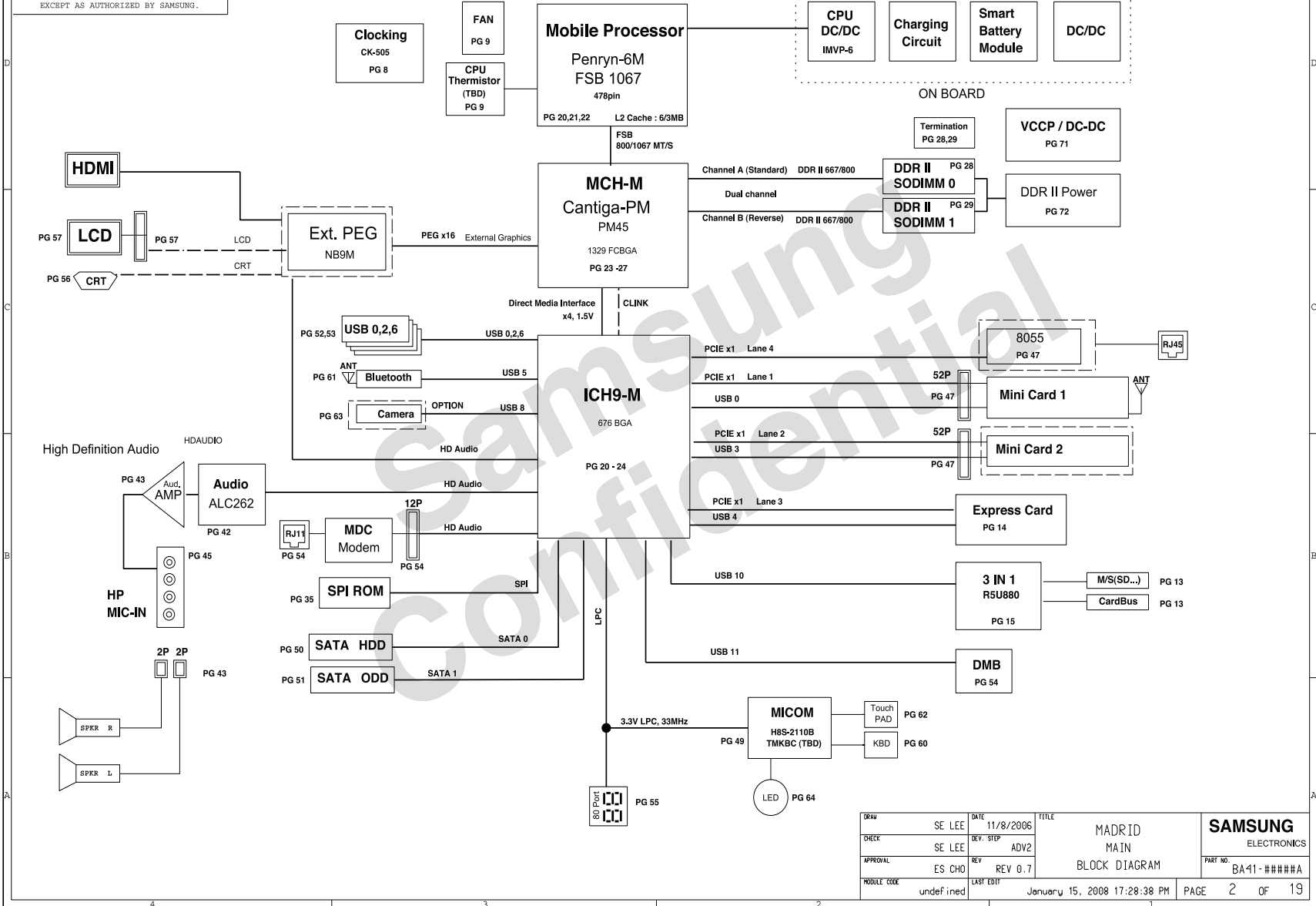
Owner : SEC Mobile R & D Signature : X

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APPROVAL	ES CHO	REV	REV 0.7			
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DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
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BOARD INFORMATION

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A, B, C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI LPC bridgeIDE/AC97/SMBUS	AD30(internal) AD31(internal)	- -	- B
Internal MAC AC Link GLAN	AD24(internal) - -	- - -	- - F, B, E

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P3.3V (VICOM)	3.3V always power rail (for Microm)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	SYSTEM PORT 2
3	NC
4	NC
5	Bluetooth
6	Mini PCI Express 2
7	Camera
8	NC
9	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Panel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

REVISION HISTORY

See rev notes for more information.

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APPROVAL	ES CHO	REV	REV 0.7	BOARD INFO	BOARD INFO	PART NO. BA11-#####A
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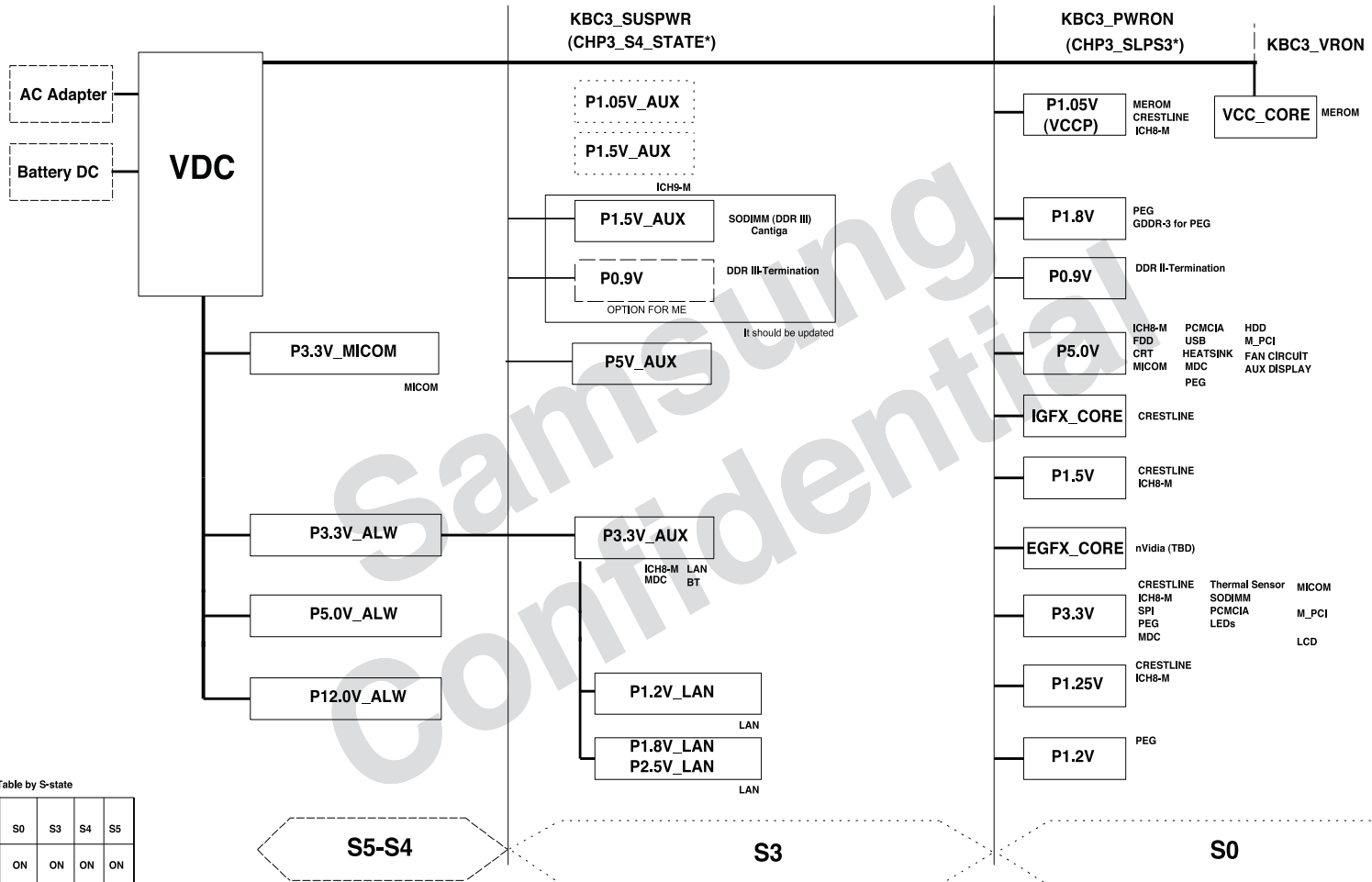
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POWER DIAGRAM

Rev 0.1

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Power On/Off Table by S-state

Rail	S0	S3	S4	S5
+V*(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	ON	ON
+1.8V_AUX	ON	ON	---	---
+0.9V	ON	ON	---	---
+V*AUX	ON	ON	---	---
+V	ON	---	---	---
+V* (CORE)	ON	---	---	---

DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID MAIN	SAMSUNG ELECTRONICS
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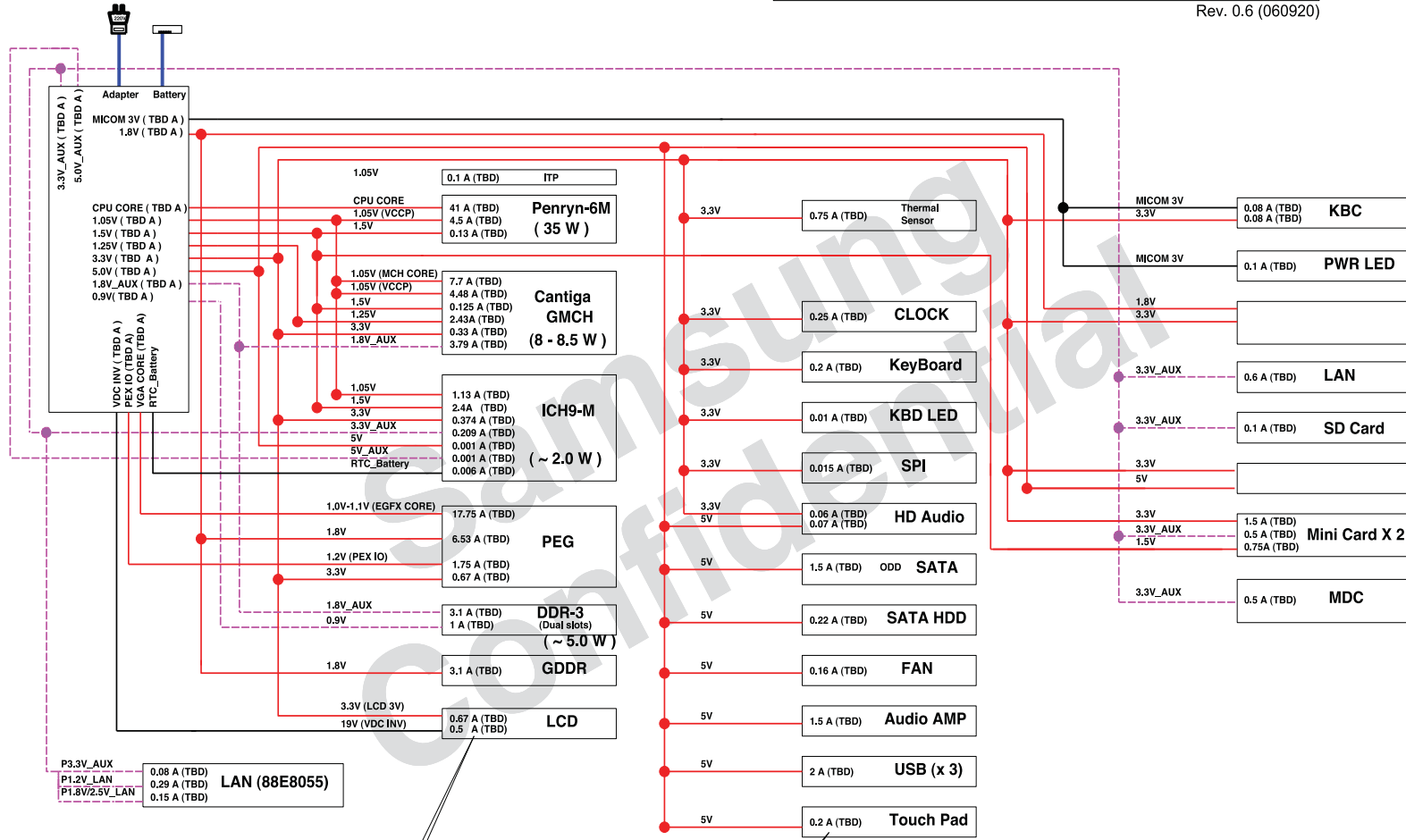
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POWER RAILS ANALYSIS

Rev. 0.6 (060920)

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Value by Datasheet/Application notes (Value by measurement)

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CHECK	SE LEE	DEV. STEP	ADV2			PART NO. BA41-####A
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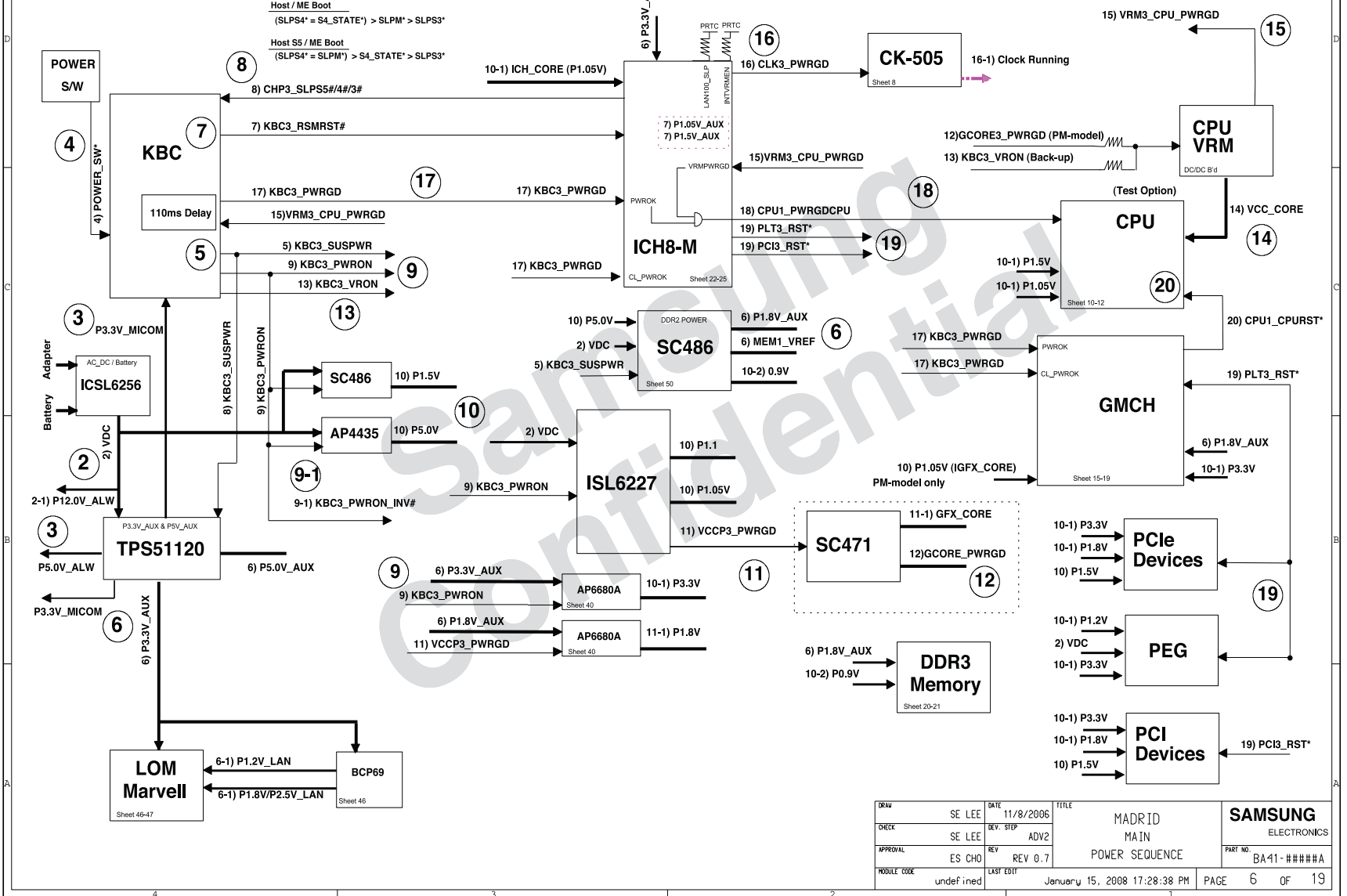
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Host Boot / ME Off
 (SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
 M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
 M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
 (SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
 (SLPS4* = SLPM*) > S4_STATE* > SLPS3*

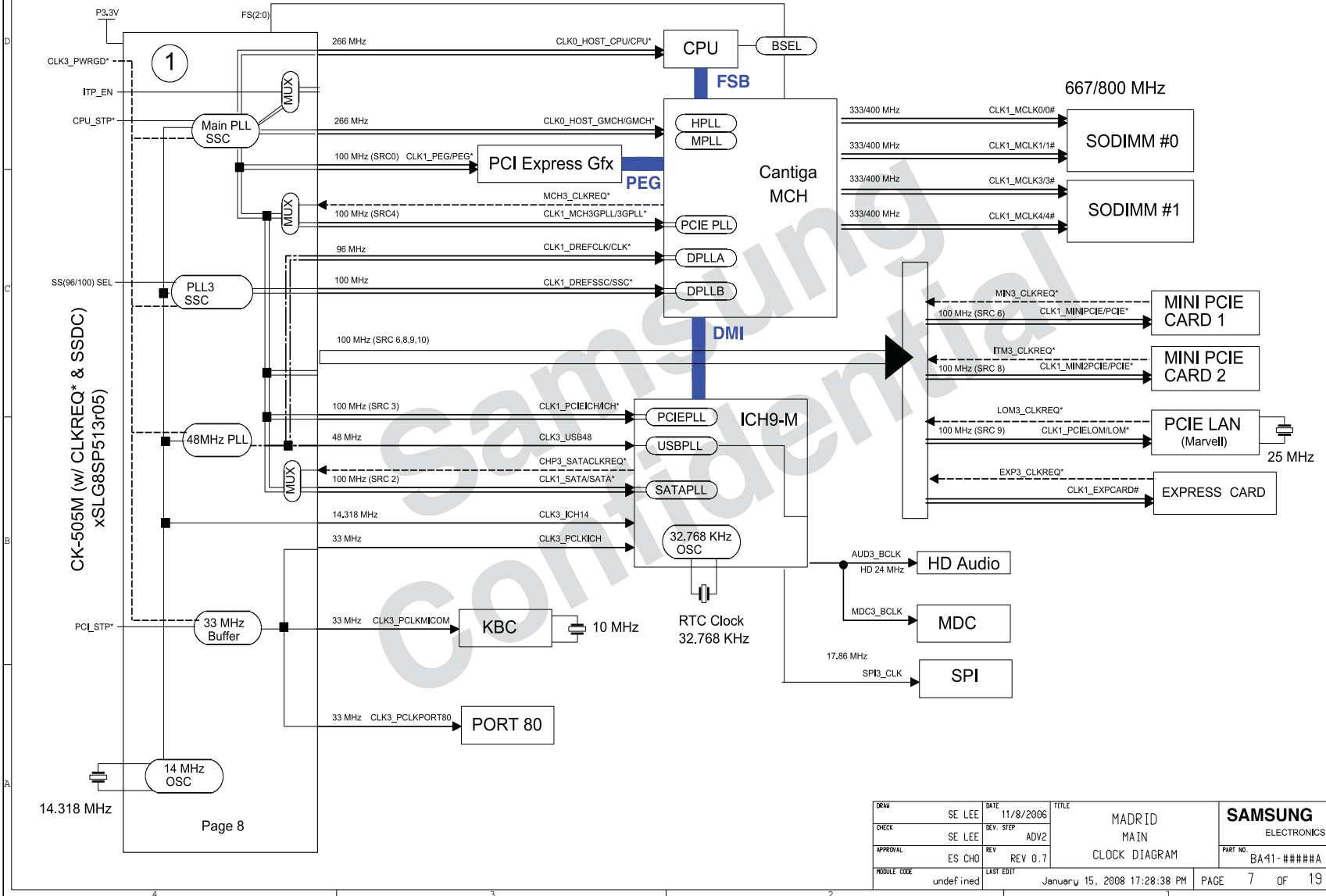


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CK-505M (w/ CLKREQ* & SSDC)
xSLG8SP513r05

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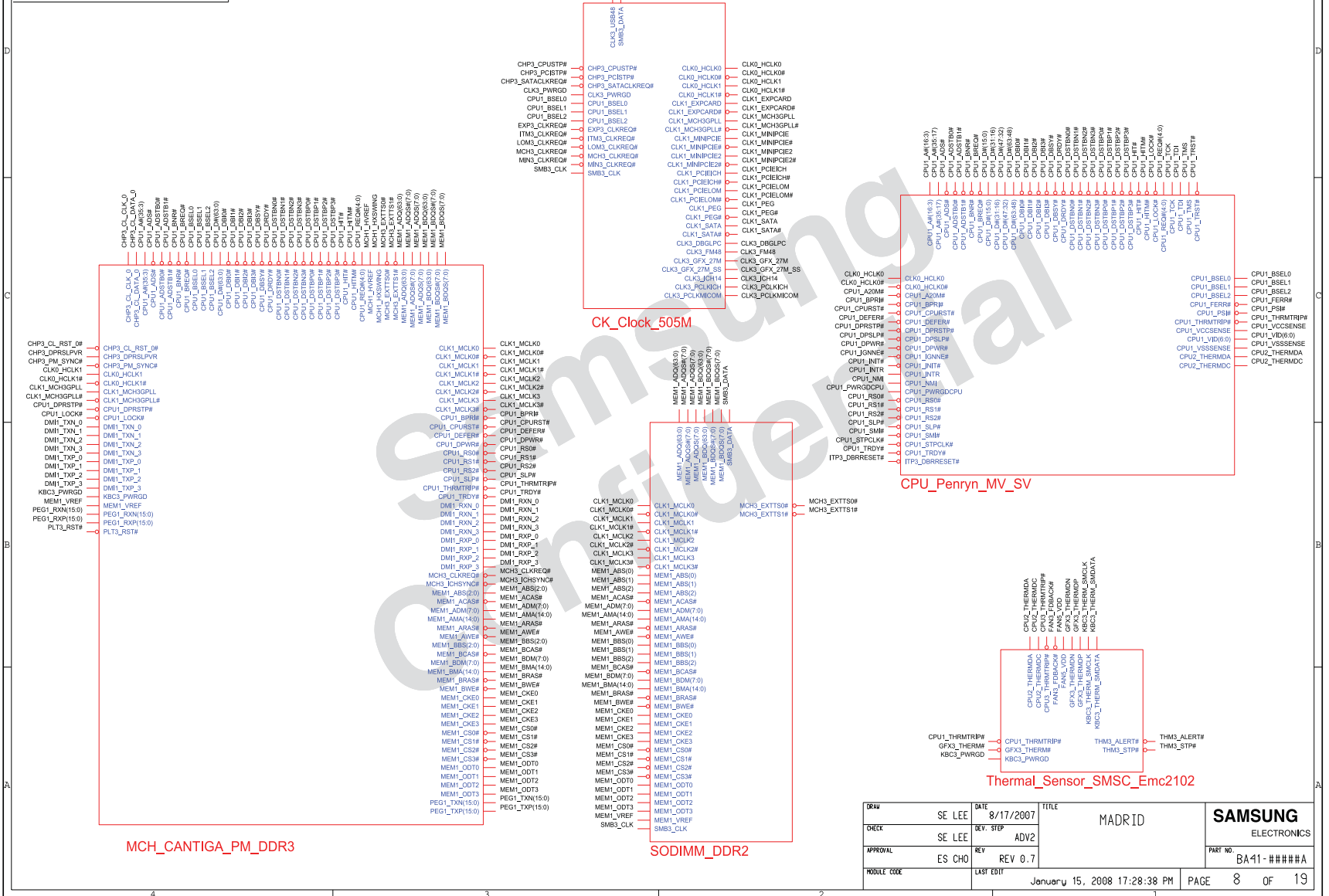
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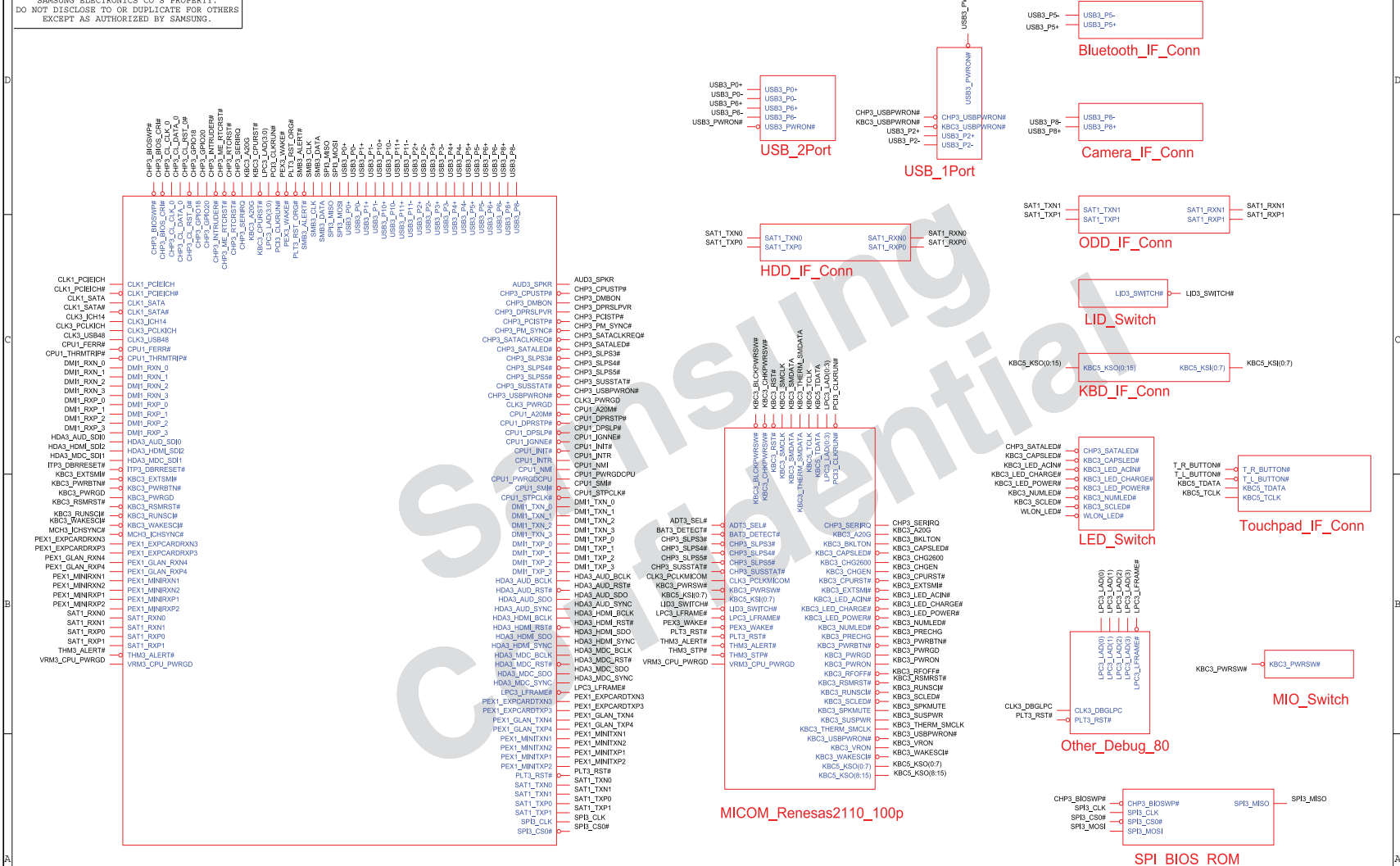
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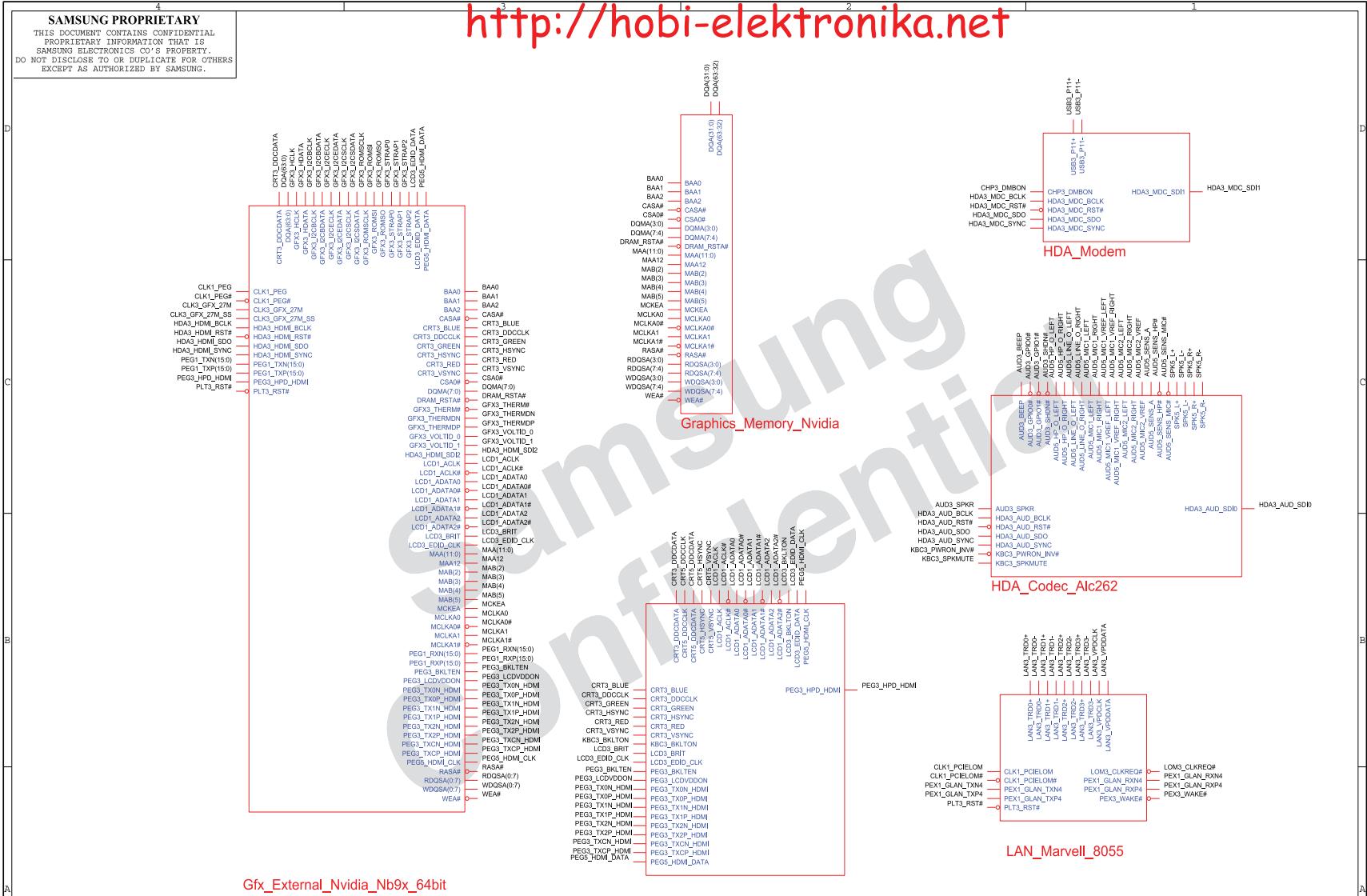
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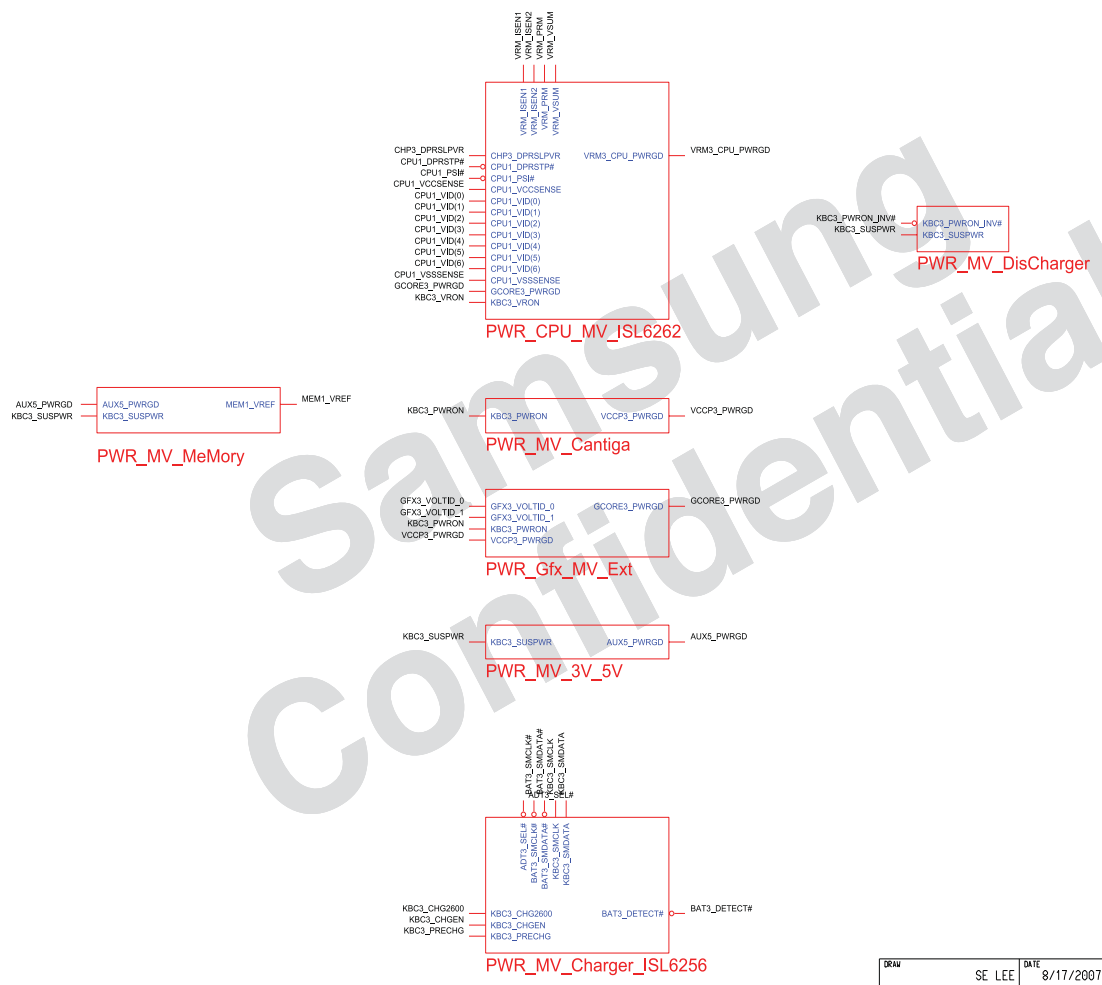


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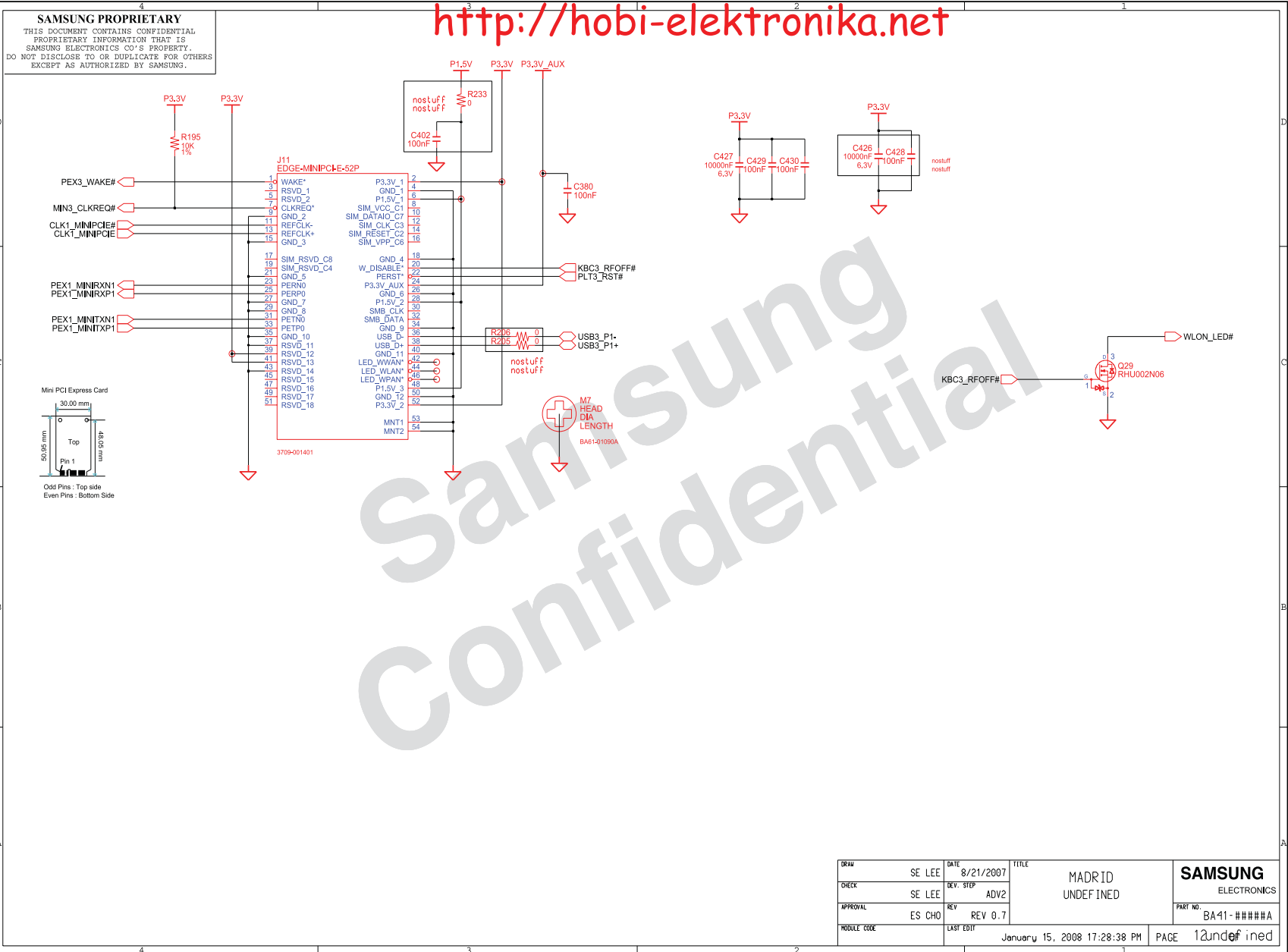
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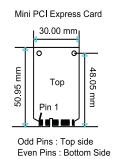
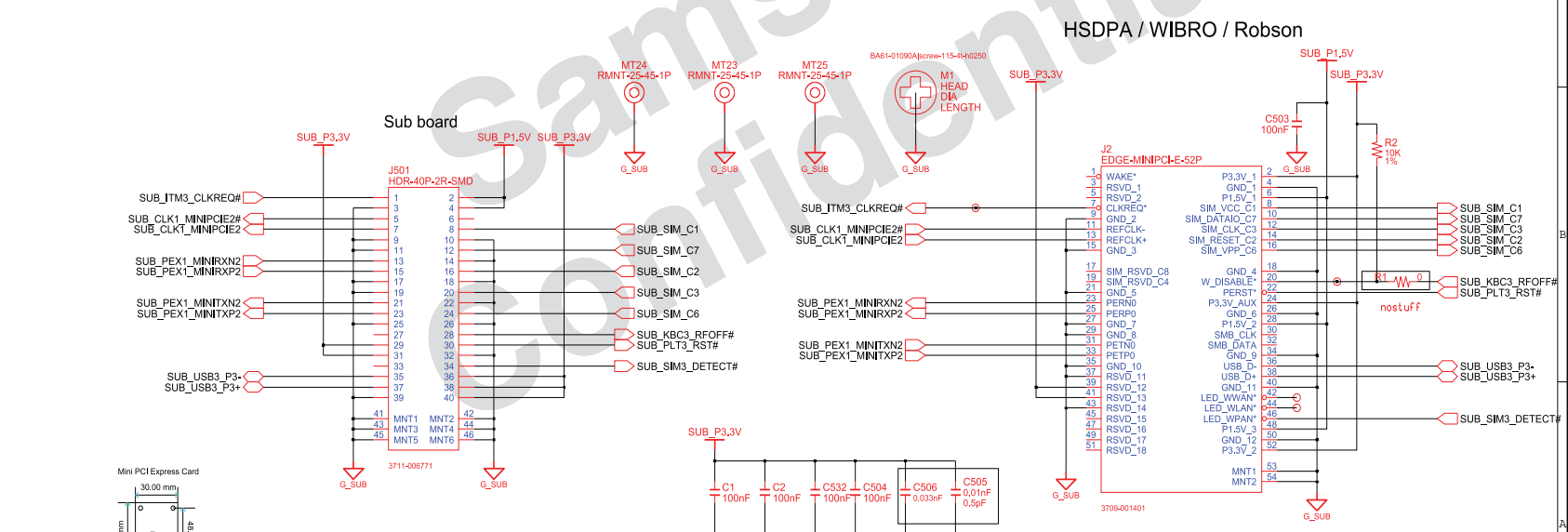
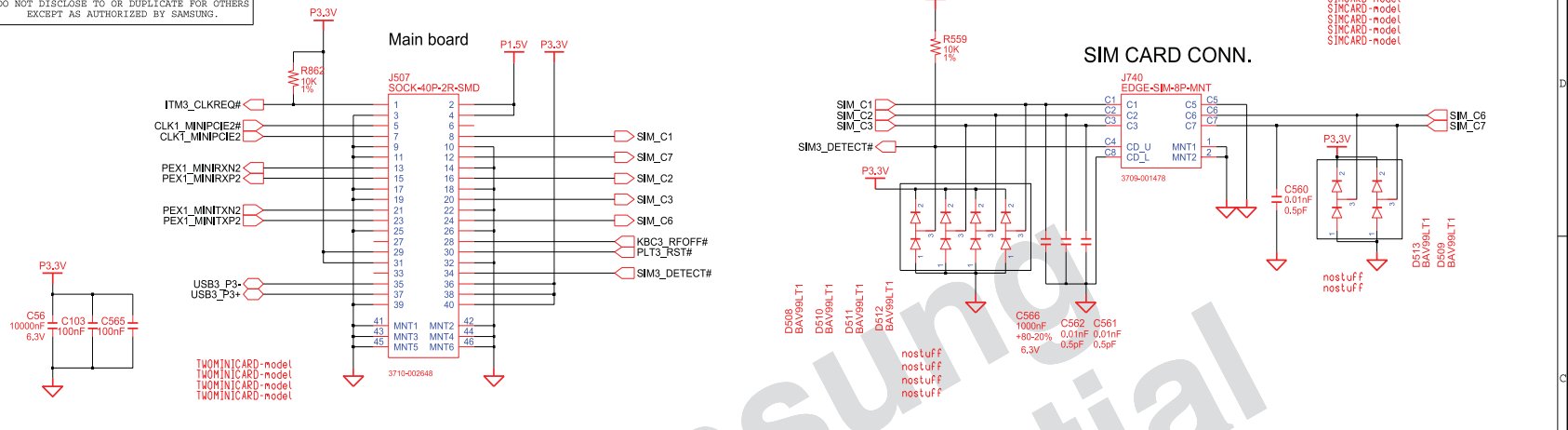
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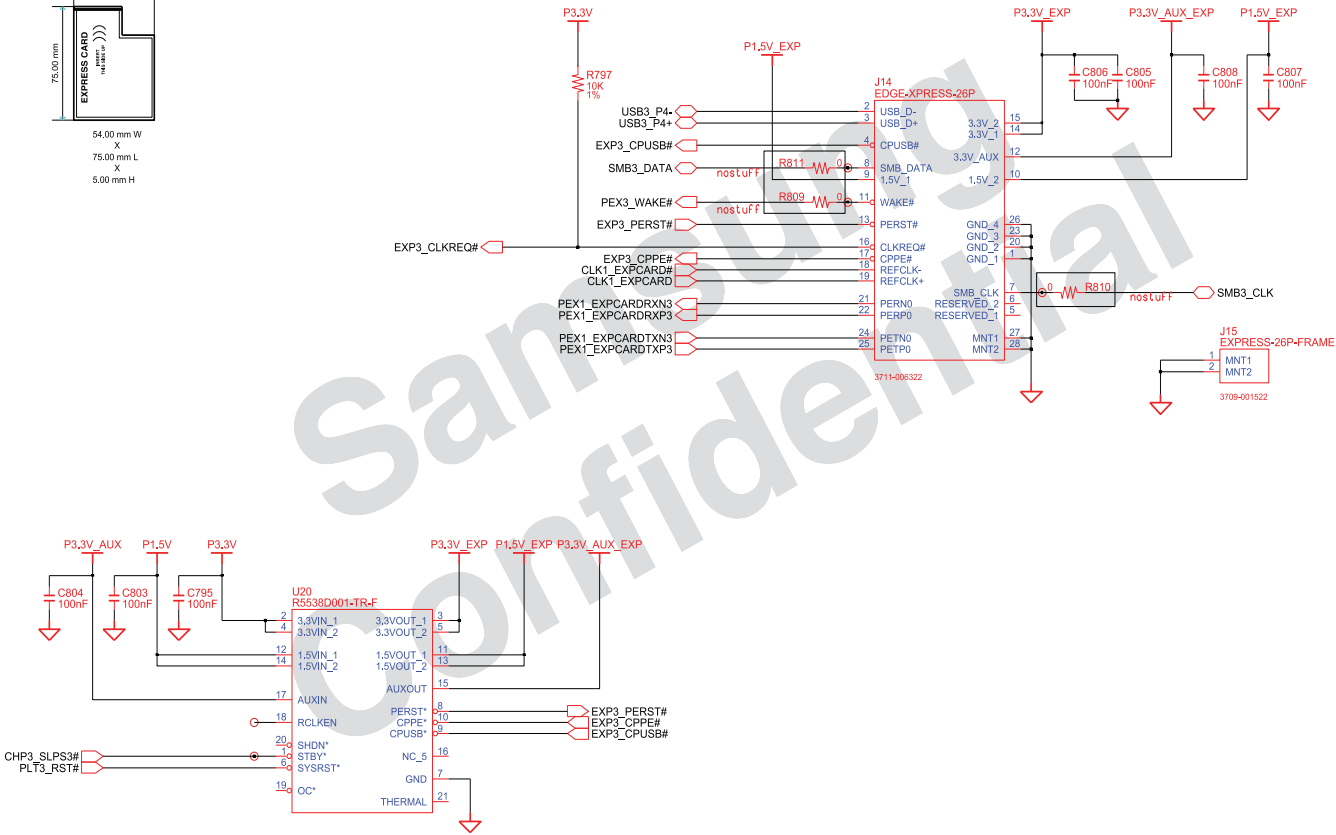
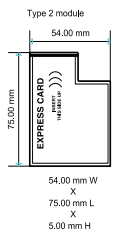
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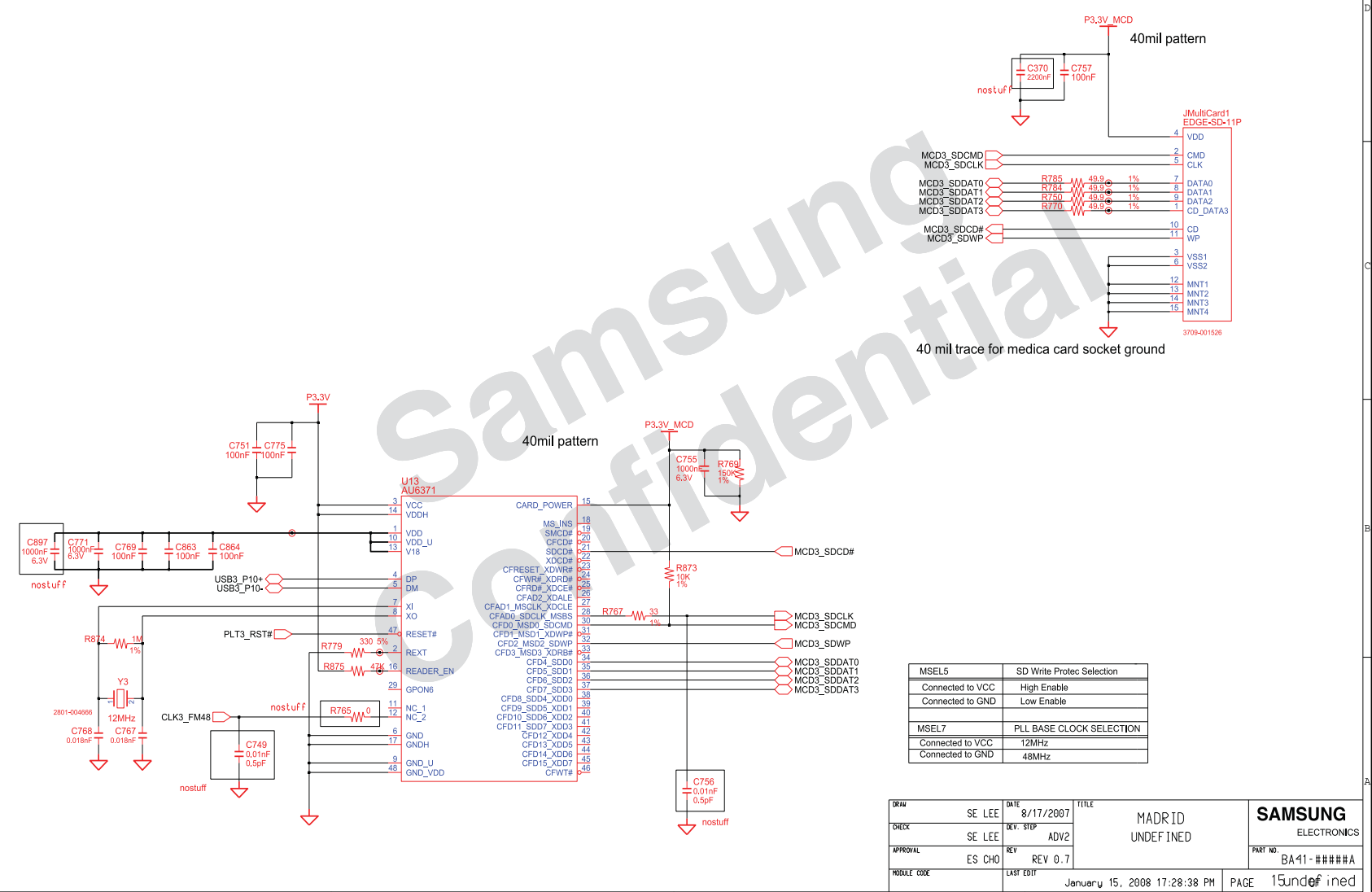
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P3.3V_MCD distance between R5U880 and socket should be less than 2 inches

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MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable

MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

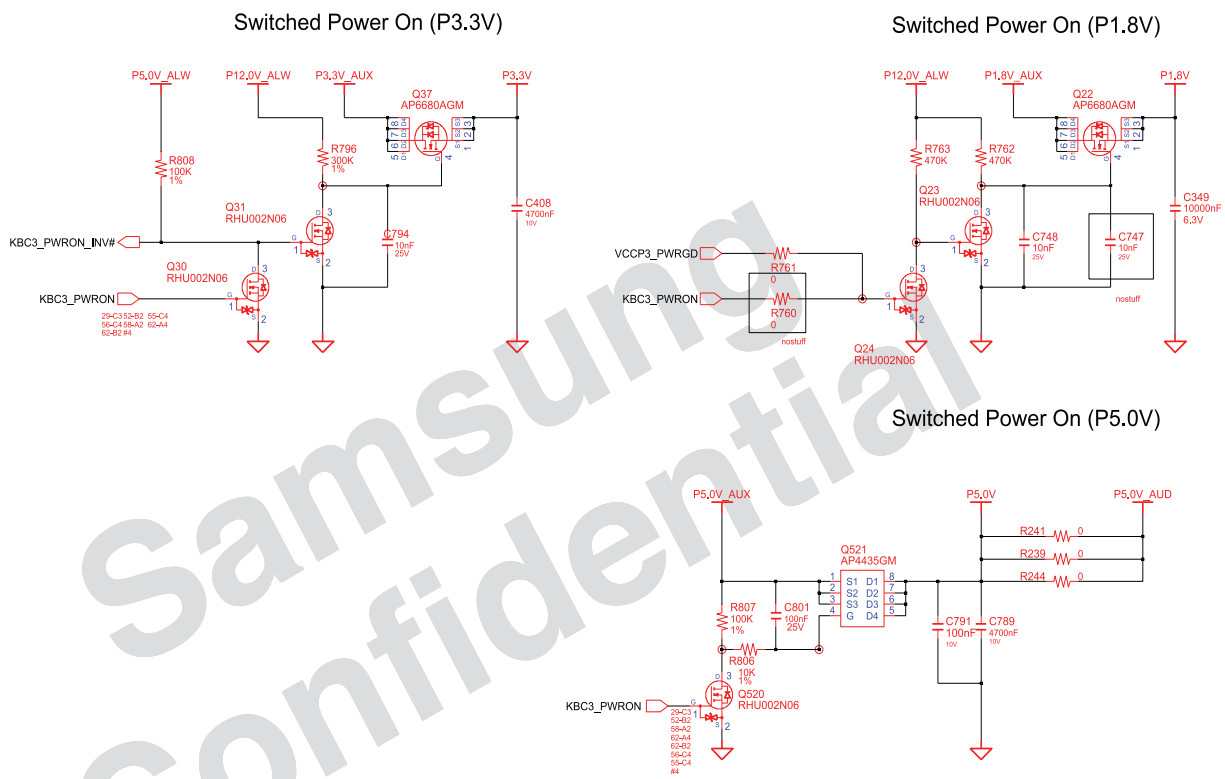
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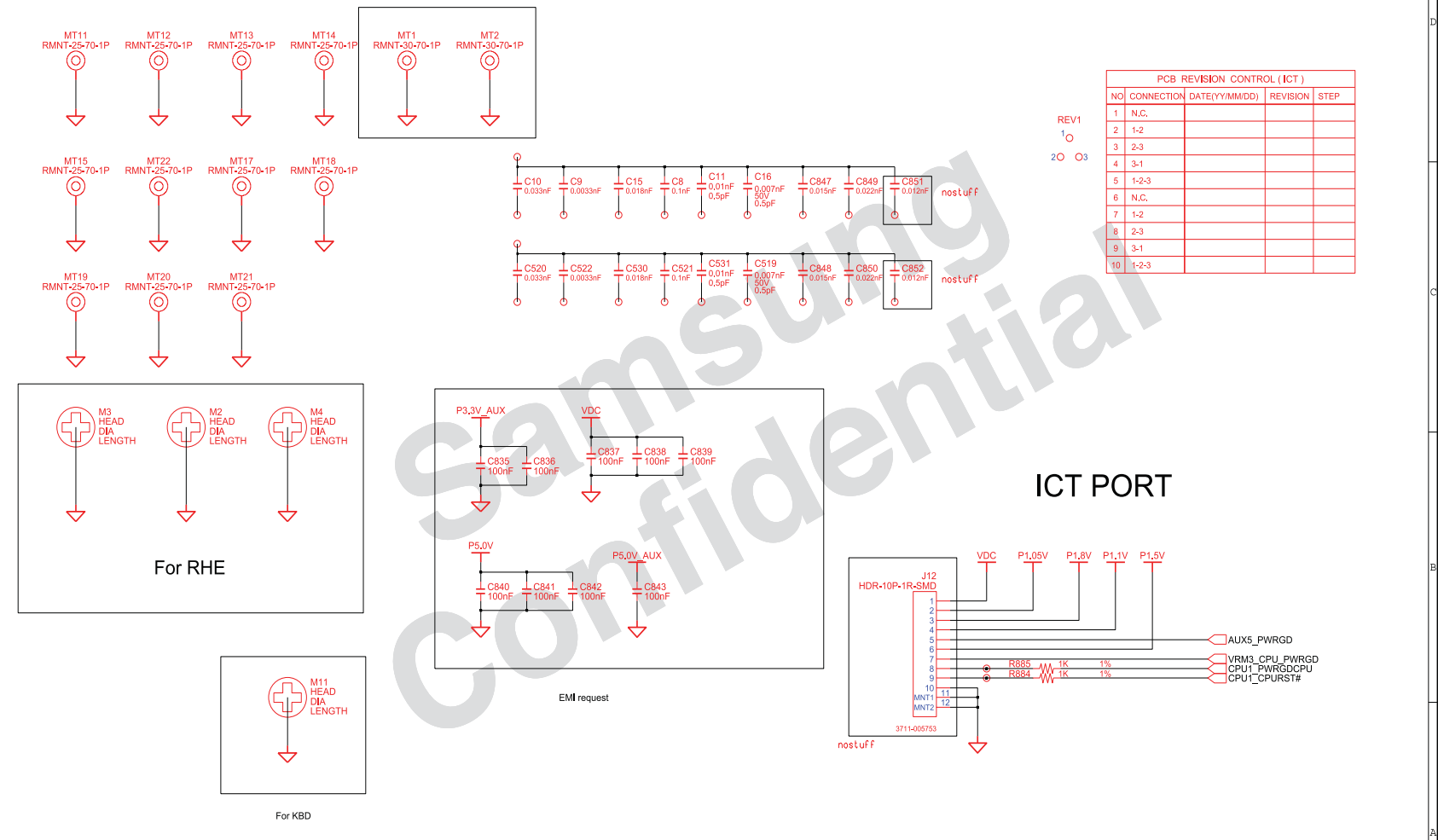
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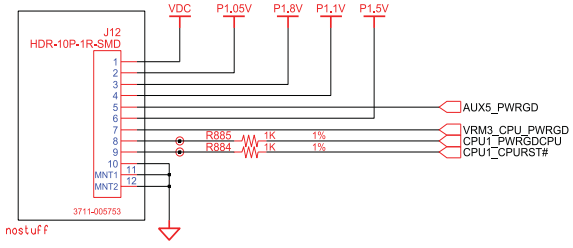
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PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV1
 1 0
 2 0 03



ICT PORT

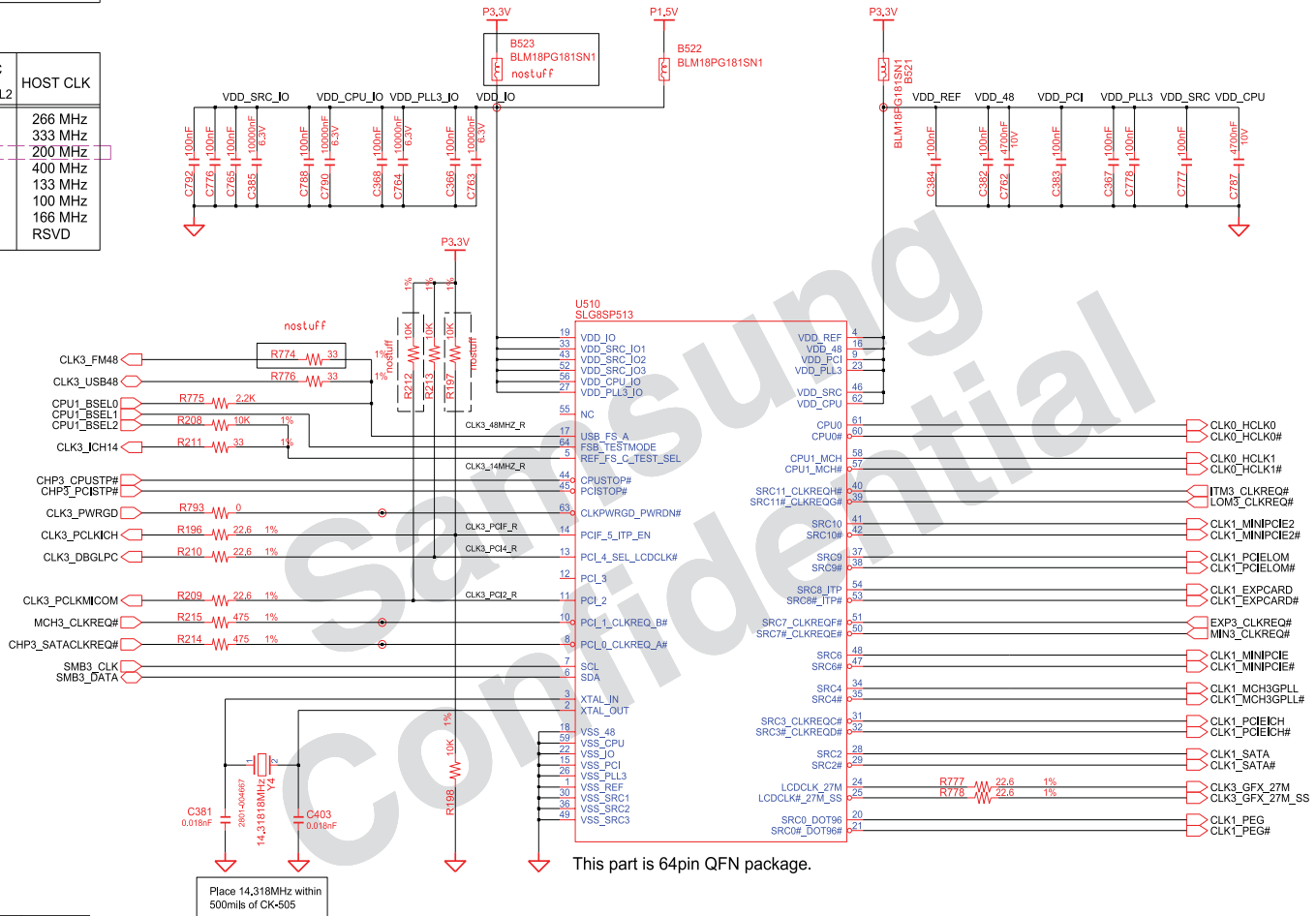


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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



Place 14.318MHz within 500mils of CK-505

This part is 64pin QFN package.

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	LOM3_CLKREQ#	SRC8

SEL_LCDCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG
CHECK	SE LEE	REV. STEP	ADV2	Main_Clock_Circuit		ELECTRONICS
APPROVAL	ES CHO	REV	REV 0.7	CK_Clock_505M		PART NO. BA41-#####
MODULE CODE	undefined	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1	OF 1

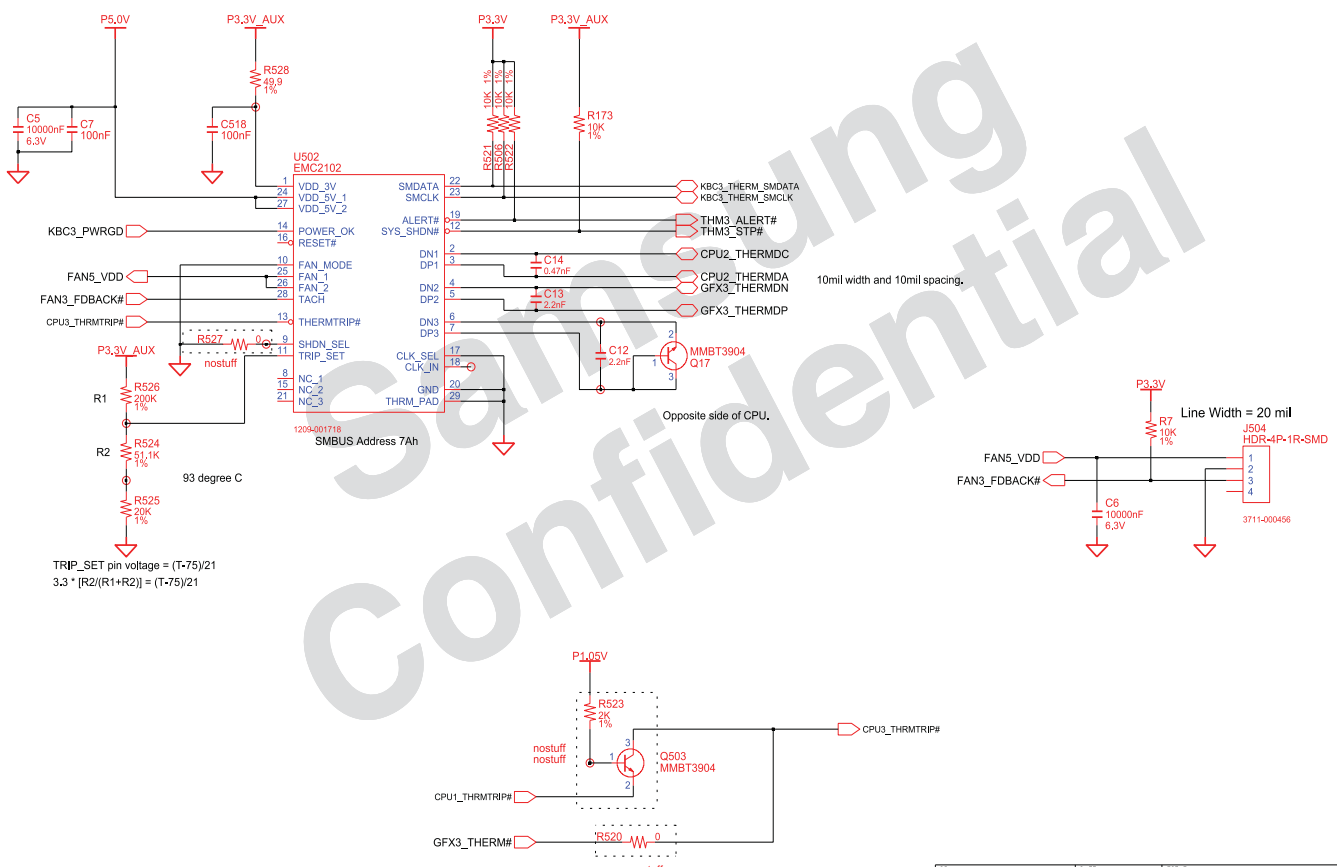
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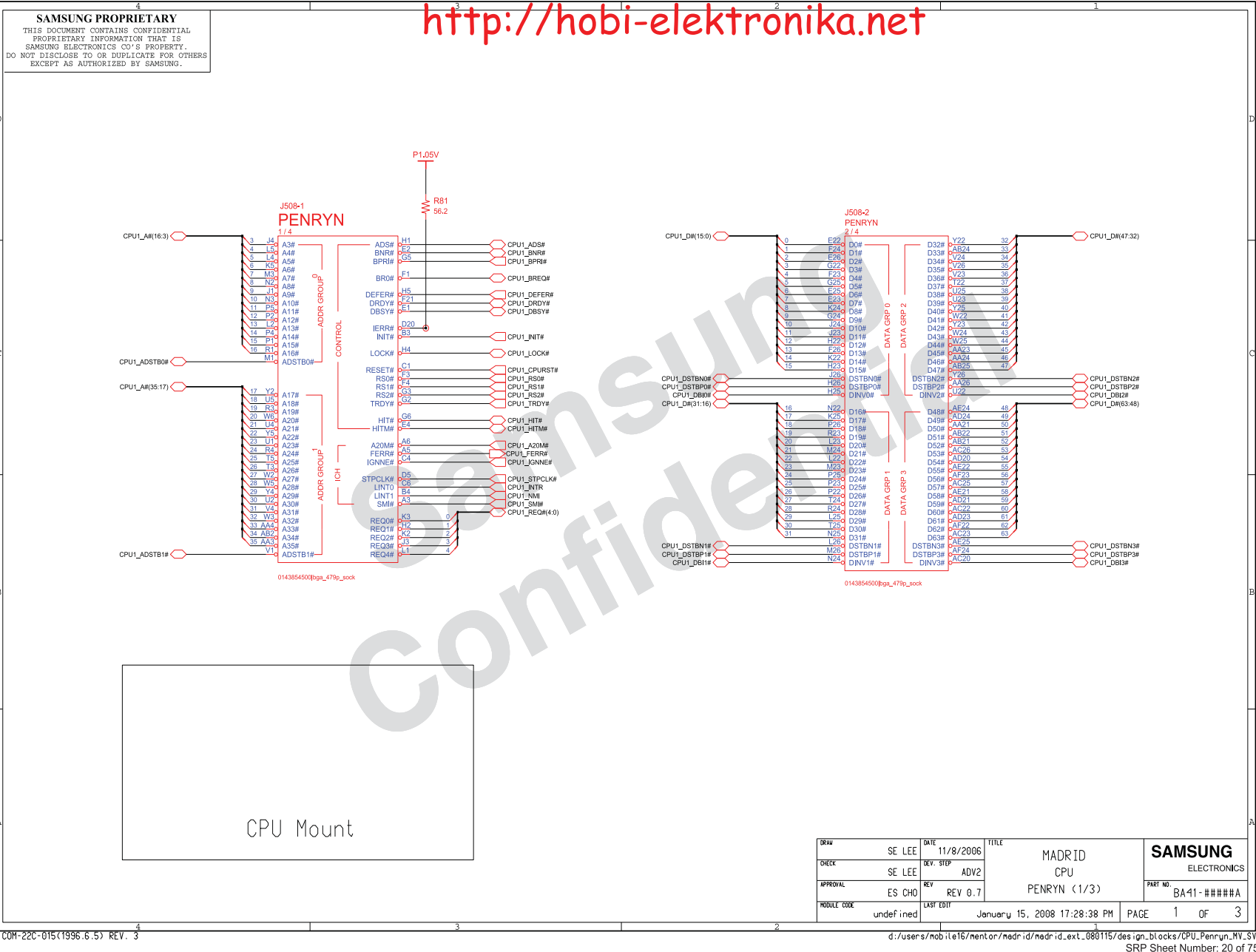
THERMAL SENSOR & FAN CONTROL



DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG
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APPROVAL	ES CHO	REV	REV 0.7	Thermal_Sensor_SMSC_Emc2102		PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM		PAGE	1 OF 1

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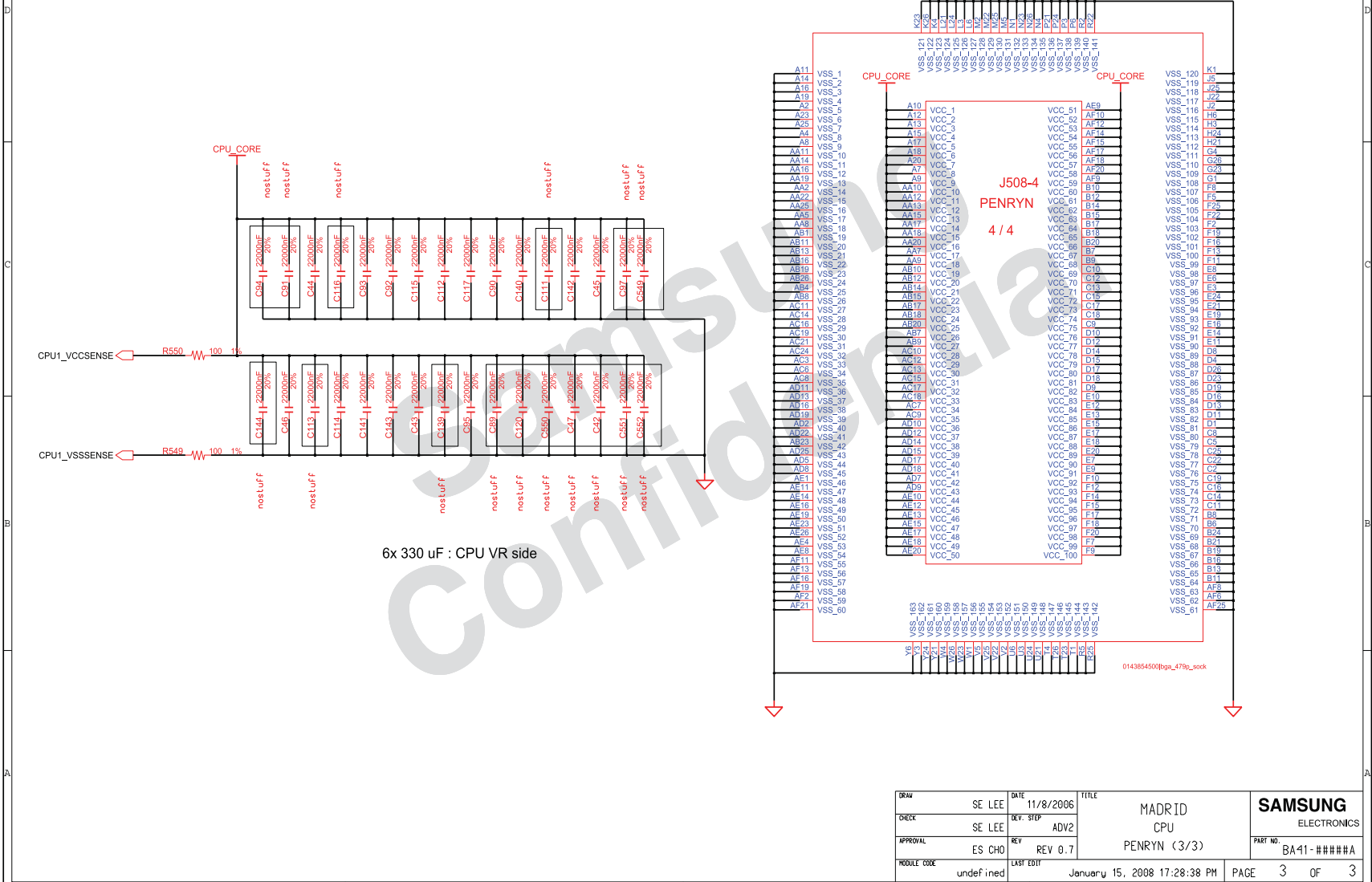


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DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID CPU PENRYN (1/3)	SAMSUNG ELECTRONICS PART NO. BA41-#####
CHECK	SE LEE	REV. STEP	ADV2			
APPROVAL	ES CHO	REV	REV 0.7			
MODULE CODE	undef in ed	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 3	

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6x 330 uF : CPU VR side

DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID CPU PENRYN (3/3)	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2			
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE	undef ined	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	3 OF 3	

8-22

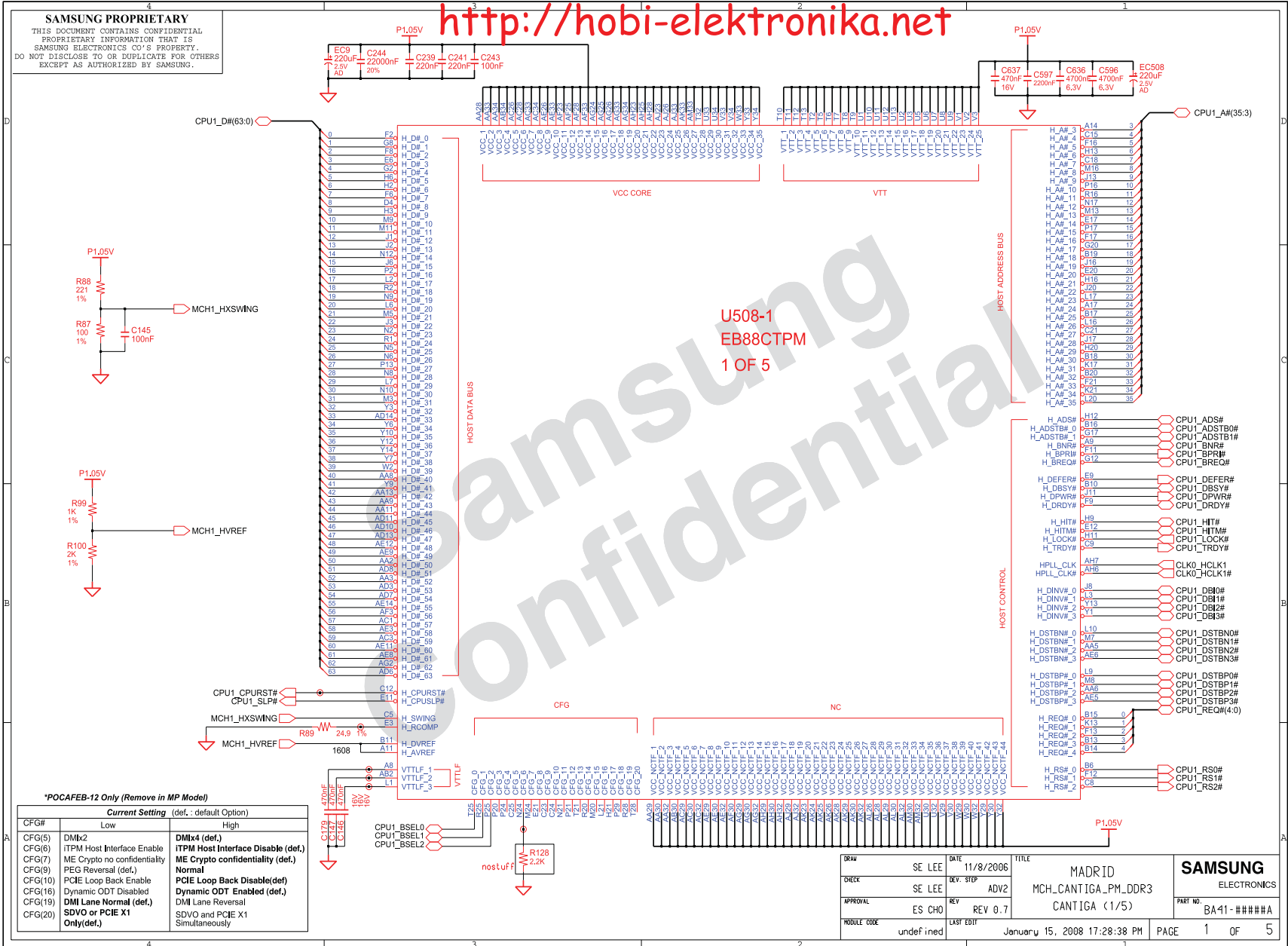
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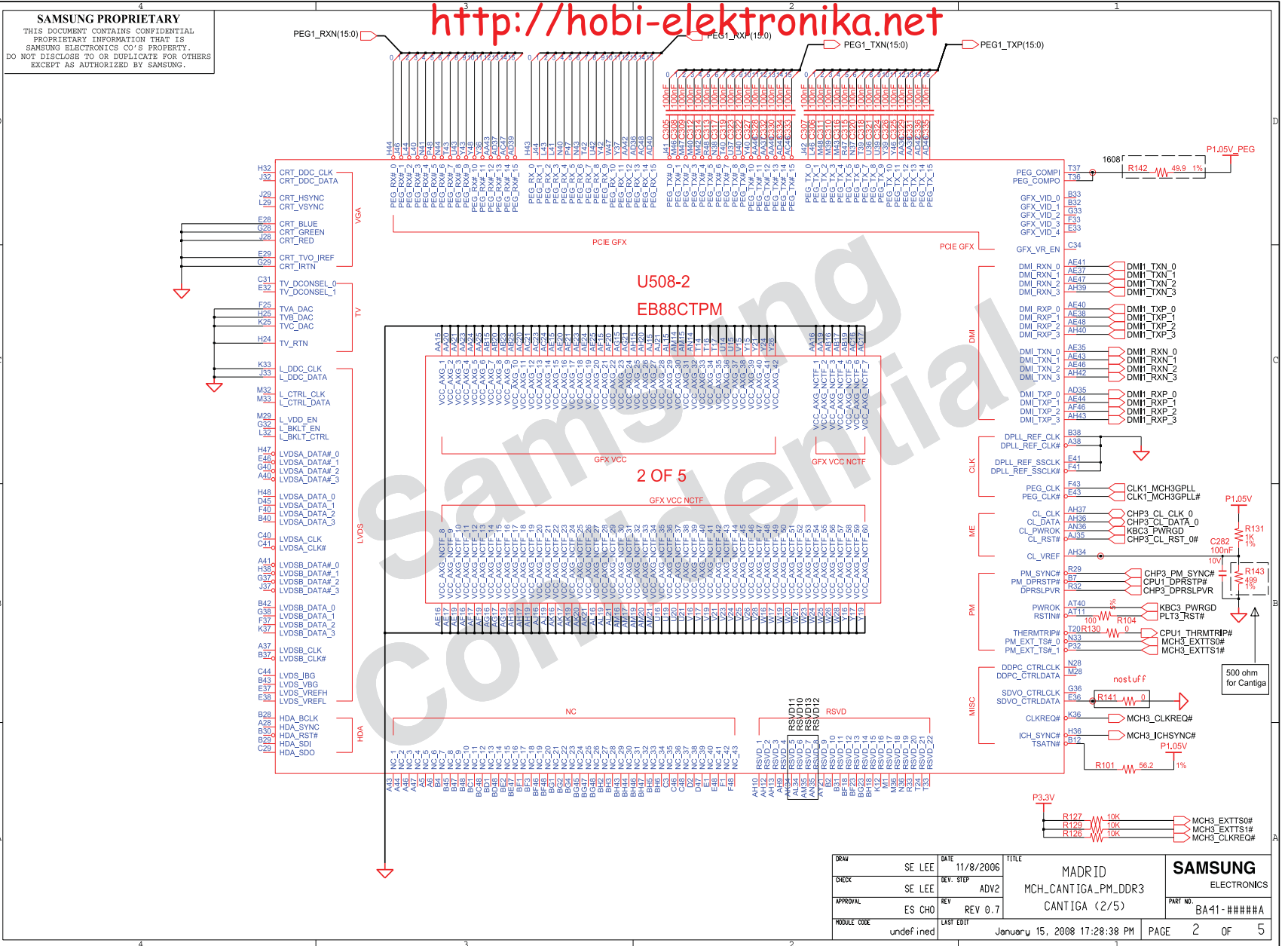
COH-22C-015(1996.6.5) REV. 3

d:\users\nob\el6\mentor\medrid\ext.080115\design_blocks\MCH_CANTIGA_PM_DDR3
 SRP Sheet Number: 23 of 75

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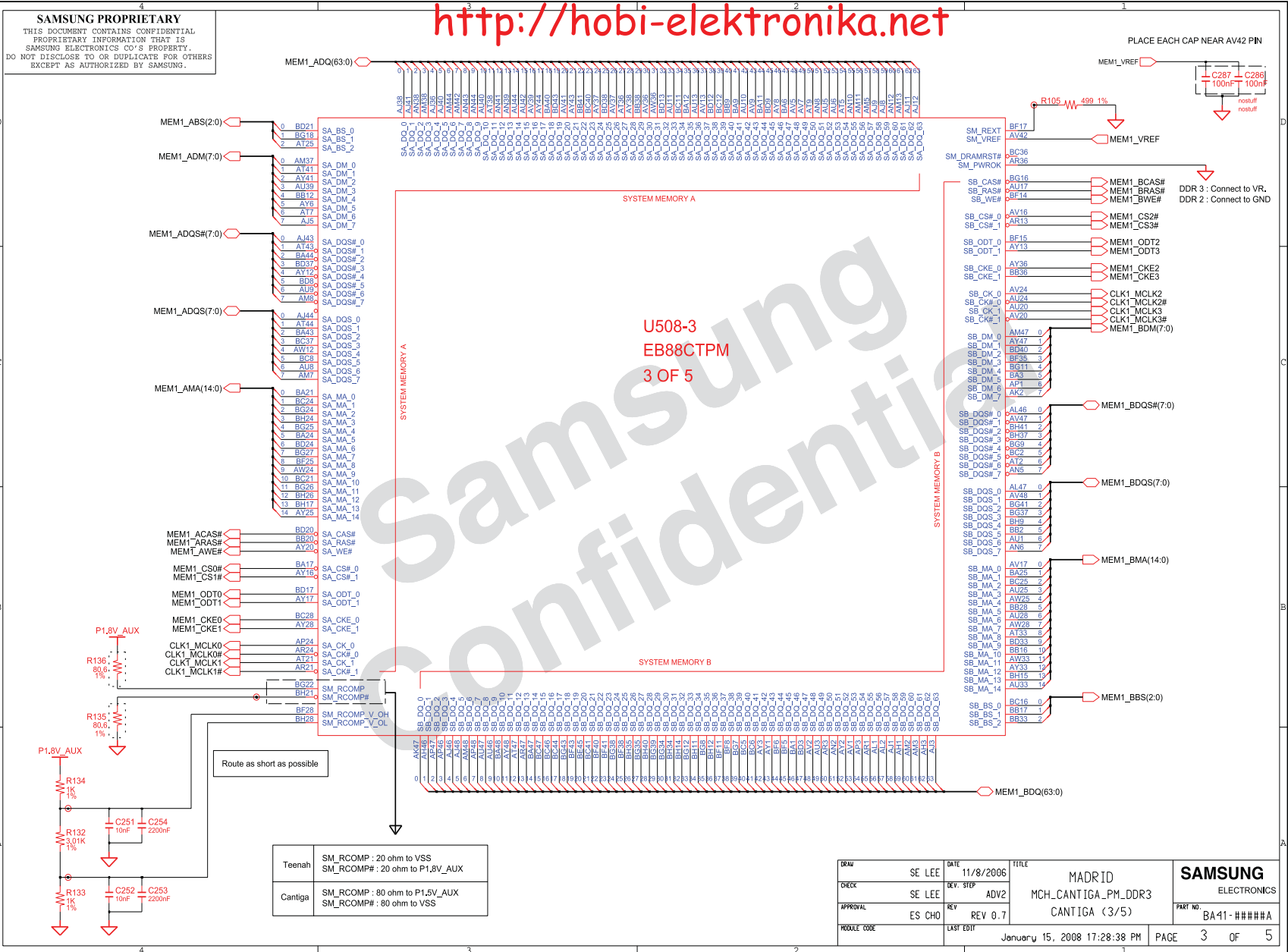


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APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE	undef in ed	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	2	OF 5

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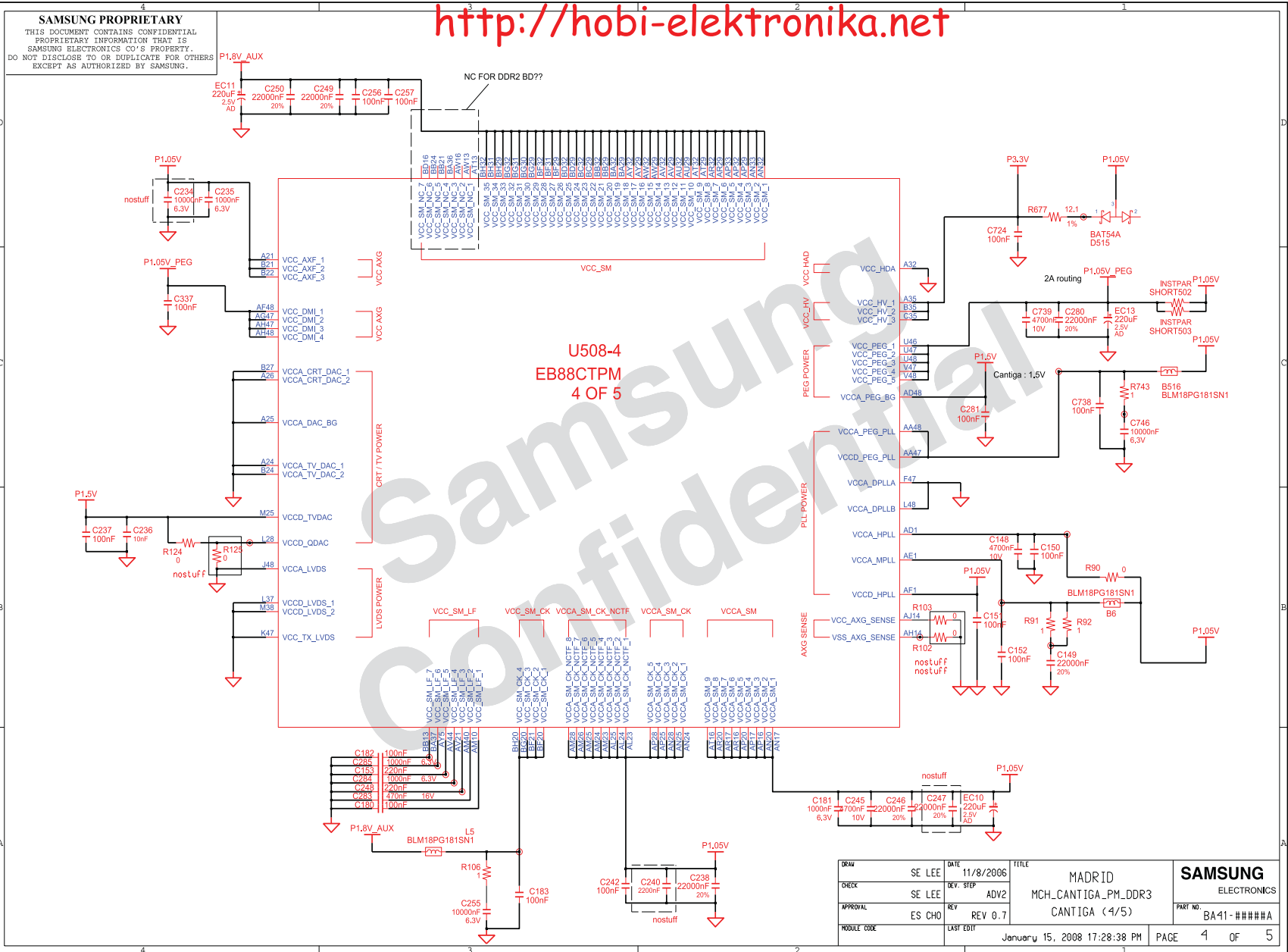
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Teenh	SM_RCMP# : 20 ohm to VSS SM_RCMP# : 20 ohm to P1.8V_AUX
Cantiga	SM_RCMP# : 80 ohm to P1.5V_AUX SM_RCMP# : 80 ohm to VSS

DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	MCH_CANTIGA_PM_DDR3		
APPROVAL	ES CHO	REV	REV 0.7	CANTIGA (3/5)		PART NO. BA41-#####
PROJ. CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	3 OF 5	



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U508-4
EB88CTPM
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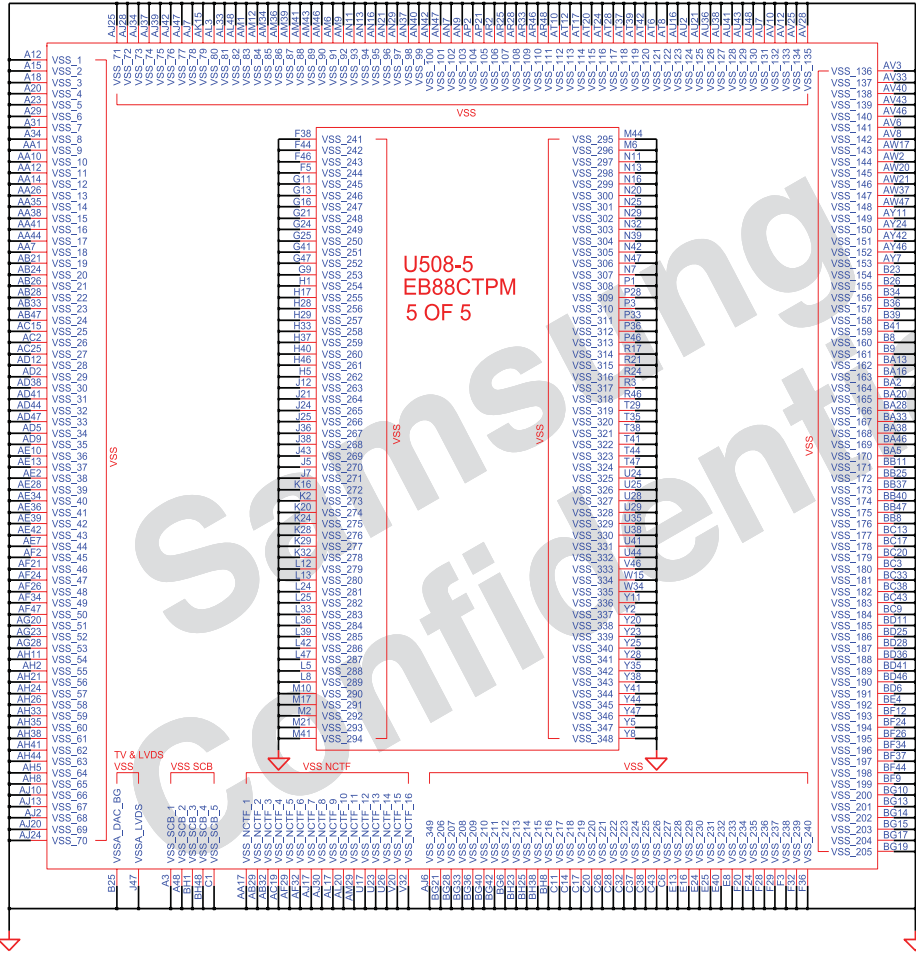
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APPROVAL	ES CHO	REV	REV 0.7	CANTIGA (4/5)	BA41-#####	
MODULE CODE		LAST EDIT		January 15, 2008 17:28:38 PM	PAGE	4 OF 5

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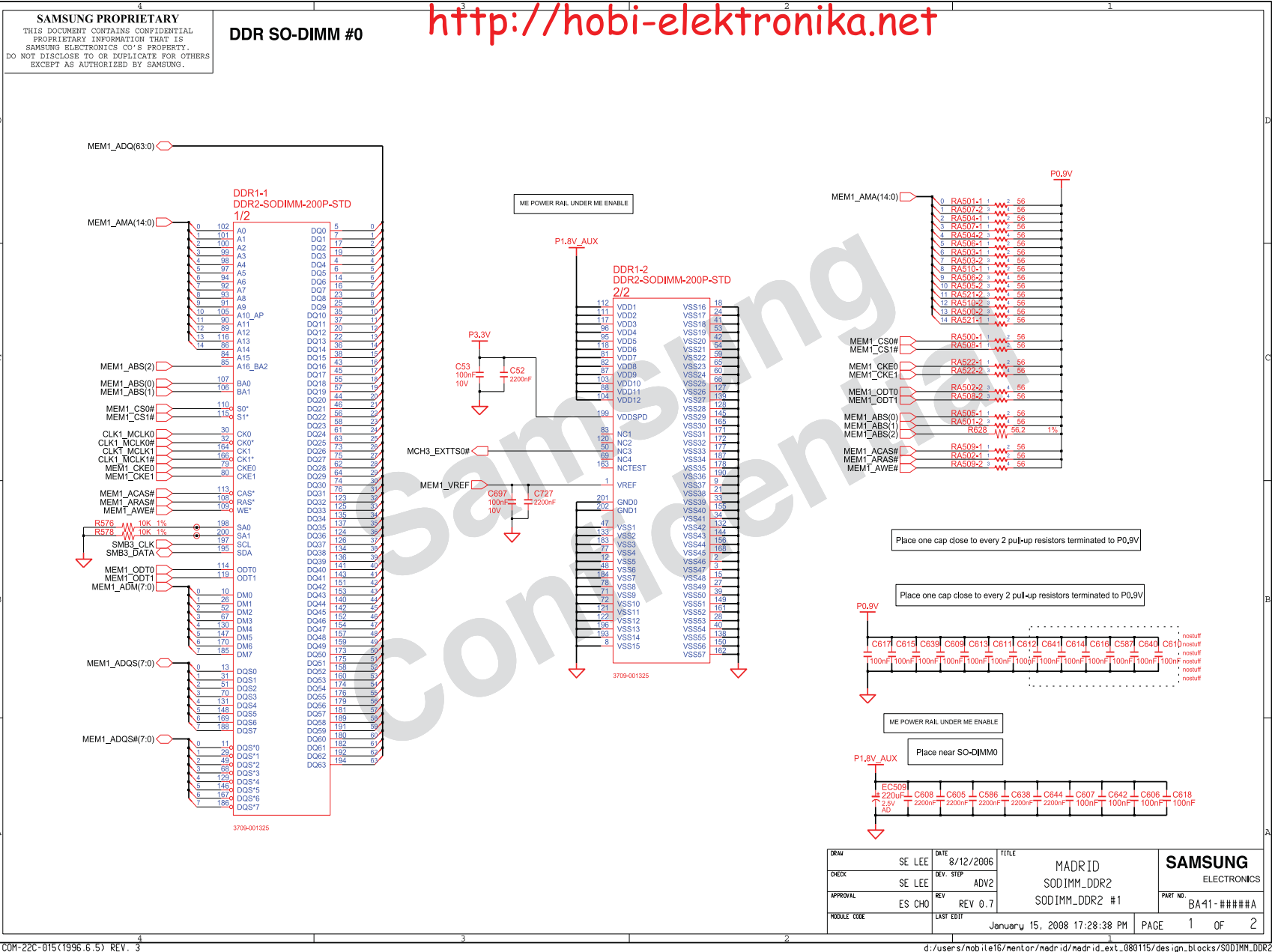
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DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	MCH_CANTIGA_PM_DDR3		
APPROVAL	ES CHO	REV	REV 0.7	CANTIGA (5/5)		PART NO. BA41-#####
MODULE CODE	LAST EDIT		January 15, 2008 17:28:38 PM		PAGE	5 OF 5

8. 블록도 및 회로도

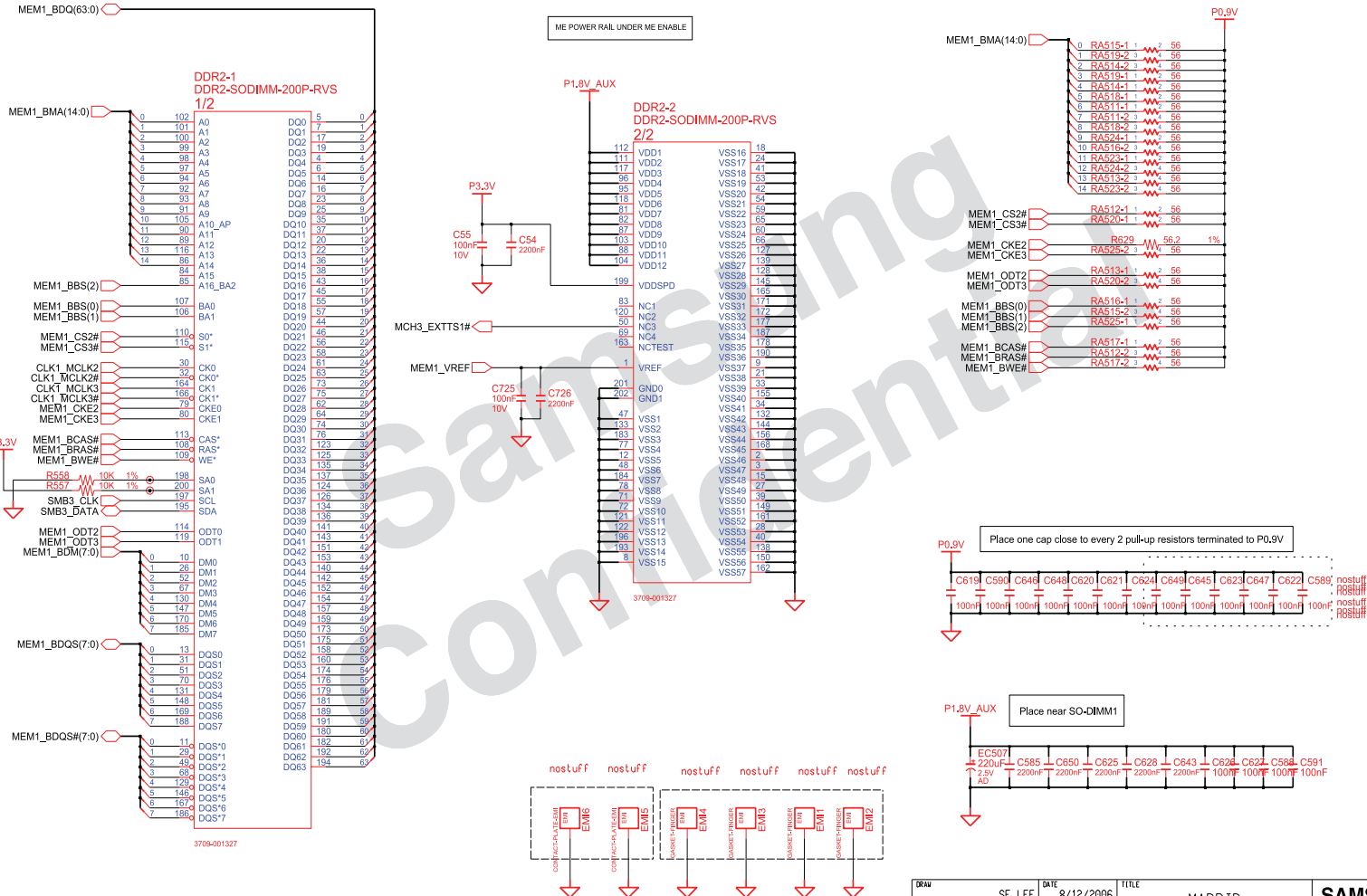
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DDR SO-DIMM #1

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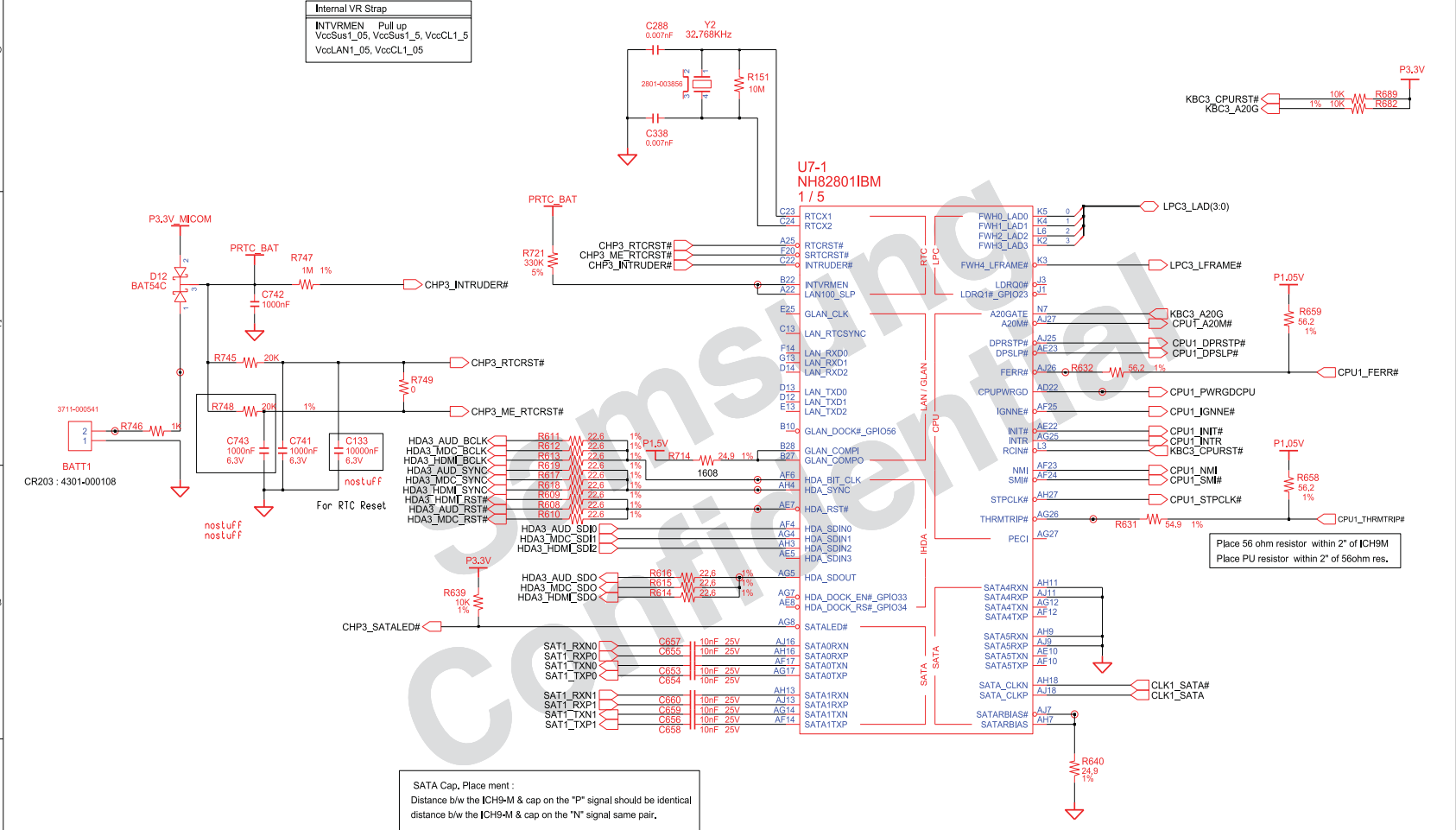
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DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	SODIMM_DDR2		
APPROVAL	ES CHO	REV	REV 0.7	SODIMM_DDR2 #2		
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	2	OF 2

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Internal VR Strap
 INTVRMEN Pull up
 VccSus1_05, VccSus1_5, VccCL1_5
 VccLAN1_05, VccCL1_05



SATA Cap. Place ment :
 Distance b/w the ICH9-M & cap on the "P" signal should be identical
 distance b/w the ICH9-M & cap on the "N" signal same pair.

Place 56 ohm resistor within 2" of ICH9M
 Place PU resistor within 2" of 56ohm res.

DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID ICH9M_B	SAMSUNG ELECTRONICS
CHECK	SE LEE	DEV. STEP	ADV2		ICH9-M (1/5)	
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
PROJ. CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 5	

8. 블록도 및 회로도

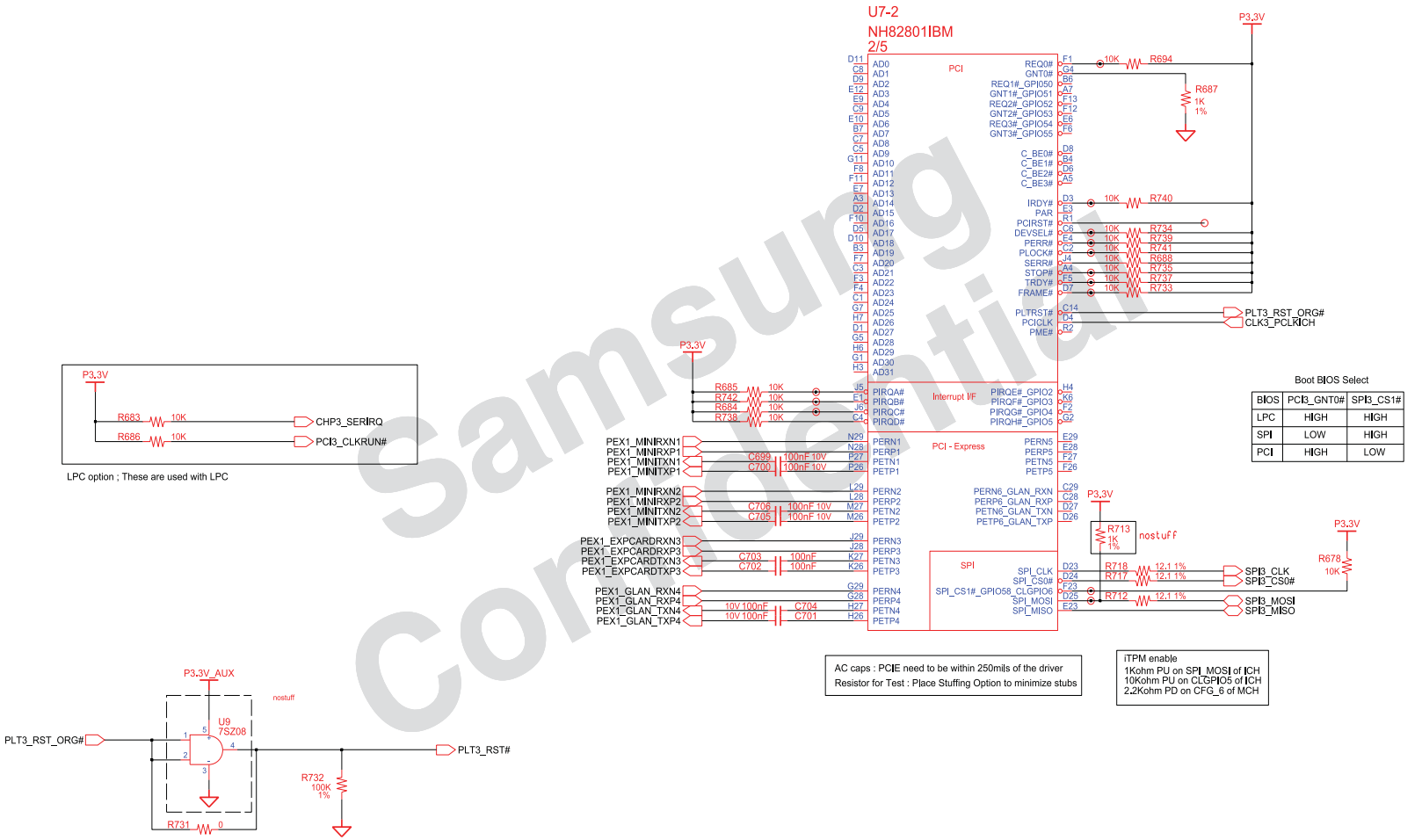
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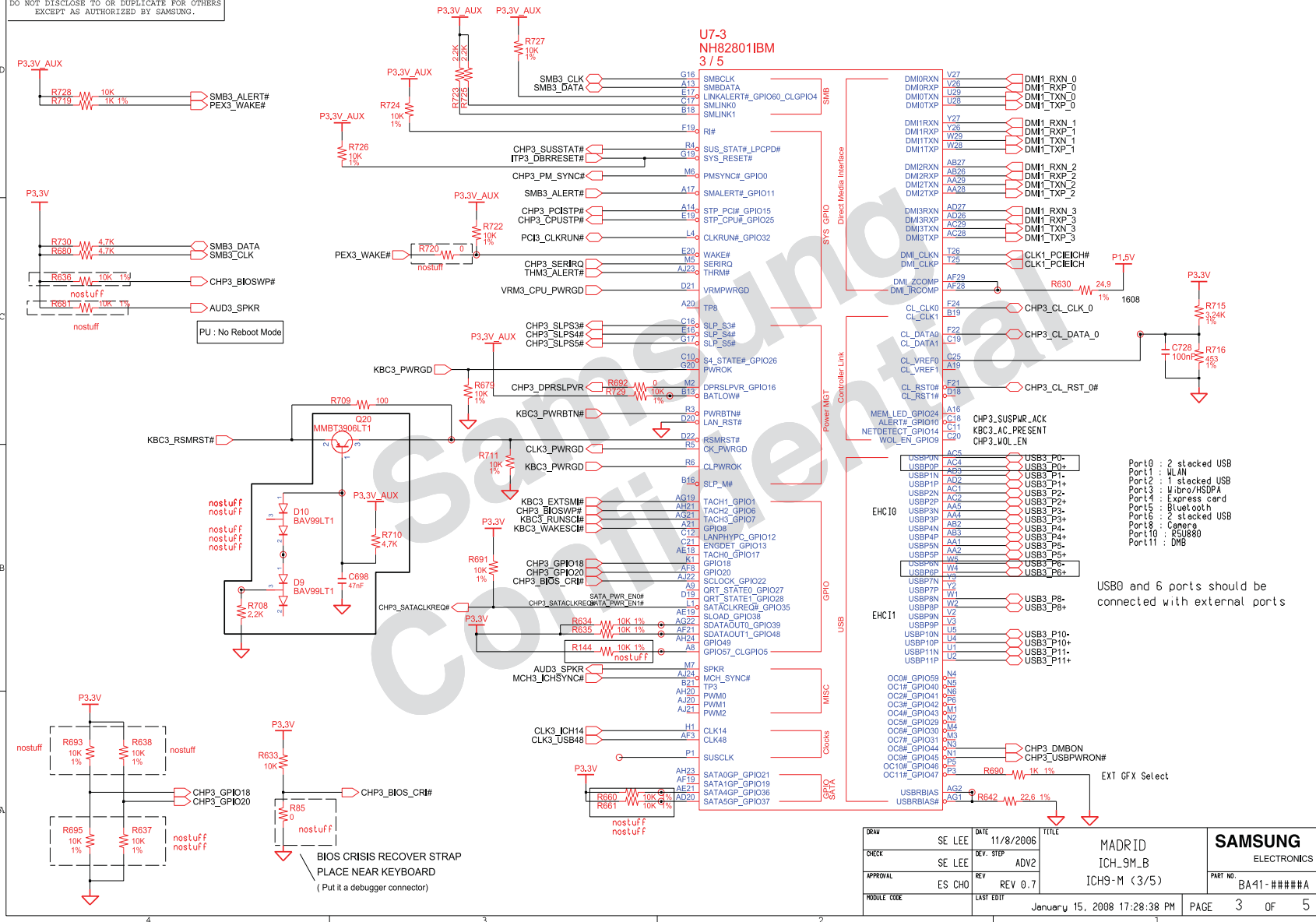
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DATE	11/8/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
SE LEE				
DEV_STEP	ADV2		MADRID	PART NO. BA41-#####
SE LEE				
REV	REV 0.7		ICH9_M_B	PAGE 2 OF 5
ES CHO			ICH9-M (2/5)	
LAST EDIT	January 15, 2008 17:28:38 PM			

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DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID ICH9M.B	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2		PART NO. BA41-#####	
APPROVAL	ES CHO	REV	REV 0.7			
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	3 OF 5	

8. 블록도 및 회로도

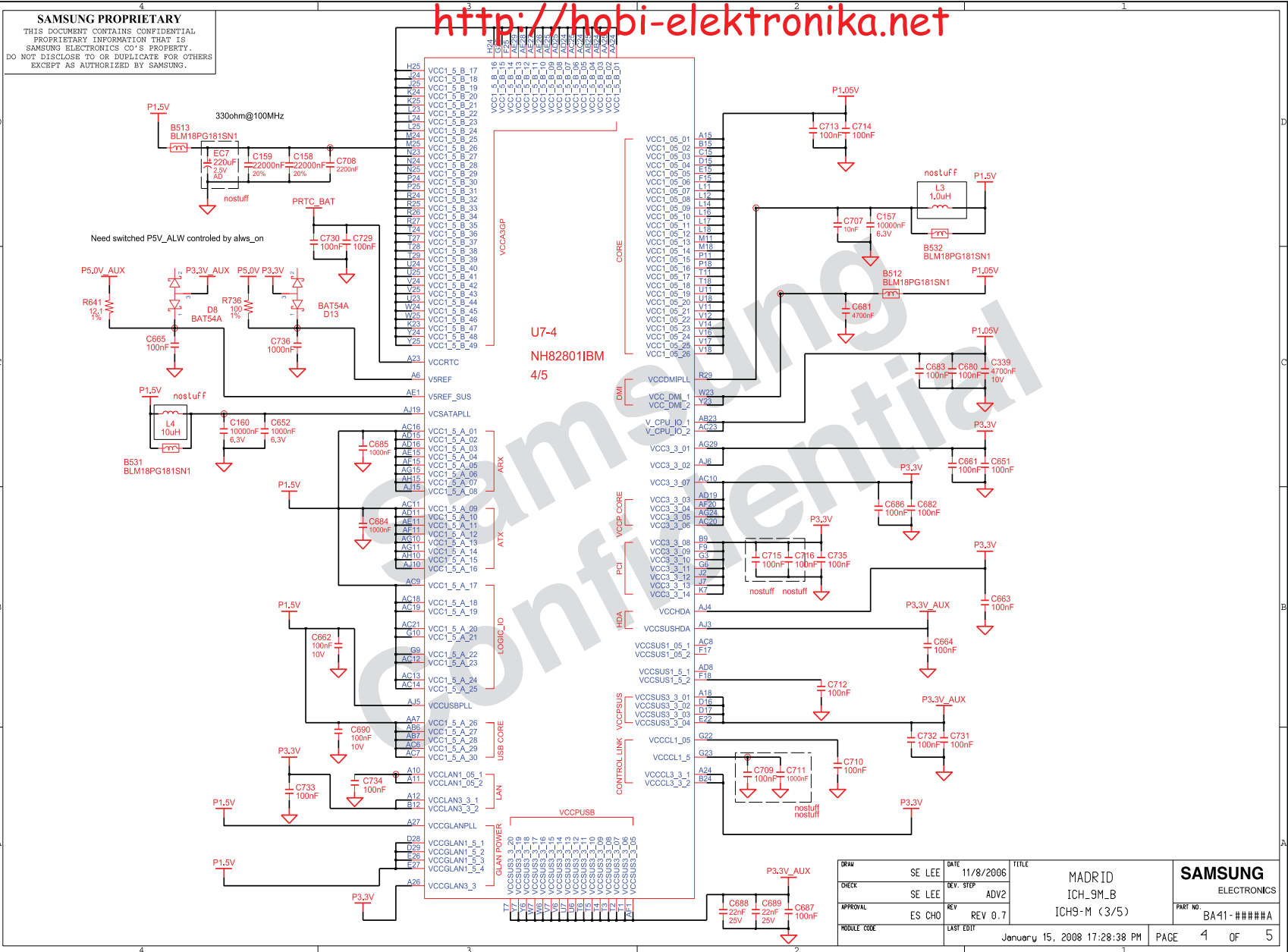
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USB0 and 6 ports should be connected with external ports

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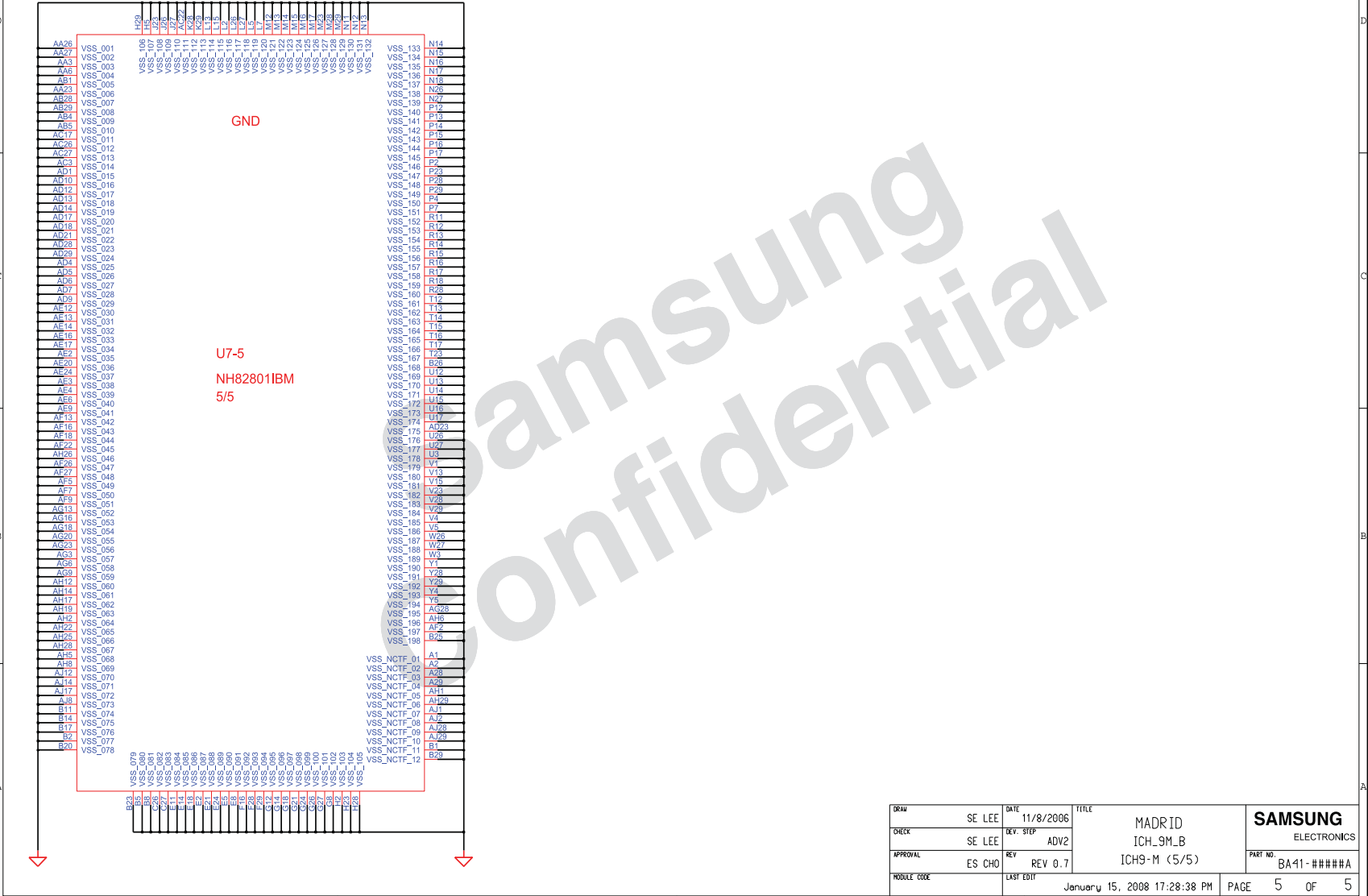
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DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
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APPROVAL	ES CHO	REV	REV 0.7		ICH9-M (3/5)	PART NO. BA419-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	4	OF 5

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DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID ICH9M_B	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2		ICH9-M (5/5)	
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	5	OF 5

8. 블록도 및 회로도

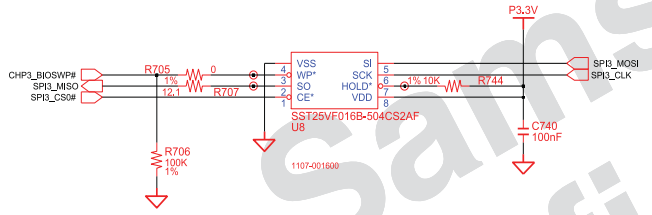
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- SPI ROM LIST -

Macronix - MX25L8005M2C-15G
 -> 1107-001646

STM - M25PE80
 -> 1107-001674



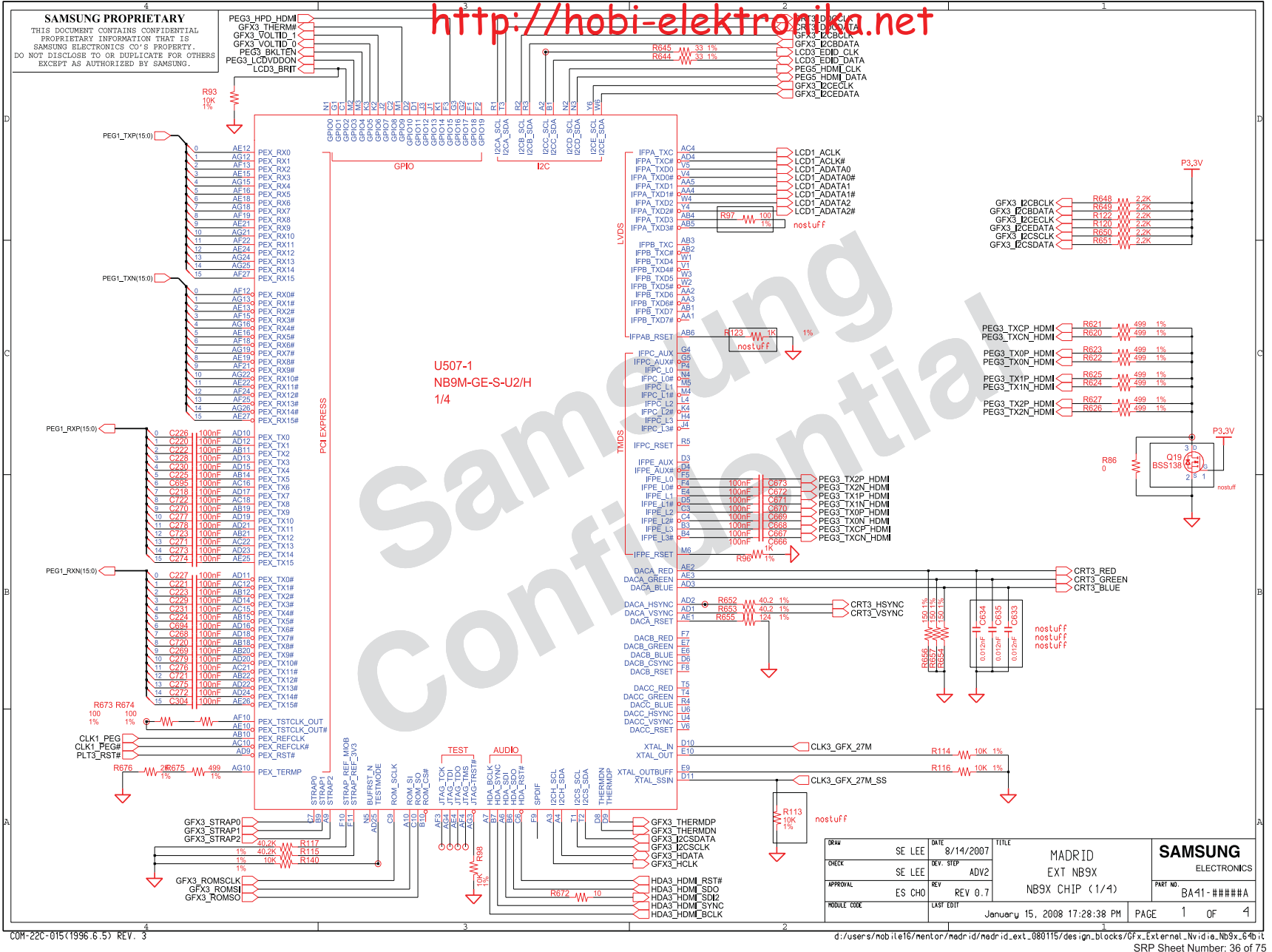
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPOMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY " PRESS SETUP"	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

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DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	SPI_BIOS_ROM		
APPROVAL	ES CHO	REV	REV 0.7	SPI_BIOS_ROM	PART NO.	BA41-#####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1	OF 1

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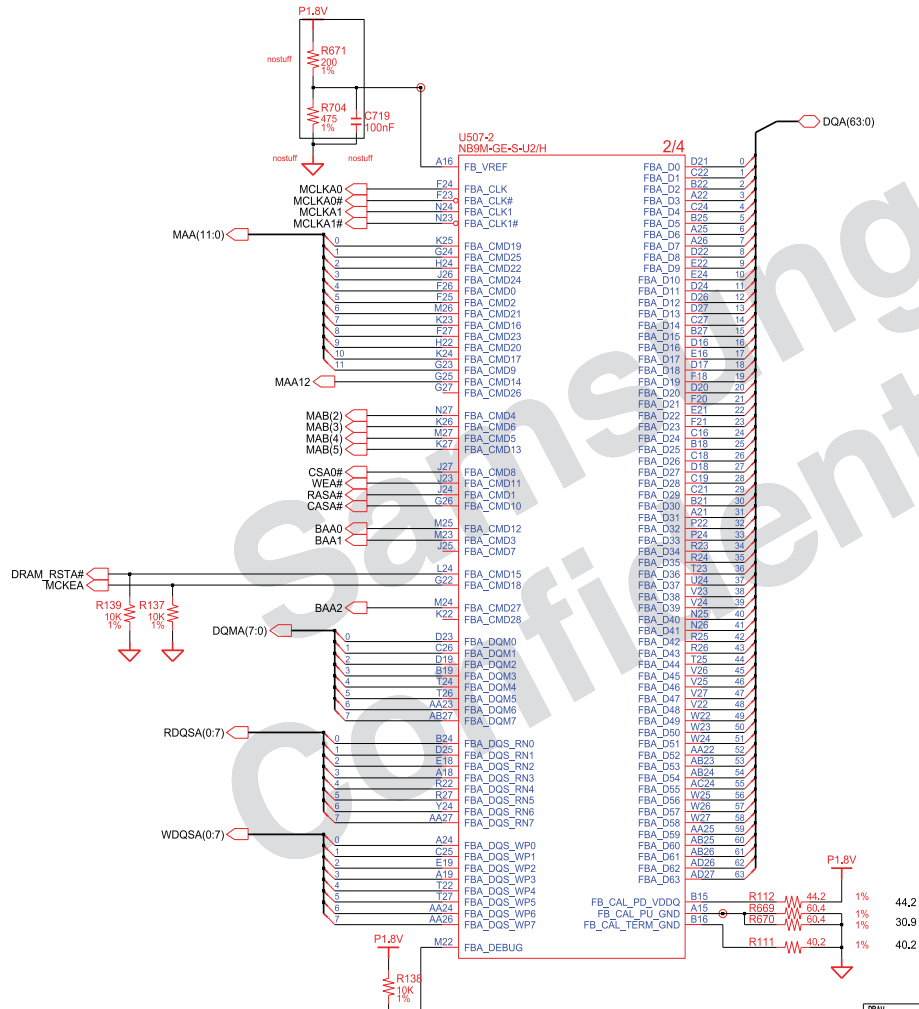


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U507-1
NB9M-GE-S-U2/H
1/4

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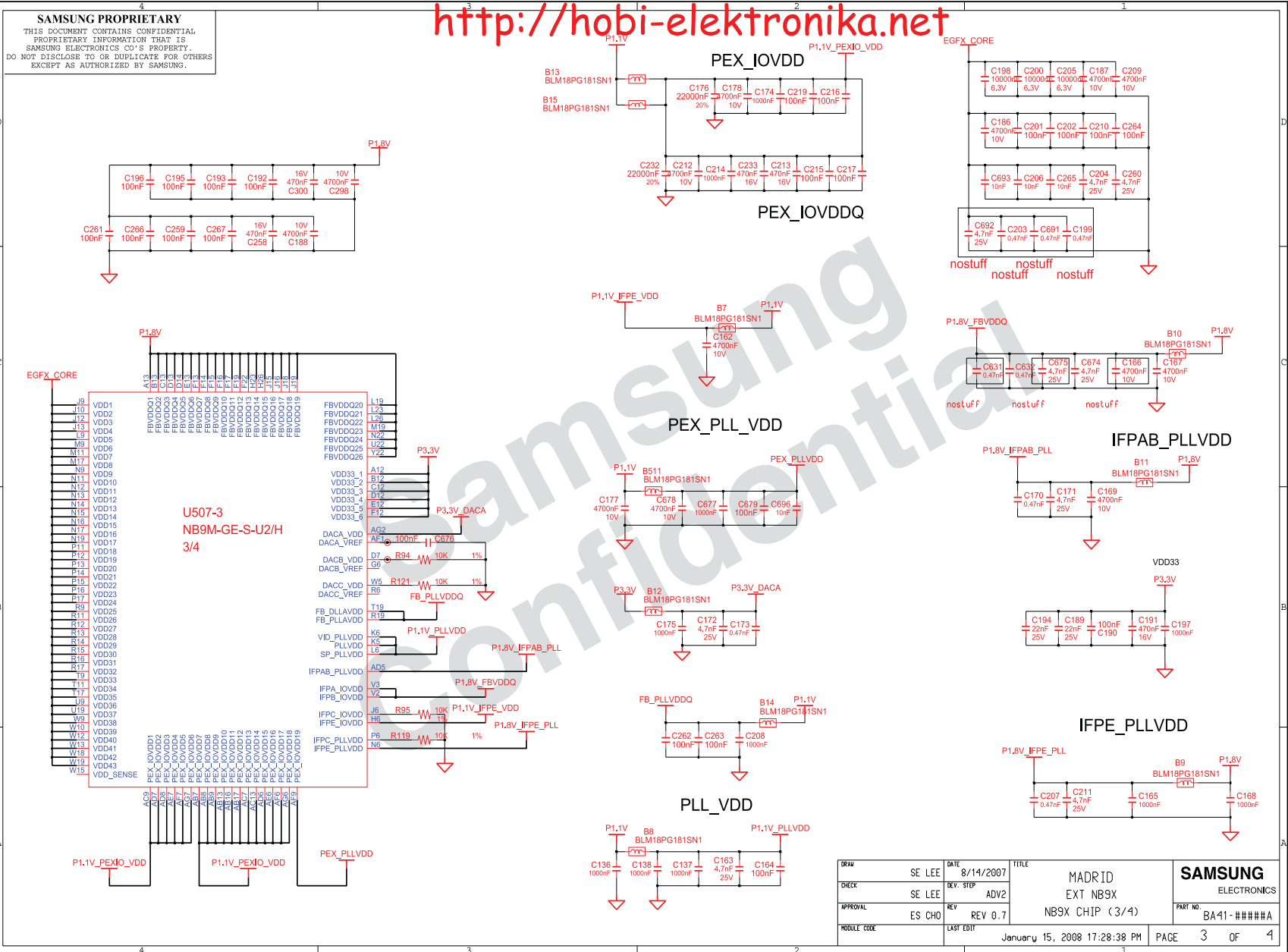
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CHECK	SE LEE	DEV. STEP	ADV2	EXT NB9X		
APPROVAL	ES CHO	REV	REV 0.7	NB9X CHIP (2/4)		PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	2	OF 4

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CHECK	SE LEE	REV. STEP	ADV2	NB9X CHIP (3/4)		
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE	LAST EDIT			January 15, 2008 17:28:38 PM		PAGE 3 OF 4

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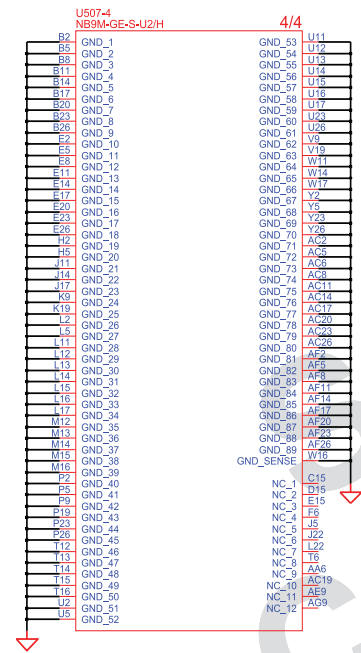
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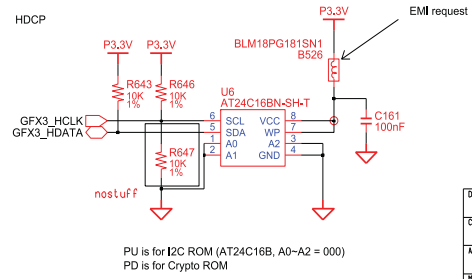
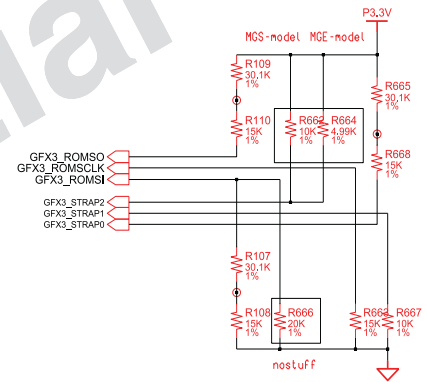
Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU VID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU VID1	NC
GPIO(7)	GPU VID2 or Mem VID	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan control	NC
GPIO(10)	Memory VREF switch	NC
GPIO(11)	SLI Rater sync	HIGH
GPIO(12)	AC Power decton input	NC
GPIO(13)	Power supply control	NC
GPIO(14)	Power supply control	NC
GPIO(15)	HDMI Detect	High
GPIO(16)	DP Detect	High

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_27	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	DEVID[4]	VEND	CLK_CFG	PULL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

Resistor value	PU to VDD	PD to GND	XCLK27 = 1.27MHz
5K ohm	1000	0000	RAM_CFG (SEC)
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit
15K ohm	1010	0010	USER[3:0]=1111 for EDD
20K ohm	1011	0011	PADCFG[3:0]=0001 of NP
25K ohm	1100	0100	[NB9M-GS:0x06E9 (01001)
30K ohm	1101	0101	NB9M-GS:0x06E8 (01000)
35K ohm	1110	0110	NB9P-GS:0x0649 (01001)
45K ohm	1111	0111	NB9P-GS:0x0646 (00110)
			NB9P-GE2:0x07?? (0????)



	Bit3	Bit2	Bit1	Bit0
ROMSO	1	1	1	1
SCLK	0	0	1	0
SI	0	0	1	1
Strap2	1	0	0	1
Strap1	0	0	0	1
Strap0	1	1	1	1



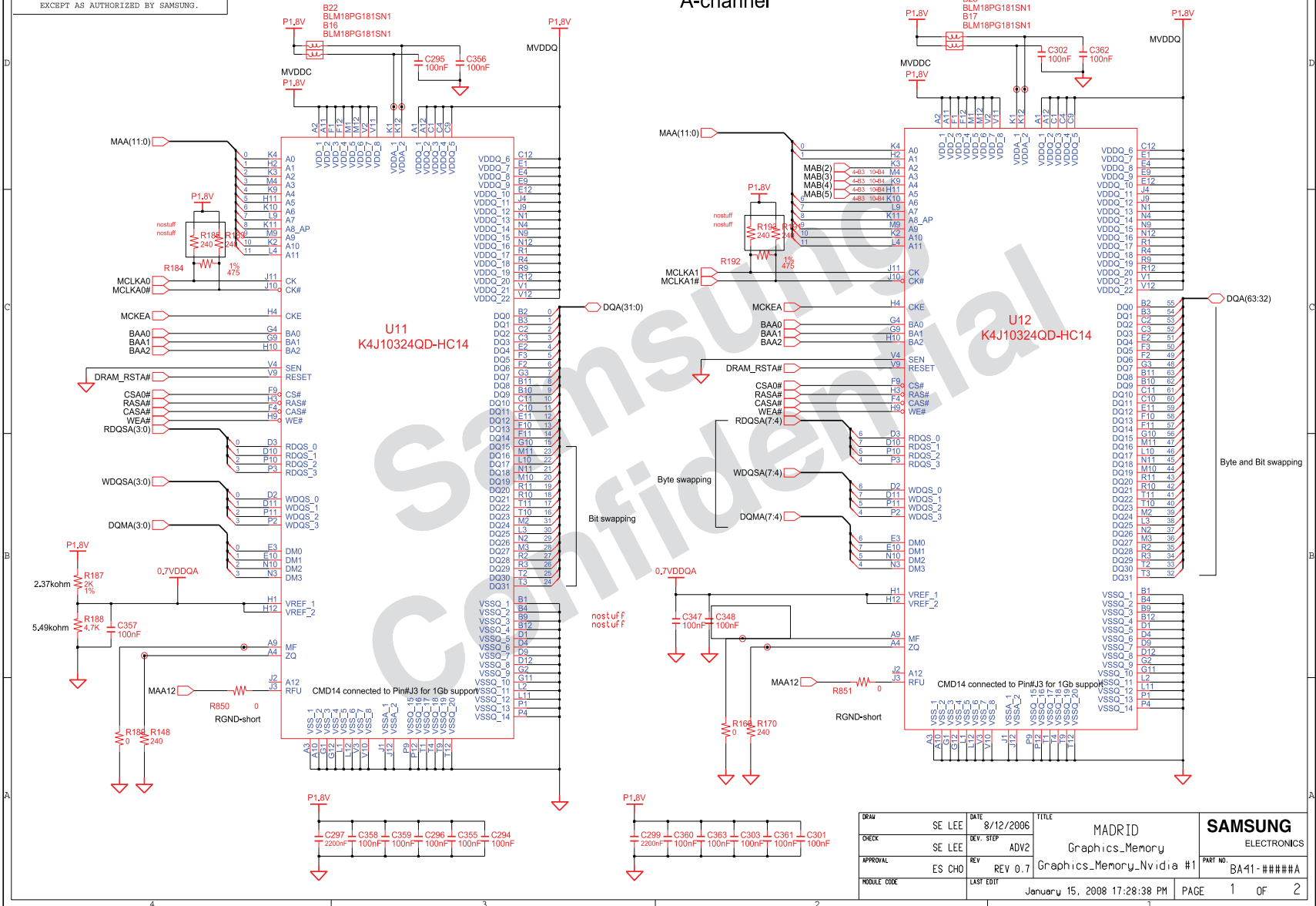
DRW	SE LEE	DATE	8/14/2007	TITLE	MADRID	SAMSUNG
CHECK	SE LEE	DEV. STEP	ADV2		EXT NB9X	ELECTRONICS
APPROVAL	ES CHO	REV	REV 0.7		NB9X CHIP (4/4)	PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM		PAGE	4 OF 4

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A-channel



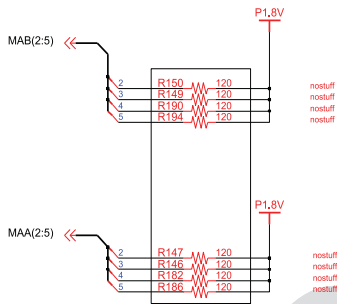
DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	DEV. STEP	ADV2	Graphics_Memory		
APPROVAL	ES CHO	REV	REV 0.7	Graphics_Memory_Nvidia #1		PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 2	

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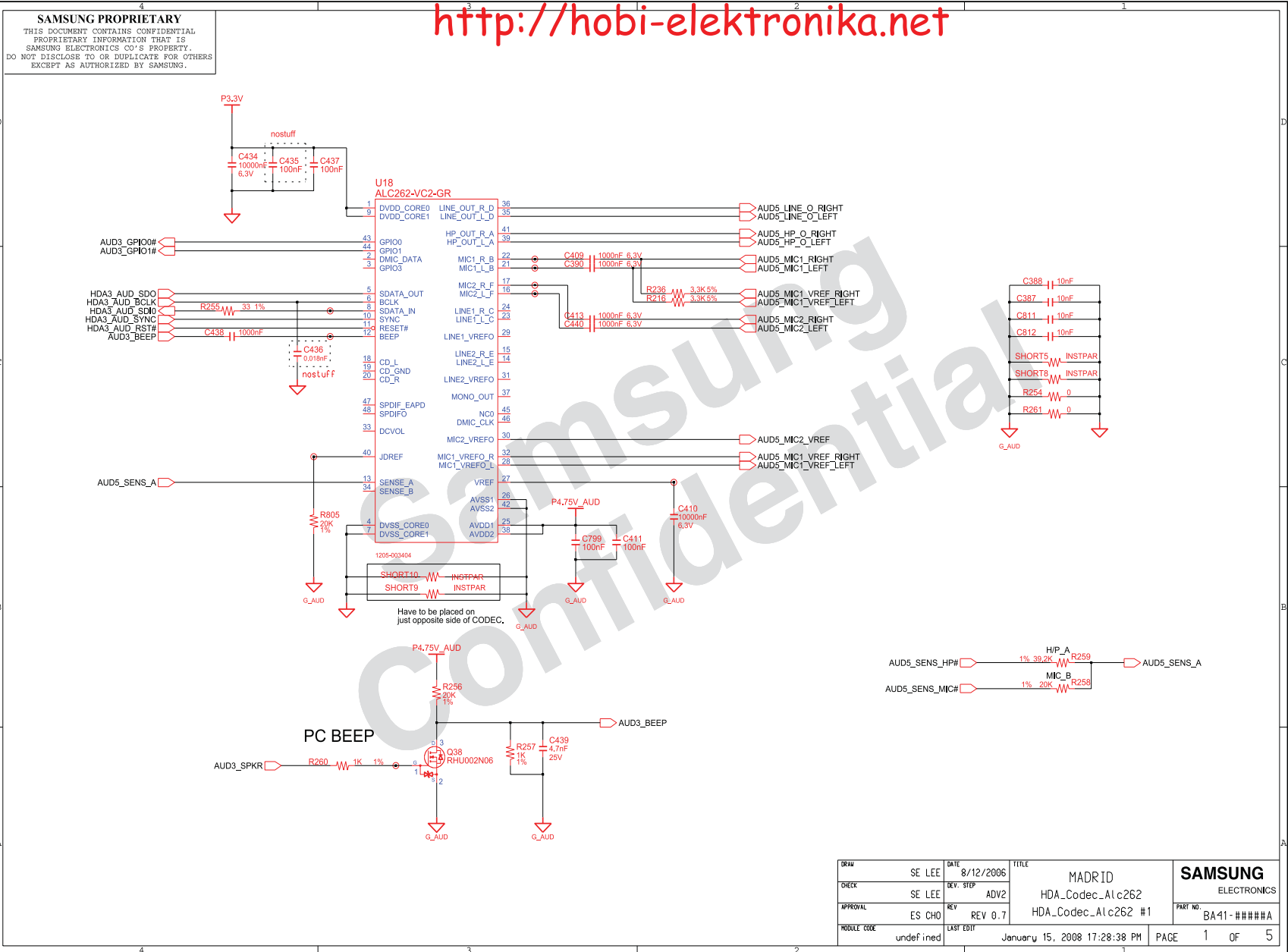
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CHECK	SE LEE	REV. STEP	ADV2	Graphics_Memory		
APPROVAL	ES CHO	REV	REV 0.7	Graphics_Memory_Nvidia #3	PART NO.	BA41-#####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	2	OF 2

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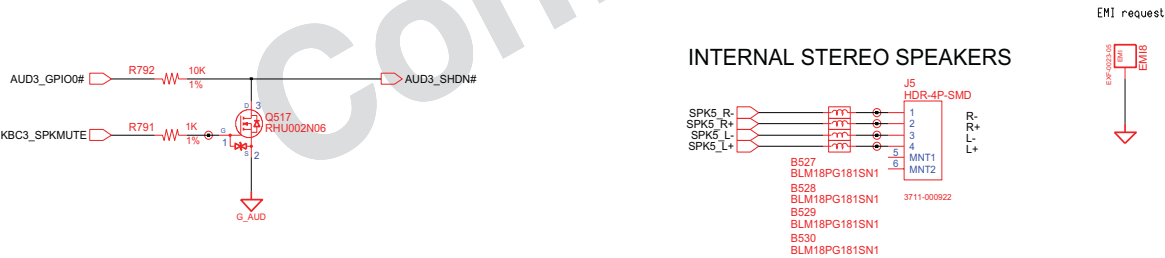
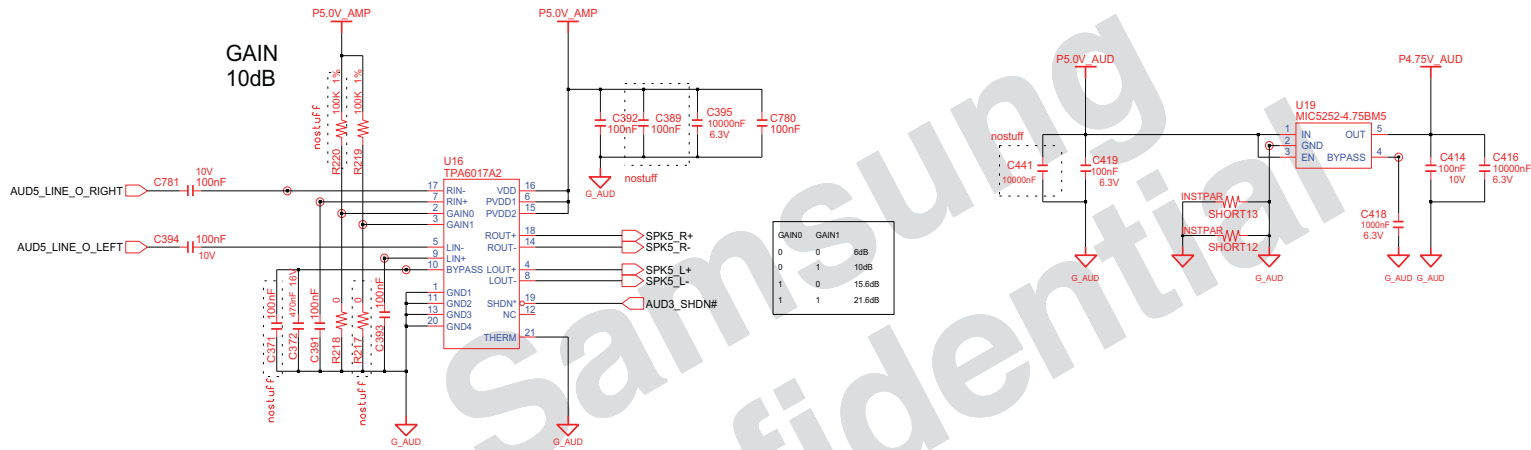


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DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
DECK	SE LEE	DEV. STEP	ADV2		HDA_Codec_A1 c262	
APPROVAL	ES CHO	REV	REV 0.7		HDA_Codec_A1 c262 #2	PART NO. BA41-####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	2	OF 5

8. 블록도 및 회로도

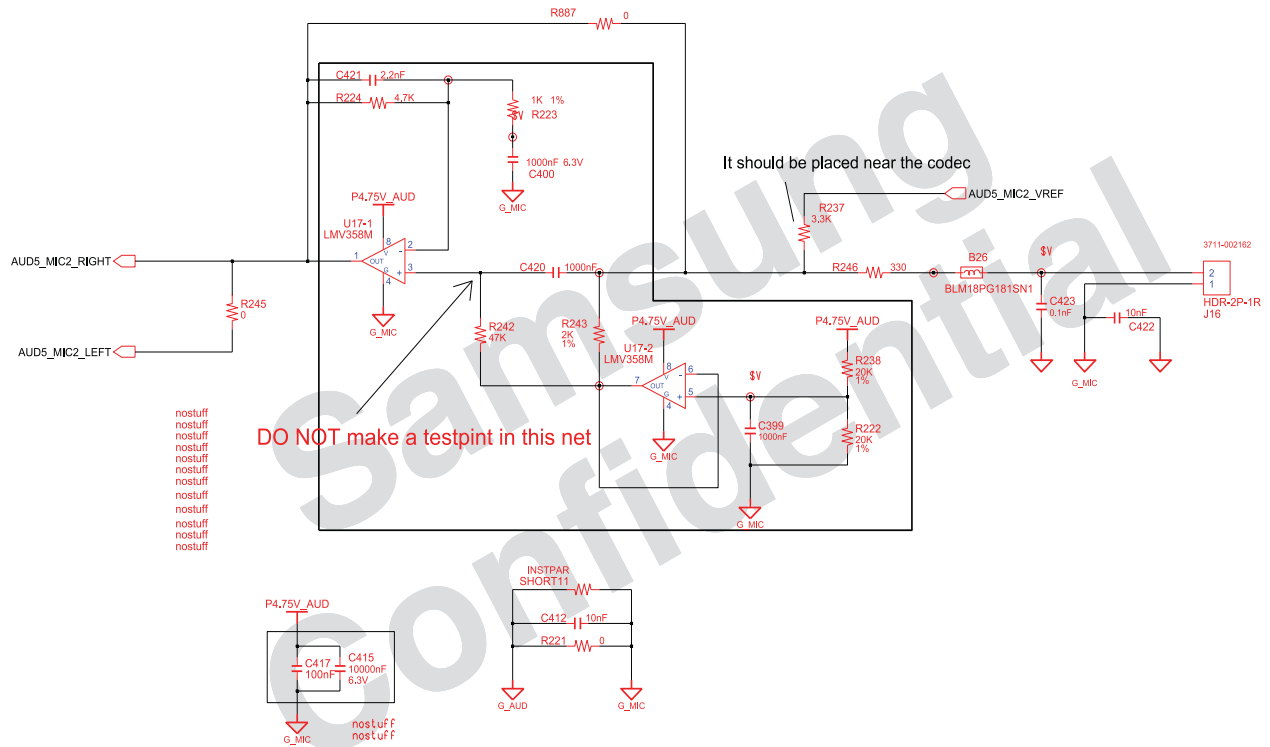
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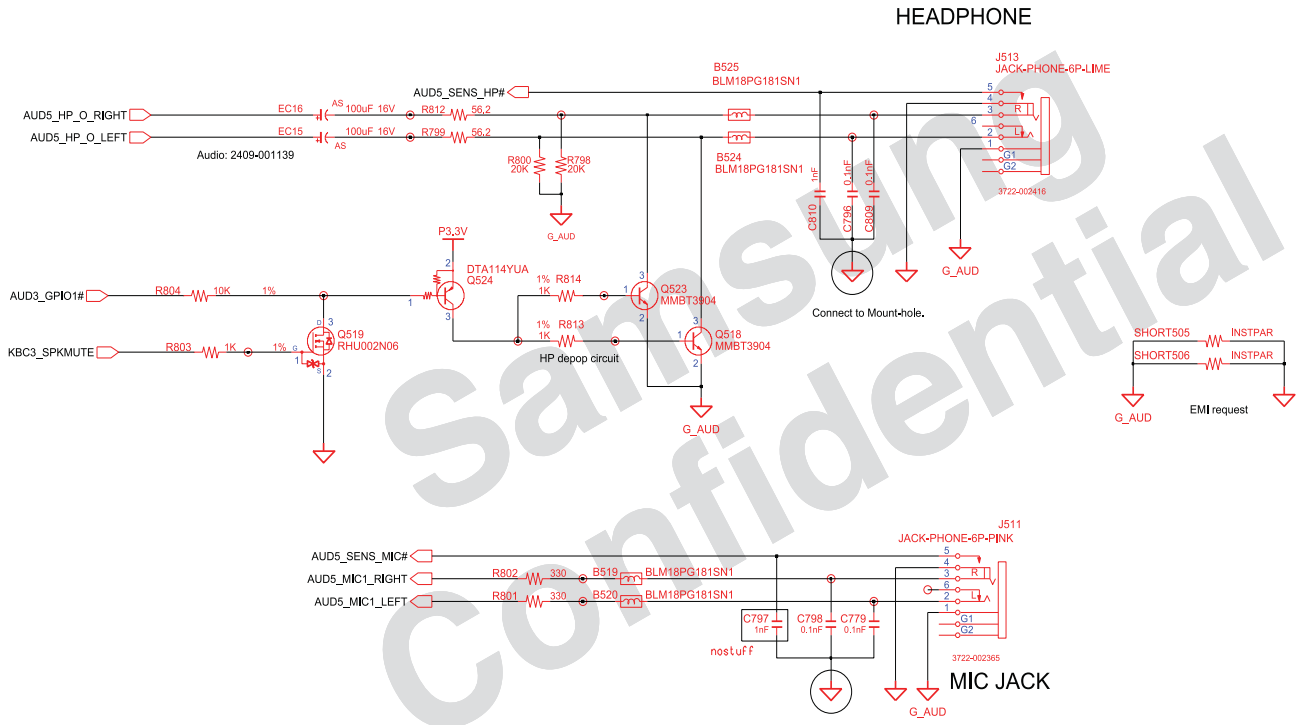
8-44

DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
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APPROVAL	ES CHO	REV	REV 0.7	HDA_Codec_At262 #3		
MODULE CODE	undefined	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	3 OF 5	

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The traces led to Audio Jacks have the width over 10mil

8-45

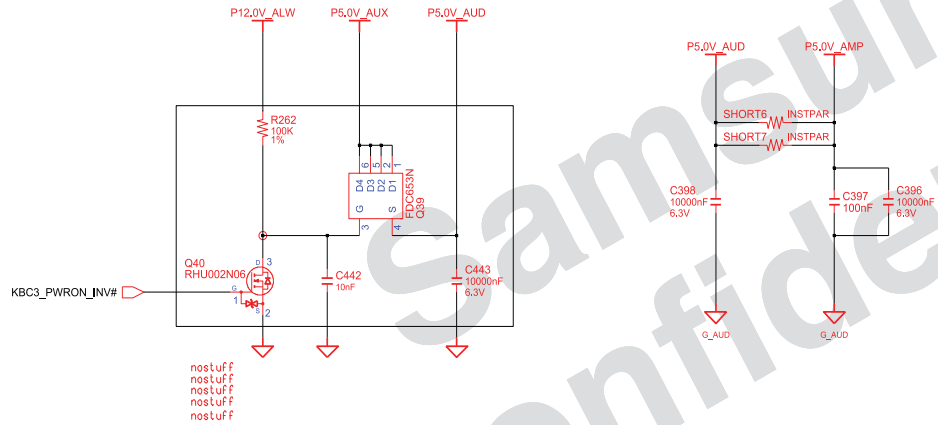
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CHECK	SE LEE	REV. STEP	ADV2	HDA_Codec_At c262		
APPROVAL	ES CHO	REV	REV 0.7	HDA_Codec_At c262 #4		
MODULE CODE	LAST EDIT		January 15, 2008 17:28:38 PM		PAGE 4 OF 5	

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AUDIO POWER

P5.0V_AUD is made from P5.0V through resistors directly.
 Please refer to power page.



nostuff
 nostuff
 nostuff
 nostuff
 nostuff

DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	HDA_Codec_At c262		
APPROVAL	ES CHO	REV	REV 0.7	HDA_Codec_At c262 #5		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	5 OF 5	

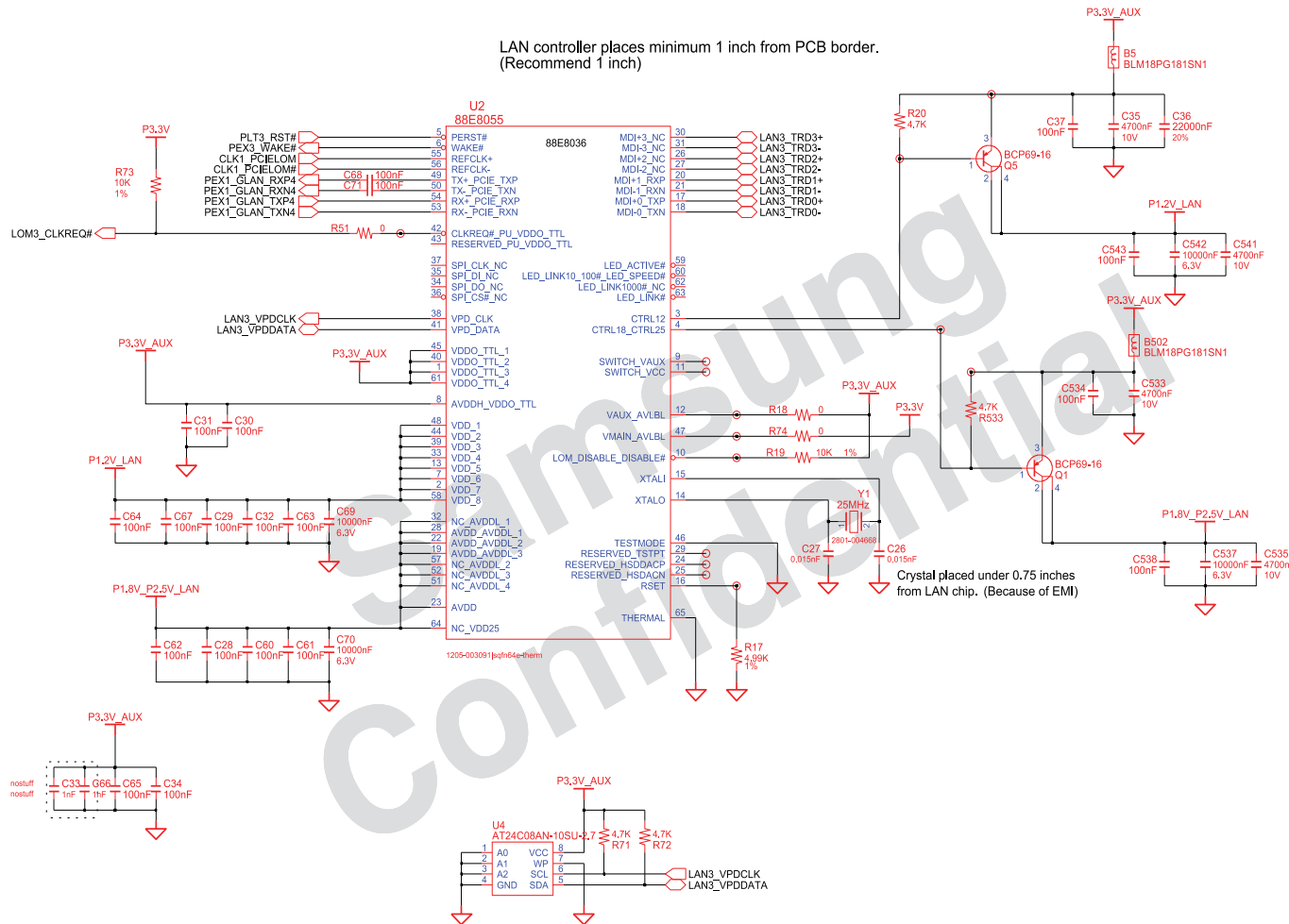
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LAN controller places minimum 1 inch from PCB border.
 (Recommend 1 inch)



Crystal placed under 0.75 inches
 from LAN chip. (Because of EMI)

DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	DEV. STEP	ADV2	LAN_Marvell_8055		
APPROVAL	ES CHO	REV	REV 0.7	LAN_Marvell_8055		
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 2	PART NO. BA41-#####

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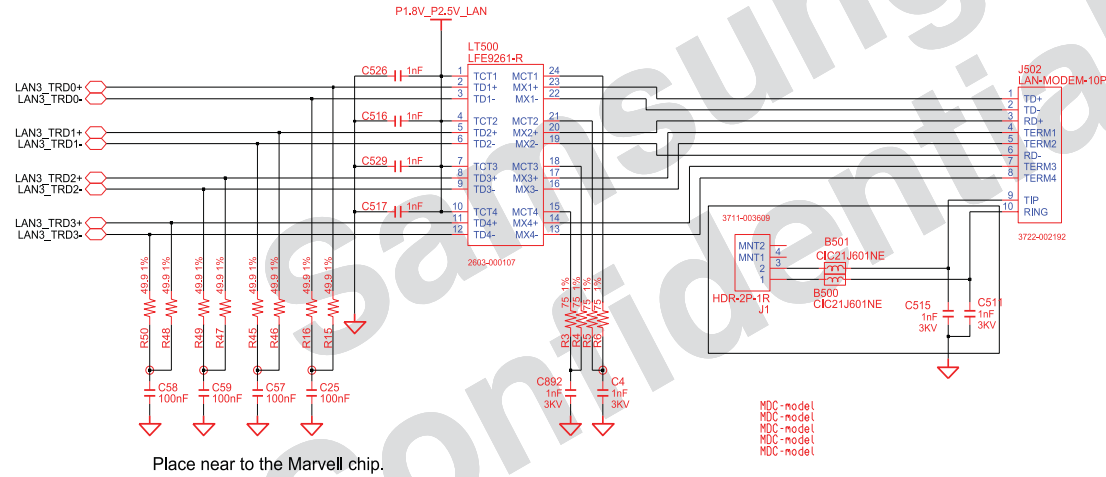
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The distance between LAN controller
 and transformer is designed to extend less than two inches.



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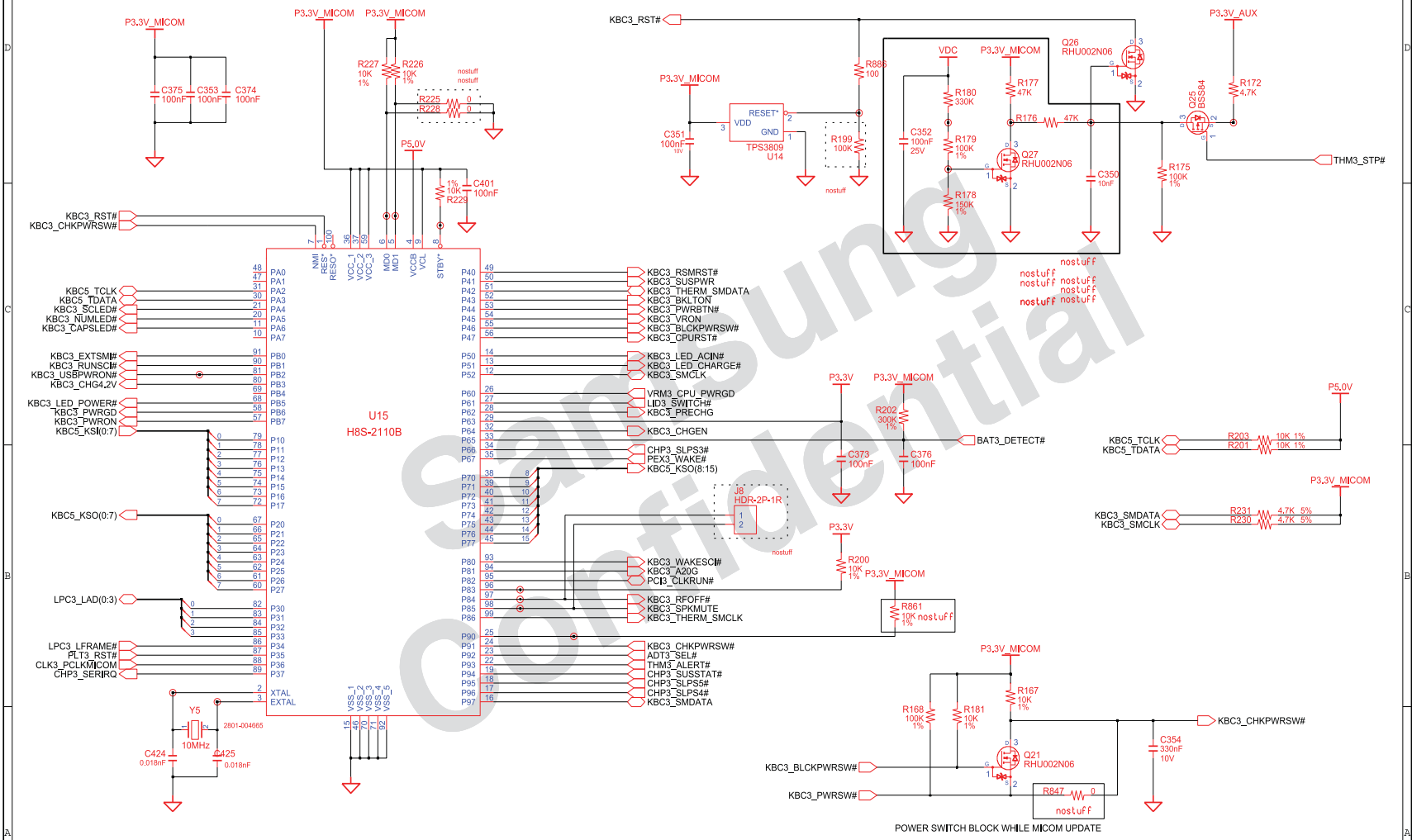
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CHECK	SE LEE	REV. STEP	ADV2	LAN_Marvell_8055	PART NO.	
APPROVAL	ES CHO	REV	REV 0.7	LAN_Marvell_8055	BA41-#####A	
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	2 OF 2	

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MICOM RESET



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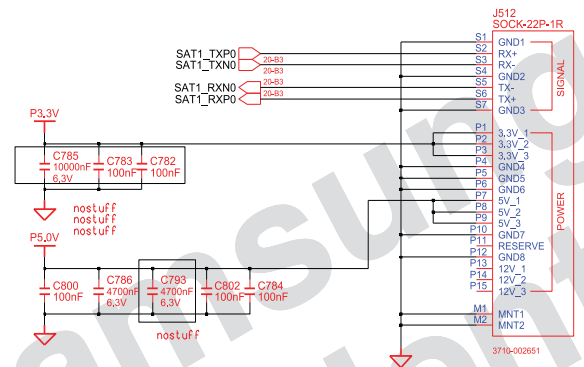
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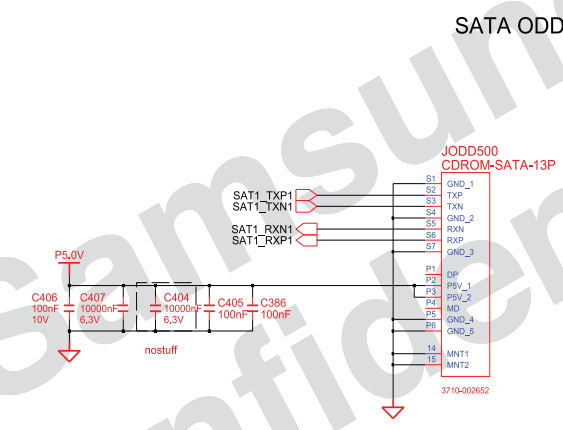


Main to HDD

DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	HDD_IF_Conn	HDD_IF_Conn	
APPROVAL	ES CHO	REV	REV 0.7	HDD_IF_Conn		PART NO. BA41-#####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

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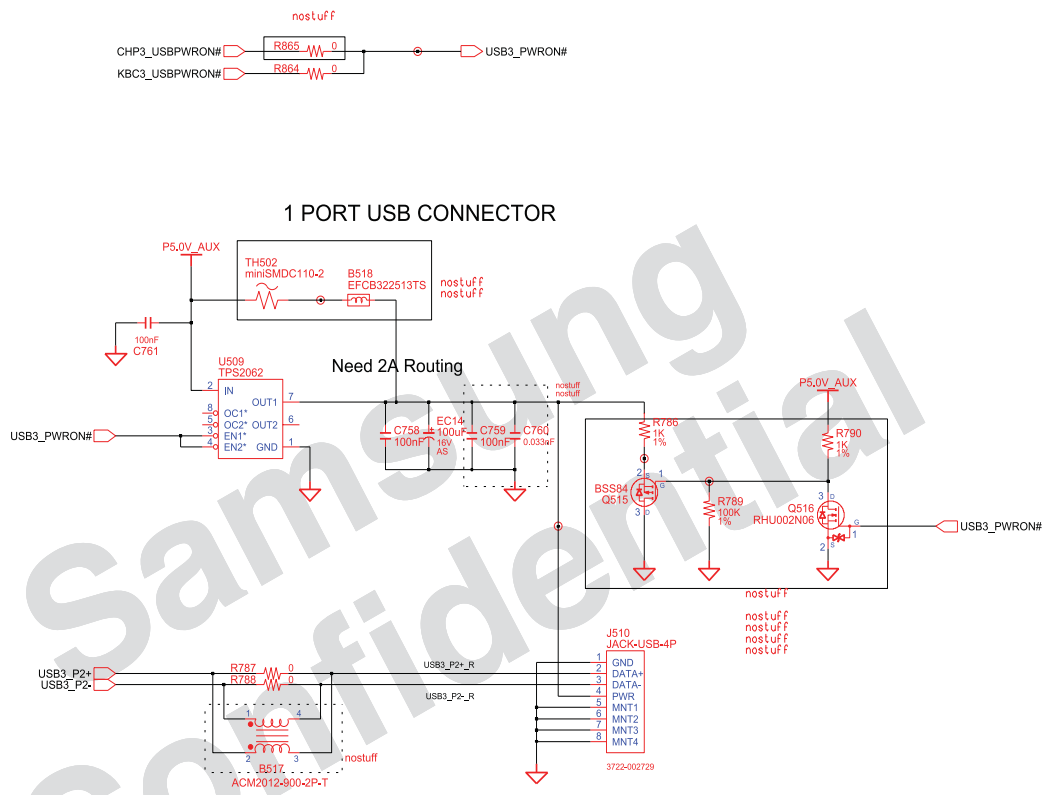
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CHECK	SE LEE	REV. STEP	ADV2	ODD_IF_Conn	ODD_IF_Conn	
APPROVAL	ES CHO	REV	REV 0.7	ODD_IF_Conn	PART NO.	BA41-#####A
MODULE CODE	LAST EDIT			January 15, 2008 17:28:38 PM	PAGE	1 OF 1

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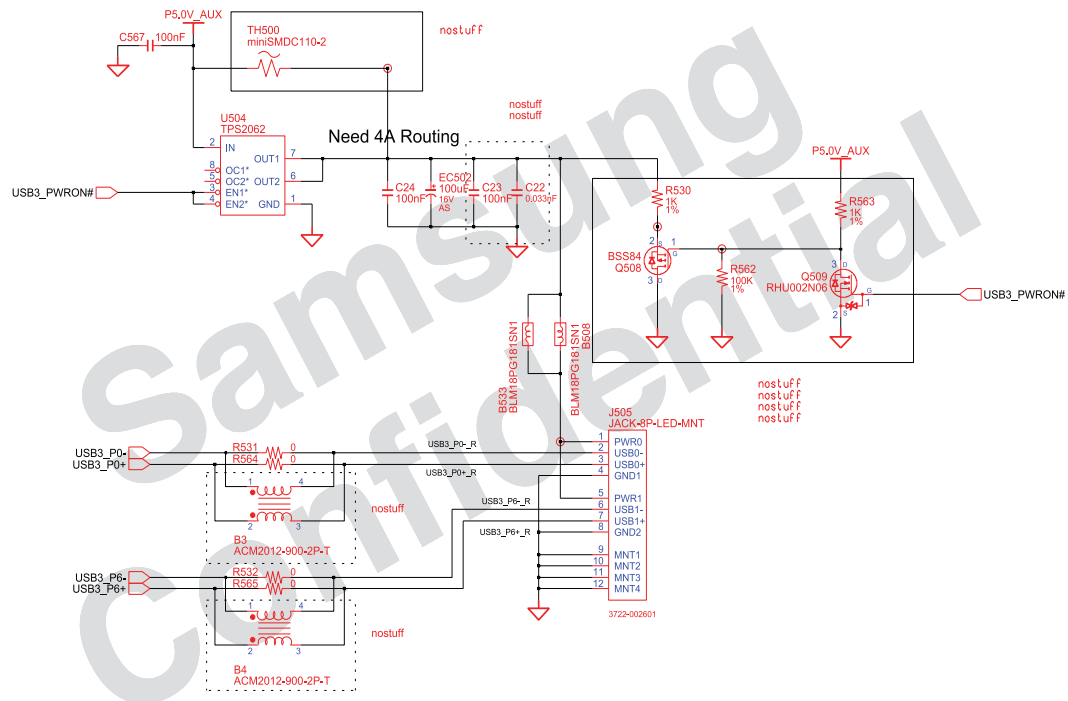


DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID USB_1Port	SAMSUNG ELECTRONICS
CHECK	SE LEE	DEV. STEP	ADV2		USB_1Port	
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

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2 PORT USB CONNECTOR

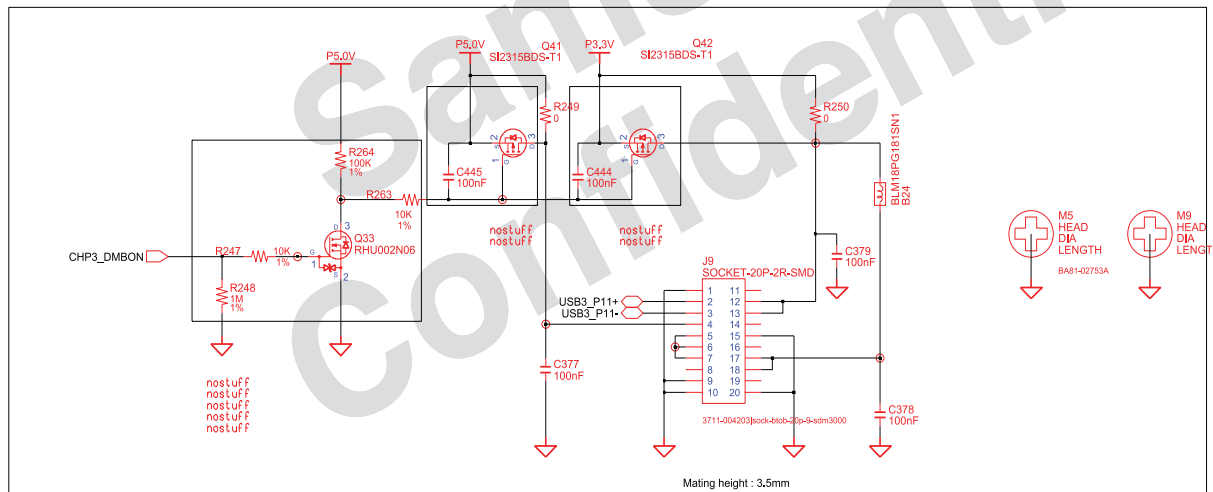
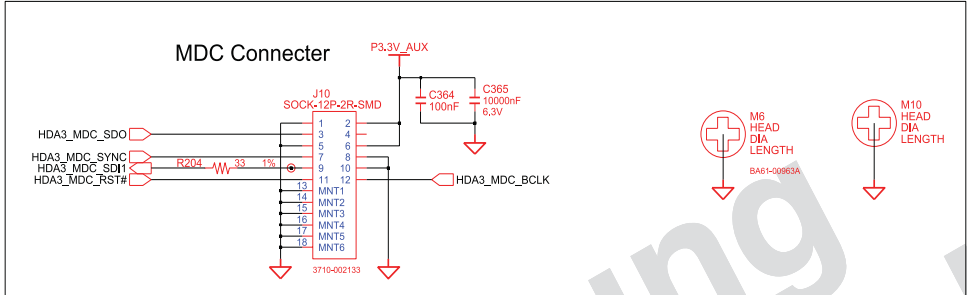


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CHECK	SE LEE	DEV. STEP	ADV2			
APPROVAL	ES CHO	REV	REV 0.7			
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

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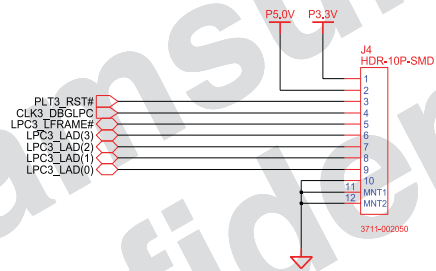
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DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	DEV. STEP	ADV2	HDA_Modem	HDA_Modem	
APPROVAL	ES CHO	REV	REV 0.7	HDA_Modem	PART NO.	BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1	OF 1

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80H DECODER CONNECTOR



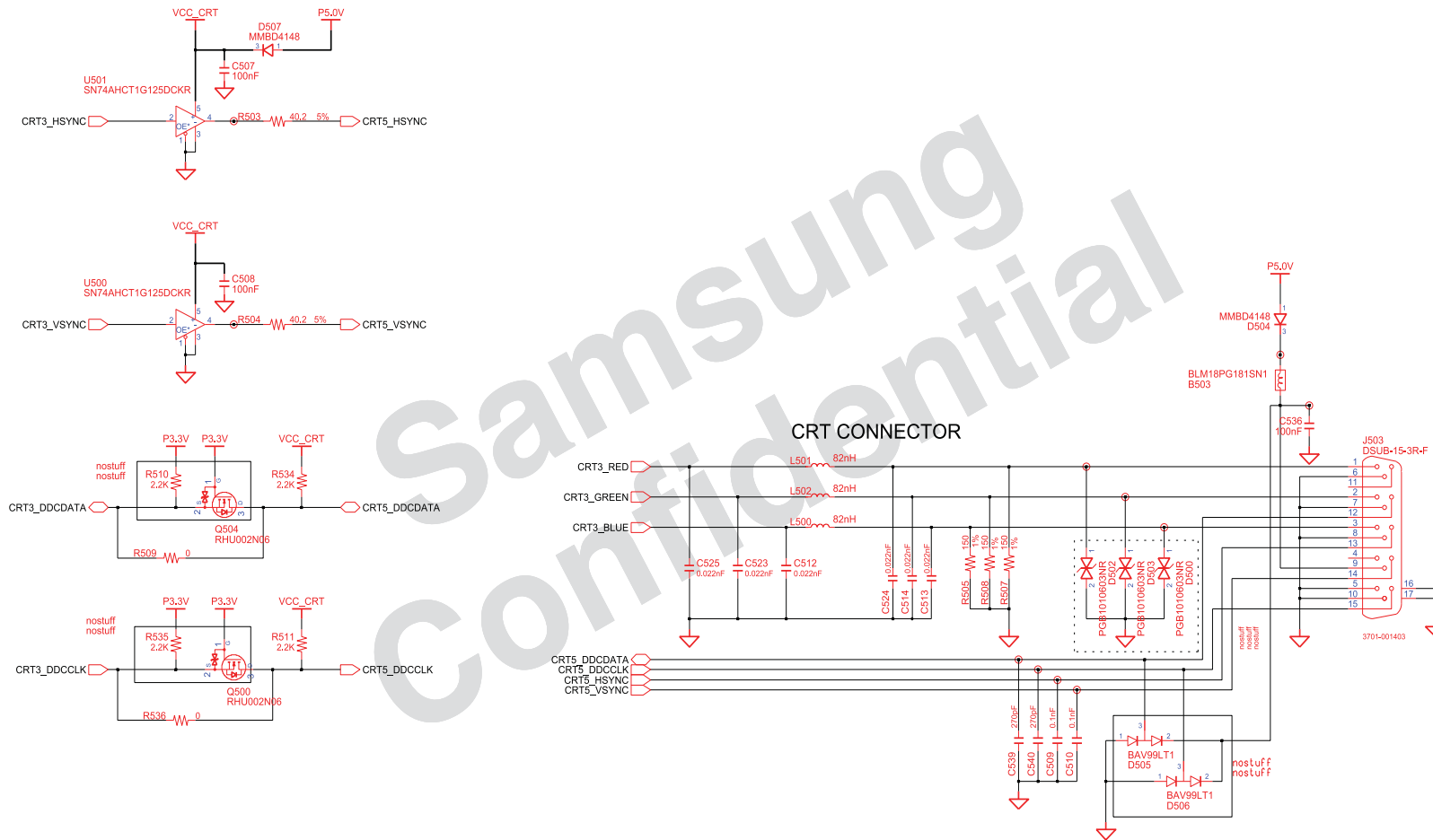
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APPROVAL	ES CHO	REV	REV 0.7	Other_Debug_80	PART NO. BA41-#####A	
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

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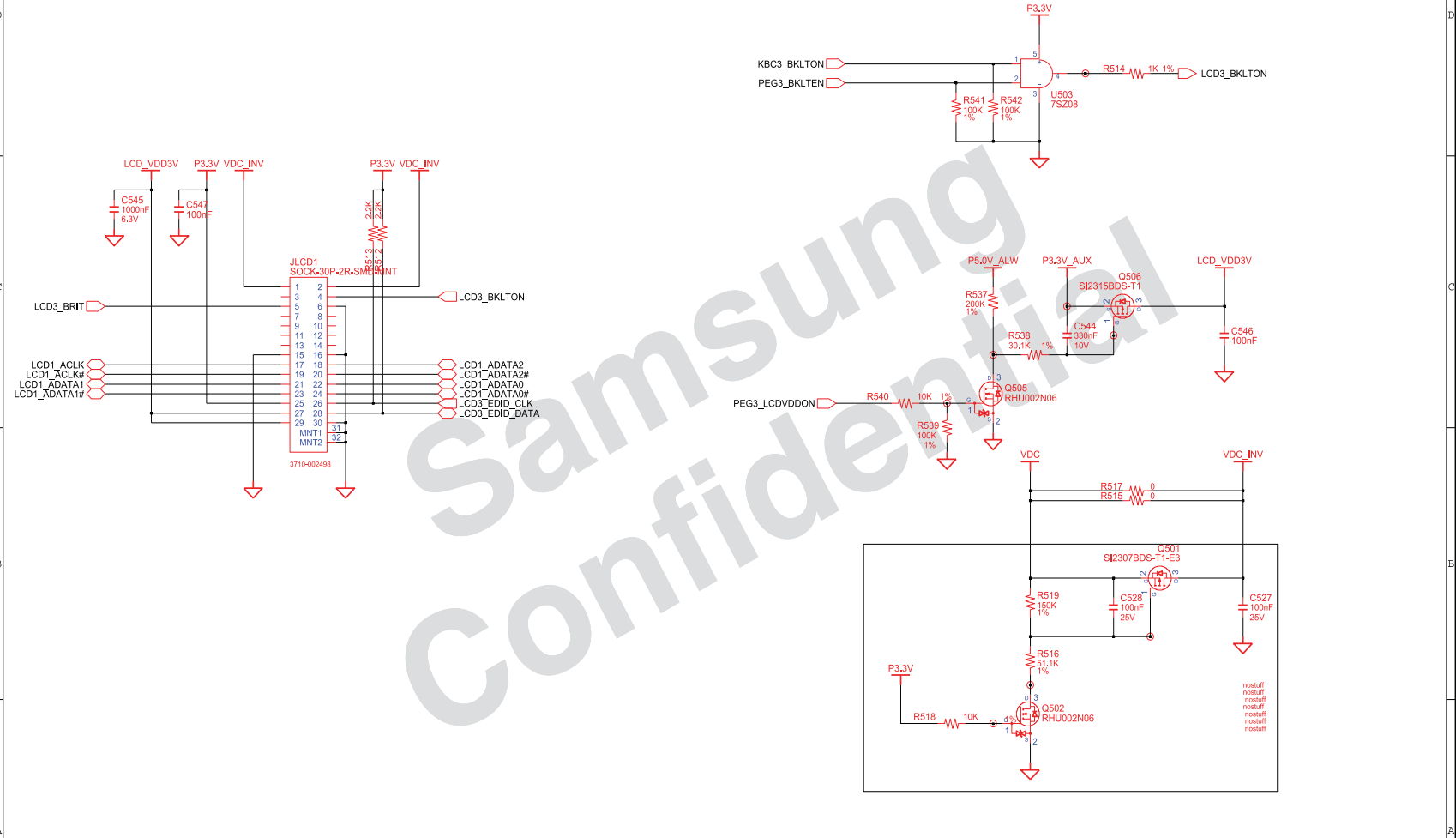


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APPROVAL	ES CHO	REV	REV 0.7	Graphics_IF_CRT	BA41-#####	
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 3	

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DRAW	SE LEE	DATE	8/17/2007	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2		UNDEFINED	
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MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM			PAGE 12 of 12

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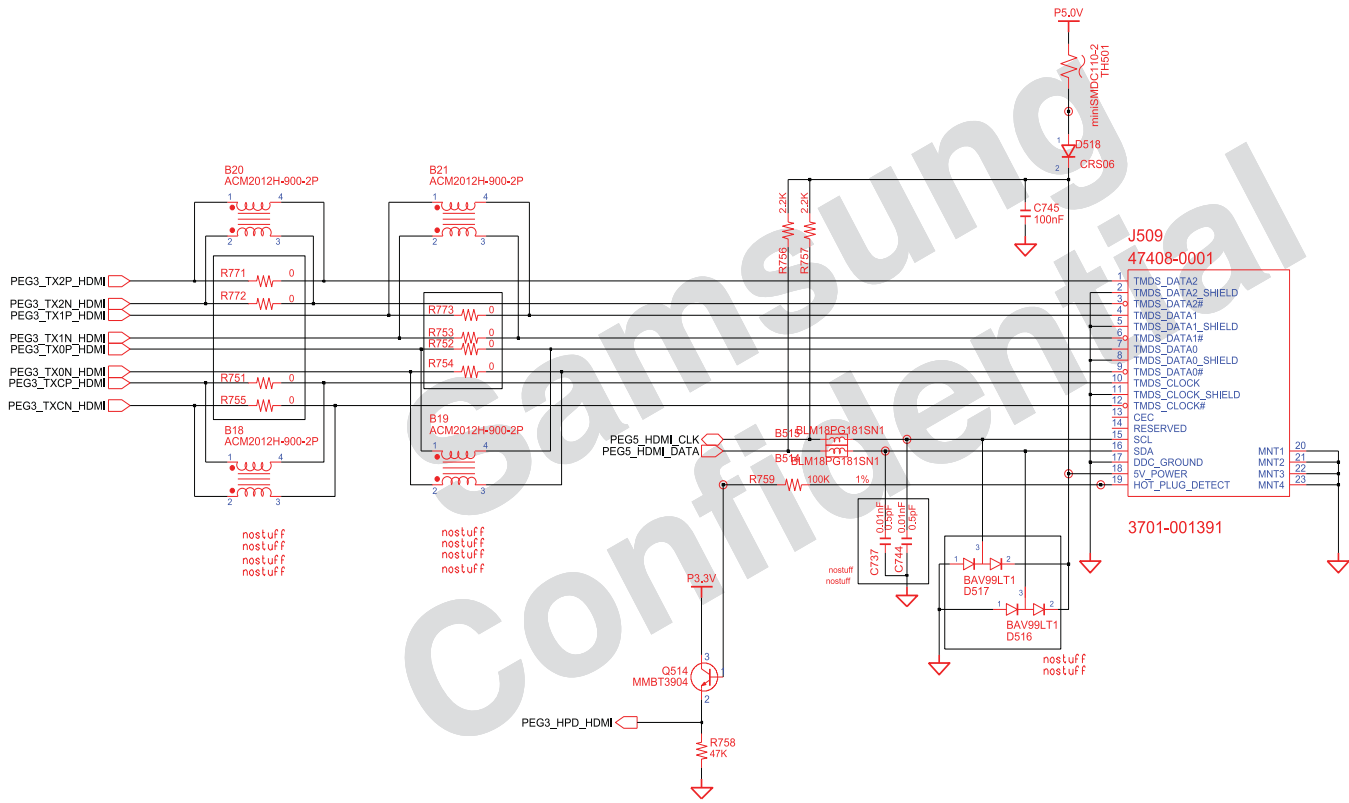
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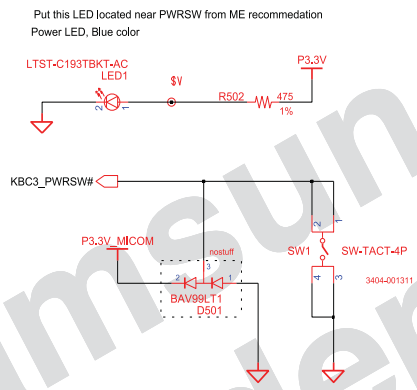
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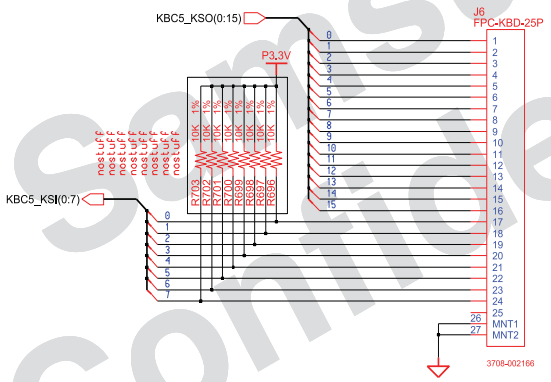
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APPROVAL	ES CHO	REV	REV 0.7	MIO_Switch		PART NO. BA41-#####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1	OF 1

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DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	DEV. STEP	ADV2	KBD_IF_Conn	KBD_IF_Conn	
APPROVAL	ES CHO	REV	REV 0.7	KBD_IF_Conn	PART NO.	BA41-#####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1	OF 1

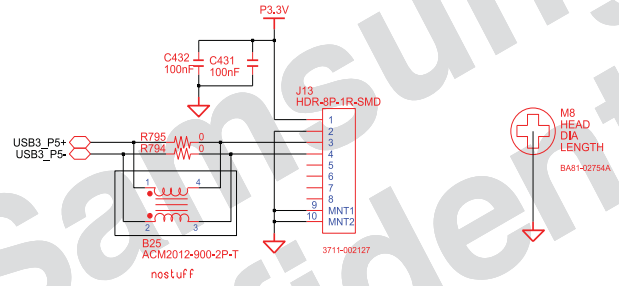
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Bluetooth Interface

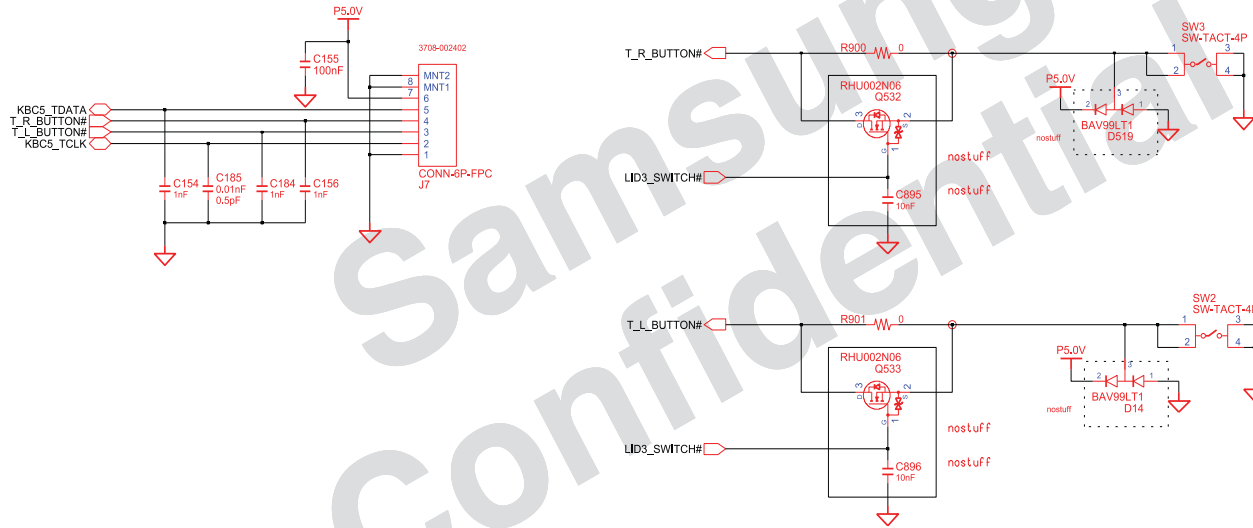


DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	Bluetooth_IF_Conn	Bluetooth_IF_Conn	
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF	1

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TOUCHPAD



DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	Touchpad_IF_Conn	Touchpad_IF_Conn	
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

8. 블록도 및 회로도

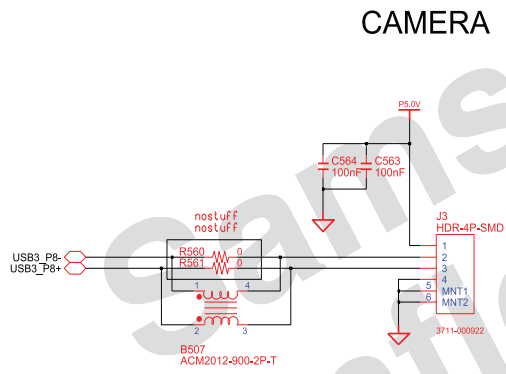
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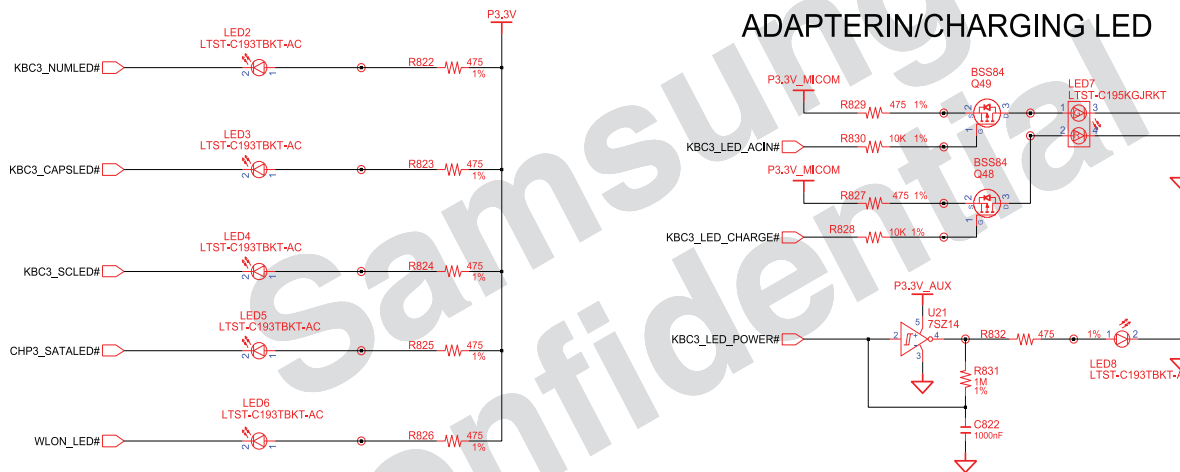
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DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	Camera_IF_Conn	Camera_IF_Conn	
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

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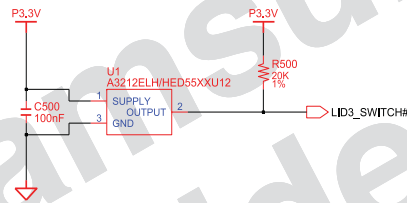
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DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	DEV. STEP	ADV2		LED_Switch	
APPROVAL	ES CHO	REV	REV 0.7		LED_Switch	PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

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LID_SWITCH



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DRAW	SE LEE	DATE	8/12/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	LID_Switch	LID_Switch	
APPROVAL	ES CHO	REV	REV 0.7	LID_Switch	LID_Switch	PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF	1

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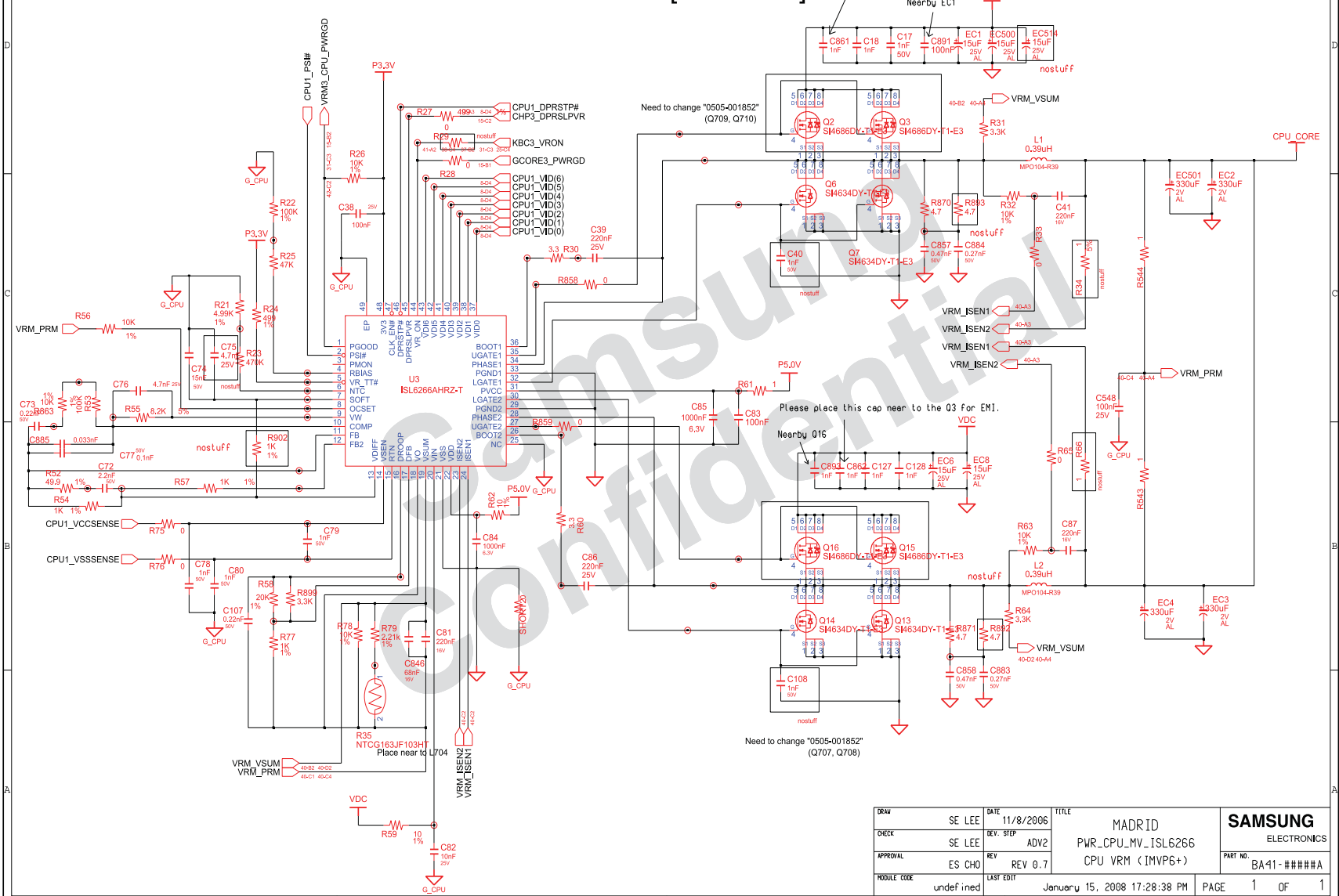
- 이 문서는 삼성전자의 기술 자산으로 승인자만이 사용할 수 있습니다 -
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CPU VRM [INTERSIL]

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DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	PWR_CPU_MV_ISL6266 CPU VRM (IMVP6+)		
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE	undef ined	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

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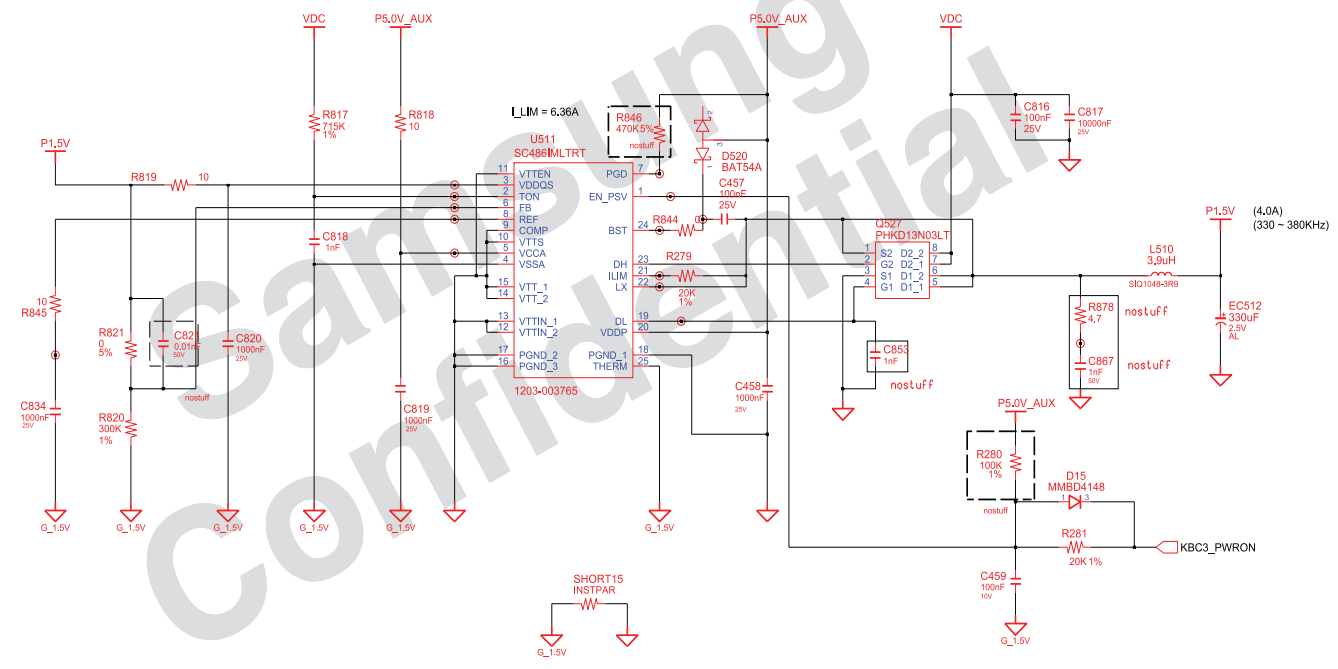
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P1.5V

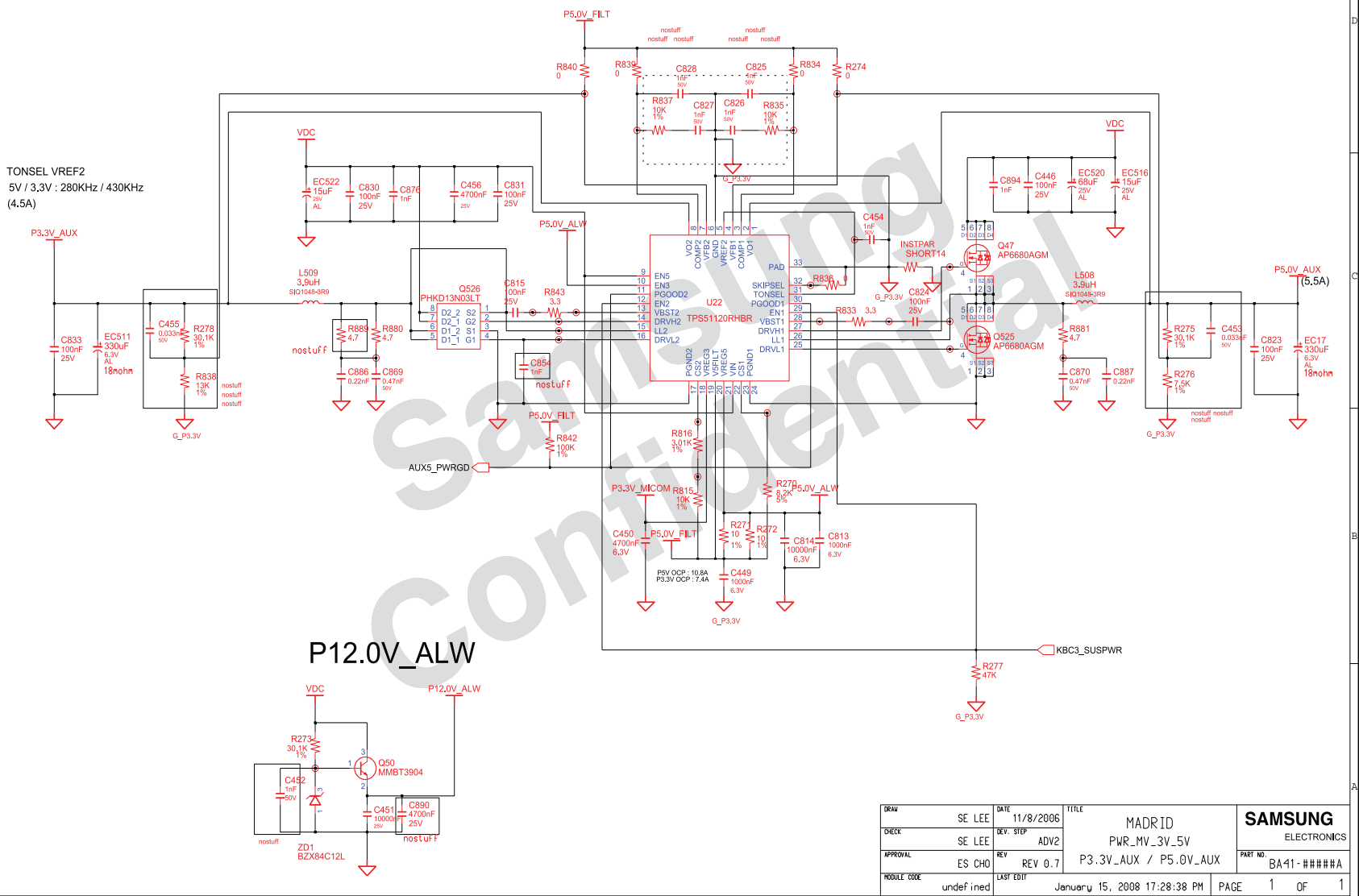


DRAW	SE LEE	DATE	8/14/2007	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	PWR_Gfx_MV_Ext	Ext Gfx Memory(SC486)	
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 2	

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 P3.3V_AUX & P5.0V_AUX

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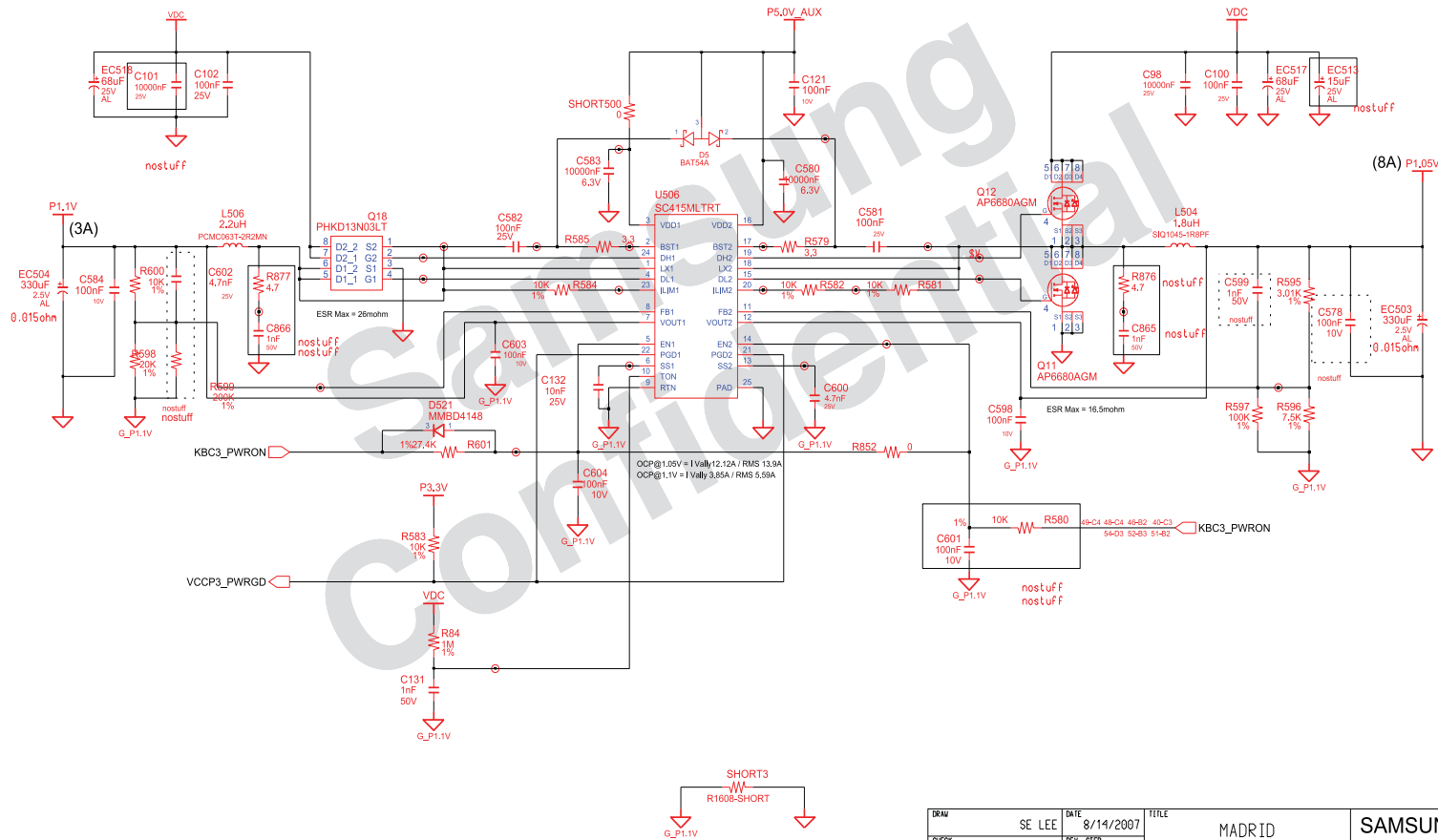


868

DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	PWR_MV_3V_5V	PART NO.	
APPROVAL	ES CHO	REV	REV 0.7	P3.3V_AUX / P5.0V_AUX	BA41-#####	
MODULE CODE	undef ined	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1 OF 1	

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CHIPSET POWER(P1.05V & P1.1V)



DRAW	SE LEE	DATE	8/14/2007	TITLE	MADRID	SAMSUNG
CHECK	SE LEE	REV. STEP	ADV2		PWR_MV_Cant iga	ELECTRONICS
APPROVAL	ES CHO	REV	0		Chipset Power (P1.05V_M,P1.2V)	PART NO. BA41-#####
PROJ. CODE	undef ined	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1	OF 1

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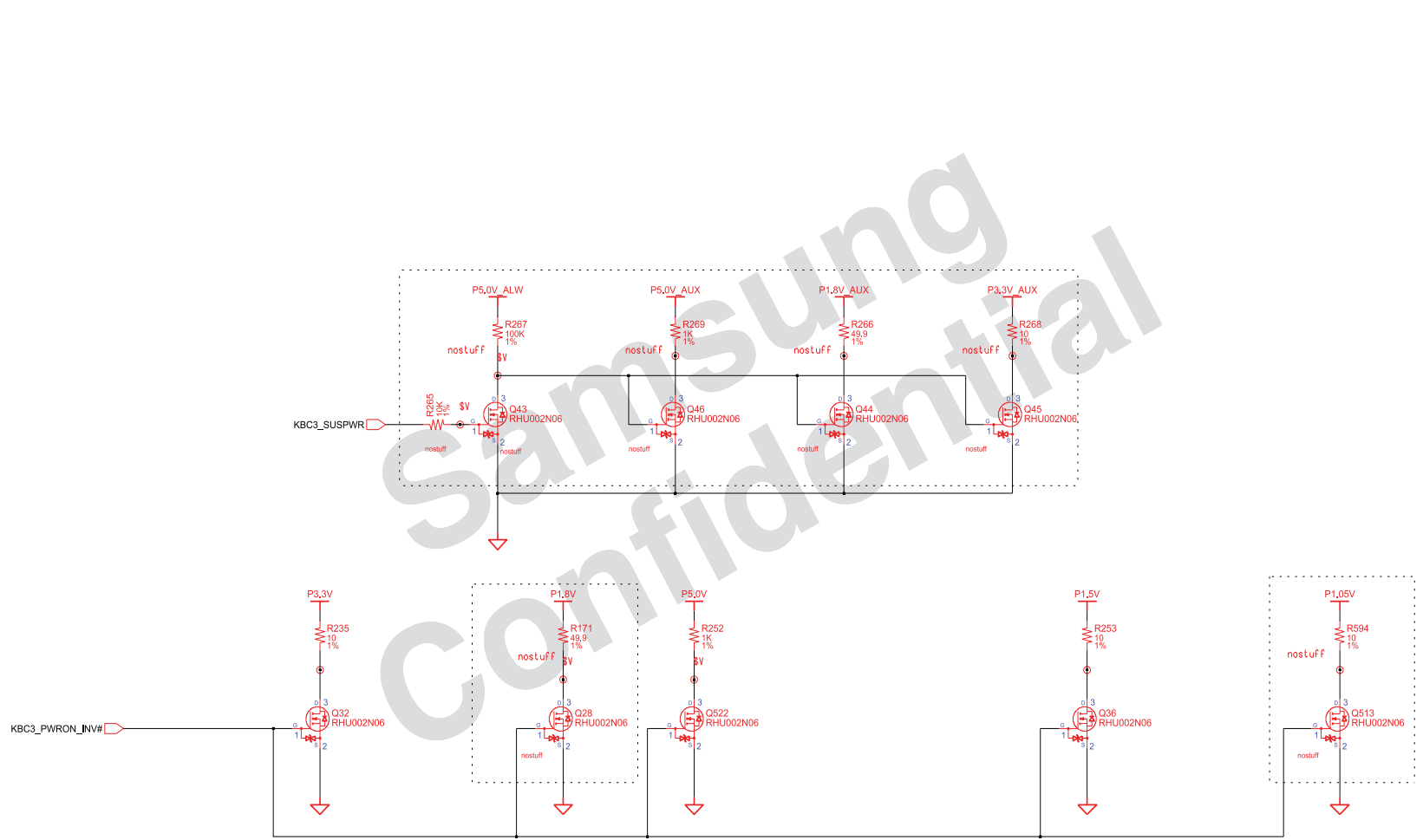
86-8

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POWER DISCHARGER

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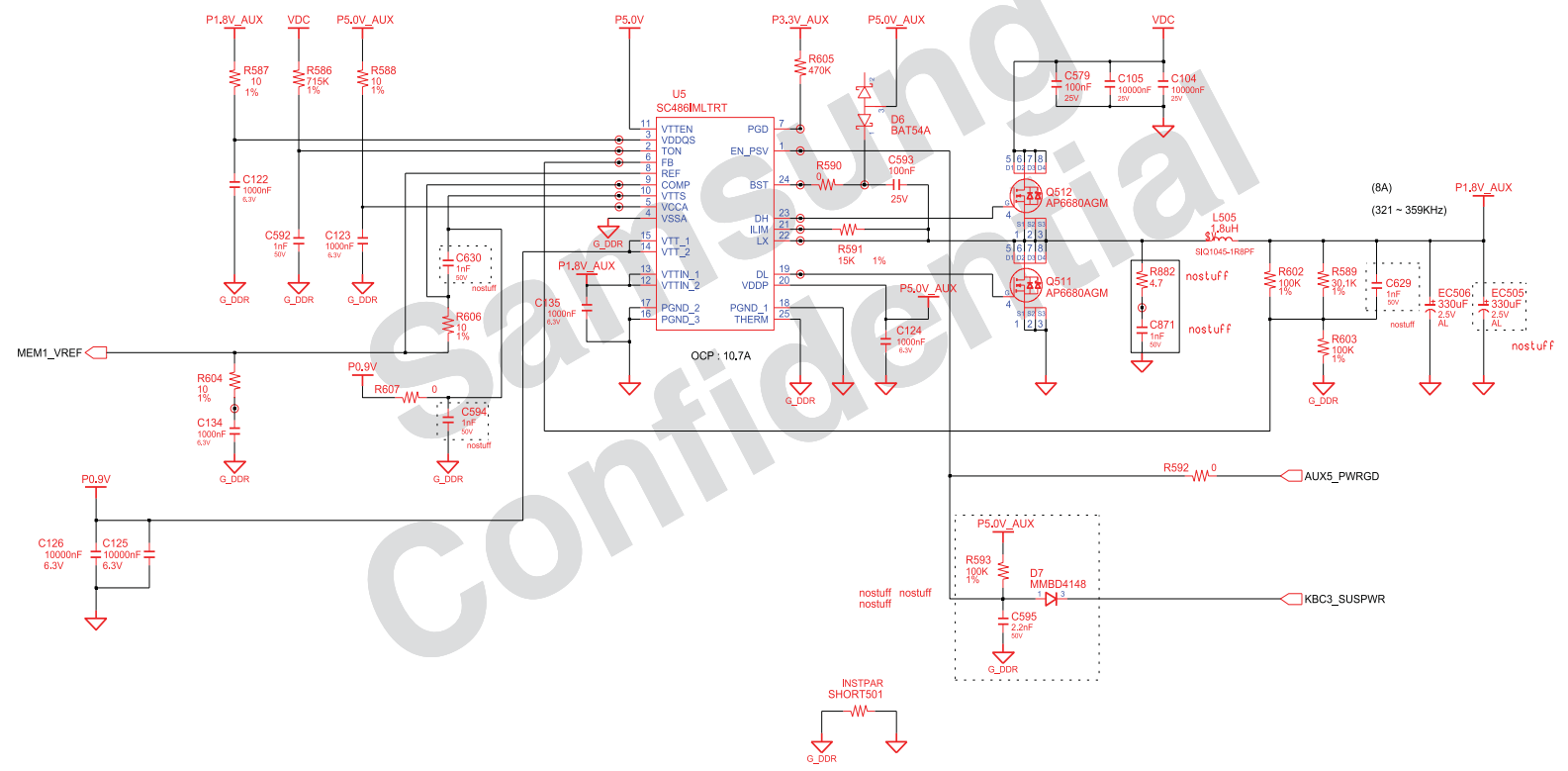
DRAW	SE LEE	DATE	8/14/2007	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	PWR_MV_DisCharger DISCHARGING LOGIC		
APPROVAL	ES CHO	REV	REV 0.7	PART NO. BA41-#####		
MODULE CODE	undef ined	LAST EDIT		January 15, 2008 17:28:38 PM	PAGE	1 OF 1

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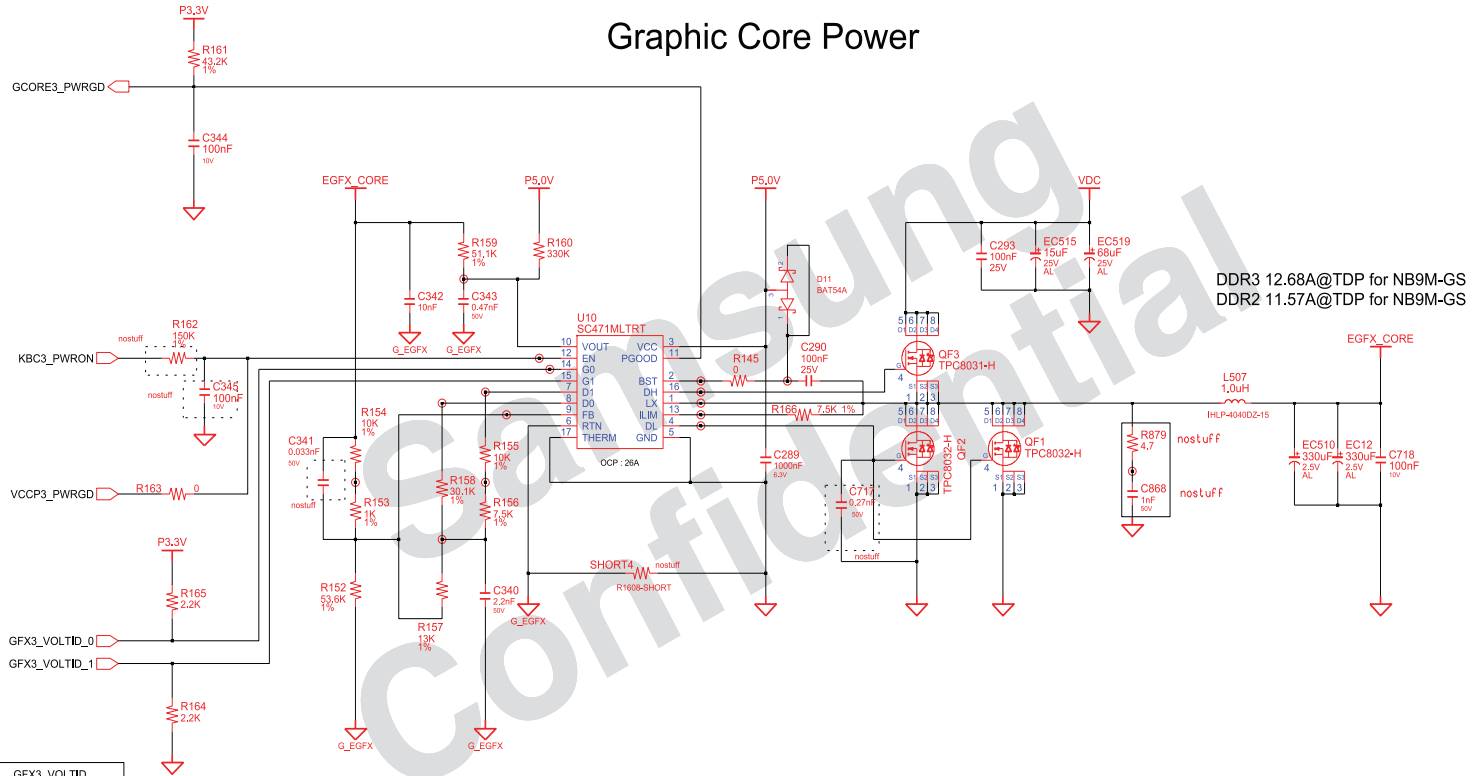
DDR2 POWER



DRAW	SE LEE	DATE	11/8/2006	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2	PWR_MV_Memory		
APPROVAL	ES CHO	REV	REV 0.7	DDR2 POWER (P1.8V_AUX)		PART NO. BA41-#####
MODULE CODE	undef ined	LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	1	OF 1

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Graphic Core Power



DDR3 12.68A@TDP for NB9M-GS
 DDR2 11.57A@TDP for NB9M-GS

GFX3_VOLTID		
G0	C1	
0	0	0.9V (0.9??V)
1	0	1.09V (1.093V)
0	1	1.17V (1.175V)
1	1	RESERVE

DRAW	SE LEE	DATE	8/14/2007	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	DEV. STEP	ADV2	PWR_Gfx_MV_Ext Ext Gfx Core(SC471)		
APPROVAL	ES CHO	REV	REV 0.7			PART NO. BA41-#####
MODULE CODE	LAST EDIT		January 15, 2008 17:28:38 PM		PAGE	2 OF 2

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○ADT3_SEL#
 ○AUD3_GPI00#
 ○AUD3_GPI01#
 ○AUD3_SHDN#
 ○AUD3_BEFP
 ○AUD3_SFR#
 ○AUD5_HP_0_LEFT
 ○AUD5_HP_0_RIGHT
 ○AUD5_LINE_0_LEFT
 ○AUD5_LINE_0_RIGHT
 ○AUD5_MIC1_LEFT
 ○AUD5_MIC1_RIGHT
 ○AUD5_MIC1_VREF_LEFT
 ○AUD5_MIC1_VREF_RIGHT
 ○AUD5_MIC2_RIGHT
 ○AUD5_MIC2_LEFT
 ○AUD5_MIC2_VREF
 ○AUD5_SENS_HP#
 ○AUD5_SENS_MIC#
 ○AUD5_PWRGD
 ○AUD5_SENS_A
 ○BAT3_DETECT#
 ○BAT3_SMCLE#
 ○BAT3_SMDATA#
 ○CHP3_BIOSWP#
 ○CHP3_BIOS_ORF#
 ○CHP3_CL_CLK_0
 ○CHP3_DMBON
 ○CHP3_DPRS1PVR
 ○CHP3_GPI01#
 ○CHP3_GPI02#
 ○CHP3_INTRUDER#
 ○CHP3_ME_RTCSR#
 ○CHP3_PM_SYNC#
 ○CHP3_RTGRST#
 ○CHP3_SAIACLKREQ#
 ○CHP3_SATALED#
 ○CHP3_SERIRQ#
 ○CHP3_SLPSS#
 ○CHP3_SLPSS#
 ○CHP3_SUSSTAT#
 ○CHP3_USBPWRON#
 ○CLK3_DBGLPC
 ○CLK3_FM48
 ○CLK3_PWRGD
 ○CLK3_USB48
 ○CPU1_A20M#
 ○CPU1_DPWR#
 ○CPU1_RS2#
 ○CPU1_TCK
 ○CPU1_TDI
 ○CPU1_TMS
 ○CPU1_TRST#
 ○CPU1_VCSSENSE
 ○CPU1_VSSSENSE

○CRT3_BLUE
 ○CRT3_DDCCLK
 ○CRT3_DDCDATA
 ○CRT3_GREEN
 ○CRT3_HSYNC
 ○CRT3_RED
 ○CRT3_VSYNC
 ○EXP3_CPPE#
 ○EXP3_CPUSE#
 ○EXP3_PFRST#
 ○FAN3_FDBACK#
 ○FANS_VDI
 ○GORE3_PWRGD
 ○GFX3_HCLK
 ○GFX3_HDATA
 ○GFX3_ROMS1
 ○GFX3_STRAP2
 ○GFX3_THERM#
 ○GFX3_VOL_TID_1
 ○HDA3_AUD_BCLK
 ○HDA3_AUD_RST#
 ○HDA3_AUD_SDI0
 ○HDA3_AUD_SDO
 ○HDA3_AUD_SYNC
 ○HDA3_HDMI_DCLK
 ○HDA3_HDMI_RST#
 ○HDA3_HDMI_SDI2
 ○HDA3_HDMI_SDO
 ○HDA3_HDMI_SYNC
 ○HDA3_MDC_BCLK
 ○HDA3_MDC_RST#
 ○HDA3_MDC_SDI1
 ○HDA3_MDC_SDO
 ○HDA3_MDC_SYNC
 ○ITM3_CLKREQ#
 ○KBC3_BCLKPWR#
 ○KBC3_THERM_SMCCLK
 ○KBC3_THERM_SMDATA
 ○KBC3_VRON
 ○KBC3_WAKESC1#
 ○LON3_CLKREQ#
 ○SUB_KBC3_RF0FF#
 ○CPU2_THRMTRIP#
 ○CFX3_CLKREQ#
 ○CPU1_DB12#
 ○CPU1_DB13#
 ○GFX3_STRAP2
 ○GFX3_THERM#
 ○GFX3_VOL_TID_1
 ○HDA3_AUD_BCLK
 ○HDA3_AUD_RST#
 ○HDA3_AUD_SDI0
 ○HDA3_AUD_SDO
 ○HDA3_AUD_SYNC
 ○HDA3_HDMI_DCLK
 ○HDA3_HDMI_RST#
 ○HDA3_HDMI_SDI2
 ○HDA3_HDMI_SDO
 ○HDA3_HDMI_SYNC
 ○HDA3_MDC_BCLK
 ○HDA3_MDC_RST#
 ○HDA3_MDC_SDI1
 ○HDA3_MDC_SDO
 ○HDA3_MDC_SYNC
 ○ITM3_CLKREQ#
 ○KBC3_BCLKPWR#
 ○KBC3_THERM_SMCCLK
 ○KBC3_THERM_SMDATA
 ○KBC3_VRON
 ○KBC3_WAKESC1#
 ○LON3_CLKREQ#
 ○SUB_KBC3_RF0FF#

○LAN3_VPCLK
 ○LAN3_VPDATA
 ○CD3_BKLTON
 ○CD3_BR1
 ○CD3_EDID_CLK
 ○CD3_EDID_DATA
 ○ID3_SW1CH#
 ○PC3_LAD(0)
 ○PC3_LAD(1)
 ○PC3_LAD(2)
 ○PC3_LAD(3)
 ○PC3_LFRAME#
 ○ITP3_DBRESET#
 ○KBC3_A20G
 ○KBC3_BKLTON
 ○KBC3_CAPSLED#
 ○KBC3_CHKPWR#
 ○KBC3_CPURST#
 ○KBC3_EVTSM#
 ○KBC3_LED_ACIN#
 ○KBC3_LED_CHARGE#
 ○KBC3_LED_POWER#
 ○KBC3_NUMLED#
 ○KBC3_PRECHG
 ○KBC3_PWRBTN#
 ○KBC3_PWRGD
 ○KBC3_PWRON
 ○KBC3_PWRON_INV#
 ○KBC3_PWRS#
 ○KBC3_RSMRST#
 ○KBC3_RST#
 ○KBC3_RUNSC1#
 ○KBC3_SMCLE#
 ○KBC3_SMDATA
 ○KBC3_SUSPWR
 ○MCD3_SDCD#
 ○MCD3_SDCCLK
 ○MCD3_SDCMD
 ○MCD3_SDDA10
 ○MCD3_SDDA11
 ○MCD3_SDDA2
 ○MCD3_SDDA3
 ○MCD3_SSWP
 ○MCH1_HXSWJNG
 ○MCH3_CLKREQ#
 ○MCH3_1CHSYNC#
 ○CPU1_FERR#
 ○CPU1_THRMTRIP#
 ○DRAM_RSTA#
 ○KBC5_KS1(0)
 ○KBC5_KS1(1)
 ○KBC5_KS1(2)
 ○KBC5_KS1(3)
 ○KBC5_KS1(4)
 ○KBC5_KS1(5)
 ○KBC5_KS1(6)
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 ○KBC5_KS0(0)
 ○KBC5_KS0(1)
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 ○KBC5_KS0(5)
 ○KBC5_KS0(6)
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 ○KBC5_KS0(8)
 ○KBC5_KS0(9)
 ○KBC5_TCLK
 ○KBC5_TDATA
 ○MCH3_1CHSYNC#
 ○CPU1_FERR#
 ○CPU1_THRMTRIP#
 ○DRAM_RSTA#
 ○MCH3_1CHSYNC#
 ○CPU1_FERR#
 ○CPU1_THRMTRIP#
 ○DRAM_RSTA#
 ○MCH3_1CHSYNC#
 ○CPU1_FERR#
 ○CPU1_THRMTRIP#
 ○DRAM_RSTA#
 ○MCH3_1CHSYNC#
 ○CPU1_FERR#
 ○CPU1_THRMTRIP#
 ○DRAM_RSTA#

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DESIGN	SE LEE	DATE	1/2/2008	TITLE	MADRID	SAMSUNG ELECTRONICS
CHECK	SE LEE	REV. STEP	ADV2		TP	
APPROVAL	ES CHO	REV	REV 0.7		TP	PART NO. BA41-#####A
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM	PAGE	18	OF 19

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DESIGN	SE LEE	DATE	1/2/2008	TITLE	MADRID	SAMSUNG ELECTRONICS PART NO. BA41-#####
CHECK	SE LEE	DEV. STEP	ADV2	TP		
APPROVAL	ES CHO	REV	REV 0.7	TP		
MODULE CODE		LAST EDIT	January 15, 2008 17:28:38 PM		PAGE 19 OF 19	

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8. **블록도 및 회로도**

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