

# QingDao\_ULCPC

CPU : Intel Penryn  
 Chip Set : Intel Cantiga & ICH9M  
 Remarks : Montevina Platform

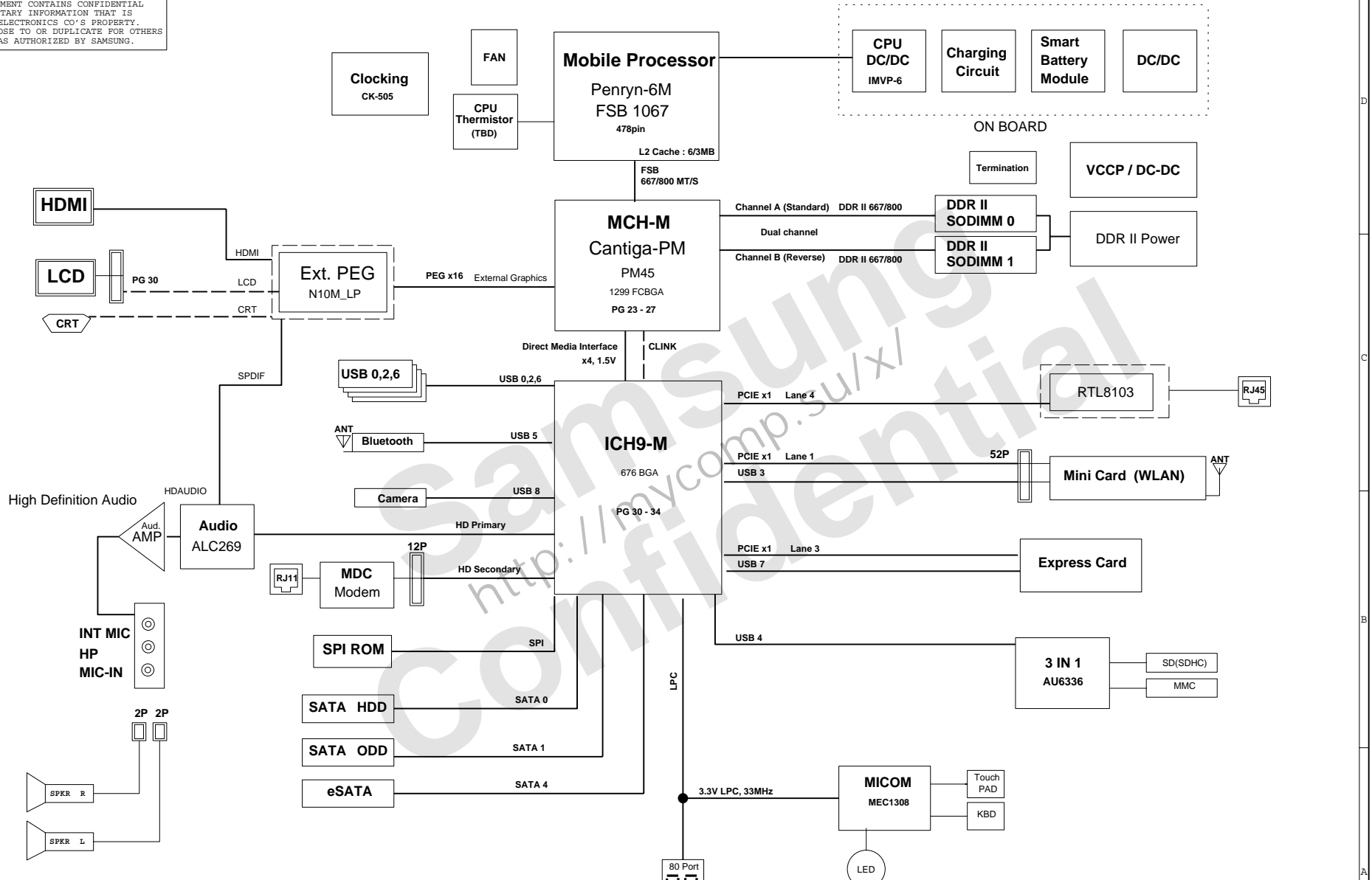
Model Name : QingDao\_ULCPC  
 PBA Name : MAIN  
 PCB Code : BA41-01100A NANYA  
                   BA41-01097A HANNST  
                   BA41-01098A GCE  
 Dev. Step : PV  
 Revision : 1.0  
 T.R. Date : 2009.04.30

## BLOCK DESIGN

Design	CHECK	APPROVAL
XIAOHONG ZHANG	RUJIN ZHENG	BC LEE

■ Owner : SESC Mobile R & D      Signature : X

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DESIGN	Xiaohong Zhang	DATE	09/30/2009	TITLE	QingDao.L MAIN BLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS PART NO. 01097/8/(1100)A
CHECK	Rujin Zheng	DEV. STEP	PV	APPROVAL	BC LEE	
MODULE CODE		REV	1.0	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE 2 OF 15

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# BOARD INFORMATION

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails	
VDC	Primary DC system power supply (7 to 21V)
CPU_CORE	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.05V	VTT for CPU, Cantiga & ICH9-M
P1.1	VTT for N10M_GE1
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

I <sup>2</sup> C / SMB Address			
Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0		
1	Mini PCI Express		
2	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
3	NC	2	NC
4	3 IN 1	3	EXPRESS CARD
5	Bluetooth	4	LOM
6	SYSTEM PORT 2	5	NC
7	EXPRESS CARD	6	NC
8	Camera		
9	NC		
10	NC		

LCD Panel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0(strap0)

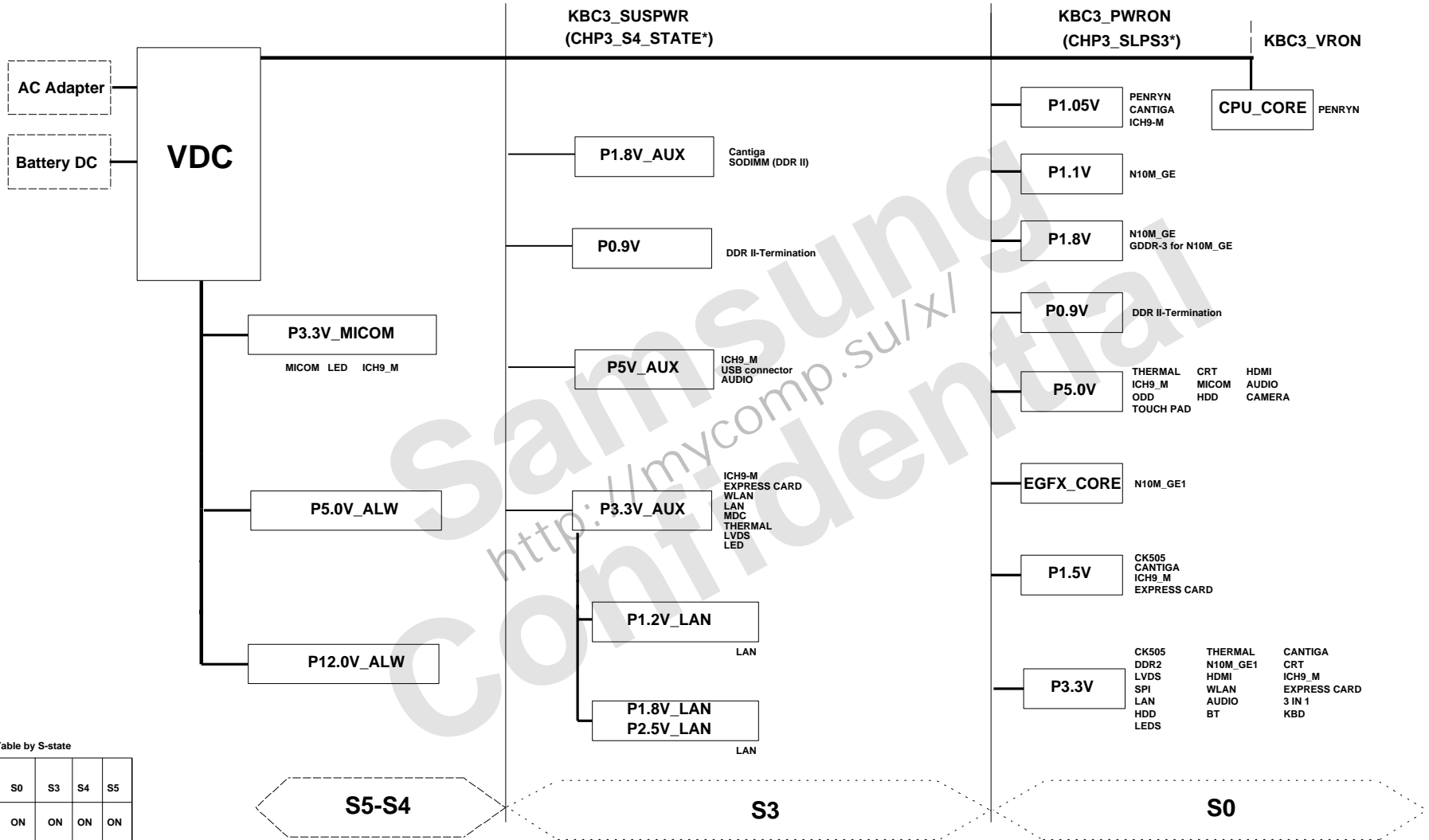
## REVISION HISTORY

See rev notes for more information.

DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	BOARD INFO	BA41-01097/8/(1100)A	
APPROVAL	BC LEE	REV	1.0			PART NO.
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM	PAGE	3 OF 15

# POWER DIAGRAM

Rev 0.1



Power On/Off Table by S-state

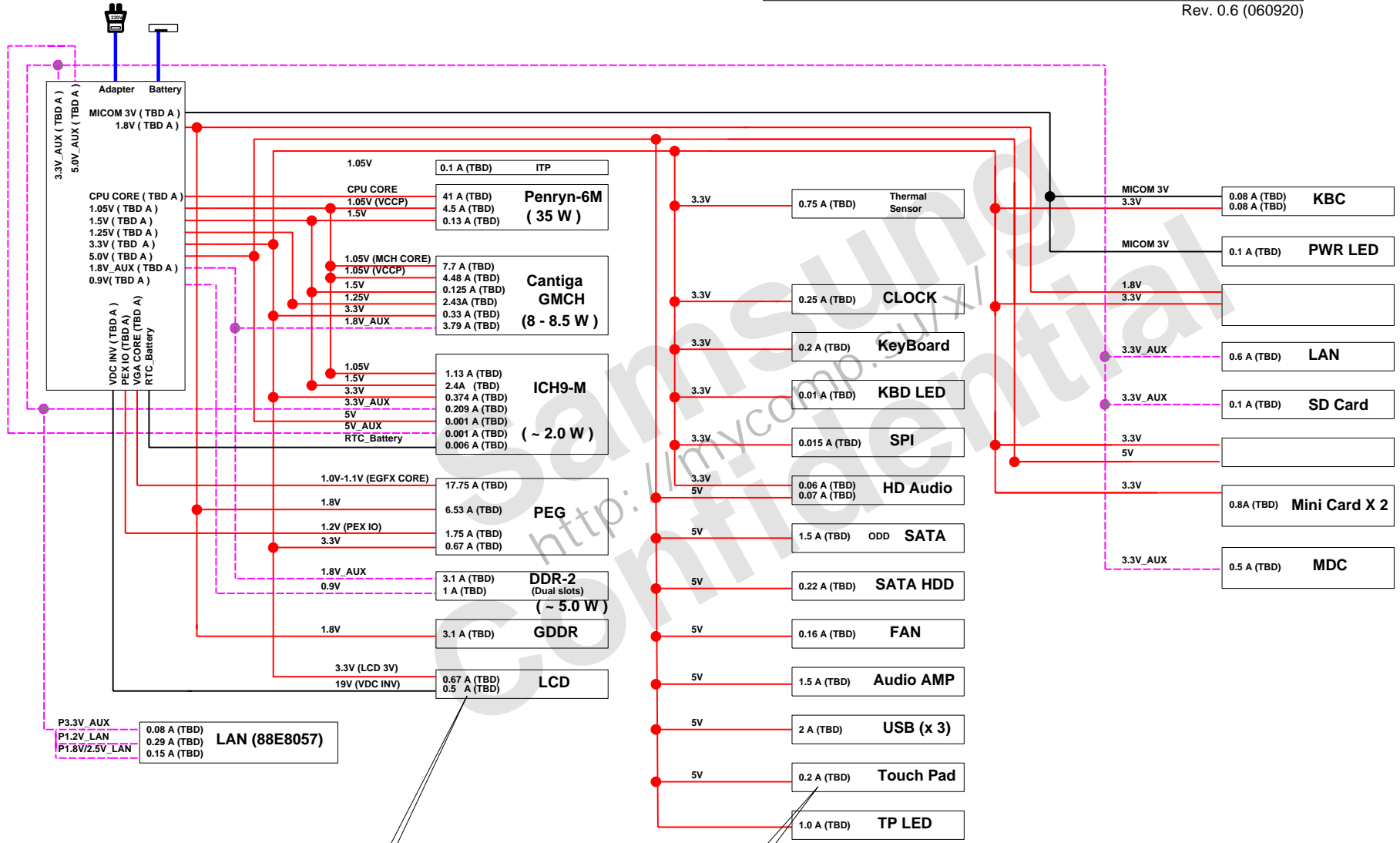
Rail State	S0	S3	S4	S5
+V*(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L MAIN POWER DIAGRAM	<b>SAMSUNG</b> ELECTRONICS PART NO. 01097/8/(1100)A
CHECK	Rujin Zheng	DEV. STEP	PV	APPROVAL	BC LEE	
MODULE CODE		REV	1.0	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE 4 OF 15

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# POWER RAILS ANALYSIS

Rev. 0.6 (060920)



P3.3V\_AUX (0.08 A (TBD))  
 P1.2V\_LAN (0.29 A (TBD))  
 P1.8V/2.5V\_LAN (0.15 A (TBD))  
**LAN (88E8057)**

Value by Datasheet/Application notes (Value by measurement)

DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L MAIN POWER RAILS	<b>SAMSUNG</b> ELECTRONICS PART NO.: BA41-01097/8/(1100)A
CHECK	Rujin Zheng	REV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT				
				April 29, 2009 21:47:17 PM	PAGE 5 OF 15	

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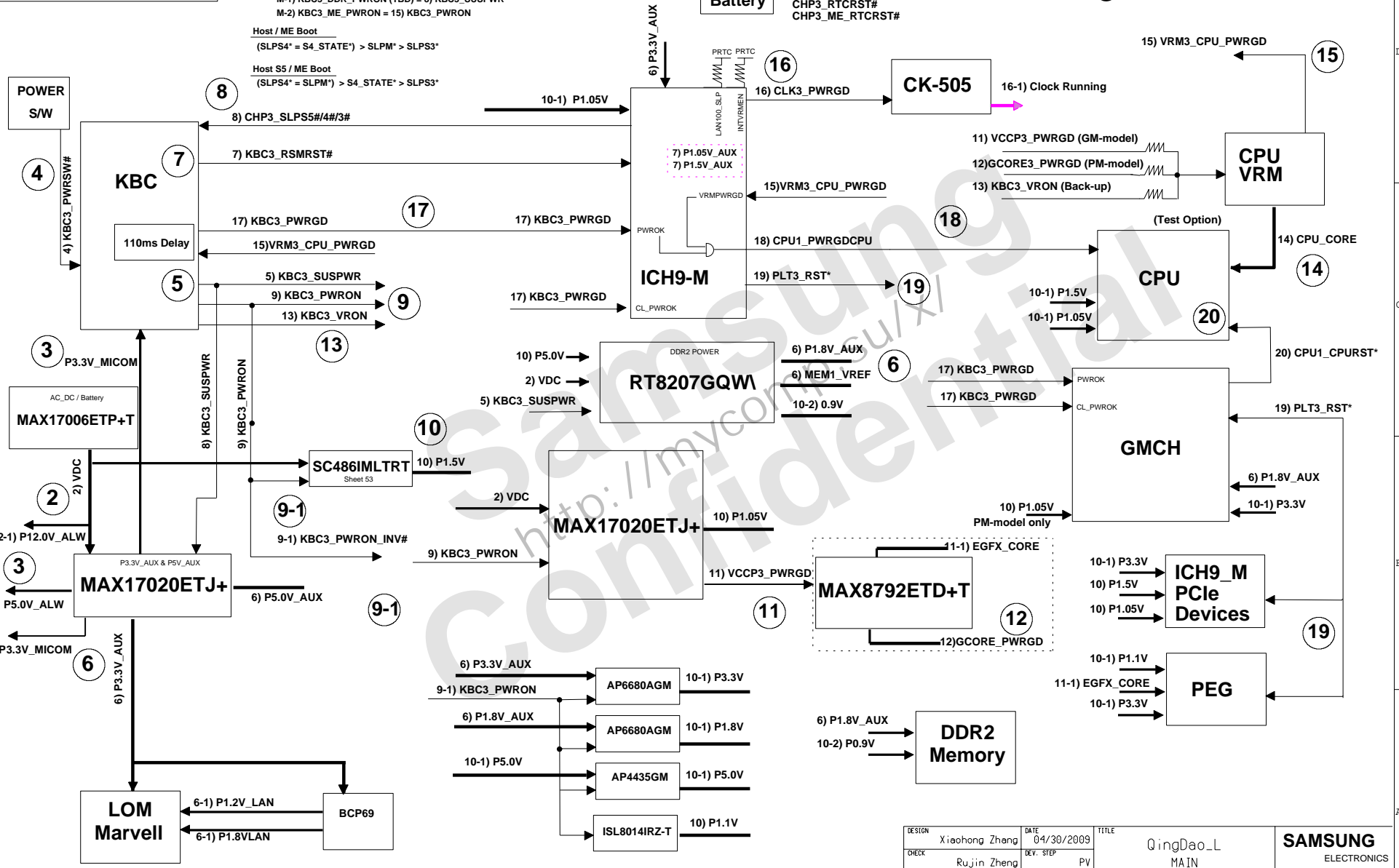
# POWER SEQUENCE

Rev. 0.7

**Host Boot / ME Off**  
 (SLPS4\* = S4\_STATE\*) > (SLPM\* = SLPS3\*)  
 M-1) KBC3\_DDR\_PWRON (TBD) = 8) KBC3\_SUSPWR  
 M-2) KBC3\_ME\_PWRON = 15) KBC3\_PWRON

**Host / ME Boot**  
 (SLPS4\* = S4\_STATE\*) > SLPM\* > SLPS3\*

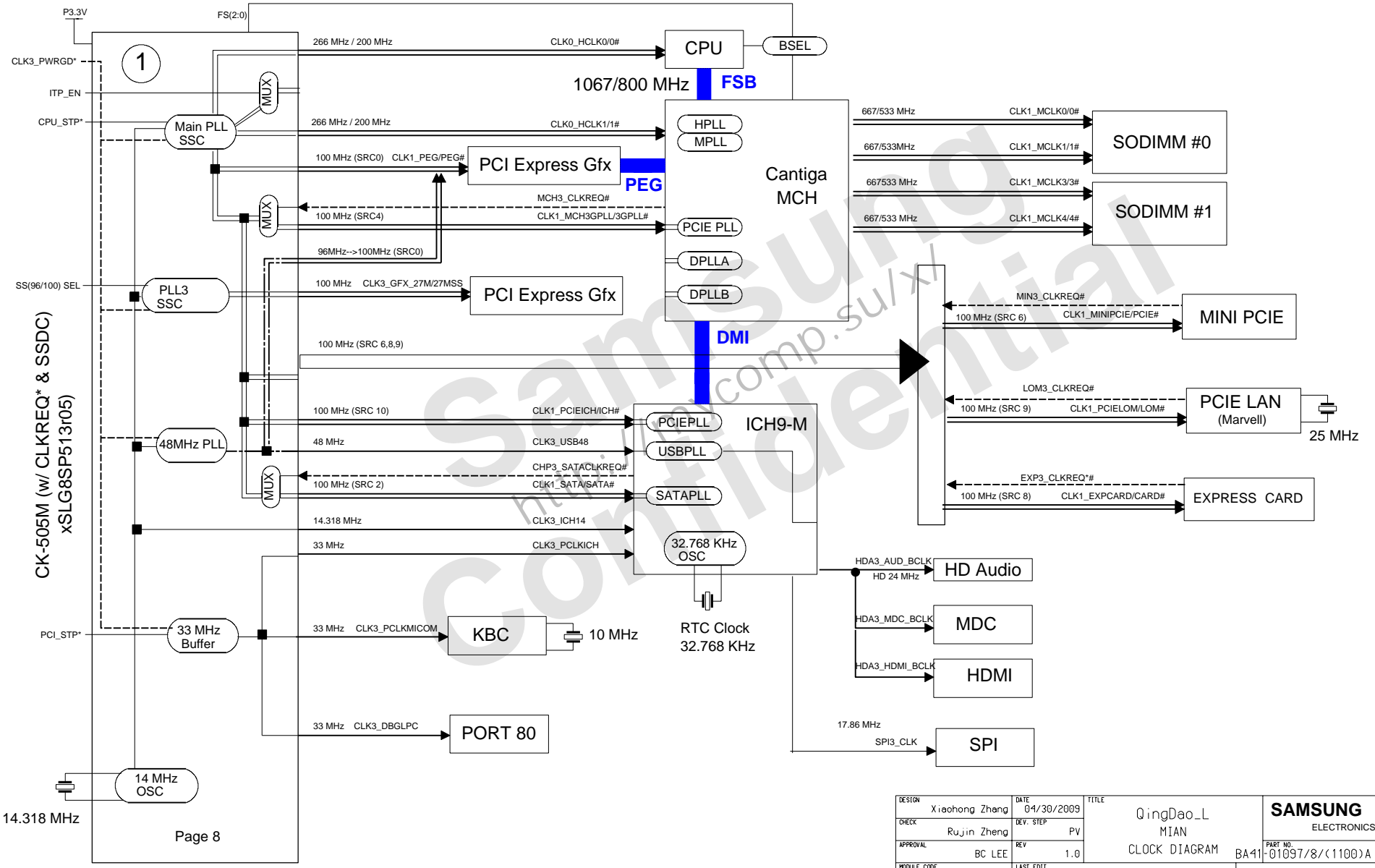
**Host S5 / ME Boot**  
 (SLPS4\* = SLPM\*) > S4\_STATE\* > SLPS3\*



DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	BA41-01097/8/((1100)A		
APPROVAL	BC LEE	REV	1.0	April 29, 2009 21:47:17 PM	PAGE 6 OF 15	
MODULE CODE		LAST EDIT				

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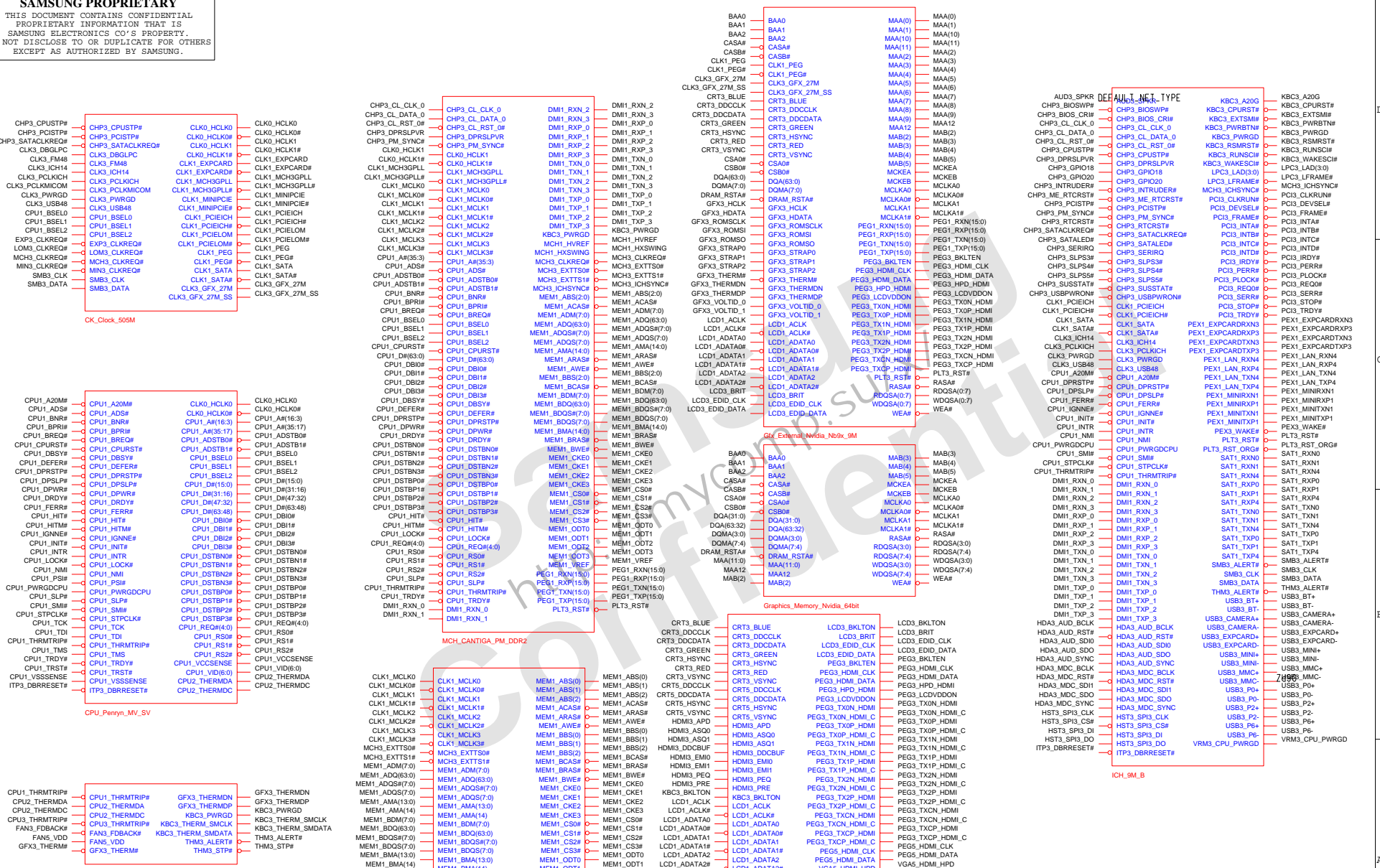
# CLOCK DISTRIBUTION Rev. 0.1



CK-505M (w/CLKREQ\* & SSDC)  
 xSLG8SP513T05

14.318 MHz  
 Page 8

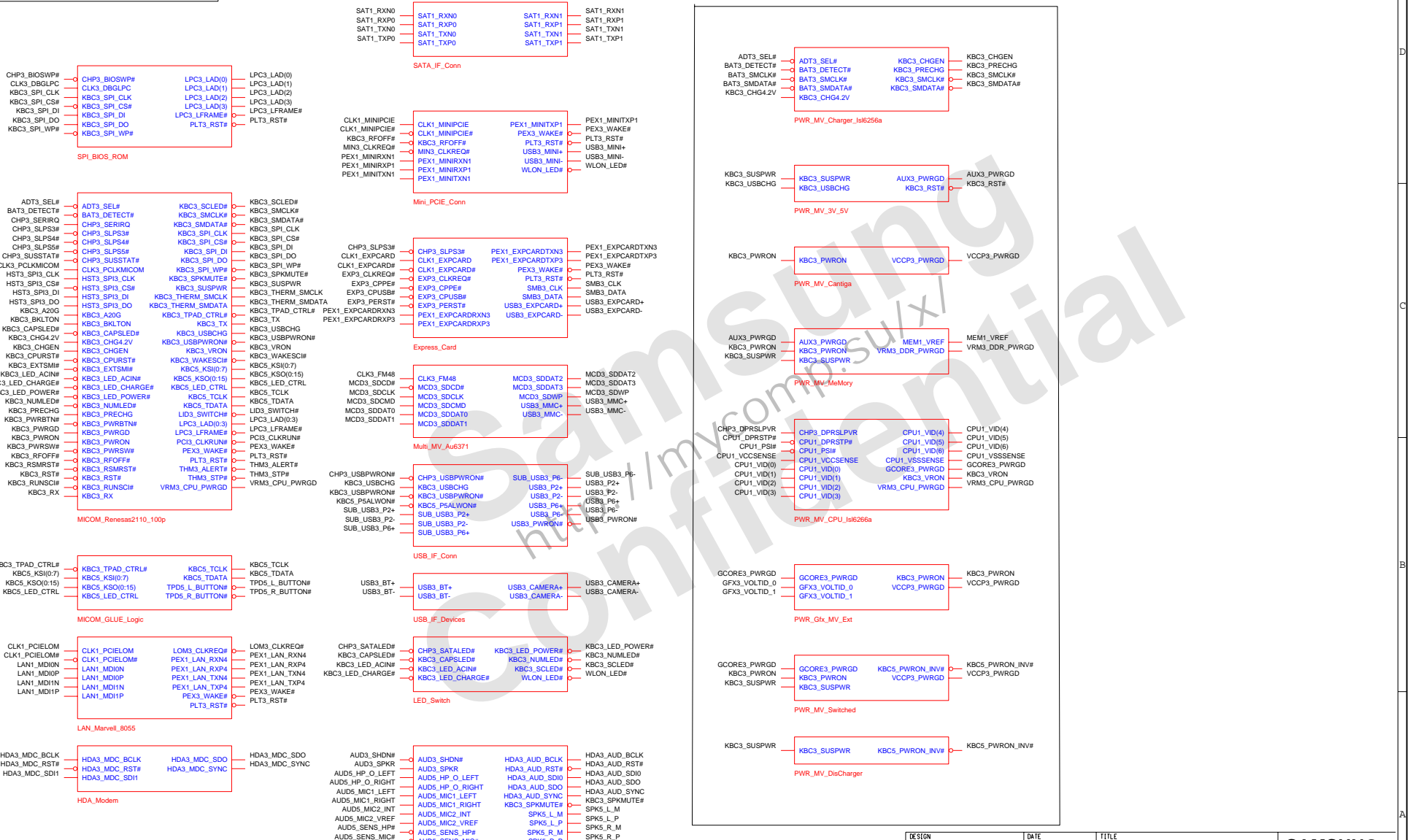
DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L MIAN CLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01097/8/(1100)A
CHECK	Rujin Zheng	REV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT				
				Apr 29, 2009 21:47:17 PM	PAGE 7 OF 15	



DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Rujin Zheng	DEV. STEP		PV	MAIN		PART NO. 01097/8/(1100) A
APPROVAL	BC LEE	REV	1.0		BLOCK		
MODULE CODE		LAST EDIT		Apr 12, 2009 21:47:17 PM	PAGE		
8 OF 15							



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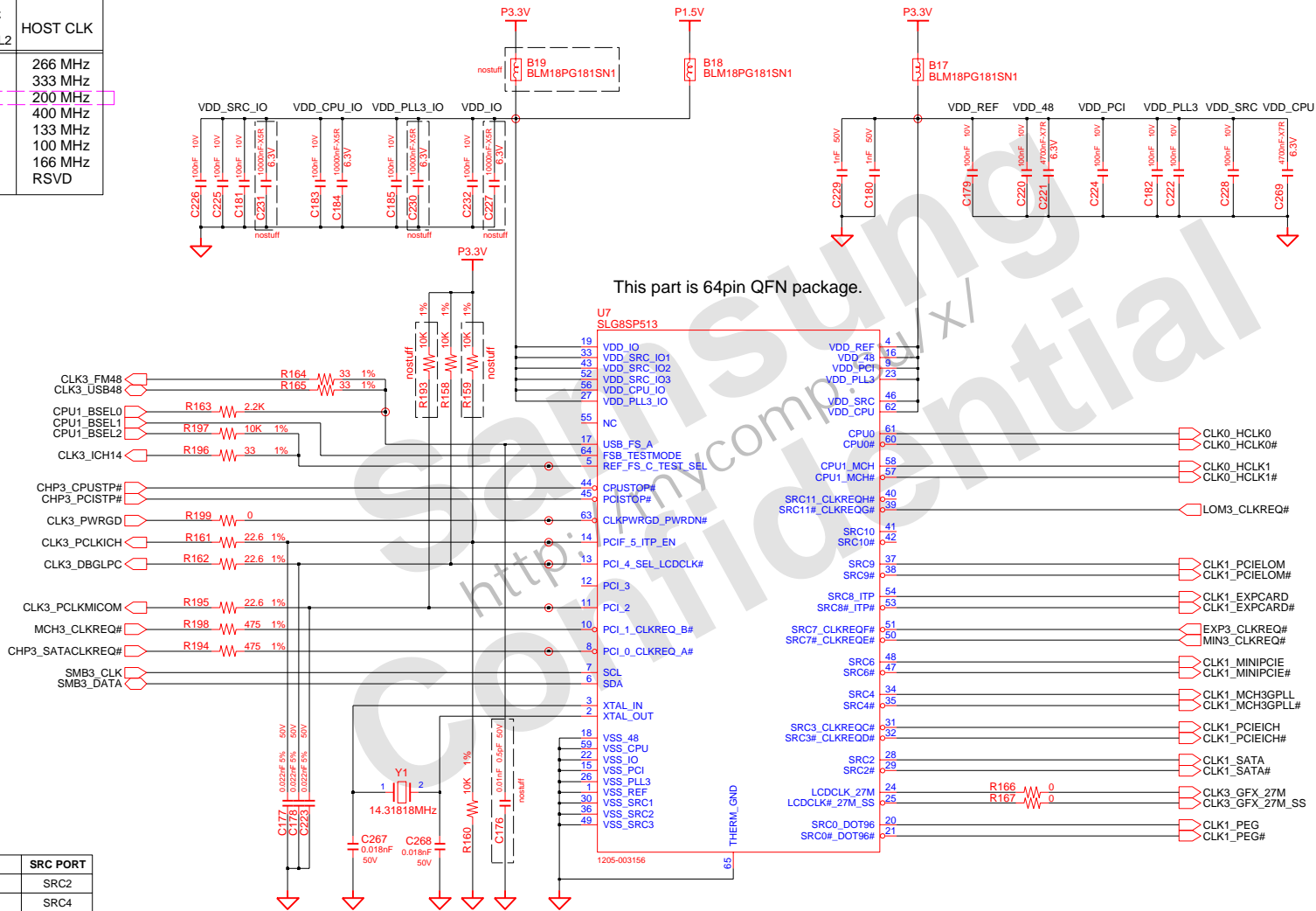


DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MAIN BLOCK	BA41-01097/8/(1100)A	
APPROVAL	BC LEE	REV	1.0	April 29, 2009 21:47:17 PM	PAGE	9 OF 15
MODULE CODE		LAST EDIT				

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# CK505M

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



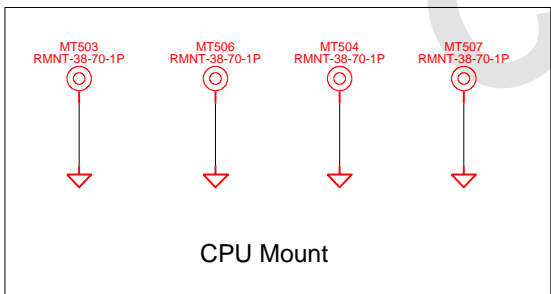
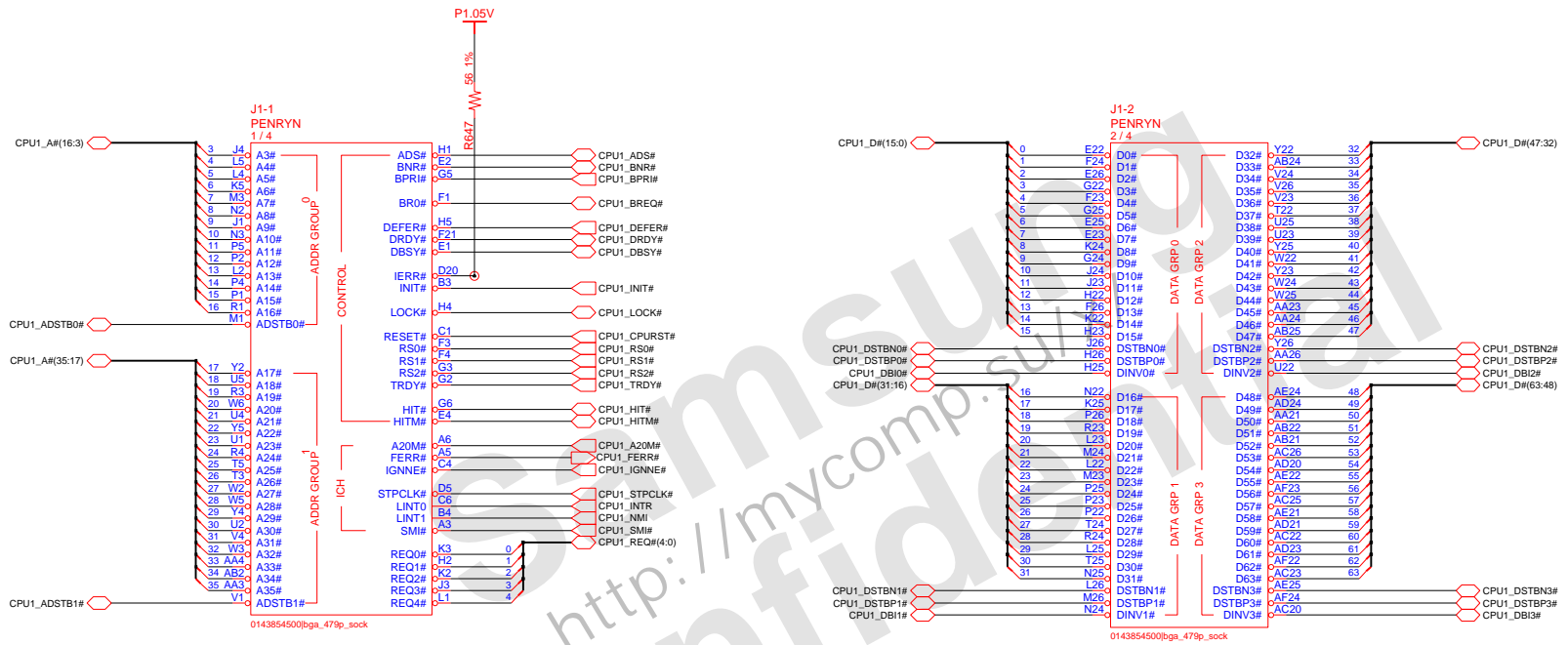
Place 14.318MHz within 500mils of CK-505

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LDCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

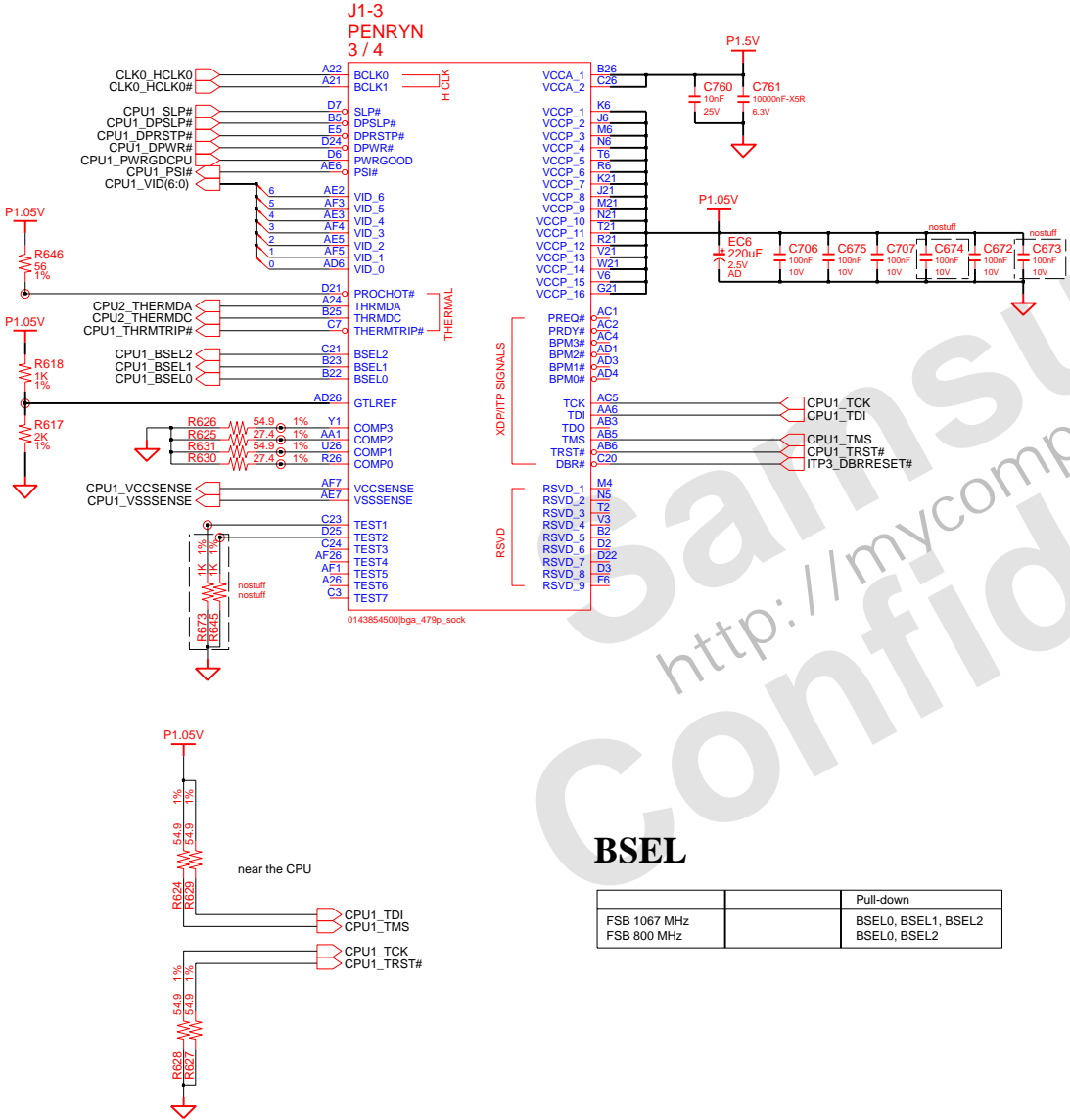
DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	Main_Clock_Circuit		
APPROVAL	BC LEE	REV	1.0	CK_Clock_505M		PART NO.
MODULE CODE	undefined	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE		1 OF 1

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DRAW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L CPU	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	REV. STEP	PV	PENRYN (1/3)	BA11-01097/8/(1100)A	
APPROVAL	BC LEE	REV	1.0	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE 1 OF 3
MODULE CODE	undefined					

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**CPU Core Voltage Table** IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 1 0 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 0	0.9625 V	1 0 1 0 1 1 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 1	0.9500 V	1 0 1 1 0 1 0	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 1 0 1 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 1 0 0 0 0	0.9250 V	1 0 1 1 0 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 0 0 1	0.9125 V	1 0 1 1 1 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 1 0	0.9000 V	1 0 1 1 1 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 1 1	0.8875 V	1 0 1 1 1 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 1 0 0 0	0.8750 V	1 0 1 1 1 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 1 0 0 1	0.8625 V	1 0 1 1 1 1 1	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 1 0 1 0	0.8500 V	1 0 1 1 1 1 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 1 0 1 1	0.8375 V	1 0 1 1 1 1 1	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 1 1 0 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 1 0 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 1 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 1 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 1 1 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 1 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 0	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 1	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 1 0 0 0	1.0000 V	1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
0 1 0 1 0 0 1	0.9875 V	1 0 0 1 1 1 1	0.4875 V	1 1 1 1 0 1 0	0.0000 V
0 1 0 1 0 0 1	0.9750 V	1 0 0 1 1 1 1	0.4750 V	1 1 1 1 0 1 1	0.0000 V
0 1 0 1 0 1 0	0.9625 V	1 0 0 1 1 1 1	0.4625 V	1 1 1 1 1 0 0	0.0000 V
0 1 0 1 0 1 1	0.9500 V	1 0 0 1 1 1 1	0.4500 V	1 1 1 1 1 1 0	0.0000 V
0 1 0 1 1 0 0	0.9375 V	1 0 0 1 1 1 1	0.4375 V	1 1 1 1 1 1 1	0.0000 V
0 1 0 1 1 0 1	0.9250 V	1 0 0 1 1 1 1	0.4250 V	1 1 1 1 1 1 1	0.0000 V
0 1 0 1 1 1 0	0.9125 V	1 0 0 1 1 1 1	0.4125 V	1 1 1 1 1 1 1	0.0000 V
0 1 0 1 1 1 1	0.9000 V	1 0 0 1 1 1 1	0.4000 V	1 1 1 1 1 1 1	0.0000 V

\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5° of the first GTLREF pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

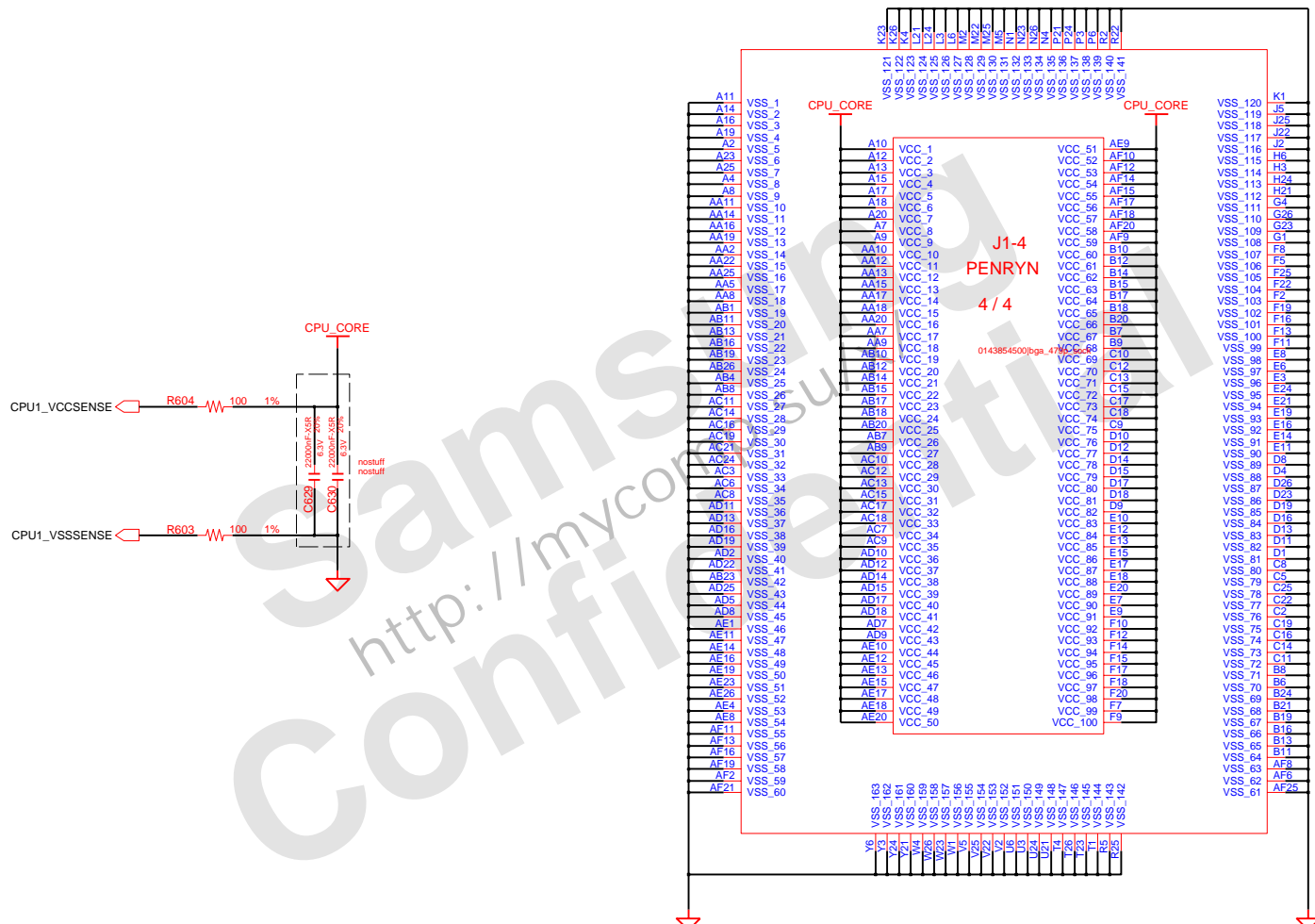
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

**BSEL**

FSB 1067 MHz		Pull-down
FSB 800 MHz		BSELO, BSEL1, BSEL2 BSELO, BSEL2

DRW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L CPU	PART NO. 01097/8/(1100)A	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PENRYN (2/3)			
APPROVAL	BC LEE	REV	1.0	April 29, 2009 21:47:17 PM		PAGE	2 OF 3
MODULE CODE	undefined	LAST EDIT					

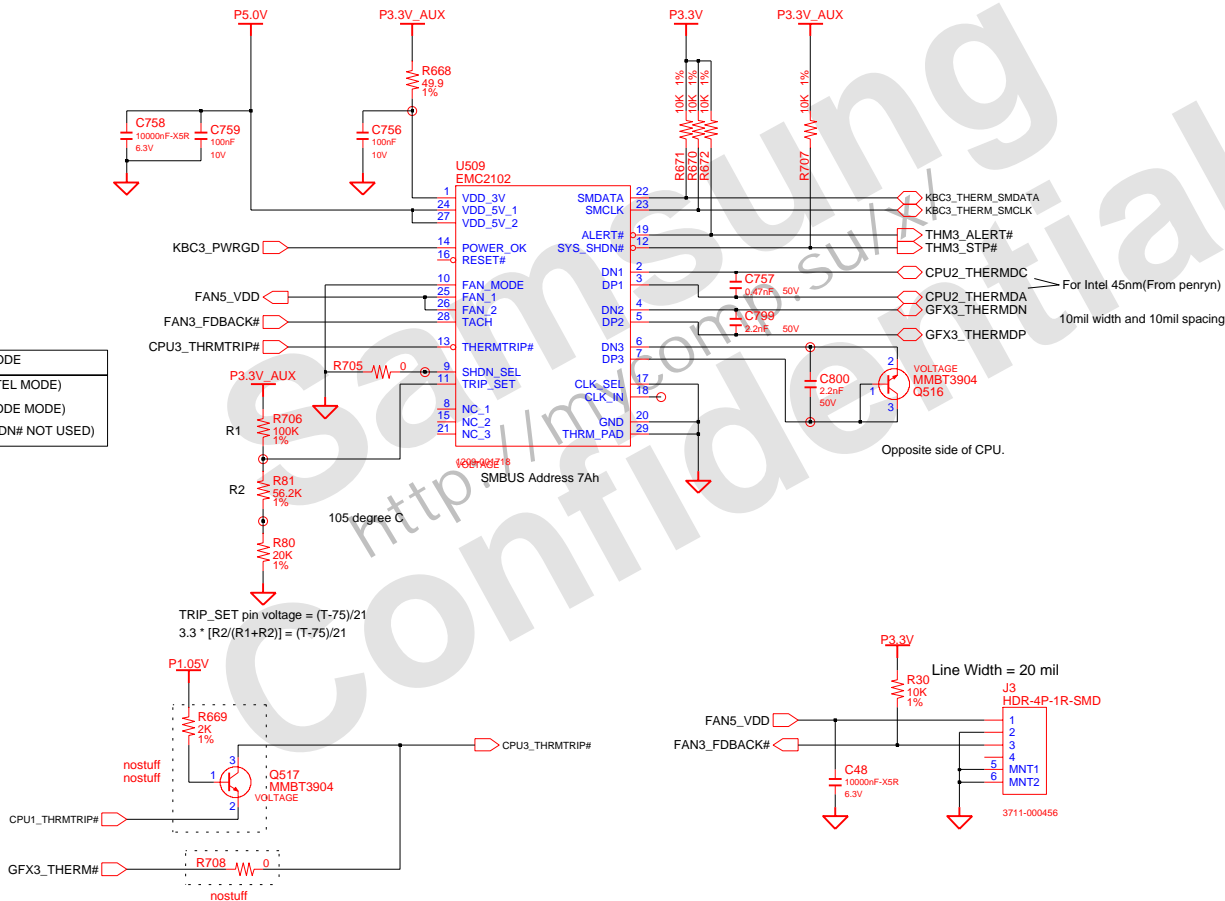
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DRW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01097/8/(1100)A
CHECK	Rujin Zheng	REV. STEP	PV		CPU	
APPROVAL	BC LEE	REV	1.0		PENRYN (3/3)	
MODULE CODE	undefined	LAST EDIT		April 29, 2009 21:47:17 PM		
					PAGE 3 OF 3	

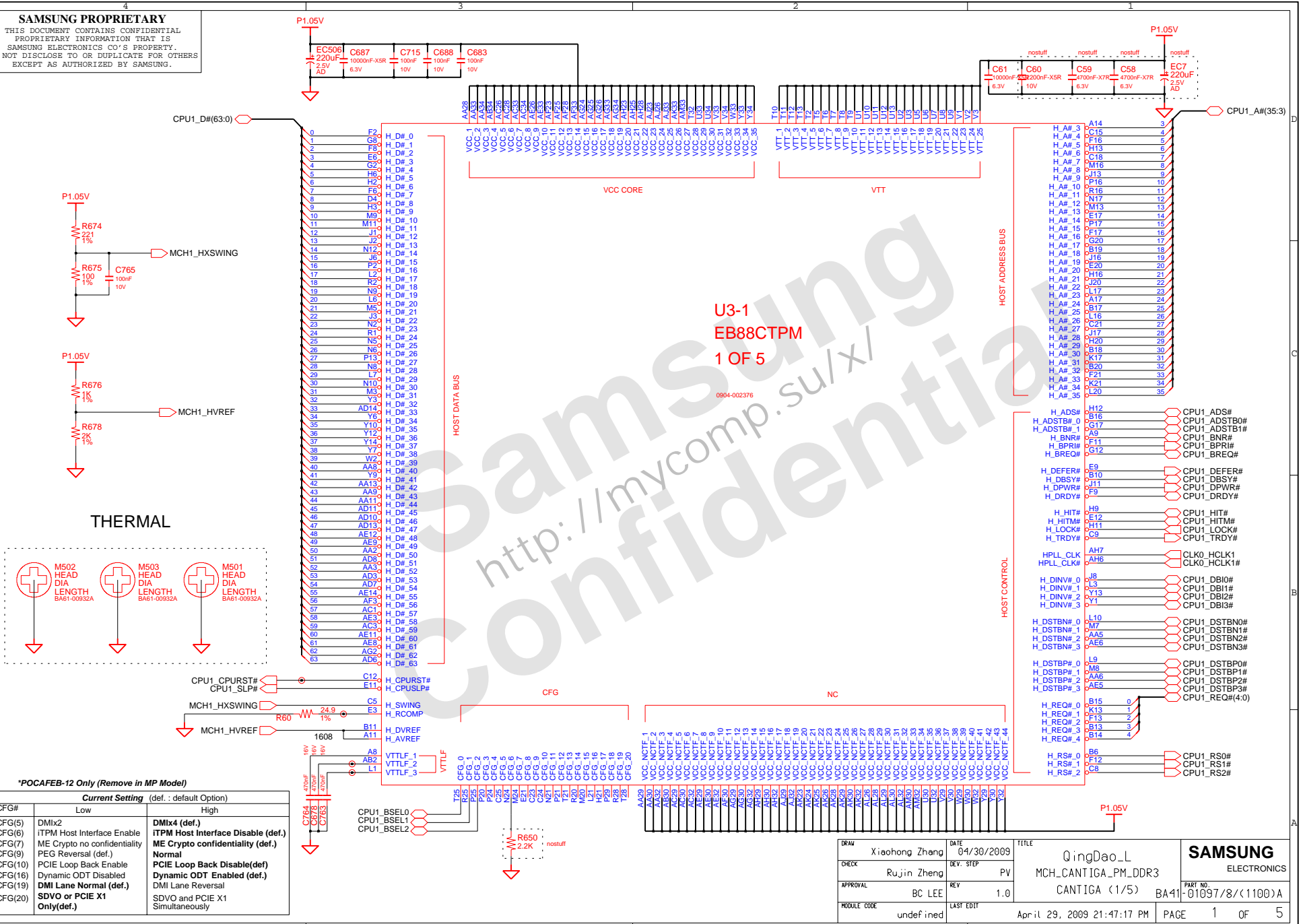
# THERMAL SENSOR & FAN CONTROL

SHDN_SEL MODE	
0	CH1(INTEL MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

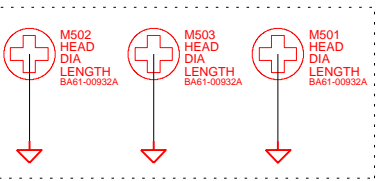


DESIGN	XIAOHONG, ZHANG	DATE	12/3/2008	TITLE	QingDao_Ext	<b>SAMSUNG</b> ELECTRONICS
CHECK	RUJIN, ZHENG	DEV. STEP	ADV1	THERMAL SENSOR EMC2102	PART NO.	
APPROVAL	BC, LEE	REV	1.0		BA41-xxxxxA	
MODULE CODE		LAST EDIT	December, 3, 2008 12:55:11 PM	PAGE	1 OF 1	

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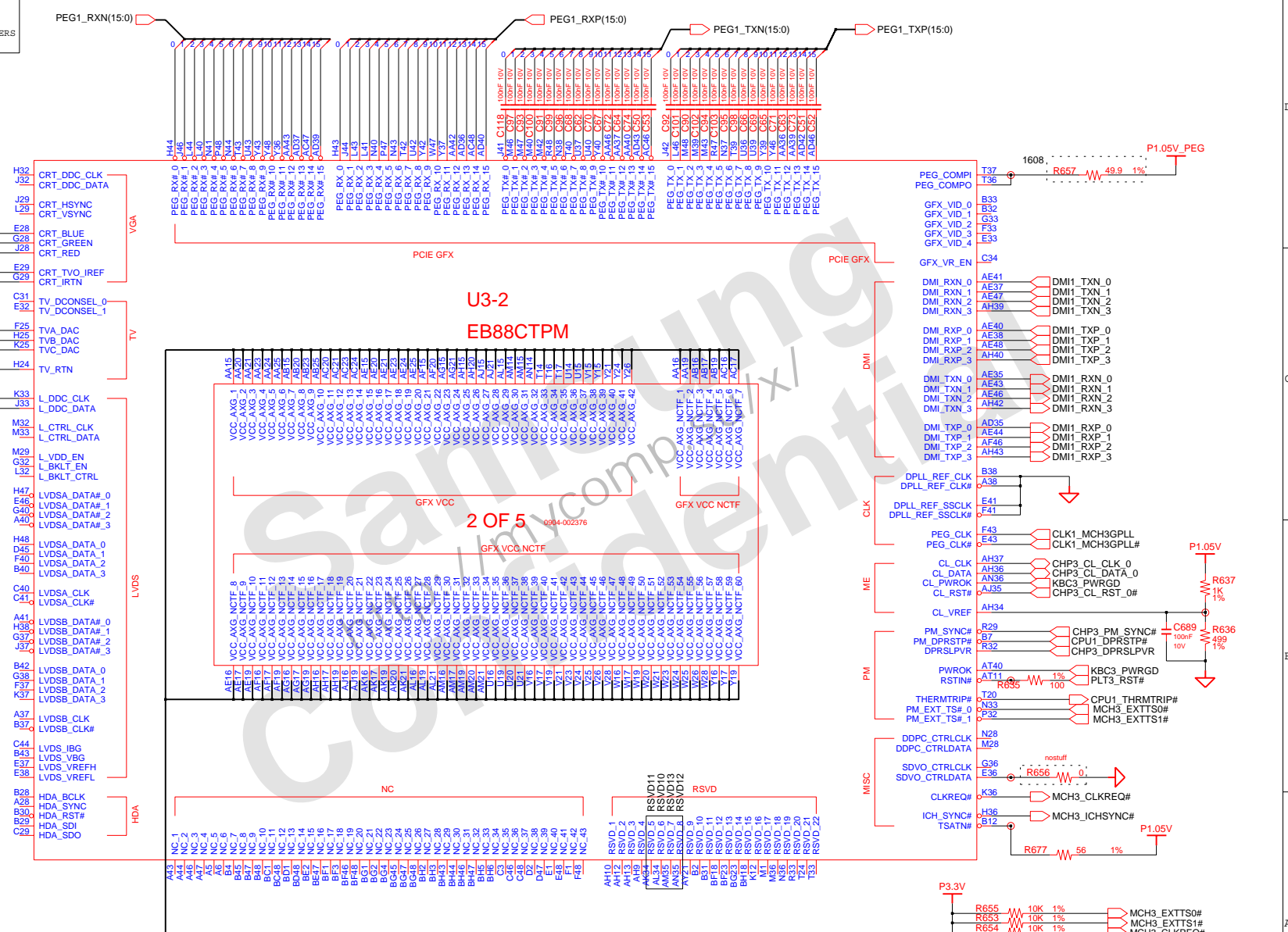
**THERMAL**



**\*POCAFEB-12 Only (Remove in MP Model)**

CFG#	Current Setting (def.: default Option)	High
CFG(5)	DMIX2	DMIX4 (def.)
CFG(6)	ITPM Host Interface Enable	ITPM Host Interface Disable (def.)
CFG(7)	ME Crypto no confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIE Loop Back Enable	PCIE Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

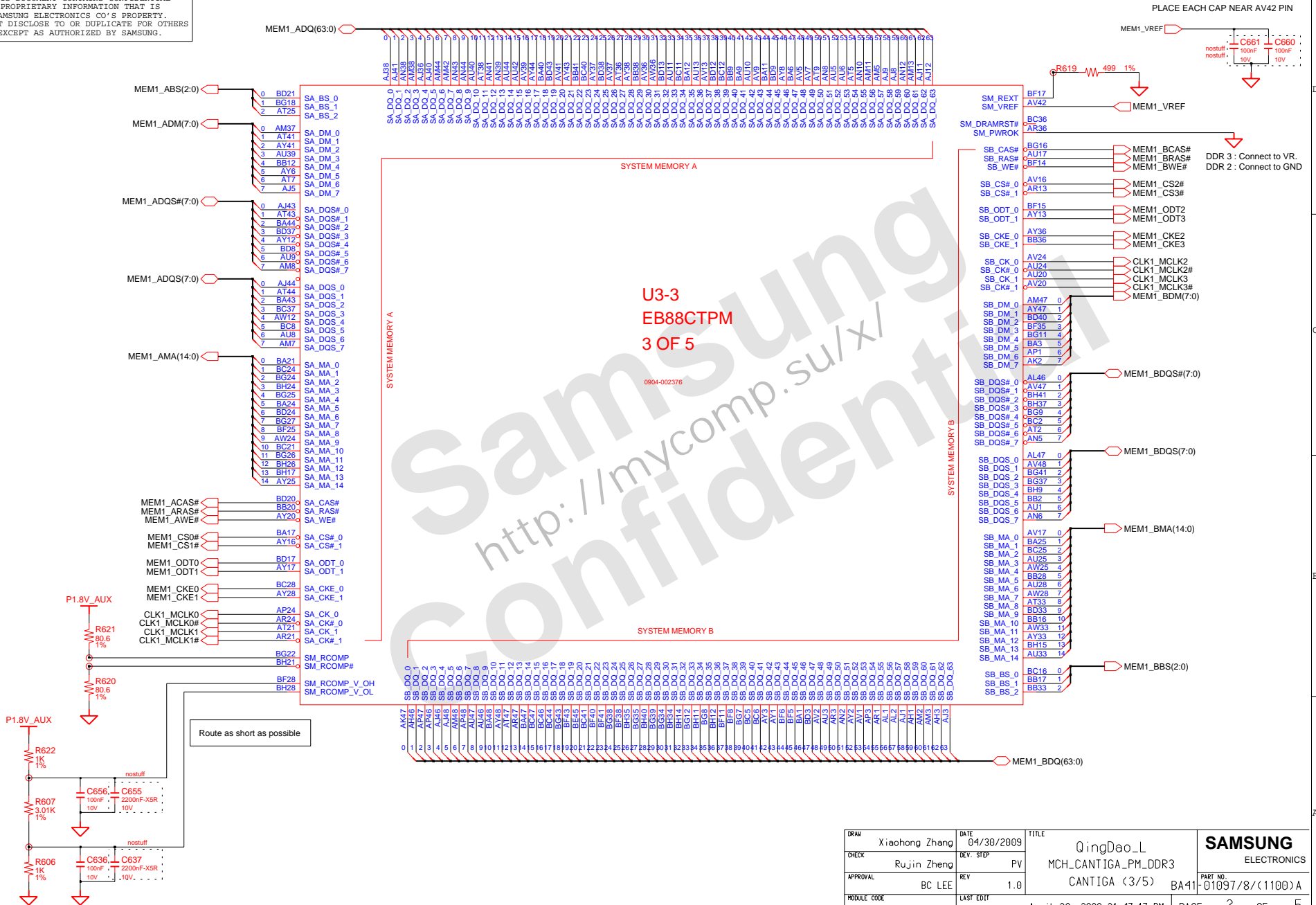
DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MCH_CANTIGA_PM_DDR3		
APPROVAL	BC LEE	REV	1.0	CANTIGA (1/5)	BA41	PART NO. 01097/8/(1100)A
MODULE CODE	undefined	LAST EDIT	Apr 19, 2009 21:47:17 PM	PAGE	1	OF 5



DRWN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Rujin Zheng	DEV. STEP	PV	MCH_CANTIGA_PM_DDR3			
APPROVAL	BC LEE	REV	1.0	CANTIGA (2/5)	BA41-01097/8/(1100)A	PART NO.	
MODULE CODE	undefined	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	2	OF	5



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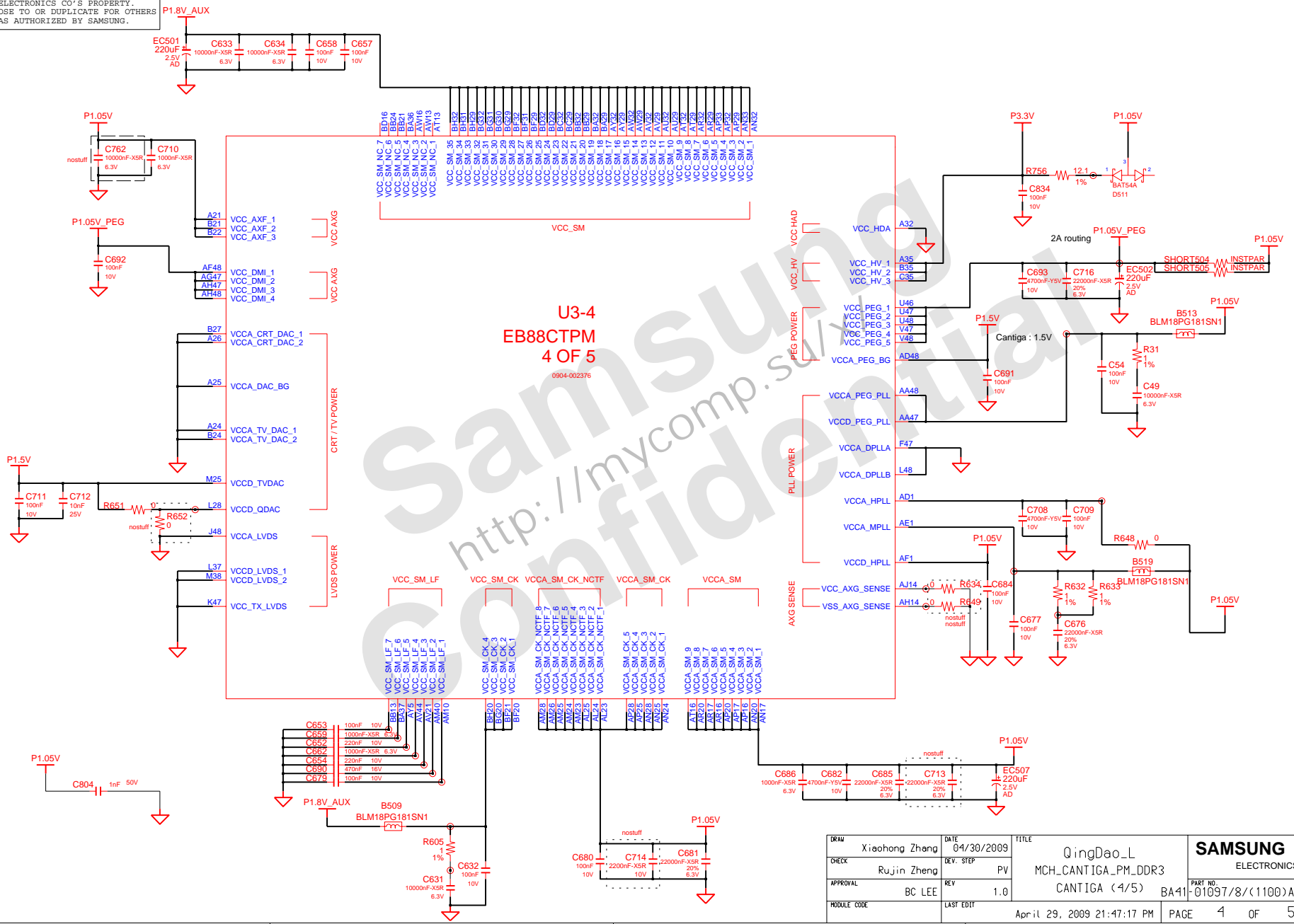
PLACE EACH CAP NEAR AV42 PIN

DDR 3 : Connect to VR.  
 DDR 2 : Connect to GND

Route as short as possible

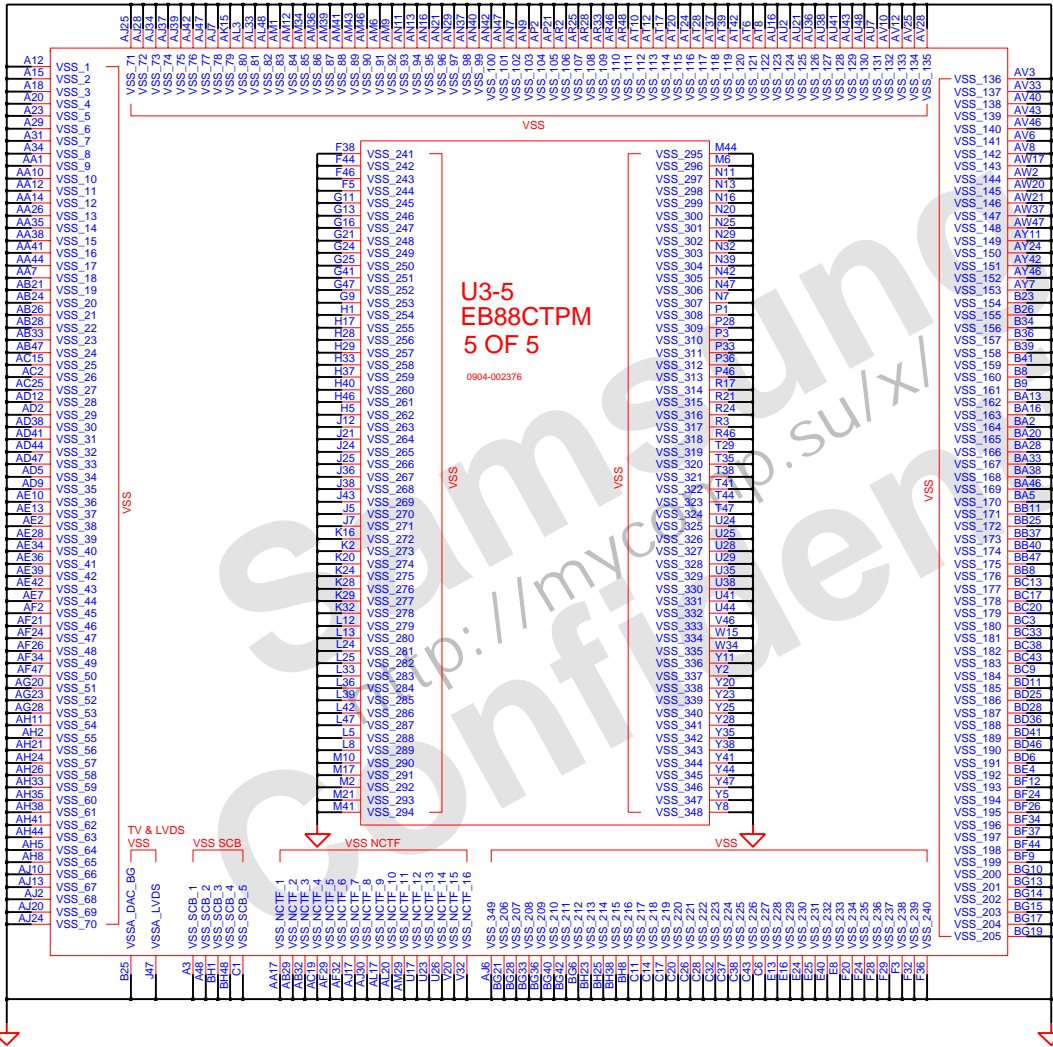
DRW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MCH_CANTIGA_PM_DDR3		
APPROVAL	BC LEE	REV	1.0	CANTIGA (3/5)	BA41	PART NO. 01097/8/(1100)A
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM	PAGE	3 OF 5

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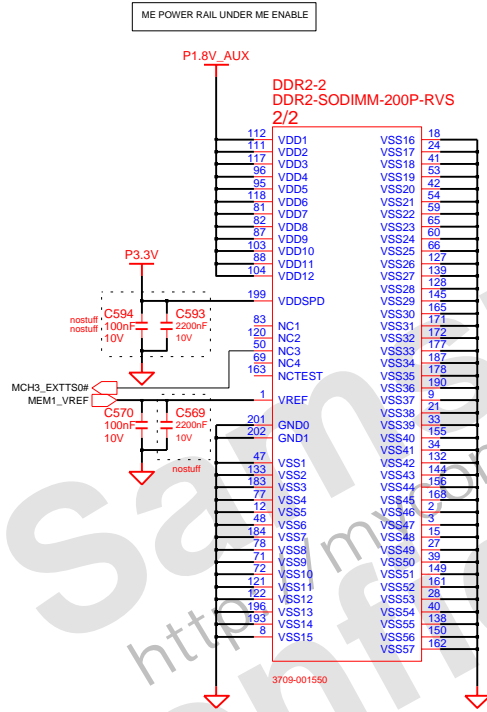
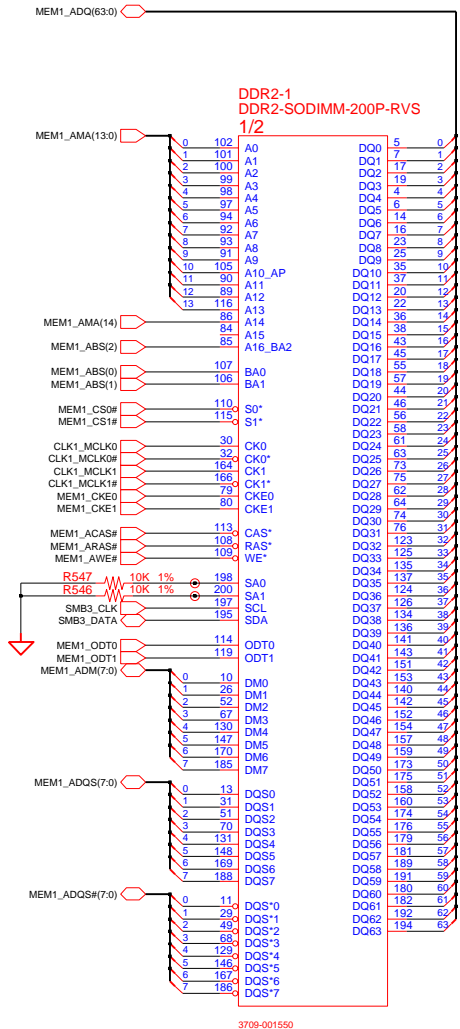
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CHECK	Rujin Zheng	DEV. STEP	PV	MCH_CANTIGA_PM_DDR3		
APPROVAL	BC LEE	REV	1.0	CANTIGA (4/5)	BA41-01097/8/(1100)A	PART NO.
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	4	OF
						5

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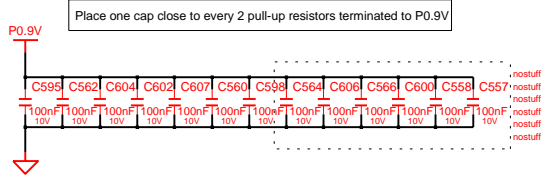
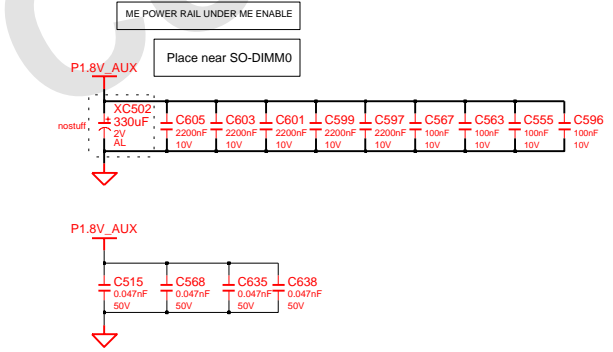
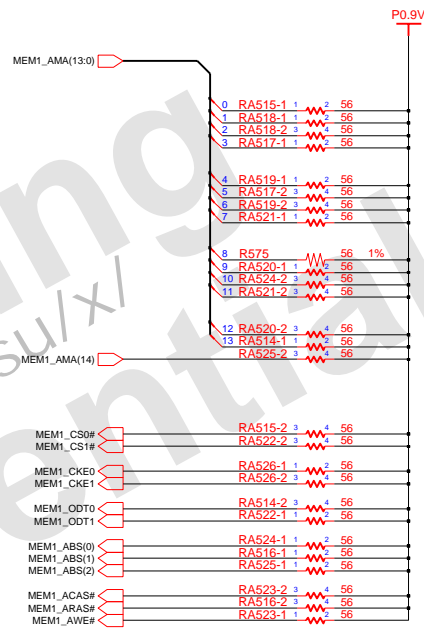


DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS PART NO. MCH-CANTIGA_PM1N/8/(1100)A 01097/8/(1100)A
CHECK	Rujin Zheng	DEV. STEP	PV	MCH-CANTIGA_PM_DDR3		
APPROVAL	BC LEE	REV	1.0	CANTIGA (5/5)		
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM		

# DDR SO-DIMM #0



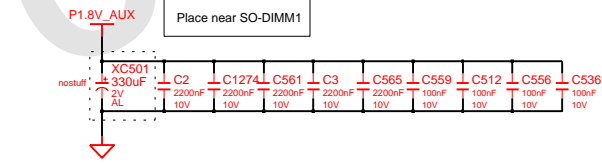
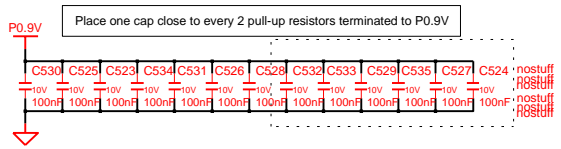
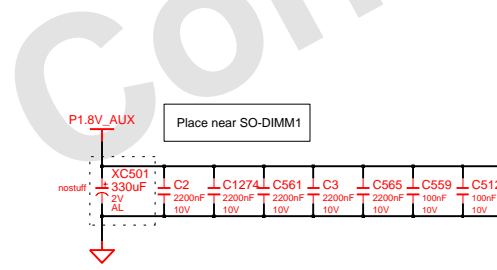
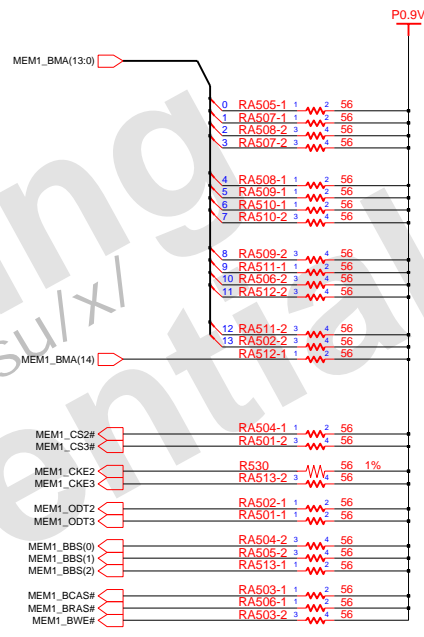
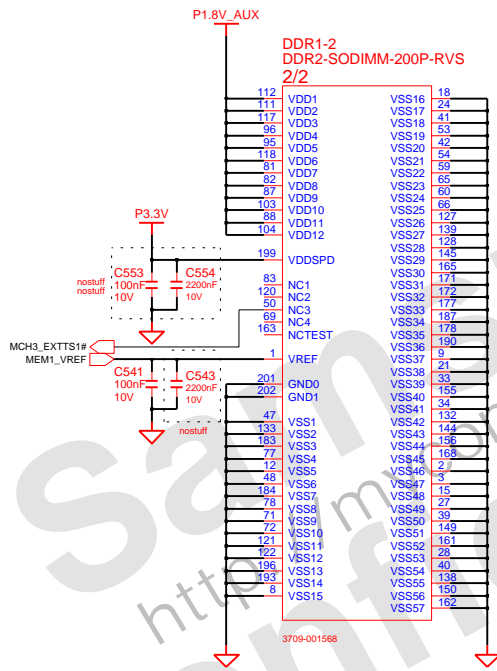
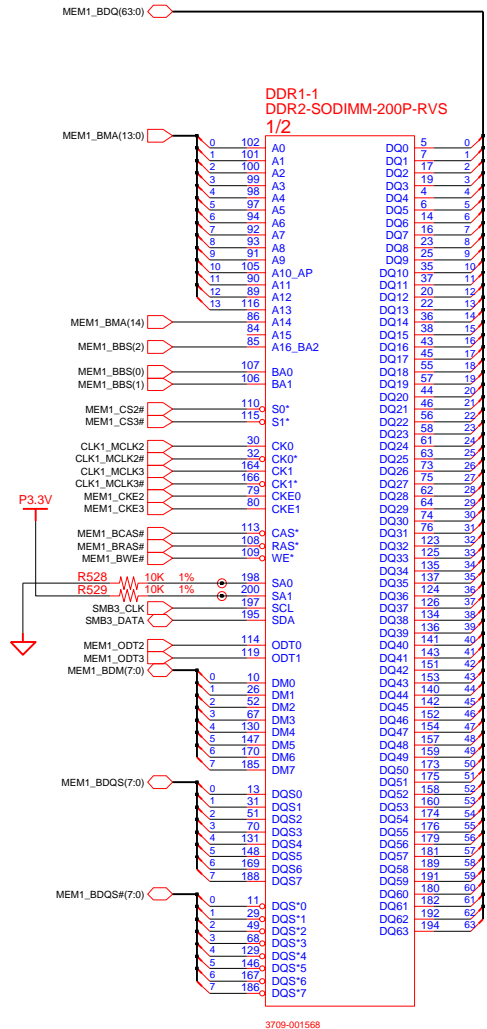
Array resistors & Single resistors used to improve layout & routing.



DRAW	XiaoHong Zheng	DATE	12/03/2008	TITLE	QingDao_Ext	<b>SAMSUNG</b> ELECTRONICS
CHECK	RuJin Zheng	DEV. STEP	ADV1	SODIMM_DDR2		
APPROVAL	BC LEE	REV	1.0	SODIMM_DDR2 #1		PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT	December 03, 2008 20:55:25 PM	PAGE	1 OF 2	

# DDR SO-DIMM #1

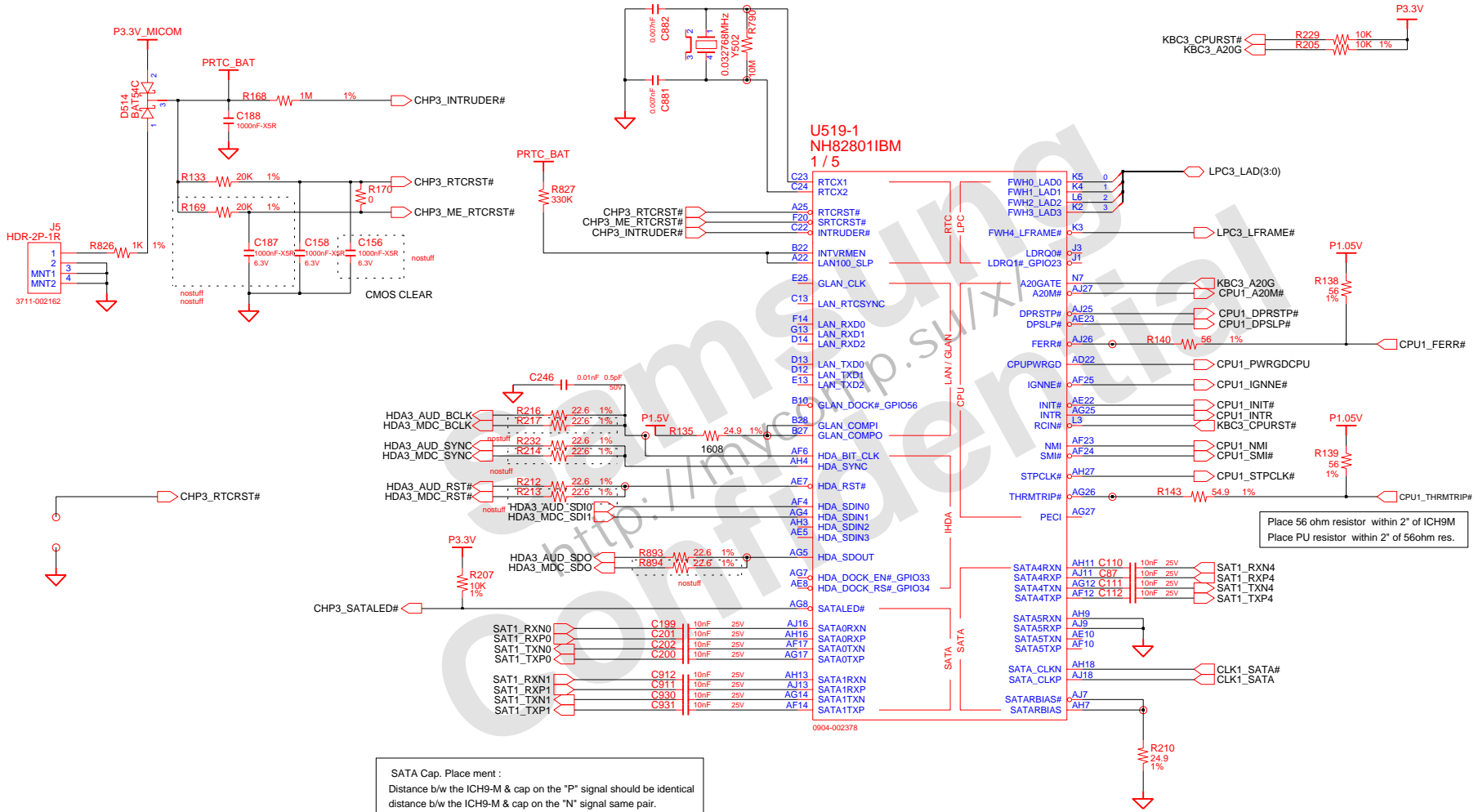
Array resistors & Single resistors used to improve layout & routing.



3709-001568

DRAW	XiaoHong Zheng	DATE	12/03/2008	TITLE	QingDao_Ext	<b>SAMSUNG</b> ELECTRONICS
CHECK	RuJin Zheng	DEV. STEP	ADV1	SODIMM_DDR2		
APPROVAL	BC LEE	REV	1.0	SODIMM_DDR2 #2		PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT	December 03, 2008 20:55:25 PM	PAGE	2 OF 2	

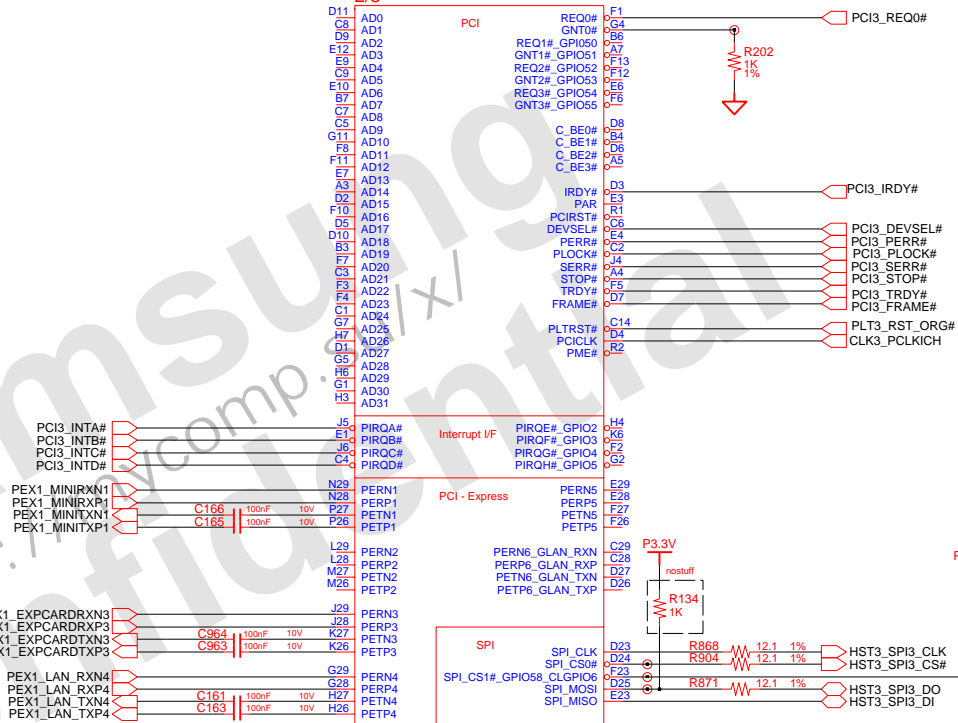
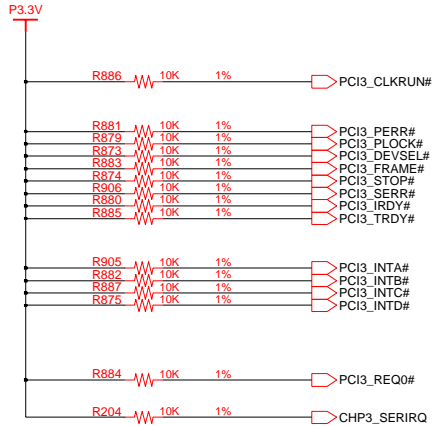
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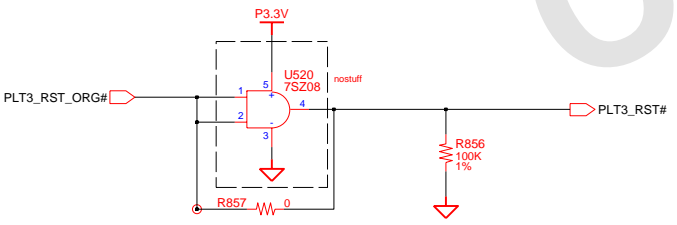
DRAW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		ICH_9M_B	
APPROVAL	BC LEE	REV	1.0		ICH9-M (1/5)	PART NO.
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM		BA41-01097/8/(1100)A
					PAGE	1 OF 5

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**U519-2**  
**NH82801IBM**  
**2/5**

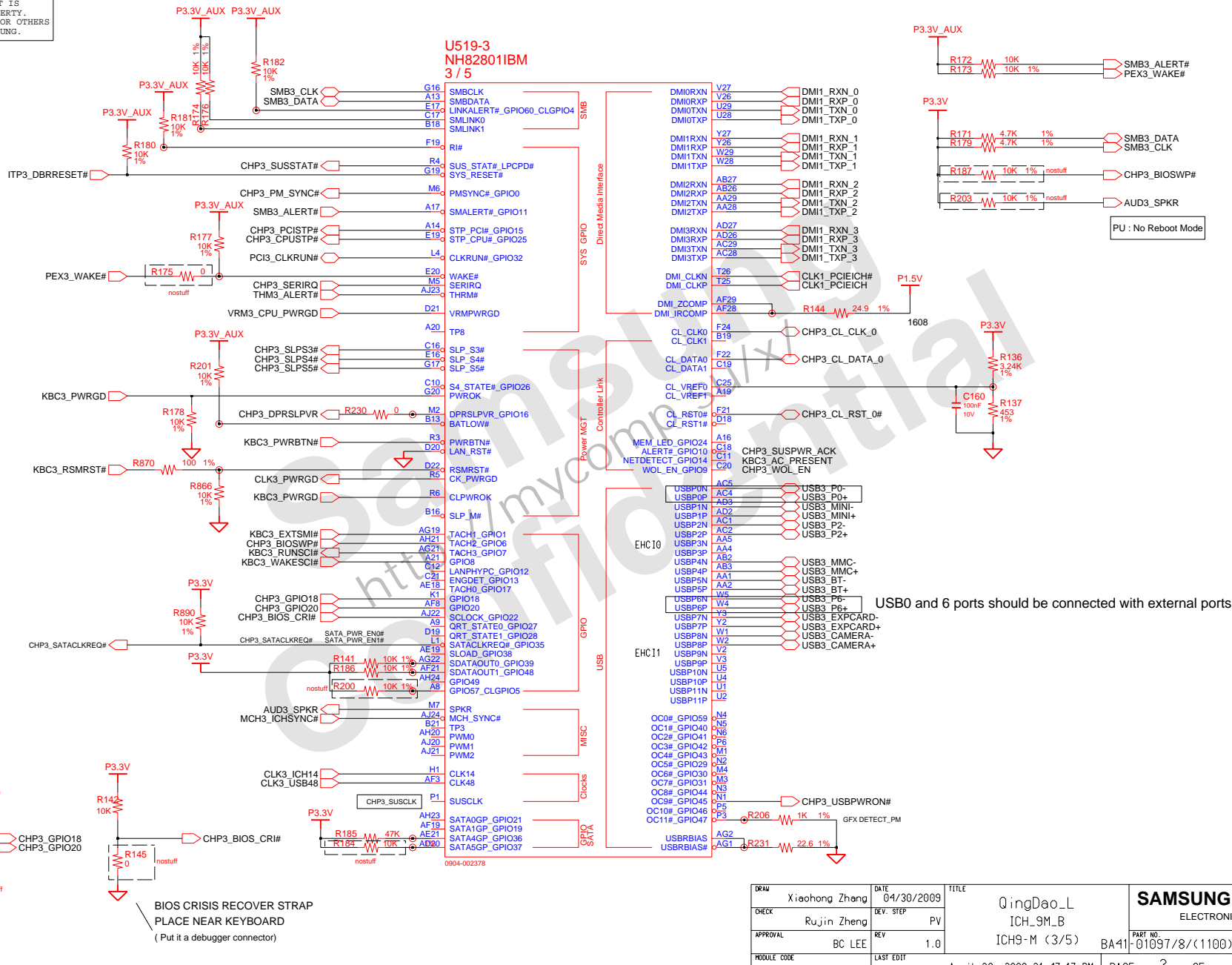


AC caps : PCIE need to be within 250mils of the driver  
 Resistor for Test : Place Stuffed Option to minimize stubs



DRW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Rujin Zheng	DEV. STEP	PV		ICH_9M_B		
APPROVAL	BC LEE	REV	1.0		ICH9-M (2/5)	PART NO.	
MODULE CODE	undefined	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	2	OF	5

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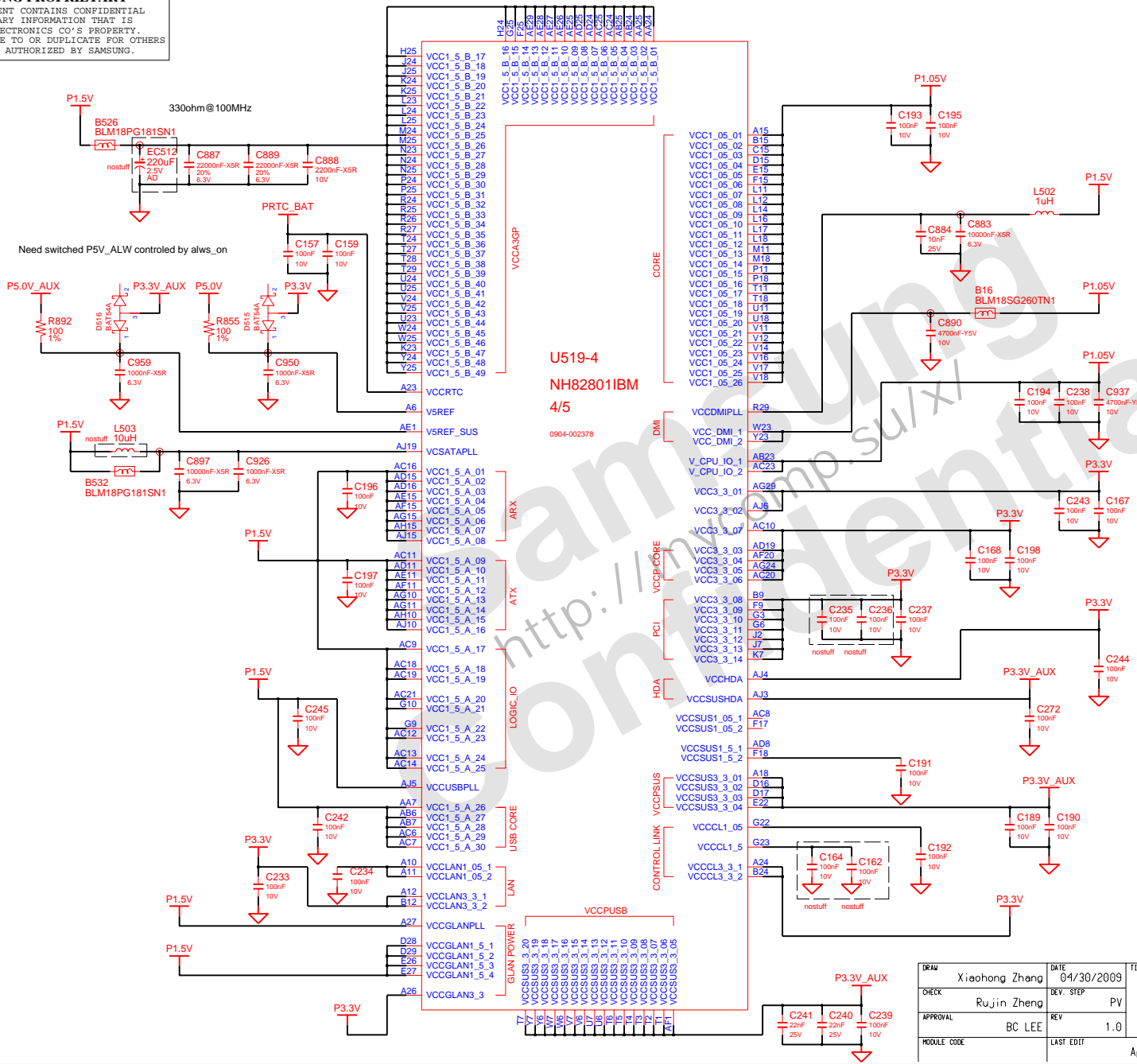


USB0 and 6 ports should be connected with external ports

DRW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Rujin Zheng	DEV. STEP	PV	ICH_9M_LB			
APPROVAL	BC LEE	REV	1.0	ICH9-M (3/5)	BA41-01097/8/(1100)A	PART NO.	
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	3	OF	5



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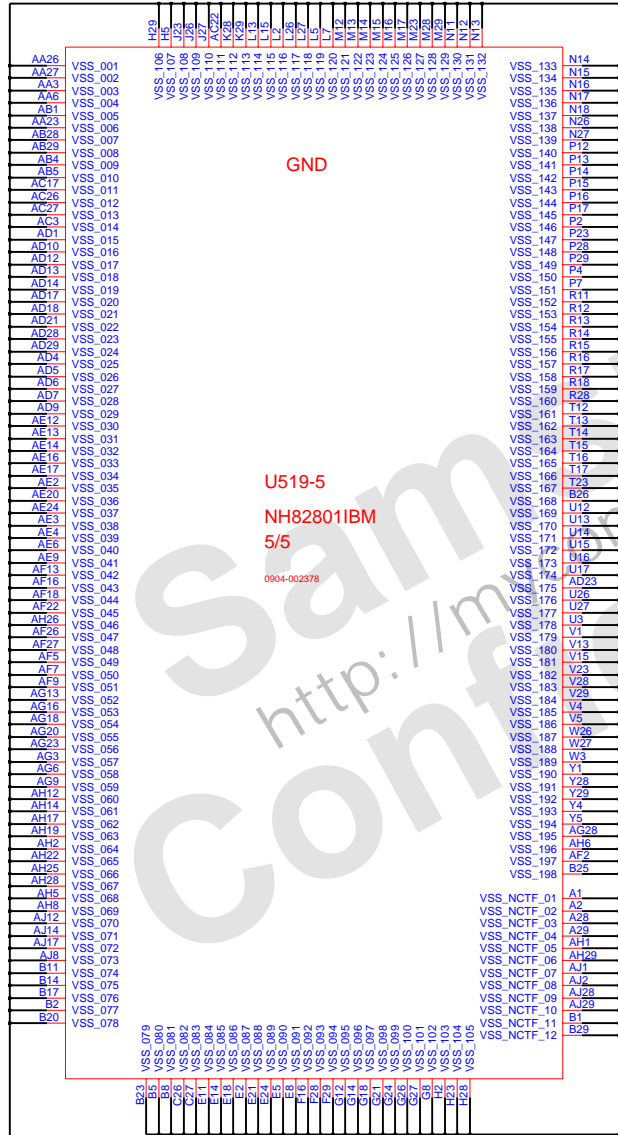


DRAW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L
CHECK	Rujin Zheng	DEV. STEP	PV		ICH_9M_B
APPROVAL	BC LEE	REV	1.0		ICH9-M (3/5)
MODULE CODE		LAST EDIT			April 29, 2009 21:47:17 PM

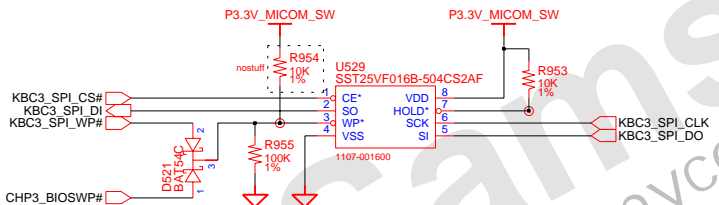
<b>SAMSUNG</b> ELECTRONICS	
PART NO.	BA41-01097/8/(1100)A
PAGE	4 OF 5

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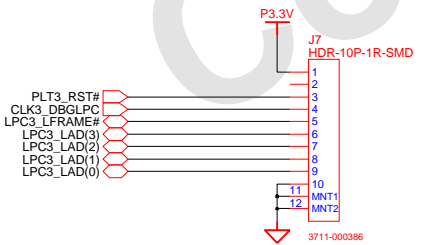


DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	ICH_9M_B	ICH9-M (3/5)	
APPROVAL	BC LEE	REV	1.0		BA41	PART NO. 01097/8/(1100)A
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM	PAGE	4 OF 5

# SPI\_BIOS\_ROM



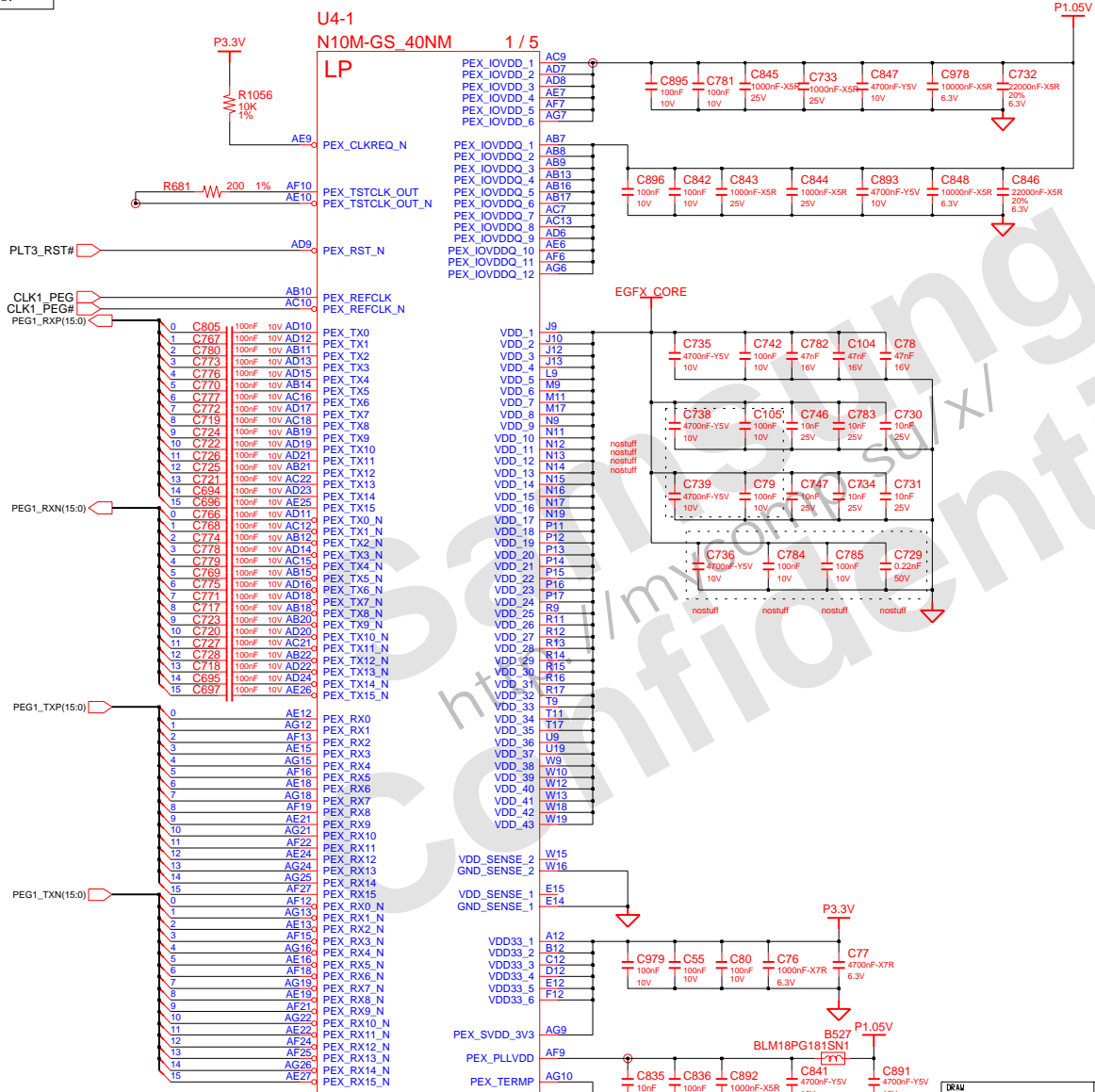
80H DECODER CONNECTOR



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT. EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE HW INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TEST CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYLOCK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY "PRESS ..... SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

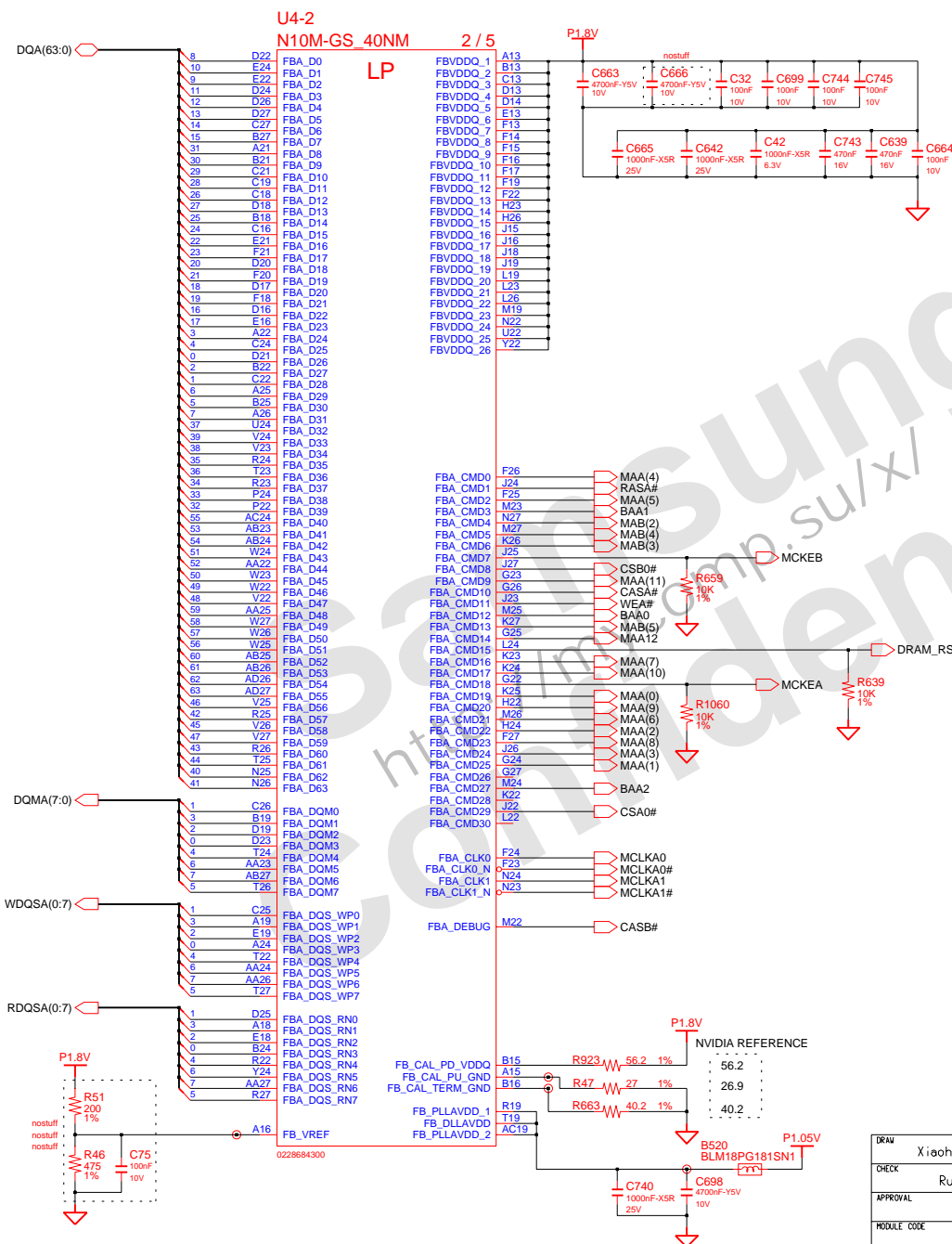
DRW	XiaoHong Zhang	DATE	12/03/2008	TITLE	QingDao_Ext	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	RuJin Zheng	DEV. STEP	ADV1		SPI_BIOS_ROM	
APPROVAL	BC LEE	REV	1.0		SPI_BIOS_ROM	
MODULE CODE		LAST EDIT	December 03, 2008 20:56:20 PM	PAGE	1 OF 1	

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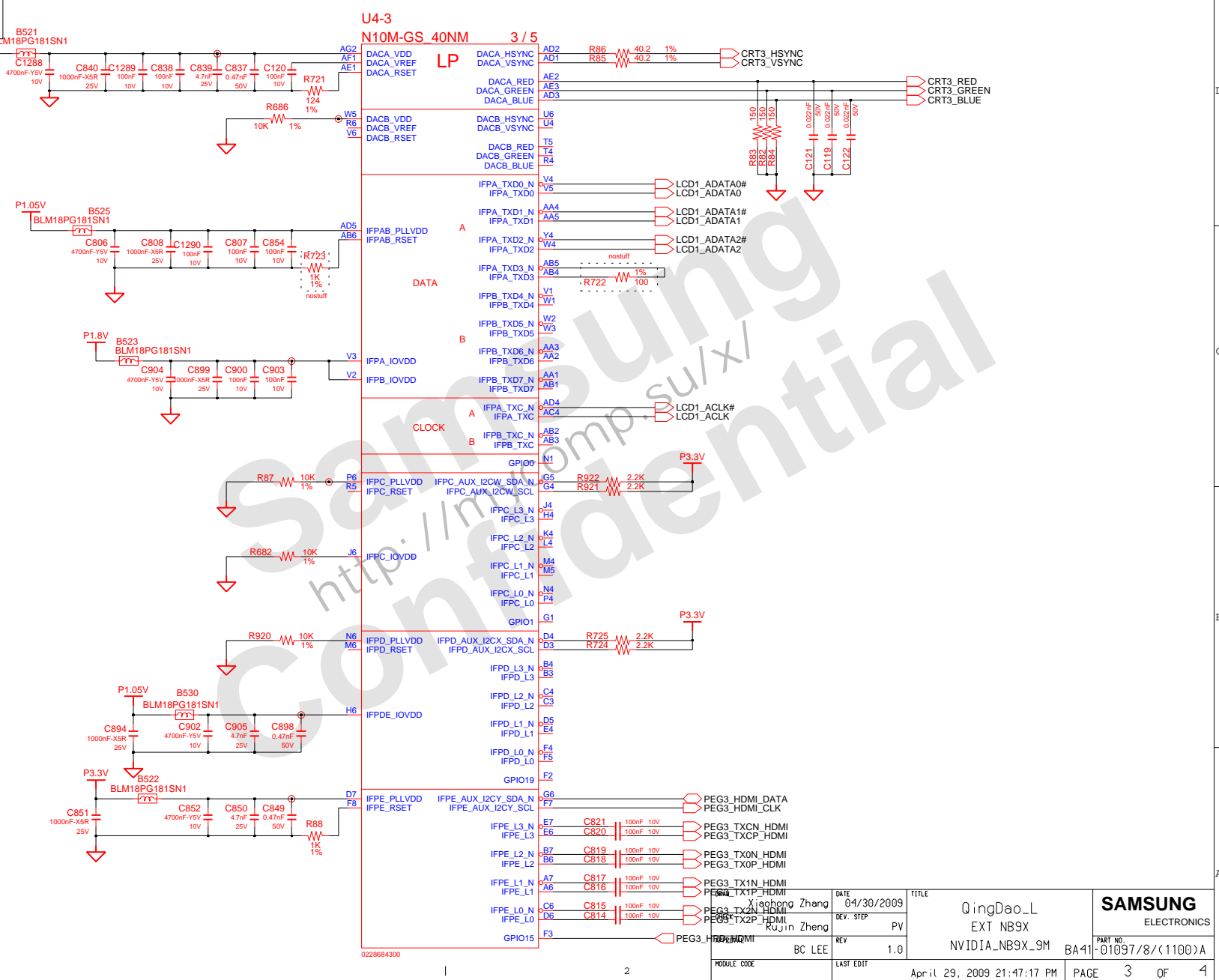
DRN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	EXT NB9X		
APPROVAL	BC LEE	REV	1.0	NVIDIA_NB9X_9M		PART NO.
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	BA41-01097/8/(1100)A		01097/8/(1100)A
				PAGE	1	OF 4

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DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L EXT NB9X	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	NVIDIA_NB9X_9M		
APPROVAL	BC LEE	REV	1.0	PART NO. BA41-01097/8/(1100)A		PAGE 2 OF 4
MODULE CODE		LAST EDIT	Apr 19, 2009 21:47:17 PM			

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DATE	04/30/2009	TITLE	QingDao_L EXT_NB9X	<b>SAMSUNG</b> ELECTRONICS
DEV. STEP	PV	REV	1.0	
DESIGNER	Xiaohong Zheng	DATE	04/30/2009	PART NO. BA41-01097/8/(1100)A
DESIGNER	Rujin Zheng	REV	1.0	
MODULE CODE	BC LEE	LAST EDIT	Apr 19, 2009 21:47:17 PM	PAGE 3 OF 4

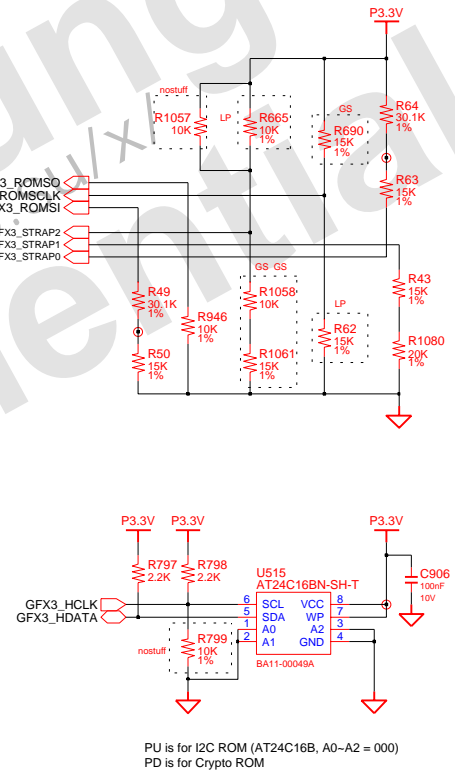
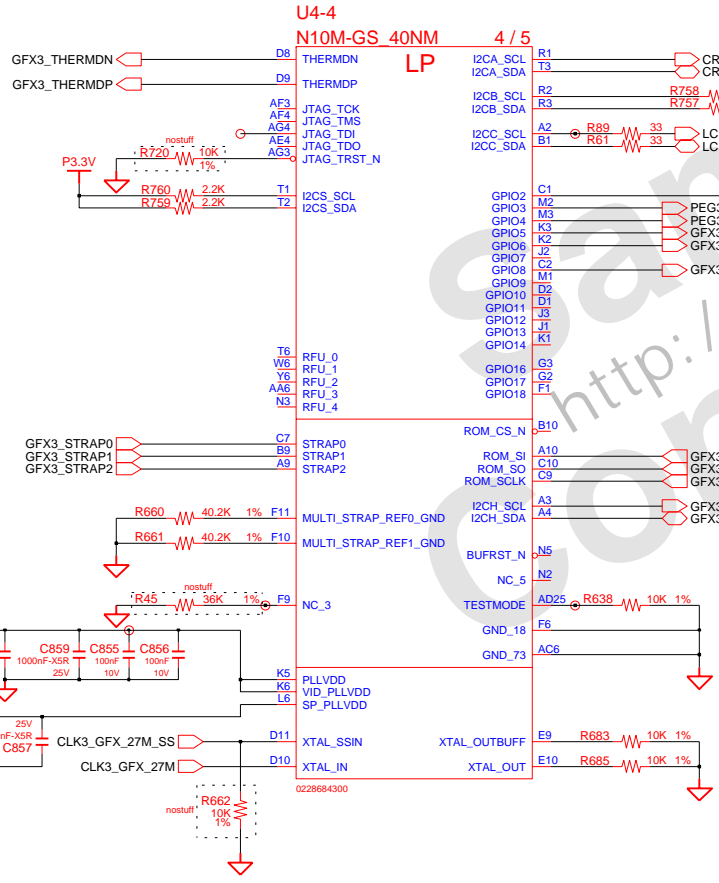
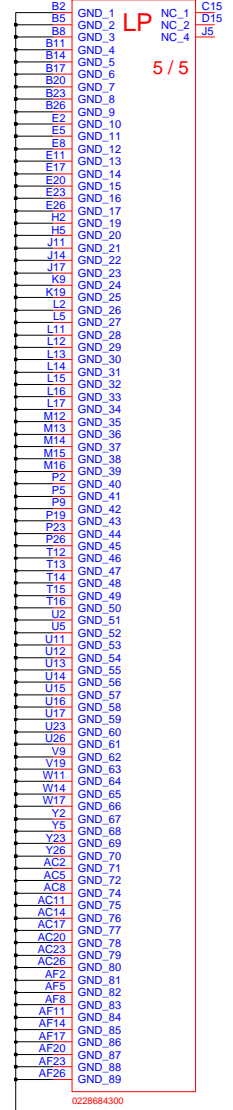
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Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCDD_BL_PWM	High
GPIO(3)	LCDD_VDD	High
GPIO(4)	LCDD_BL_EN	High
GPIO(5)	GPU VID0	00 0.8V
GPIO(6)	GPU VID1	10 0.85V
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK417 = 0.27MHz	
5K ohm	1000	0000	RAM CFG (SEC)	
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit	
15K ohm	1010	0010	USER[3:0]=1111 for EDID	
20K ohm	1011	0011	PADCFG[3:0]=0110 for NB	
25K ohm	1100	0100	N10M-GS:0x0A74	
30K ohm	1101	0101	N10M-GE:0x0A68	
35K ohm	1110	0110	N10M-LP:0x0A69	
45K ohm	1111	0111	N10M-NS:0x0A6C	
			N10M-NE:0x0A6A	
			N10M-GLM:0x0A7C	

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	GFXTYPE
SI	0	1	1	1	1Gb
Strap2	1	0	0	1	N10M-LP DEVICE ID
Strap1	0	1	1	0	For NB
Strap0	1	1	1	1	EDID_EN

U4-5  
 N10M-GS\_40NM



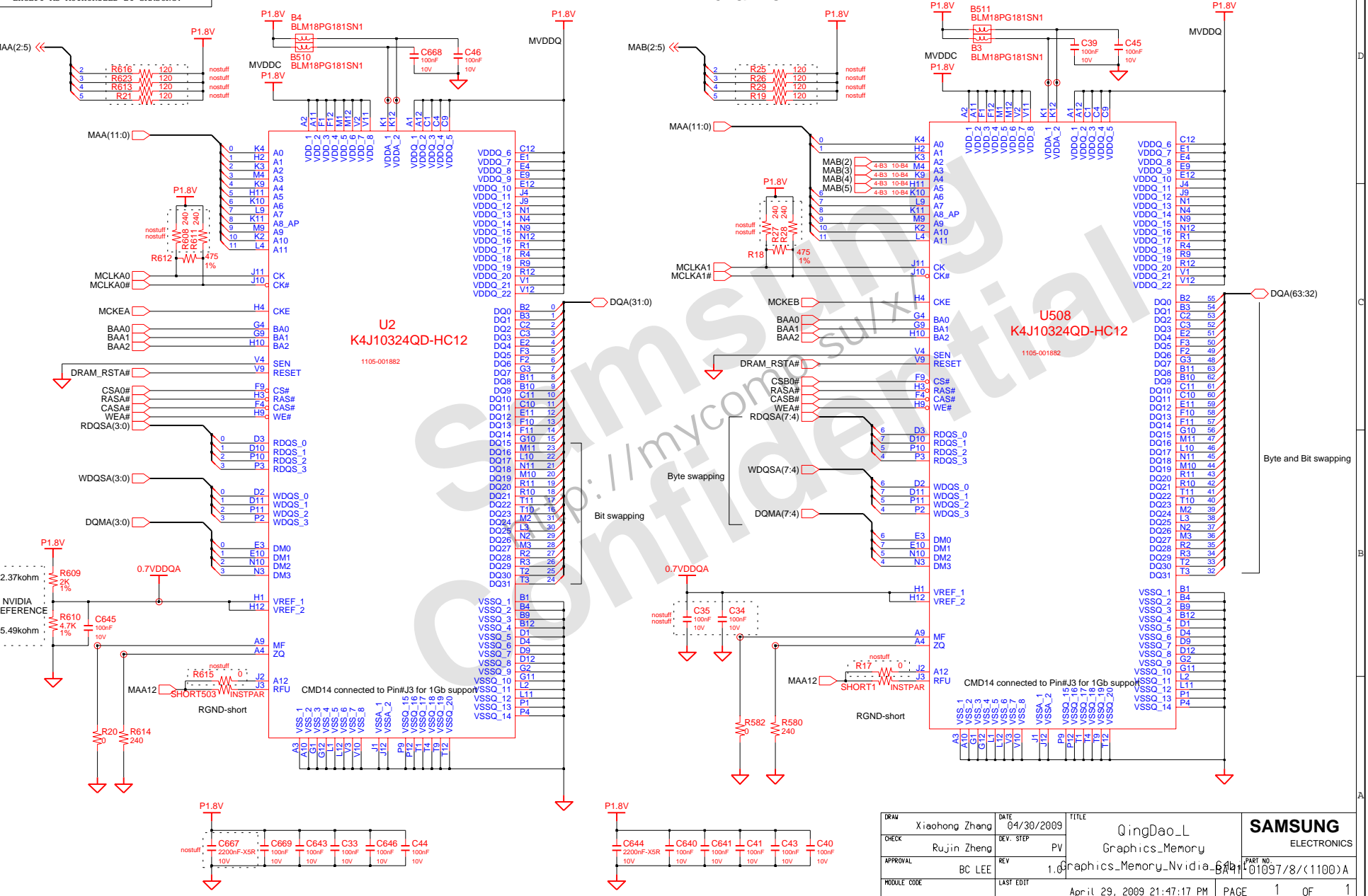
PU is for I2C ROM (AT24C16B, A0-A2 = 000)  
 PD is for Crypto ROM

DRWN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L EXT_NB9X NVIDIA_NB9X_9M	PART NO.	BA11-01097/8/(1100)A
CHECK	Rujin Zheng	REV. STEP	PV				
APPROVAL	BC LEE	REV	1.0				
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM			

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nVidia can support 700MHz, but for N10M\_GE, there only debug 800MHz about VBIOS

**A-channel**



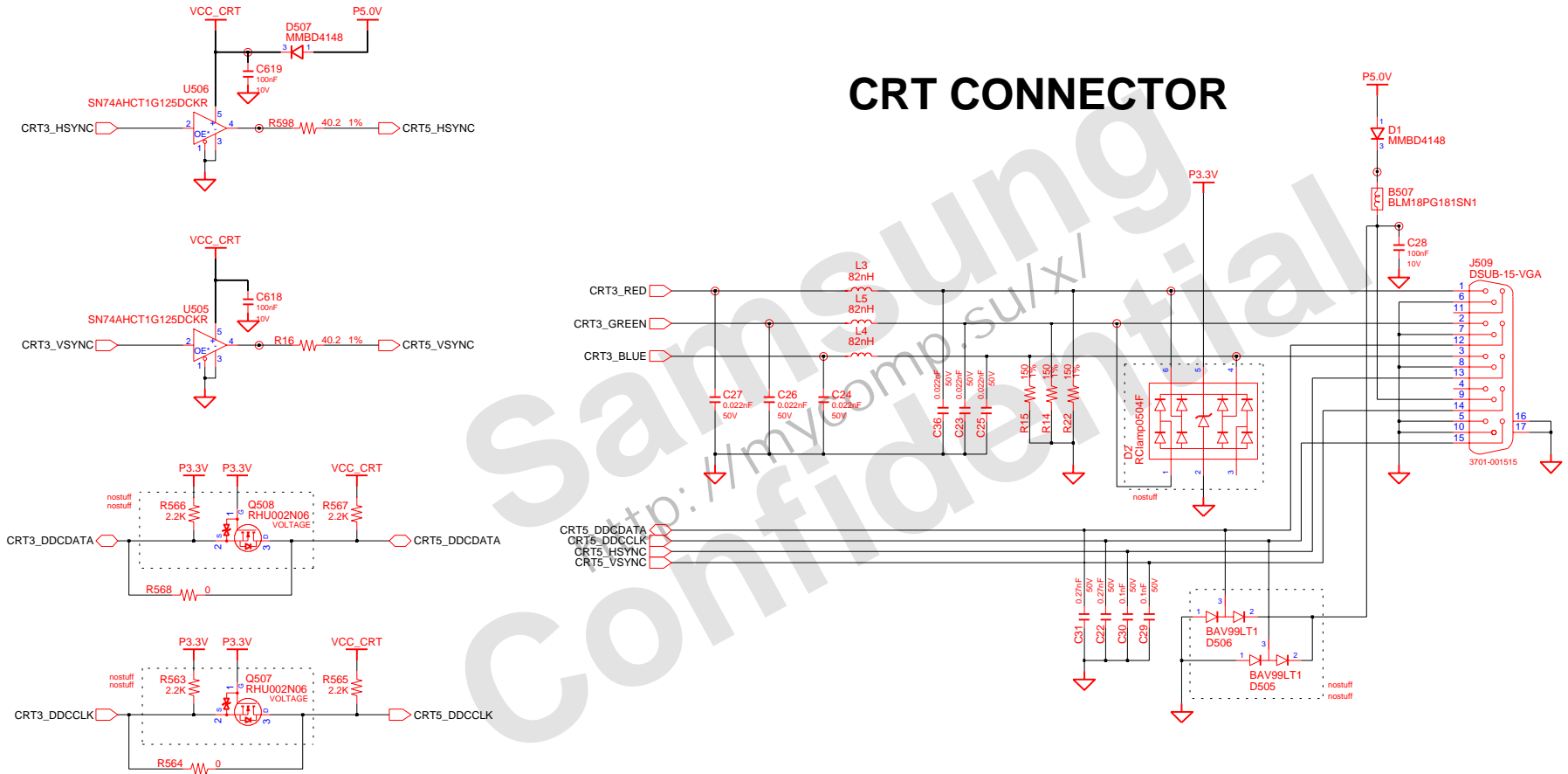
DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	Graphics_Memory		
APPROVAL	BC LEE	REV	1.0	Graphics_Memory_Nvidia_64bit		PART NO. E01097/8/(1100)A
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM		PAGE	1 OF 1



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# CRT

## CRT CONNECTOR

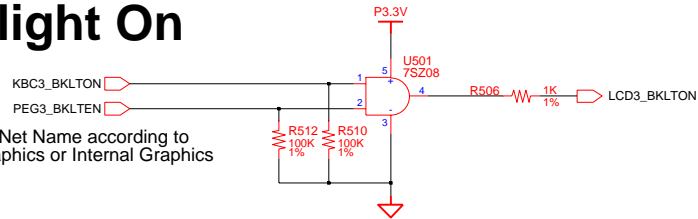


Check "CRT3\_DDCCLK/DATA" Voltage Level  
 2N06 Can be replaced with SM6K2

DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L GRAPHICS_IF CRT	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	BA11-01097/8/(1100)A		
APPROVAL	BC LEE	REV	1.0	April 29, 2009 21:47:17 PM	PAGE	undefined
MODULE CODE		LAST EDIT				

# LVDS

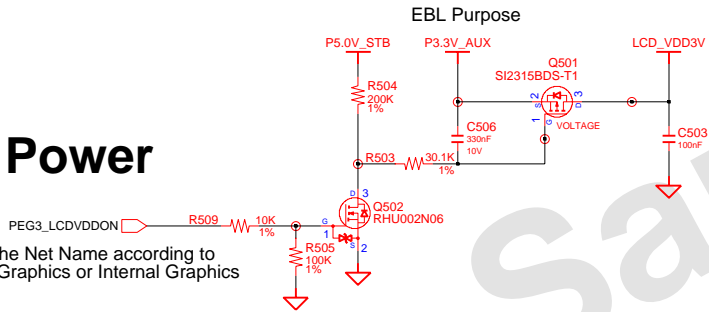
## Backlight On



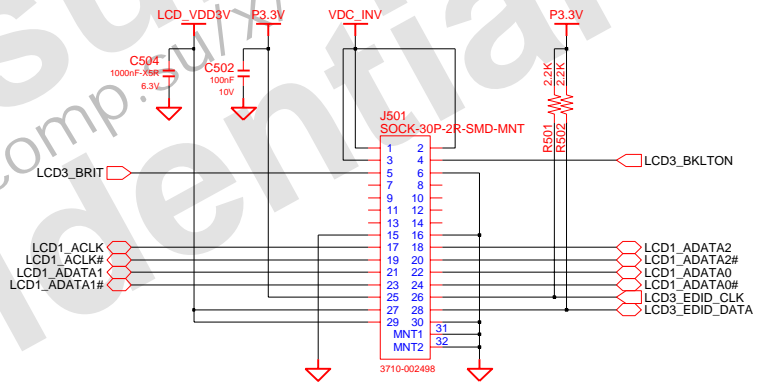
Change the Net Name according to External Graphics or Internal Graphics

## LCD Power

Change the Net Name according to External Graphics or Internal Graphics

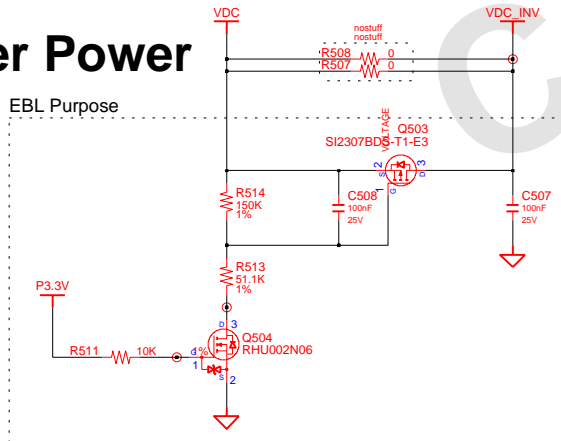


## 1Ch. LCD Connector



## Inverter Power

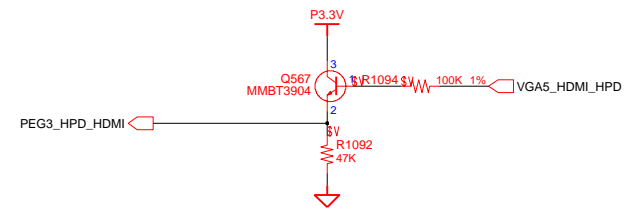
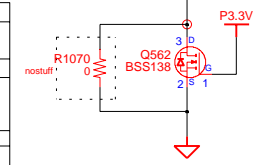
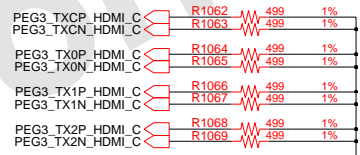
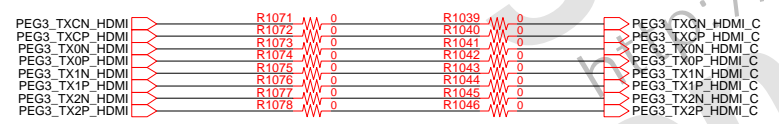
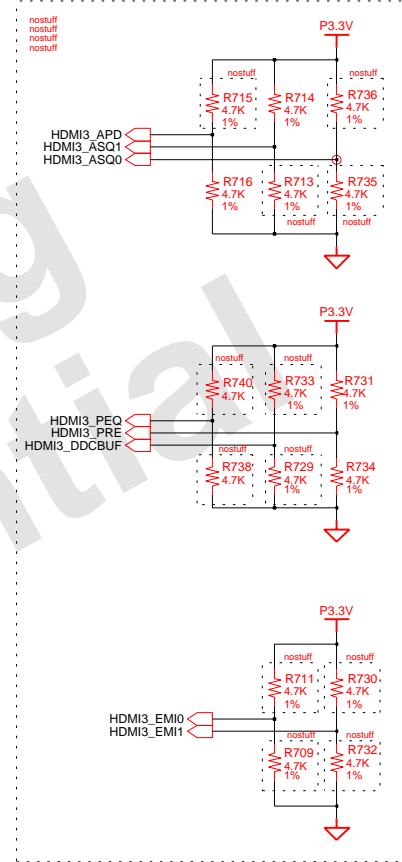
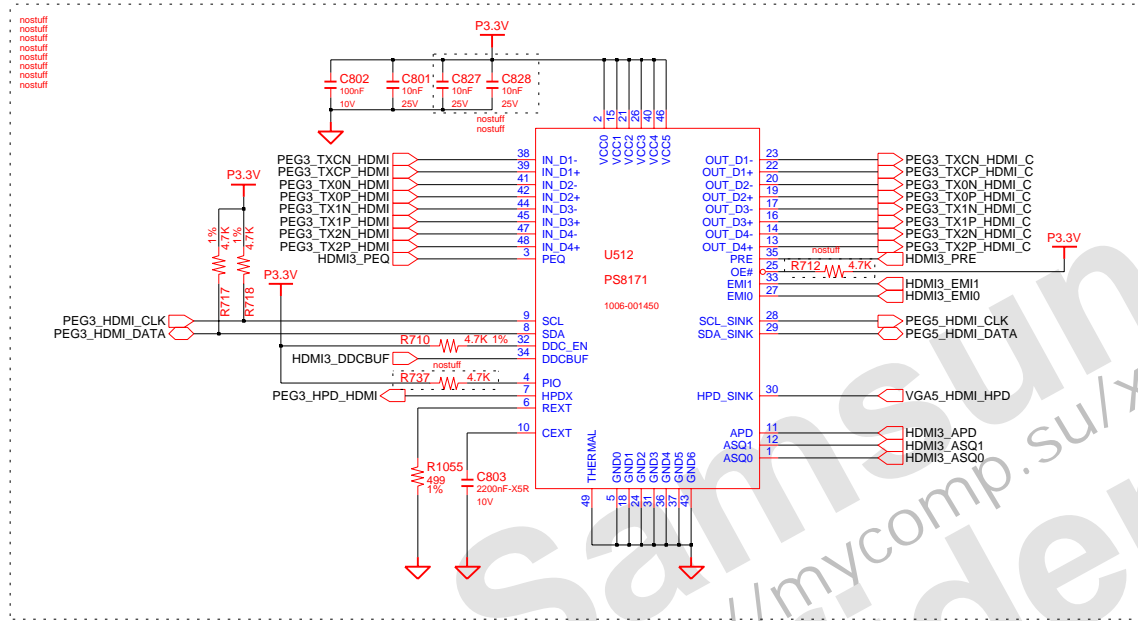
EBL Purpose



DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	GRAPHICS_IF		
APPROVAL	BC LEE	REV	1.0	LCD	BA41-	PART NO. 01097/8/(1100)A
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	2	undofined

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# HDMI Level Shifter(Pre-emp)



APD ASQ0,ASQ1 Same setting as PS8101. Debug in PV stage, then confirm value.

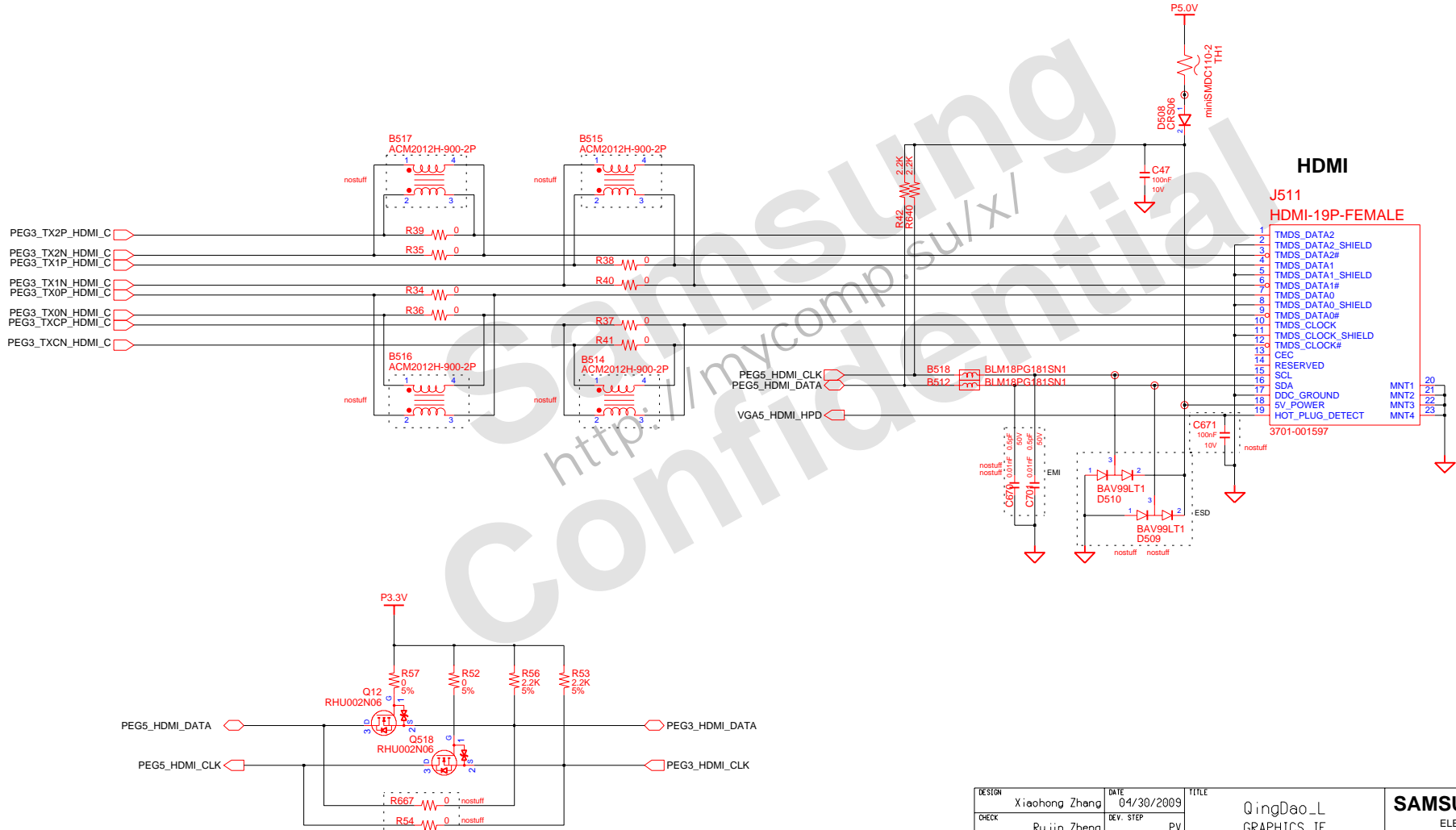
APD	Automatic power down management internal PU: R=500Kohm APD=LOW: Automatic power down disable APD=High: Automatic power down enable APD=MID: Reserved
EMIOEM1	EMI reduction and filter setting EMI1:internal PU: R=500Kohm EMI0:internal PD: R=500Kohm [EMI1,EMIO]=HL: no EMI reduction EMIO=High: Reduced rise/fall time MID: Reduced rise/fall time 2nd EM1=LOW: EMI filter setting 1 MID: Reserved
ASQ0,ASQ1	Automatic squelch function internal PD: R=500Kohm [ASQ1,ASQ0]= HL: No automatic squelch LL: Automatic squelch enable, Level=120mVpp, default timer LH: Automatic squelch enable, Level=100mVpp, default timer HH: Automatic squelch enable, Level=80mVpp, default timer ML: Automatic squelch enable, Level=120mVpp, extended timer MH: Automatic squelch enable, Level=100mVpp, extended timer LM: Automatic squelch enable, Level=80mVpp, extended timer HM: Reserved MM: Reserved

HPDX	Define by PIO PIO=Low: HPD=HPD_SINK @ 3.3V COMS output PIO=High: HPD=HPD_SINK@(inverted HPD) @ 0.9V
PEO	TMDS inputs equalization, internal PD=500Kohm PEO=Low: Mid level EQ (default) PEO=High: High level EQ PEO=MID: Low level EQ
DDCBUF	DDC Active Buffer enable and setting, internal PD=500Kohm DDCBUF=LOW: No DDC active buffer passive DDC level shifter DDCBUF=High: Active DDC buffer enable, setting 1 DDCBUF=MID: Active DDC buffer enable, setting 2
PRE	TMDS output driver pre-emphasis level setting PRE=LOW: No pre-emphasis PRE=High: Low level pre-emphasis is added PRE=MID: High level pre-emphasis is added

DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L GRAPHICS_IF	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	HDMI LEVEL SHIFTER_BA41		
APPROVAL	BC LEE	REV	1.0	PART NO. 01097/8/(1100)A		April 29, 2009 21:47:17 PM PAGE 4 of 4
MODULE CODE		LAST EDIT				

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# HDMI

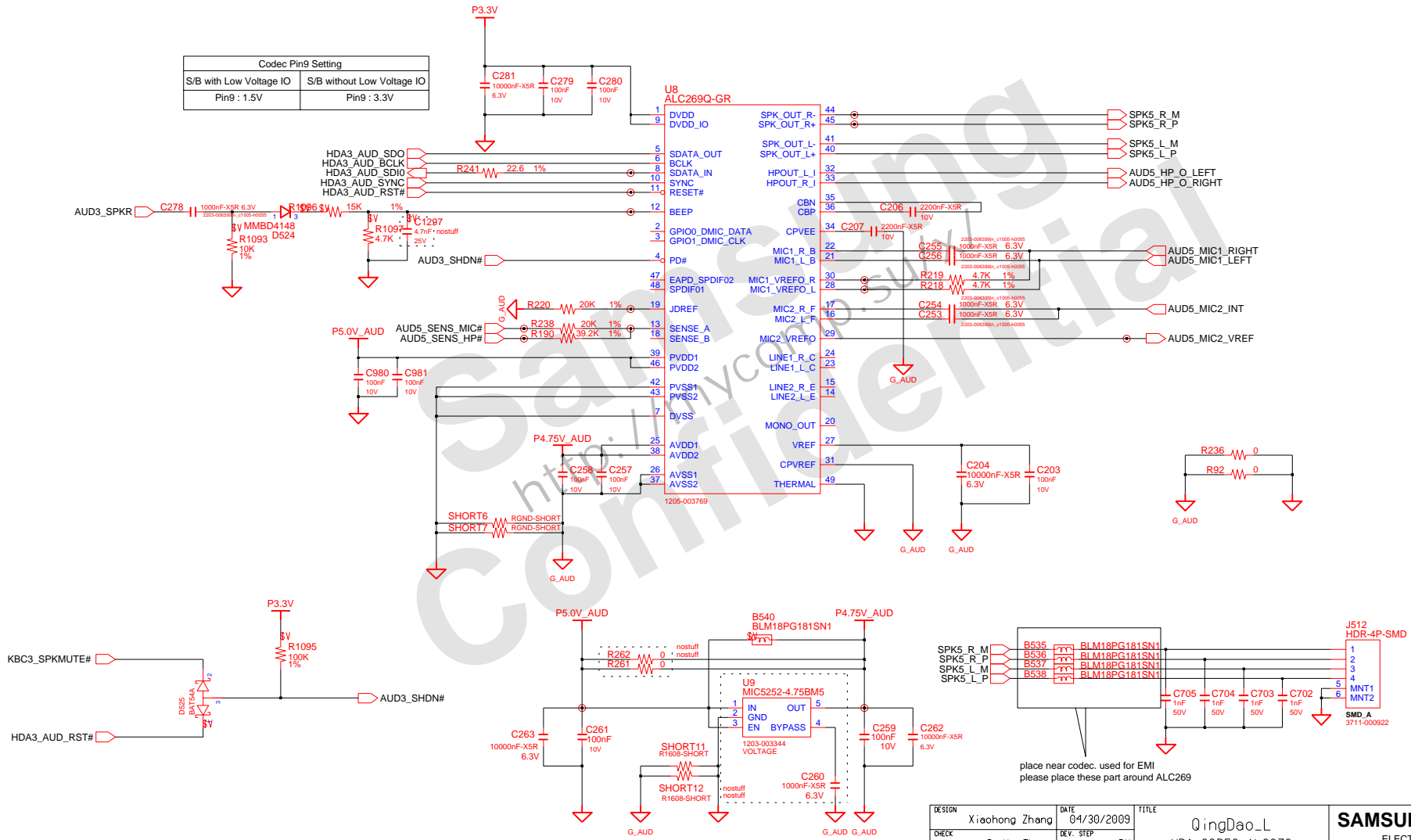


DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L GRAPHICS_IF	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	HDMI	BA41-01097/8/(1100)A	
APPROVAL	BC LEE	REV	1.0	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE 3 of 3
MODULE CODE						undefined

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# AUDIO

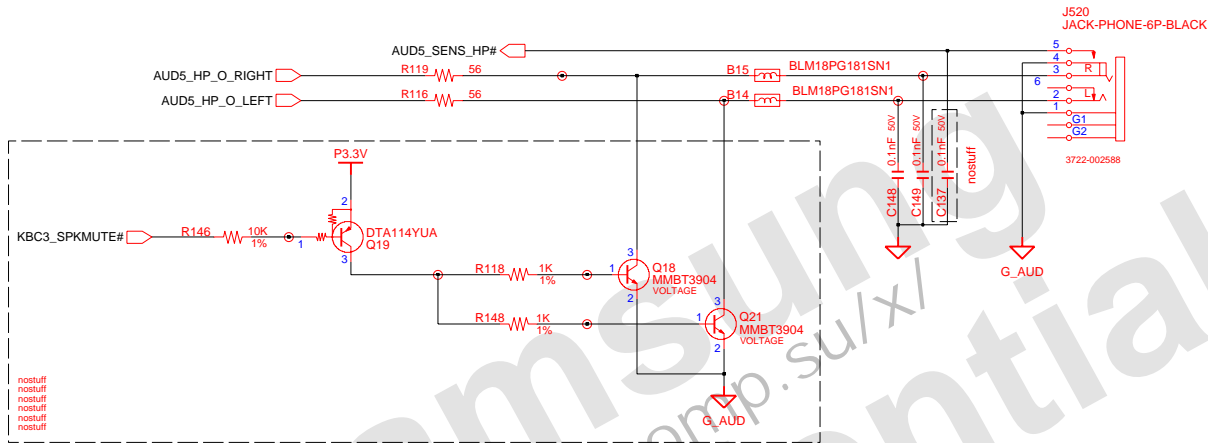
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



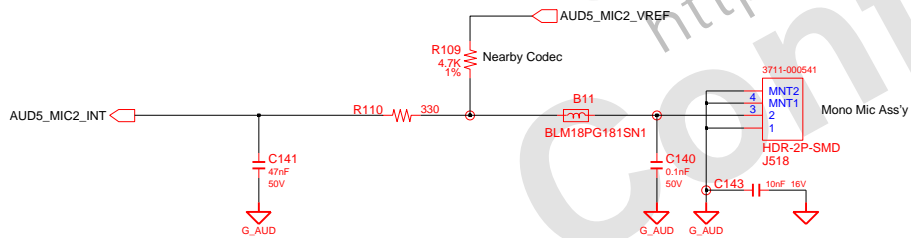
DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS PART NO. HDA_CODEC_ALC272 AUDIO CODEC ALC272BA41-01097/8/(1100)A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM	PAGE 1 OF 5	

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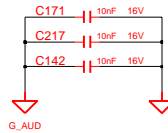
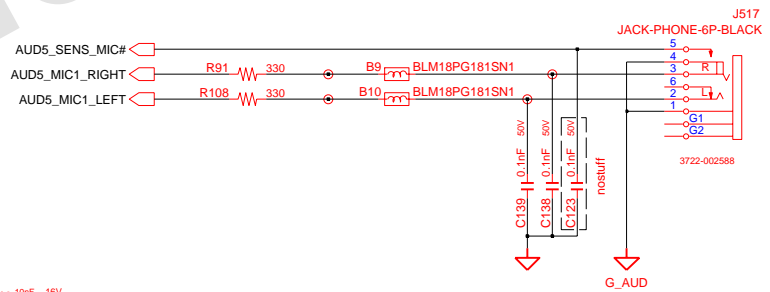
# HEADPHONE



## Analog MIC



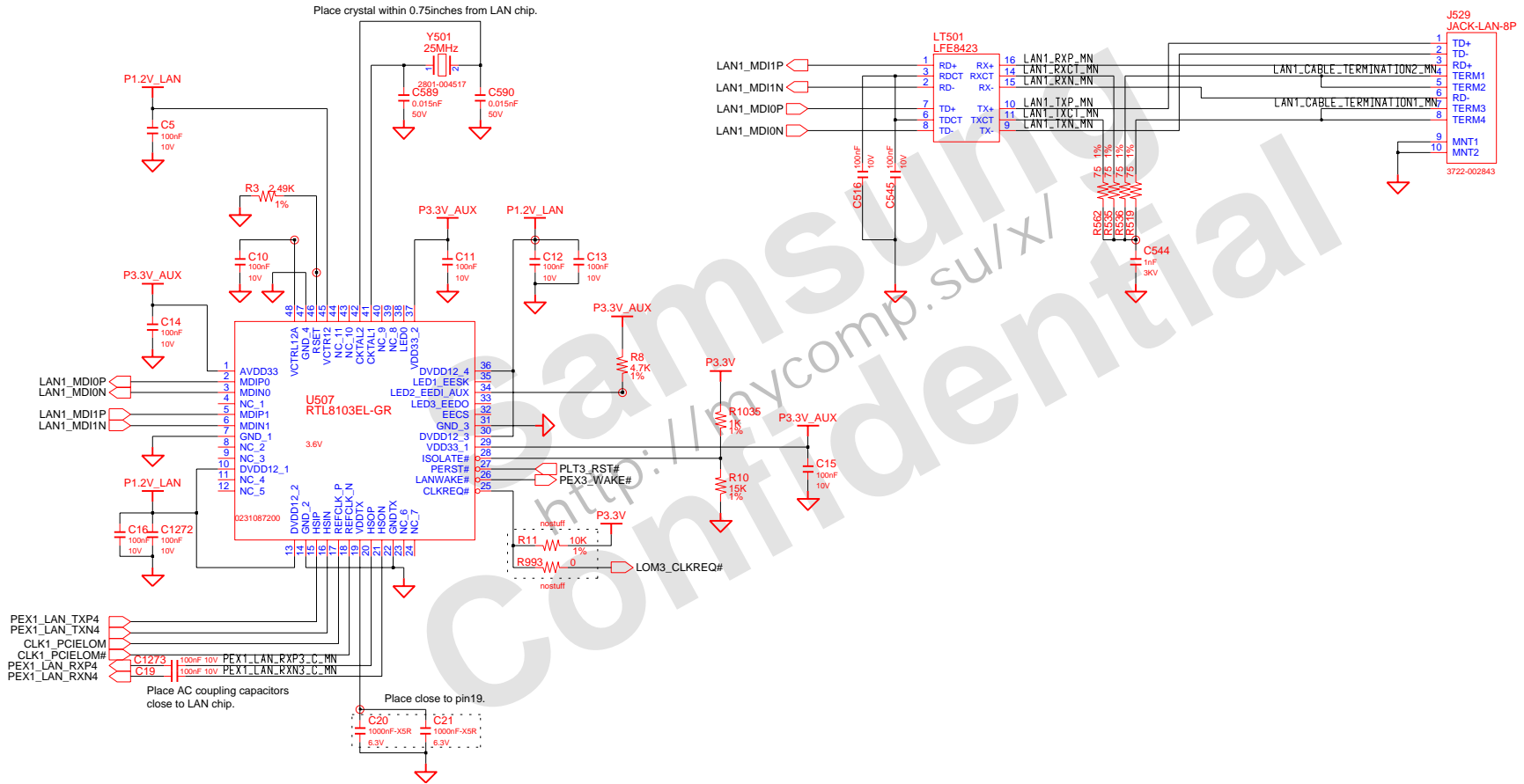
## MIC JACK



DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	HDA_CODEC_ALC272		
APPROVAL	BC LEE	REV	1.0	SPK AMP TPA6017	BA41	PART NO. 01097/8/(1100)A
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	2	OF 5

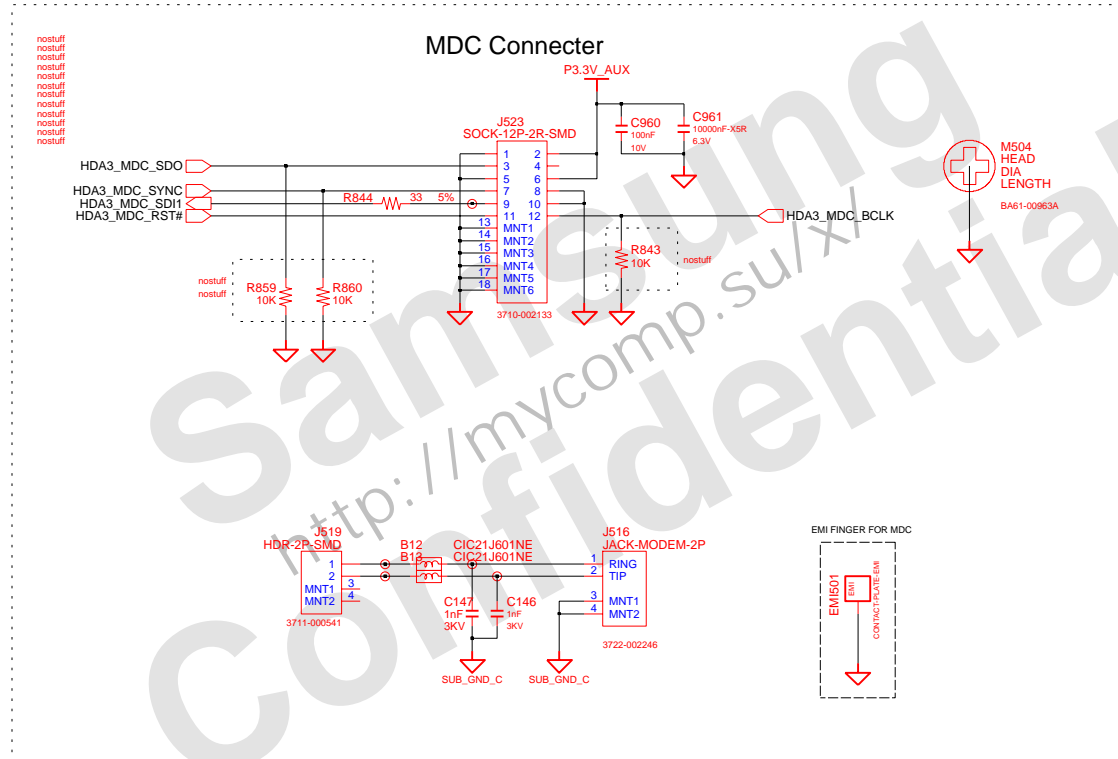
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# LAN



DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	REV. STEP	PV	LAN_MARVELL_8055		
APPROVAL	BC LEE	REV	1.0	LAN		PART NO.
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	BA41-01097/8/((1100)A		undef ined

# MDC



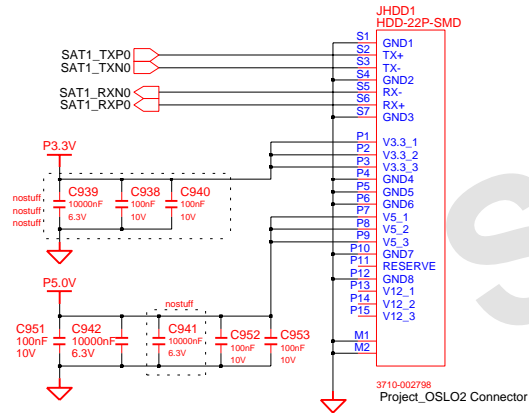
DRAW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		HDA_Modem	
APPROVAL	BC LEE	REV	1.0		HDA_Modem	PART NO. BA41-01097/8/<1100>A
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM	PAGE	1 OF 1



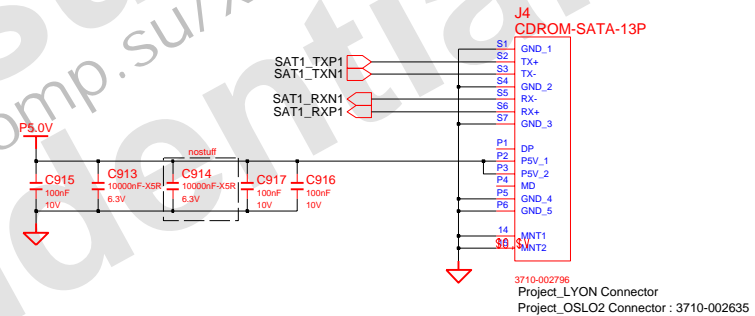
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# SATA I/F CONN

SATA HDD CONN



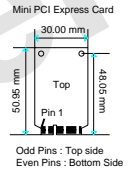
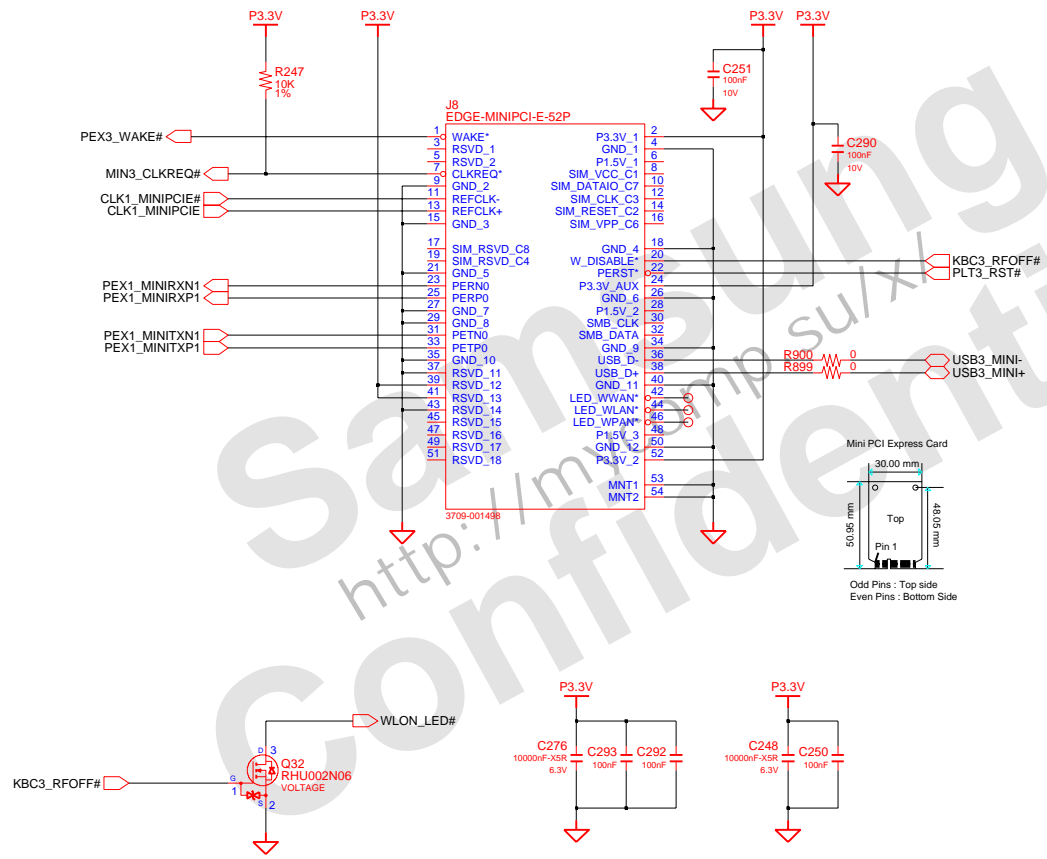
SATA ODD CONN



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<http://mycomp.su/x/>

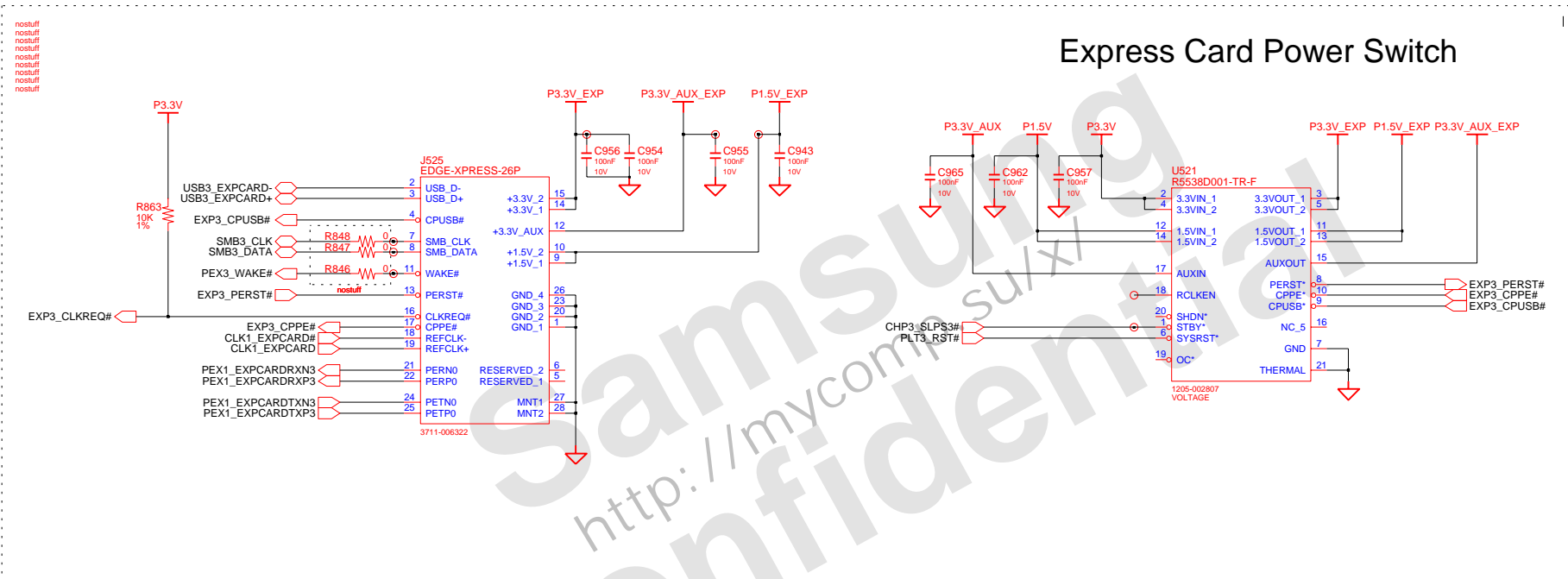
DESIGN	XiaoHong Zheng	DATE	12/3/2008	TITLE	QingDao_Ext SATA_DEVICES HDD ODD	<b>SAMSUNG</b> ELECTRONICS	
CHECK	RuJin Zheng	DEV. STEP	ADV1	PART NO.			BA41-xxxxxA
APPROVAL	BC LEE	REV	1.0	PAGE			1 OF
MODULE CODE	undefined	LAST EDIT	December , 3, 2008 12:06:51 PM				

# WLAN 7mm

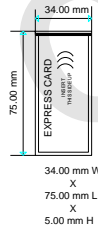


DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L MINI_PCIE_CONN	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	REV	1.0	
APPROVAL	BC LEE	REV	1.0	MODULE CODE	undef ined	PART NO. 01097/8/((1100)A
LAST EDIT				Apr il 29, 2009 21:47:17 PM	PAGE	1 OF

# Express Card

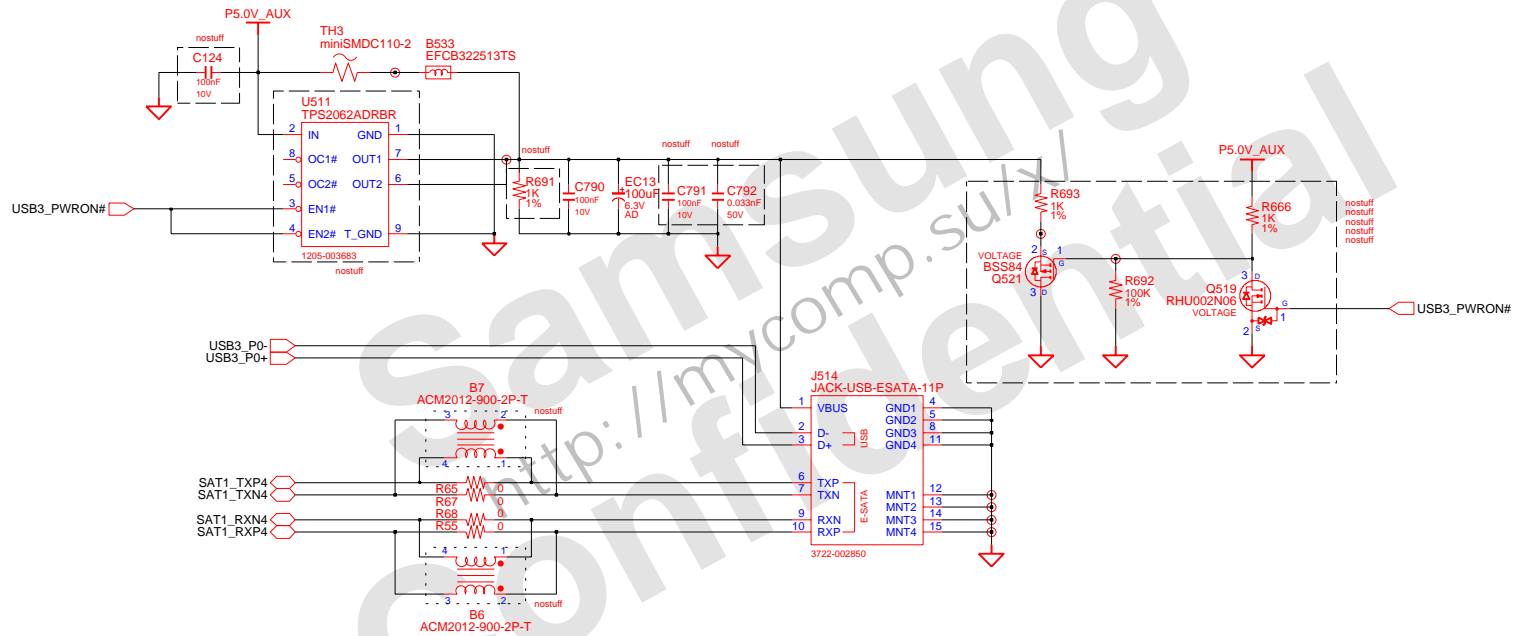


Type 1 module



DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L EXPRESS CARD	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01097/8/(1100)A
MODULE CODE	undefined	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	1	OF

# eSATA

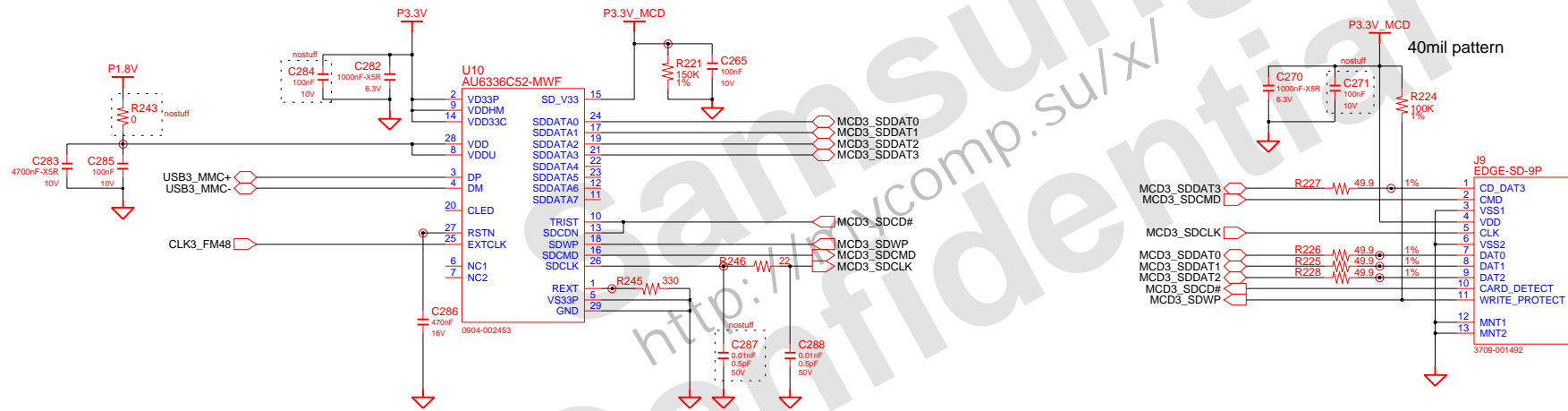


DESIGN	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MAIN		
APPROVAL	BC LEE	REV	1.0	eSATA	BA41-01097/8/(1100)A	PART NO.
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM		PAGE	10 OF 15

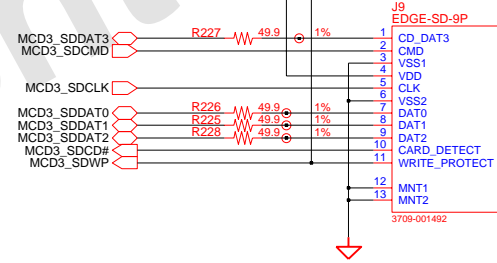
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# 3 IN 1

P3.3V\_MCD distance between R5U880 and socket should be less than 2 inches



40mil pattern



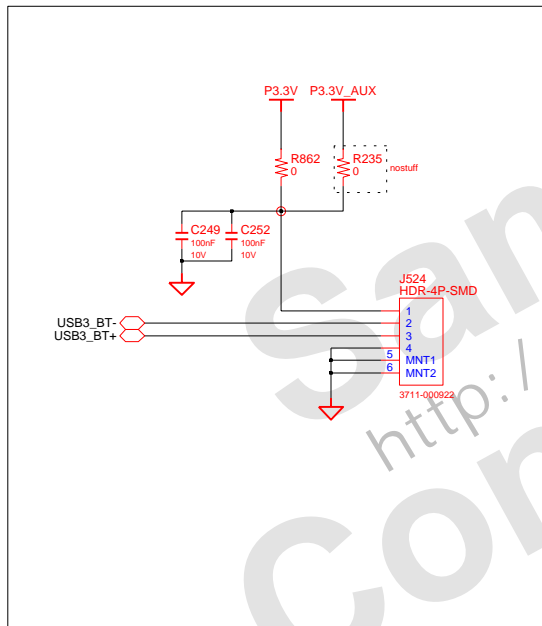
40 mil trace for medica card socket ground

MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable
MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

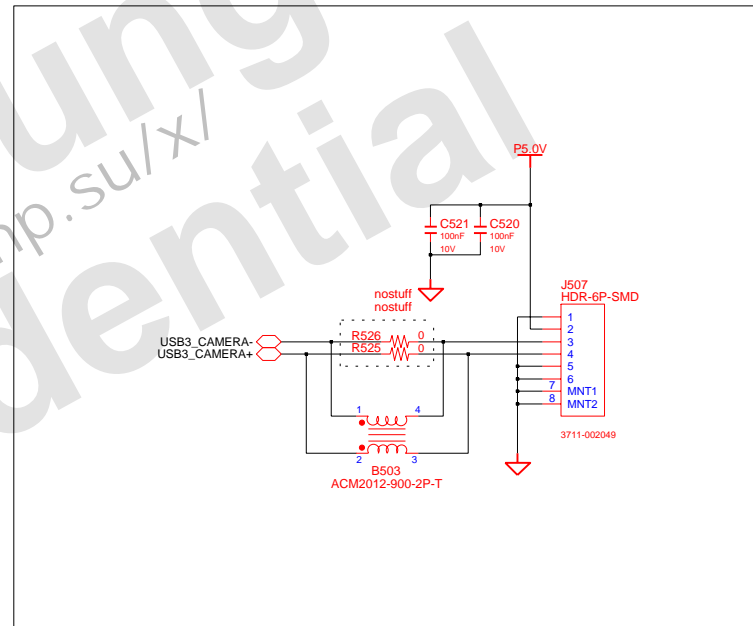
DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L AU6336	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01097/8/(1100)A
MODULE CODE	undef ined	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	1	OF

# USB I/F Devices

## Bluetooth Interface

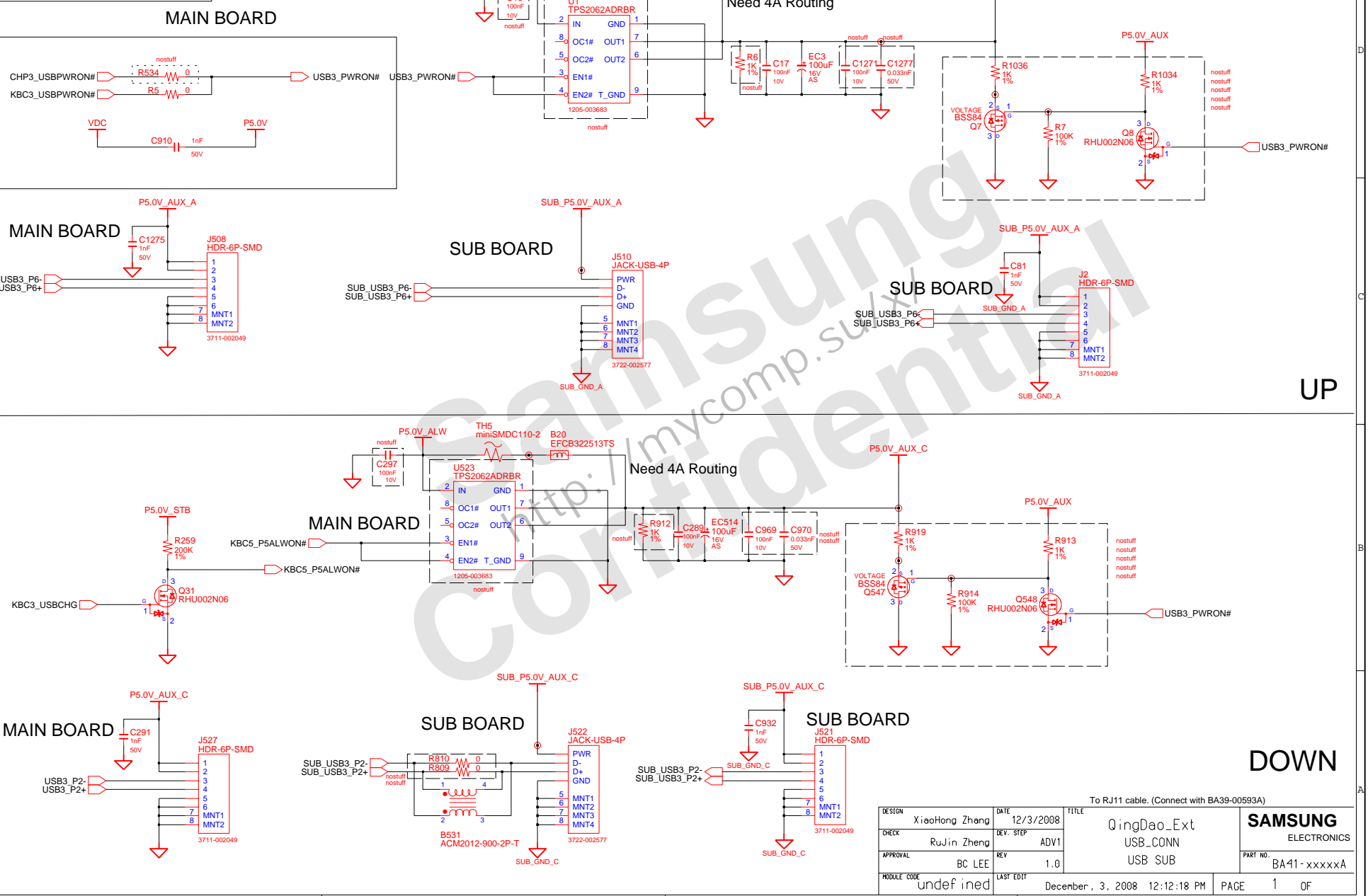


## CAMERA



DESIGN	XiaoHong Zhang	DATE	12/3/2008	TITLE	QingDao_Ext	<b>SAMSUNG</b> ELECTRONICS
CHECK	RuJin Zheng	DEV. STEP	ADV1	USB_DEVICES	BA41-xxxxxA	
APPROVAL	BC LEE	REV	1.0	BT CAMERA	undefined	
MODULE CODE		LAST EDIT	December, 3, 2008 12:12:55 PM	PAGE		

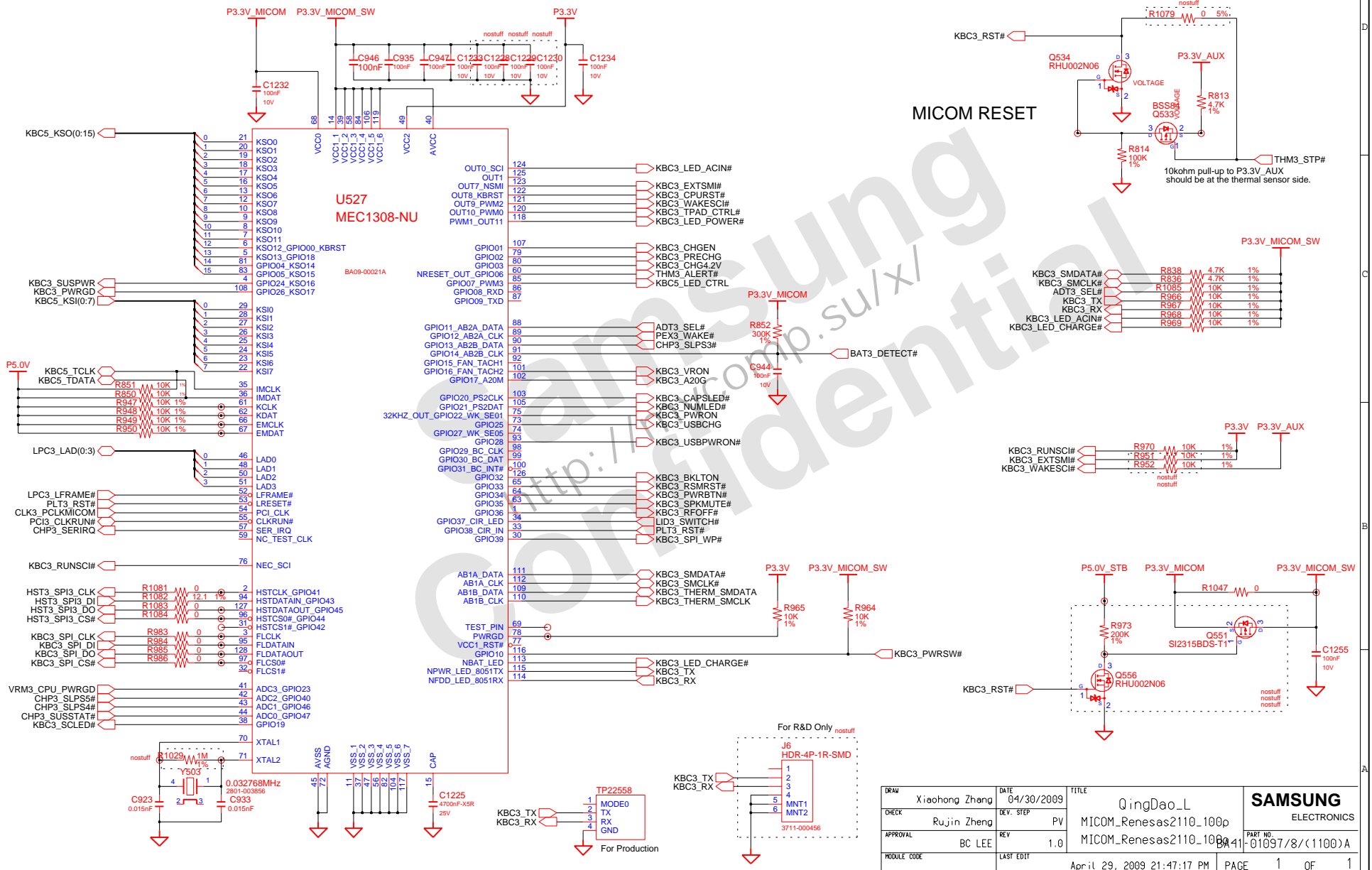
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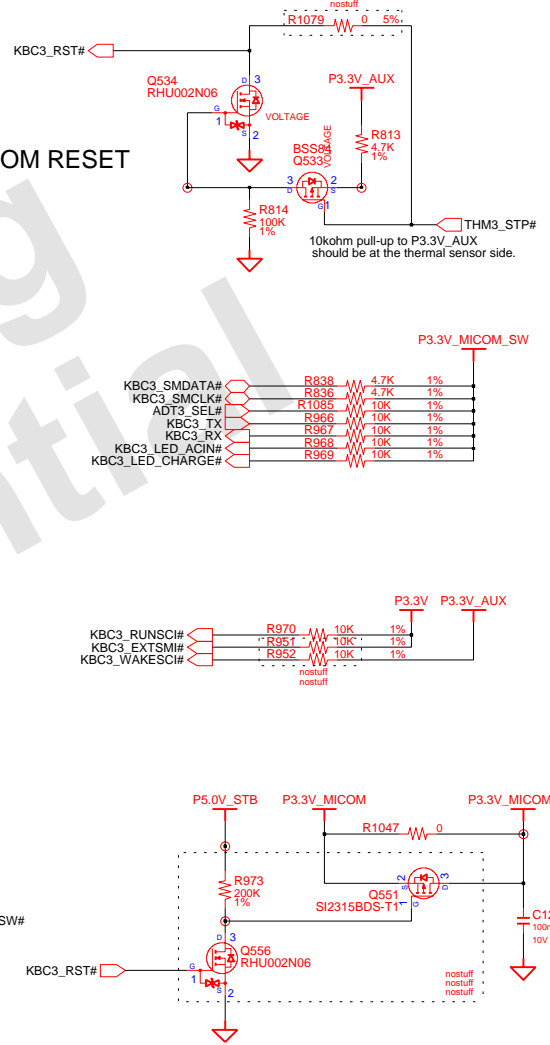
DESIGN	XiaoHong Zhang	DATE	12/3/2008	TITLE	QingDao_Ext USB_CONN USB SUB	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	RuJin Zheng	DEV. STEP	ADV1			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	December, 3, 2008 12:12:18 PM	PAGE	1 OF	

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# MICOM



## MICOM RESET

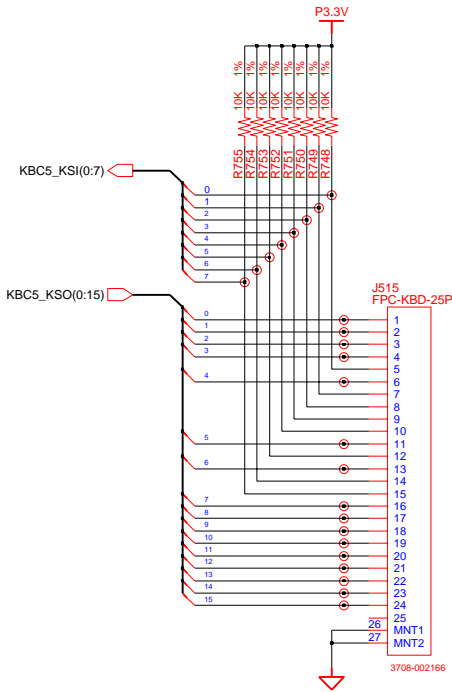


DRW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS PART NO. 01097/8/(1100)A
CHECK	Rujin Zheng	DEV. STEP	PV	MICOM_Renesas2110_100p		
APPROVAL	BC LEE	REV	1.0	MICOM_Renesas2110_100p		
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM			
			PAGE	1	OF 1	

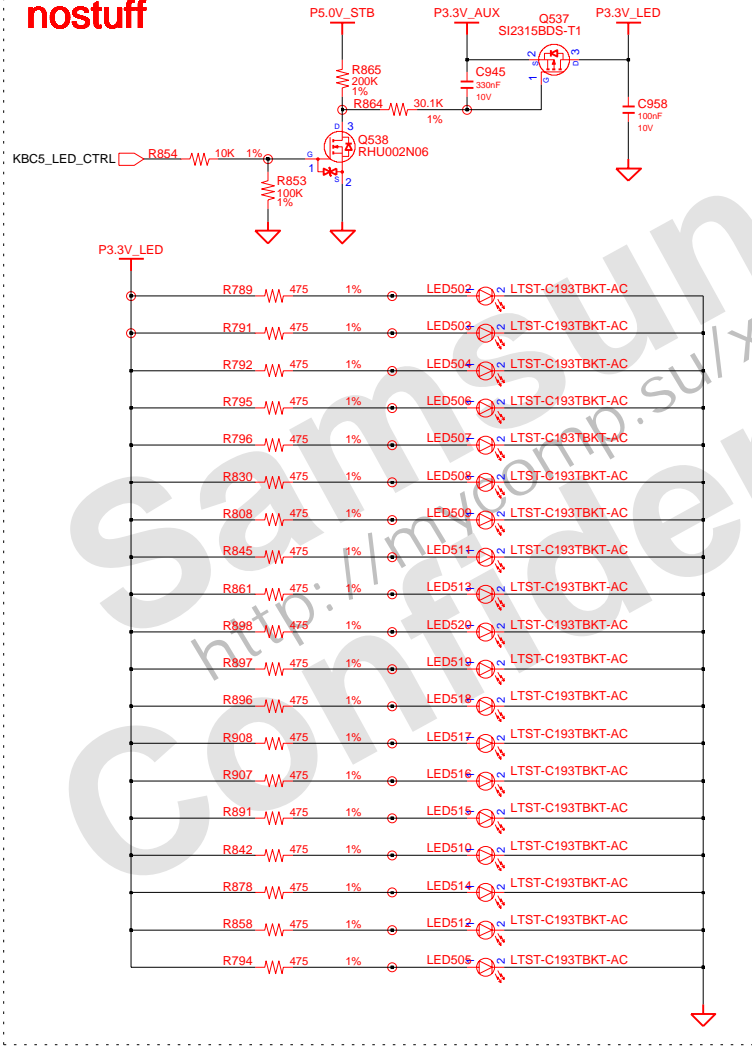


# Micom Glue Logic

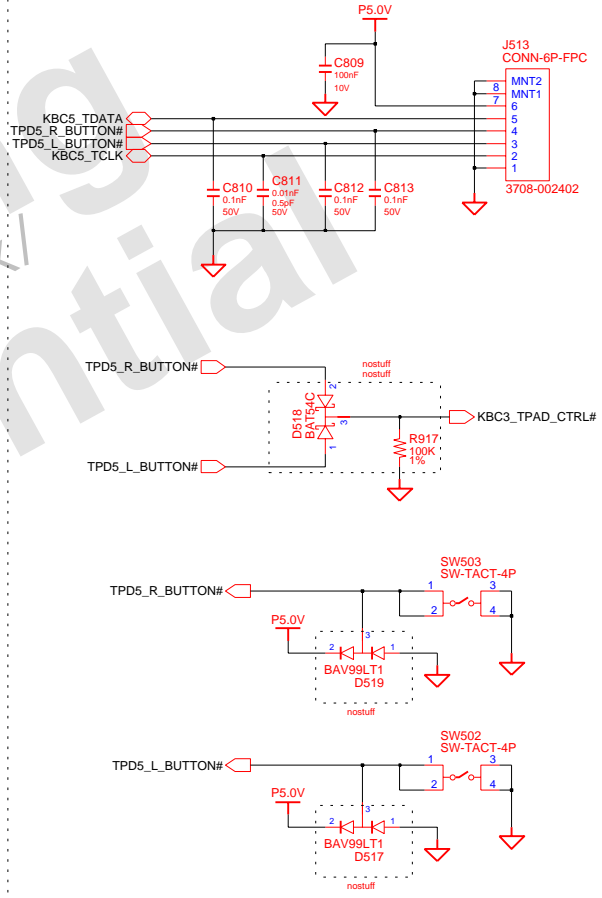
## KEYBOARD



## nostuff



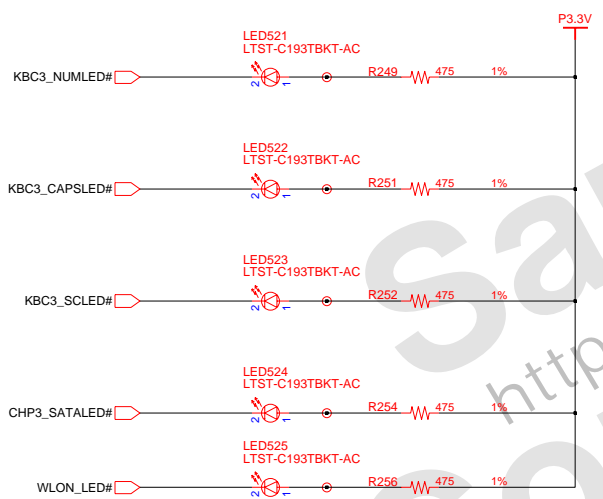
## TOUCHPAD



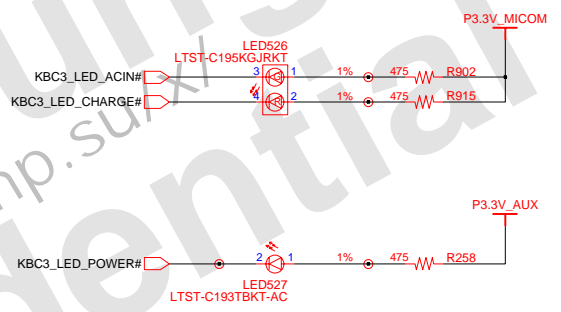
DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MICOM_GLUE_LOGIC		
APPROVAL	BC LEE	REV	1.0	KBD TP	BA41	PART NO. 01097/8/(1100)A
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM	PAGE	undefined

# LED SWITCH LOGIC

## Function Key LEDES



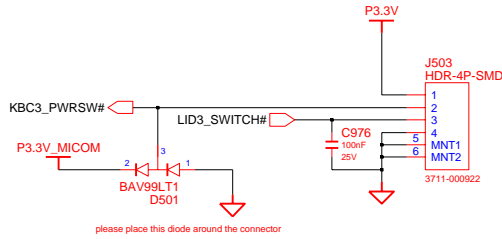
## ADAPTERIN/CHARGING LED



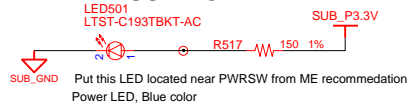
DRW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Rujin Zheng	DEV. STEP	PV	LED_Switch			
APPROVAL	BC LEE	REV	1.0	LED_Switch	BA41-01097/8/(1100)A	PART NO.	
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	1	OF	1

# SUB Board

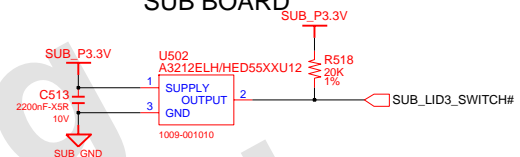
## MAIN BOARD



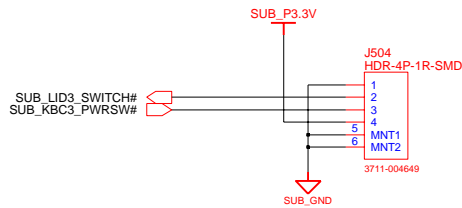
## Power LED SUB BOARD



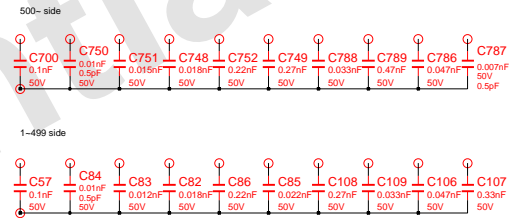
## LID\_SWITCH SUB BOARD



## SUB BOARD



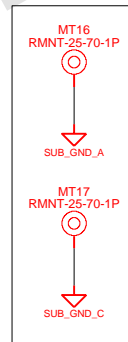
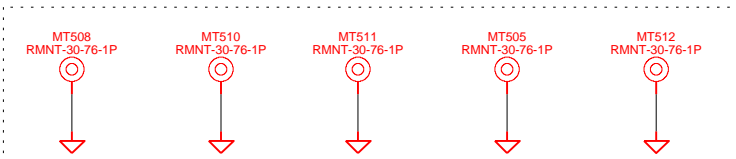
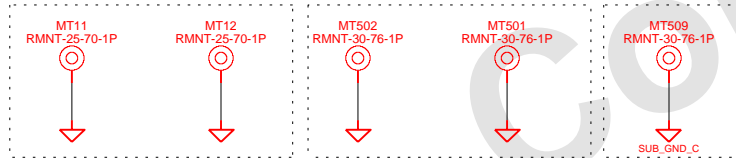
## Power Switch SUB BOARD



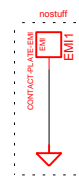
### PCB & BOTTOM

### KBD & BOTTOM

### USB\_SUB & BOTTOM



### USB S/B MT



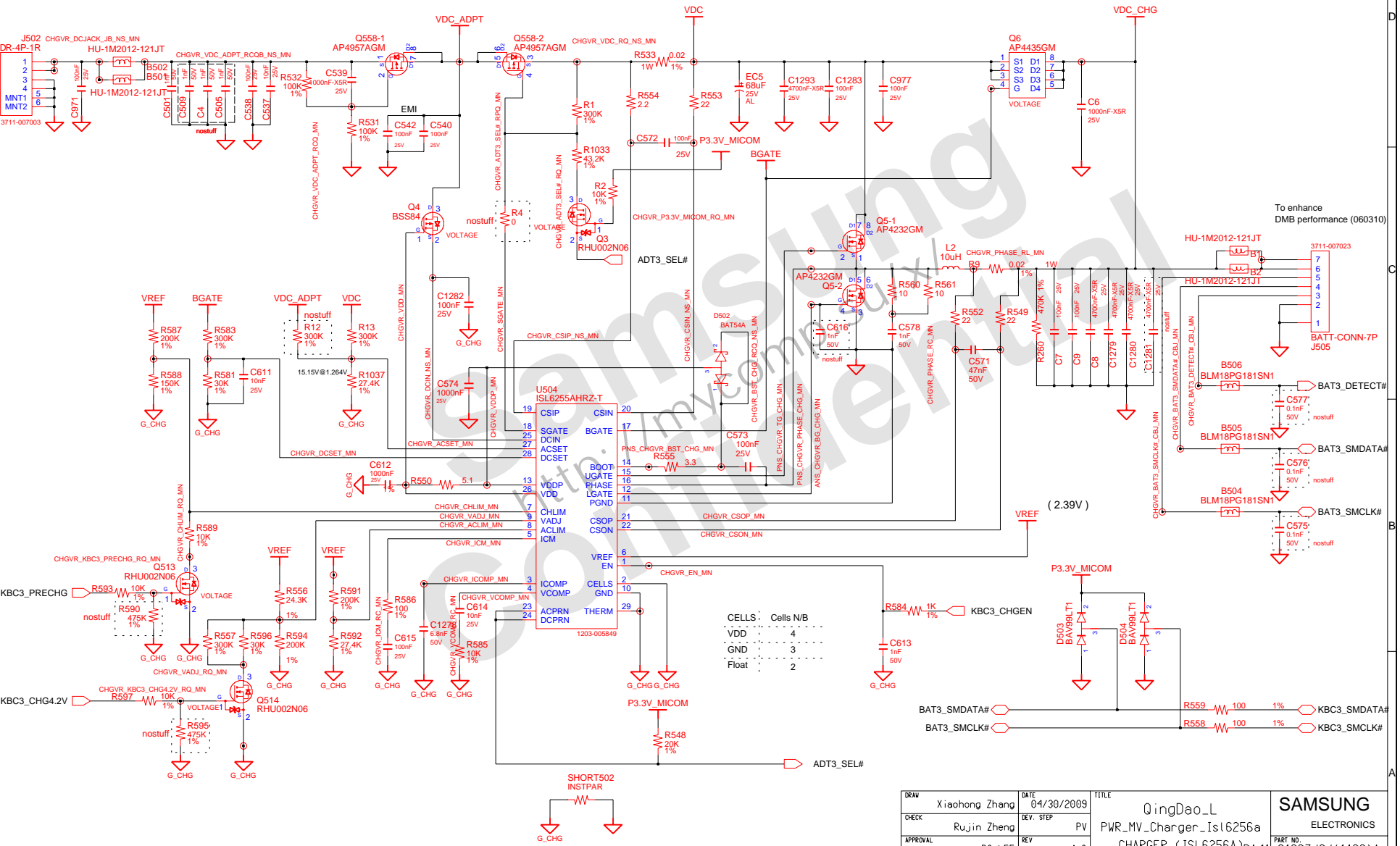
REV1  
 1 0  
 2 0 O3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MAIN		
APPROVAL	BC LEE	REV	1.0	PWR SW SUB	BA41	PART NO. 01097/8/(1100)A
MODULE CODE		LAST EDIT		April 29, 2009 21:47:17 PM	PAGE	11 OF 15

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# CHARGER & POWER MANAGEMENT

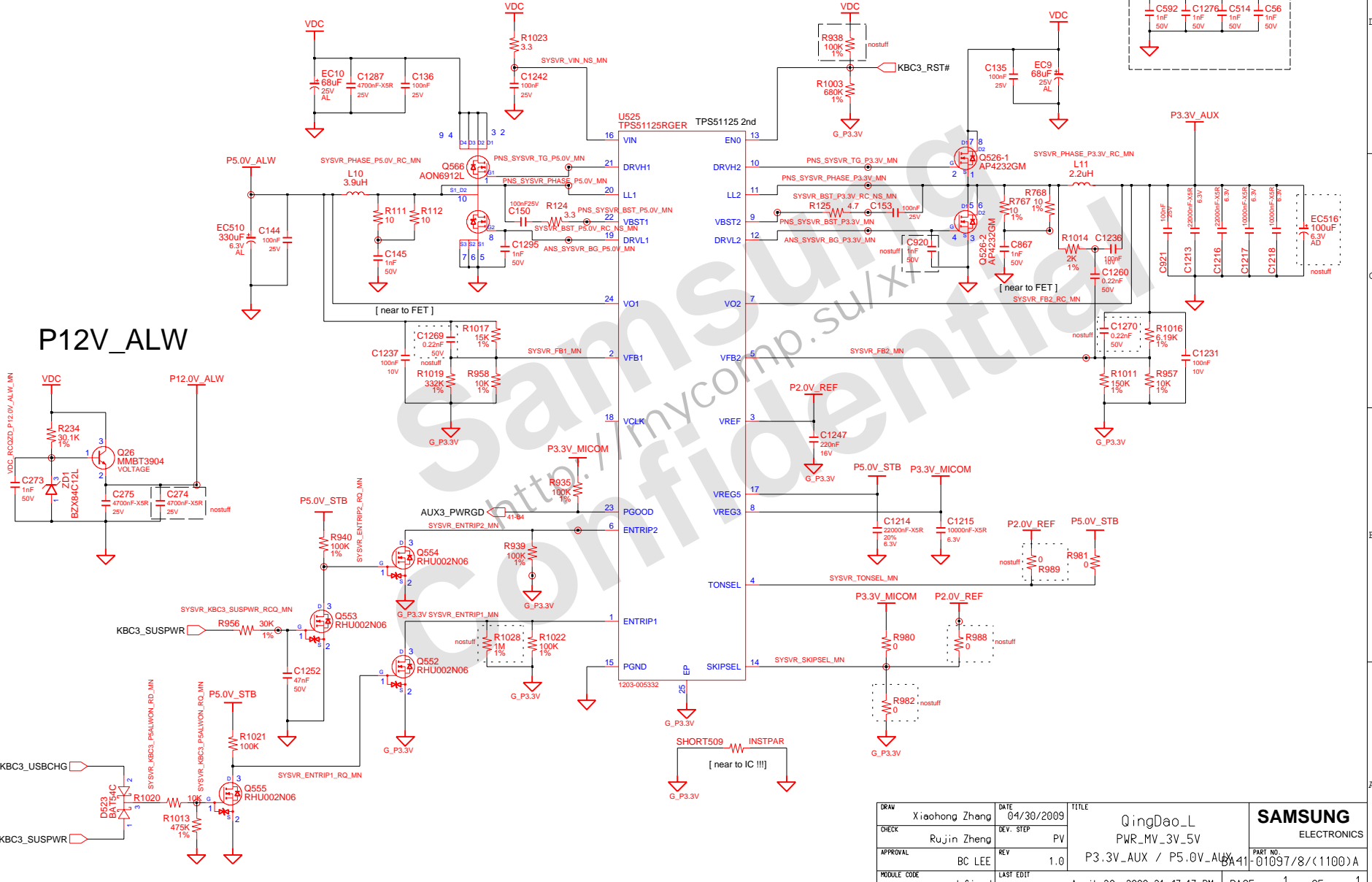
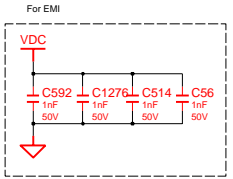


To enhance  
 DMB performance (060310)

DRAW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	REV. STEP	PV	PWR_MV_Charger_Isl6256a		
APPROVAL	BC LEE	REV	1.0	CHARGER (ISL6256A)BA41		PART NO. 01097/8/(1100)A
MODULE CODE	undef ined	LAST EDIT	Apr 12, 2009 21:47:17 PM	PAGE	1	OF 1

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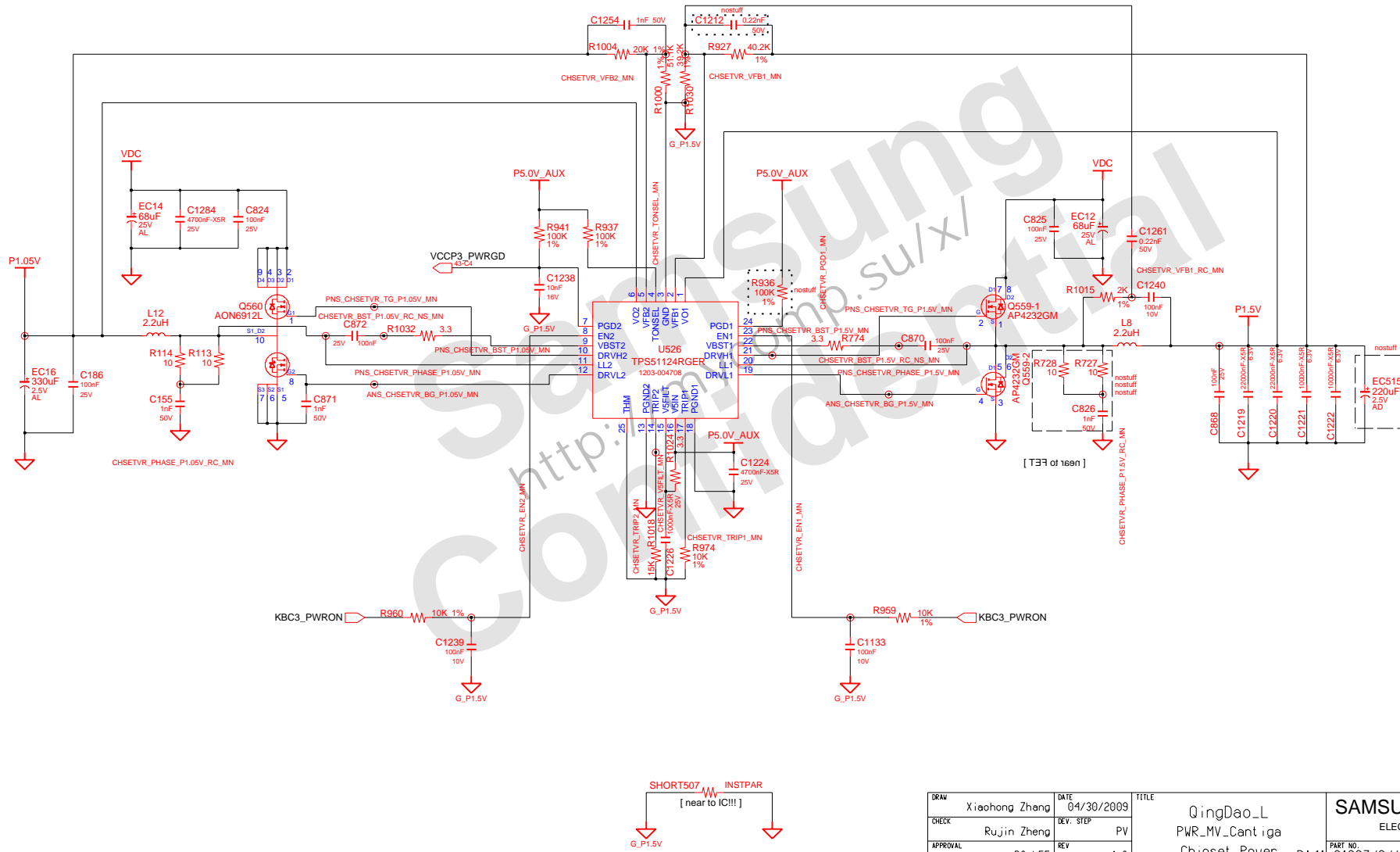
# P3.3V\_AUX & P5.0V\_AUX



## P12V\_ALW

DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_3V_5V	PART NO.	
APPROVAL	BC LEE	REV	1.0	P3.3V_AUX / P5.0V_AUX	01097/8/(1100)A	PAGE 1 OF 1
MODULE CODE	undefined	LAST EDIT	April 29, 2009 21:47:17 PM	BA41-		

# 1.05V & P1.5V

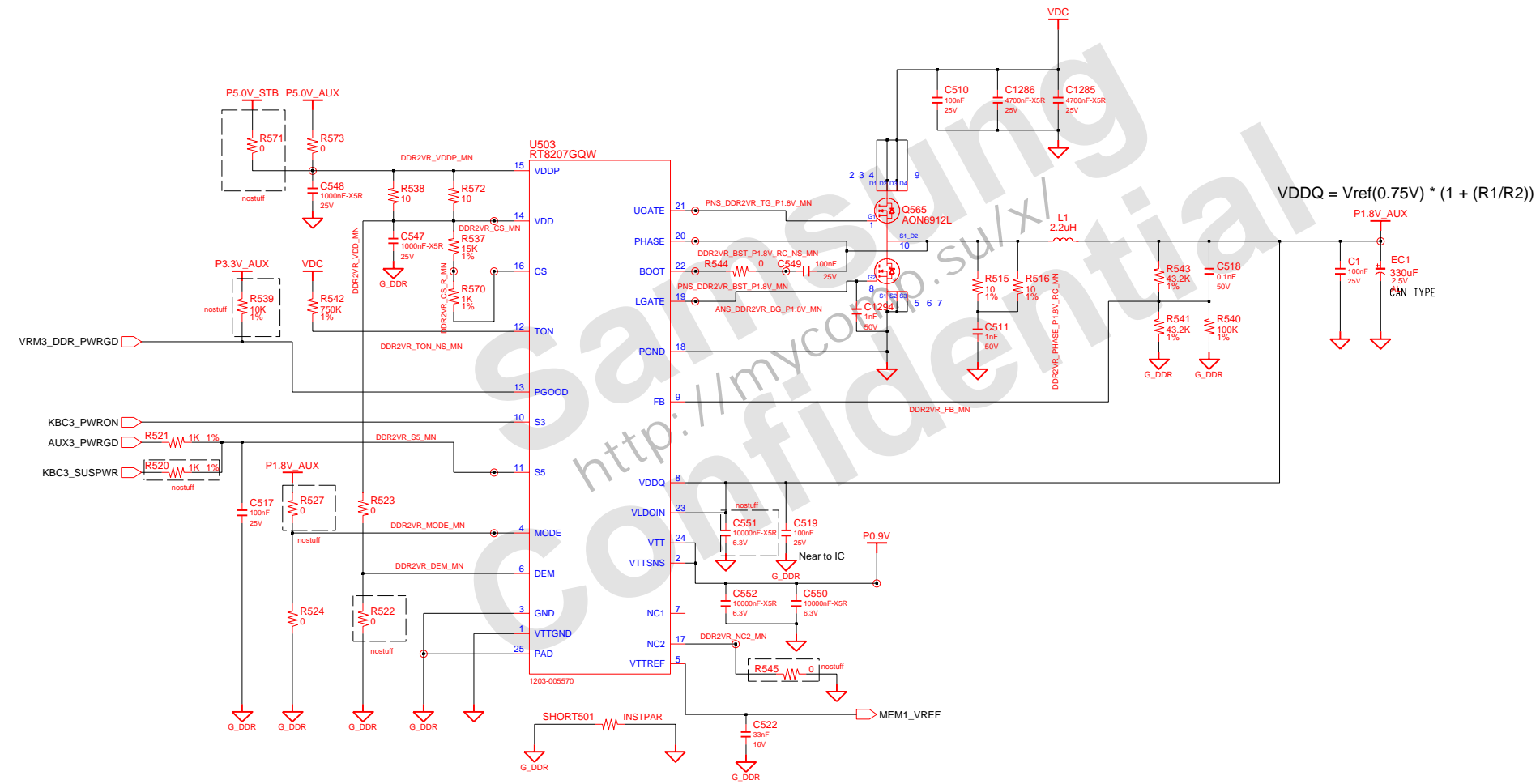


SHORT50Z INSTPAR  
 [near to IC!!!]  
 G\_P1.5V

DRAW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L PWR_MV_Cantiga Chipset Power	<b>SAMSUNG</b> ELECTRONICS PART NO. BA11-01097/8/(1100)A
CHECK	Rujin Zheng	REV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	1 OF 1	

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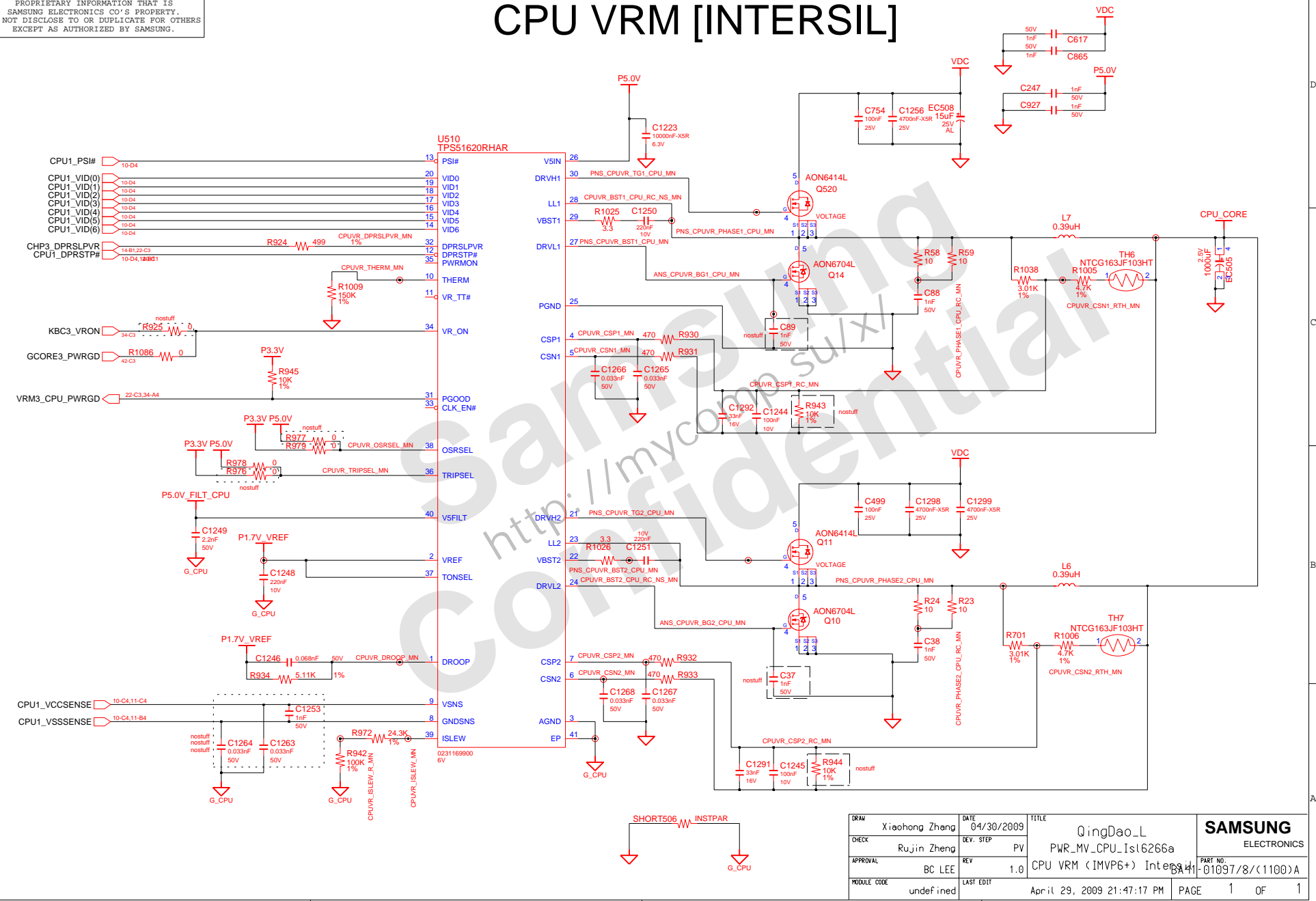
# DDR2 Power



DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_Memory		
APPROVAL	BC LEE	REV	1.0	DDR3 POWER (P1.5V_AUX)A1	PART NO.	01097/8/(1100)A
MODULE CODE	undefined	LAST EDIT		April 29, 2009 21:47:17 PM	PAGE	1 OF 1

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# CPU VRM [INTERSIL]

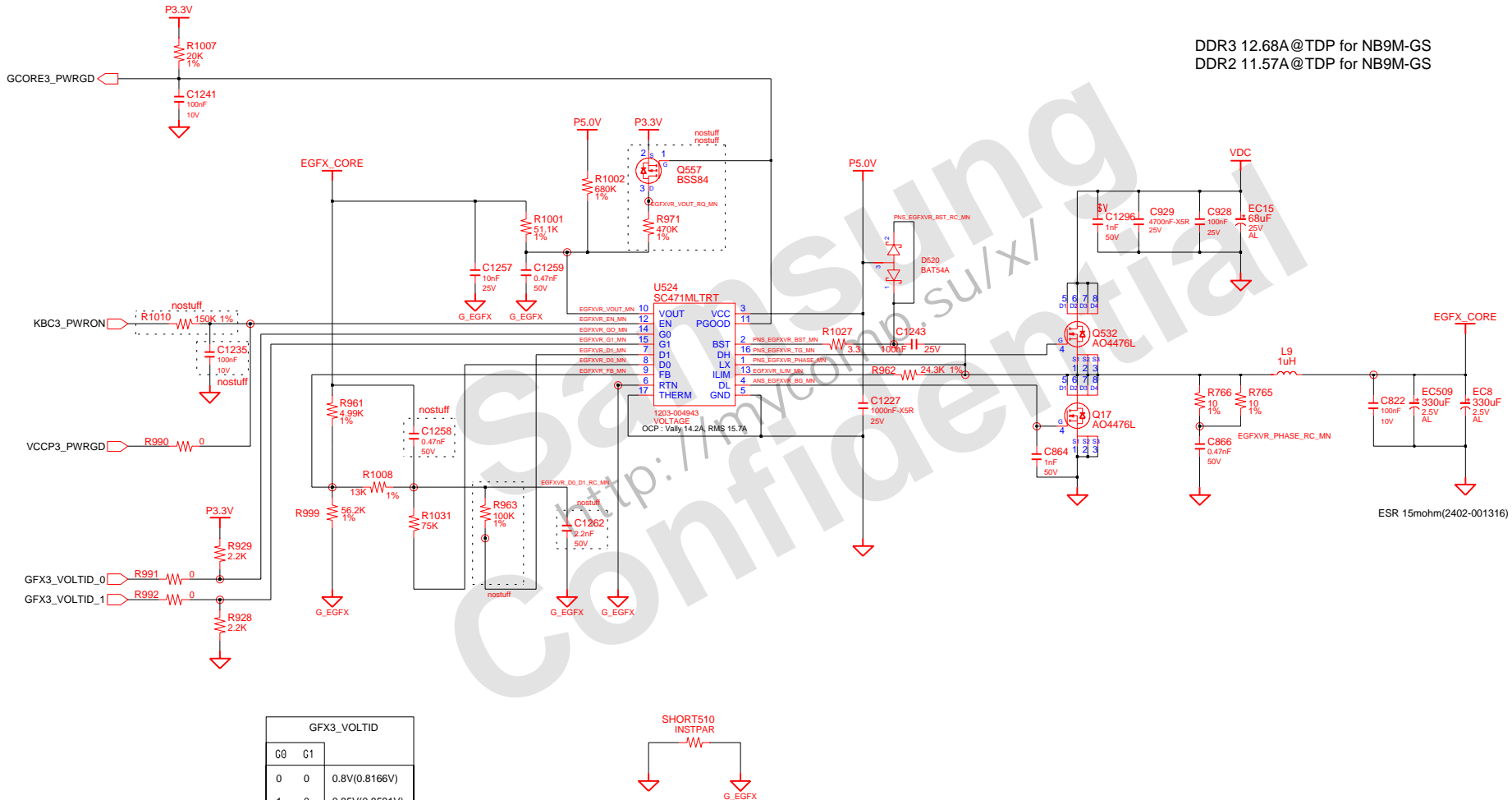


DRAW	DATE	TITLE	<b>SAMSUNG</b> ELECTRONICS
Xiaohong Zheng	04/30/2009	QingDao_L	
CHECK	DEV. STEP	PV	
Rujin Zheng		PWR_MV_CPU_Is16266a	
APPROVAL	REV	1.0	
BC LEE		CPU VRM (IMVP6+) Intersil	
MODULE CODE	LAST EDIT	April 29, 2009 21:47:17 PM	PART NO. 01097/8/(1100)A
undefined			PAGE 1 OF 1

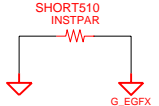


# Graphic Core Power

DDR3 12.68A@TDP for NB9M-GS  
 DDR2 11.57A@TDP for NB9M-GS



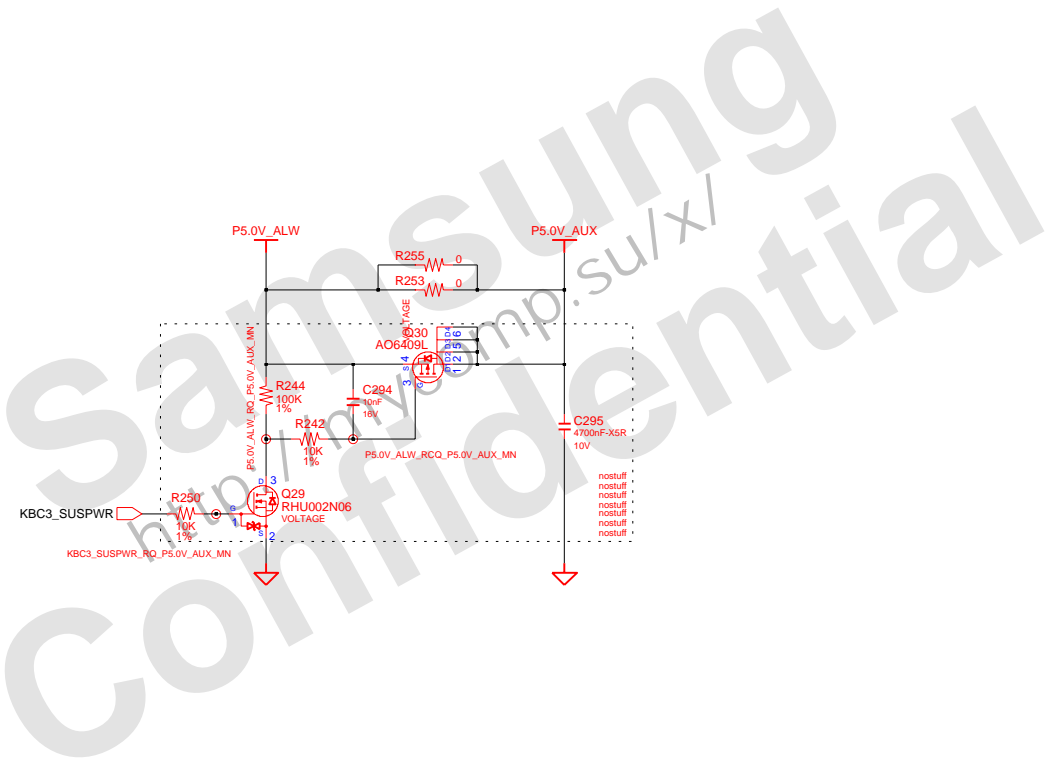
GFX3_VOLTID		
G0	G1	
0	0	0.8V(0.8166V)
1	0	0.85V(0.8591V)
0	1	RESERVE
1	1	RESERVE



DRW	Xiaohong Zhang	DATE	04/30/2009	TITLE	QingDao_L	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_Gfx_MV_Ext		
APPROVAL	BC LEE	REV	1.0	Ext Gfx Memory(SC486)		PART NO.
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	PAGE		1 OF 1

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# Switched Power

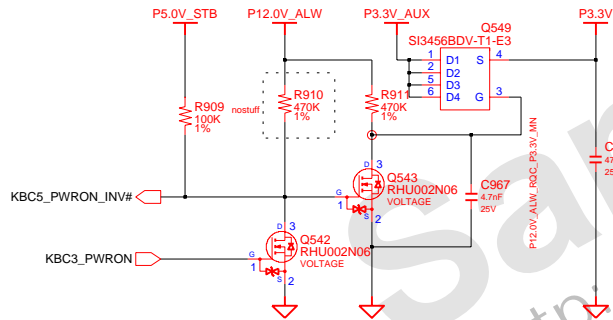


DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_Switched		
APPROVAL	BC LEE	REV	1.0	SWITCHED POWER	BA41-	PART NO. 01097/8/(1100)A
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM		PAGE	1 OF 2

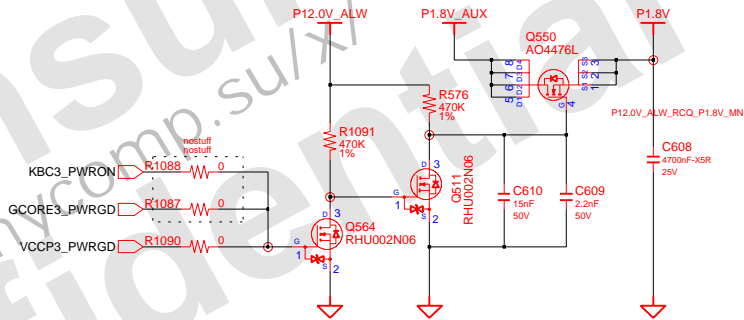
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# Switched Power

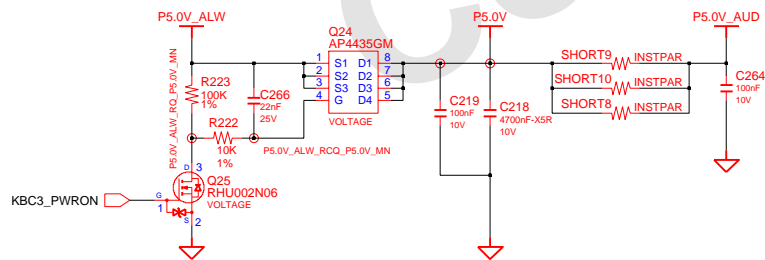
Switched Power On (P3.3V)



Switched Power On (P1.8V)

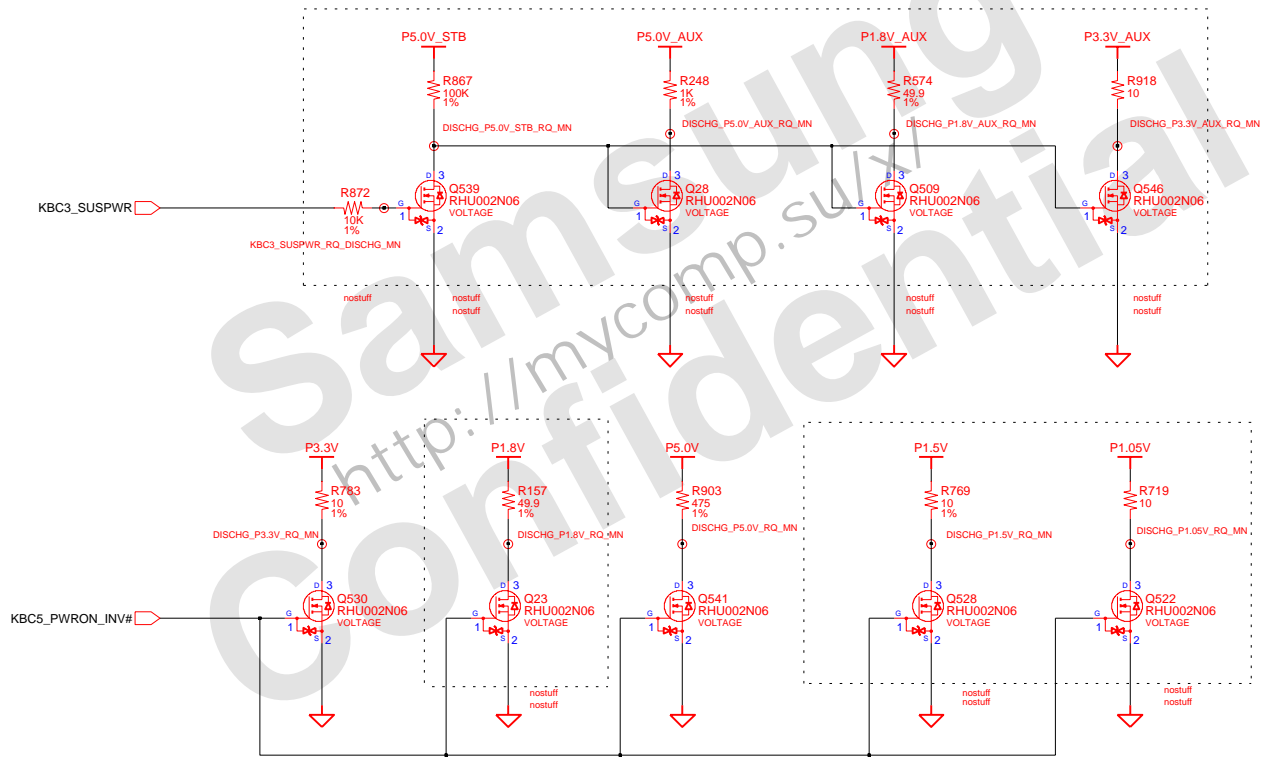


Switched Power On (P5.0V)



DESIGN	XIAOHONG, ZHANG	DATE	12/3/2008	TITLE	QingDao_Ext PWR_MV_SWITCHED Switched Power	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	RUJIN, ZHENG	DEV. STEP	ADV1			
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT				
				December, 3, 2008 3:39:16 PM	PAGE	2 OF

# POWER DISCHARGER



DRAW	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_DisCharger		
APPROVAL	BC LEE	REV	1.0	DISCHARGING LOGIC BA41		PART NO. 01097/8/(1100)A
MODULE CODE	undefined	LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	1	OF 1

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- CPU1\_NMI
- CPU1\_TCK
- CPU1\_TDI
- CPU1\_TMS
- FANS\_VDD
- SMB3\_CLK
- ADT3\_SEL#
- CLK3\_FMS#
- CPU1\_ADS#
- CPU1\_BNR#
- CPU1\_HIT#
- CPU1\_INTR
- CPU1\_PSI#
- CPU1\_SMI#
- GFX3\_HCLK
- KBC3\_A20G
- KBC3\_VRON
- KBC5\_TCLK
- LCD3\_BRIT
- MCD3\_SDWP
- MEM1\_VREF
- PLT3\_RST#
- SMB3\_DATA
- THM3\_STP#
- WLON\_LED#
- CLK3\_PWRGD
- CLK3\_ICH14
- CLK3\_PWRGD
- CLK3\_USB48
- CPU1\_A20M#
- CPU1\_BPR#
- CPU1\_BREQ#
- CPU1\_DBSY#
- CPU1\_DPWR#
- CPU1\_DRDY#
- CPU1\_FERR#
- CPU1\_INIT#
- CPU1\_LOCK#
- CPU1\_TRDY#
- CPU1\_TRST#
- CRT3\_HSYNC
- CRT3\_VSYNC
- CRT5\_HSYNC
- CRT5\_VSYNC
- DRAM\_RST#
- EXP3\_OPPE#
- GFX3\_HDATA
- GFX3\_ROMS#
- GFX3\_ROMSO
- KBC3\_CHGEN
- KBC3\_PWRGD
- KBC3\_PWRON
- KBC5\_TDATA
- MCD3\_SDOP#
- MCD3\_SDCLK
- MCD3\_SDCMD
- MCH1\_HVREF
- PC13\_INTA#
- PC13\_INTB#
- PC13\_INTC#
- PC13\_INTD#
- PC13\_IRDY#
- PC13\_PERR#
- PC13\_SERR#
- PC13\_STOP#
- PC13\_TRDY#
- PE33\_WAKE#
- BAT3\_SMCLK#
- CHP3\_GPIO18
- CHP3\_GPIO20
- CHP3\_SERIRQ
- CHP3\_SLP#
- CHP3\_SLPSS#
- CLK3\_DBG LPC
- CPU1\_DPSLP#
- CPU1\_IGNNE#
- CPU1\_VID(0)
- CPU1\_VID(1)
- CPU1\_VID(2)
- CPU1\_VID(3)
- CPU1\_VID(4)
- CPU1\_VID(5)
- CPU1\_VID(6)
- CRT3\_DDCCLK
- CRT5\_DDCCLK
- EXP3\_CLKUSB#
- EXP3\_PERR#
- GFX3\_STRAP2
- KBC3\_BKLTON
- KBC3\_PRECHG
- KBC3\_PWRSW#
- KBC3\_RFOFF#
- KBC3\_SCLED#
- KBC3\_SMCLK#
- KBC3\_SUSPWR
- LCD3\_BKLTON
- LPC3\_LAD(0)
- LPC3\_LAD(1)
- LPC3\_LAD(2)
- LPC3\_LAD(3)
- MCD3\_SDDAT0
- MCD3\_SDDAT1
- MCD3\_SDDAT2
- MCD3\_SDDAT3
- PC13\_FRAME#
- PC13\_PLOCK#
- PE33\_BKLTEN
- SMB3\_ALERT#
- THM3\_ALERT#
- USB3\_PWRON#
- VCCP3\_PWRGD
- BAT3\_DETECT#
- BAT3\_SMDATA#
- CHP3\_BIOSW#
- CHP3\_CPURST#
- CHP3\_PCISTP#
- CLK3\_GFX\_27M
- CLK3\_PCLKMCOM
- CPU1\_DPRSTP#
- CPU1\_DSTRB#
- CPU2\_THERMDA
- CPU2\_THERMDC
- CRT3\_DDCDATA
- CRT5\_DDCDATA
- EXP3\_CLKREQ#
- FANS\_FBACK#
- SCORE3\_PWRGD
- GFX3\_ROMSCLK
- GFX3\_THERMDN
- GFX3\_THERMDP
- HDA3\_MDC\_SDO
- KBC3\_CHG1.2V
- KBC3\_CPURST#
- KBC3\_EXTSMI#
- KBC3\_NUMLED#
- KBC3\_PWRON\_INV#
- KBC3\_LED\_ACIN#
- KBC3\_USBWRON#
- LCD3\_EDID\_DATA
- PE33\_HDMI\_DATA
- PE35\_HDMI\_DATA
- TPDS\_L\_BUTTON#
- TPDS\_R\_BUTTON#
- VRM3\_CPU\_PWRGD
- VRM3\_DDR\_PWRGD
- CHP3\_ME\_RTCRST#
- CLK3\_GFX\_27M\_SS
- KBC3\_SATACLKREQ#
- KBC3\_LED\_CHARGE#
- KBC3\_THERM\_SMCLK
- SUB\_LID3\_SWITCH#
- KBC3\_THERM\_SMDATA
- KBC3\_PWRBTN#
- KBC3\_RSMRST#
- KBC3\_RUNSC#
- KBC3\_SMDATA#
- KBC3\_SPMUTE#
- LID3\_SWITCH#
- LOM3\_CLKREQ#
- LPC3\_LFRAME#
- MCH1\_HASWING
- MCH3\_CLKREQ#
- MCH3\_EXTS#
- MCH3\_EXTS1#
- MCH3\_CLKREQ#
- PC13\_CLKRUN#
- PC13\_DEVSEL#
- CHP3\_CL\_CLK\_0
- CHP3\_DPRSLPVR
- CHP3\_PM\_SYNC#
- CHP3\_SATALED#
- CHP3\_SUSSTAT#
- CPU1\_PWRGD CPU
- CPU1\_VCCSENSE
- CPU1\_VSSSENSE
- GFX3\_VOLTID\_0
- GFX3\_VOLTID\_1
- LPC3\_LAD(0)
- LPC3\_LAD(1)
- LPC3\_LAD(2)
- LPC3\_LAD(3)
- MCD3\_SDDAT0
- MCD3\_SDDAT1
- MCD3\_SDDAT2
- MCD3\_SDDAT3
- PC13\_PLOCK#
- PE33\_BKLTEN
- SMB3\_ALERT#
- THM3\_ALERT#
- USB3\_PWRON#
- VCCP3\_PWRGD
- BAT3\_DETECT#
- BAT3\_SMDATA#
- CHP3\_BIOS\_CR#
- CHP3\_CL\_DATA\_0
- CHP3\_CL\_RST\_0#
- CHP3\_INTRUDER#
- CHP3\_USBWRON#
- CLK3\_PCLKMCOM
- CPU1\_DPRSTP#
- CPU3\_THRMTRIP#
- ITP3\_DBRESET#
- KBC3\_LED\_ACIN#
- KBC3\_USBWRON#
- LCD3\_EDID\_DATA
- PE33\_HDMI\_DATA
- PE35\_HDMI\_DATA
- TPDS\_L\_BUTTON#
- TPDS\_R\_BUTTON#
- VRM3\_CPU\_PWRGD
- VRM3\_DDR\_PWRGD
- CHP3\_ME\_RTCRST#
- CLK3\_GFX\_27M\_SS
- KBC3\_PWRON\_INV#
- KBC3\_SATACLKREQ#
- KBC3\_LED\_CHARGE#
- KBC3\_THERM\_SMCLK
- SUB\_LID3\_SWITCH#
- KBC3\_THERM\_SMDATA
- P3.3V\_MICOM
- SUB\_GND
- SUB\_GND\_A
- SUB\_GND\_C
- SUB\_P3.3V
- P5.0V\_AUX

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DESIGN	Xiaohong Zheng	DATE	04/30/2009	TITLE	QingDao_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MAIN		
APPROVAL	BC LEE	REV	1.0	TP	BA41	PART NO. 01097/8/(1100)A
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM	PAGE	12	OF 15

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- HDMI3\_APD
- HDMI3\_PEO
- HDMI3\_PRE
- AUD5\_MIC2\_INT
- HDA3\_AUD\_SDO
- CPU1\_BSEL0
- CPU1\_BSEL1
- CPU1\_BSEL2
- CPU1\_HITM#
  
- HDMI3\_AS01
- HDMI3\_EMIO
- HDMI3\_EMI1

- GFX3\_THERM#
- KBC3\_SPI\_DI
- KBC3\_SPI\_DO
- KBC3\_USBCHG
- CPU1\_STPCLK#
- HDMI3\_DDCBUF
- HST3\_SPI3\_DI
- HST3\_SPI3\_DO
- KBC3\_SPI\_CLK
- KBC3\_SPI\_CS#
- KBC3\_SPI\_WP#

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D  
 C  
 B  
 A

4

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2

1

D  
C  
B  
A

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- HDA3\_AUD\_BCLK
- HDA3\_AUD\_SDI0
- HDA3\_AUD\_SYNC
- HST3\_SPI0\_CLK
- HST3\_SPI0\_CS#
- VGA5\_HDMI\_HPD
- AUD5\_HP\_O\_LEFT
- AUD5\_MIC1\_LEFT
- AUD5\_HP\_O\_RIGHT
- AUD5\_MIC1\_RIGHT
- KBC3\_TPAD\_CTRL#

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3

2

1