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Bremen-UL

CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : Bremen-UL
PBA Name : MAIN
PCB Code : GCE : BA41-01177A
 NAN : BA41-01178A
 HAN : BA41-01179A
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.10.19

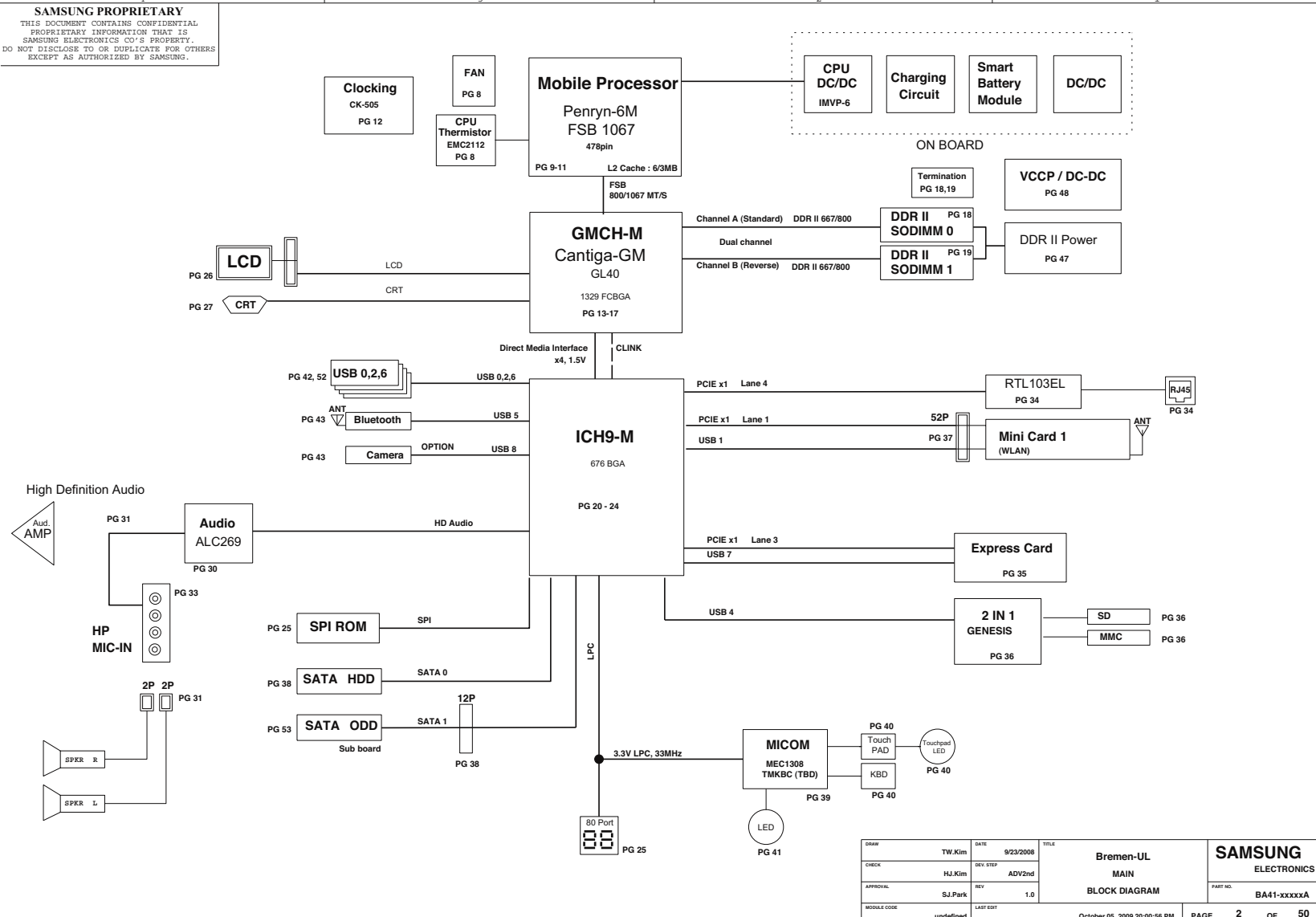
Design	CHECK	APPROVAL

■ Owner : SEC Mobile R & D Signature : X

DRAW	TW.Kim	DATE	10/10/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd	MAIN	COVER	
APPROVAL	S.J.Park	REV	1.0	COVER	PART NO.	BA41-xxxxxA
MODEL CODE		LAST EDIT				
				October 05, 2009 20:00:56 PM	PAGE	1 OF 50

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CHECK	Hj.Kim	DEV. STEP	ADV2nd			
APPROVAL	S.J.Park	REV	1.0		BLOCK DIAGRAM	PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EST				
October 05, 2009 20:00:56 PM					PAGE	2 OF 50

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	F
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	NC
1	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
2	SYSTEM PORT 2	2	NC
3	NC	3	LOM
4	NC	4	Mini Card 2 (ROBSON or DVB-T)
5	Bluetooth	5	NC
6	Mini PCI Express 2		
7	Camera		
8	NC		
9	NC		

(This table will be update.)

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

LCD Panel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

REVISION HISTORY

See rev notes for more information.

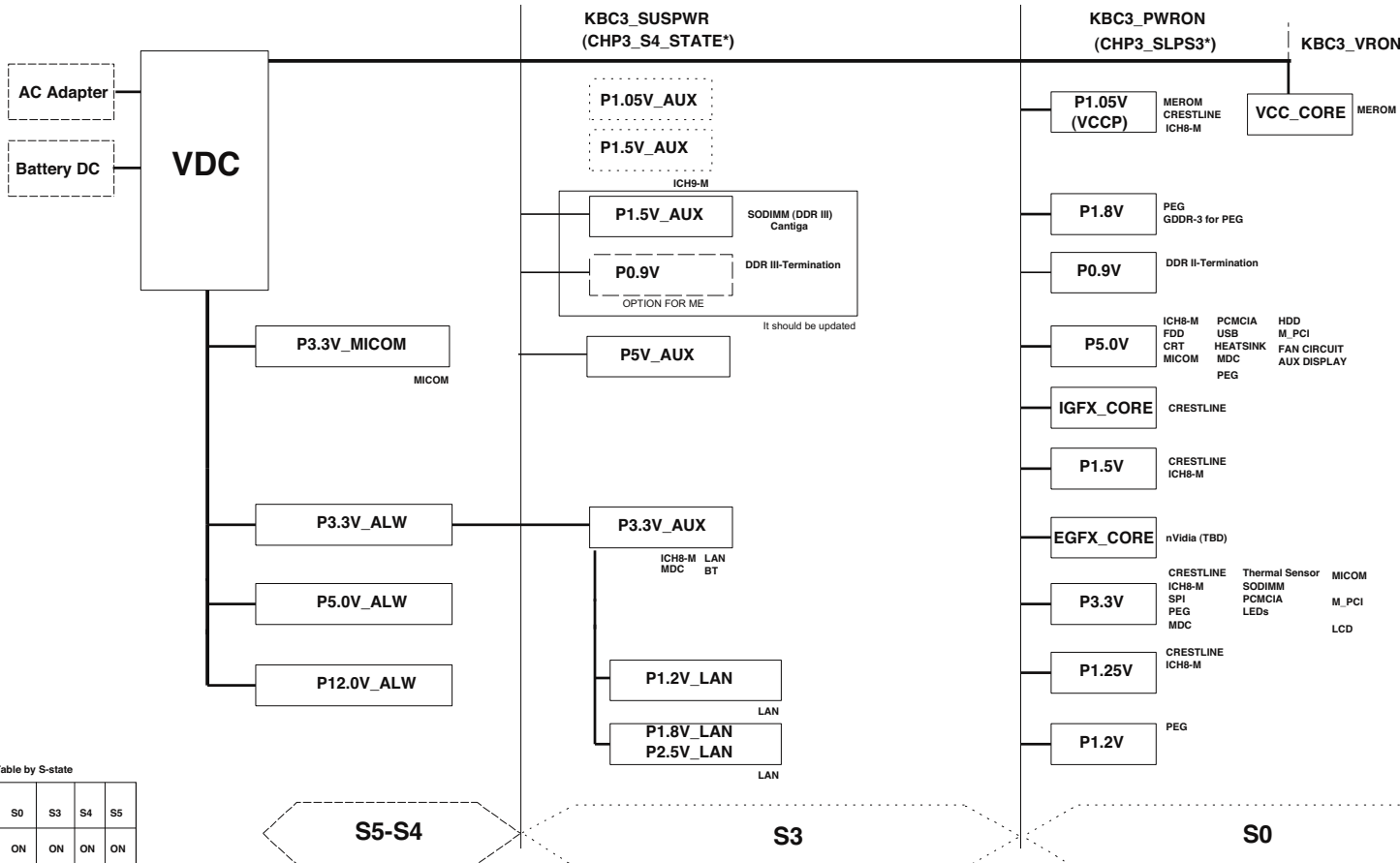
DRWN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd	MAIN	BOARD INFO	
APPROVAL	S.J.Park	REV	1.0			
MOBILE CODE	undefined	LAST EST				
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POWER DIAGRAM

Rev 0.1



Power On/Off Table by S-state

Rail \ State	S0	S3	S4	S5
+V'A(LWS) +V'LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	---	---
+V'AUX	ON	ON	---	---
+V	ON	---	---	---
+V' (CORE)	ON	---	---	---

4 3 2 1

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BLANK

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CHECK	HJ.Kim	DEV. STEP	ADV2nd			
APPROVAL	SJ.Park	REV	1.0		BLANK	PART NO.
MOBILE CODE		LAST EDIT				BA41-xxxxxA
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BLANK

DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL		SAMSUNG ELECTRONICS
CHECK	HJ.Kim	DEV. STEP	ADV2nd	MAIN			
APPROVAL	SJ.Park	REV	1.0	BLANK		PART NO.	BA41-xxxxxA
MOBILE CODE	undefined	LAST EST	October 05, 2009 20:00:56 PM		PAGE	6	OF 50

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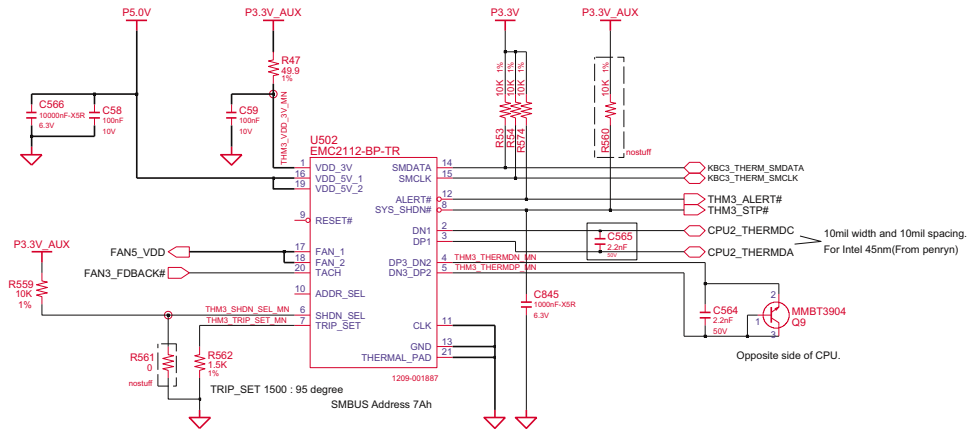
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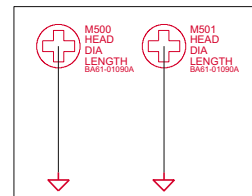
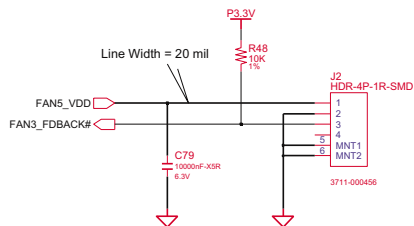
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THERMAL SENSOR & FAN CONTROL



SHDN_SEL MODE	
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
<input checked="" type="checkbox"/>	EXT.DIODE 2 MODE

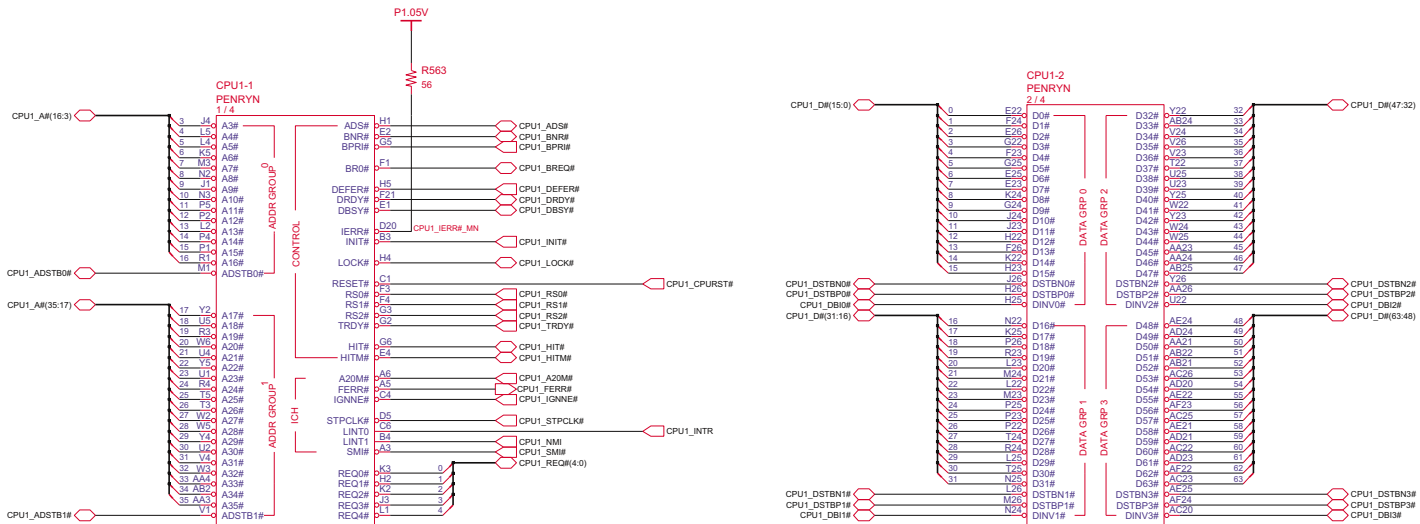
ADDRESSSEL MODE	
0	0101 111xb
<input checked="" type="checkbox"/>	0111 101xb (7A)
1	0101 110xb



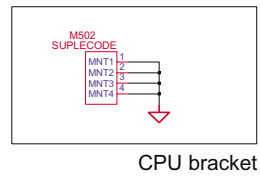
To support heatsink

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CPU Socket : 3704-001153



CPU bracket

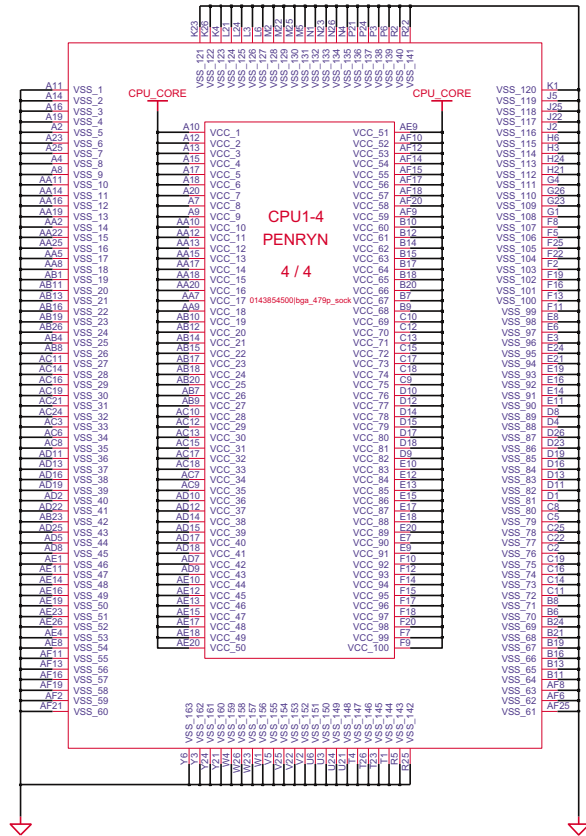
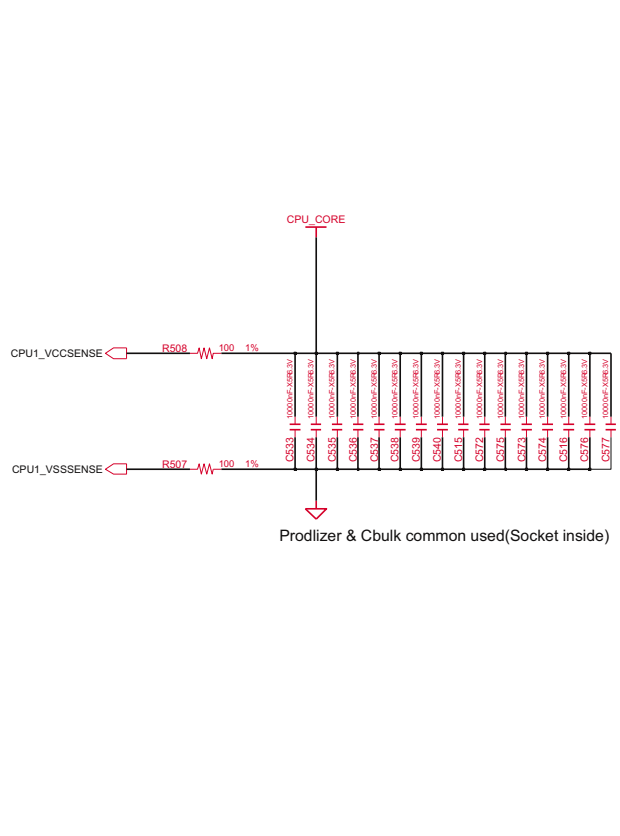
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CHECK	H.J.Kim	DEV. STEP	ADV2nd		CPU	
APPROVAL	S.J.Park	REV	1.0		PENRYN (1/3)	PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EST				

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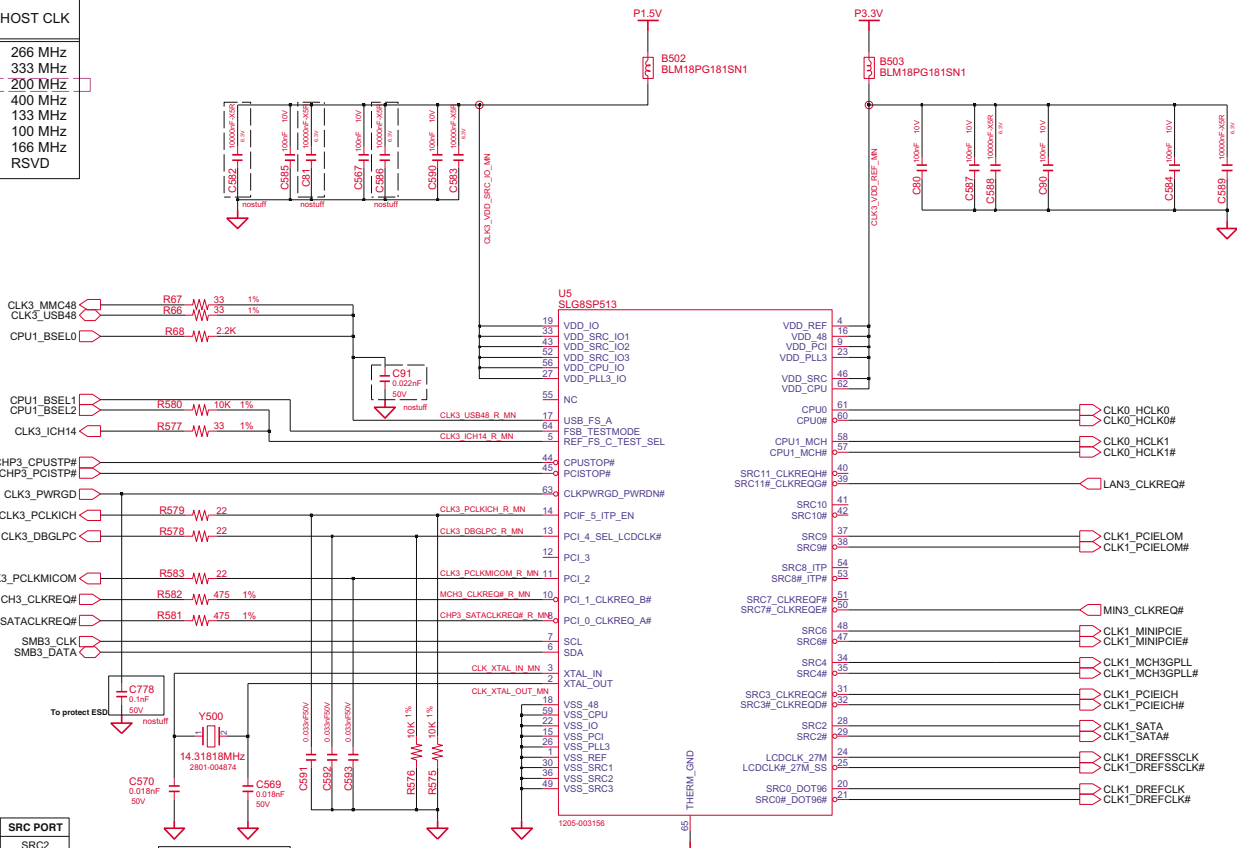
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DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL																								
CHECK	HJ.Kim	DEV. STEP	ADV2nd		CPU																								
APPROVAL	S.J.Park	REV	1.0		PENRYN (3/3)																								
MODULE CODE	undefined	LAST EST																											
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PART NO.	B441-xxxxxA																												
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CK505M

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LDCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

Place 14.31818MHz within 500mils of CK-505

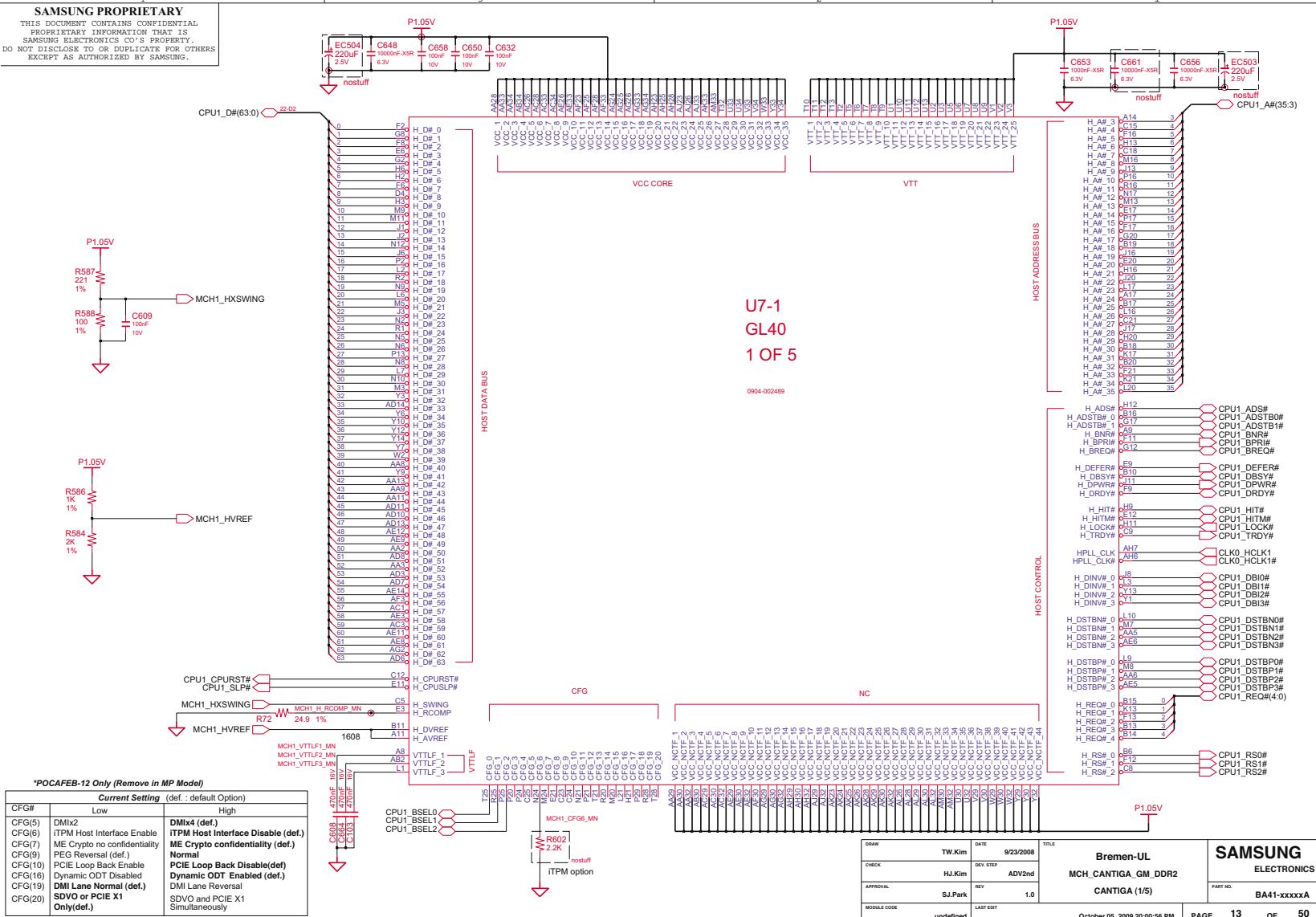
This part is 64pin QFN package.

IDT : 1205-003159
SL : 1205-003533

DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	
CHECK	H.J.Kim	DEV_STEP	ADV2nd	MAIN_CLOCK_CIRCUIT		
APPROVAL	S.J.Park	REV	1.0	CK_Clock_505M		
MOBILE_CODE	undefined	LAST_EDIT		PART NO. BA41-xxxxxA		
				October 05, 2009 20:00:56 PM	PAGE	12 OF 50

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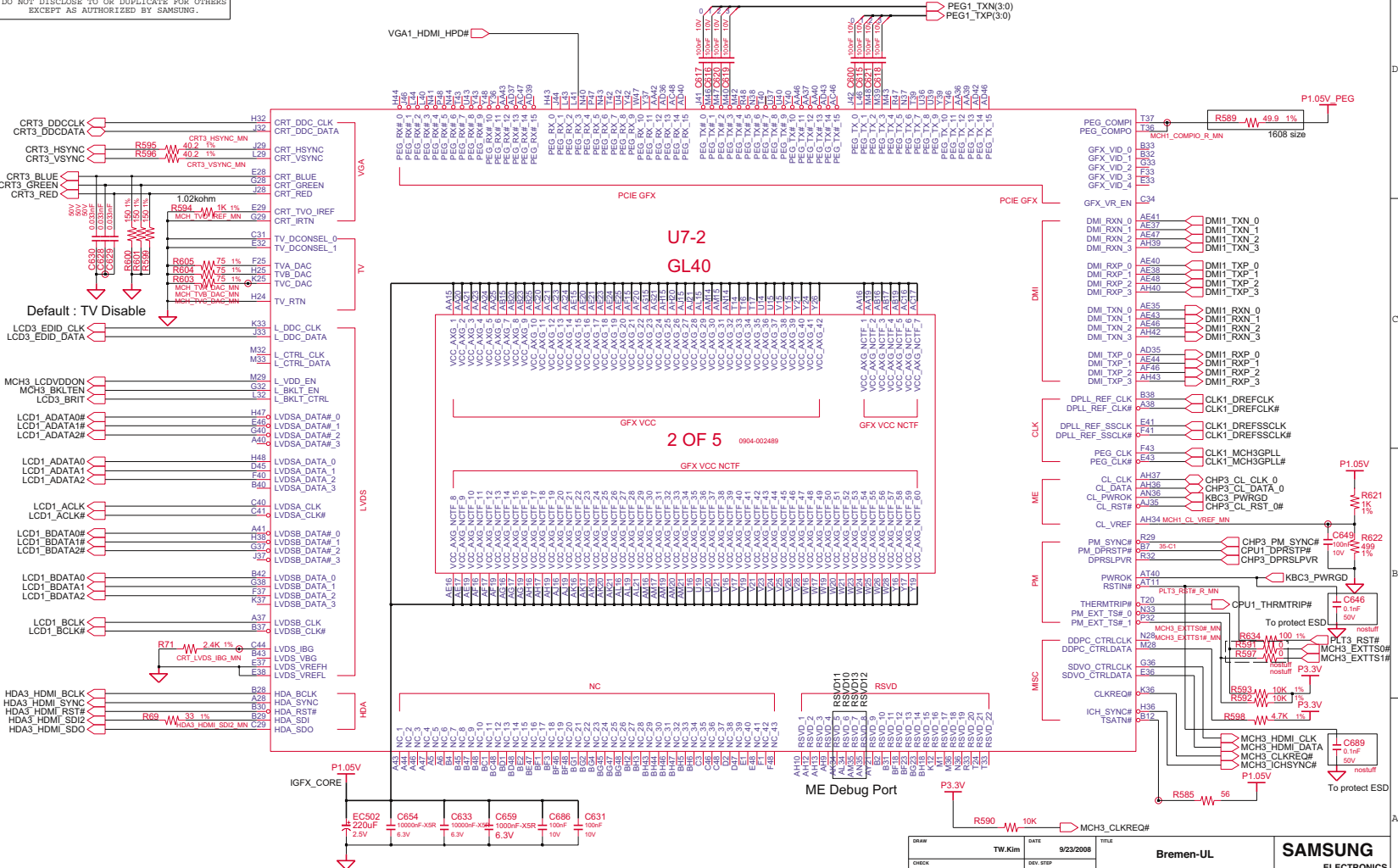
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***POCAFEB-12 Only (Removes in MP Model)**

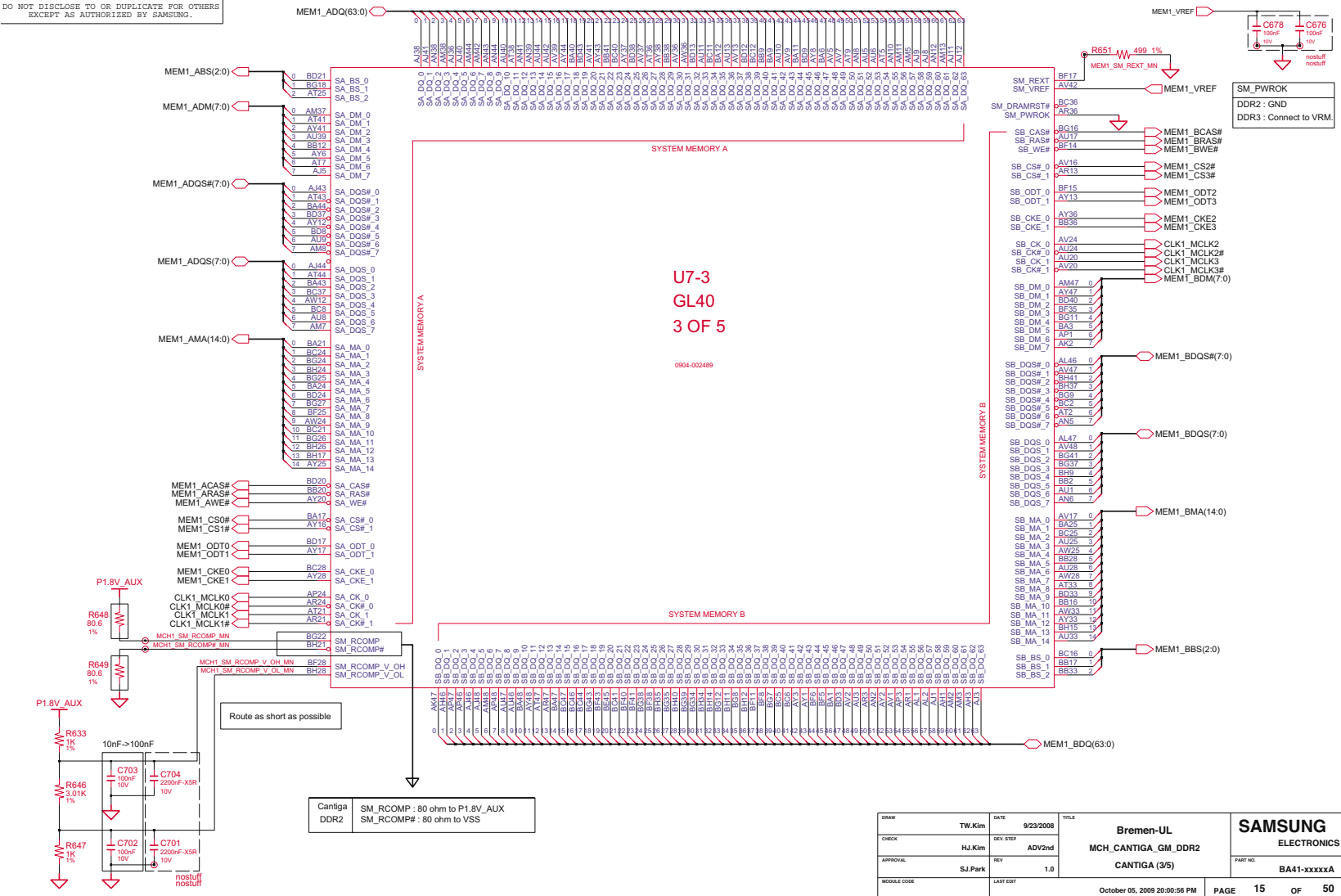
Current Setting (def.: default Option)		
CFG#	Low	High
CFG(5)	DMi2	DMi2x (def.)
CFG(6)	ITPM Host Interface Enable	ITPM Host Interface Disable (def.)
CFG(7)	ME Crypto no confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIE Loop Back Enable	PCIE Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneous

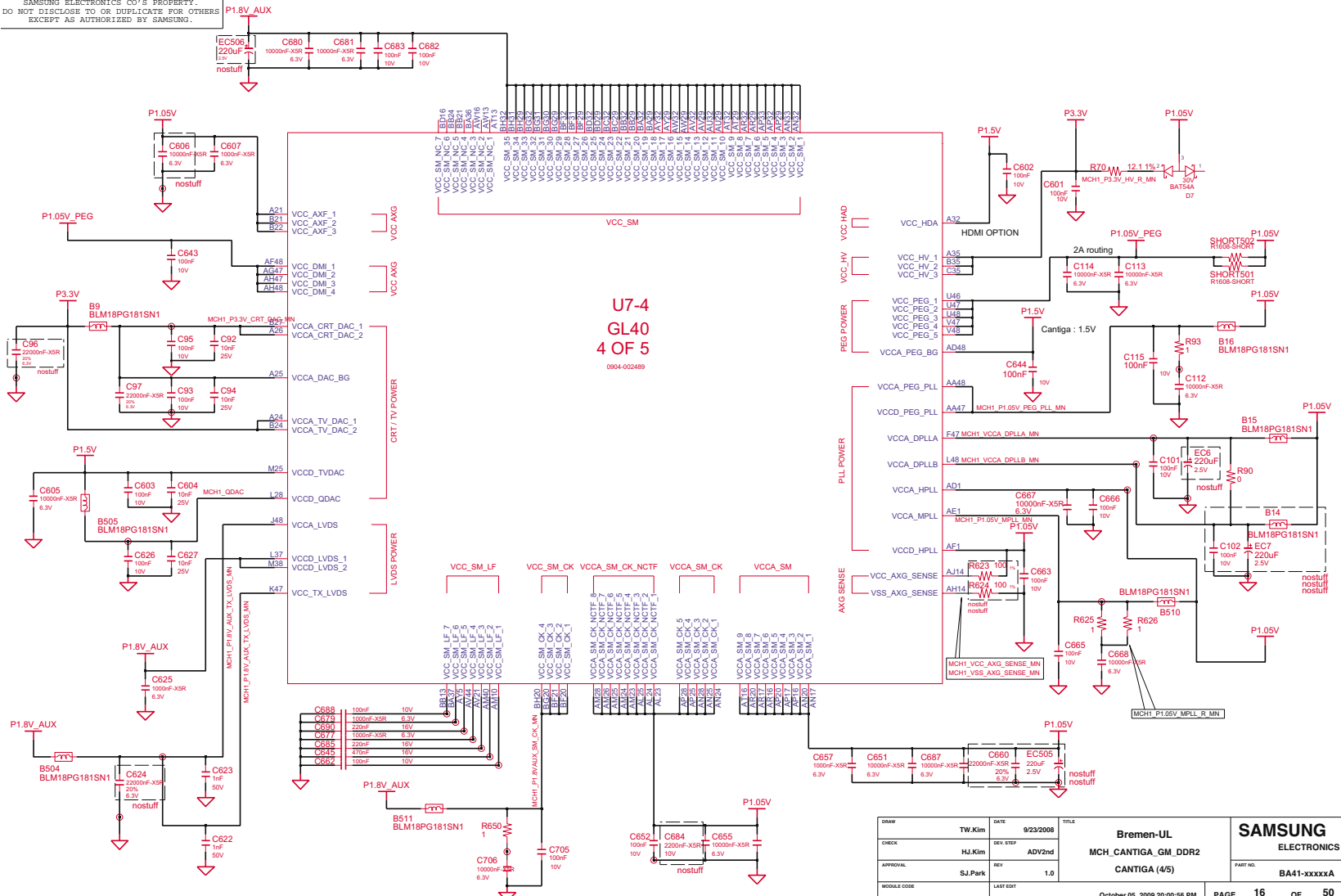
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CHECK	H.J.Kim	DEV STEP	ADV2nd	MCH_CANTIGA_GM_DDR2		
APPROVAL	S.J.Park	REV	1.0	CANTIGA (1/5)		PART NO. BA41-xxxxxA
MOUL CODE	undefined	LAST EST				
				October 05, 2009 20:00:56 PM	PAGE	13 OF 50



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PLACE EACH CAP NEAR AV42 PIN

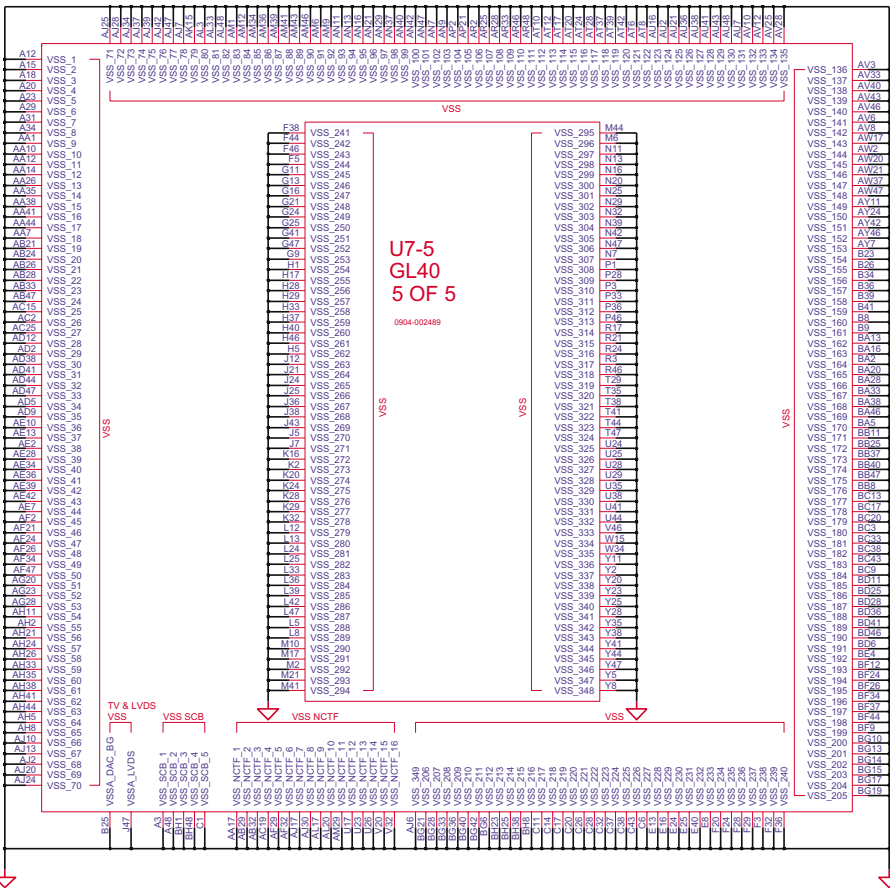




**U7-4
GL40
4 OF 5**
0904-002489

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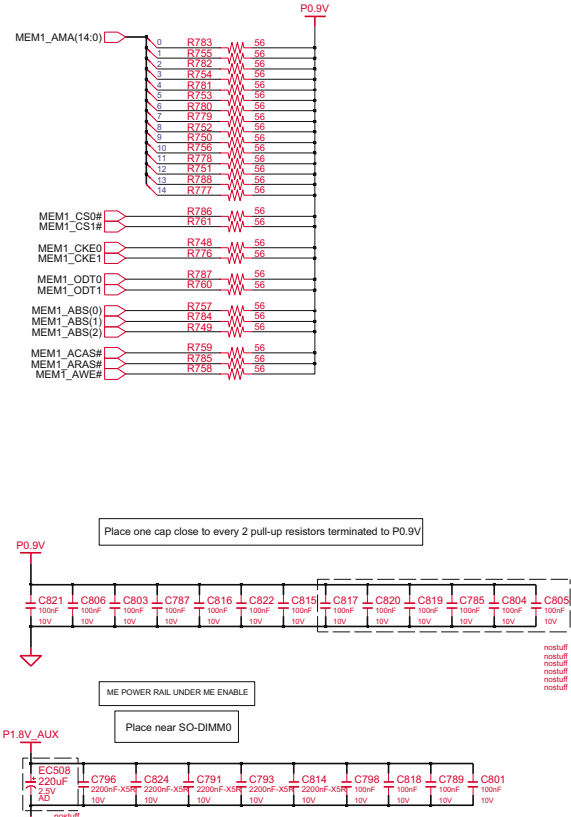
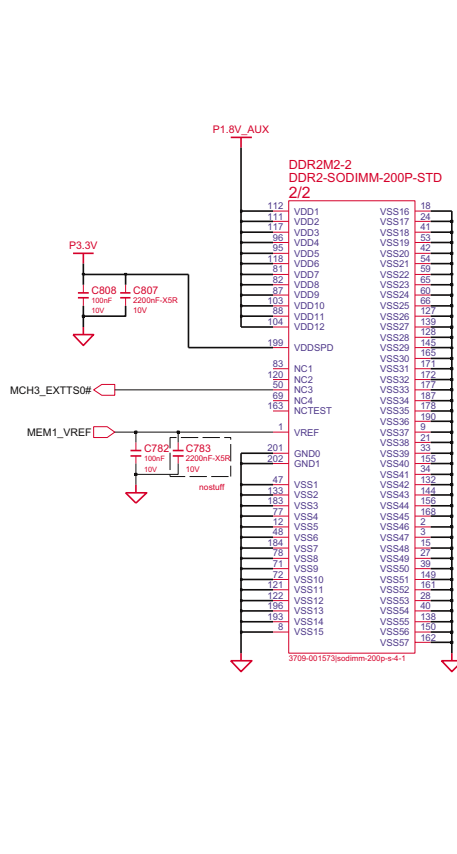
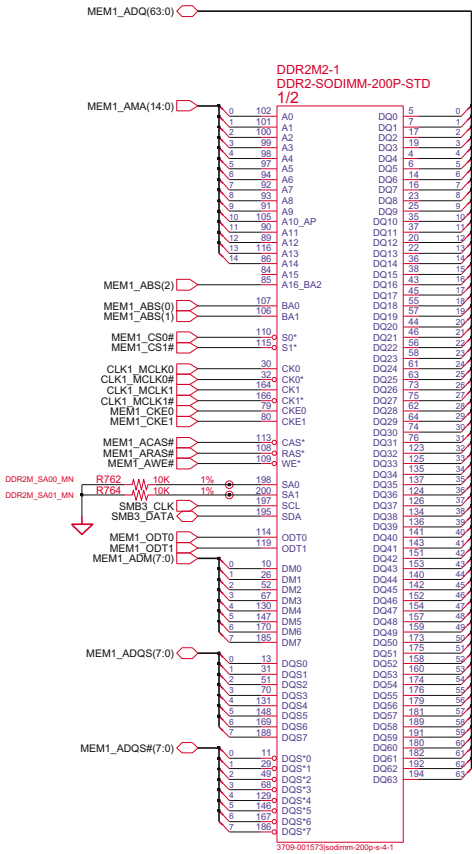
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CHECK	Hj.Kim	DEV_STEP	ADV2nd	MCH_CANTIGA_GM_DDR2		
APPROVAL	SJ.Park	REV	1.0	CANTIGA (5/5)		PART NO. BA41-xxxxxA
MOBILE CODE		LAST EDIT				
			October 05, 2009 20:00:56 PM		PAGE	17 OF 50

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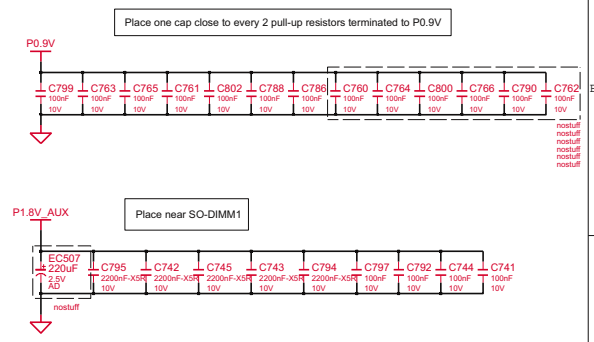
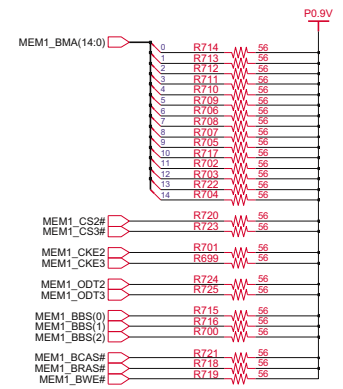
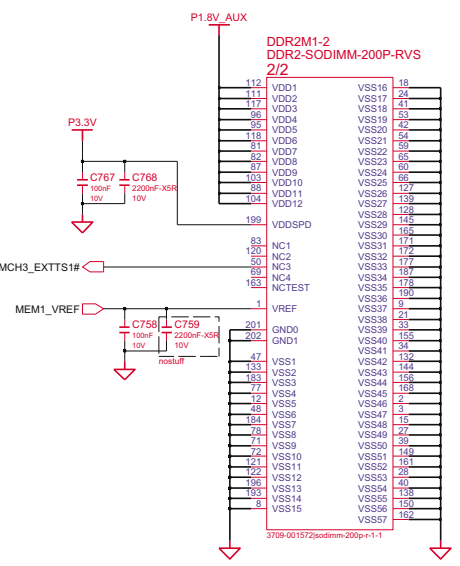
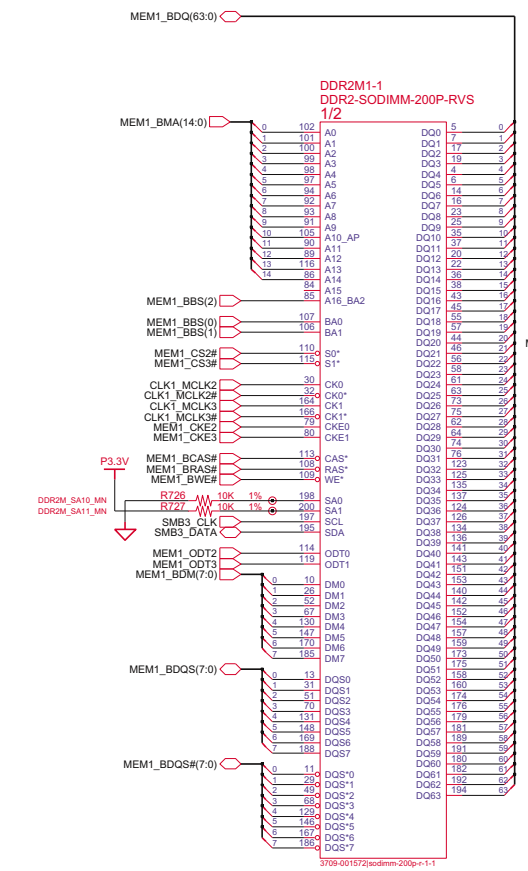
DDR2 SO-DIMM #0

Height : 4mm (Standard)

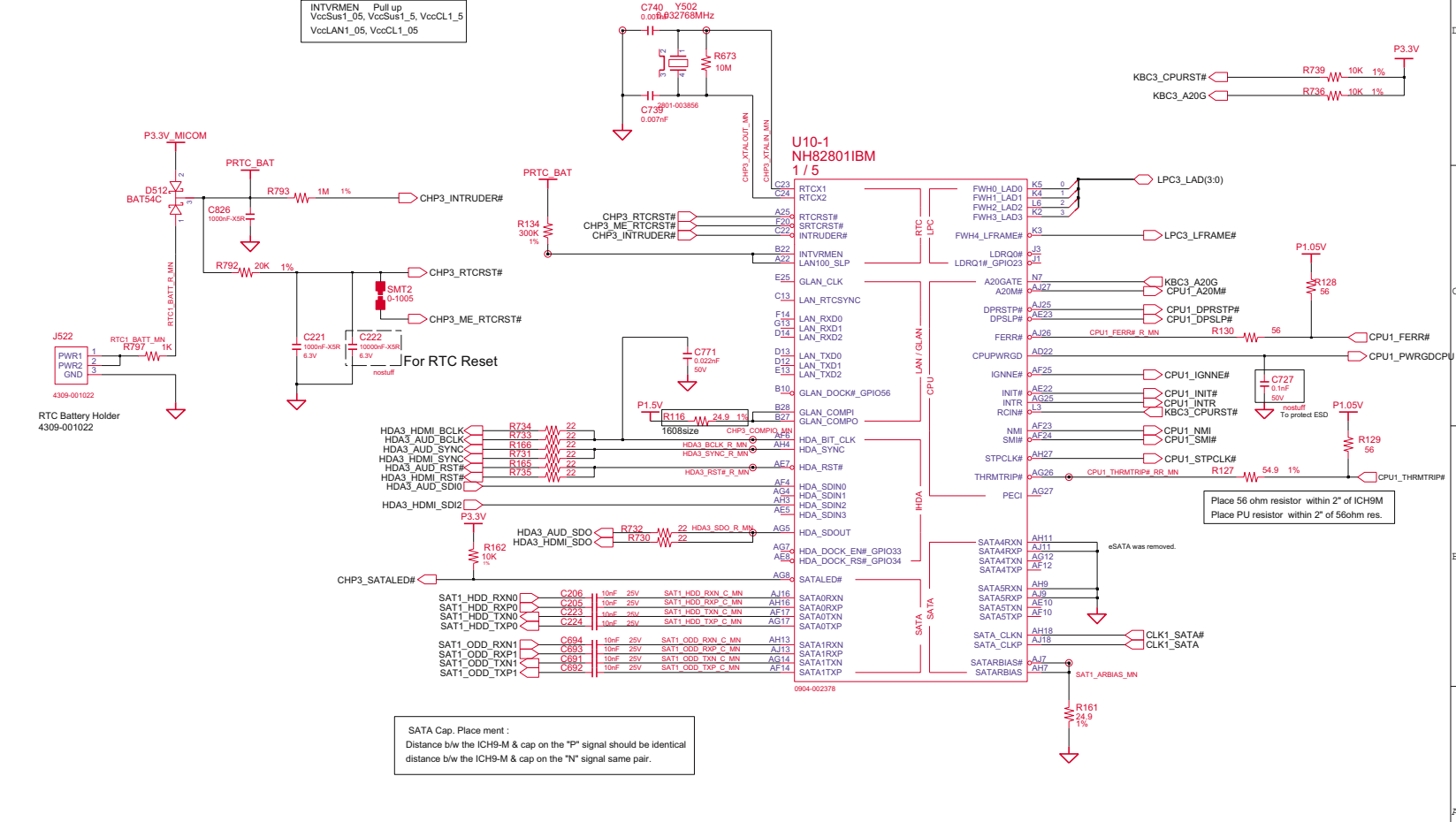


DDR2 SO-DIMM #1

Height : 4mm (Reverse)



Internal VR Strap
 INTVRMEN Pull up
 VccSus1_05, VccSus1_5, VccCL1_5
 VccLAN1_05, VccCL1_05



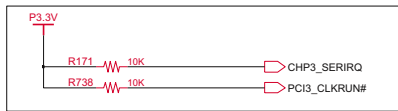
SATA Cap. Place ment :
 Distance b/w the ICH9-M & cap on the "P" signal should be identical
 distance b/w the ICH9-M & cap on the "N" signal same pair.

Place 56 ohm resistor within 2" of ICH9M
 Place PU resistor within 2" of 56ohm res.

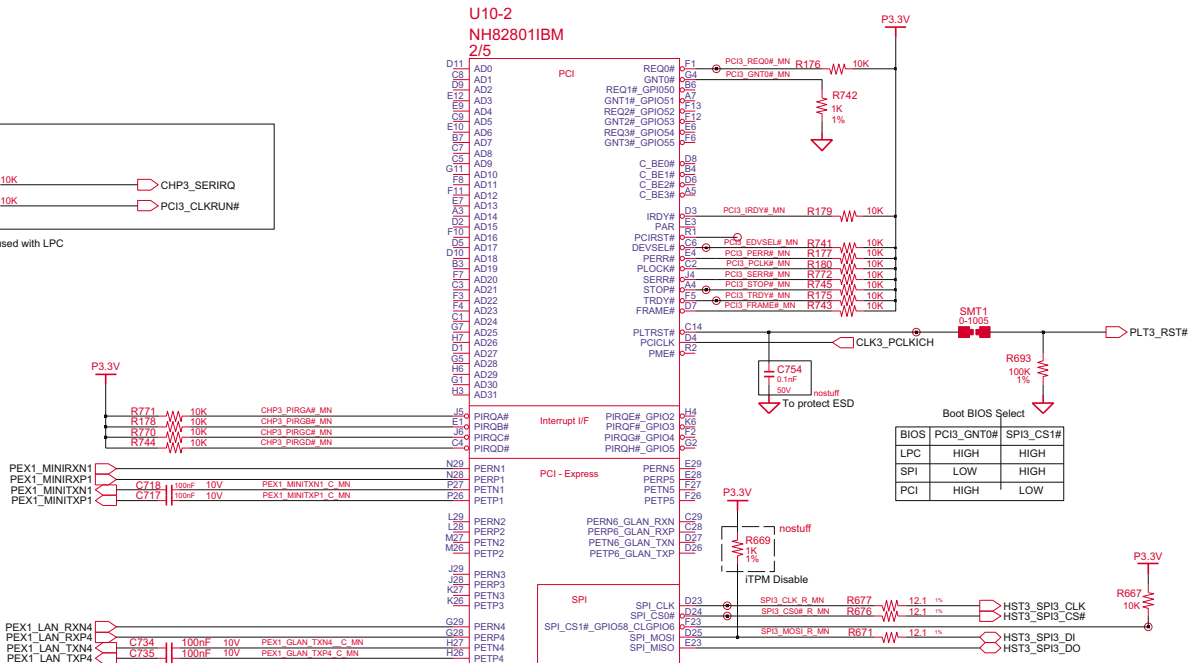
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**U10-2
NH82801IBM
2/5**

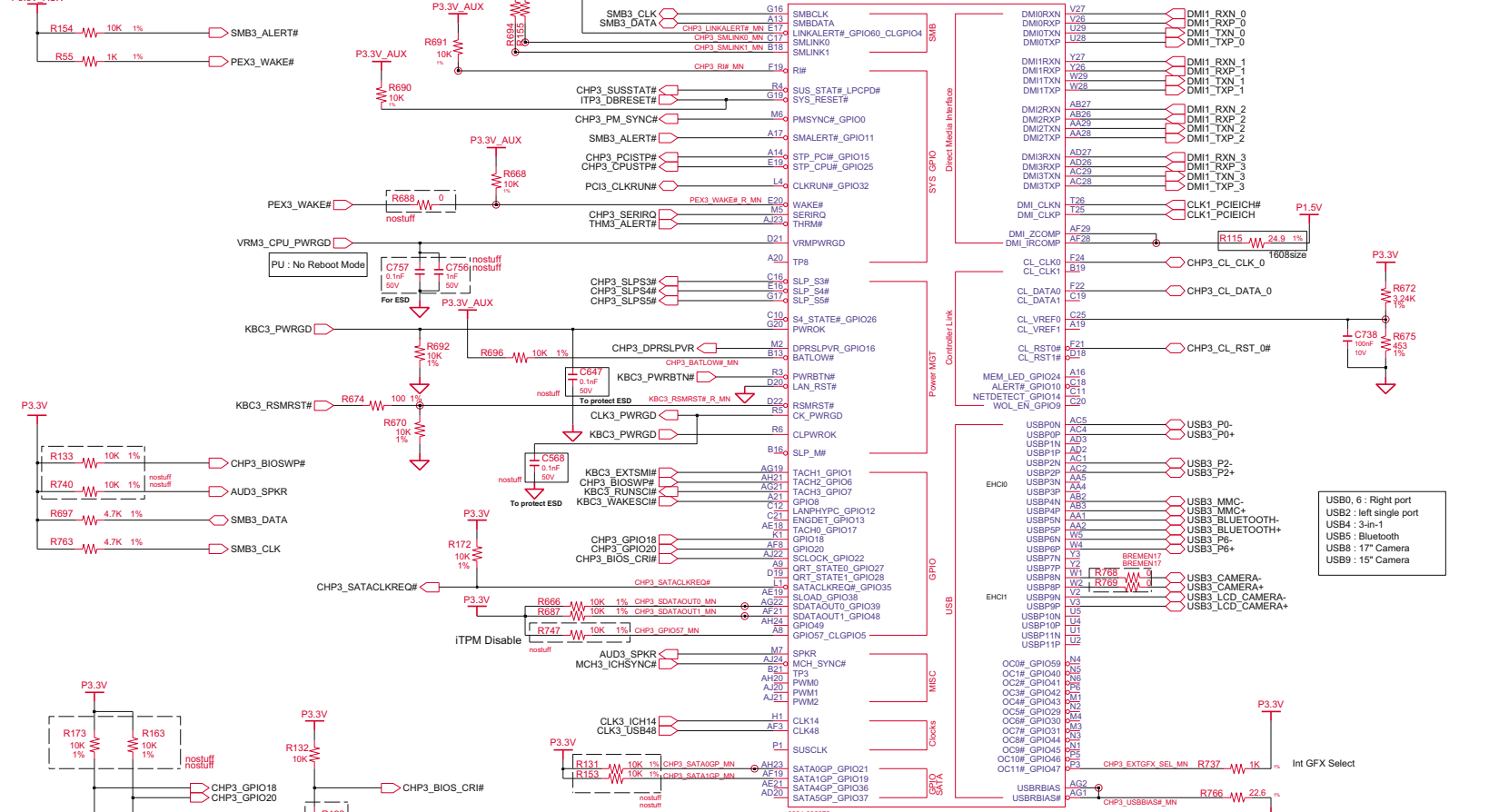


LPC option ; These are used with LPC



DATE	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS	
CHECK	Hj.Kim	DEV_STEP	ADV2nd		ICH_9M_B		
APPROVAL	S.J.Park	REV	1.0		ICH9-M (2/5)	PART NO. BA41-xxxxxA	
MOBILE CODE	undefined	LAST EST					
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**U10-3
 NH828011BM
 3 / 5**



PU : No Reboot Mode

To protect ESD

To protect ESD

BIOS CRISIS RECOVER STRAP
 PLACE NEAR KEYBOARD
 (Put it a debugger connector)

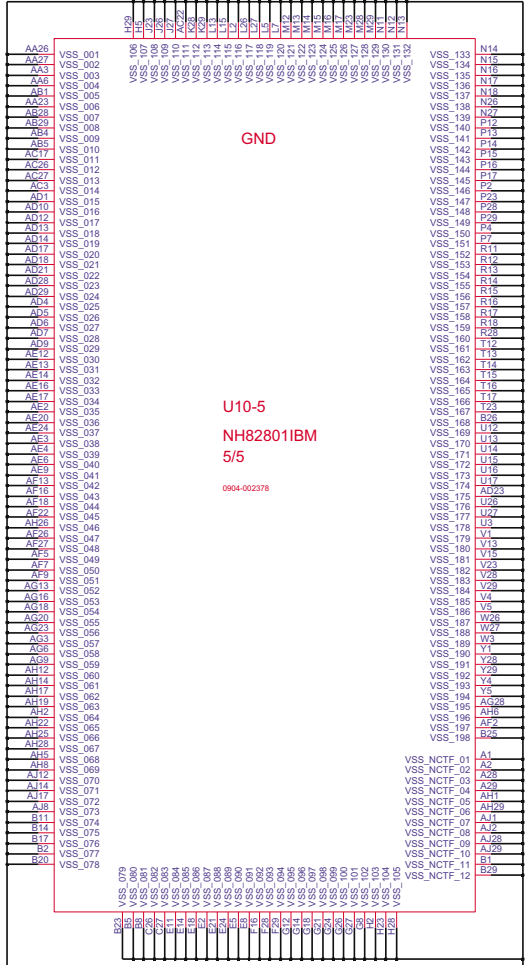
USB0 : 6 ; Right port
 USB2 : left single port
 USB4 : 3-in-1
 USB5 : Bluetooth
 USB8 : 17" Camera
 USB9 : 15" Camera

DATE	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL
CHECK	H.J.Kim	DEV. STEP	ADV2nd		
APPROVAL	S.J.Park	REV	1.0		
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PART NO. BA41-xxxxxA

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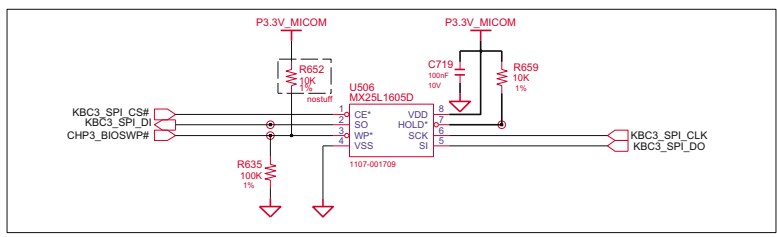


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CHECK	H.J.Kim	DEV. STEP	ADV2nd	ICH_9M_B		PART NO.	
APPROVAL	S.J.Park	REV	1.0	ICH9-M (5/5)		BA41-xxxxxA	
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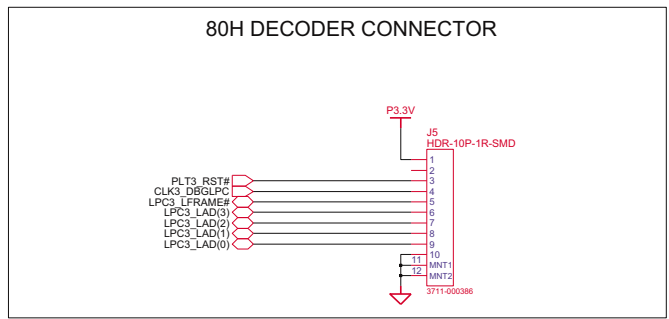
SPI_BIOS_ROM

16MBit

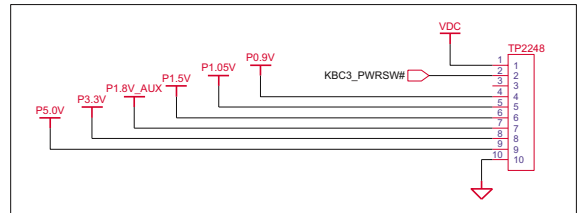


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGES
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU I/O	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	SET COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
	WITH INITIAL POST VALUE	8A	INIT. EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	9A	SHADOW OPTION ROMS
18	8254 TIMER INIT	9C	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT	9E	ENABLE HW INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
32	COMPUTE THE CPU SPEED	B2	CHECK FOR ERRORS
34	TEST CMOS RAM	B4	POST DONE/PREPARE TO BOOT I/O
36	SHADOW SYSTEM BIOS ROM	B8	ONE BEEP
38	AUTO SIZING CACHE	BA	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	BC	ACPI INIT
3D	LOAD ALTERNATE REG. WITH CMOS VALUE	BE	DMI INIT
42	INIT. INTERRUPT VECTOR	BF	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I2O SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	SHUTDOWN 5
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	DE	ENABLE NMI
54	SET KEYCLICK IF ENABLED	90	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 2
5A	DISPLAY *PRESS_* SETUP	94	DISABLE A20 ADDRESS LINE
60	TEST RAM BETWEEN 512K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
64	TEST EXTENDED MEMORY ADDRESS LINE		
	JUMP TO USER PATCH 1		

80H DECODER CONNECTOR



80port will be removed in MP stage.

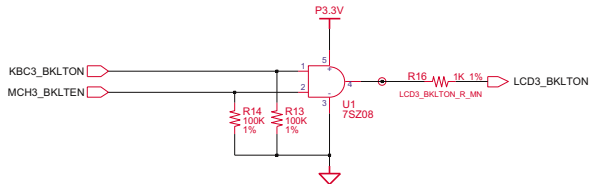


TP for ICT free

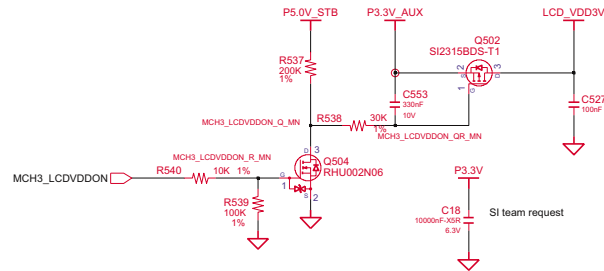
DATE	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd		SPI_BIOS_ROM	
APPROVAL	S.J.Park	REV	1.0		SPI_BIOS_ROM & ICT FREE TP	PART NO.
MODEL CODE		LAST EDIT				BA41-xxxxxA

LVDS

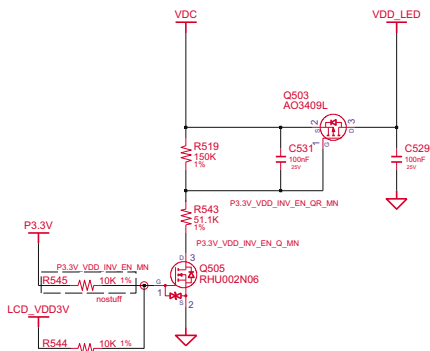
Backlight On



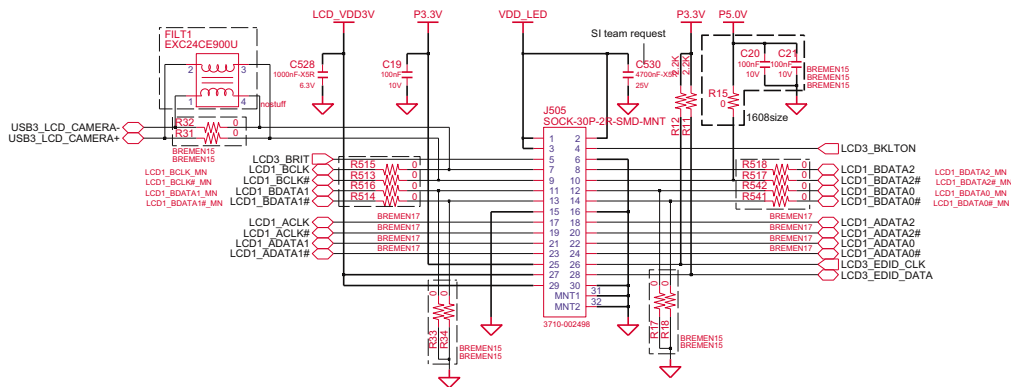
LCD Power EBL Purpose



LED Power



Camera + LCD Connector

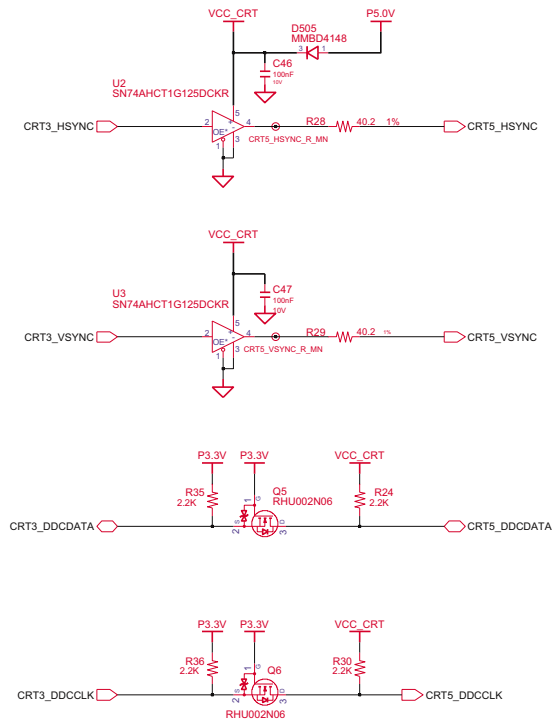


DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS	
CHECK	Hj.Kim	DEV. STEP	ADV2nd		GRAPHICS_IF		
APPROVAL	S.J.Park	REV	1.0		LVDS	PART NO. BA41-xxxxxA	
MODULE CODE		LAST EST					
October 05, 2009 20:00:56 PM						PAGE	26
1						OF	50

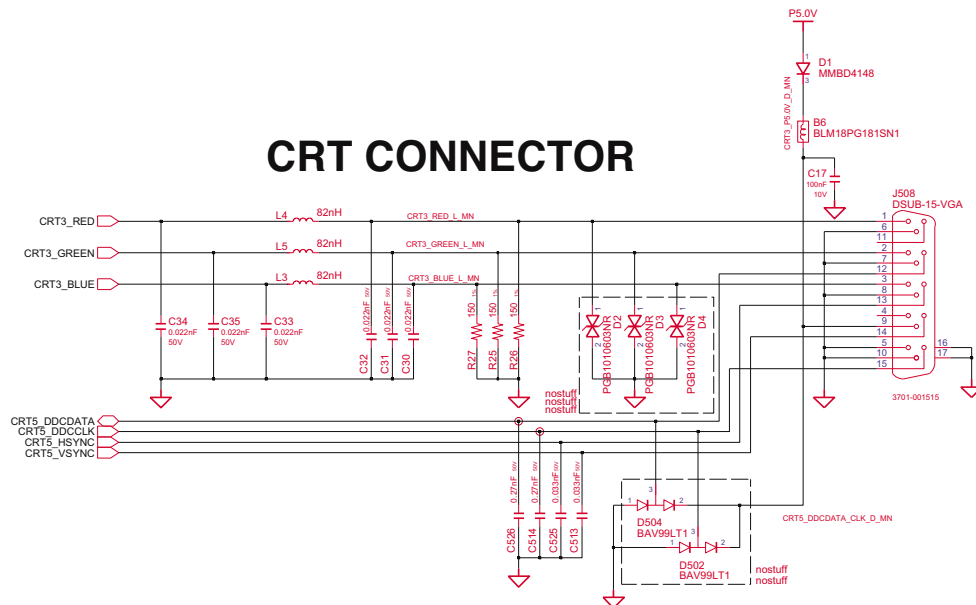
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CRT



CRT CONNECTOR



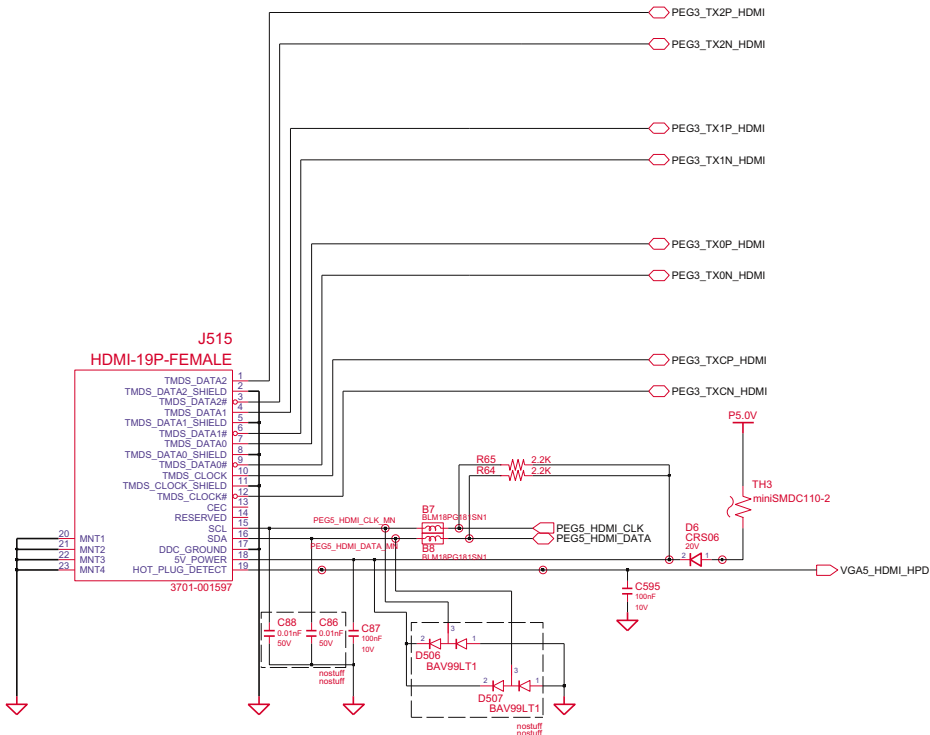
Check "CRT3_DDCCLK/DATA" Voltage Level
 2N06 Can be replaced with SM6K2

DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd	GRAPHICS_IF	PART NO.	
APPROVAL	S.J.Park	REV	1.0	CRT	BA41-xxxxxA	
MOBILE CODE		LAST EST				
				October 05, 2009 20:00:56 PM	PAGE	27 OF 50

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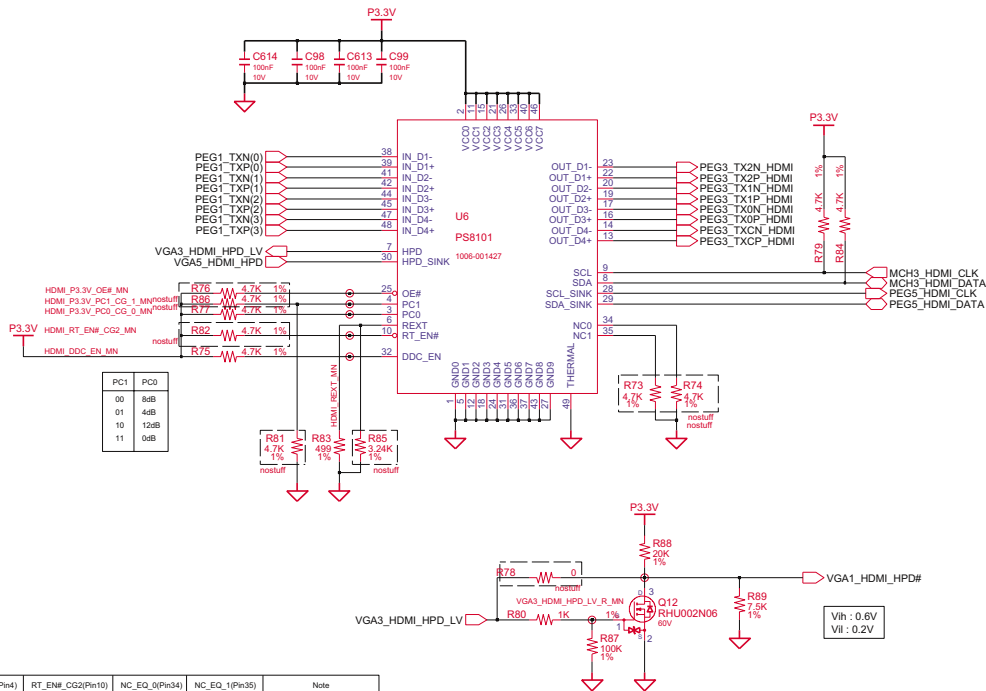
HDMI



DESIGN	TW.Kim	DATE	8/14/2009	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
CHECK	HJ.Kim	DEV. STEP	ADV2nd		HDMI	
APPROVAL	SJ.Park	REV	1.0		HDMI	PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT				
October 05, 2009 20:00:56 PM						PAGE 28 OF 50

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HDMI Level Shifter for Int. Graphic only



CG_2	CG_1	CG_0	Swing	Pre-amp	Slew rate
0	0	0	450mV	0dB	0dB
0	0	1	490mV	0dB	-3dB
0	1	0	450mV	0dB	-3dB
0	1	1	460mV	0dB	-4dB
1	0	0	340mV	0dB	0dB
1	0	1	400mV	2dB	0dB
1	1	0	400mV	2dB	0dB
1	1	1	420mV	0dB	0dB

PC1	PC0
00	8dB
01	4dB
10	12dB
11	0dB

EQ_1	EQ_0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

Internal Default Value

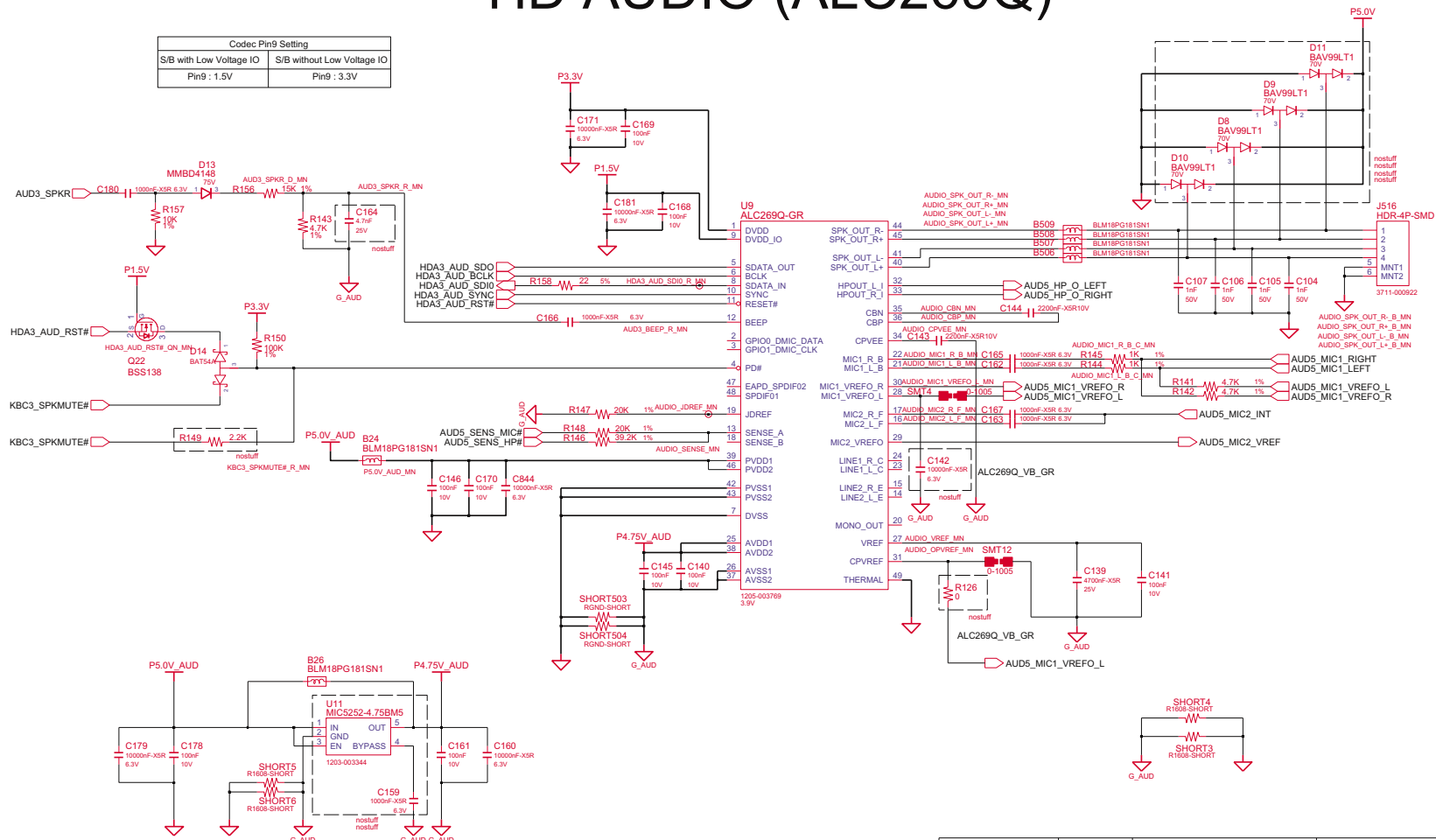
HDMI Level Shifter	REXT(Pin6)	PC1_C00(Pin3)	PC1_CG1(Pin4)	RT_EN#_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC	
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PU/PD exist CGs nostuff is 450mV swing

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HD AUDIO (ALC269Q)

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

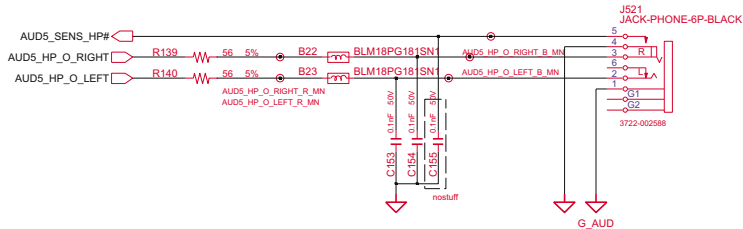


DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL HDA_CODEC	SAMSUNG ELECTRONICS
CHECK	H.J.Kim	DEV. STEP	ADV2nd			
APPROVAL	S.J.Park	REV	1.0		AUDIO CODEC ALC269Q_GR	PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT				
October 05, 2009 20:30:56 PM						PAGE 30 OF 50

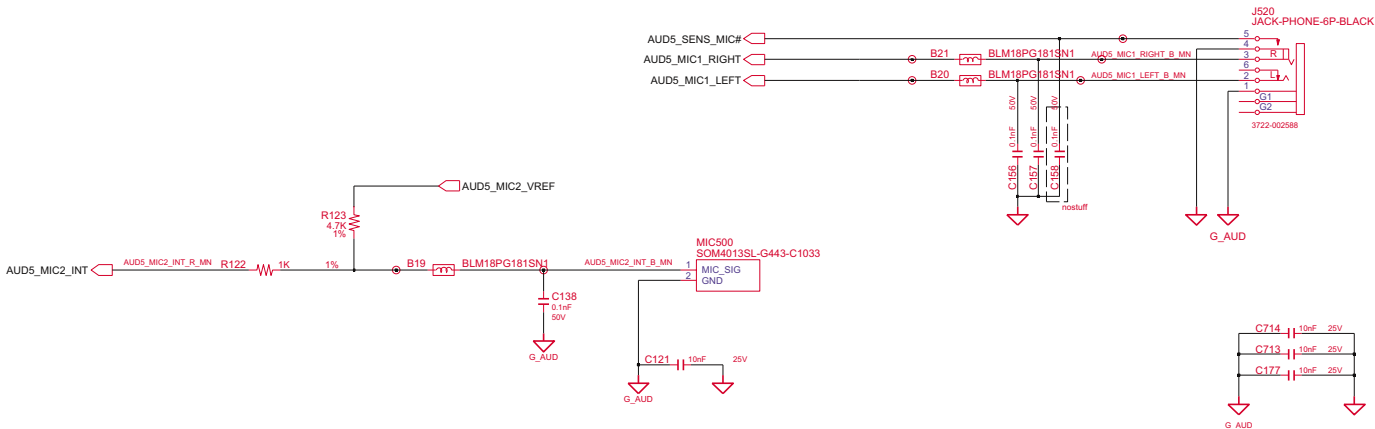
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HEADPHONE(BLACK)



MIC JACK(BLACK)



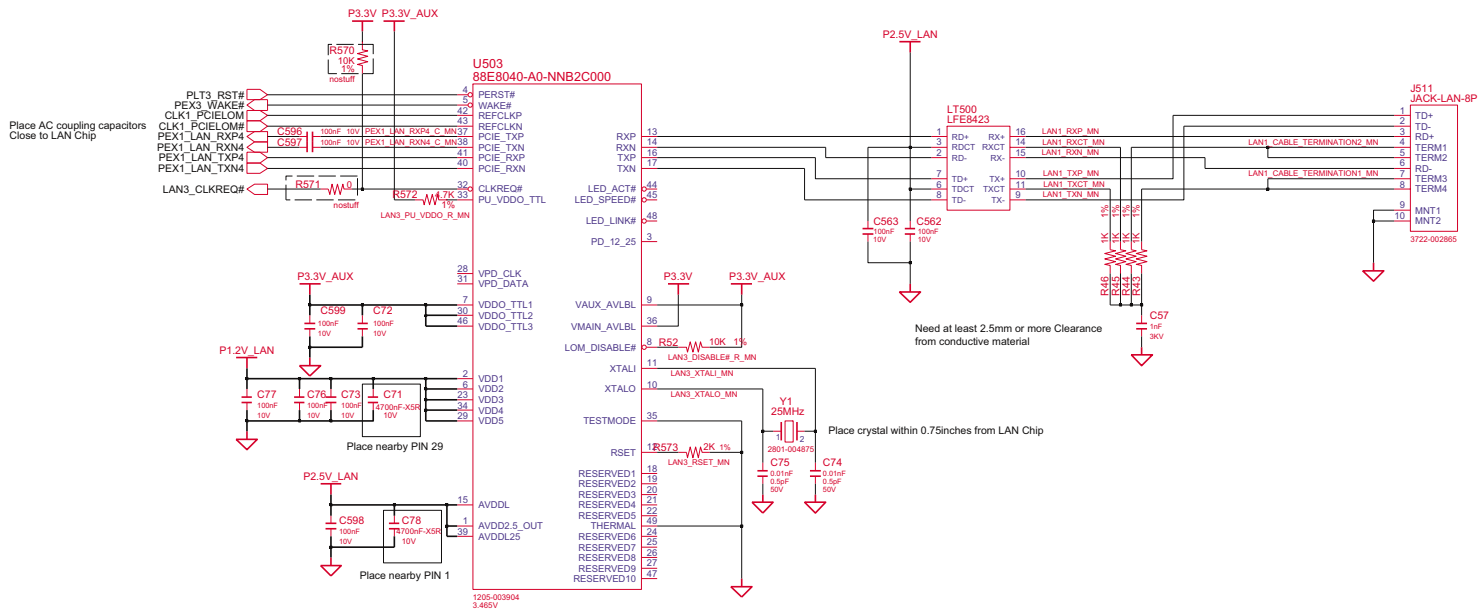
DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL HDA_CODEC	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd			
APPROVAL	S.J.Park	REV	1.0	AUDIO INPUT/OUTPUT		PART NO.
MOBILE CODE		LAST EST				BA41-xxxxxA
						PAGE
						31
						OF
						50

October 05, 2009 20:00:56 PM

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LAN Controller (88E8040)

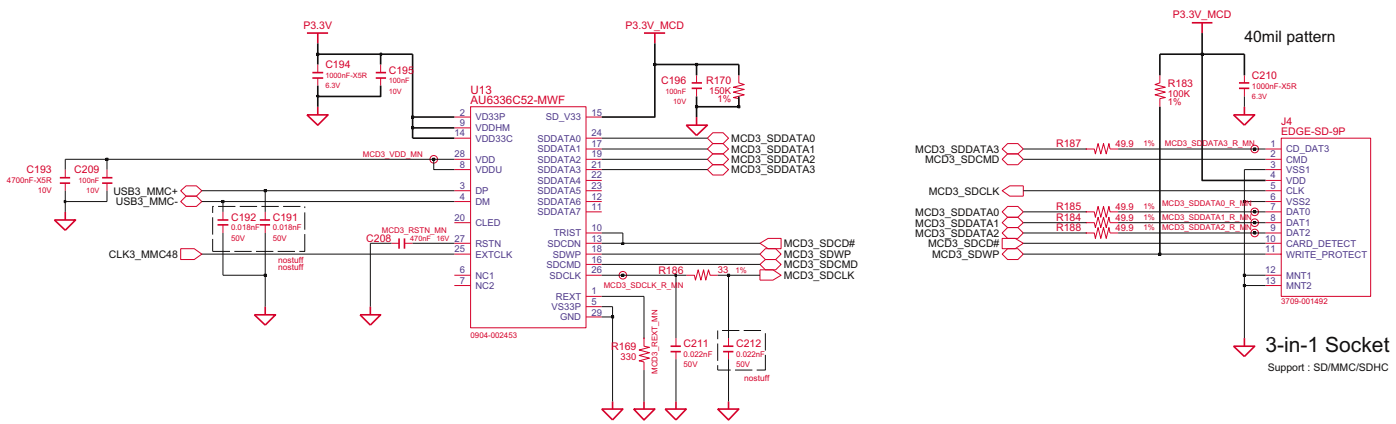


DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS	
CHECK	Hj.Kim	DEV. STEP	ADV2nd		LAN		
APPROVAL	S.J.Park	REV	1.0		LAN_MARVELL_8040	PART NO.	
MOBILE CODE		LAST EST				BA41-xxxxxA	
October 05, 2009 20:00:56 PM						PAGE	32 OF 50

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3 IN 1 CARD (GL827S)



DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd		MULTICARD	
APPROVAL	S.J.Park	REV	1.0		3 IN 1 CARD	PART NO.
MODEL CODE		LAST EST				BA41-xxxxxA

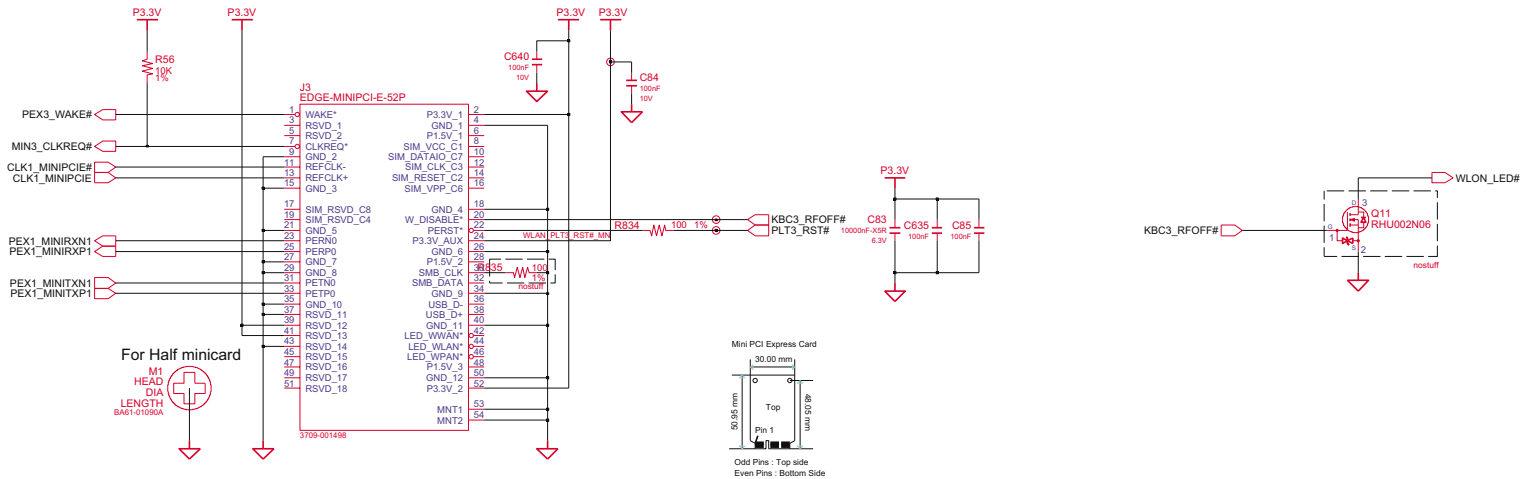
October 05, 2009 20:00:56 PM PAGE 33 OF 50

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Wireless LAN

WLAN, 4mm



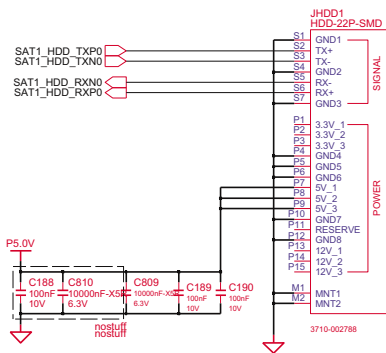
DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL MINI_PCIE_CONN		SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd	REV	WLAN		
APPROVAL	S.J.Park	REV	1.0	LAST EDIT	October 05, 2009 20:00:56 PM		PART NO. BA41-xxxxxA
MOBILE CODE					PAGE	34	OF 50

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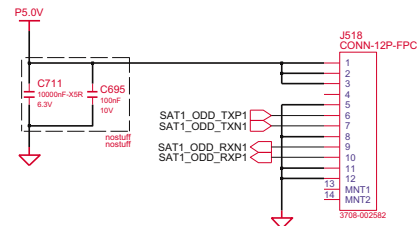
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SATA I/F CONN

SATA HDD CONN



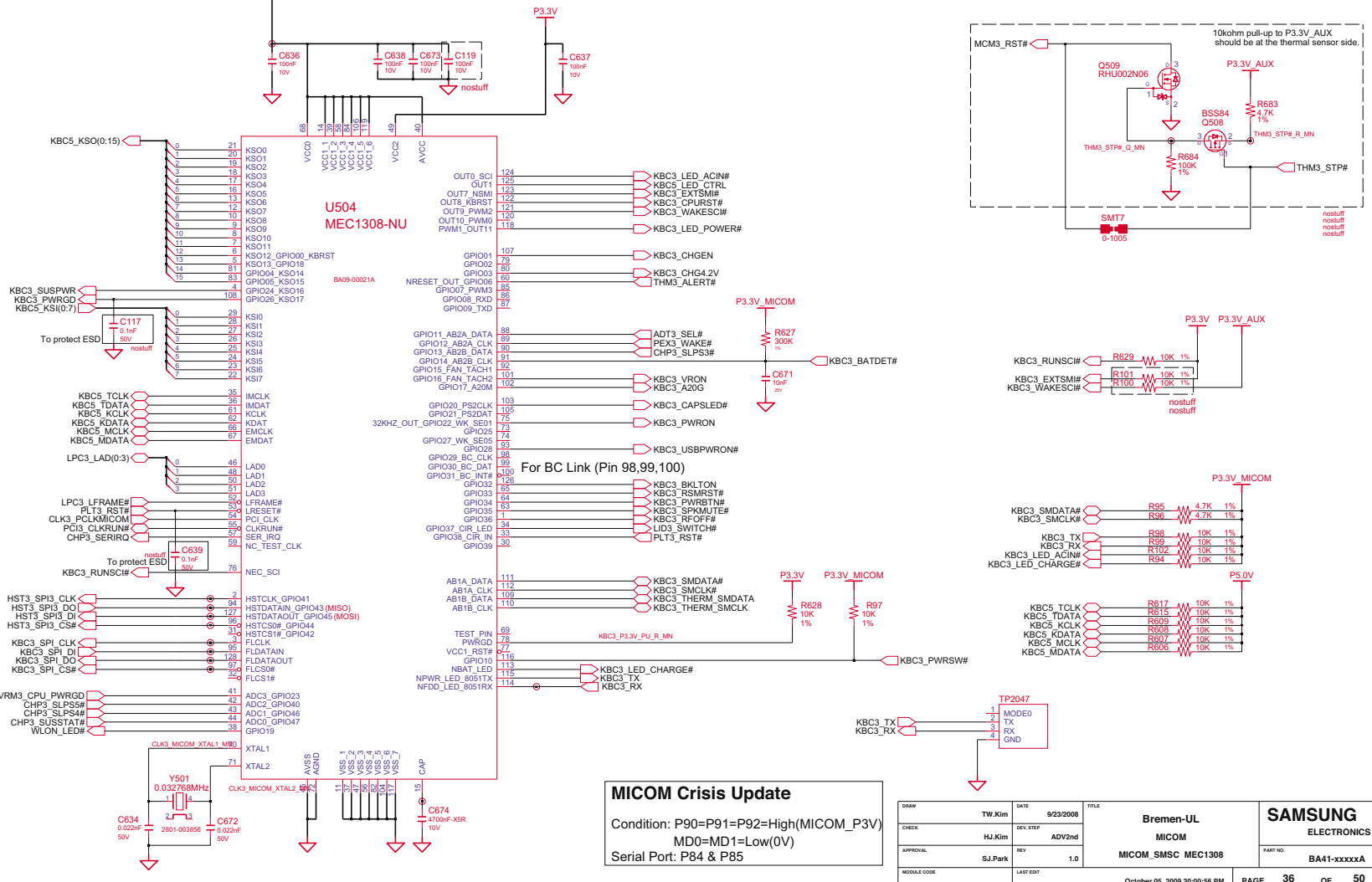
MAIN TO SUB SATA ODD CONN



DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL SATA_DEVICES	SAMSUNG ELECTRONICS	
CHECK	Hj.Kim	DEV. STEP	ADV2nd				
APPROVAL	S.J.Park	REV	1.0	HDD & ODD SUB CONNECTOR		PART NO.	
MODULE CODE		LAST EST				BA41-xxxxxA	
October 05, 2009 20:00:56 PM						PAGE	35 OF 50

MICOM_MEC1308

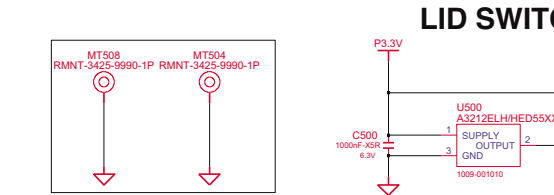
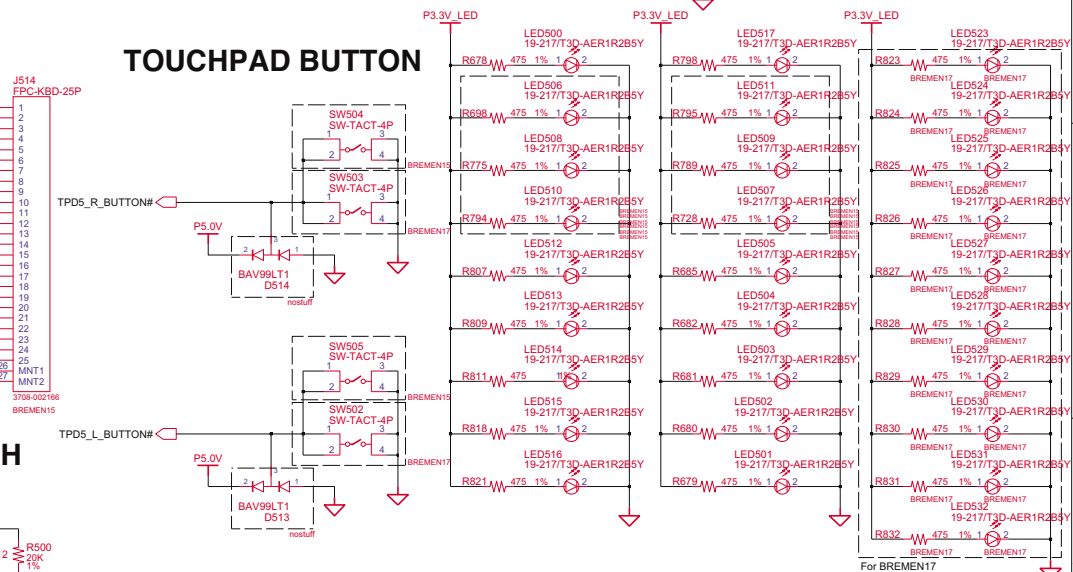
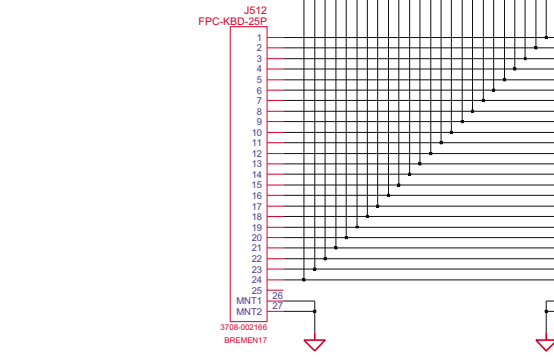
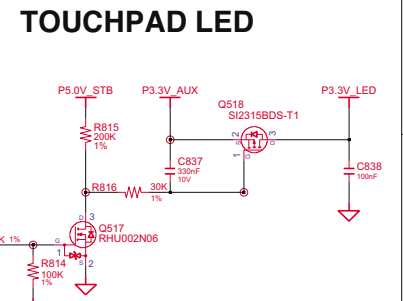
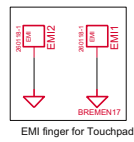
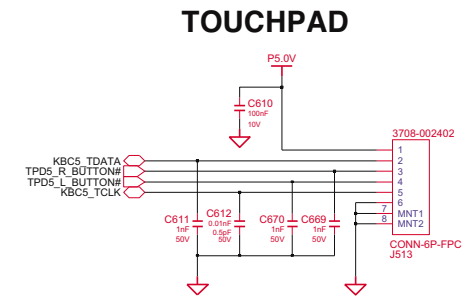
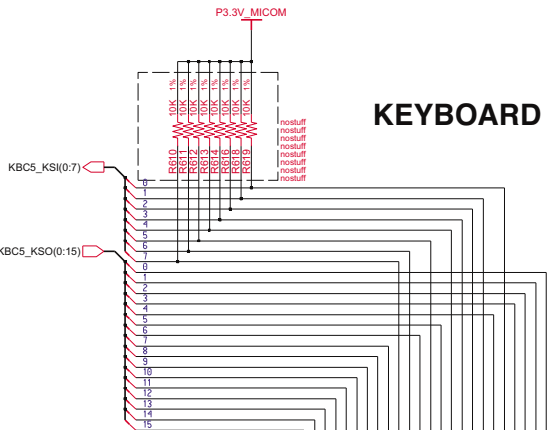
MICOM RESET



MICOM Crisis Update
 Condition: P90=P91=P92=High(MICOM_P3V)
 MD0=MD1=Low(0V)
 Serial Port: P84 & P85

DATE	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
DESIGN	H.J.Kim	DEV. STEP	ADV2nd	MICOM		
APPROVAL	S.J.Park	REV	1.0	MICOM_SMSC MEC1308	PART NO.	BA41-xxxxxA
MOBILE CODE		LAST EDIT			PAGE	36 OF 50
				October 05, 2009 20:00:56 PM		

Micom Glue Logic



Keyboard Mount(15", 17")

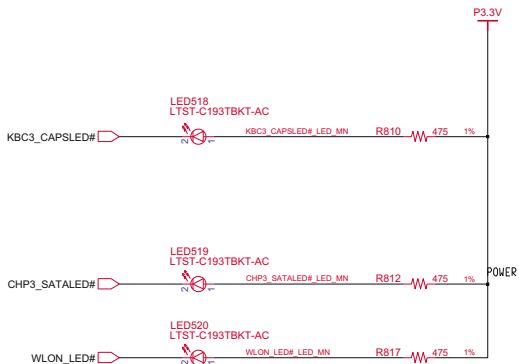
DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	
CHECK	Hj.Kim	DEV. STEP	ADV2nd	MICOM GLUE LOGIC		
APPROVAL	SJ.Park	REV	1.0	KBD & TOUCHPAD		
MIDDLE CODE	LAST EDIT			PART NO.	BA41-xxxxxA	
October 05, 2009 20:00:56 PM				PAGE	37	OF 50

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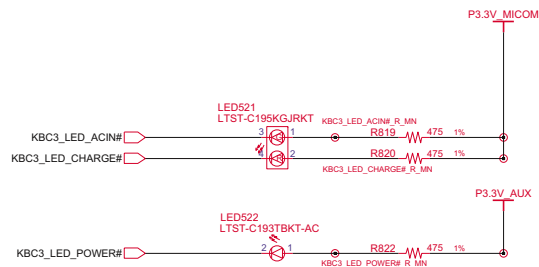
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LEDs

FUNCTION KEY LED



ADAPTERIN/CHARGING LED

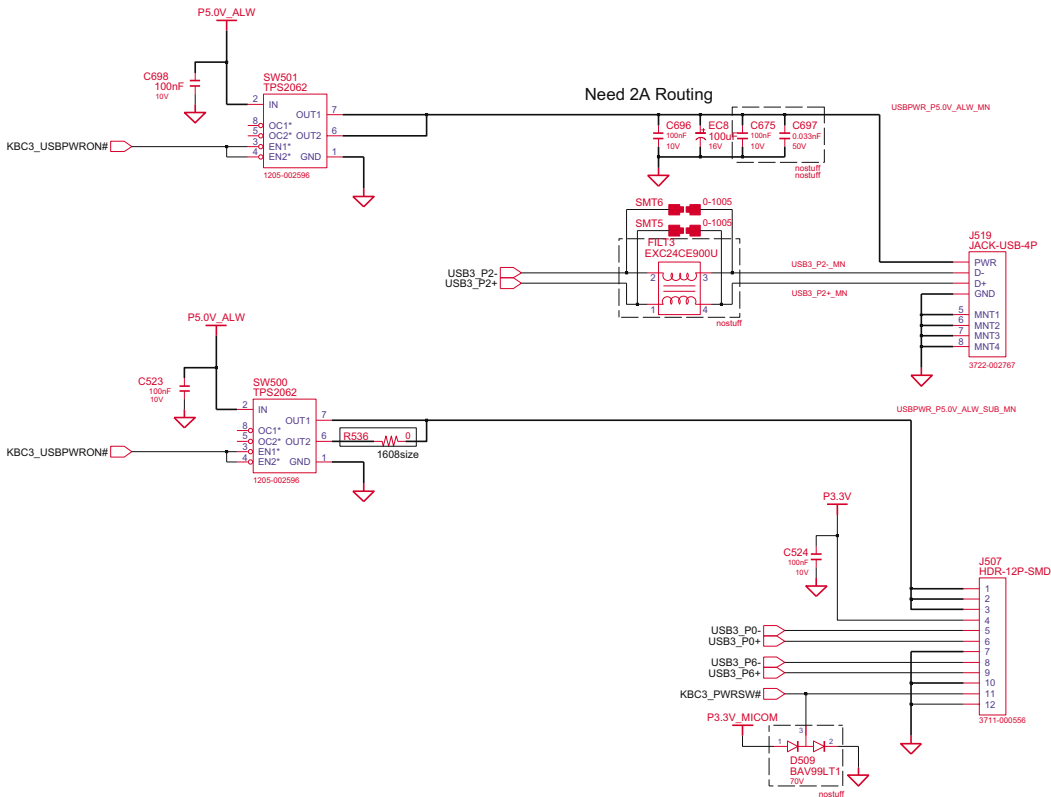


DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL LED_SWITCH	PART NO. BA41-xxxxxA			
CHECK	Hj.Kim	DEV. STEP	ADV2nd						
APPROVAL	S.J.Park	REV	1.0		LED_SWITCH				
MODULE CODE		LAST EST							
October 05, 2009 20:00:56 PM						PAGE	38	OF	50

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USB Single connector



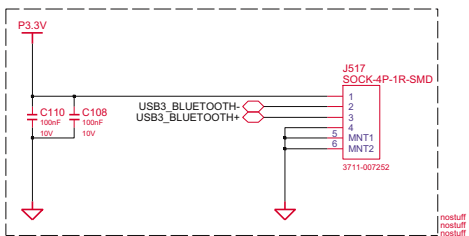
DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS	
CHECK	Hj.Kim	DEV. STEP	ADV2nd		USB_CONN		
APPROVAL	S.J.Park	REV	1.0		USB	PART NO.	
MOBILE CODE		LAST EST				BA41-xxxxxA	
October 05, 2009 20:00:56 PM						PAGE	39
						OF	50

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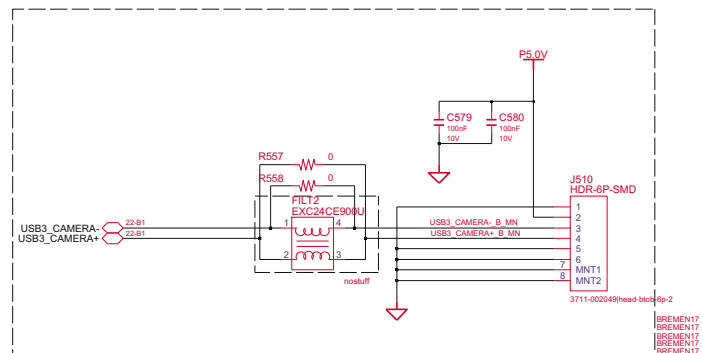
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USB I/F Devices

Bluetooth Interface

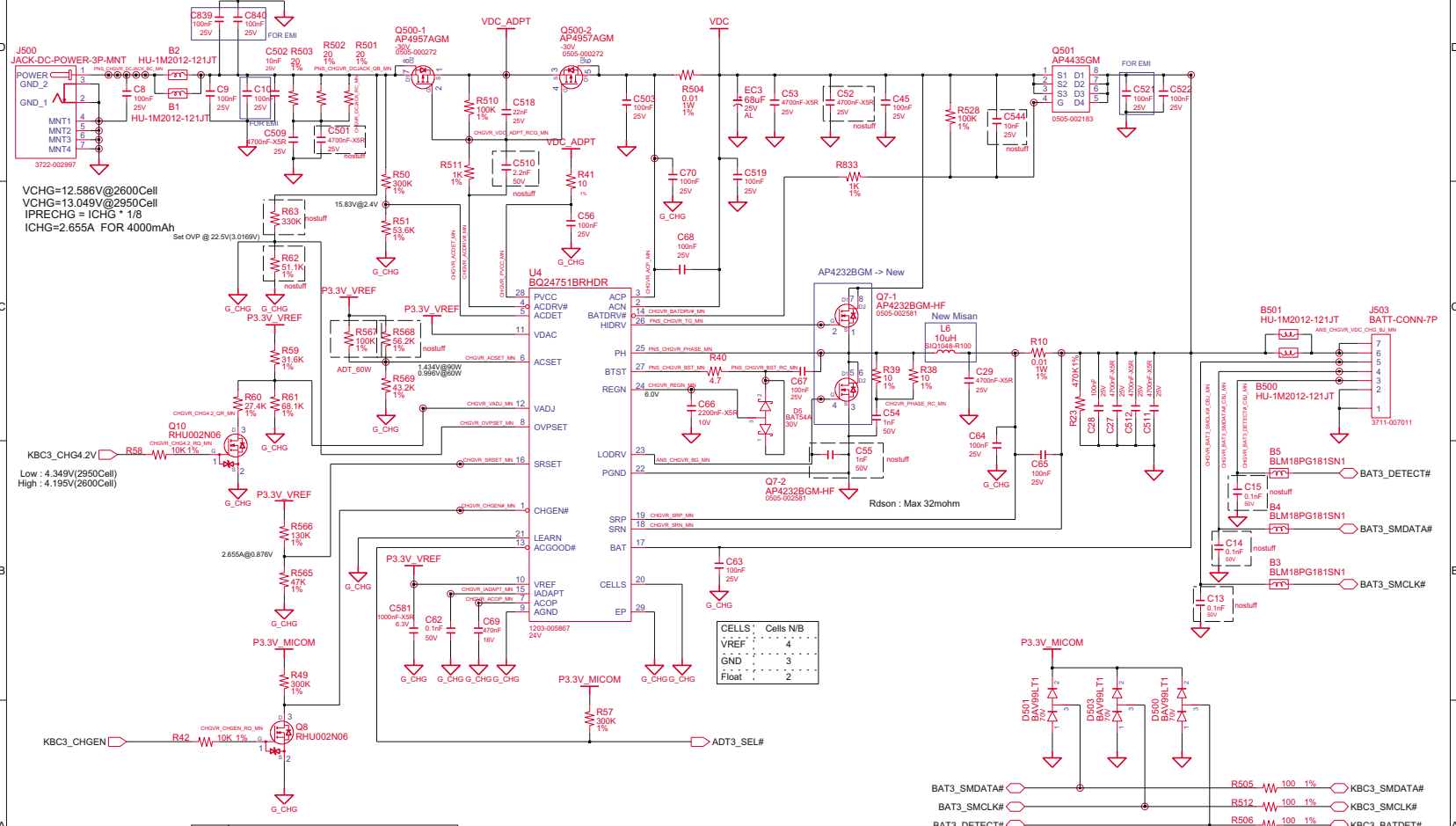


CAMERA



DESIGN	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL USB_DEVICES	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd			
APPROVAL	S.J.Park	REV	1.0		BLUETOOTH & CAMERA	PART NO.
MOBILE CODE		LAST EST				BA41-xxxxxA
October 05, 2009 20:00:56 PM						PAGE 40 OF 50

CHARGE & POWER MANAGEMENT



VCHG=12.586V@2600Cell
 VCHG=13.049V@2950Cell
 IPRECHG = ICHG * 1/8
 ICHG=2.655A FOR 4000mAh

Set OVP @ 22.5V (3.0189V)

KBC3_CHG4.2V
 Low : 4.349V (2950Cell)
 High : 4.195V (2600Cell)

2.655A@876V

CELLS :	Cells N/B
VREF :	4
GND :	3
Float :	2

Adapter configuration				
	60W / 3.0A / 94.9%	90W / 4.36A / 92.3%		
Value	SEC Code	Value	SEC Code	
Rtop	100K	2007-007107	56.2K	2007-008133
Rbot	43.2K	2007-007108	43.2K	2007-007108

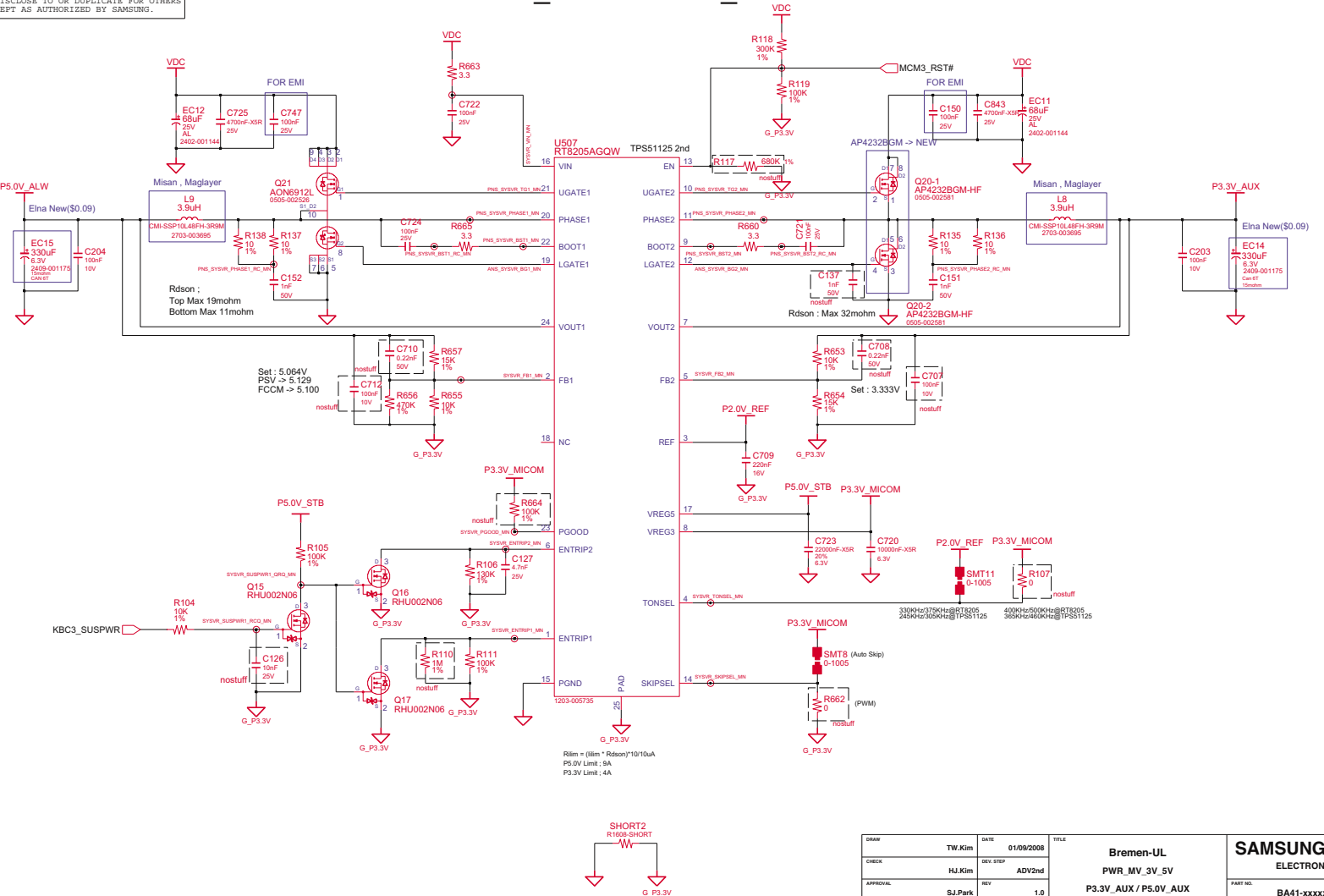


DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG
CHECK	HJ.Kim	REV. STEP	ADV2nd		Charger	
APPROVAL	SJ.Park	REV	1.0		CHARGER (BQ24751BRHDR)	PART NO.
MODULE CODE	undefined	LAST EDIT				BA41-xxxxxA

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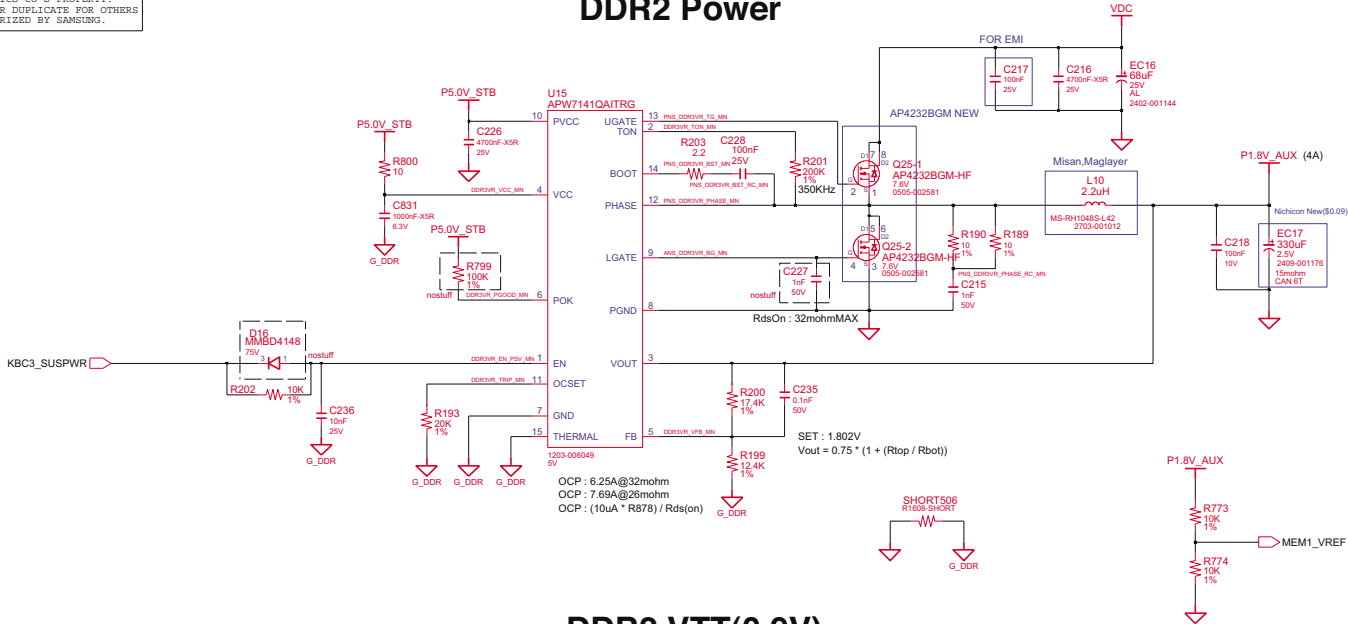
P3.3V_AUX & P5.0V_ALW



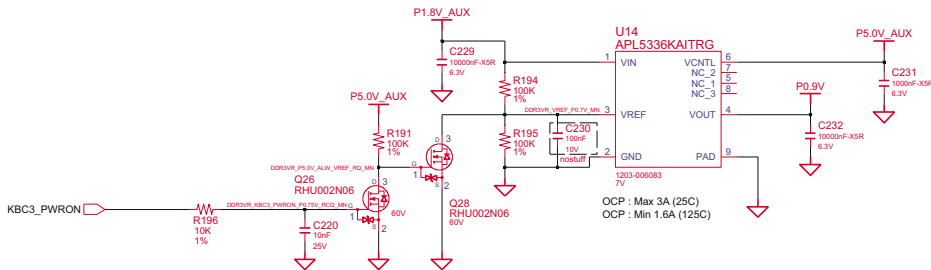
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DDR2 Power



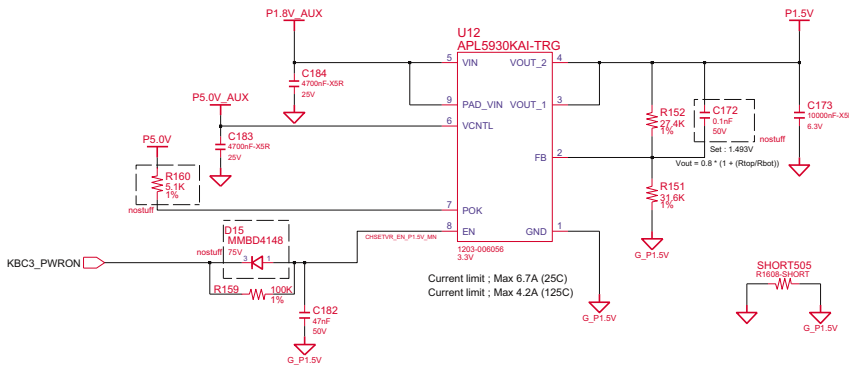
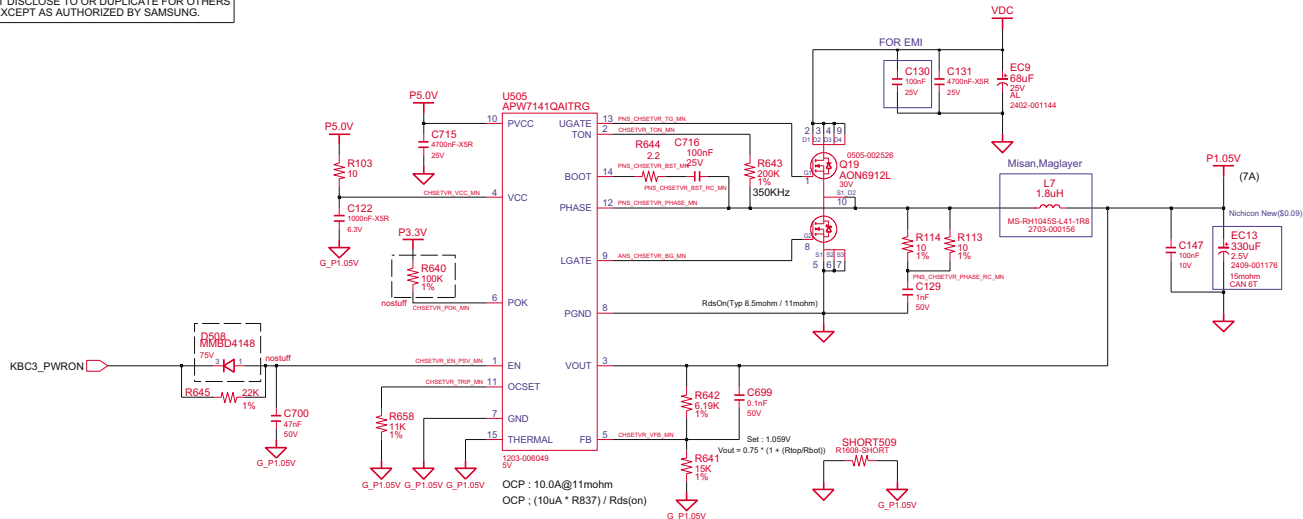
DDR2 VTT(0.9V)



DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd	PWR_MEMORY	PART NO.	
APPROVAL	S.J.Park	REV	1.0	DDR2 POWER	BA41-xxxxxA	
MODULE CODE	undefined	LAST EST				
				October 05, 2009 20:00:56 PM	PAGE	43 OF 50

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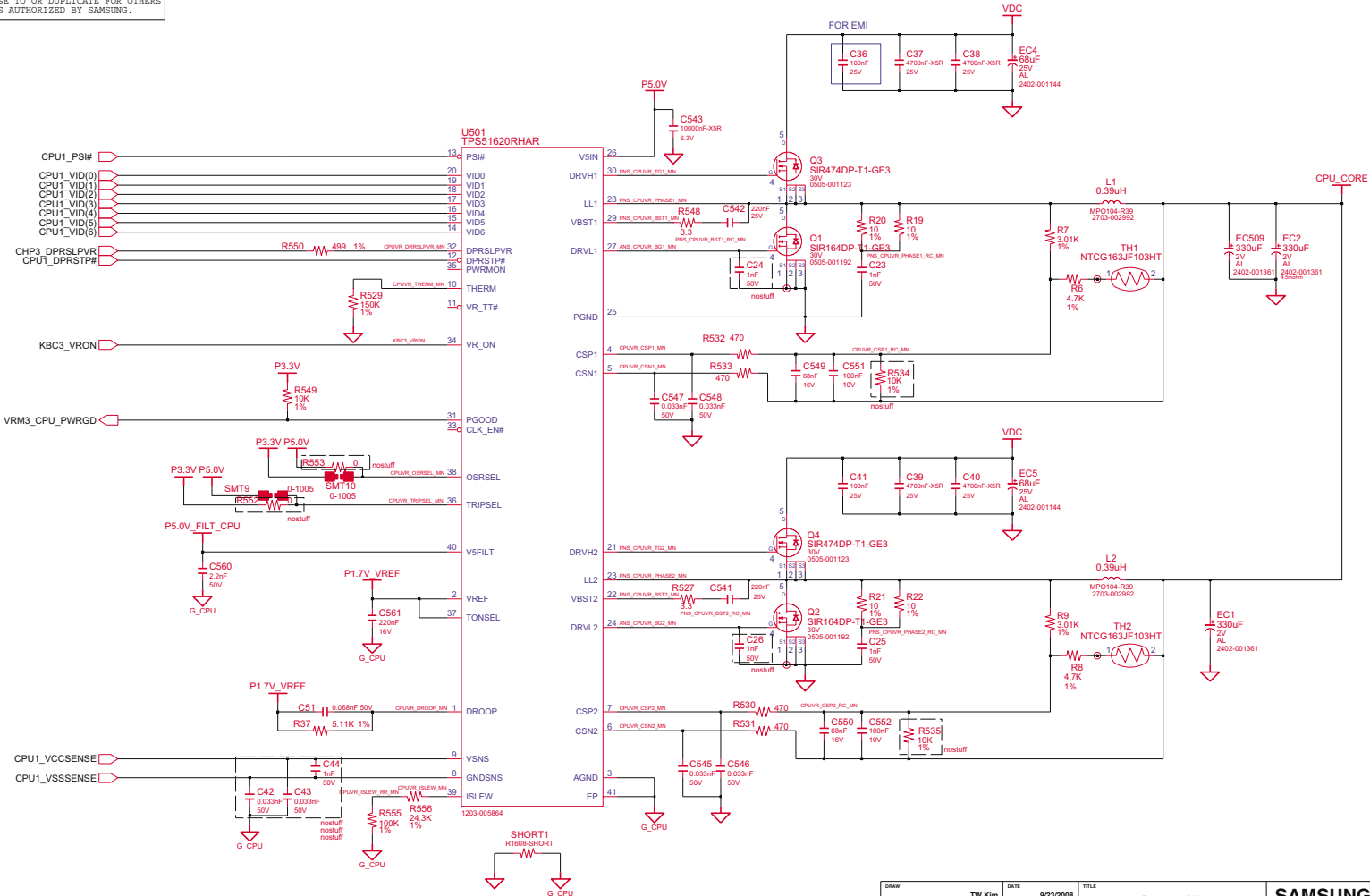
CHIPSET POWER (P1.05V & P1.5V)



DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	
CHECK	HJ.Kim	DEV. STEP	ADV2nd		PWR_MV_Cantiga	
APPROVAL	S.J.Park	REV	1.0		P1.5V_AUX, P1.05V	
MODULE CODE	undefined	LAST EDIT			PART NO.	BA41-xxxxxA
					October 05, 2009 20:00:56 PM	PAGE 44 OF 50

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CPU VRM [TI IMVP6+]



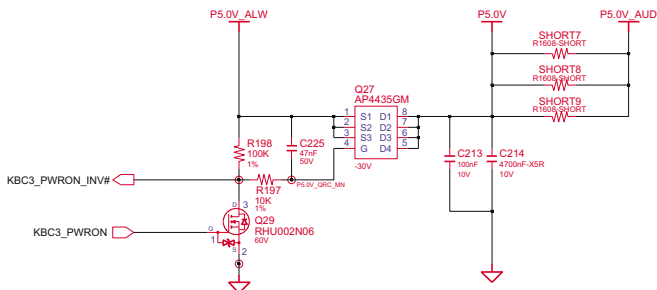
DATE	TITLE	DATE	TITLE
9/23/2008	Bremen-UL	9/23/2008	Bremen-UL
DEV. STEP	PWR_CPU_MV_TPS51620	DEV. STEP	PWR_CPU_MV_TPS51620
ADV2nd	CPU1 VRM (IMVP6+)	ADV2nd	CPU1 VRM (IMVP6+)
REV	1.0	REV	1.0
LAST EDIT		LAST EDIT	
MOBILE CODE	undefined	MOBILE CODE	undefined
DATE	October 05, 2009 20:00:56 PM	DATE	October 05, 2009 20:00:56 PM
PAGE	45	PAGE	45
OF	50	OF	50

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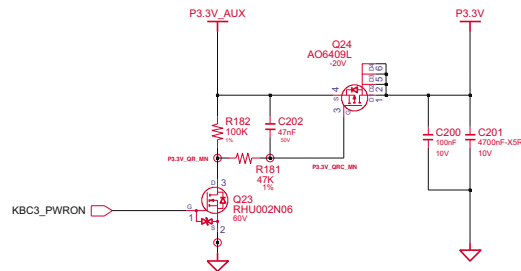
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Switched Power

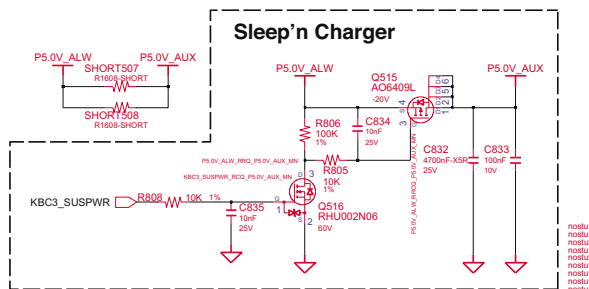
Switched Power On (P5.0V)



Switched Power On (P3.3V)



Sleep'n Charger

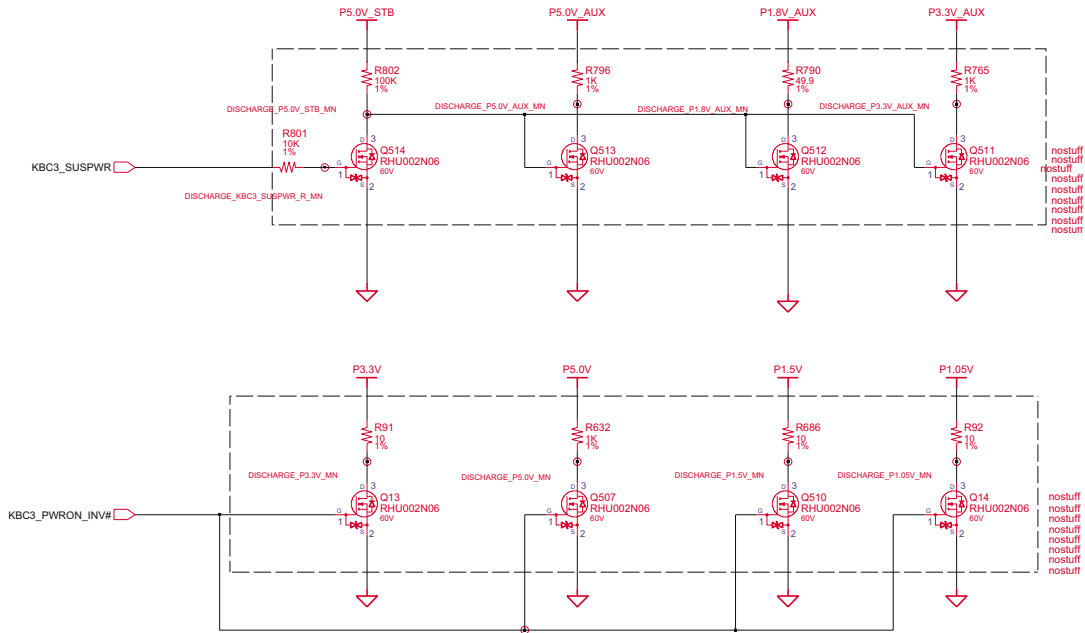


DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd		PWR_MV_SWITCHED	
APPROVAL	S.J.Park	REV	1.0		SWITCHED POWER	PART NO. BA41-xxxxxA
MOBILE CODE		LAST EST				PAGE 46 OF 50

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POWER DISCHARGER

This page will be deleted in PV stage.

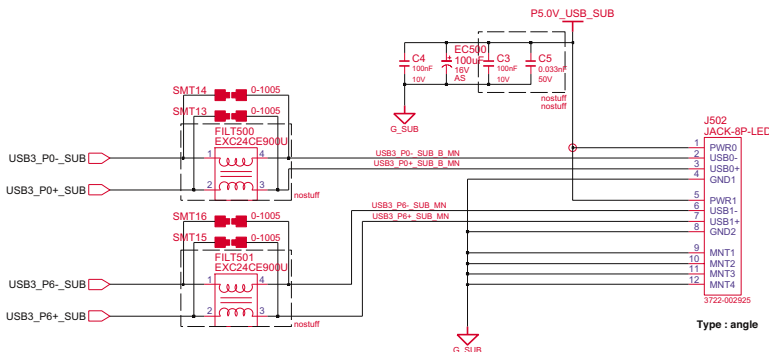


DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL		SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd	PWR_MV_DISCHARGER		PART NO.	
APPROVAL	S.J.Park	REV	1.0	DISCHARGING LOGIC		BA41-xxxxxA	
MODULE CODE	undefined	LAST EST		October 05, 2009 20:00:56 PM		PAGE	47 OF 50

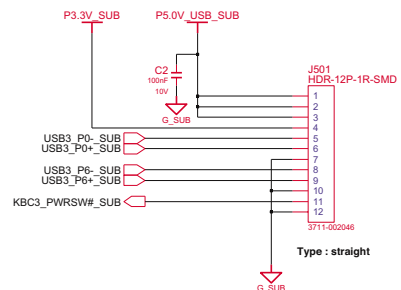
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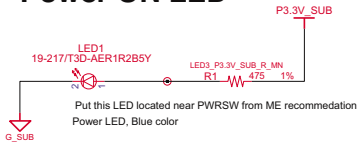
2 USB PORT & POWER S/W SUB B'D



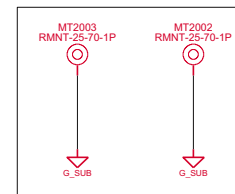
SUB TO MAIN USB CONN



Power ON LED



Power Button



USB sub board mount hole

DESIGN	TW.Kim	DATE	8/22/2009	TITLE	Bremen-UL SUB BOARD1	SAMSUNG ELECTRONICS	
CHECK	HJ.Kim	DEV. STEP	ADV2nd	REV	USB SUB BOARD		
APPROVAL	SJ.Park	REV	1.0	LAST EDIT		PART NO. BA41-xxxxxA	
MODEL CODE						October 05, 2009 20:00:56 PM	
						PAGE	48
						OF	

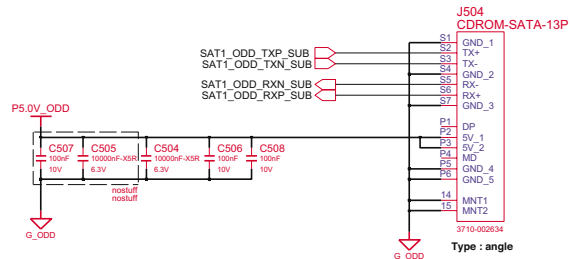
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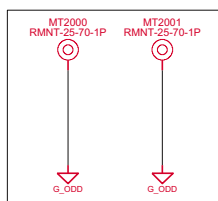
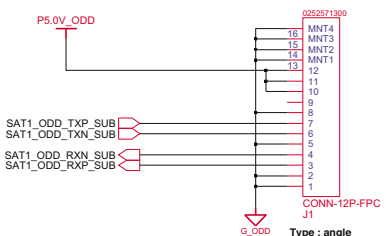
SATA ODD SUBBOARD

BATTERY SUBBOARD (17")

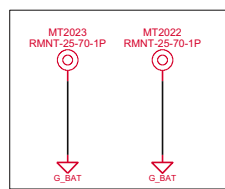
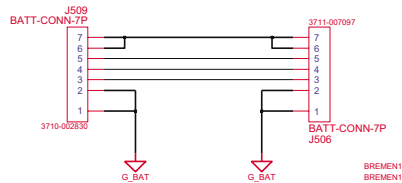
SATA ODD CONN



SUB TO MAIN SATA ODD CONN



ODD sub board mount hole



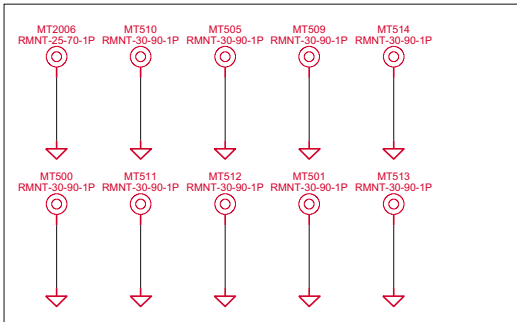
battery sub board mount hole

DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL SUB BOARD2	SAMSUNG ELECTRONICS
CHECK	Hj.Kim	DEV. STEP	ADV2nd			
APPROVAL	S.J.Park	REV	1.0		SATA ODD SUB BOARD	PART NO.
MOBILE CODE	undefined	LAST EST				BA41-xxxxxA
				October 05, 2009 20:00:56 PM	PAGE	49 OF 50

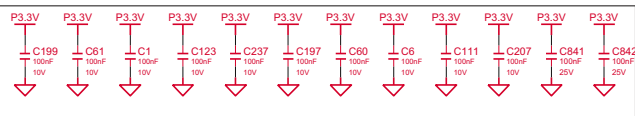
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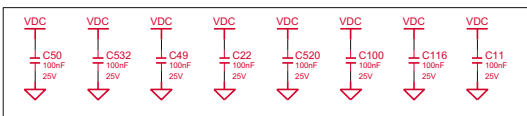
Mainboard Mount



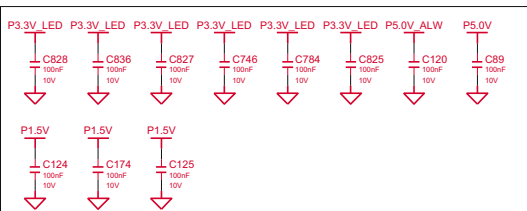
(30.90) x 7, (25.70) x 1



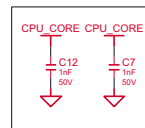
Add for EMC (5th Layer), 2008.11.19



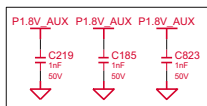
Add for EMC (Bottom), 2008.11.19



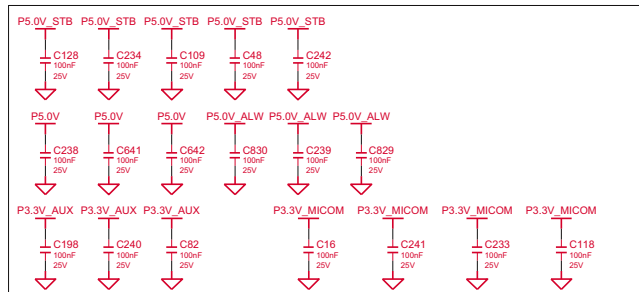
Add for EMC (Bottom), 2009.09.07



Add for EMC (Top), 2008.11.19



Add for EMC (Bottom), 2008.11.19



Add for EMC (Bottom), 2009.01.28

DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL ETC		SAMSUNG ELECTRONICS
CHECK	H.J.Kim	REV. STEP	ADV2nd	EMC CAP & Mount hole		PART NO.	
APPROVAL	S.J.Park	REV	1.0				BA41-xxxxxA
MODULE CODE		LAST EDIT					
				October 05, 2009 20:00:56 PM		PAGE	50 OF 50