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HAINAN

CPU : Intel Yonah -2M
 Chip Set : Intel Calistoga & ICH7-M
 Remarks : Mobility Platform

Model Name : HAINAN
 PBA Name : MAIN
 PCB Code : BA41-00574A
 Dev. Step : PR
 Revision : 1.0
 T.R. Date : 2005.11.28

DRAW	CHECK	APPROVAL
KI IM	SS BAIK	KK BIN

Owner : SEC Mobile R & D Signature : X

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DRAW	KI IM	DATE	9/15/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PV	COVER	PART NO.	
APPROVAL	KK BIN	REV	1.0		BA41-00574A	
MODULE CODE		LAST EDIT	September 15, 2005 10:33:16 PM	PAGE	1 OF 55	

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus LAN	AD25 AD21	0 1	E, F, G G
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308-1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail (off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_DTV	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_ALWS	3.3V power rail (Always On)
P2.5V_ALWS	2.5V power rail (Always On)
P1.2V_ALWS	1.2V power rail (Always On)

I C / SMB Address

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A4h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0,1	SYSTEM PORT A, B
2	SYSTEM PORT C
3	DMB
4	BLUETOOTH
5	DOCKING STATION
6	MINI PCIE EXPRESS CARD
7	EXPRESS CARD

System Power States

- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH7-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 0 1 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 0	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 0 1 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
1 0 0 0 0 0 0	1.0000 V	1 0 0 1 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active: DPRSLPVR 0, DPRSTP* 1, PSI2* 0 or 1
 Deeper Slip: DPRSLPVR 1, DPRSTP* 0, PSI2* 0 or 1

11111111 - 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

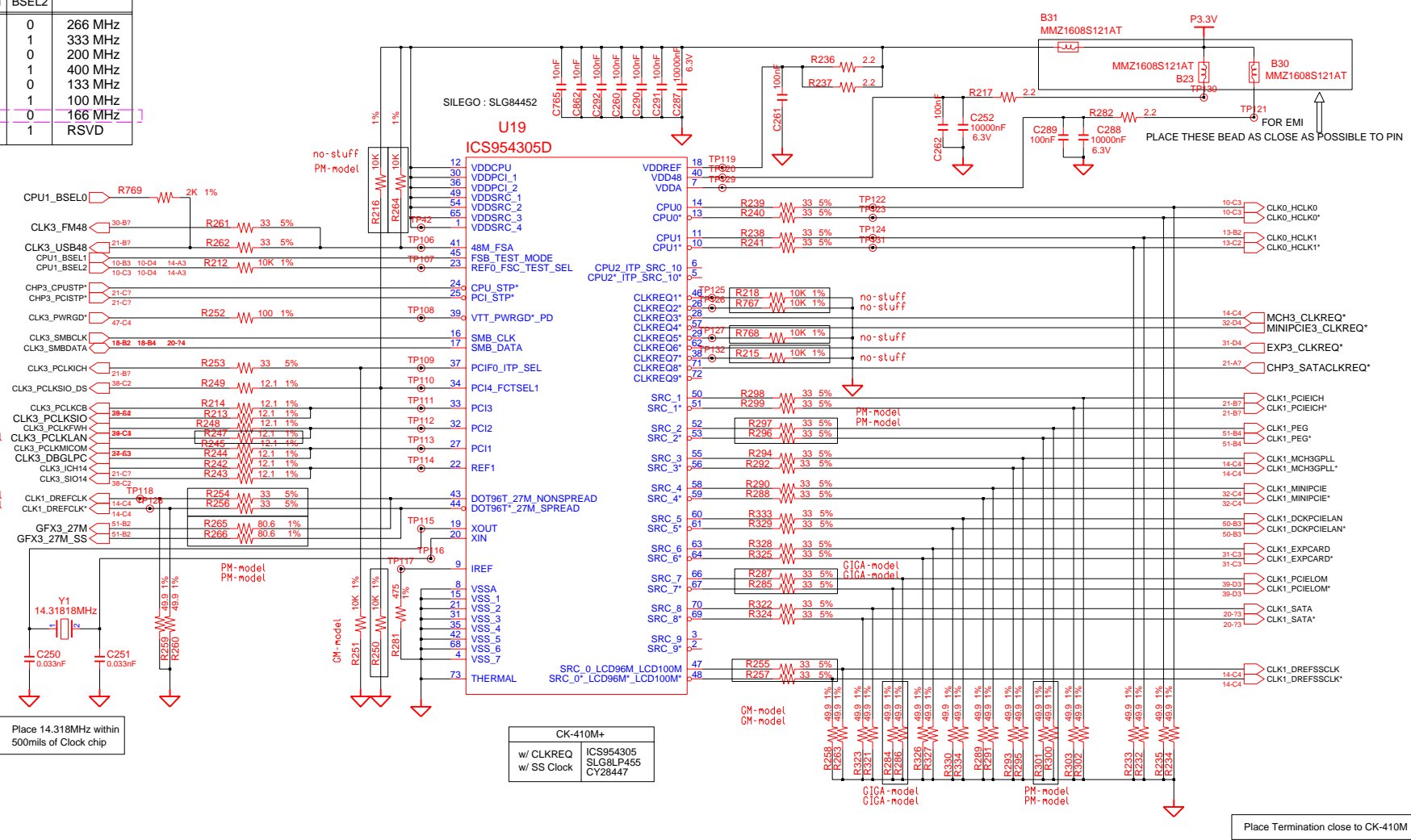
DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV		MAIN	
APPROVAL	KK BIN	REV	1.0		BOARD INFORMATION	PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	7	OF 55

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PCI4_FCTSEL1(PIN34)	PIN 43, 44	PIN 47, 48
0	DOT96	LCD96/100
1	27MHZ	SRC0

CPU	FSA	FSB	FSC	HOST CLK
	BSEL0	BSEL1	BSEL2	
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD



Place 14.318MHz within 500mils of Clock chip

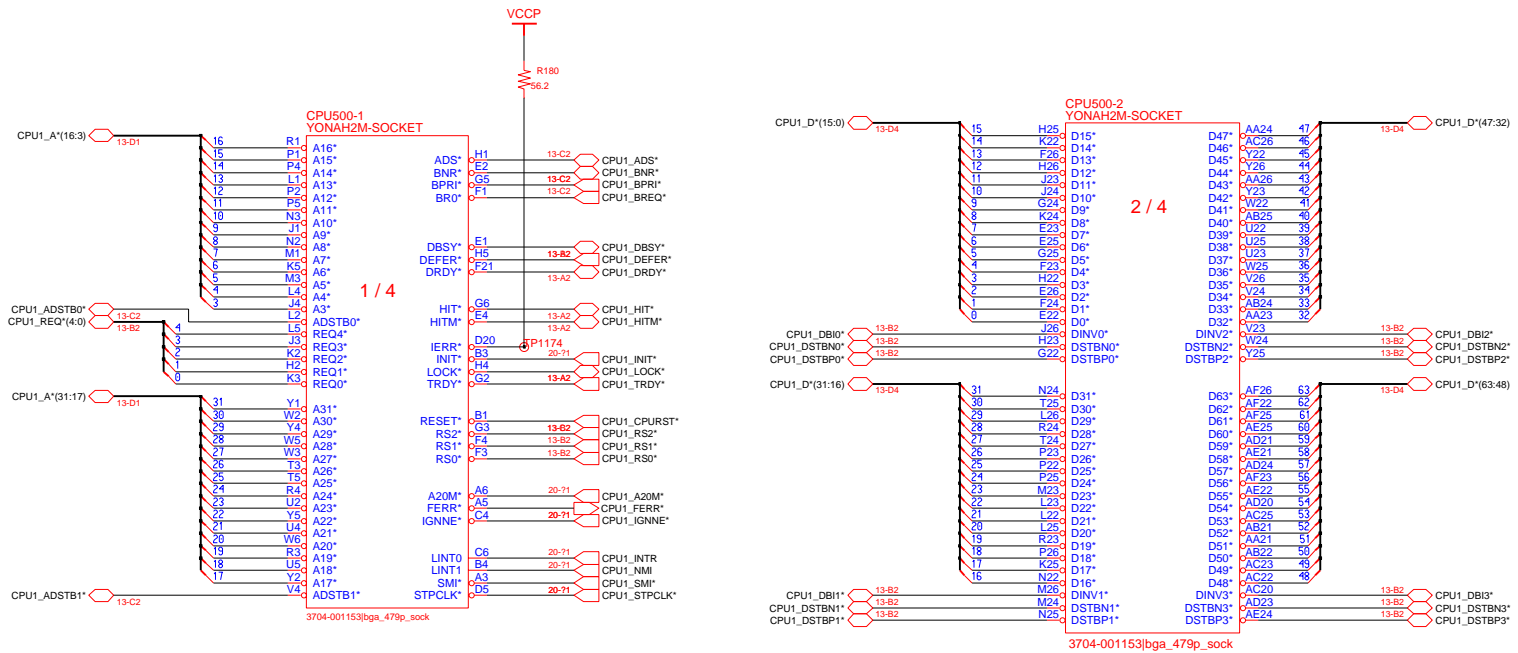
CK-410M+
w/ CLKREQ ICS954305
w/ SS Clock SLG84452
CY28447

Place Termination close to CK-410M

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	SS BAIK	DEV. STEP	DV	REV	1.0	
APPROVAL	KK BIN	LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	8	OF 55

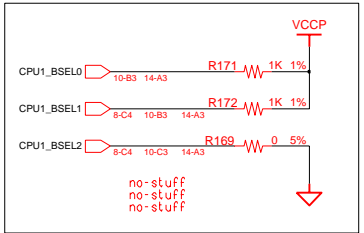
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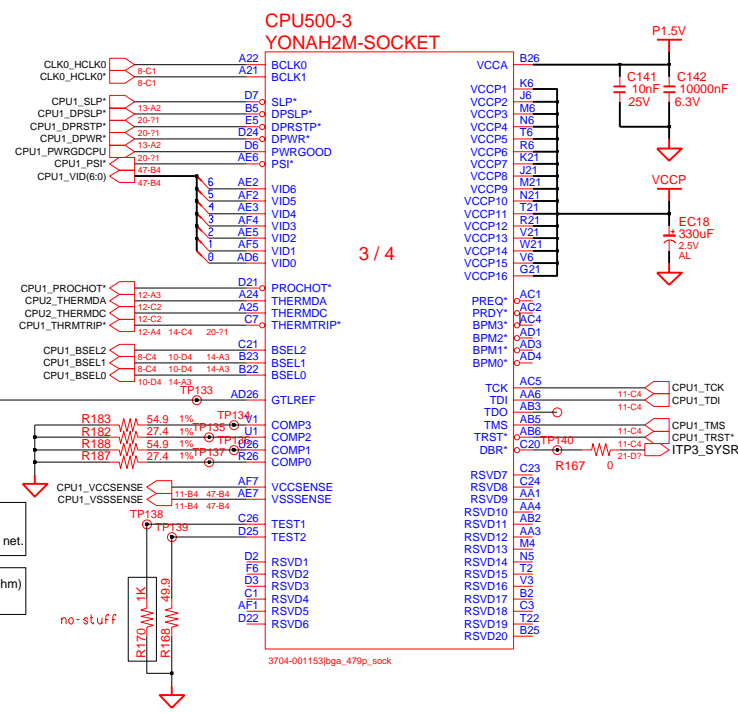


DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	YONAH CPU (1/3)		PART NO. BA41-*****A
MODULE CODE		LAST EDIT		July 19, 2005 8:53:48 AM	PAGE	9 OF 55

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FSB 533 MHz	Pull-up	Pull-down
FSB 667 MHz	BSEL0, BSEL1	BSEL1, BSEL2 BSEL2



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0.2(COMP1.3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

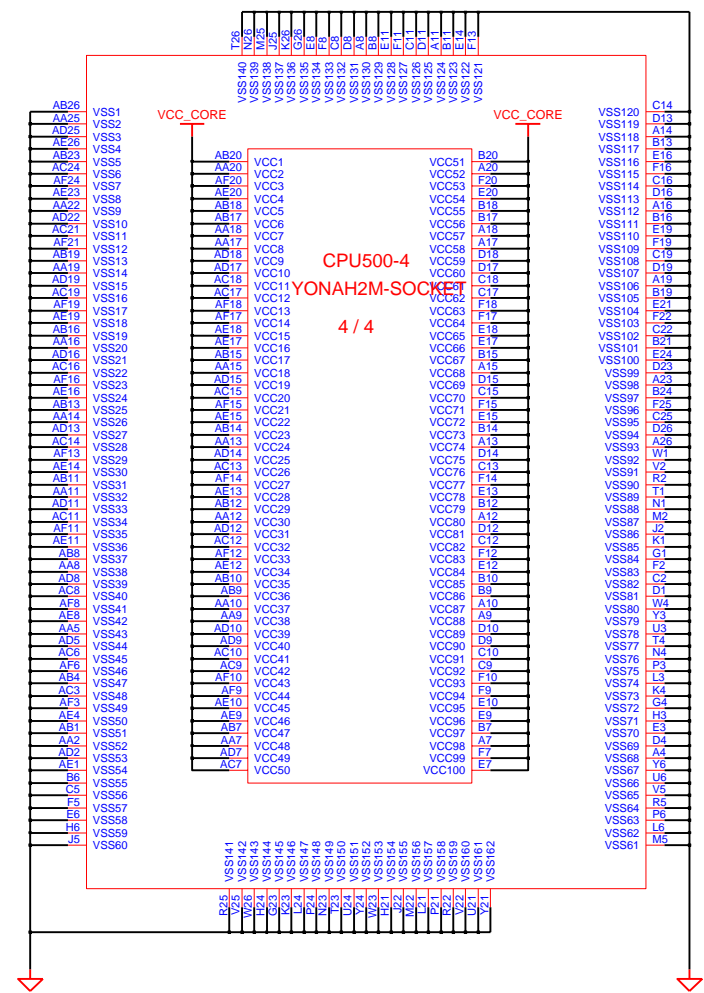
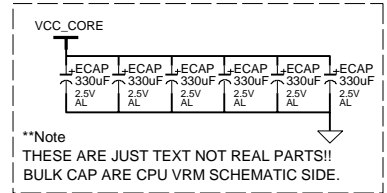
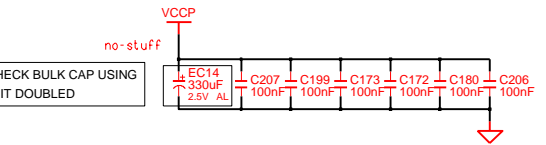
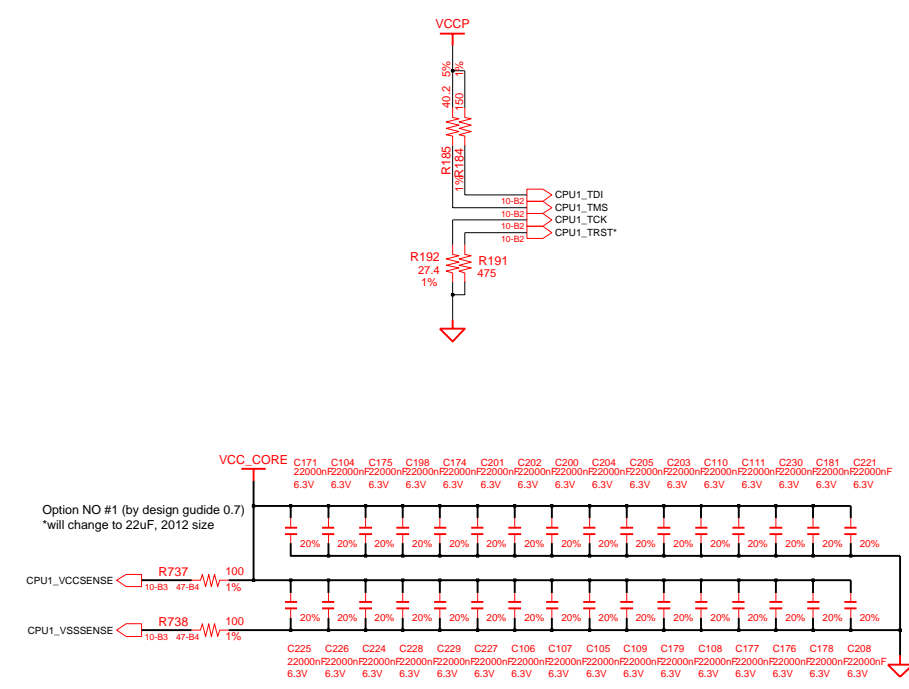
CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 0 1	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 0	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 0 1	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 0 1	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				***11111111** : 0V power good asserted.	

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	YONAH CPU(2/3)	PART NO.	BA41-*****A
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DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN MAIN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	YONAH CPU(3/3)		
APPROVAL	KK BIN	REV	1.0	July 19, 2005 8:53:48 AM		PART NO. BA41-*****A
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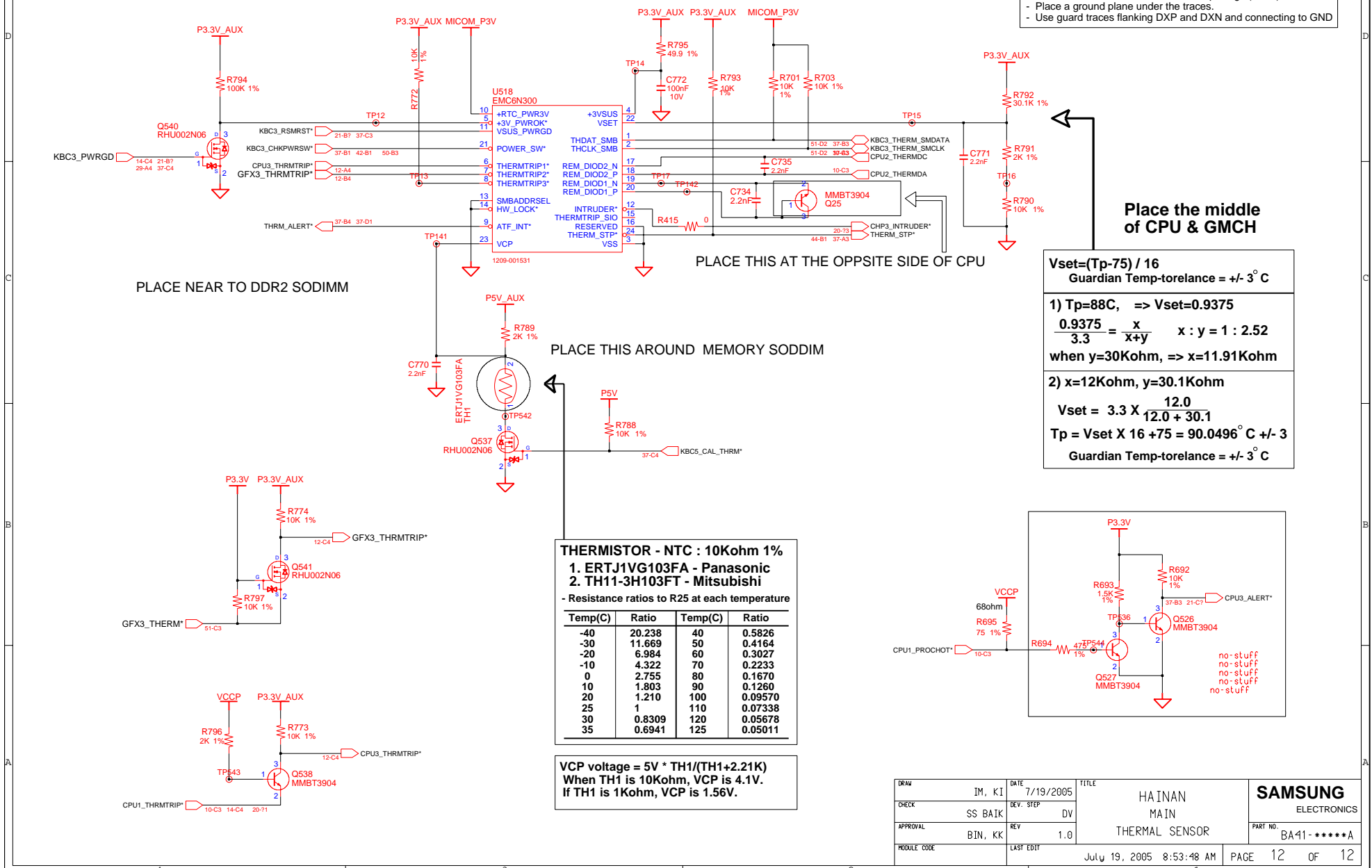
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CPU / DDR2 Thermal Sensor

Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus).
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND



PLACE NEAR TO DDR2 SODIMM

PLACE THIS AT THE OPPOSITE SIDE OF CPU

PLACE THIS AROUND MEMORY SODDIM

Place the middle of CPU & GMCH

Vset=(Tp-75) / 16
Guardian Temp-tolerance = +/- 3° C

1) Tp=88C, => Vset=0.9375

$$\frac{0.9375}{3.3} = \frac{x}{x+y} \quad x : y = 1 : 2.52$$

when y=30Kohm, => x=11.91Kohm

2) x=12Kohm, y=30.1Kohm

$$Vset = 3.3 \times \frac{12.0}{12.0 + 30.1}$$

Tp = Vset X 16 + 75 = 90.0496° C +/- 3° C
Guardian Temp-tolerance = +/- 3° C

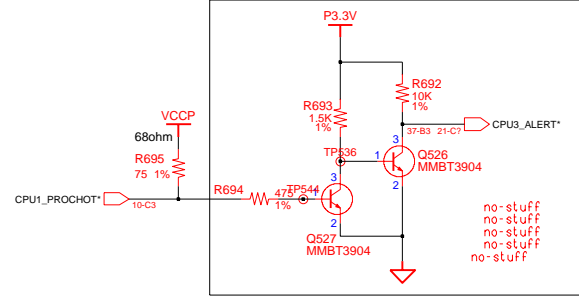
THERMISTOR - NTC : 10Kohm 1%

1. ERTJ1VG103FA - Panasonic
2. TH11-3H103FT - Mitsubishi

- Resistance ratios to R25 at each temperature

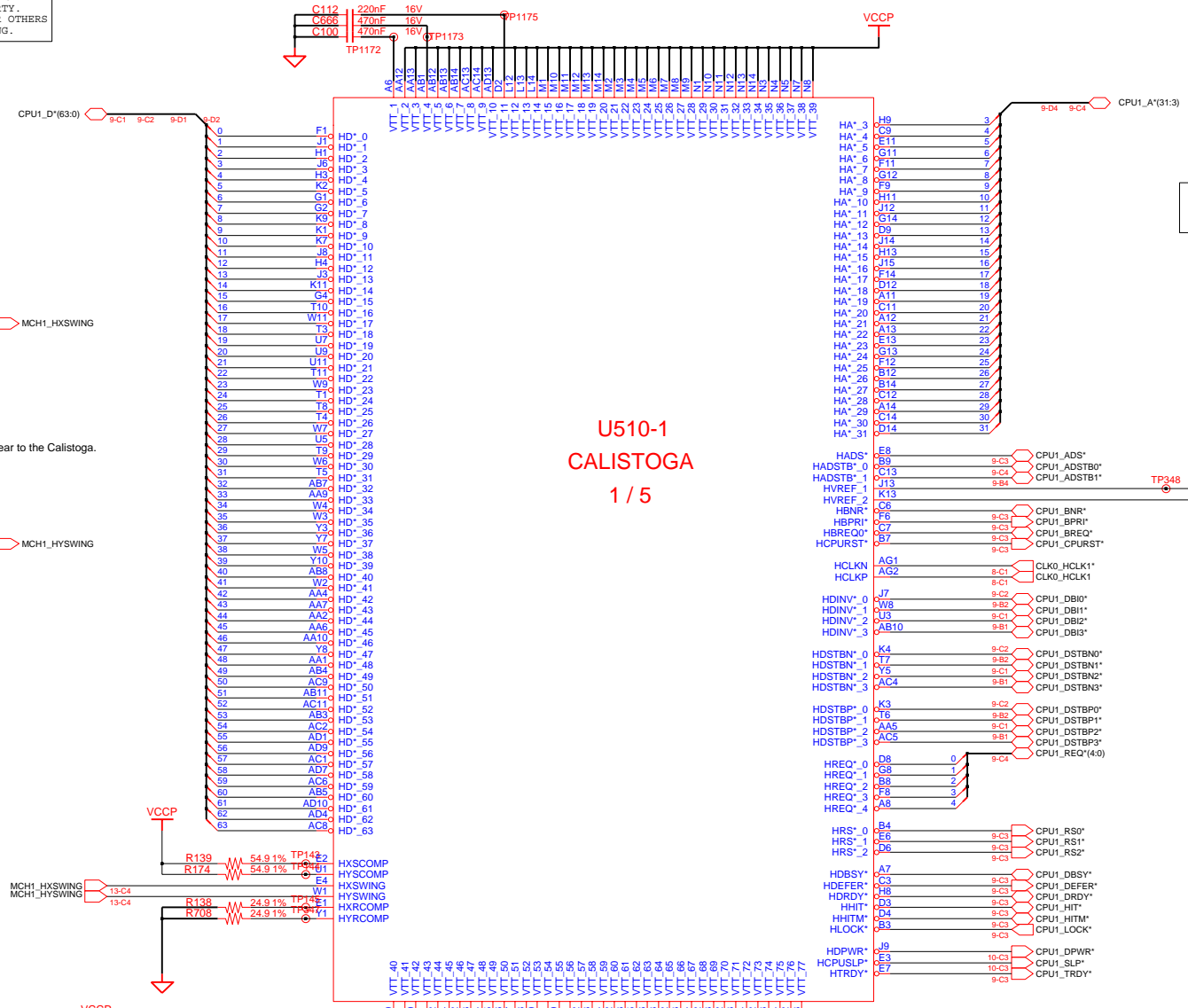
Temp(C)	Ratio	Temp(C)	Ratio
-40	20.238	40	0.5826
-30	11.669	50	0.4164
-20	6.984	60	0.3027
-10	4.322	70	0.2233
0	2.755	80	0.1670
10	1.803	90	0.1260
20	1.210	100	0.09570
25	1	110	0.07338
30	0.8309	120	0.05678
35	0.6941	125	0.05011

VCP voltage = 5V * TH1/(TH1+2.21K)
When TH1 is 10Kohm, VCP is 4.1V.
If TH1 is 1Kohm, VCP is 1.56V.



DRAW	IM, KI	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	THERMAL SENSOR	PART NO.	BA41 - *****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	12	OF 12

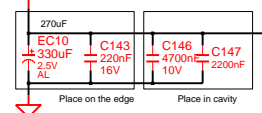
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External GFx model : PM
 Internal GFx model : GM

Place near to the Calistoga.

Place near to the Calistoga.

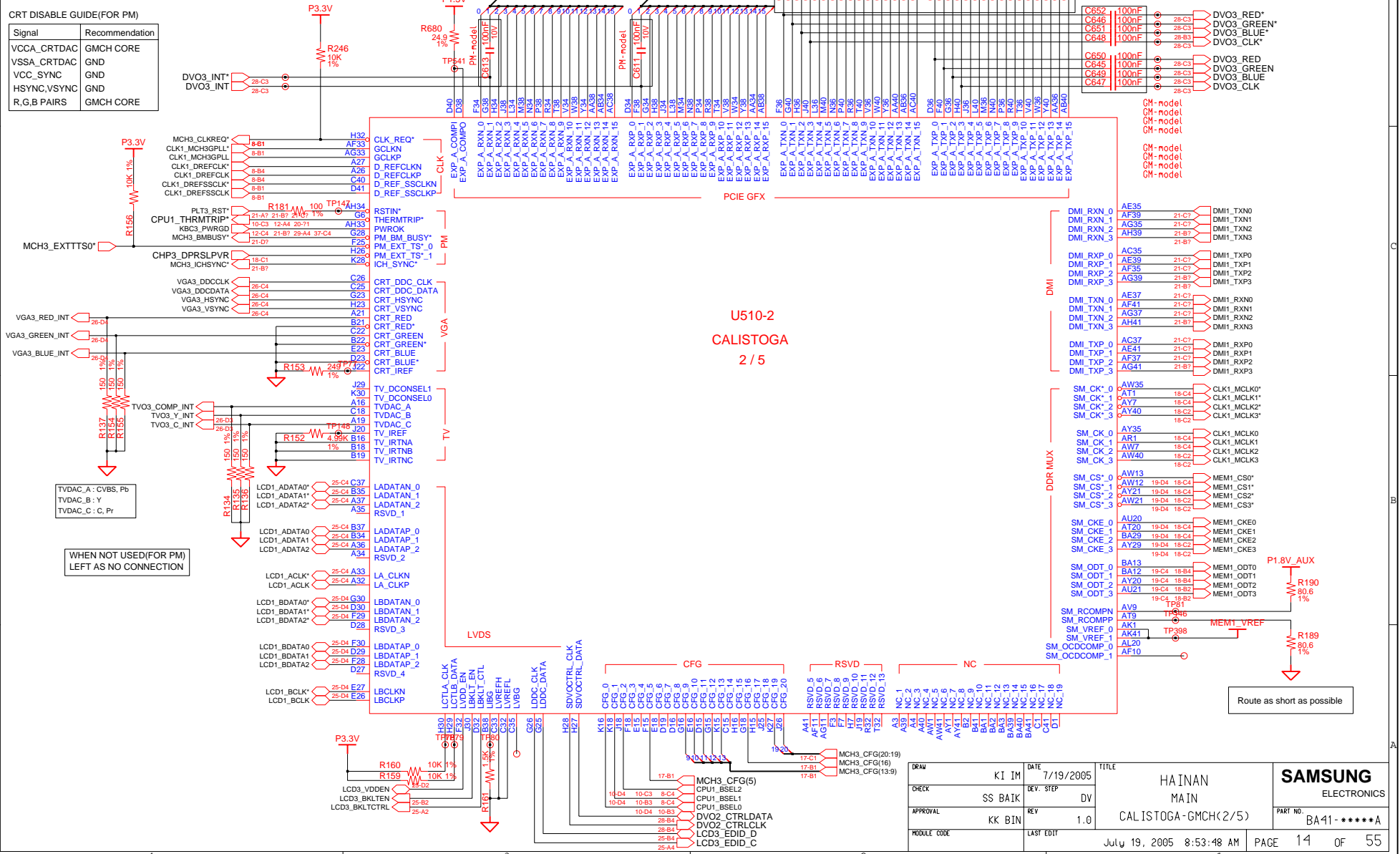


DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV		MAIN	
APPROVAL	KK BIN	REV	1.0		CALISTOGA-GMCH(1/5)	PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	13	OF 55

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CRT DISABLE GUIDE(FOR PM)

Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC_VSYNC	GMCH CORE
R,G,B PAIRS	GMCH CORE

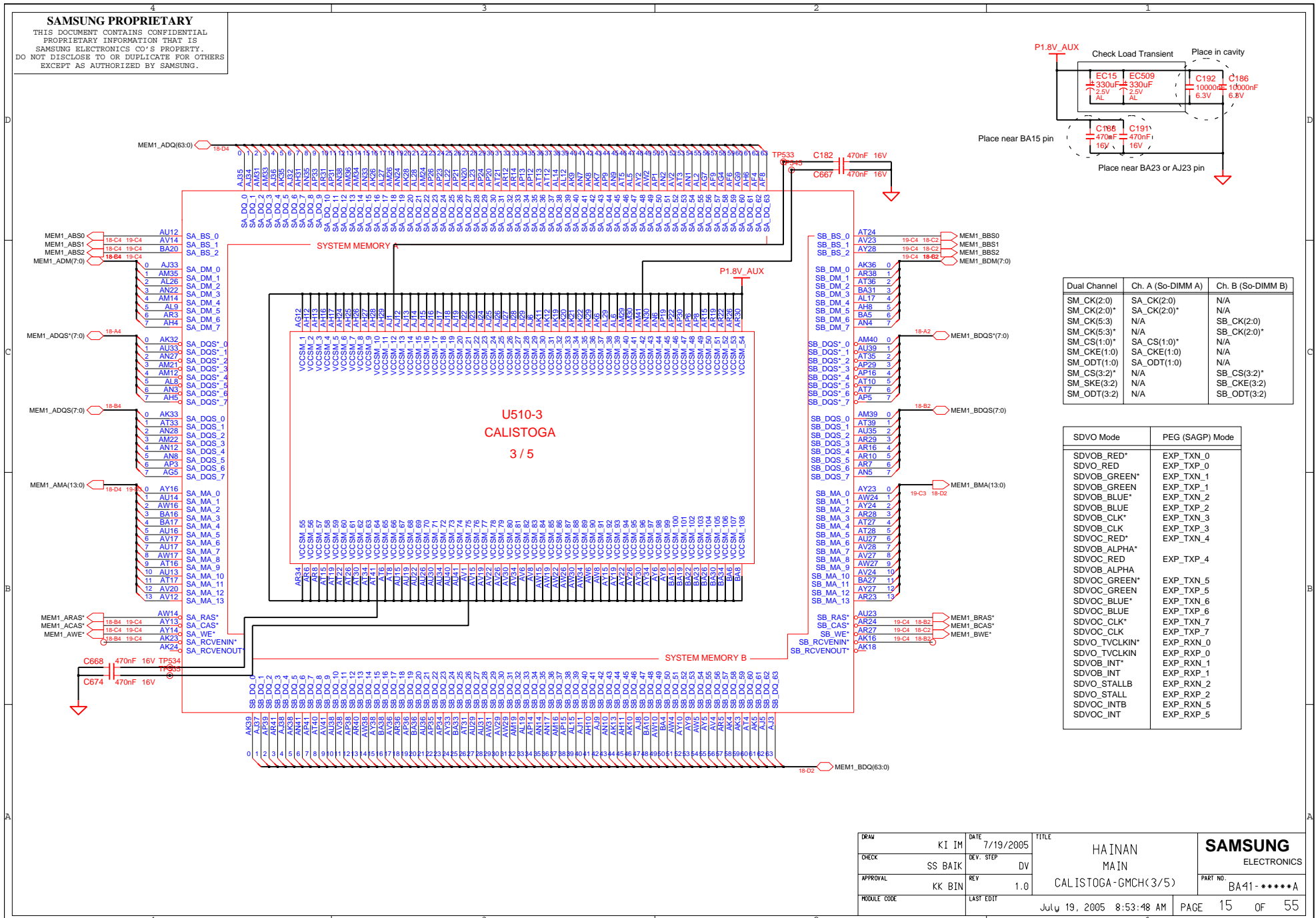


WHEN NOT USED(FOR PM)
 LEFT AS NO CONNECTION

Route as short as possible

DATE	7/19/2005	TITLE	HAINAN MAIN CALISTOGA-GMCH(2/5)	SAMSUNG ELECTRONICS PART NO. BA41-*****A
DEV. STEP	DV	REV	1.0	
LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	14	OF 55

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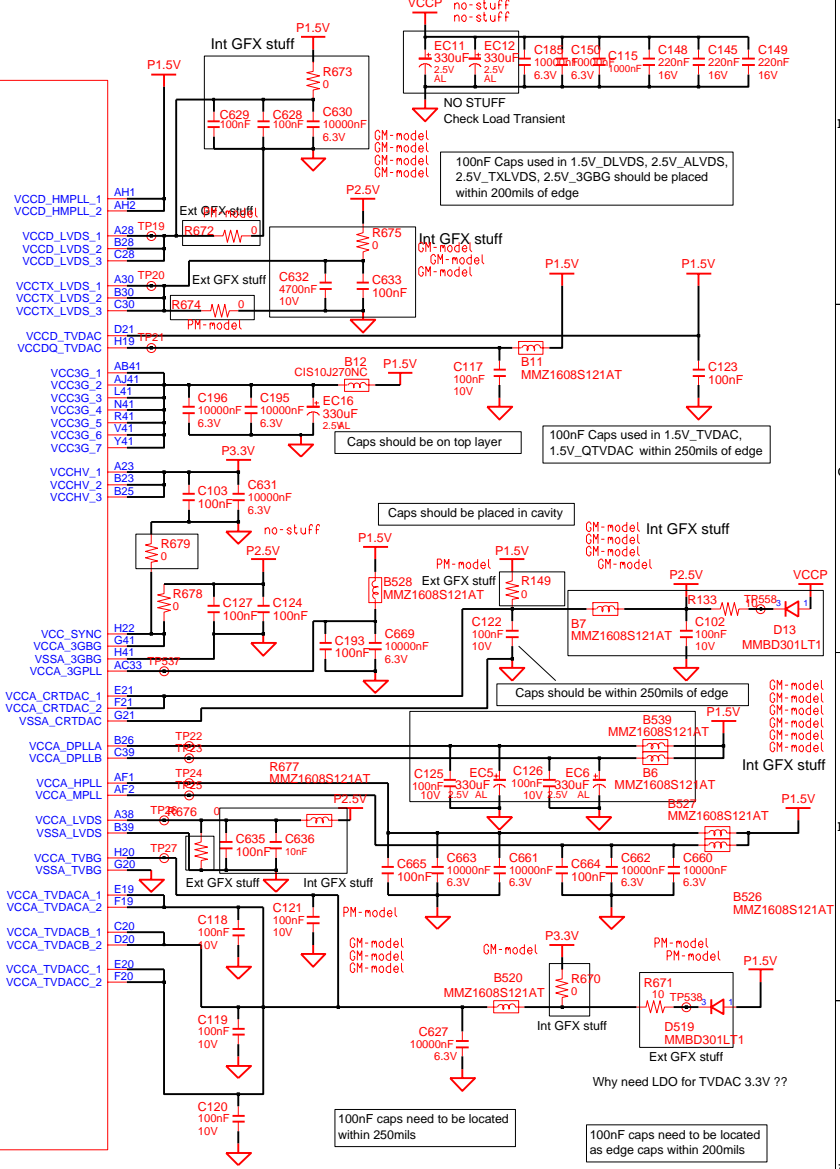
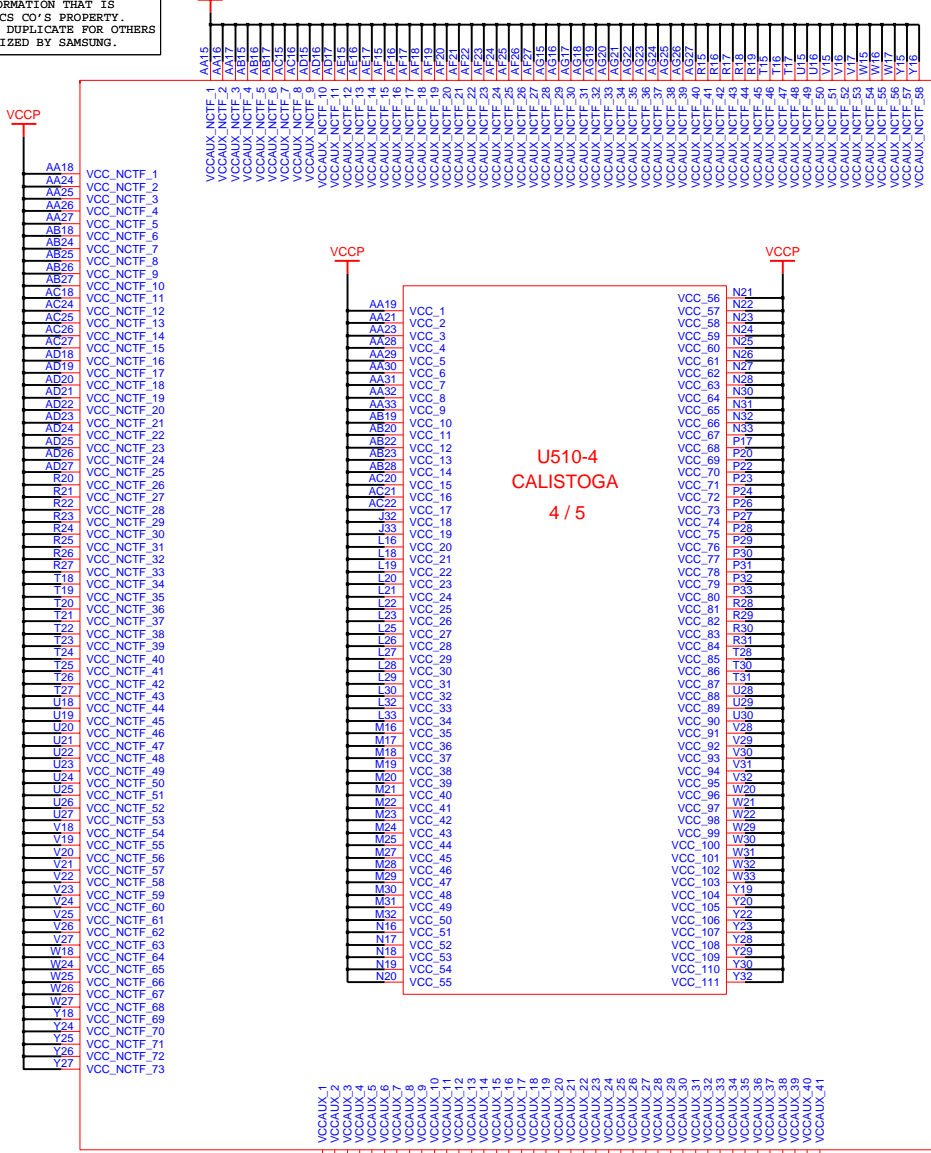
Dual Channel	Ch. A (So-Dimm A)	Ch. B (So-Dimm B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXN_5
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	EXP_TXN_6
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	CALISTOGA-GMCH(3/5)		PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	15	OF 55

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100nF Caps used in 1.5V_DLVDs, 2.5V_ALVDs, 2.5V_TXLVDs, 2.5V_3GBG should be placed within 200mils of edge

100nF Caps used in 1.5V_TVADC, 1.5V_QTVADC within 250mils of edge

Caps should be placed in cavity

Caps should be within 250mils of edge

100nF caps need to be located within 250mils

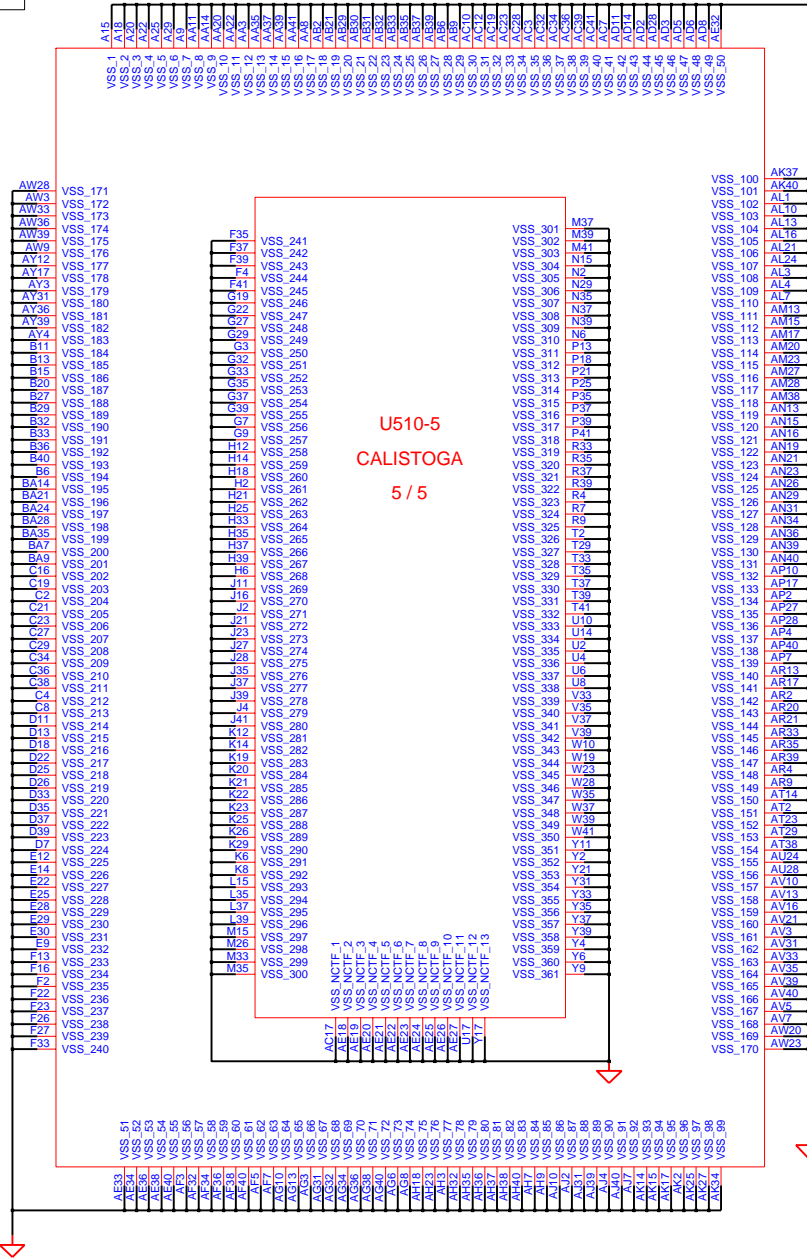
100nF caps need to be located as edge caps within 200mils

Why need LDO for TVDAC 3.3V ??

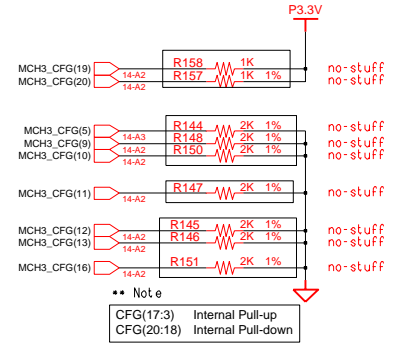
DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN	PART NO.	
APPROVAL	KK BIN	REV	1.0	CALISTOGA-GMCH(4/5)	BA41-****A	
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	16	OF 55

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**U510-5
CALISTOGA
5 / 5**



**** Note**
CFG(17:3) Internal Pull-up
CFG(20:18) Internal Pull-down

When CFG13:12 are pulled down to '00', certain clocks within Calistoga will become free-running clocks. This will lead to a rise in avg. power, but eliminates any possible clock-timing marginalities involved in clockpower-up/power-down. Intel strongly recommends leaving CFG13:12=NC (Internal PU to '11') to ensure low avg.

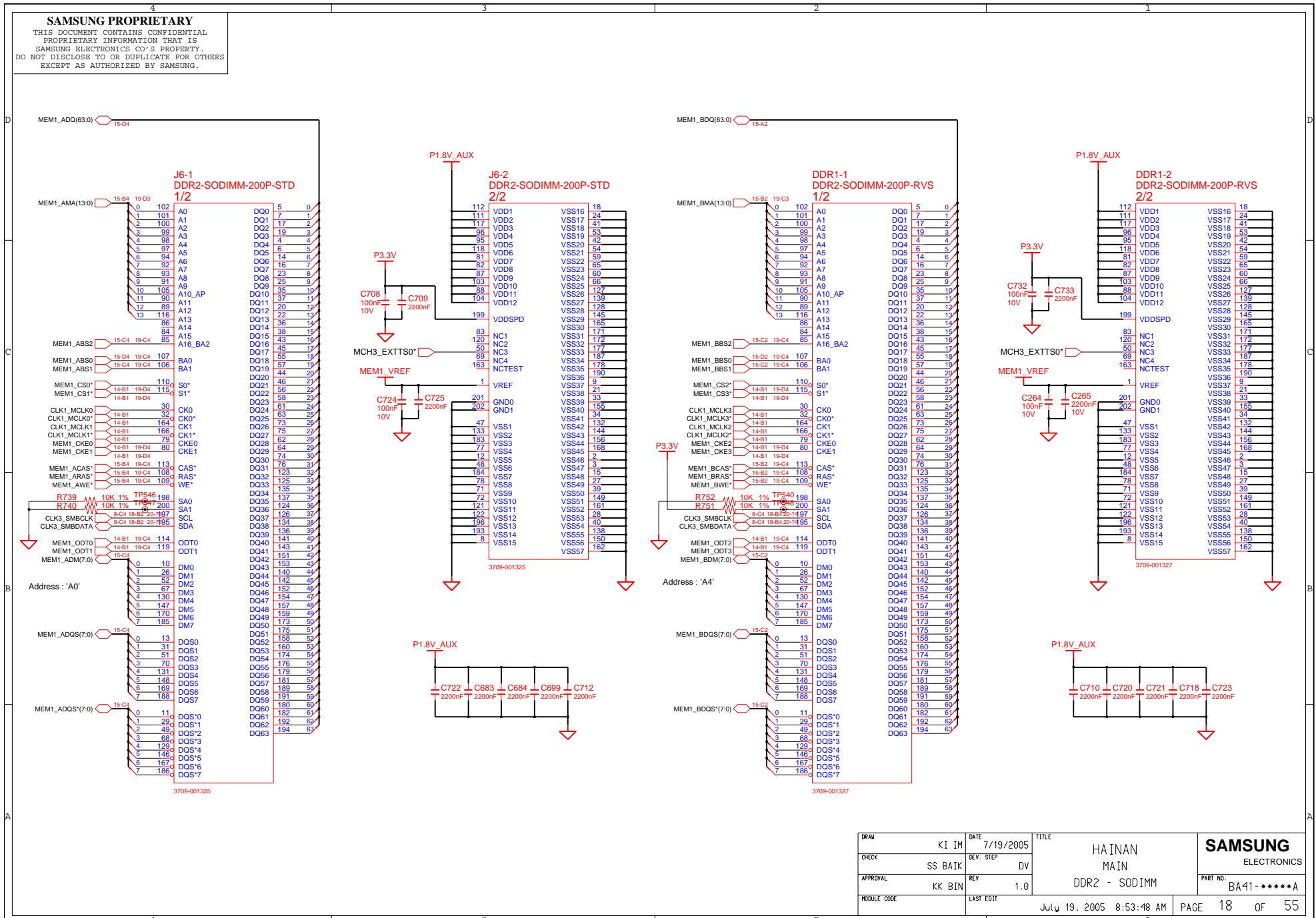
**** Note *POCAFEB-10 Only (Remove in MP Model)**

CFG#	Current Setting (def.: default Option)	
	Low	High
CFG(5)	DMIX2	DMIX4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN MAIN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	CALISTOGA-GMCH(5/5)		
APPROVAL	KK BIN	REV	1.0	July 19, 2005 8:53:48 AM		PART NO. BA41-*****A
MODULE CODE		LAST EDIT		PAGE 17 OF 55		

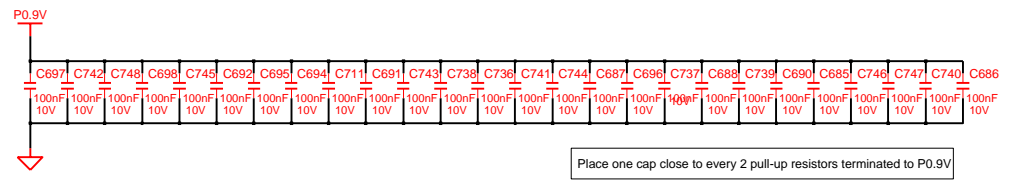
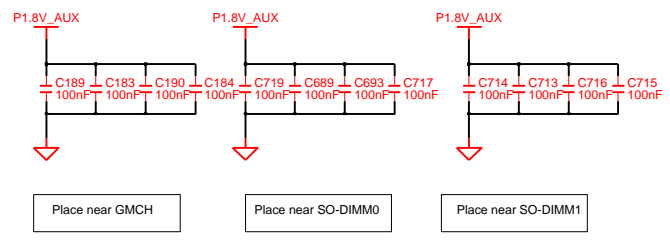
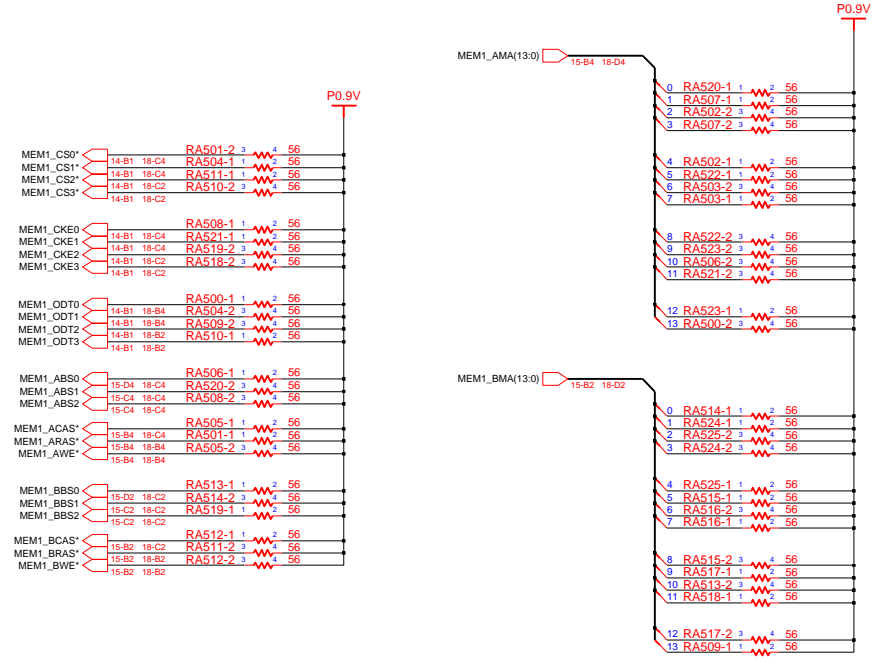
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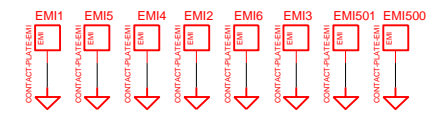
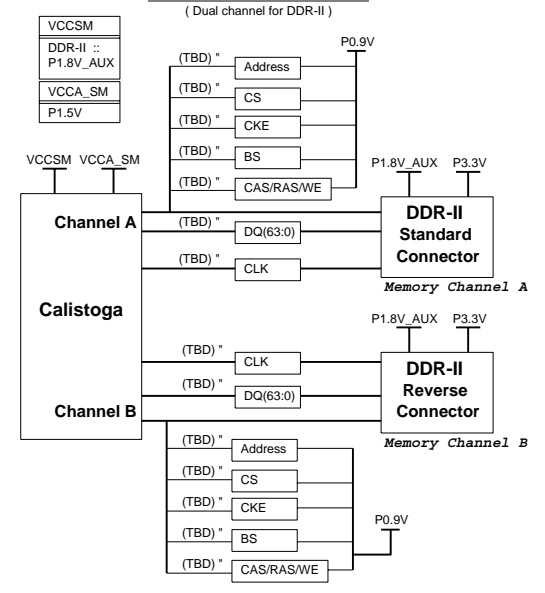


DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	DDR2 - SODIMM		PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	18	OF 55

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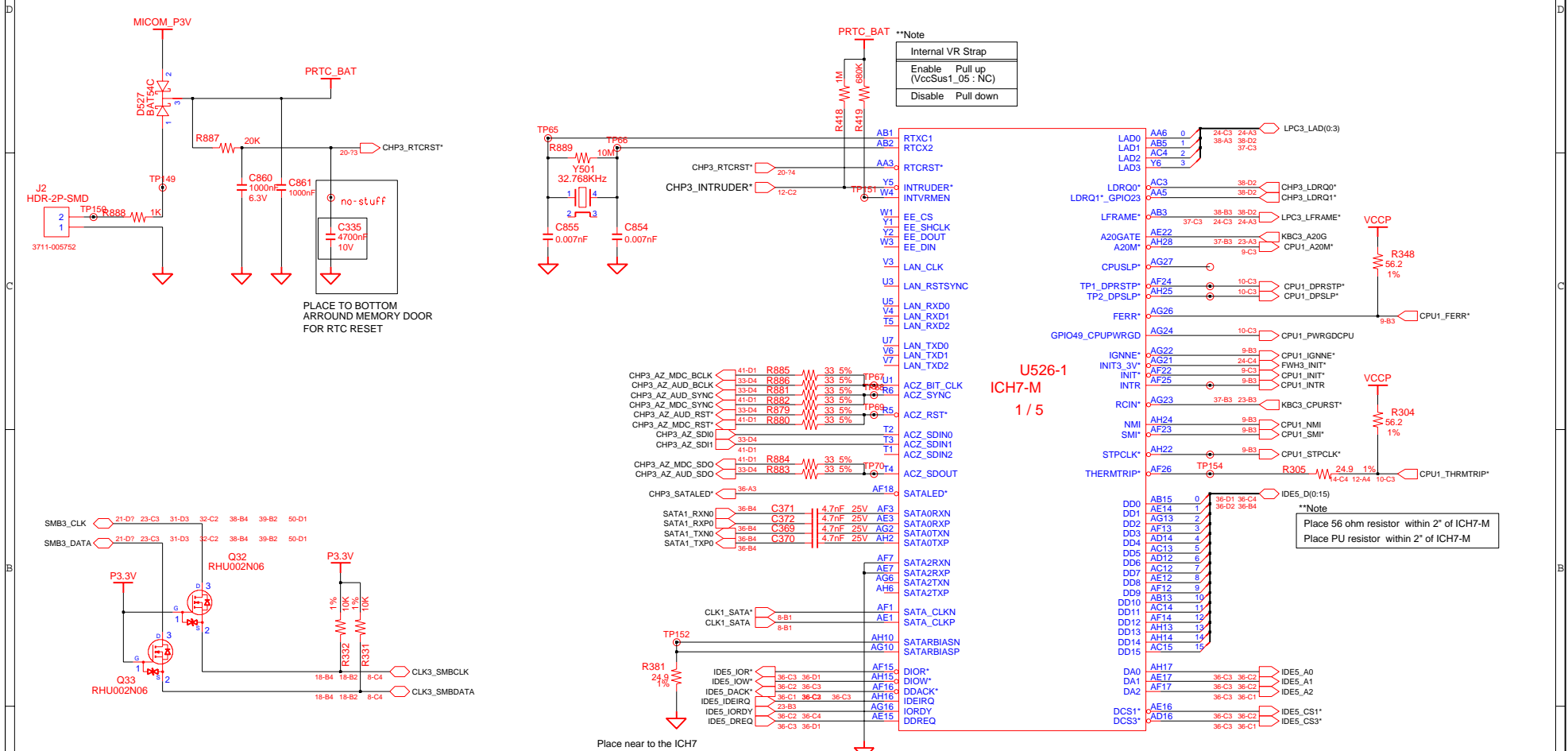


Memory Topology



DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN	MAIN	
APPROVAL	KK BIN	REV	1.0	DDR2 - TERMINATION	PART NO.	BA41 - *****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	19	OF 55

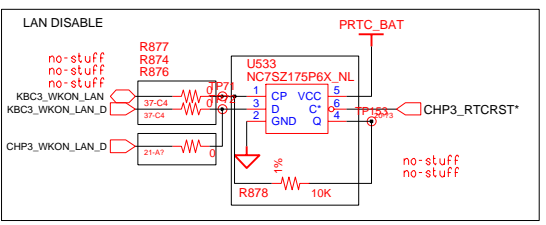
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****Note**
 Internal VR Strap
 Enable Pull up (VccSus1_05 : NC)
 Disable Pull down

****Note**
 Place 56 ohm resistor within 2" of ICH7-M
 Place PU resistor within 2" of ICH7-M

U526-1
ICH7-M
1 / 5

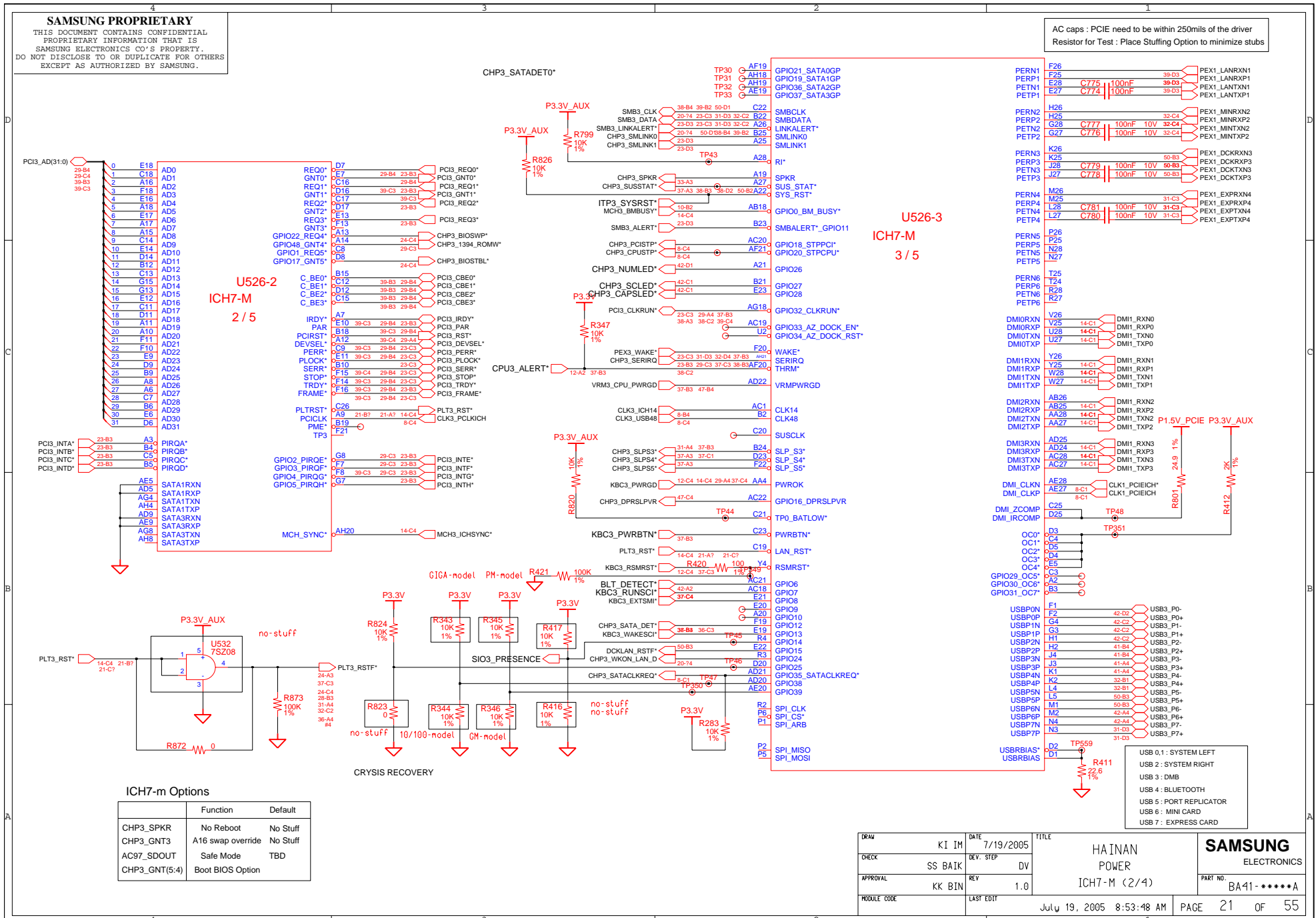


DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	ICH7 - M(1/4)		PART NO. BA41-*****A
MODULE CODE		LAST EDIT				
				July 19, 2005 8:53:48 AM	PAGE	20 OF 55

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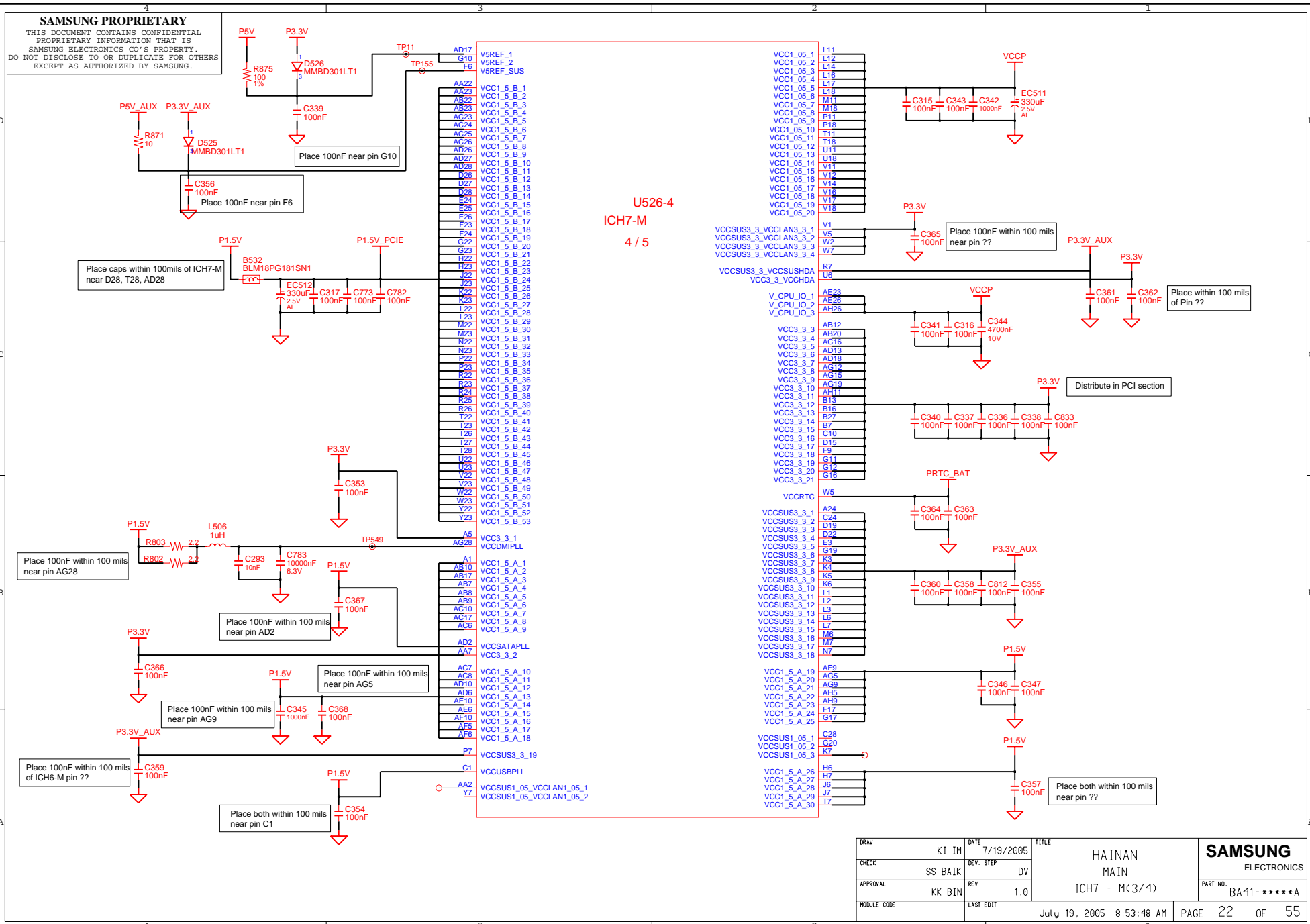
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AC caps : PCIe need to be within 250mils of the driver
Resistor for Test : Place Stuffed Option to minimize stubs



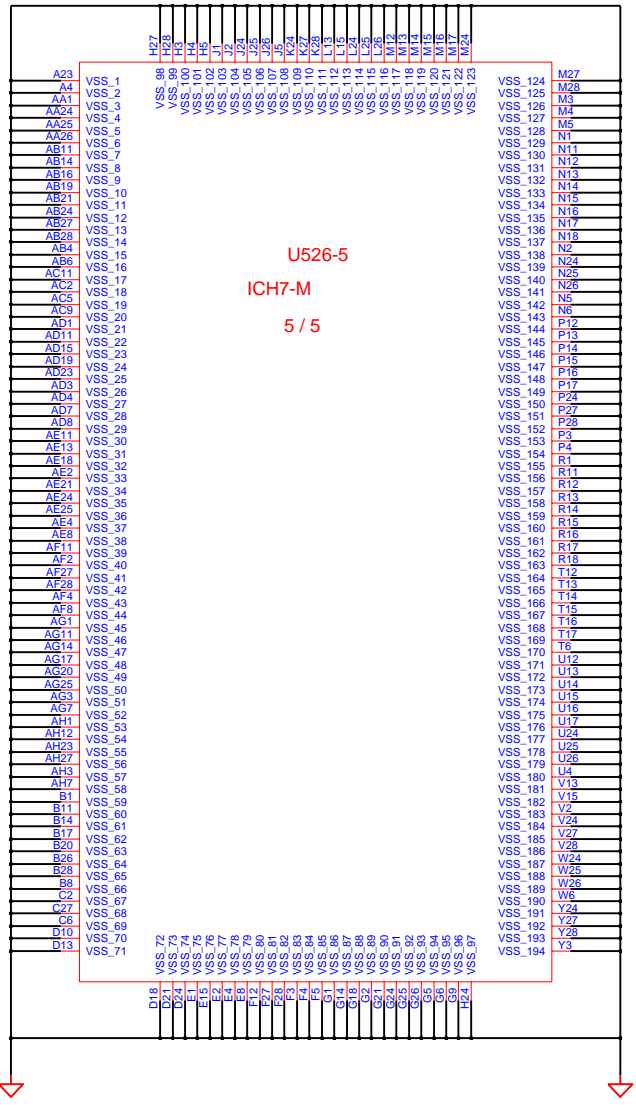
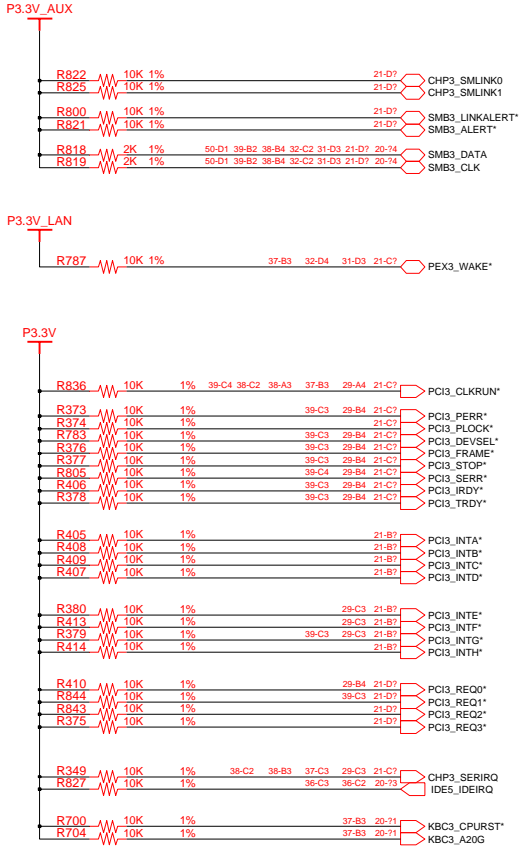
- USB 01 : SYSTEM LEFT
- USB 2 : SYSTEM RIGHT
- USB 3 : DMB
- USB 4 : BLUETOOTH
- USB 5 : PORT REPLICATOR
- USB 6 : MINI CARD
- USB 7 : EXPRESS CARD

DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN POWER ICH7-M (2/4)	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	21 OF 55	



DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	ICH7 - M(3/4)	PART NO.	BA41-*****A
MODULE CODE		LAST EDIT		July 19, 2005 8:53:48 AM	PAGE	22 OF 55

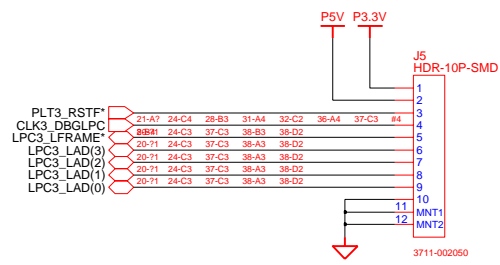
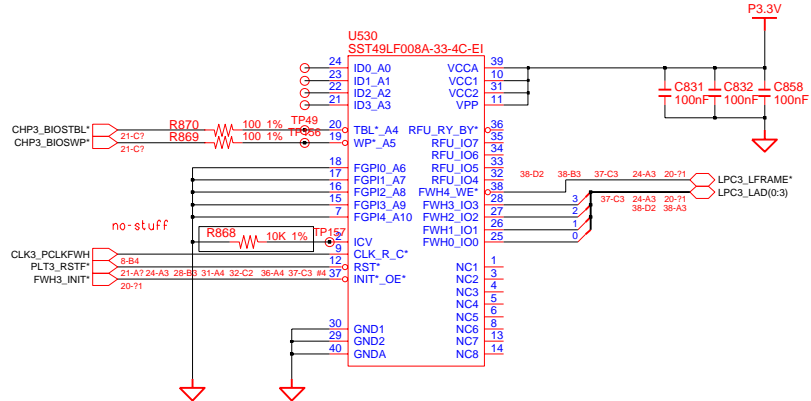
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U526-5
 ICH7-M
 5 / 5

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN	BA41-*****A	
APPROVAL	KK BIN	REV	1.0	ICH7 - M(4/4)		
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	23	OF 55

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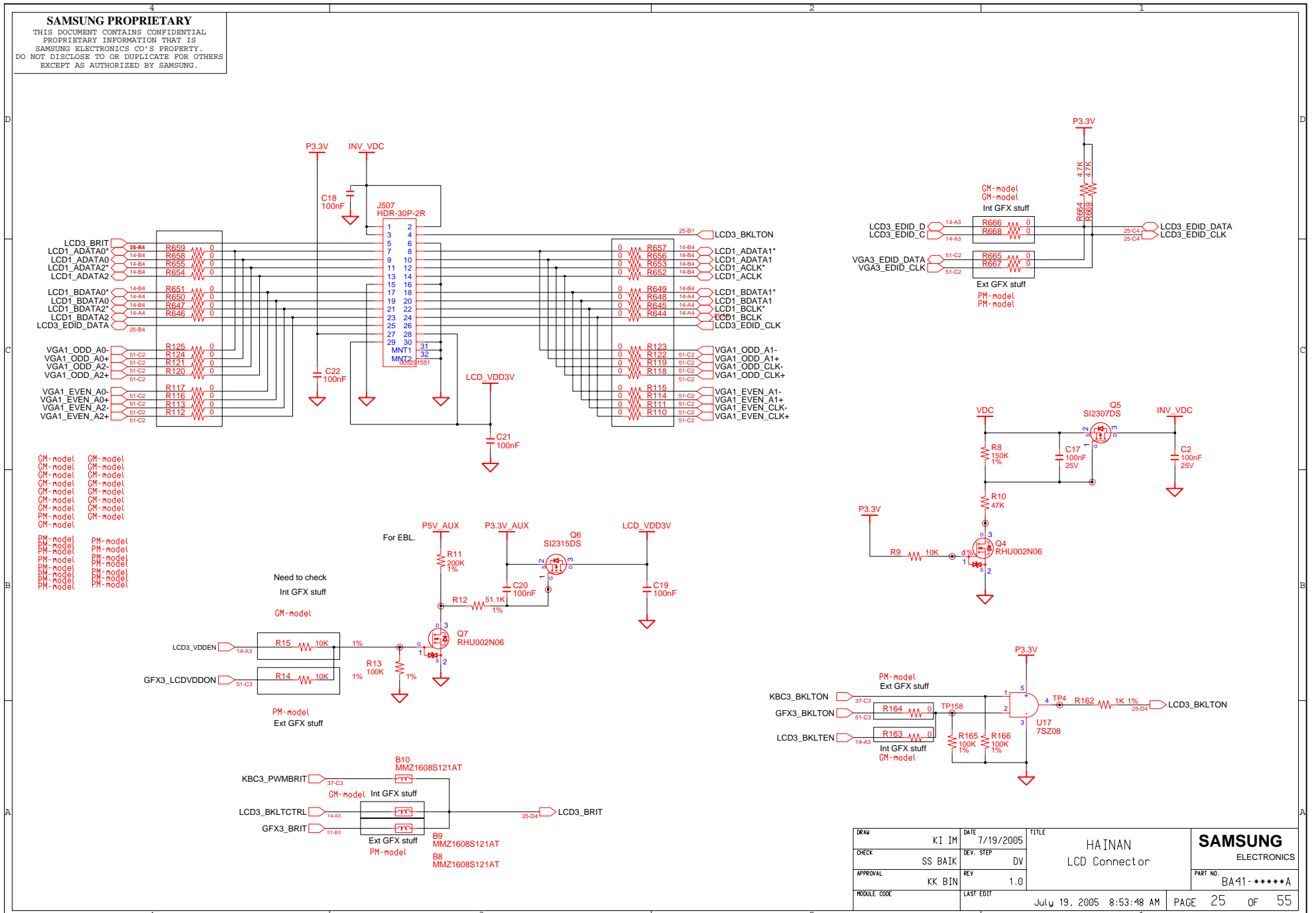


INSERT BIOS CODE

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN MAIN FIRMWARE HUB	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	24	OF 55

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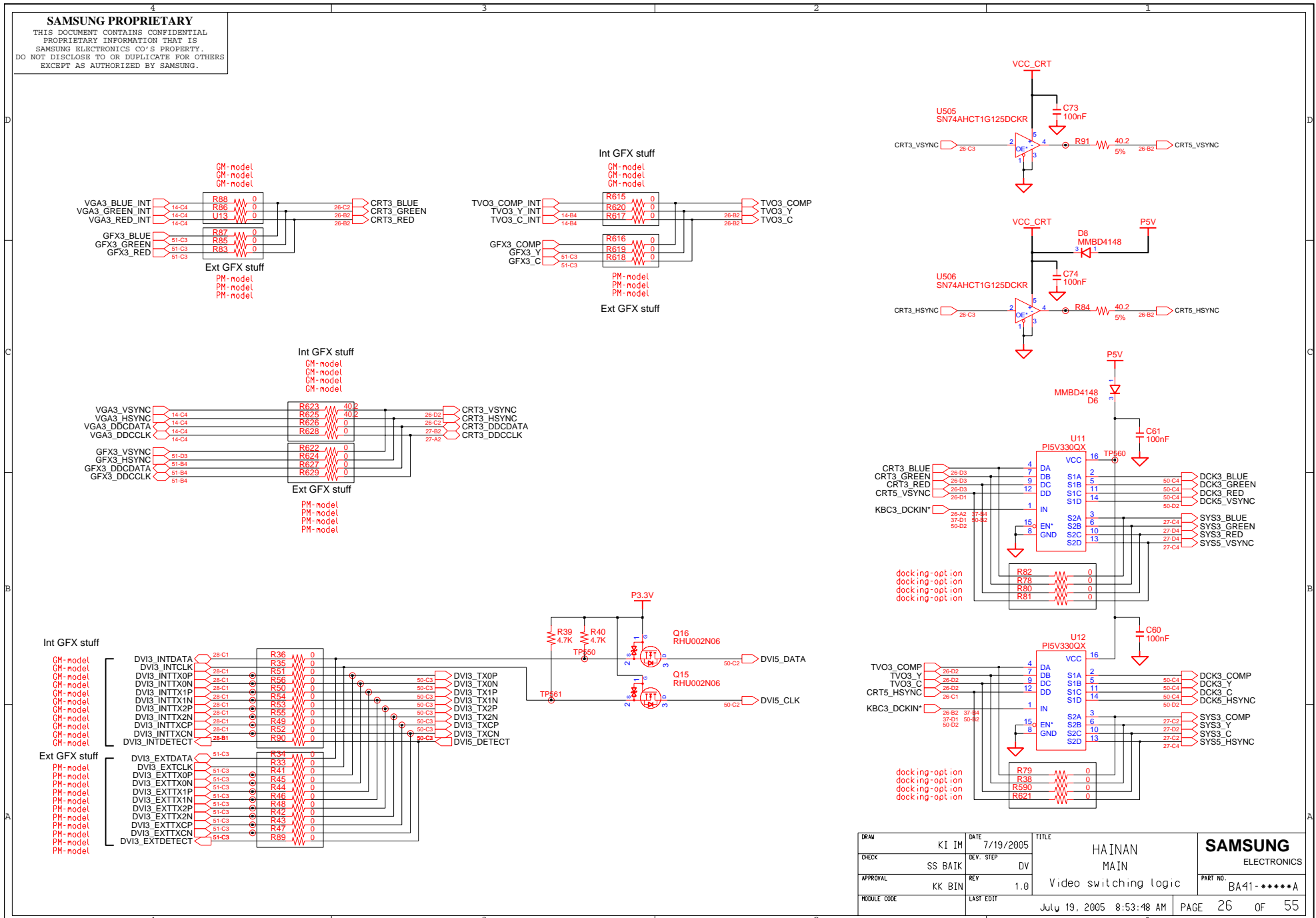
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DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN LCD Connector	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE	LAST EDIT			July 19, 2005 8:53:48 AM		PAGE 25 OF 55

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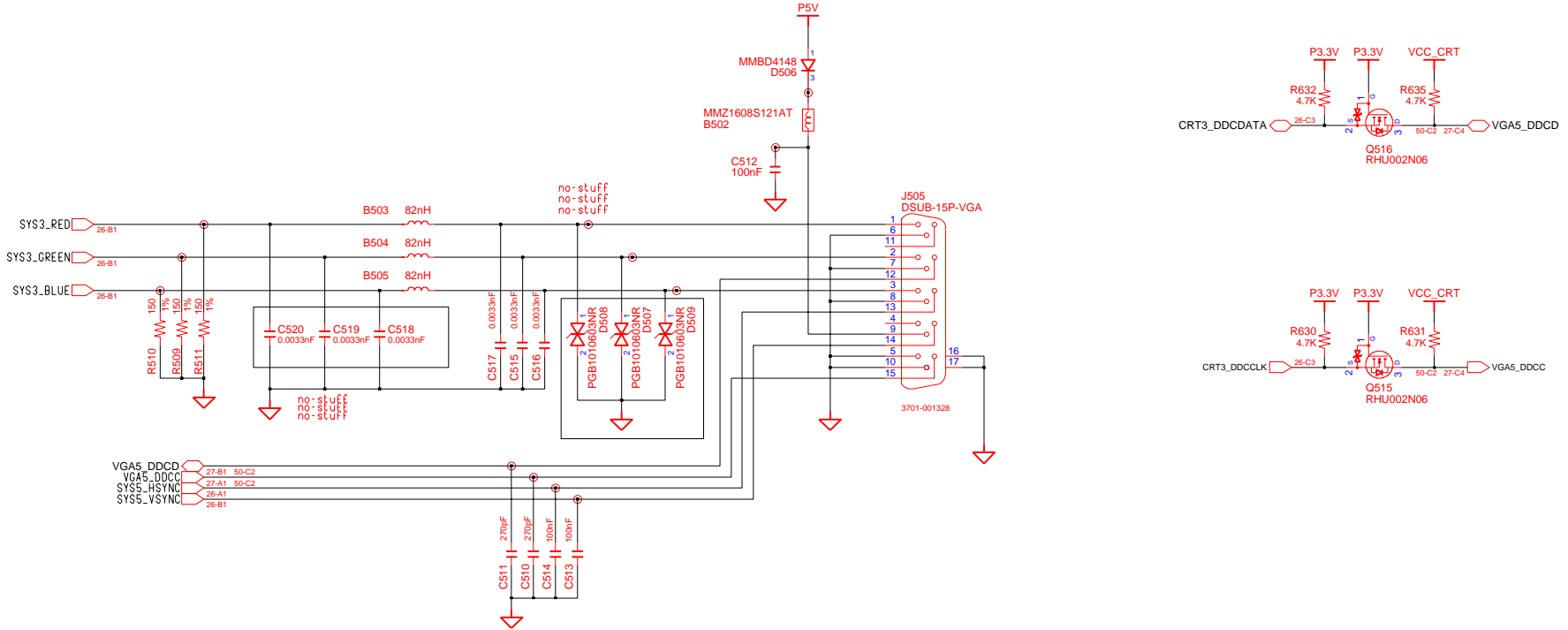
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DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	Video switching logic		PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	26	OF 55

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CRT CONNECTOR

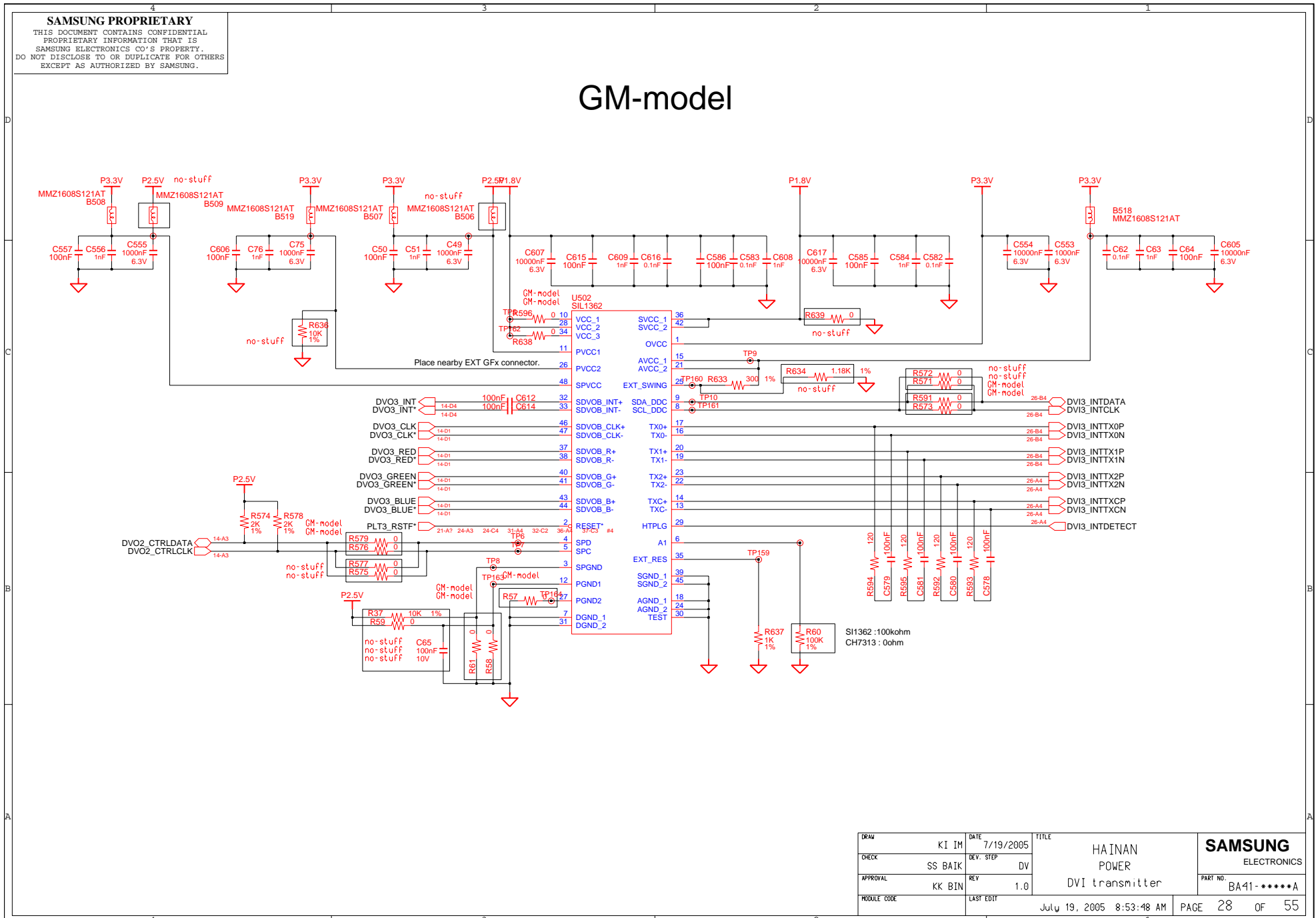


VGA5_DDCCD 27-B1 50-C2
 VGA5_DDCC 27-A1 50-C2
 SYS5_HSYNC 26-A1
 SYS5_VSYNC 26-B1

DRAW	IM, KI	DATE	7/19/2005	TITLE	HAINAN POWER CRT connector	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July, 19, 2005 8:59:59 AM	PAGE	27	OF 27

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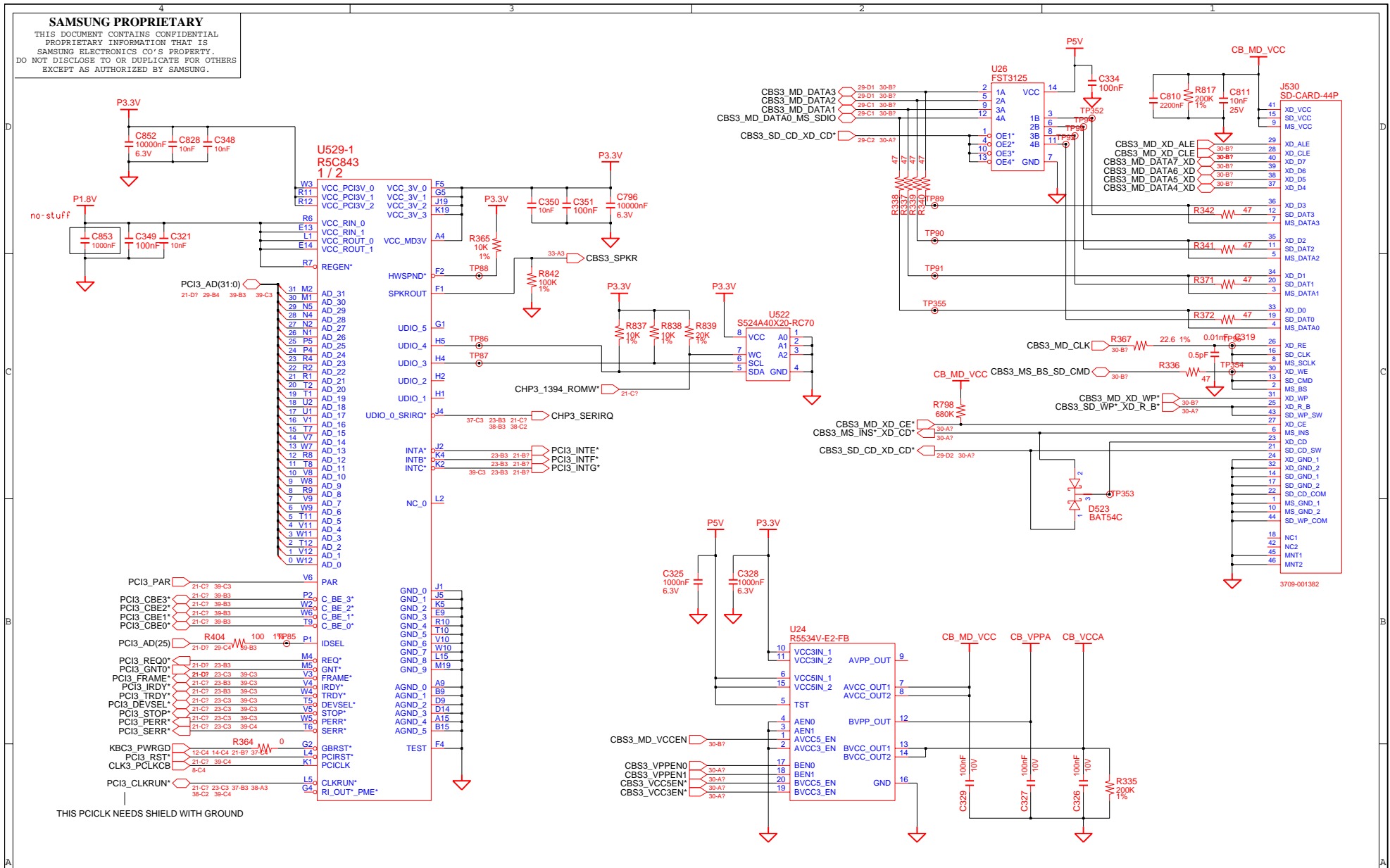
GM-model



DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN POWER DVI transmitter	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	28 OF 55	

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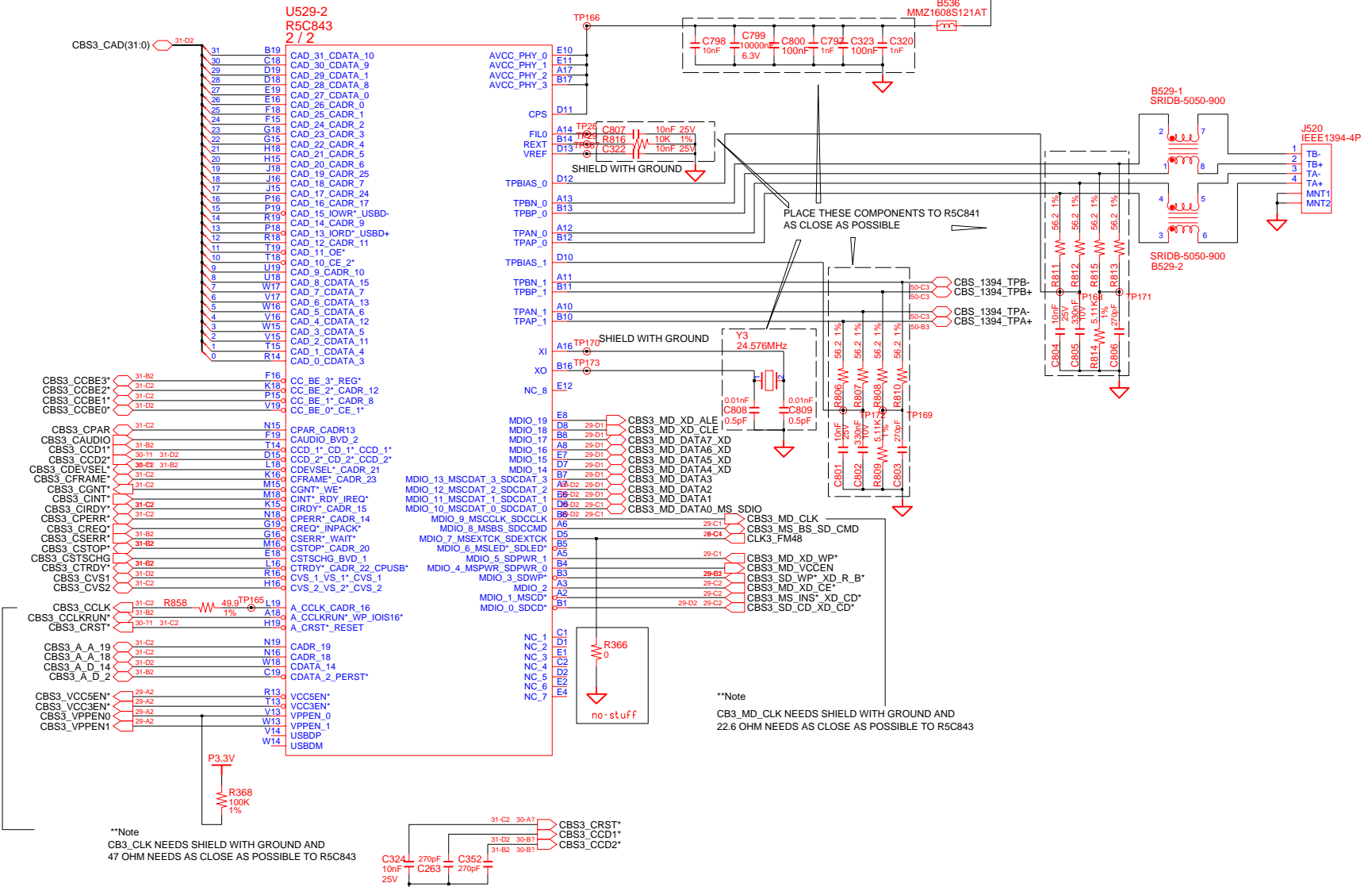


THIS PCICLK NEEDS SHIELD WITH GROUND

DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	CARDBUS / 1394 (1/2)	PART NO.	BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	29	OF 55

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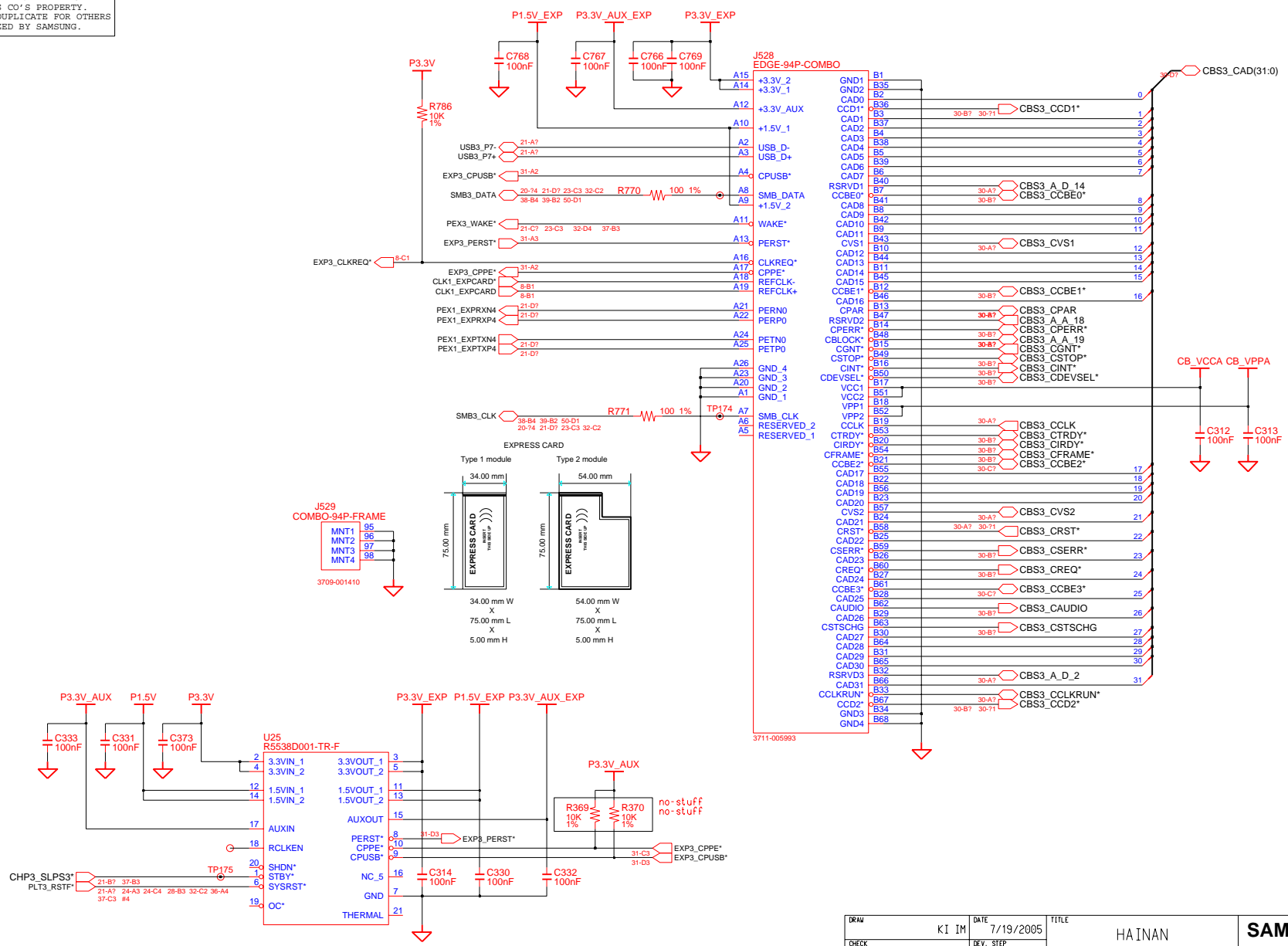


**Note
CB3_CLK NEEDS SHIELD WITH GROUND AND 47 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

**Note
CB3_MD_CLK NEEDS SHIELD WITH GROUND AND 22.6 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	POWER		
APPROVAL	KK BIN	REV	1.0	CardBus & 1394 (2/2)	PART NO.	BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	30	OF 55

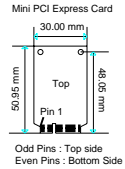
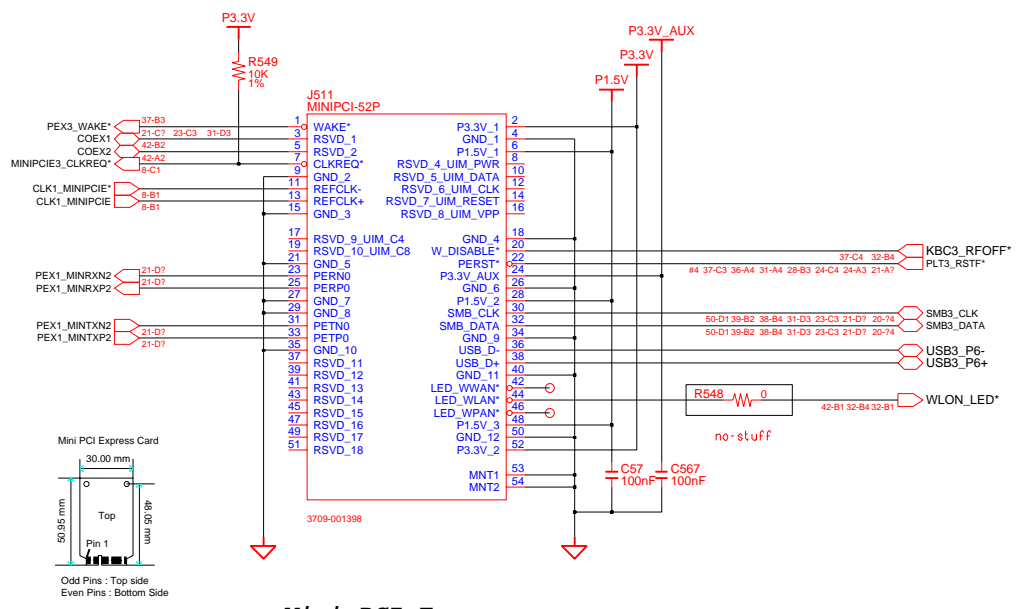
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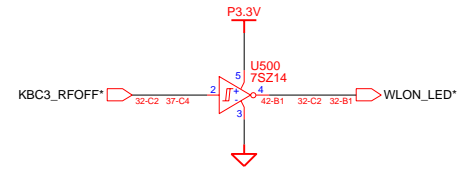
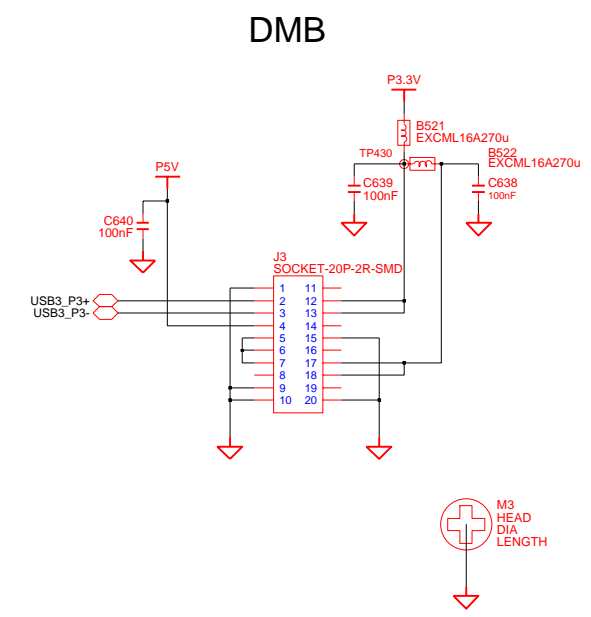
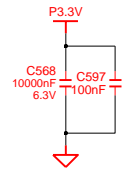
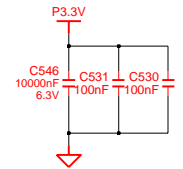
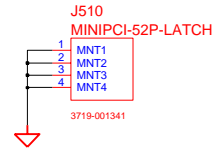
B1	+3.3V_2	GND1	B35
B2	+3.3V_1	GND2	B35
B3	+3.3V_AUX	CAD0	B36
B4	+1.5V_1	CAD1	B37
B5	USB_D-	CAD2	B4
B6	USB_D+	CAD3	B4
B7	CPUSB*	CAD4	B5
B8	SMB_DATA +1.5V_2	CAD5	B39
B9	WAKE*	CAD6	B6
B10	PERST*	CAD7	B6
B11	CLKREQ*	RSRVD1	B7
B12	CPPE*	CCBE0*	B41
B13	REFCLK-REFCLK+	CAD8	B8
B14	PERNO	CAD9	B8
B15	PETNO	CAD10	B42
B16	PETPO	CAD11	B43
B17	GND_3	CAD12	B10
B18	GND_2	CAD13	B44
B19	GND_1	CAD14	B45
B20	RESERVED_2	CAD15	B12
B21	RESERVED_1	CCBE1*	B12
B22		CAD16	B46
B23		CPAR	B13
B24		RSRVD2	B47
B25		CPERR*	B14
B26		CBLOCK*	B48
B27		CGNT*	B15
B28		CSTOP*	B49
B29		CINT*	B16
B30		CDEVSEL*	B50
B31		VCC1*	B17
B32		VPP1*	B52
B33		VPP2*	B52
B34		CLK	B19
B35		CTRDY*	B53
B36		CIRDY*	B53
B37		CFRAME*	B54
B38		CCBE2*	B54
B39		CCBE2*	B55
B40		CAD17	B22
B41		CAD18	B22
B42		CAD19	B23
B43		CAD20	B57
B44		CVS2*	B24
B45		CRST*	B58
B46		CSERR*	B25
B47		CREQ*	B26
B48		CCBE3*	B61
B49		CAUDIO	B28
B50		CSTSCHG	B62
B51		CAD21	B29
B52		CAD22	B63
B53		CAD23	B30
B54		CAD24	B64
B55		CAD25	B31
B56		CAD26	B65
B57		RSRVD3	B32
B58		CAD27	B66
B59		CAD28	B66
B60		CAD29	B33
B61		CAD30	B67
B62		CAD31	B67
B63		CCLKRUN*	B34
B64		CCD2*	B34
B65		GND3	B68
B66		GND4	B68

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	EXPRESS CARD & PCMCIA		
APPROVAL	KK BIN	REV	1.0	PART NO. BA41-*****A		
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	31	OF 55

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Mini PCI Express
 PCI Express Mini Card ElectroMechanical Spec. 1.0



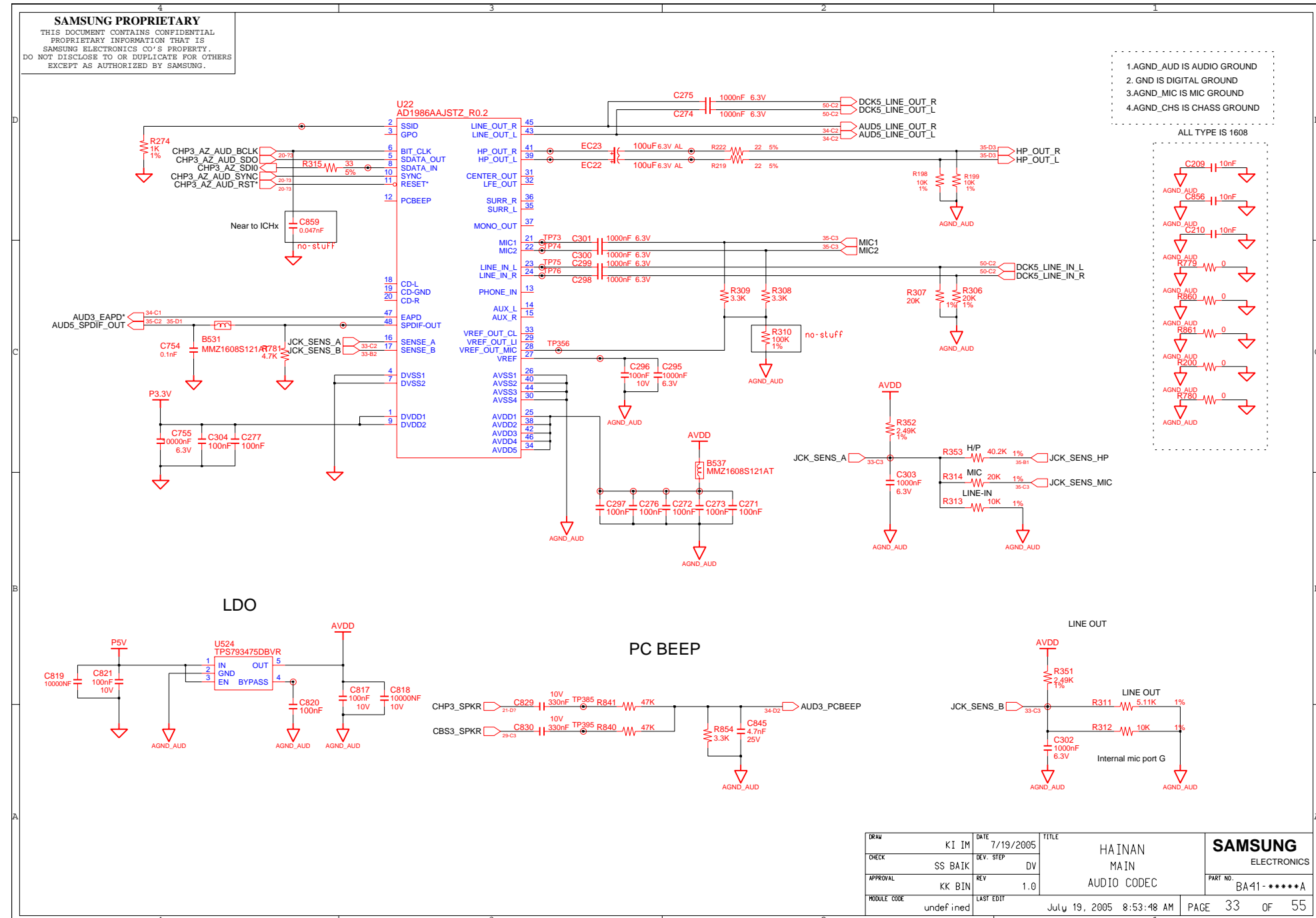
DRAW	IM, KI	DATE	7/19/2005	TITLE	HAINAN MAIN	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MINI PCIEX & DMB & IR		
APPROVAL	BIN, KK	REV	1.0	Jul., 19, 2005 9:01:07 AM		PART NO. BA41-*****A
MODULE CODE		LAST EDIT		PAGE 32 OF 32		

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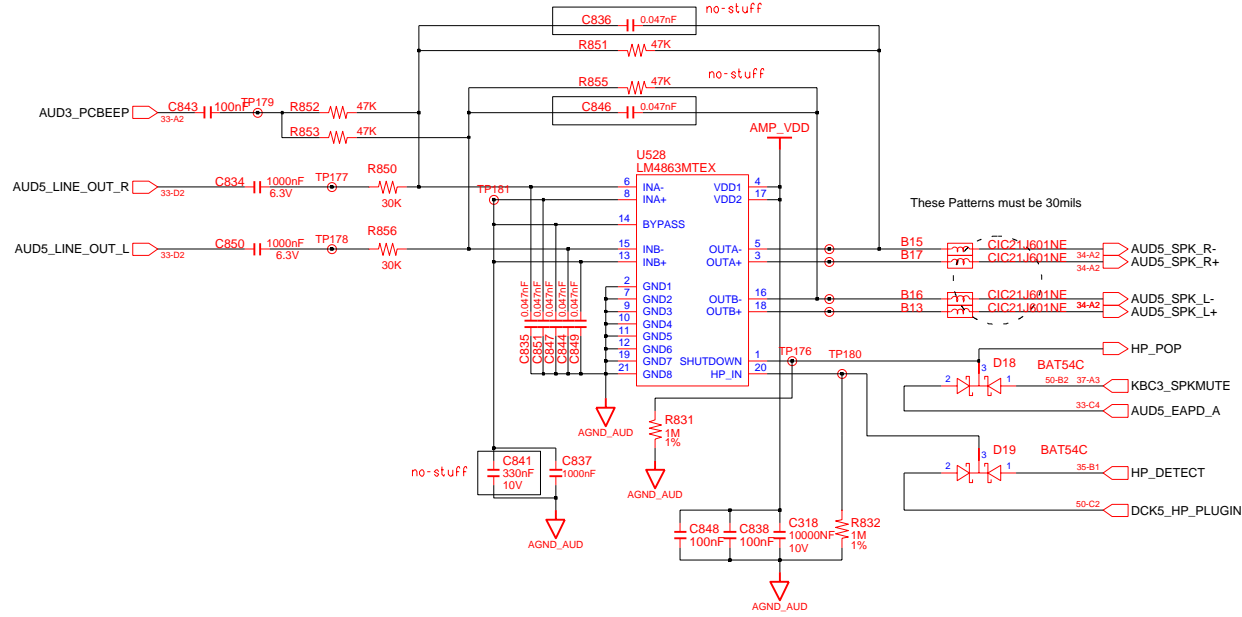
- 1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASSIS GROUND

ALL TYPE IS 1608



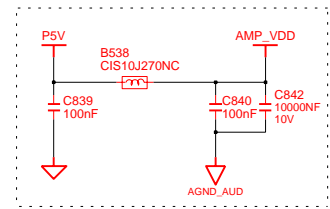
DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN MAIN AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41 - *****A
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 19, 2005 8:53:48 AM	PAGE 33 OF 55		

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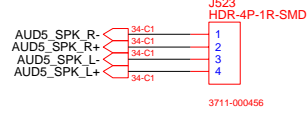


These Patterns must be 30mils

AMP_VDD



INTERNAL STEREO SPEAKERS



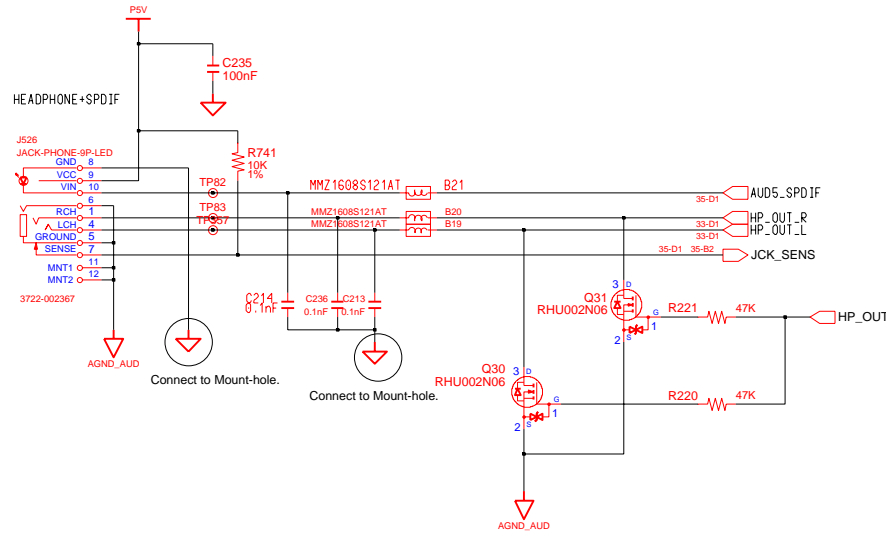
Should be written sign "L", "R" on the PCB

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN MAIN LIMITER & AMP	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	34 OF 55	

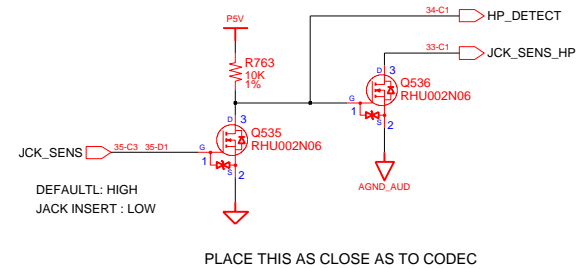
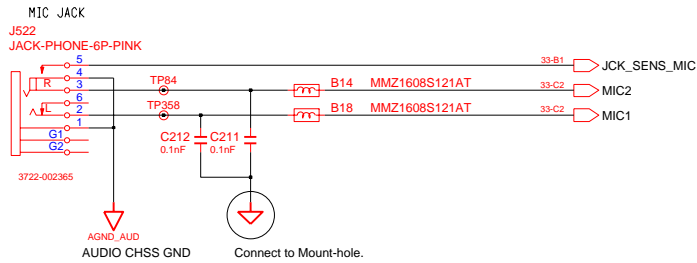
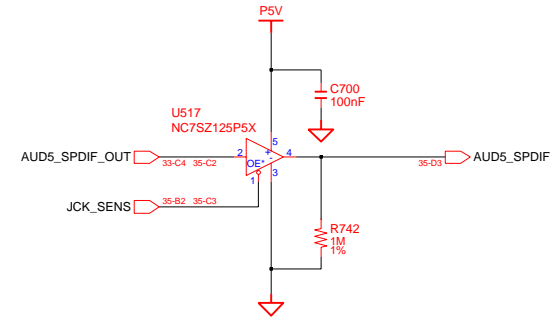
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Default: 5-7-6 open
STEREO JACK: 5-7-6 SHORT
S/PDIF 5-7 SHORT



SPDIF DETECT

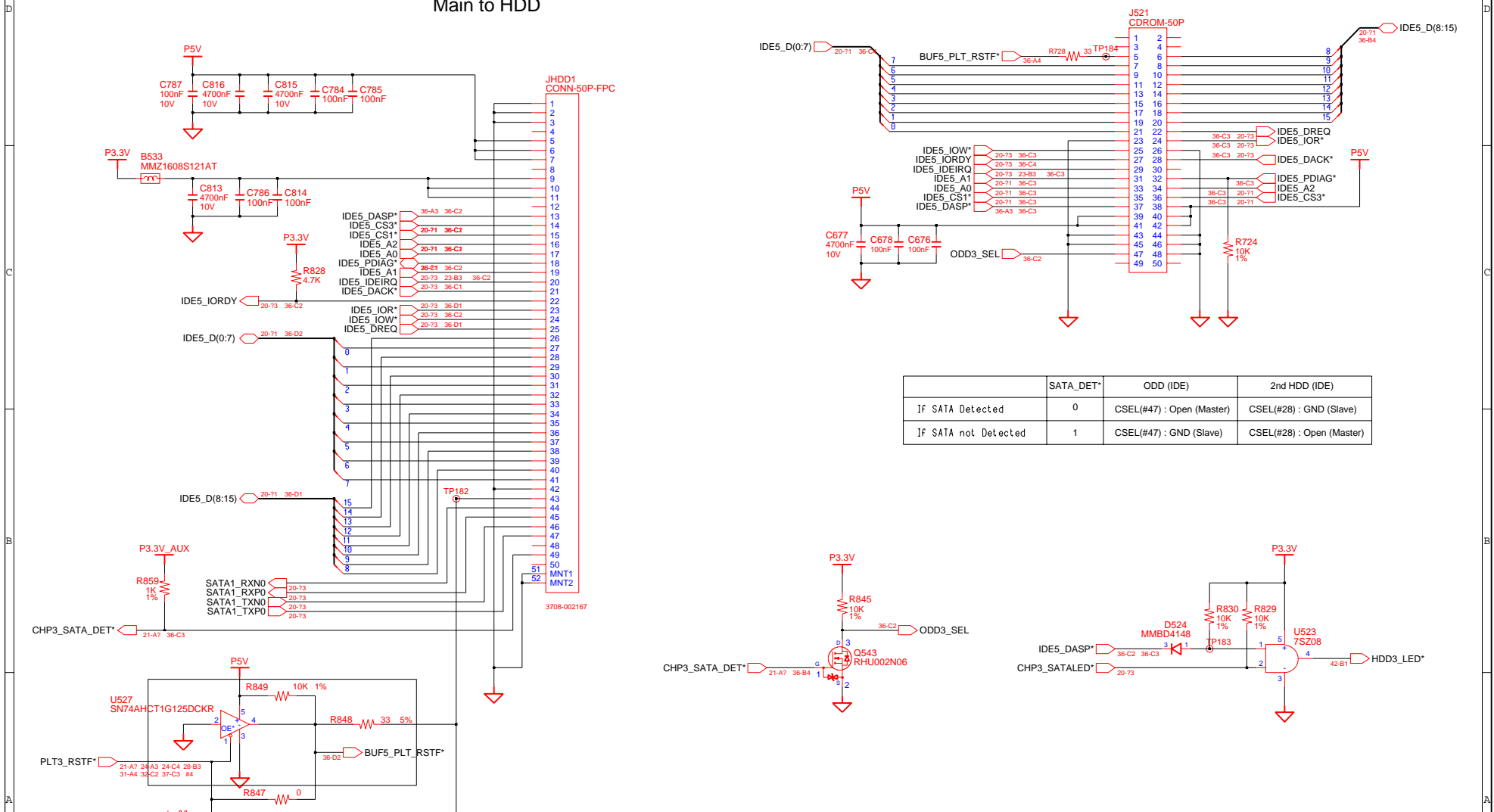


DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV		MAIN	
APPROVAL	KK BIN	REV	1.0	Headphone & MIC jack		PART NO. BA41-*****A
MODULE CODE		LAST EDIT		July 19, 2005 8:53:48 AM	PAGE	35 OF 55

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Main to Swap B'd

Main to HDD

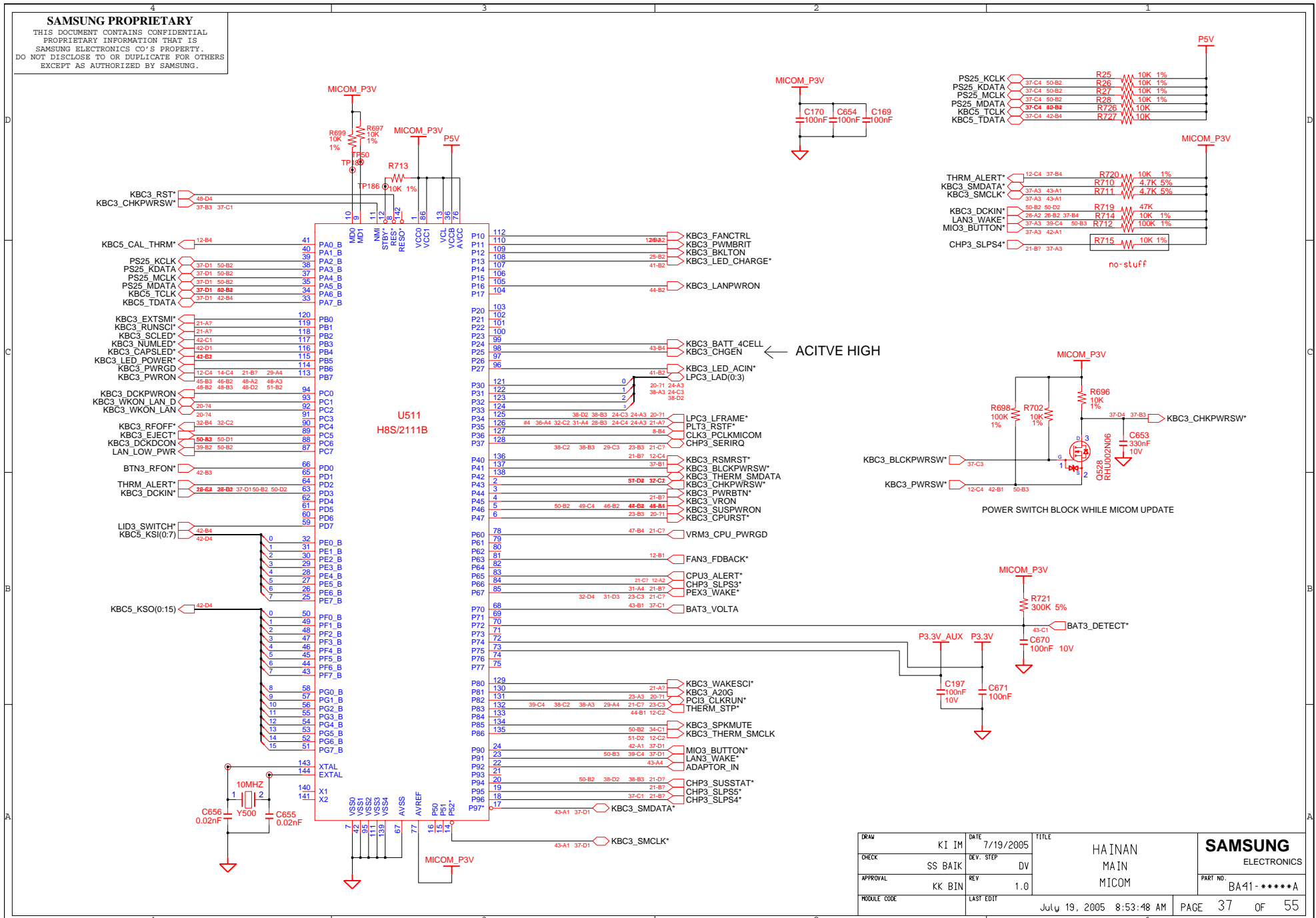


	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Slave)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Master)

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	HDD ODD CONNECTOR		PART NO. BA41 - *****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	36	OF 55

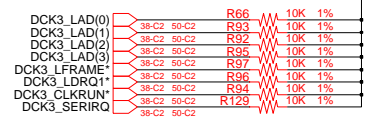
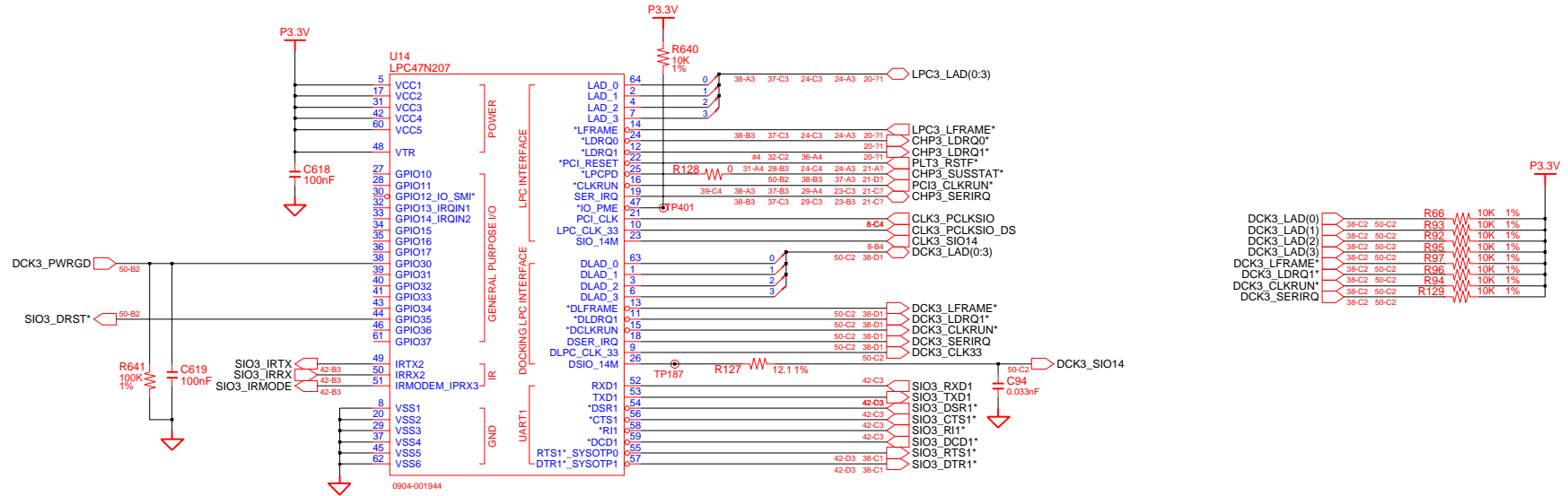
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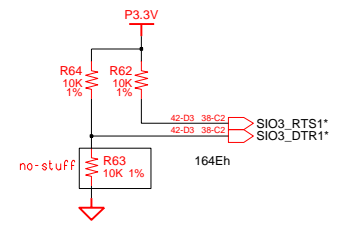
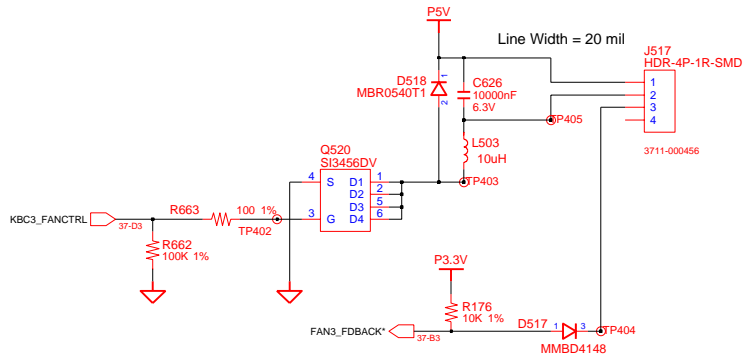


DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	MICOM		PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	37	OF 55

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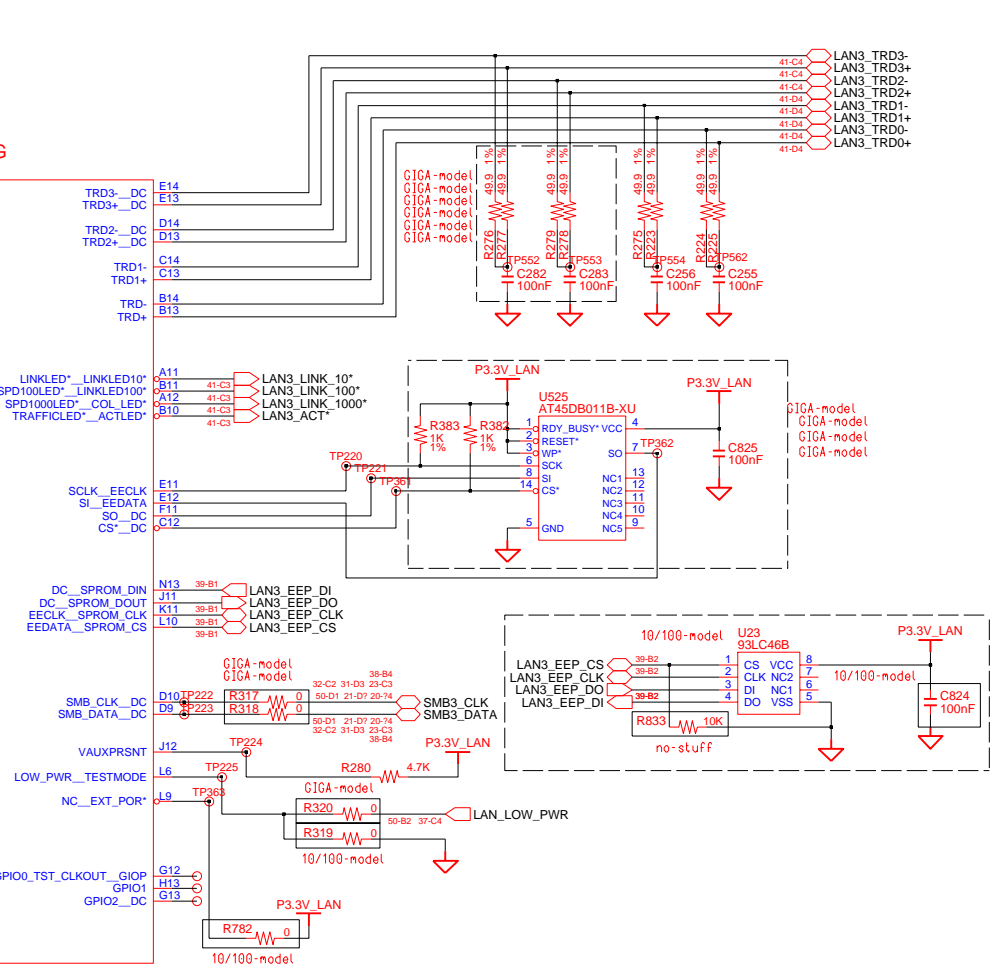
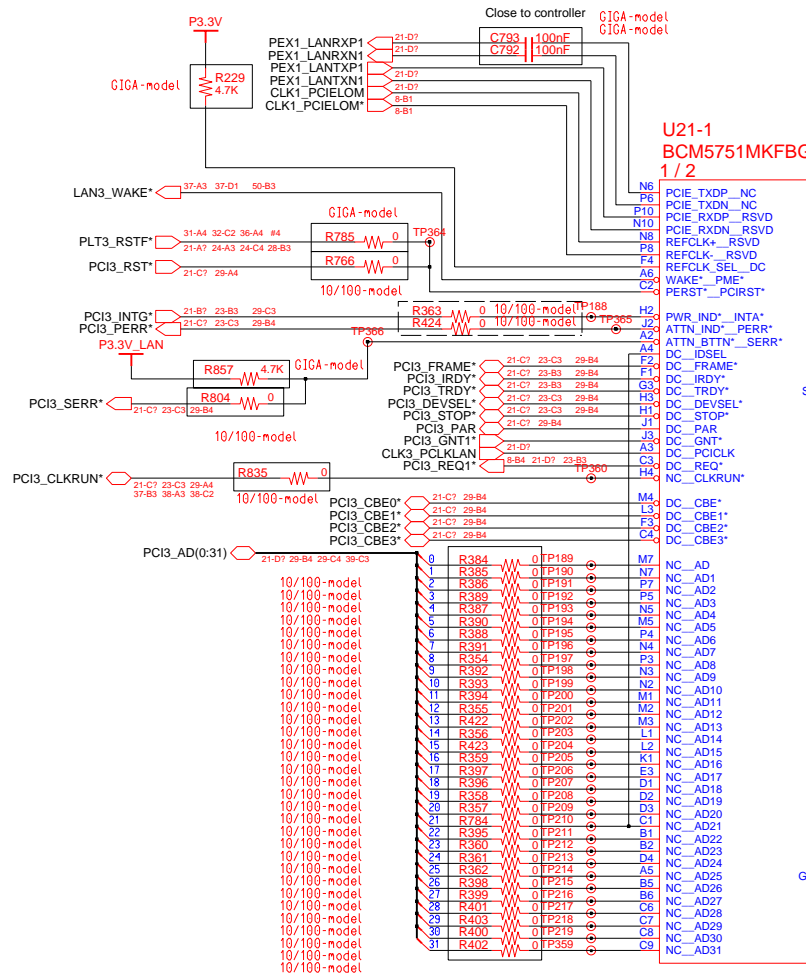
FAN Control Logic



Changed to Control Methode(EBL)

DRAW	IM, KI	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	SUPER IO & FAN CONTROLLER	PART NO.	BA41-*****A
MODULE CODE		LAST EDIT	Jul, 19, 2005 9:02:46 AM	PAGE	38	OF 38

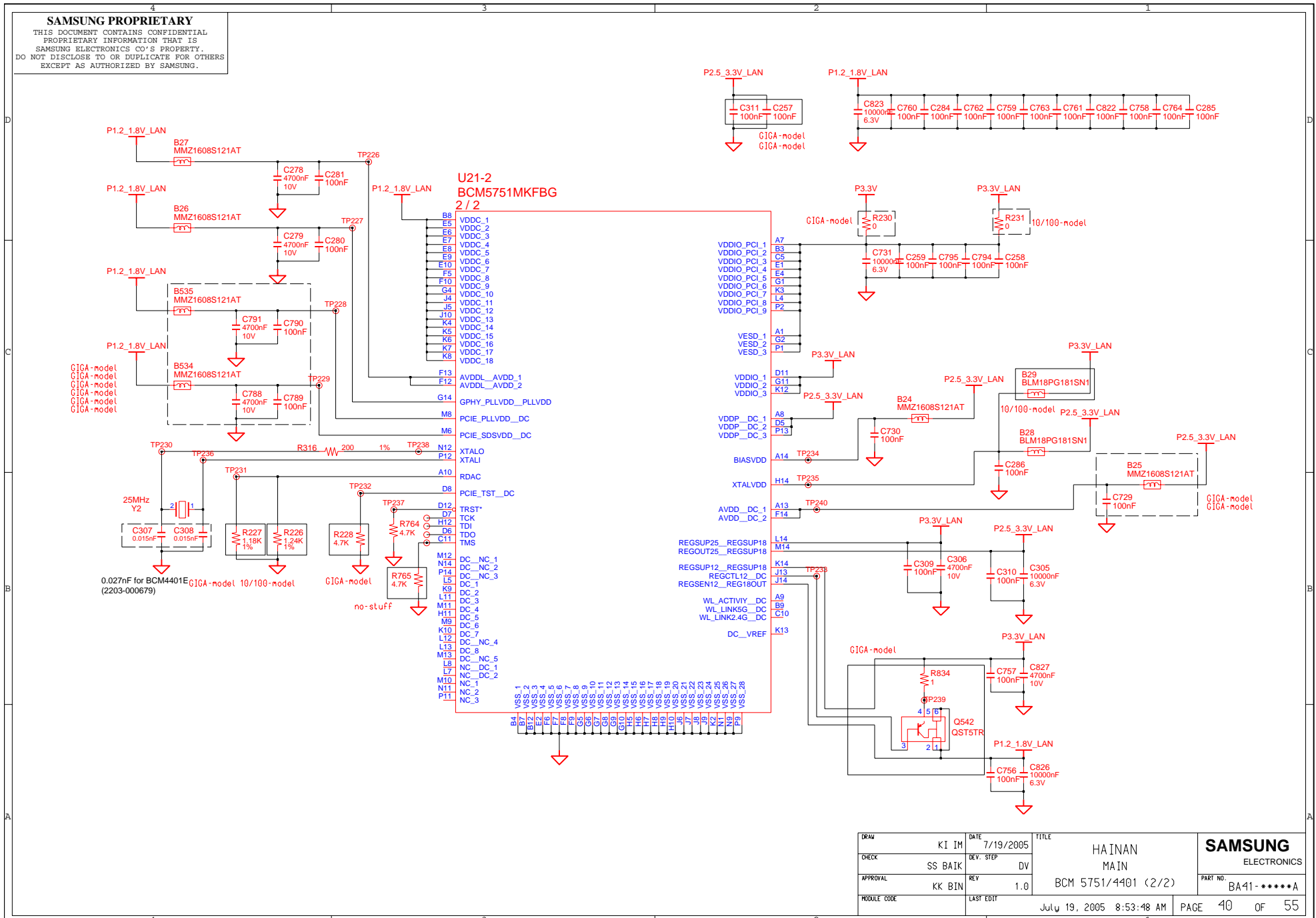
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DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	BCM 5751/4401 (1/2)		PART NO. BA41-*****A
MODULE CODE	undef ined	LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	39	OF 55

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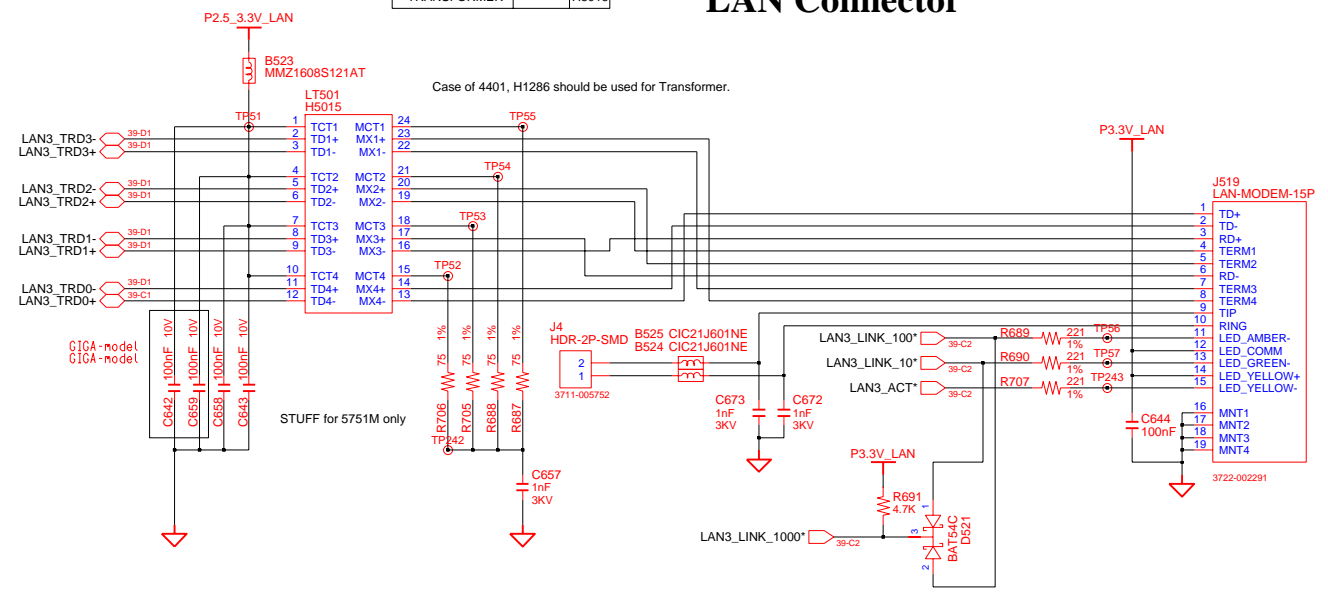


DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	BCM 5751/4401 (2/2)	PART NO.	BA41-*****A
MODULE CODE		LAST EDIT		July 19, 2005 8:53:48 AM	PAGE	40 OF 55

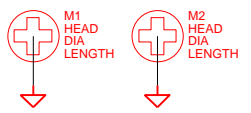
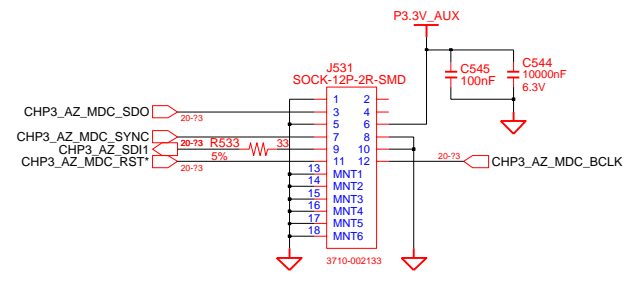
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LAN CONTROLLER	4401E	5751
TRANSFORMER	H1321NL	H5015

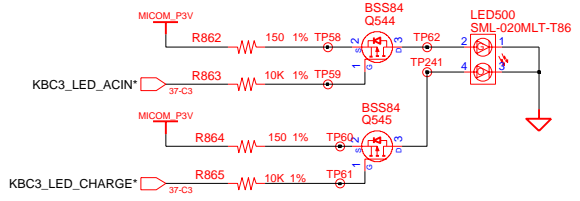
LAN Connector



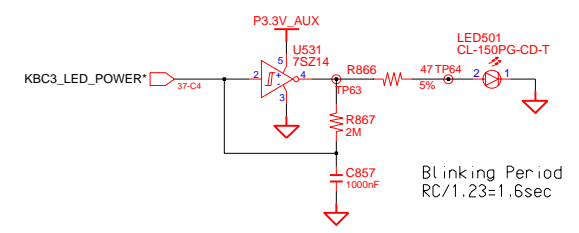
MDC Connector



ADAPTERIN/CHARGING LED



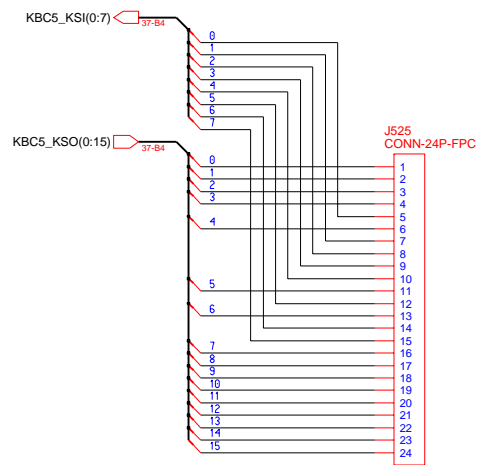
POWER_ON / LB LED



DRAW	IM, KI	DATE	7/19/2005	TITLE	HAINAN MAIN	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	LAN MODEM Conn & LED.		
APPROVAL	BIN, KK	REV	1.0	PART NO. BA41-*****A		PAGE 41 OF 41
MODULE CODE	LAST EDIT		Jul, 19, 2005 9:04:06 AM			

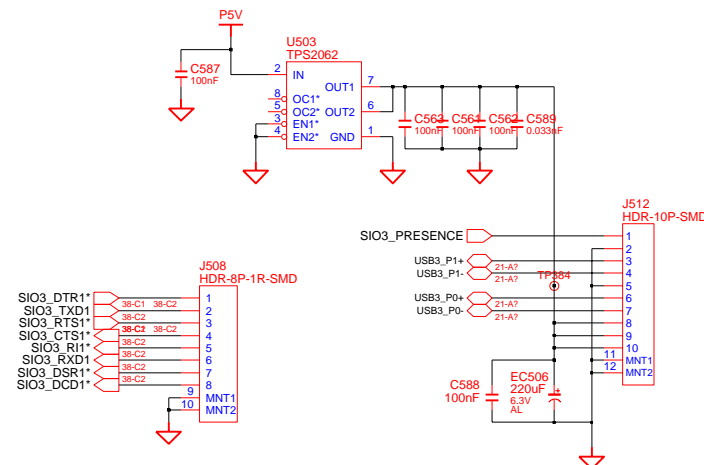
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KEYBOARD

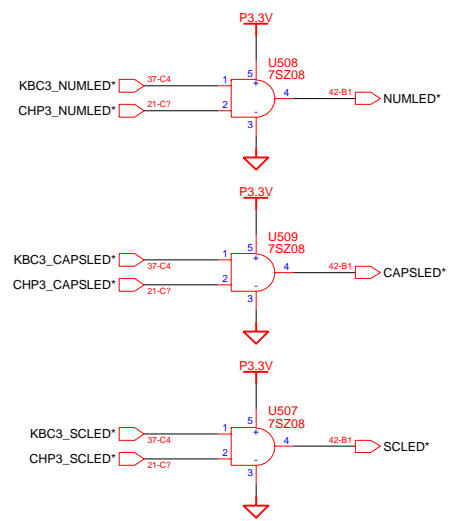


3708-001282

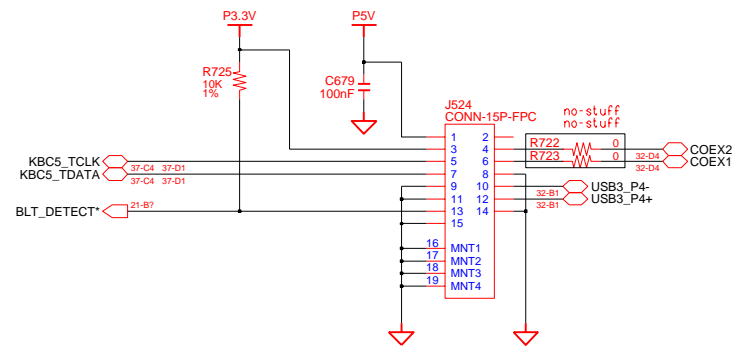
USB_SIO BOARD



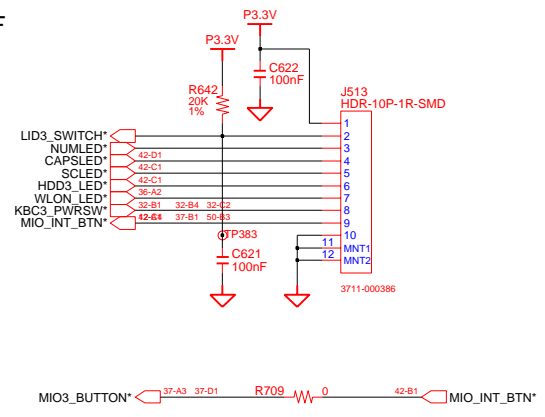
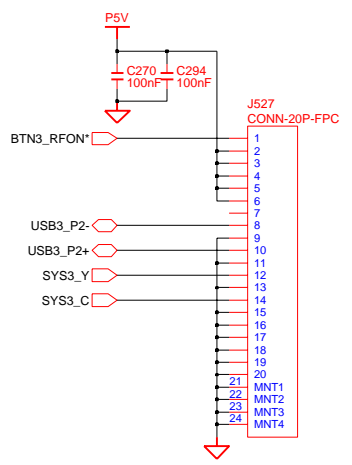
LED BOARD



TOUCHPAD BLUETOOTH I/F



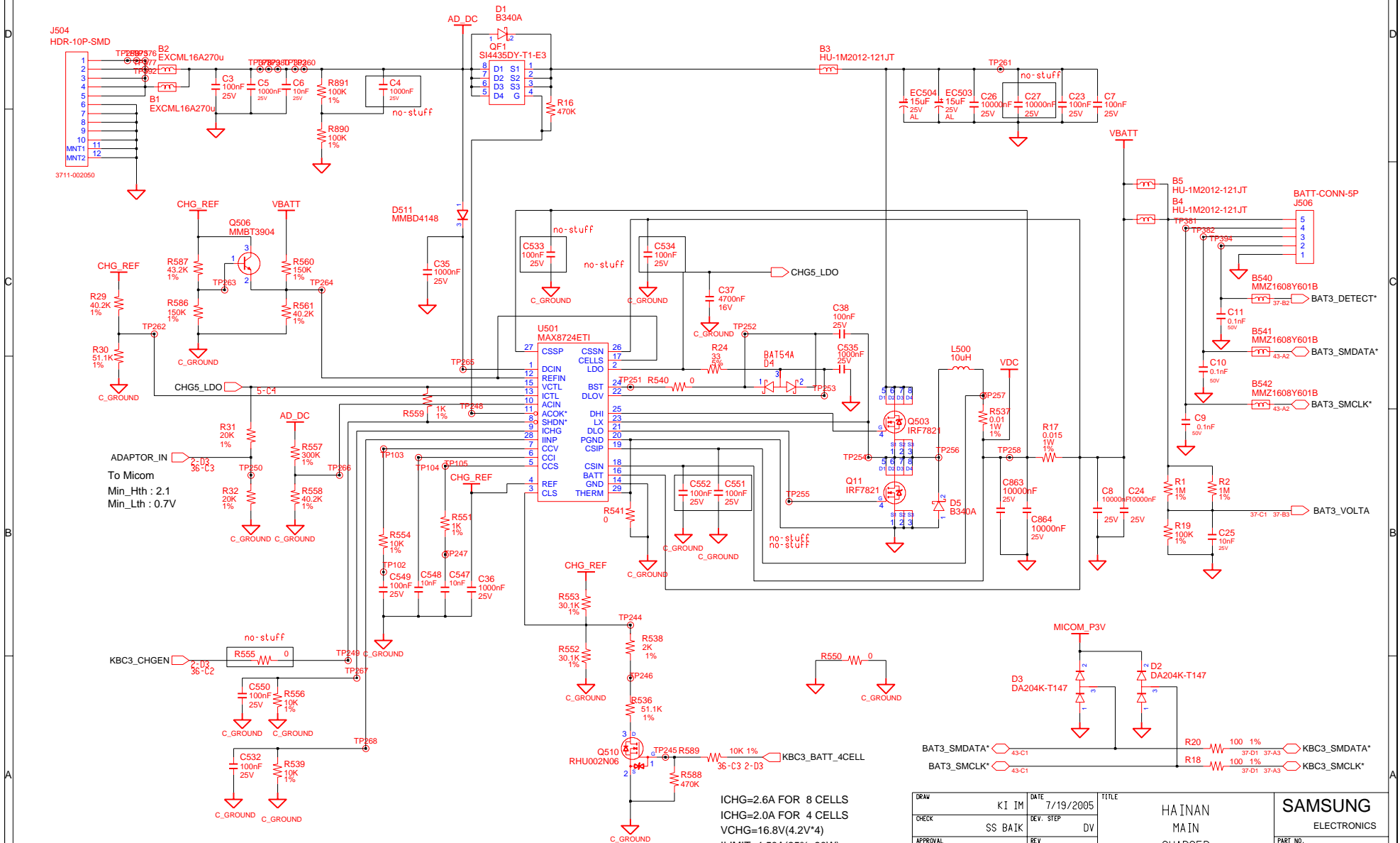
USB_SVHS_RF OFF SWITCH I/F



DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	MAIN		
APPROVAL	KK BIN	REV	1.0	SUB B'D CONNECTOR	PART NO.	BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	42	OF 55

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CHARGER & POWER MANAGEMENT



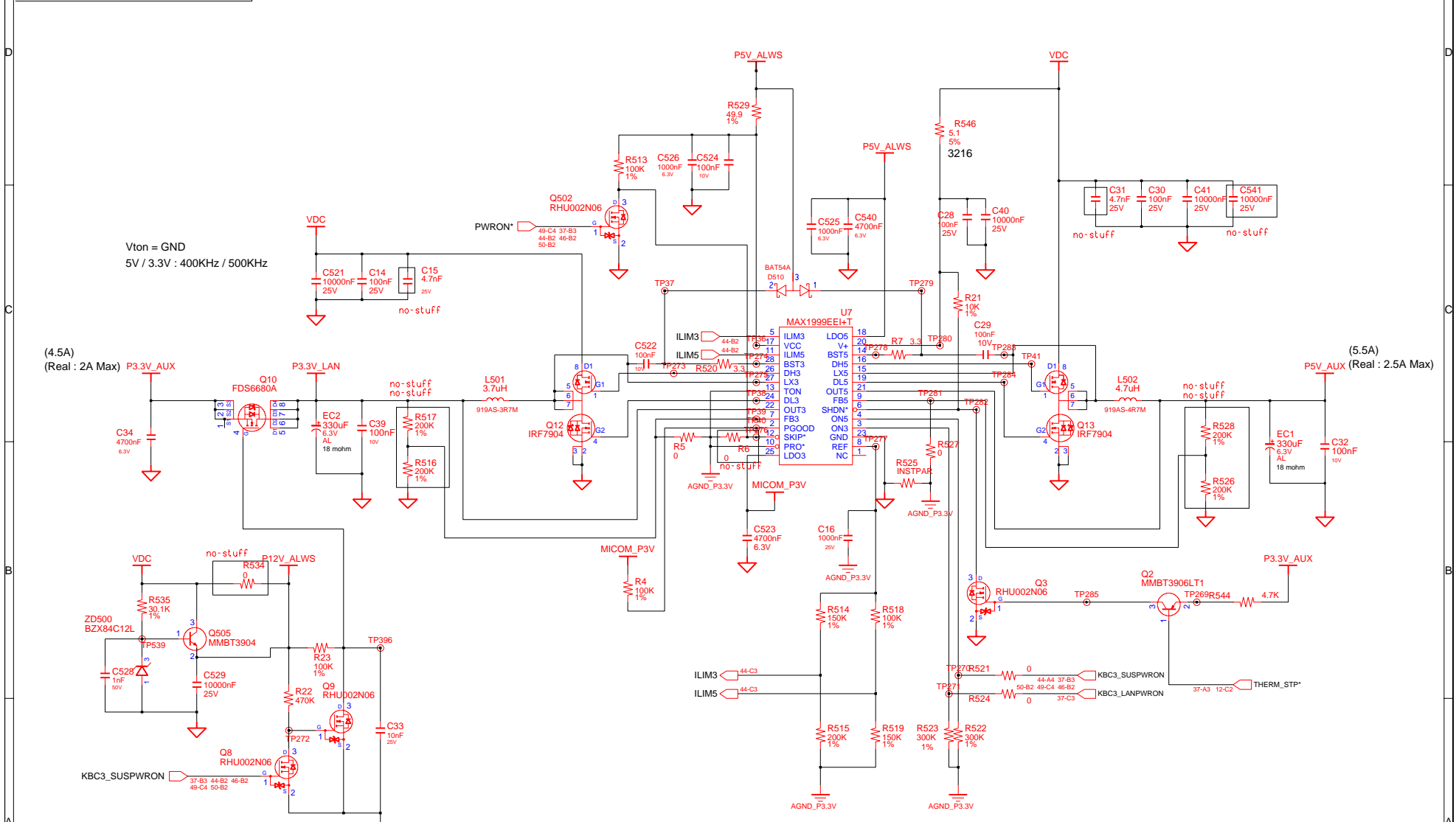
ADAPTOR_IN
 To Micom
 Min_Hth : 2.1
 Min_Lth : 0.7V

ICHG=2.6A FOR 8 CELLS
 ICHG=2.0A FOR 4 CELLS
 VCHG=16.8V(4.2V*4)
 ILIMIT=4.50A(85%*90W)

DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	43 OF 55	

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P3.3V_LAN/AUX & P5V_AUX



(4.5A)
 (Real : 2A Max) P3.3V_AUX

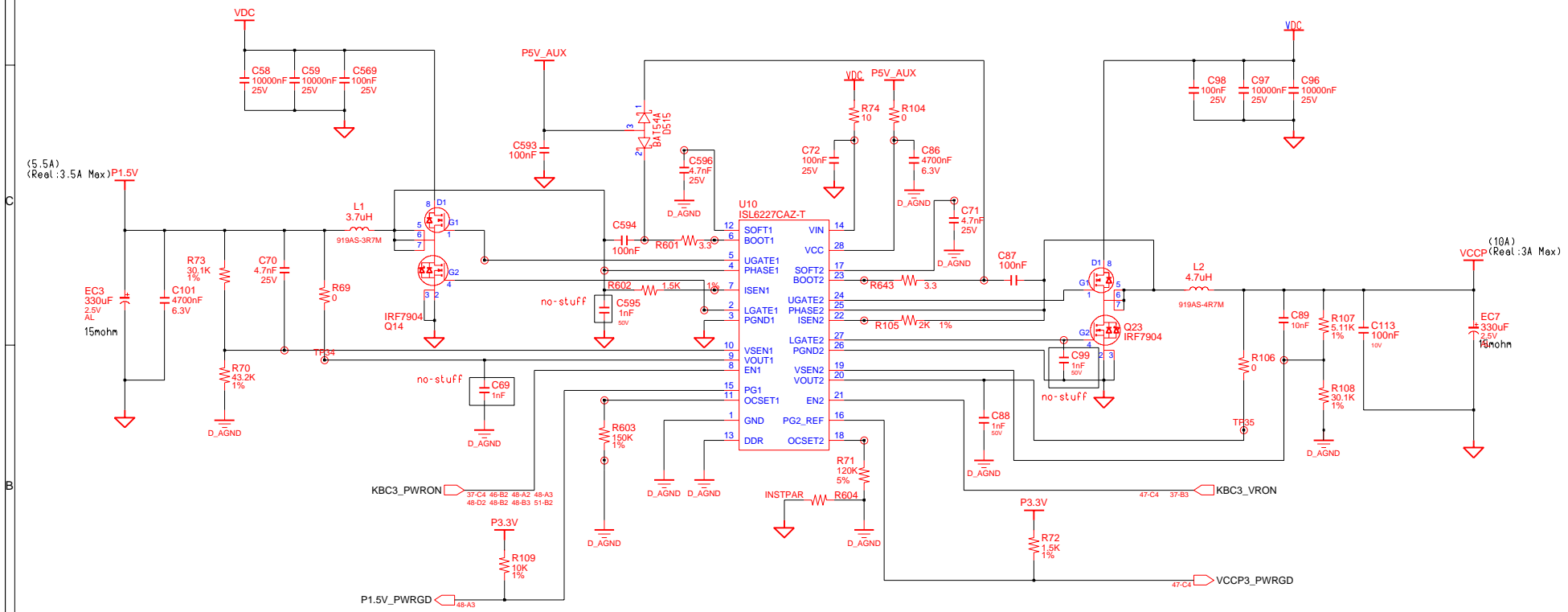
(5.5A)
 (Real : 2.5A Max) P5V_AUX

Vton = GND
 5V / 3.3V : 400KHz / 500KHz

DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN POWER	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	P3.3V LAN & P5V_AUX		
APPROVAL	KK BIN	REV	1.0	July 19, 2005 8:53:48 AM		PART NO. BA41-*****A
MODULE CODE		LAST EDIT		PAGE	44	

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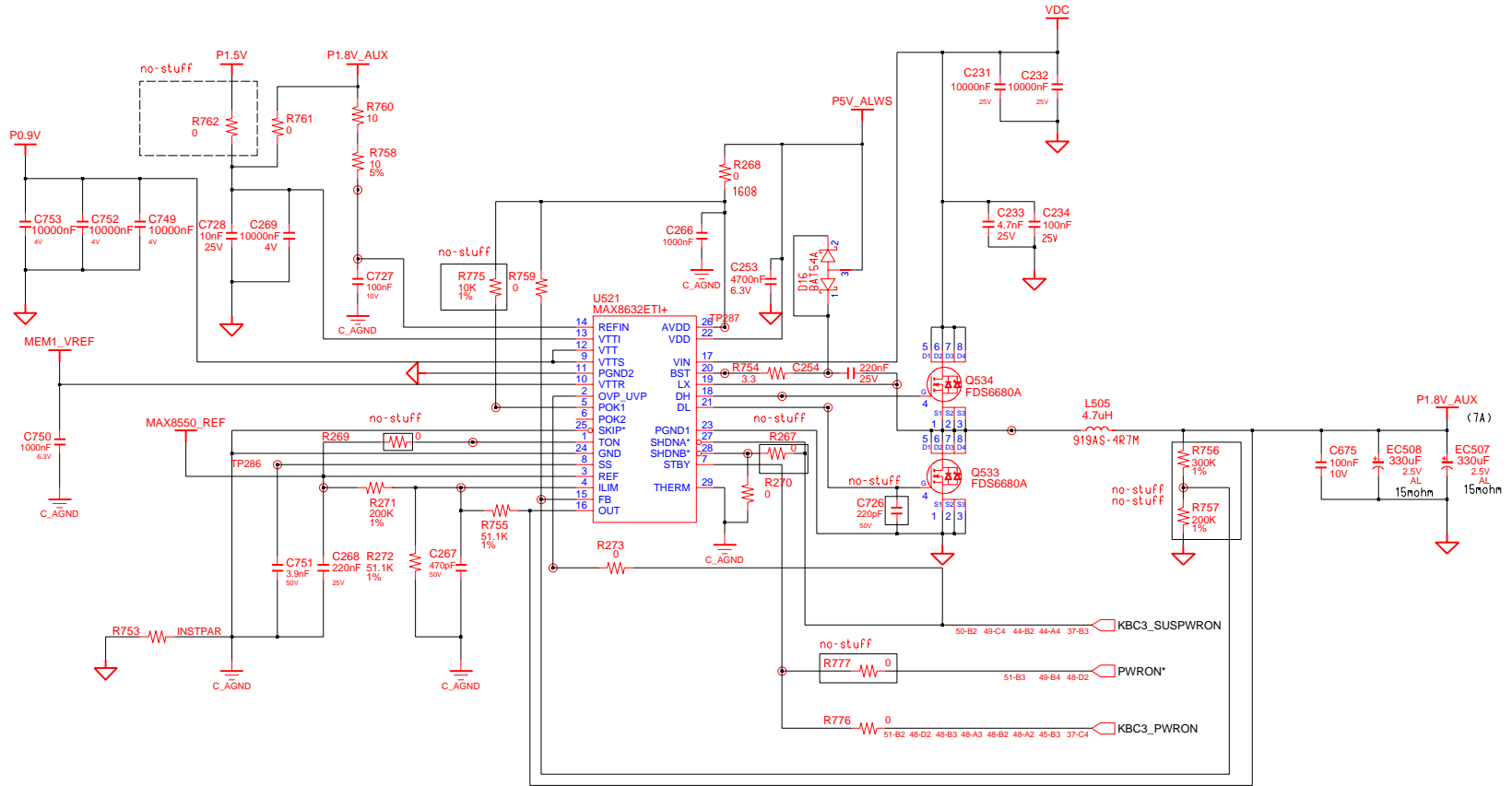
P1.5V & VCCP (1.05V)



DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN POWER P1.5V & VCCP	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV			PART NO. BA41-*****A
APPROVAL	KK BIN	REV	1.0			
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	45	OF 55

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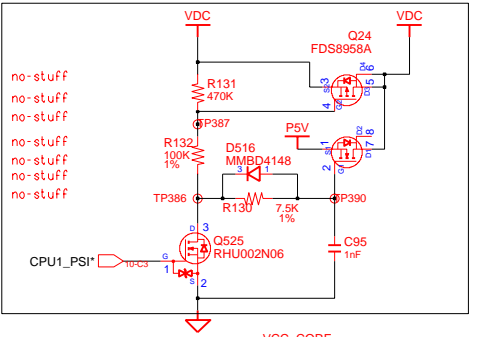
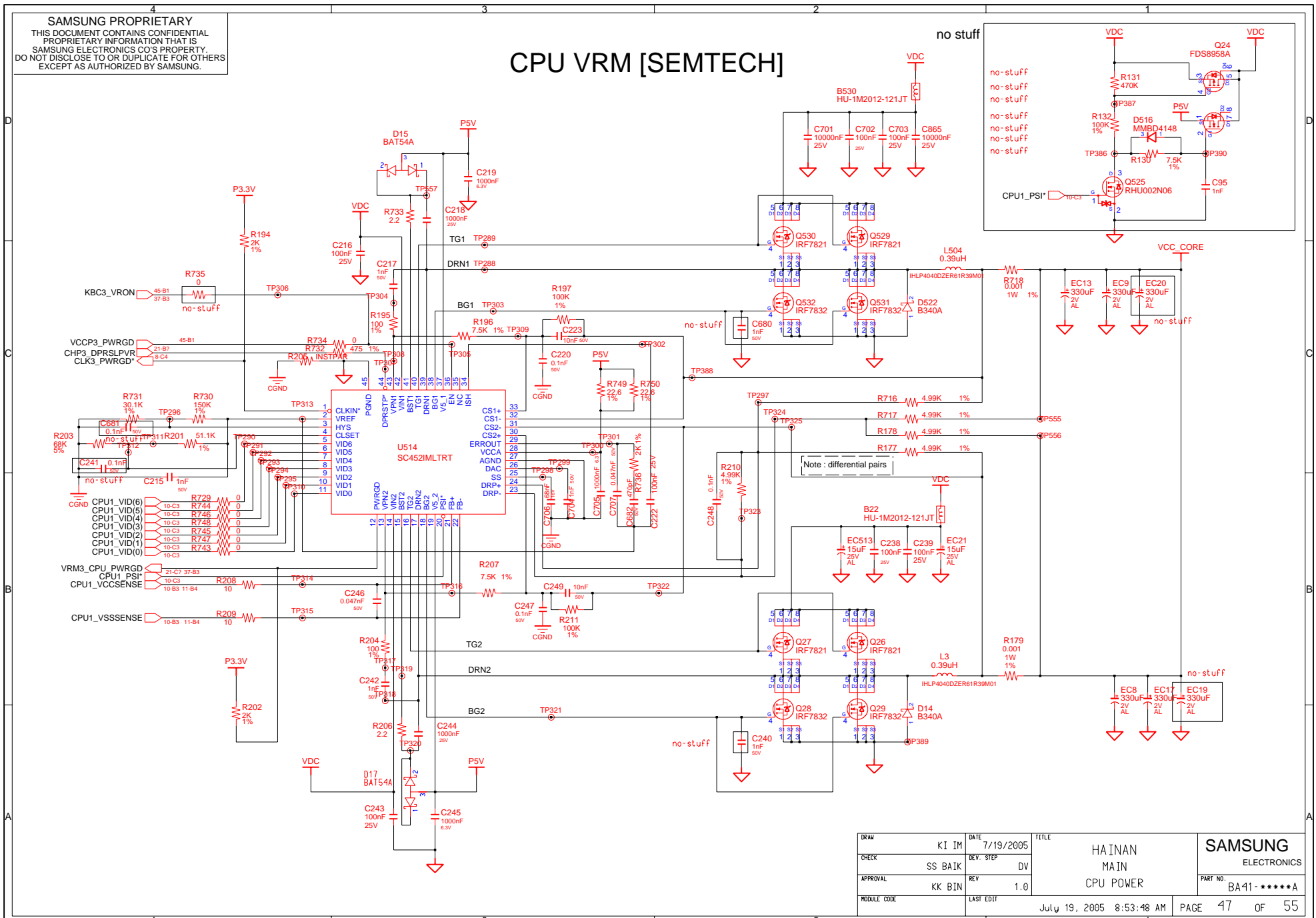
DDR2 Power



DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV		MAIN	
APPROVAL	KK BIN	REV	1.0		DDR2 POWER	PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	46	OF 55

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CPU VRM [SEMTECH]



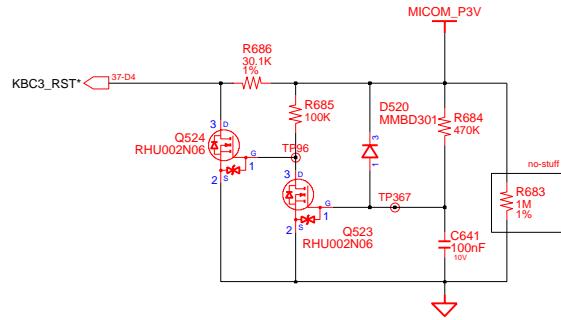
DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA41 - *****A
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE		LAST EDIT				
				July 19, 2005 8:53:48 AM		PAGE 47 OF 55

COM-22C-015(1996.6.5) REV. 3

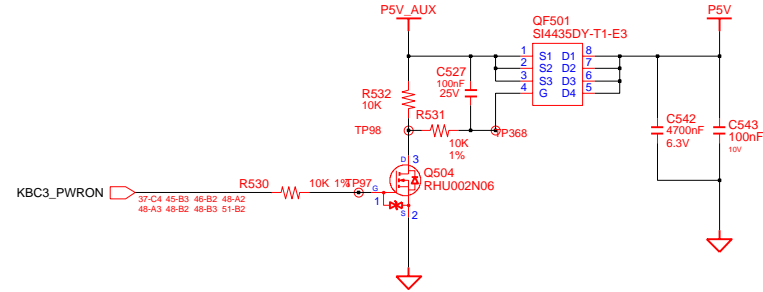
d:\users\mobile22\mentor\hainan\hainan_v

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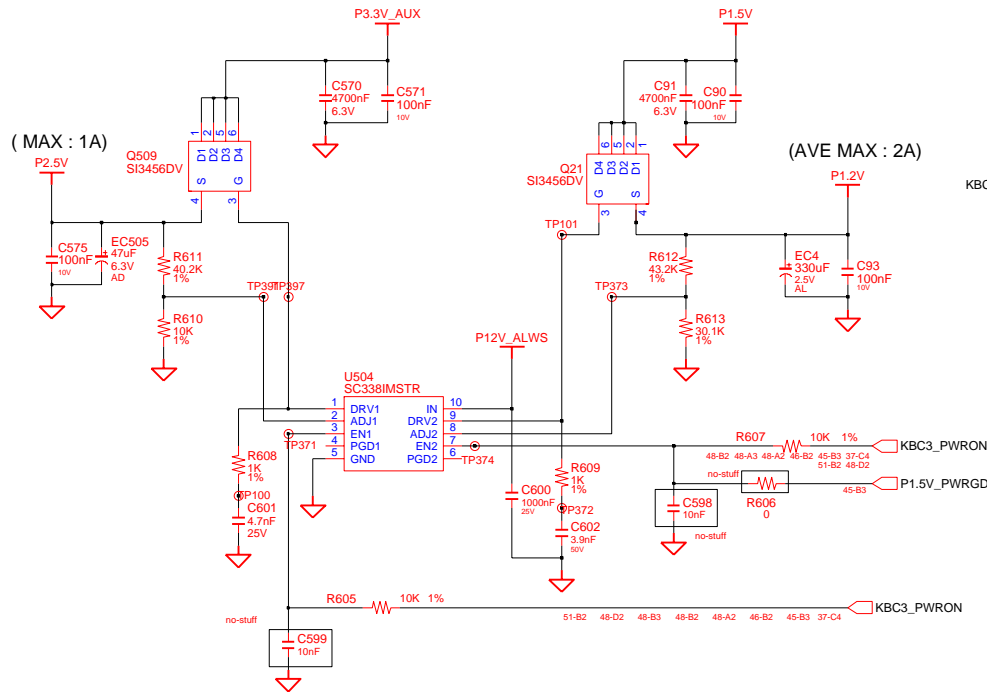
MICOM RESET



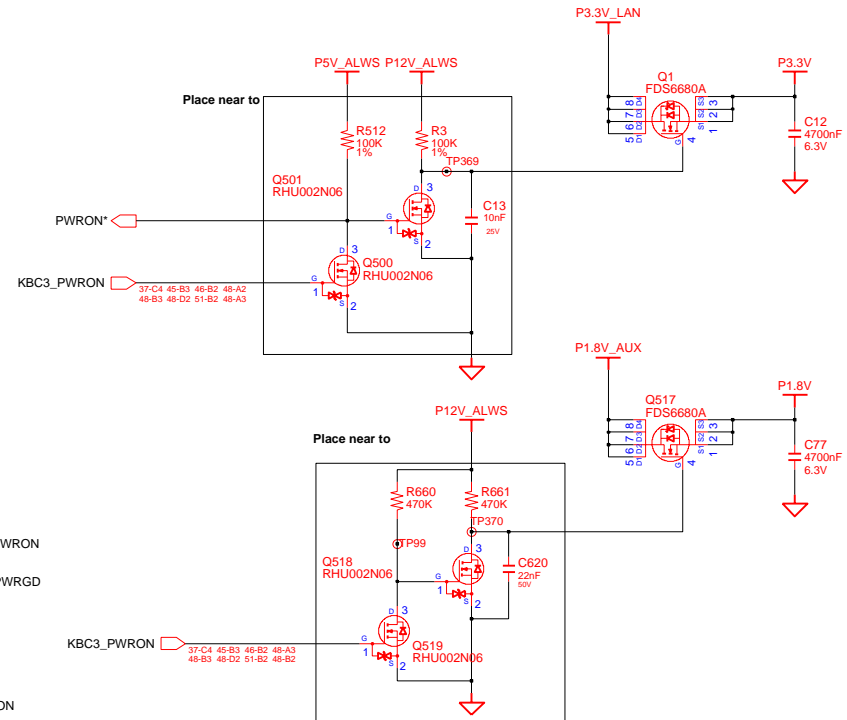
Switched Power On (P5V)



P1.2V / P2.5V POWER

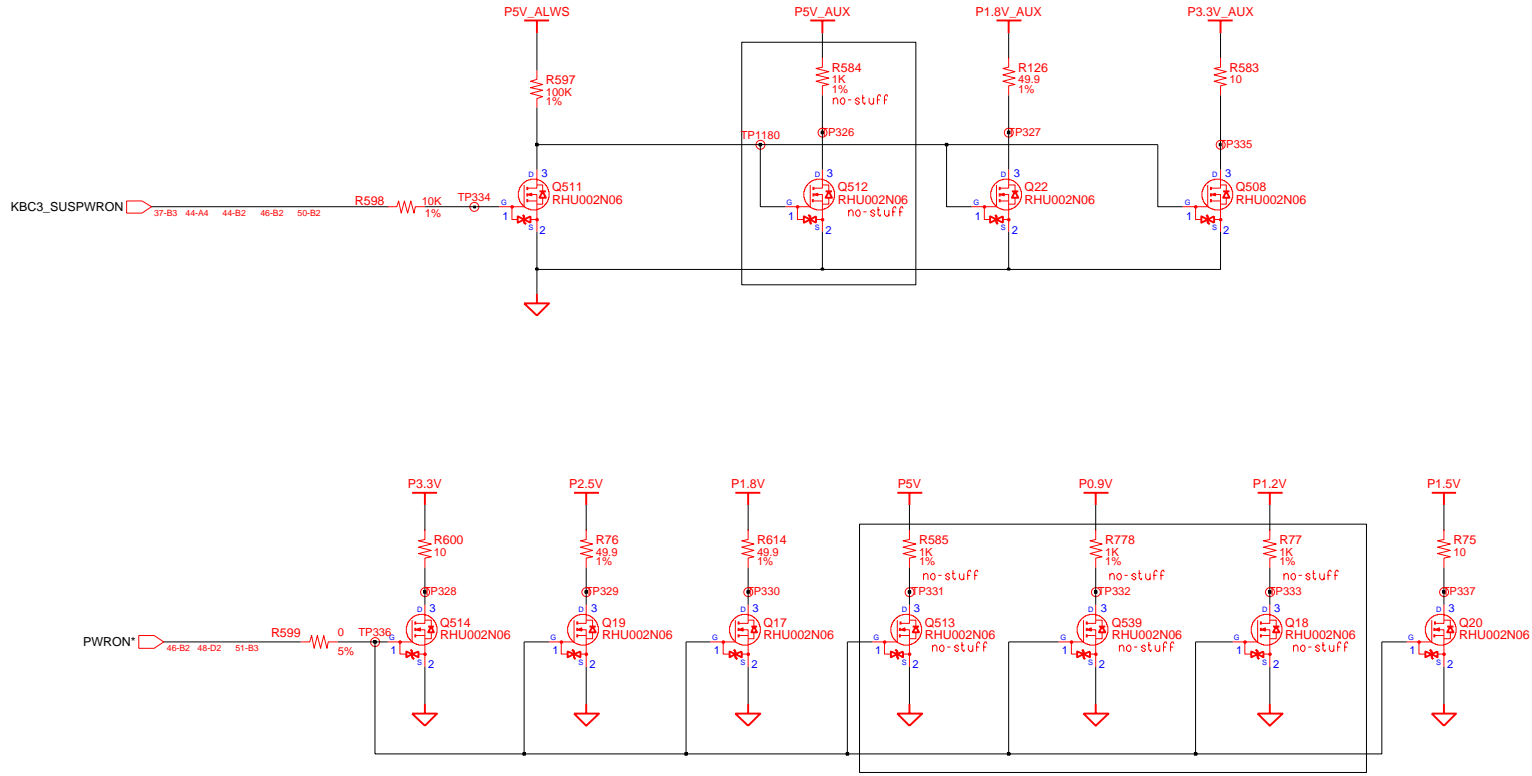


Switched Power On (P3.3V & 1.8V)



DATE	7/19/2005	TITLE	HAINAN MAIN	SAMSUNG ELECTRONICS
DEV. STEP	DV	MICOM & SWITCHED POWER		
DRIVER	KI IM	APPROVAL	KK BIN	PART NO. BA41-*****A
CHECK	SS BAIK	MODULE CODE		
LAST EDIT				PAGE 48 OF 55
July 19, 2005 8:53:48 AM				

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DRW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	GFX POWER		
APPROVAL	KK BIN	REV	1.0	Discharging Logic		PART NO. BA41-*****A
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	49	OF 55

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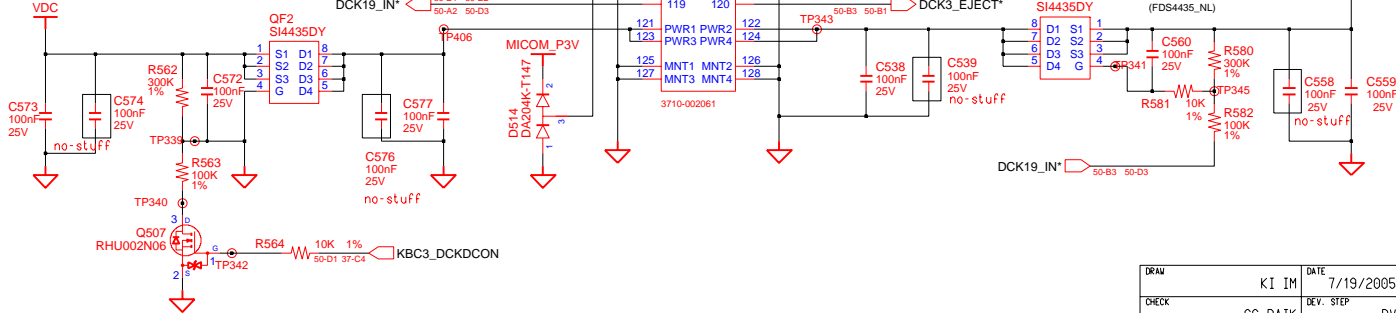
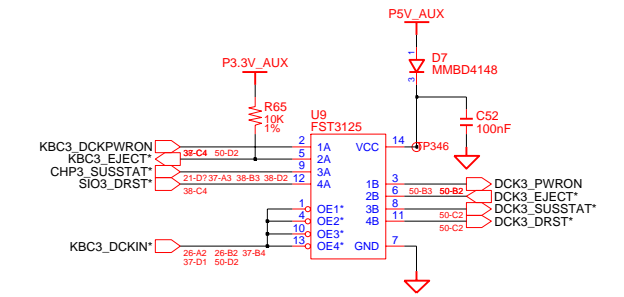
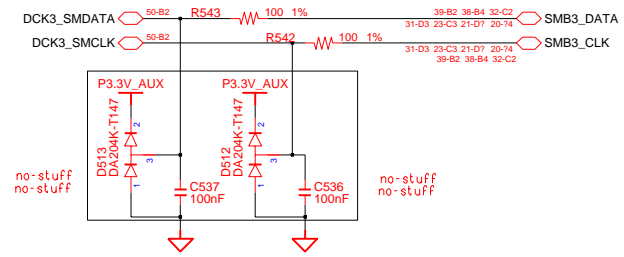
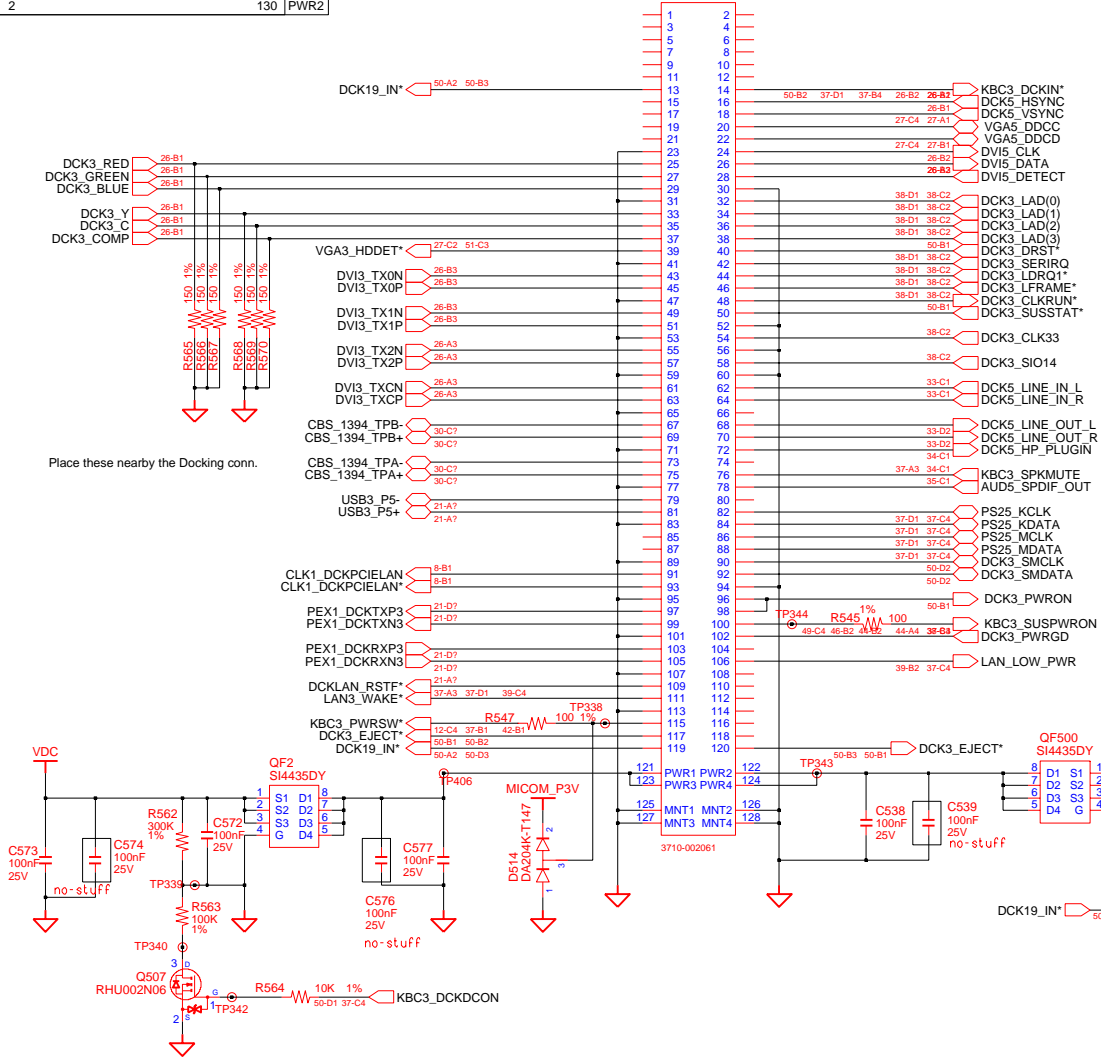
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DOCKING CONNECTOR (130PIN)

Docking Placement



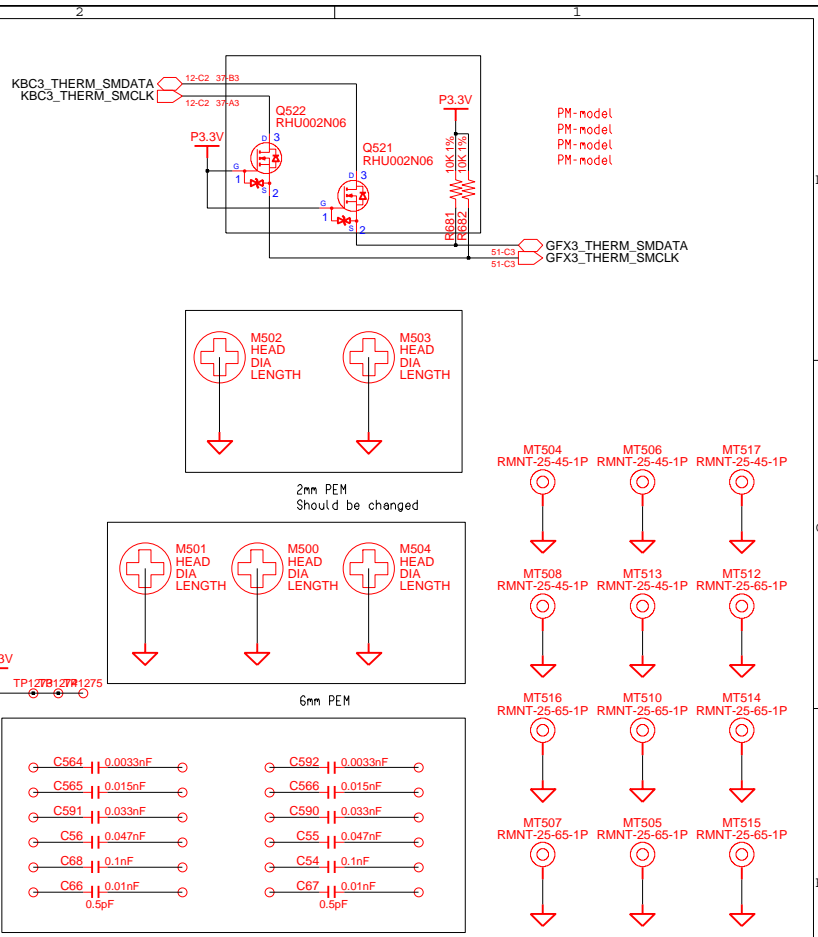
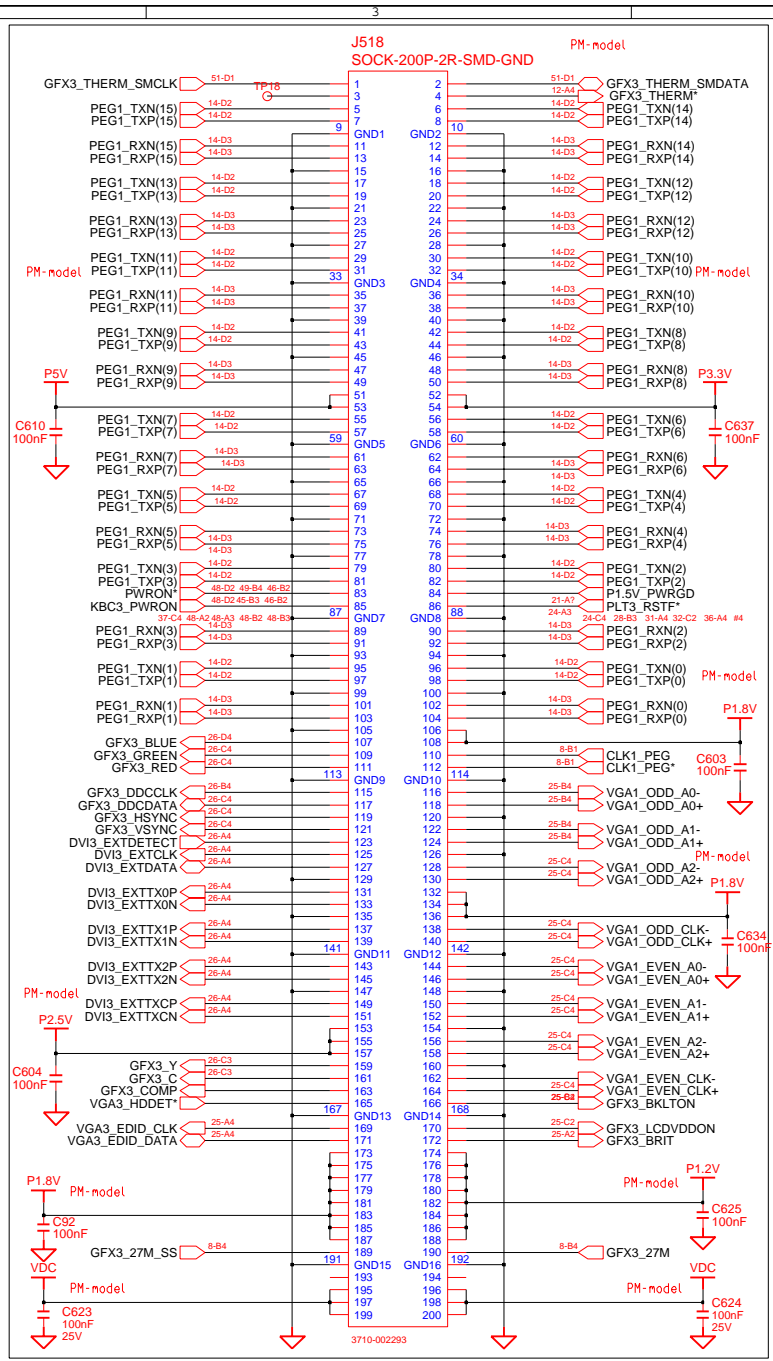
DOCK1 SOCK-DOCKING-120P



DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN MAINBD	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	Docking connector		
APPROVAL	KK BIN	REV	1.0	July 19, 2005 8:53:48 AM		PART NO. BA41-*****A
MODULE CODE		LAST EDIT		PAGE 50 OF 55		

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These are for ICT using.

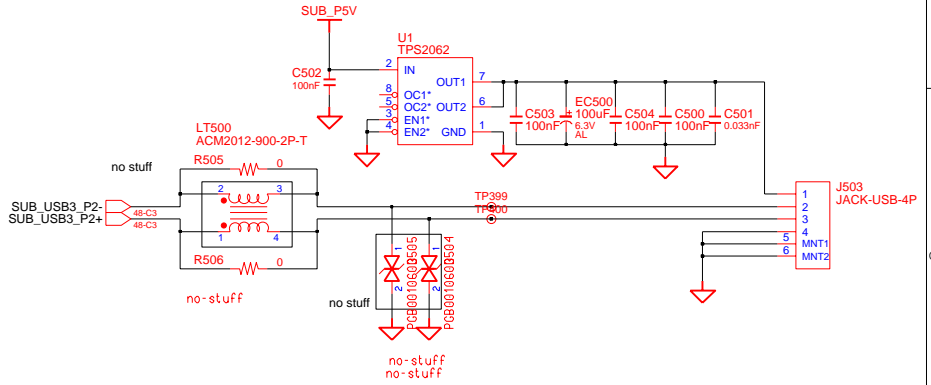
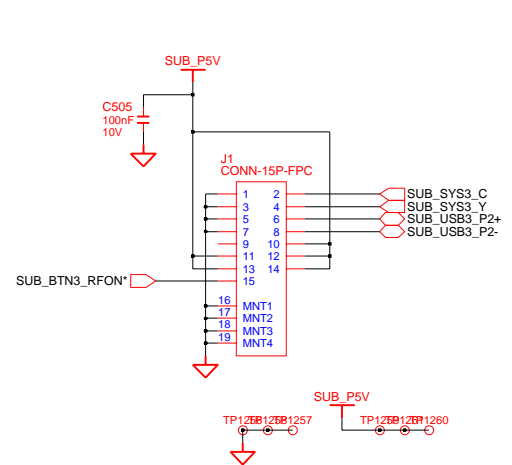
PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	K1 IM	DATE	7/19/2005	TITLE	HAINAN MAIN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	Ext Gfx connector		
APPROVAL	KK BIN	REV	1.0	July 19, 2005 8:53:48 AM		PART NO. BA41-*****A
MODULE CODE		LAST EDIT		PAGE 51 OF 55		

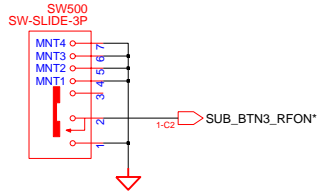
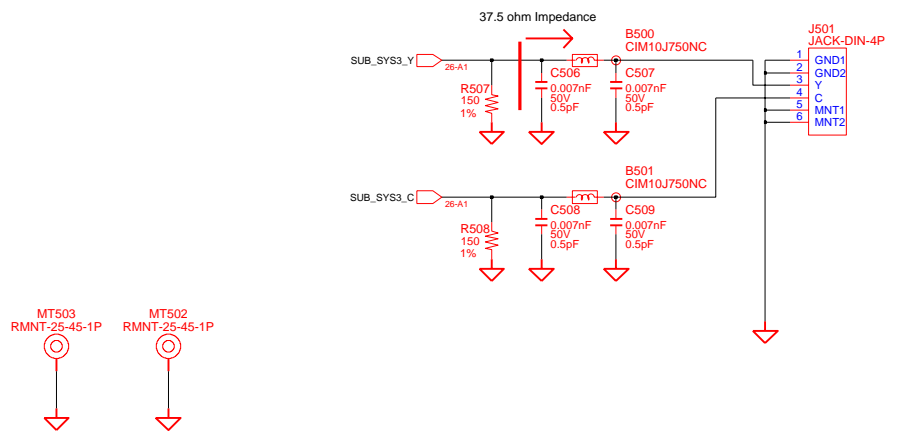
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USB Connector

USB_SVHS_SLIDE SWITCH BOARD



TV-OUT(S-VHS,COMPONENT)

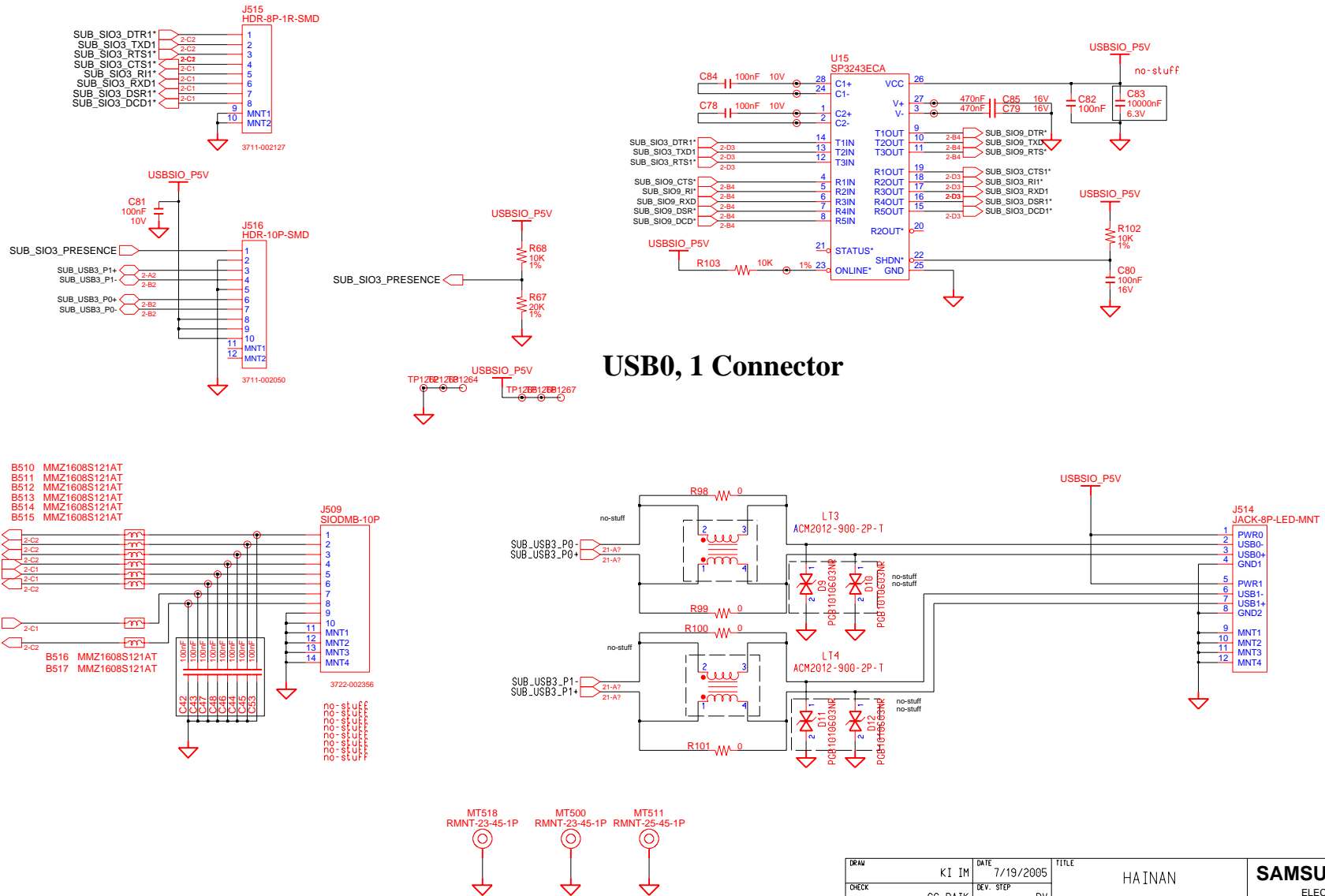


DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN POWER	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	Audio Sub B'd	PART NO.	
APPROVAL	KK BIN	REV	1.0		BA41-*****A	
MODULE CODE	undefined	LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	52	OF 55

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USB_SIO BOARD



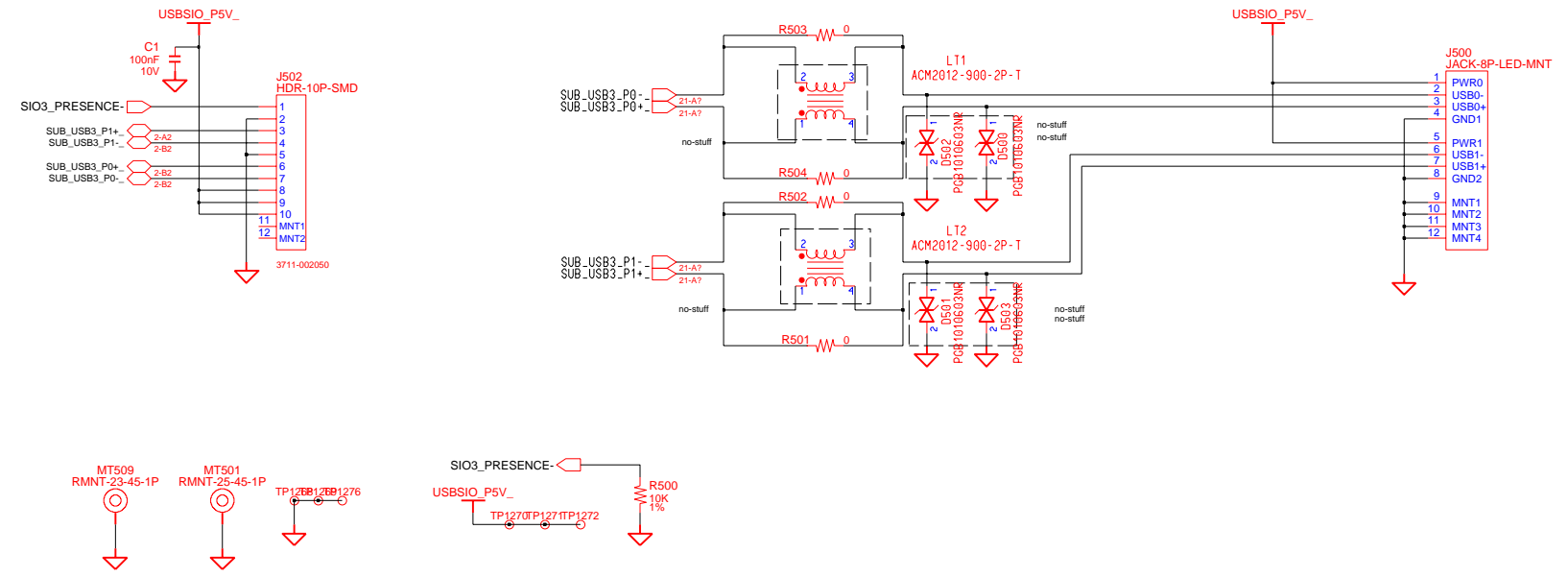
USB0, 1 Connector

DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV	REVISION HISTORY	PART NO.	
APPROVAL	KK BIN	REV	1.0		BA41 - *****A	
MODULE CODE		LAST EDIT	July 19, 2005 8:53:48 AM	PAGE	53	OF 55

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USB & DMB SUBBOARD

USB0, 1 Connector



DRAW	KI IM	DATE	7/19/2005	TITLE	HAINAN POWER AUDIO SUB B'D	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	DV			
APPROVAL	KK BIN	REV	1.0			PART NO. BA41-*****A
MODULE CODE		LAST EDIT		July 19, 2005 8:53:48 AM	PAGE 54 OF 55	

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EXT GFx

CPU :
Chip Set : NVIDIA 7X series
Remarks :

Model Name : HABANA EXT GFx
PBA Name :
PCB Code :
Dev. Step : MP
Revision : 1.0
T.R. Date : 2005.11.14

DRAW	CHECK	APPROVAL
SE LEE	ES CHO	BL LEE

Sheet 1. COVER
Sheet 2. GFX CONNECTOR
Sheet 3~6. GFX CHIP (G73M)
Sheet 7. GFX STRAP OPTION
Sheet 8~9. GDDR3 MEMORY
Sheet 10. GDDR3 TERMINATION, THERMAL SENSOR, HDCP ROM
Sheet 11. GFX CORE REGULATOR

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX COVER	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP			
APPROVAL	LEE, BL	REV	1.0			
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	PAGE	1	OF 12

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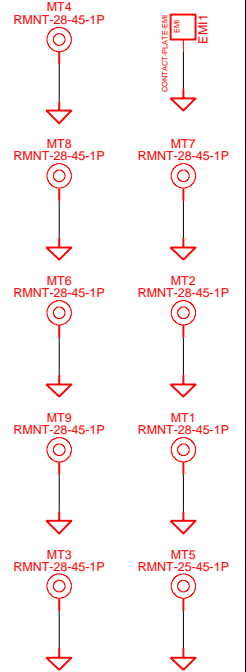
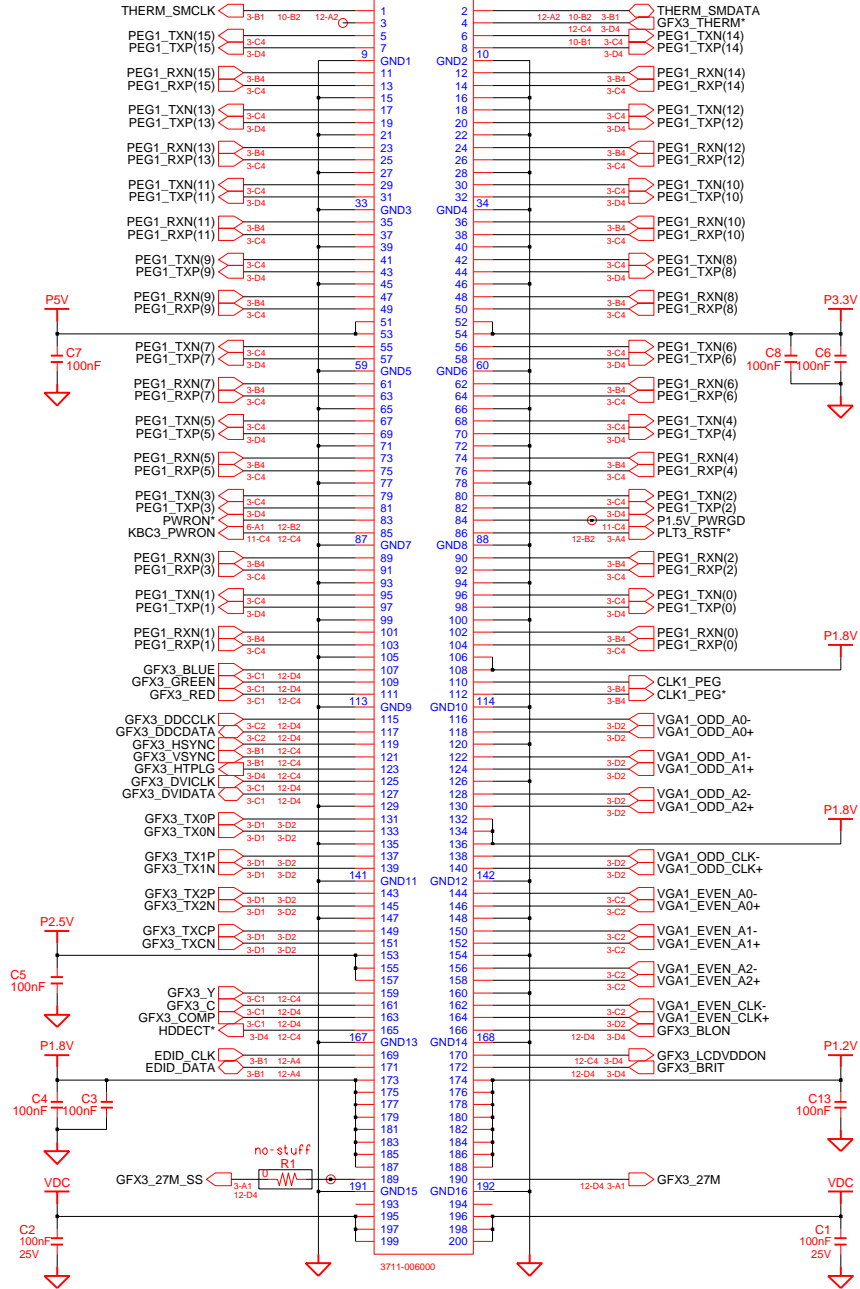
D

C

B

A

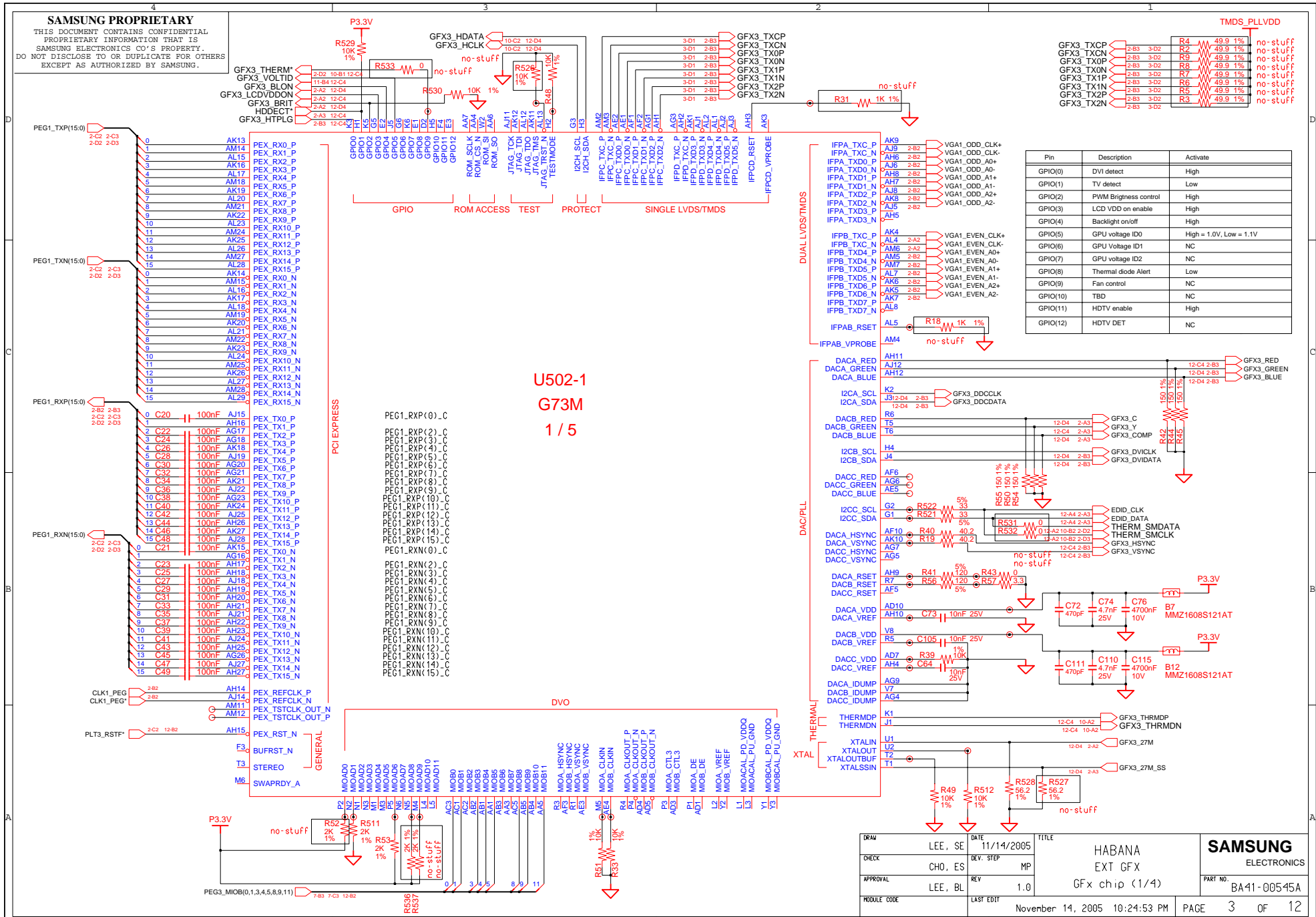
J501 HEAD-200P-2R-SMD-GND



DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	Gfx connector		
APPROVAL	LEE, BL	REV	1.0			PART NO. BA41-00545A
MODULE CODE	LAST EDIT		November 14, 2005 10:24:53 PM		PAGE	2 OF 12

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Pin	Description	Activate
GPIO(0)	DVI detect	Low
GPIO(1)	TV detect	High
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU voltage ID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU voltage ID2	NC
GPIO(8)	Thermal diode Alert	Low
GPIO(9)	Fan control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	High
GPIO(12)	HDTV DET	NC

Pin	Description	Activate
GF3X_TXCP	2-83 3-02	R4 49.9 1% no-stuff
GF3X_TXCN	2-83 3-02	R9 49.9 1% no-stuff
GF3X_TXOP	2-83 3-02	R7 49.9 1% no-stuff
GF3X_TXIP	2-83 3-02	R8 49.9 1% no-stuff
GF3X_TXIN	2-83 3-02	R6 49.9 1% no-stuff
GF3X_TX2P	2-83 3-02	R5 49.9 1% no-stuff
GF3X_TX2N	2-83 3-02	R3 49.9 1% no-stuff

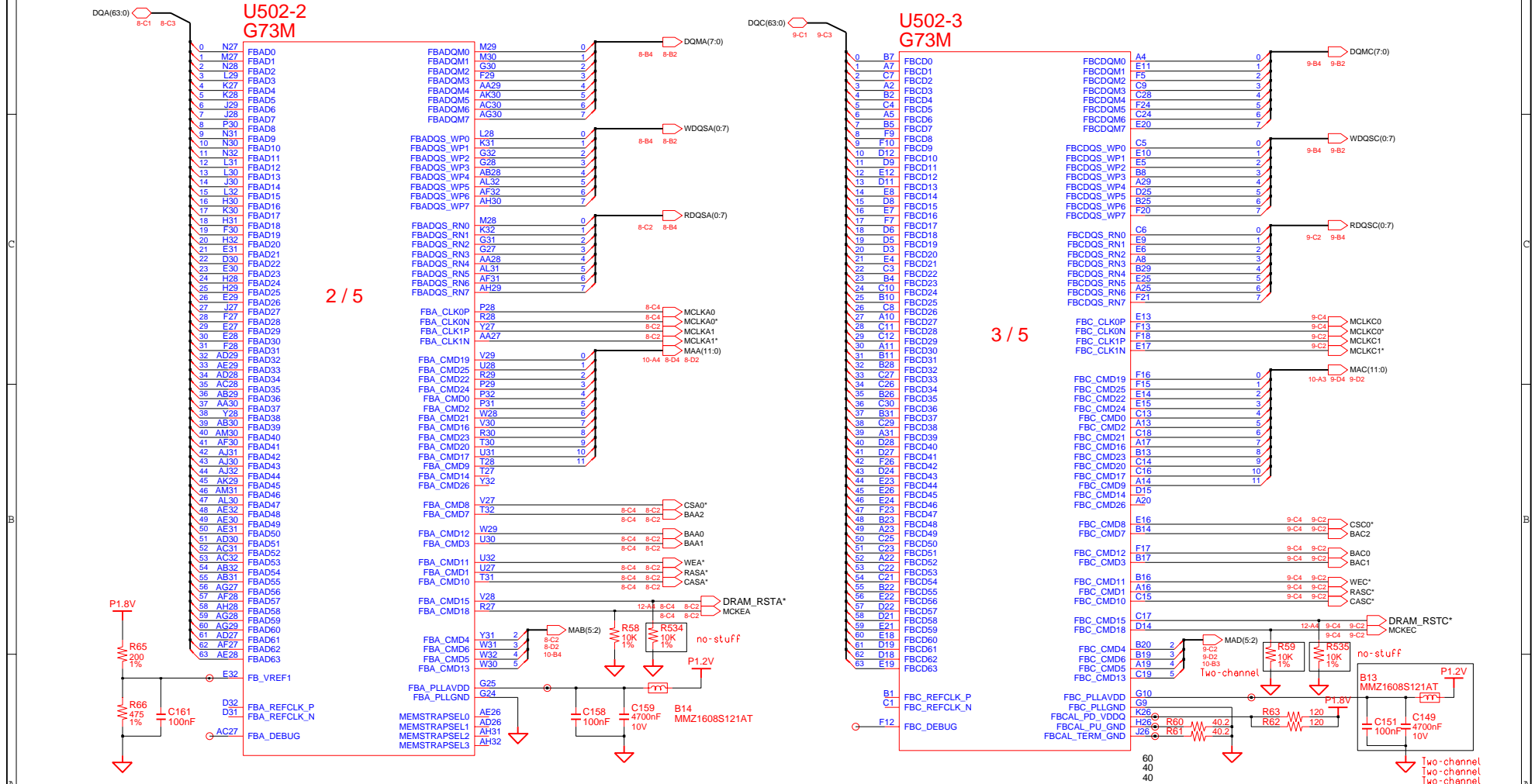
U502-1
G73M
1 / 5

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	
CHECK	CHO, ES	DEV. STEP	MP	Gfx chip (1/4)		
APPROVAL	LEE, BL	REV	1.0	PART NO. BA41-00545A		November 14, 2005 10:24:53 PM PAGE 3 OF 12
MODULE CODE	LAST EDIT					

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Graphic Memory I/F (Using FBA Channel)

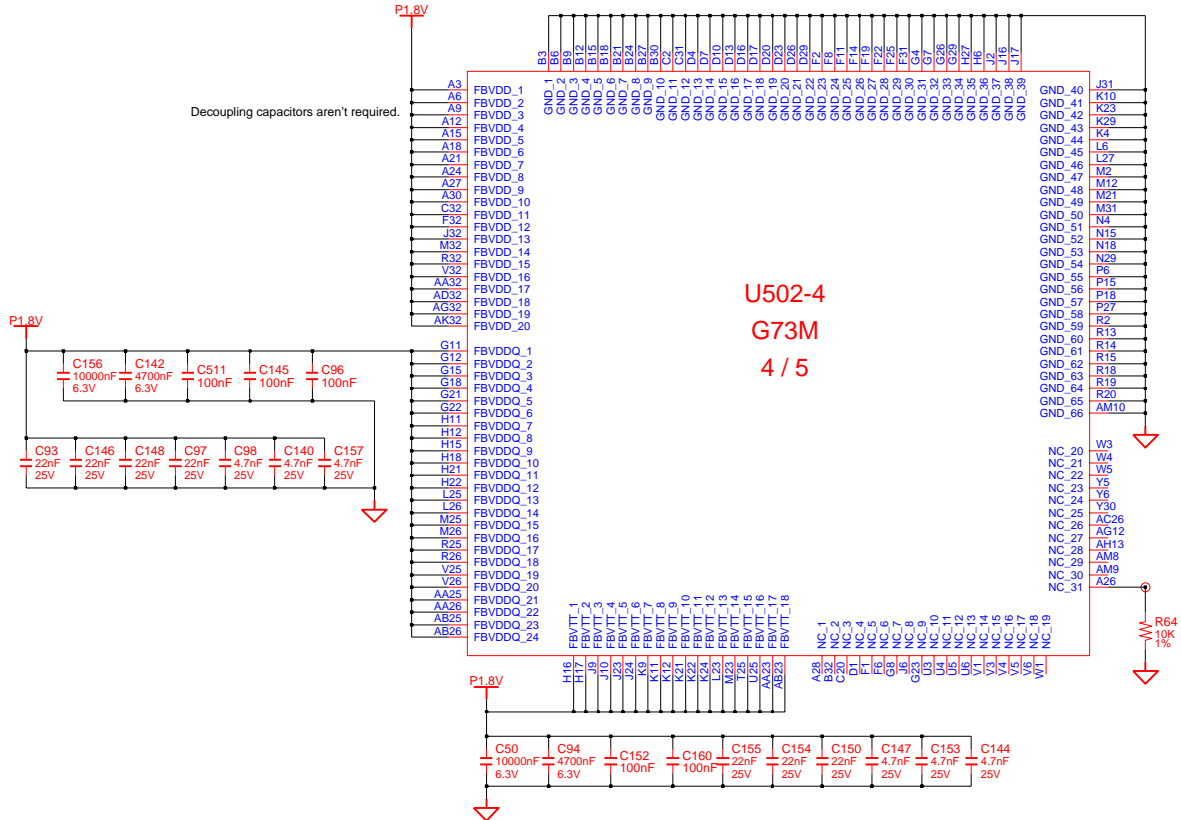
Graphic Memory I/F (Using FBC Channel)



DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
DEV. STEP	MP	REV	GfX chip (2/4)	
DRAW	LEE, SE	REV	1.0	PART NO. BA41-00545A
CHECK	CHO, ES	LAST EDIT	November 14, 2005 10:24:53 PM	PAGE 4 OF 12
APPROVAL	LEE, BL			
MODULE CODE				

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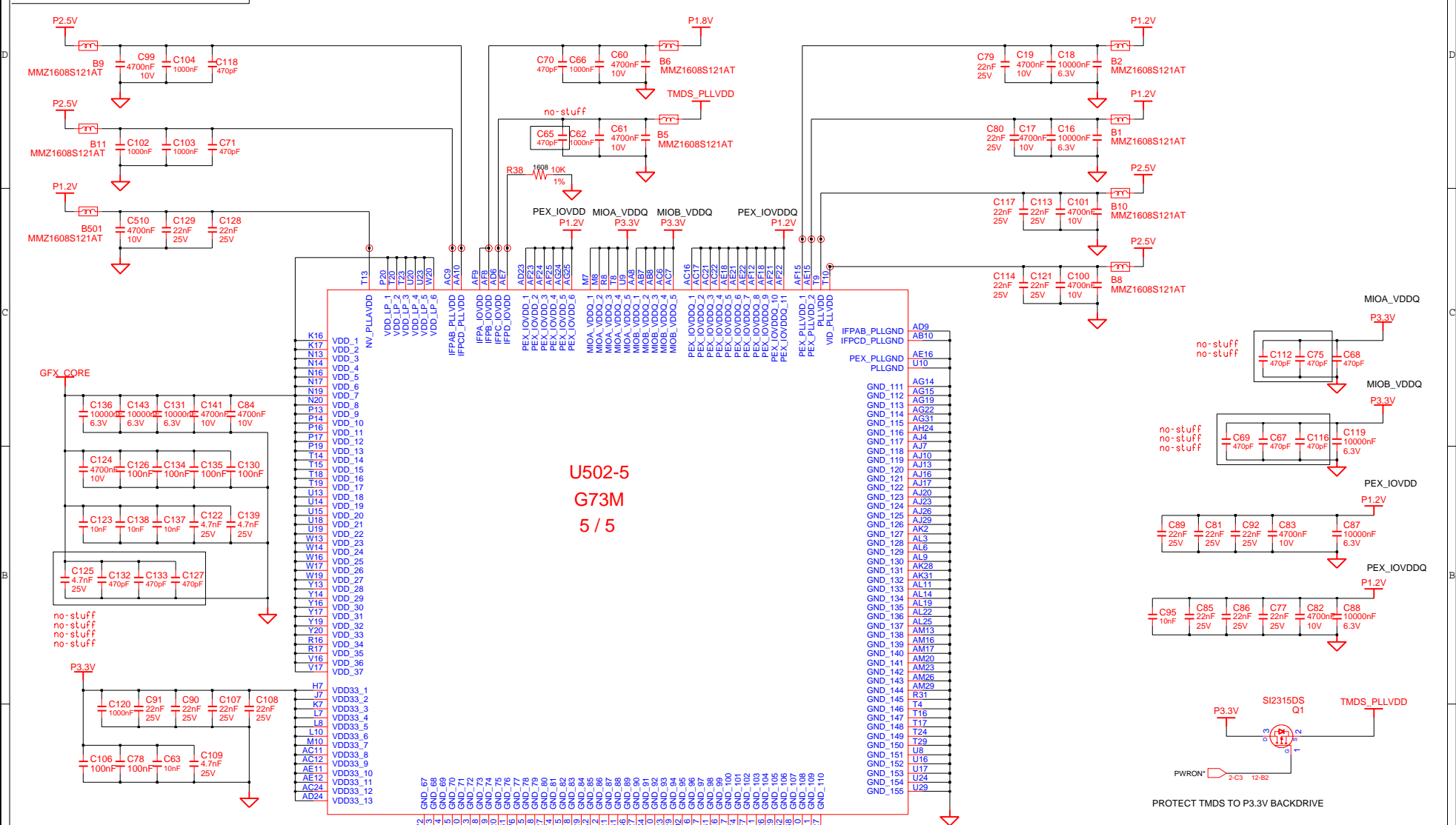
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DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS PART NO. BA41-00545A
CHECK	CHO, ES	DEV. STEP	MP	GFx chip (3/4)		
APPROVAL	LEE, BL	REV	1.0			
MODULE CODE	LAST EDIT		November 14, 2005 10:24:53 PM		PAGE	5 OF 12

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U502-5
G73M
5/5

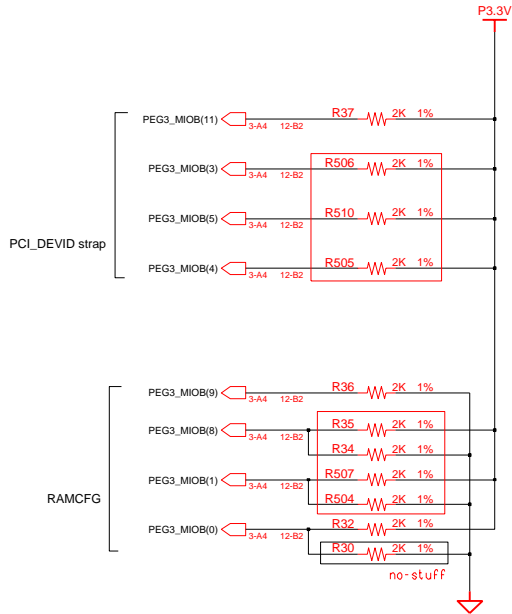
PROTECT TMDS TO P3.3V BACKDRIVE

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	GFX chip (4/4)		
APPROVAL	LEE, BL	REV	1.0			PART NO. BA41-00545A
MODULE CODE	LAST EDIT		November 14, 2005 10:24:53 PM		PAGE	6 OF 12

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	R37	R506	R510	R505
72M-V	no-stuff	stuff	stuff	stuff
72M	stuff	no-stuff	no-stuff	no-stuff
73M	stuff	no-stuff	no-stuff	no-stuff



	R35	R34	R507	R504
SS 256Mb	stuff	no-stuff	stuff	no-stuff
INF 256Mb	stuff	no-stuff	no-stuff	stuff
SS 512Mb	no-stuff	stuff	stuff	no-stuff
INF 512Mb	no-stuff	stuff	no-stuff	stuff

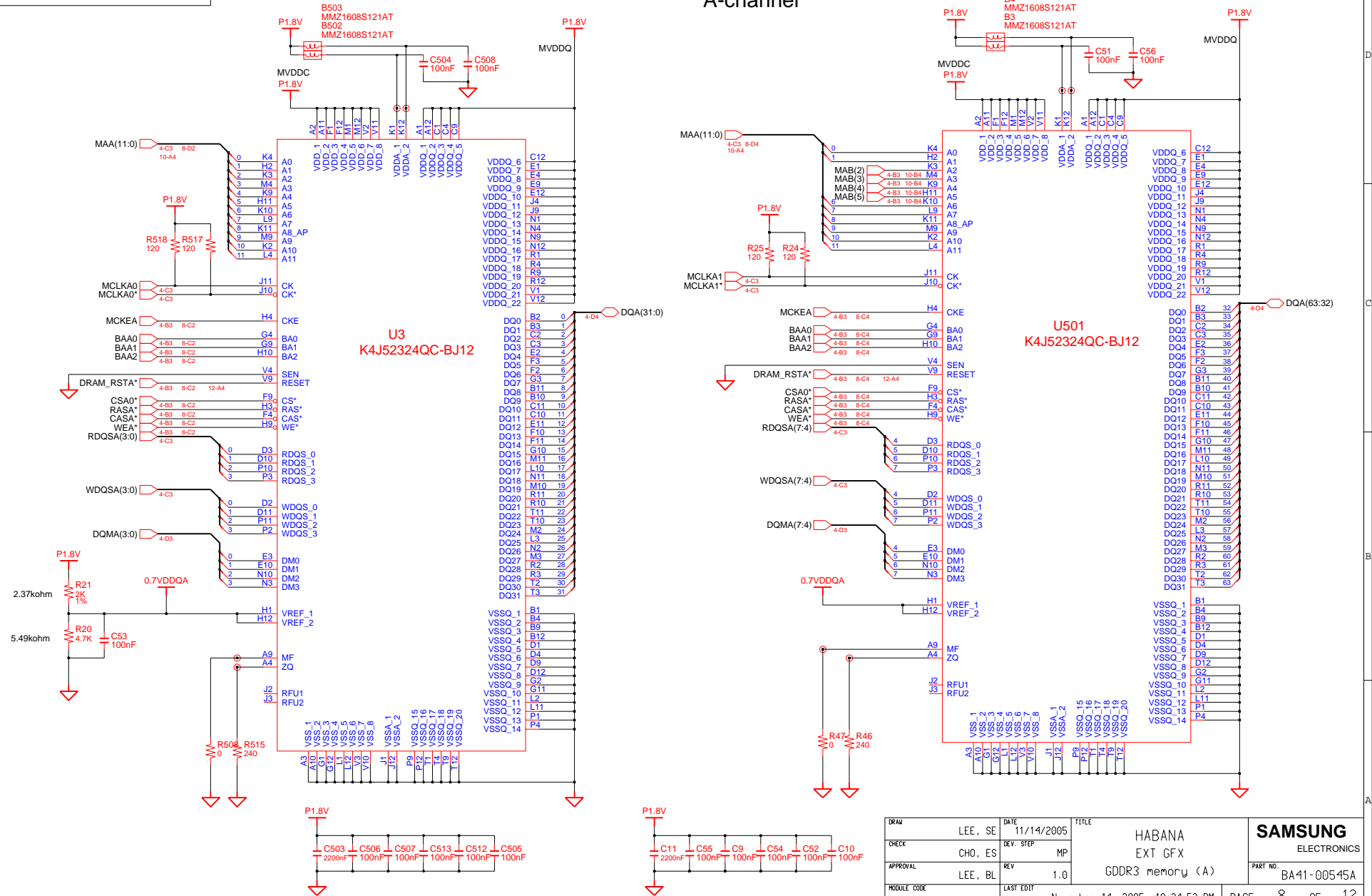
Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS(Default)
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : samsung GDDR3 256Mbit 0101 : infineon GDDR3 256Mbit 0011 : samsung GDDR3 512Mbit 0001 : infineon GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz (Default) 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC (Default) 10 : PAL 11 : CRT
PCI_DEVID(3:0) [11,3,5,4]	MIOB(11) MIOB(3) MIOB(5) MIOB(4)	72M : 0X01D8 72M-V : 0X01D7 73M : 0X0398
ROM_TYPE(1:0)	MIOB(10) MIOBVSYN	No ROM (NC)
USER STRAP	MIOAD(2:5)	EDID

DRW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP			
APPROVAL	LEE, BL	REV	1.0	Gfx strap option		PART NO. BA41-00545A
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	PAGE	7	OF 12

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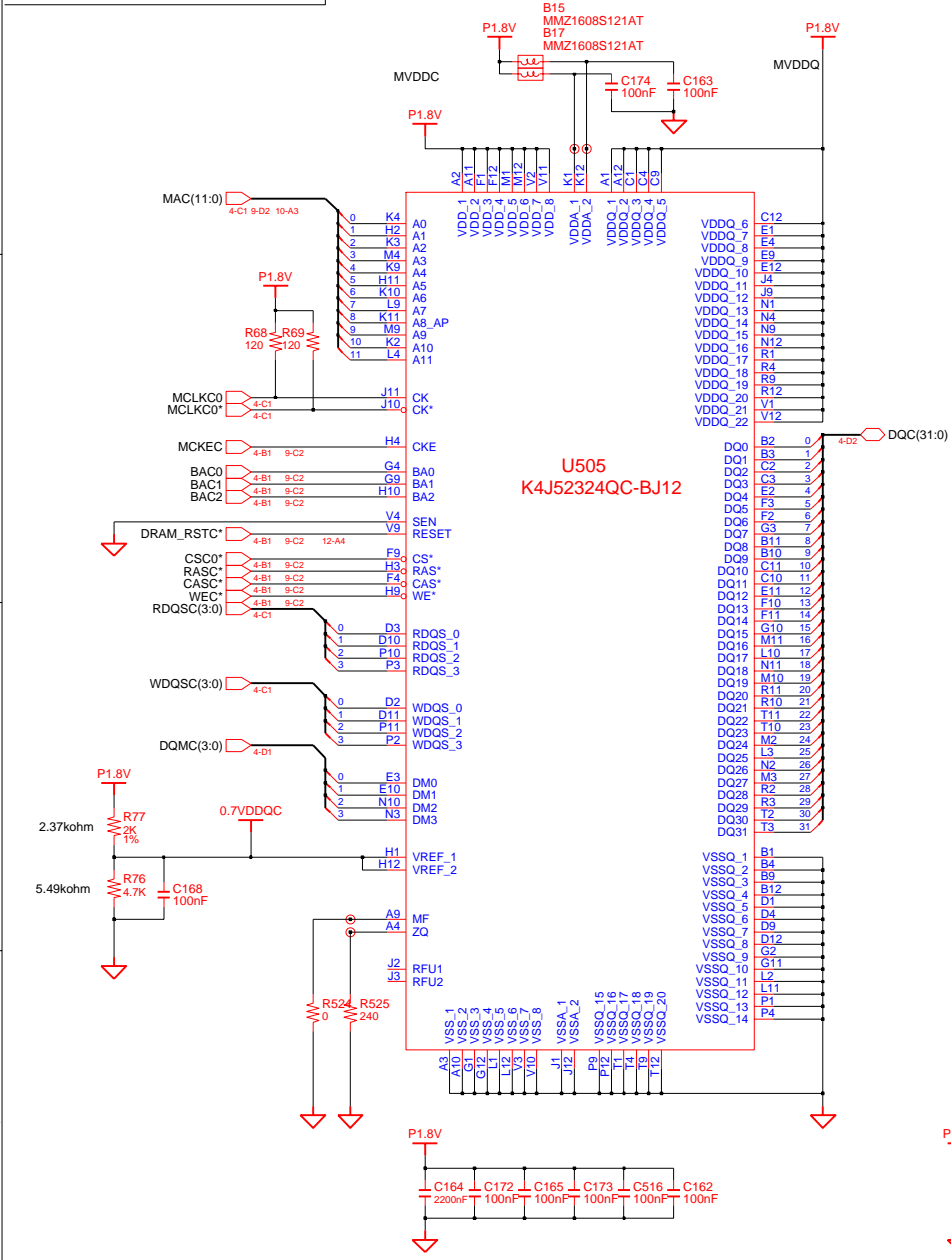
A-channel



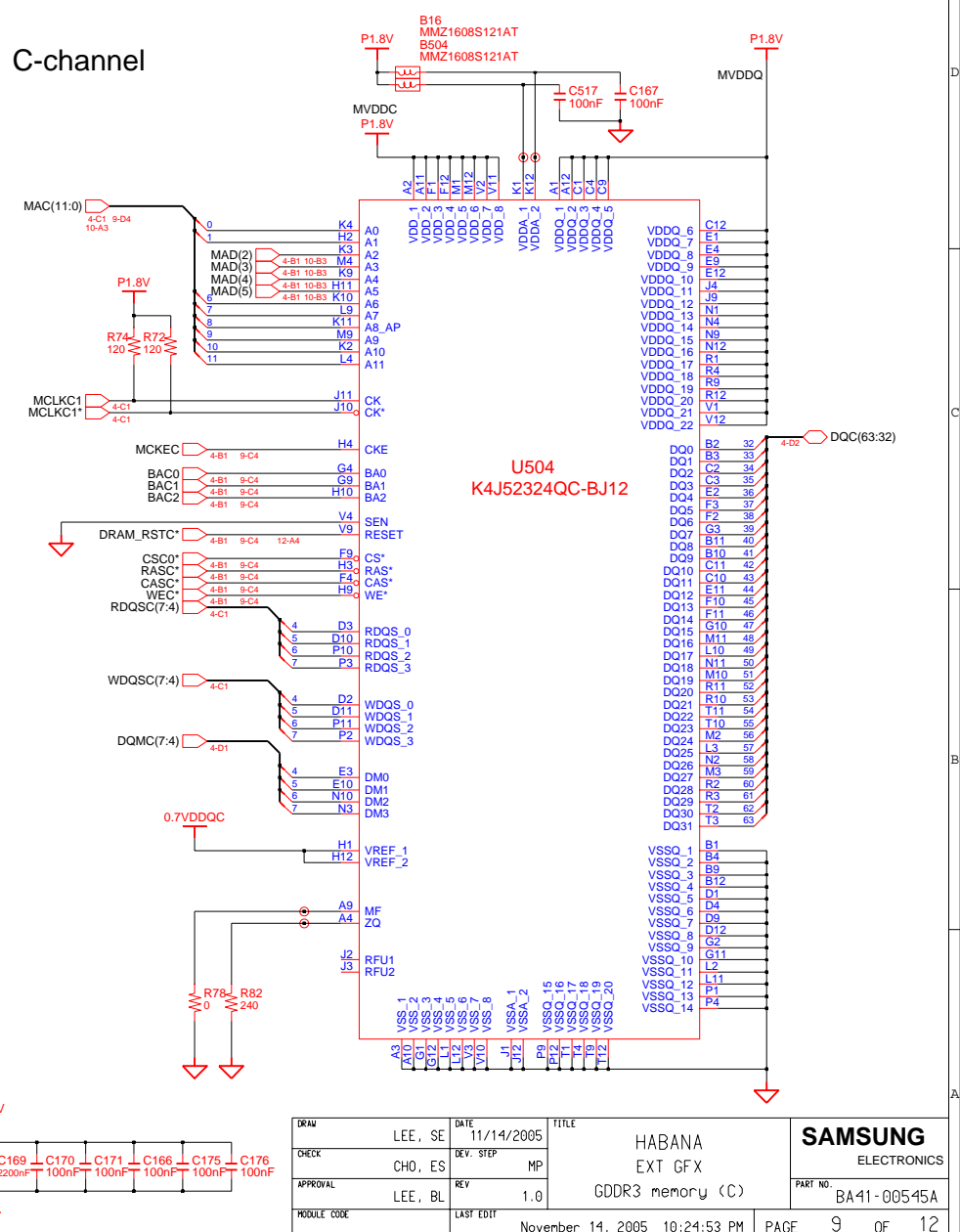
DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	LEE, SE	DEV. STEP	MP	
APPROVAL	LEE, BL	REV	1.0	PART NO. BA41-00545A
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	

This page is for "2channel-model".

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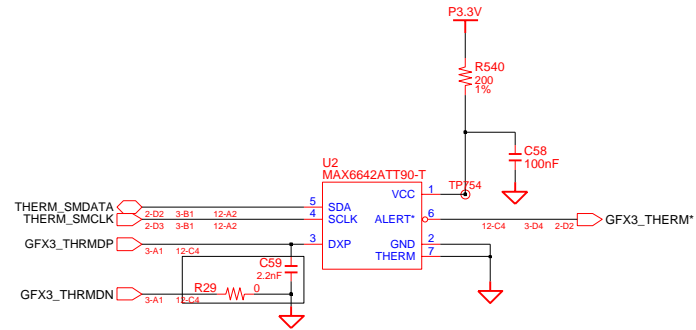
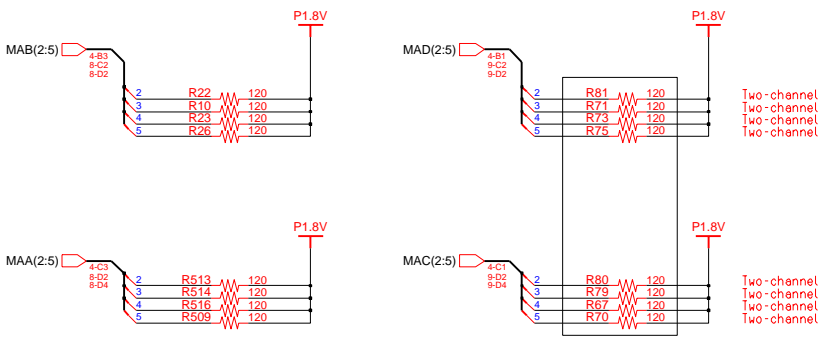
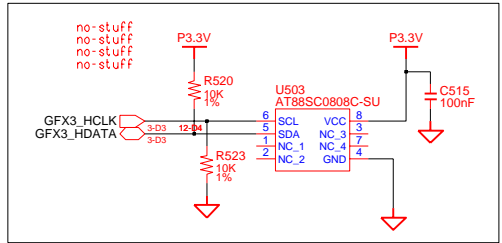
C-channel



DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	GDDR3 memory (C)		
APPROVAL	LEE, BL	REV	1.0	November 14, 2005 10:24:53 PM		PART NO. BA41-00545A
MODULE CODE	LAST EDIT		PAGE		9	OF 12

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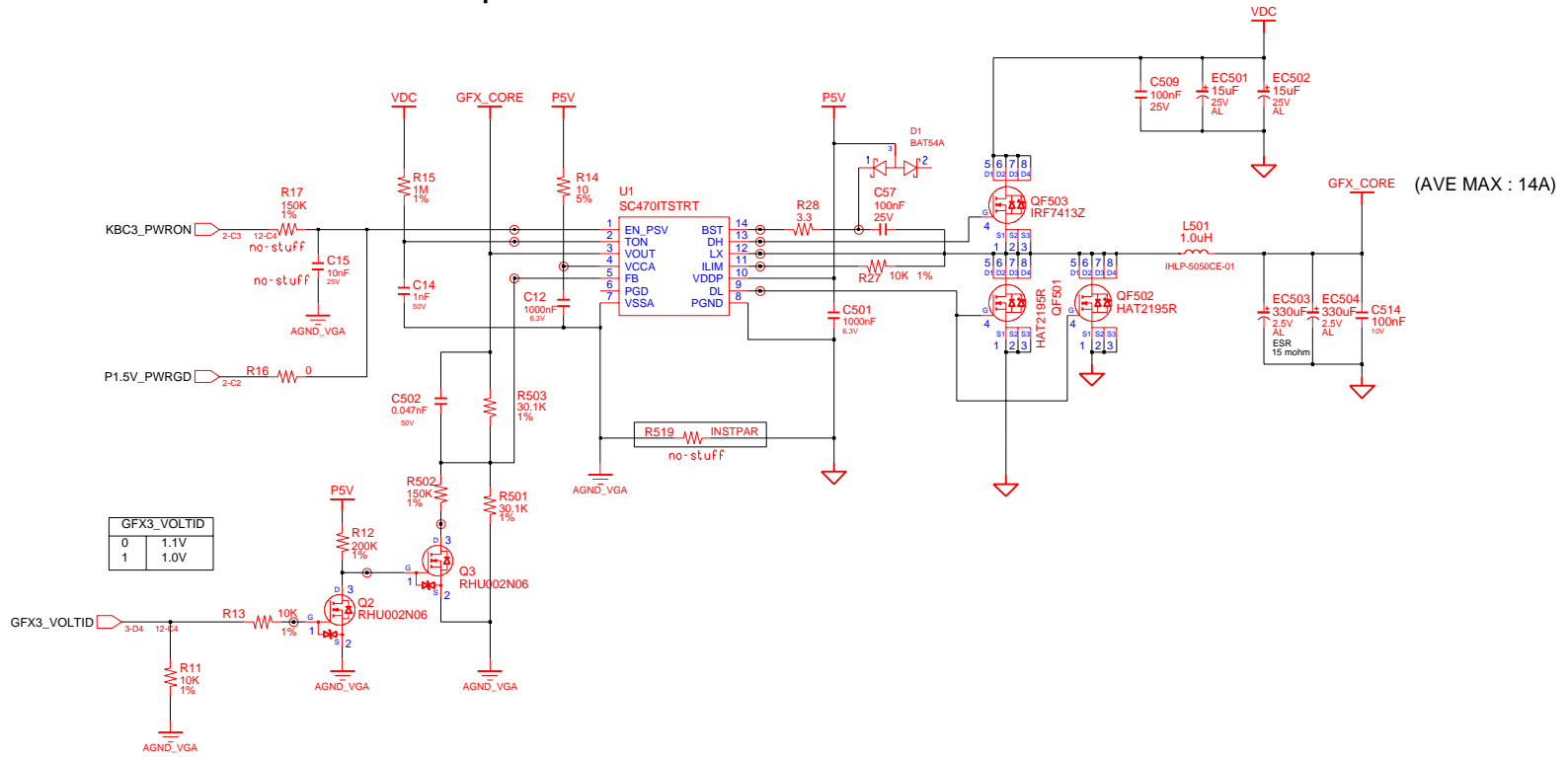
Place near to the MAX6642. SMBus address : 1001000x

DRW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS PART NO. BA41-00545A
CHECK	CHO, ES	DEV. STEP	MP			
APPROVAL	LEE, BL	REV	1.0	GDDR3 Term. Thermal sensor		
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	PAGE	10	OF 12

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Graphic Core Power



GFX3_VOLTID	
0	1.1V
1	1.0V

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	Gfx core Regulator		
APPROVAL	LEE, BL	REV	1.0			PART NO. BA41-00545A
MODULE CODE	LAST EDIT		November 14, 2005 10:24:53 PM		PAGE	11 OF 12

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○GFX3_27M
 ○GFX3_27M_SS
 ○GFX3_BLON
 ○GFX3_BLUE
 ○GFX3_BR11
 ○GFX3_C
 ○GFX3_COMP
 ○GFX3_DDCCLK
 ○GFX3_DDCDATA
 ○GFX3_DVICLK
 ○GFX3_DVIDATA

○GFX3_GREEN
 ○GFX3_HCLK
 ○GFX3_HDATA
 ○GFX3_HSYNC
 ○GFX3_HITPLG
 ○GFX3_CDVDDON
 ○GFX3_RED
 ○GFX3_THERM*
 ○GFX3_THRMDN
 ○GFX3_THRMOP

○GFX3_VOLTID
 ○GFX3_VSYNC
 ○GFX3_Y
 ○HDDTECT*
 ○KBC3_PWRON

○DRAM_RSTA*
 ○DRAM_RSTC*
 ○EDID_CLK
 ○EDID_DATA

○PSV
 ○PSV
 ○PSV
 ○PSV
 ○TMSD_PLLVDD
 ○TMSD_PLLVDD

○VDC
 ○VDC
 ○VDC
 ○VDC

○0.7VDDQA
 ○0.7VDDQA

○0.7VDDQC
 ○0.7VDDQC

○AGND_VGA
 ○AGND_VGA

○PEG3_MIOB(0)
 ○PEG3_MIOB(1)
 ○PEG3_MIOB(11)
 ○PEG3_MIOB(3)
 ○PEG3_MIOB(4)
 ○PEG3_MIOB(5)
 ○PEG3_MIOB(8)
 ○PEG3_MIOB(9)
 ○PL13_RST1*
 ○PWRON*

○CFX_CORE
 ○GFX_CORE
 ○GFX_CORE
 ○GFX_CORE
 ○GFX_CORE

○GROUND
 ○GROUND
 ○GROUND
 ○GROUND
 ○GROUND
 ○P1_2V
 ○P1_2V
 ○P1_2V
 ○P1_2V
 ○P1_2V
 ○P1_8V
 ○P1_8V
 ○P1_8V
 ○P1_8V
 ○P1_8V
 ○P2_5V
 ○P2_5V
 ○P2_5V
 ○P2_5V
 ○P2_5V
 ○P2_5V
 ○P2_5V
 ○P3_3V
 ○P3_3V
 ○P3_3V
 ○P3_3V
 ○P3_3V
 ○PSV

○THERM_SMCLK
 ○THERM_SMDATA

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP			
APPROVAL	LEE, BL	REV	1.0	GDDR3 Term. Thermal sensor		PART NO. BA41-00545A
MODULE CODE	LAST EDIT		November 14, 2005 10:24:53 PM		PAGE	12 OF 12