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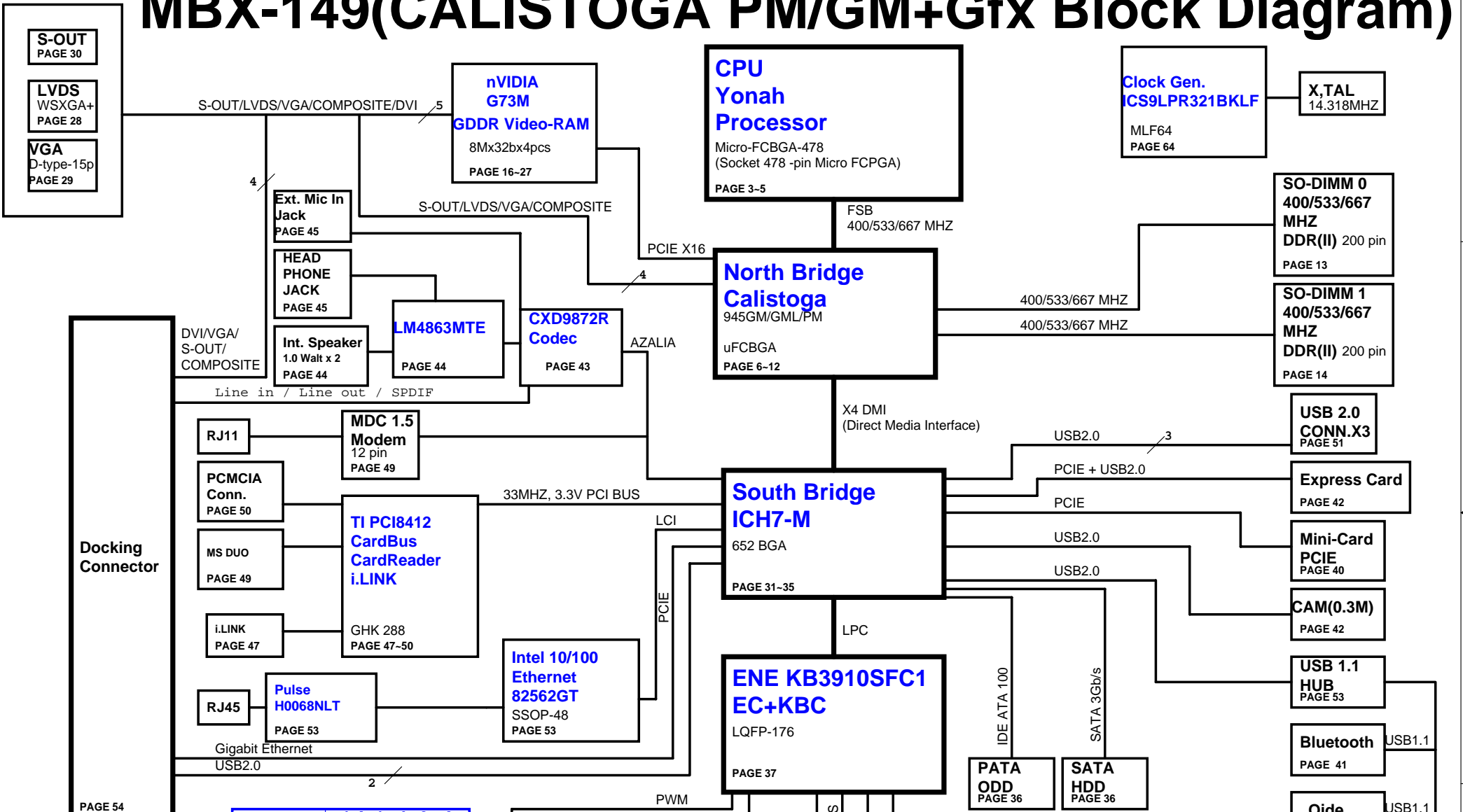
P. Leader	Check by	Design by

Project Code & Schematics Subject: MS12 Main Board

PCB P/N: 1P-0067100-8M11(FUBAI)
1P-0067200-8M11(NAN YA)
1P-0067500-8M11(HANSTAR)

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
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MBX-149(CALISTOGA PM/GM+Gfx Block Diagram)

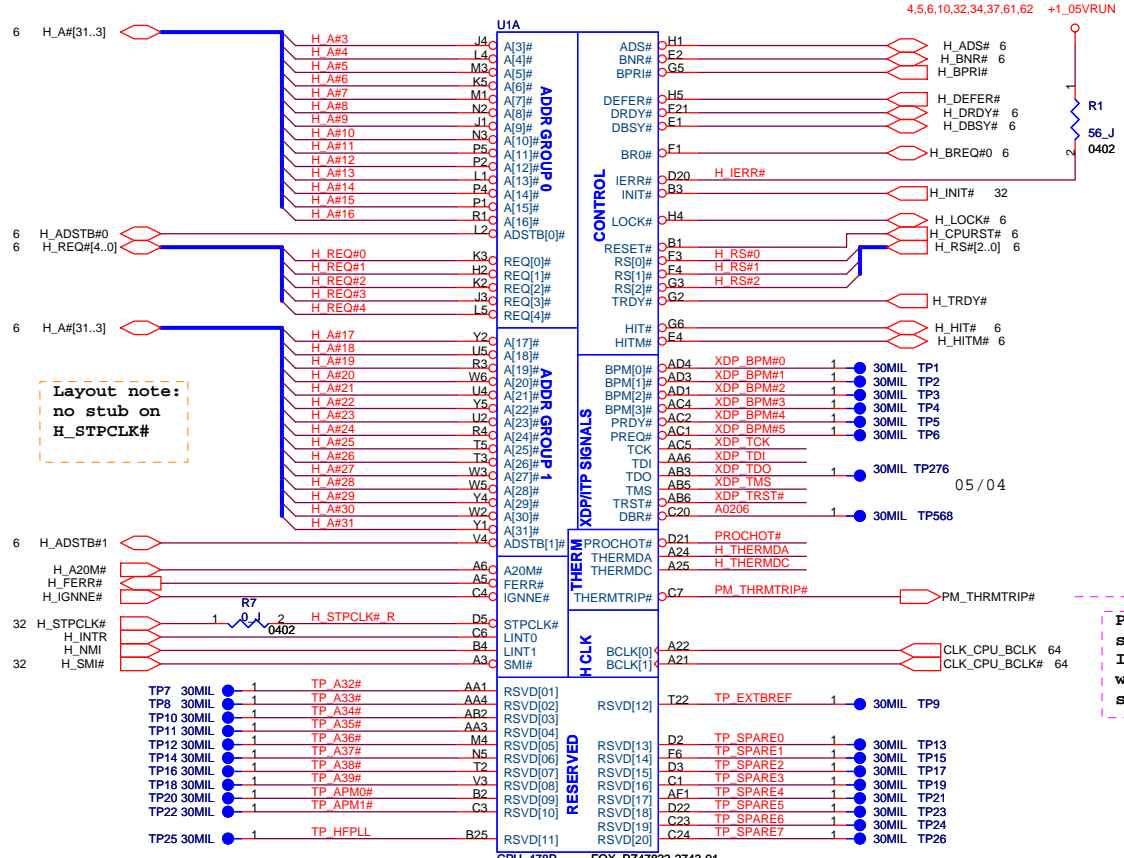


BOM configuration

	Symbol ahead of value for NC components
BOTH	NC_
945PM + NV72M/73M	CA_
945GM/GML	NV_
945PM+G72M or GM/GML	NV73_
945PM+G73M_A2 or GM/GML	NV72_

	Symbol ahead of value for NC components
G72M/G73M /GML	GM_
G72M/G73M /GM	GML_
Hynix 8Mx32	NVS_
G72M and Hynix 8Mx32	NV73S_
945PM+G73M_A2 or GM/GML	NV7273B01_
945PM+G73M_B01 or GM/GML	NV73A02_

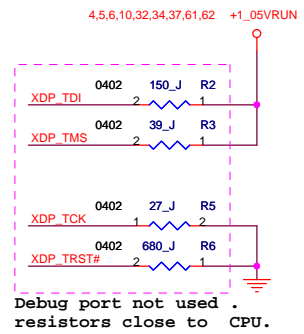
Modify for MP 07/11



Layout note:
no stub on
H_STPCLK#

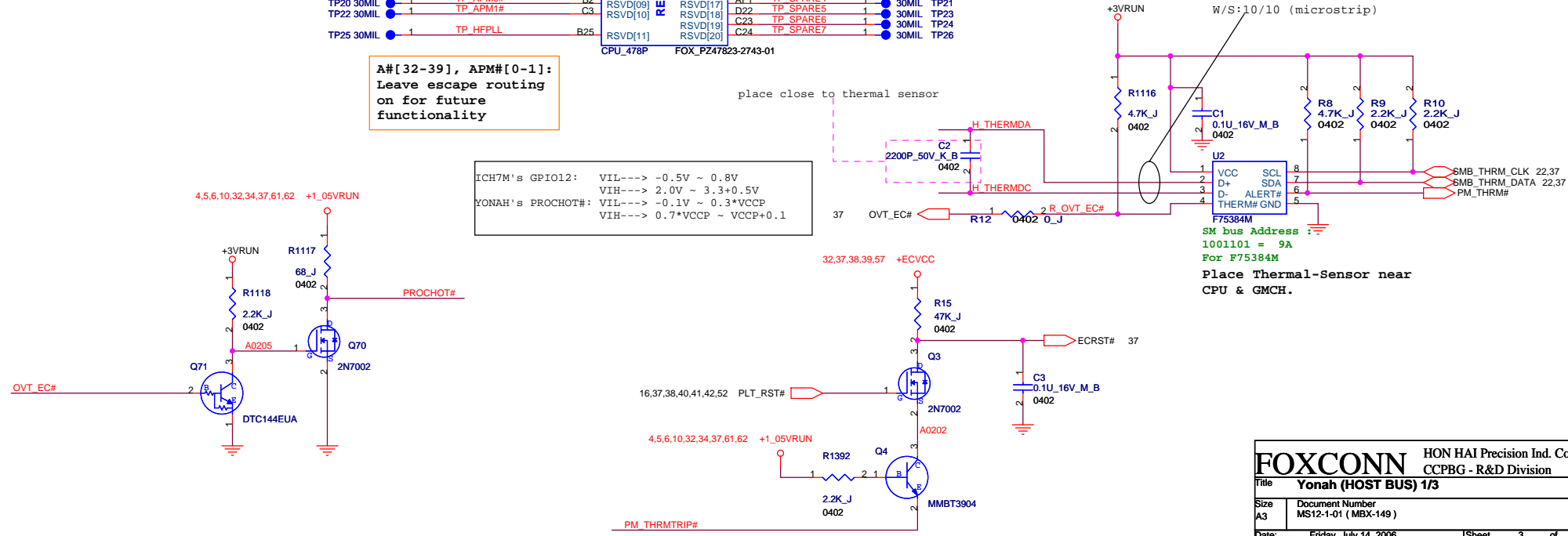
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

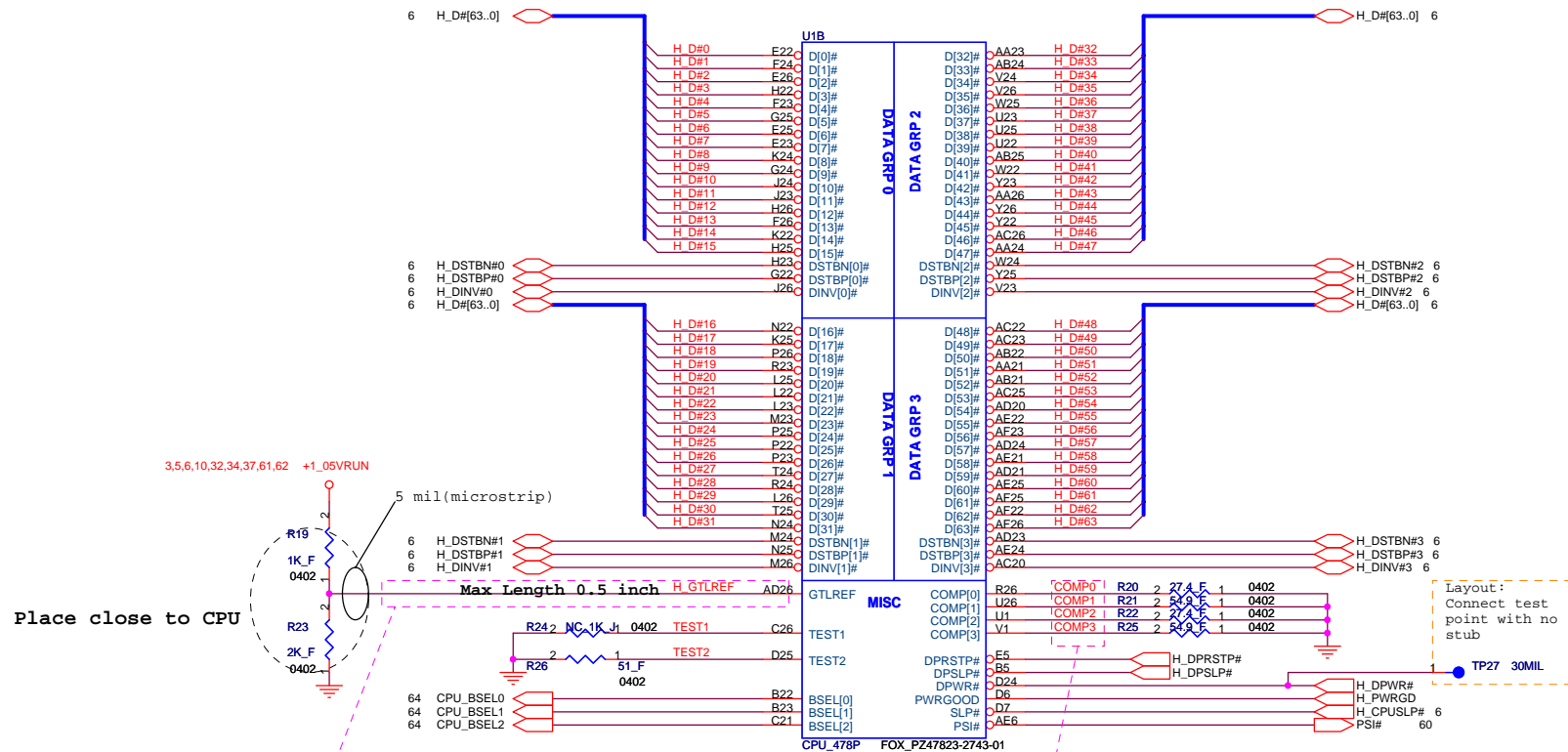
ICH7M's GPIO12: VIL----> -0.5V ~ 0.8V
VIH----> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V ~ 0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1



Debug port not used.
resistors close to CPU.

PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)

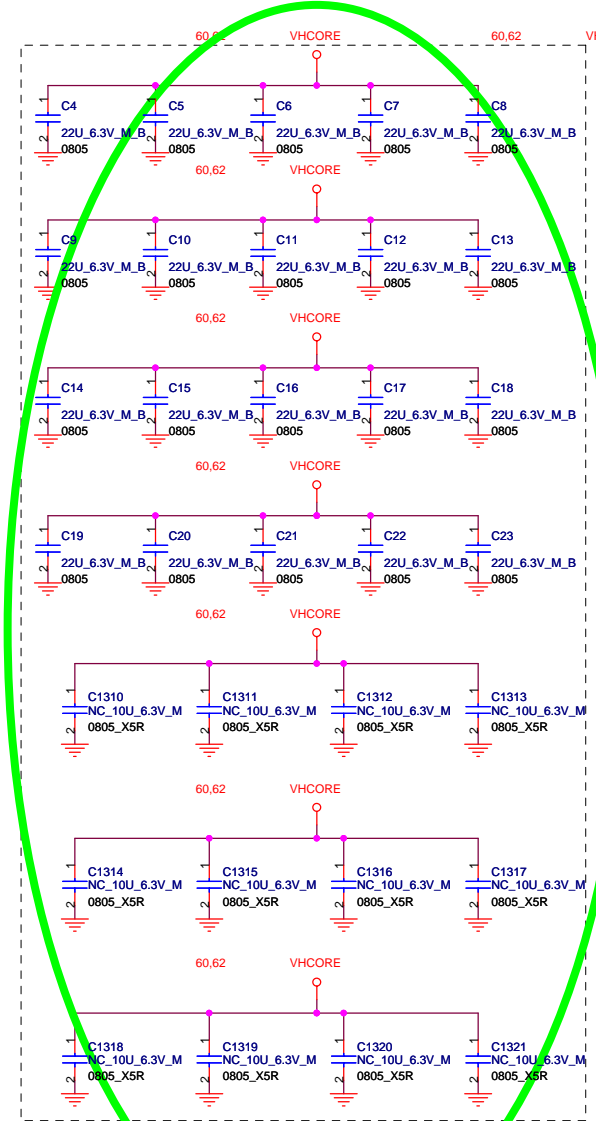




Layout Note:
Zo=55 ohm, 0.5" max for GTLREF.

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter then 0.5".

Layout:
Connect test point with no stub

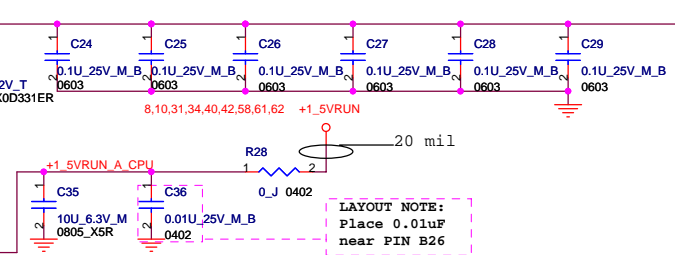


10uF *32 instead of 22uF*20 for 22uF_6.3V_0805 shortage

6/16
MS12 PVT Modify

U1C	VCC	U1D	VSS
A7	VCC[001]	A4	VSS[001]
A9	VCC[002]	A8	VSS[002]
A10	VCC[003]	A11	VSS[003]
A12	VCC[004]	A14	VSS[004]
A13	VCC[005]	A16	VSS[005]
A15	VCC[006]	A19	VSS[006]
A17	VCC[007]	A23	VSS[007]
A18	VCC[008]	A26	VSS[008]
A20	VCC[009]	B6	VSS[009]
B7	VCC[010]	B8	VSS[010]
B9	VCC[011]	B11	VSS[011]
B10	VCC[012]	B13	VSS[012]
B12	VCC[013]	B16	VSS[013]
B14	VCC[014]	B19	VSS[014]
B15	VCC[015]	B21	VSS[015]
B17	VCC[016]	B24	VSS[016]
B18	VCC[017]	C5	VSS[017]
B20	VCC[018]	C8	VSS[018]
C9	VCC[019]	C11	VSS[019]
C10	VCC[020]	C14	VSS[020]
C12	VCC[021]	C16	VSS[021]
C13	VCC[022]	C19	VSS[022]
C15	VCC[023]	C22	VSS[023]
C17	VCC[024]	C25	VSS[024]
C18	VCC[025]	C27	VSS[025]
D9	VCC[026]	D1	VSS[026]
D10	VCC[027]	D4	VSS[027]
D12	VCC[028]	D8	VSS[028]
D14	VCC[029]	D11	VSS[029]
D15	VCC[030]	D13	VSS[030]
D17	VCC[031]	D19	VSS[031]
D18	VCC[032]	D23	VSS[032]
E7	VCC[033]	D26	VSS[033]
E9	VCC[034]	E3	VSS[034]
E10	VCC[035]	E6	VSS[035]
E12	VCC[036]	E8	VSS[036]
E13	VCC[037]	E11	VSS[037]
E15	VCC[038]	E14	VSS[038]
E17	VCC[039]	E16	VSS[039]
E18	VCC[040]	E19	VSS[040]
E20	VCC[041]	E21	VSS[041]
F7	VCC[042]	E24	VSS[042]
F9	VCC[043]	F8	VSS[043]
F10	VCC[044]	F8	VSS[044]
F12	VCC[045]	F11	VSS[045]
F14	VCC[046]	F13	VSS[046]
F15	VCC[047]	F16	VSS[047]
F17	VCC[048]	F19	VSS[048]
F18	VCC[049]	F22	VSS[049]
F20	VCC[050]	F25	VSS[050]
AA7	VCC[051]	G4	VSS[051]
AA9	VCC[052]	G1	VSS[052]
AA10	VCC[053]	G1	VSS[053]
AA12	VCC[054]	G23	VSS[054]
AA13	VCC[055]	G26	VSS[055]
AA15	VCC[056]	H3	VSS[056]
AA17	VCC[057]	H6	VSS[057]
AA18	VCC[058]	H21	VSS[058]
AA20	VCC[059]	H24	VSS[059]
AB9	VCC[060]	H24	VSS[060]
AC10	VCC[061]	J2	VSS[061]
AB10	VCC[062]	J5	VSS[062]
AB12	VCC[063]	J25	VSS[063]
AB14	VCC[064]	K1	VSS[064]
AB15	VCC[065]	K4	VSS[065]
AB17	VCC[066]	K23	VSS[066]
AB18	VCC[067]	K26	VSS[067]
		L3	VSS[068]
		L6	VSS[069]
		L21	VSS[070]
		L24	VSS[071]
		M2	VSS[072]
		M5	VSS[073]
		M22	VSS[074]
		M25	VSS[075]
		N1	VSS[076]
		N4	VSS[077]
		N23	VSS[078]
		N26	VSS[079]
		P3	VSS[080]
			VSS[081]

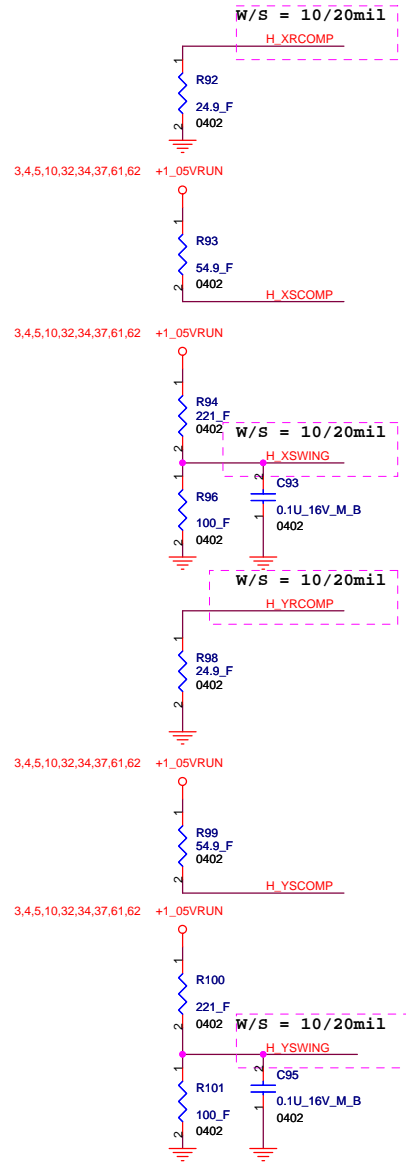
CPU_VCCA---->120mA
CPU_VCCP----->2.5A
CPU_VCC----->44A



LAYOUT NOTE:
Place 0.01uF near PIN B26

Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
width=18 mil
spacing=7 mil

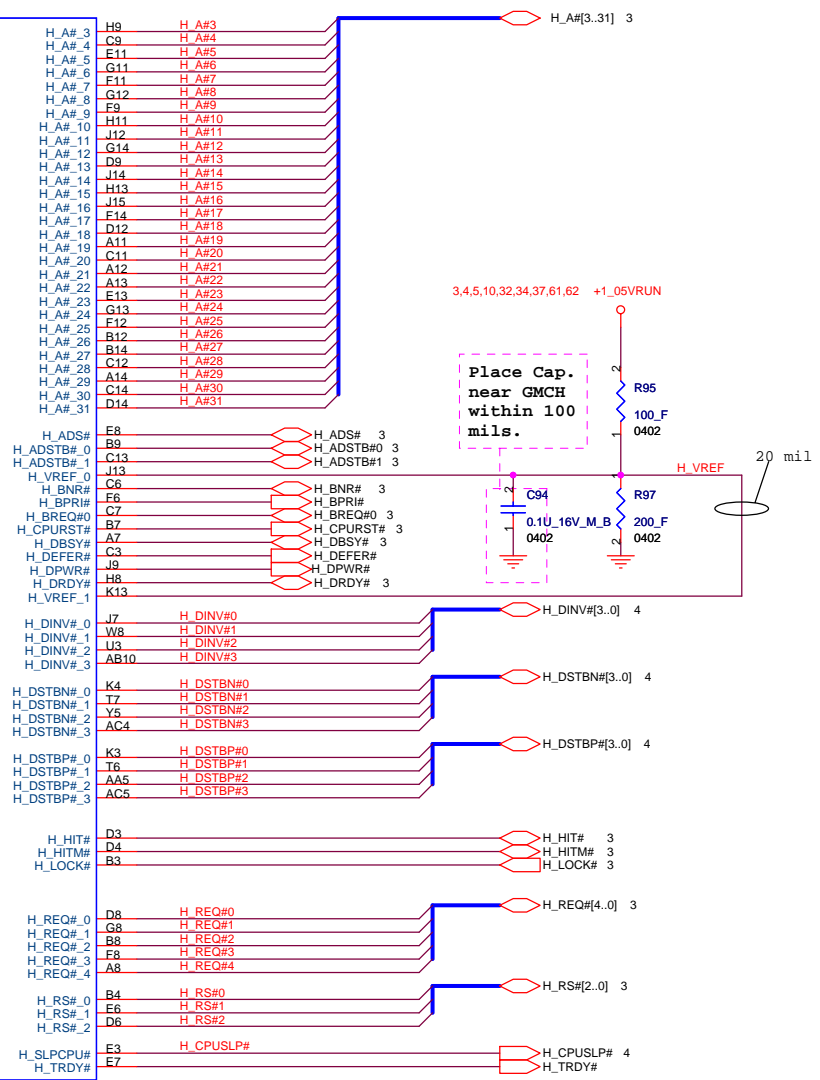
U1D	VSS	P6
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
A26	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	U2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C22	VSS[023]	W26
C25	VSS[024]	Y6
D1	VSS[025]	Y21
D4	VSS[026]	Y24
D8	VSS[027]	AA2
D11	VSS[028]	AA5
D13	VSS[029]	AA9
D19	VSS[030]	AA11
D23	VSS[031]	AA14
D26	VSS[032]	AA16
E3	VSS[033]	AA19
E6	VSS[034]	AA22
E8	VSS[035]	AA25
E11	VSS[036]	AB1
E14	VSS[037]	AB4
E16	VSS[038]	AB8
E19	VSS[039]	AB11
E21	VSS[040]	AB13
E24	VSS[041]	AB16
F8	VSS[042]	AB19
F11	VSS[043]	AB23
F13	VSS[044]	AB26
F16	VSS[045]	AC3
F19	VSS[046]	AC6
F22	VSS[047]	AC8
F25	VSS[048]	AC11
G4	VSS[049]	AC14
G1	VSS[050]	AC16
G23	VSS[051]	AC19
G26	VSS[052]	AC21
H3	VSS[053]	AC24
H6	VSS[054]	AD2
H21	VSS[055]	AD5
H24	VSS[056]	AD8
J2	VSS[057]	AD11
J5	VSS[058]	AD13
J25	VSS[059]	AD16
K1	VSS[060]	AD19
K4	VSS[061]	AD22
K23	VSS[062]	AD25
K26	VSS[063]	AE1
L3	VSS[064]	AE4
L6	VSS[065]	AE8
L21	VSS[066]	AE11
L24	VSS[067]	AE14
M2	VSS[068]	AE19
M5	VSS[069]	AE23
M22	VSS[070]	AE26
M25	VSS[071]	AE3
N1	VSS[072]	AE6
N4	VSS[073]	AE8
N23	VSS[074]	AE11
N26	VSS[075]	AE14
P3	VSS[076]	AE19
	VSS[077]	AE23
	VSS[078]	AE26
	VSS[079]	AF1
	VSS[080]	AF3
	VSS[081]	AF6
		AF8
		AF11
		AF13
		AF16
		AF19
		AF21
		AF24

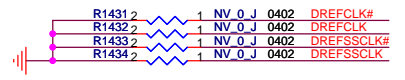
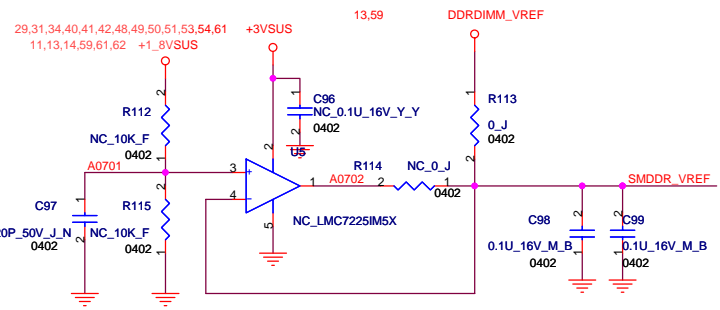
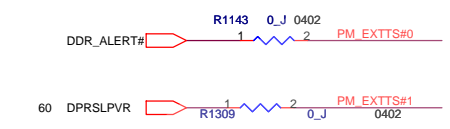
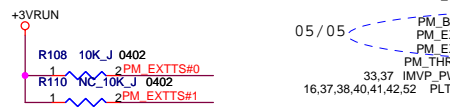
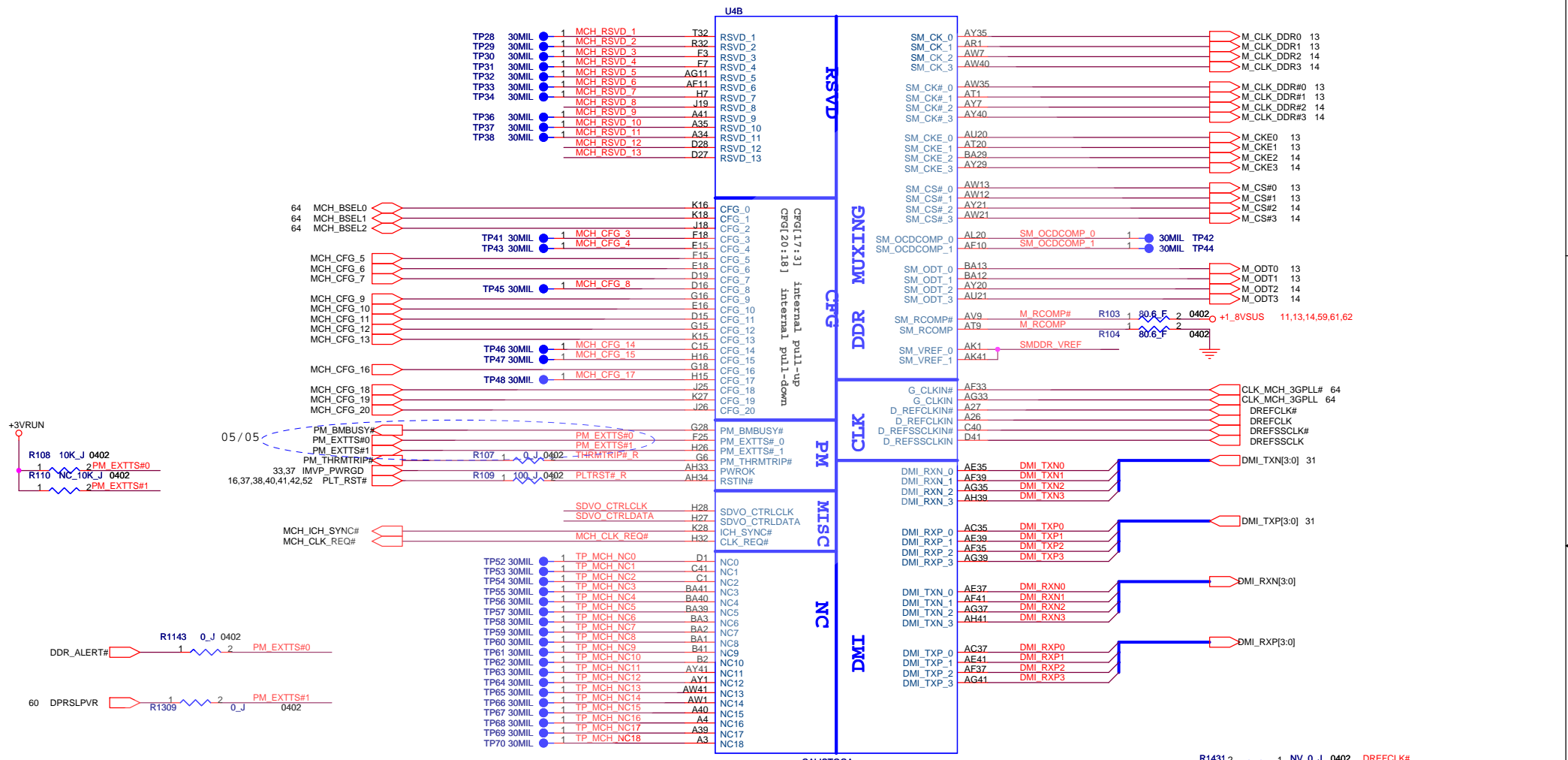


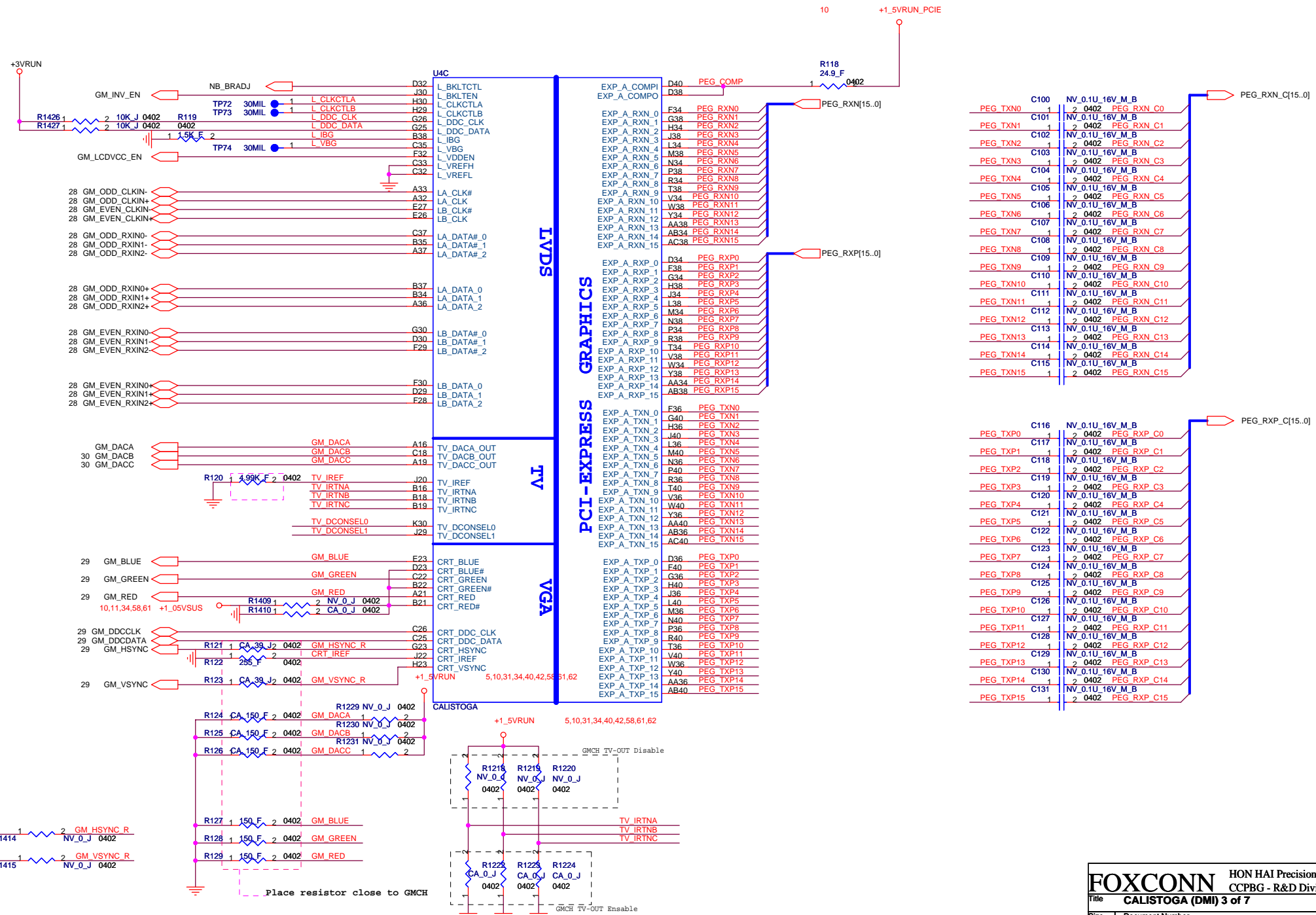
4 H_D#[63..0] H_D#[63..0]

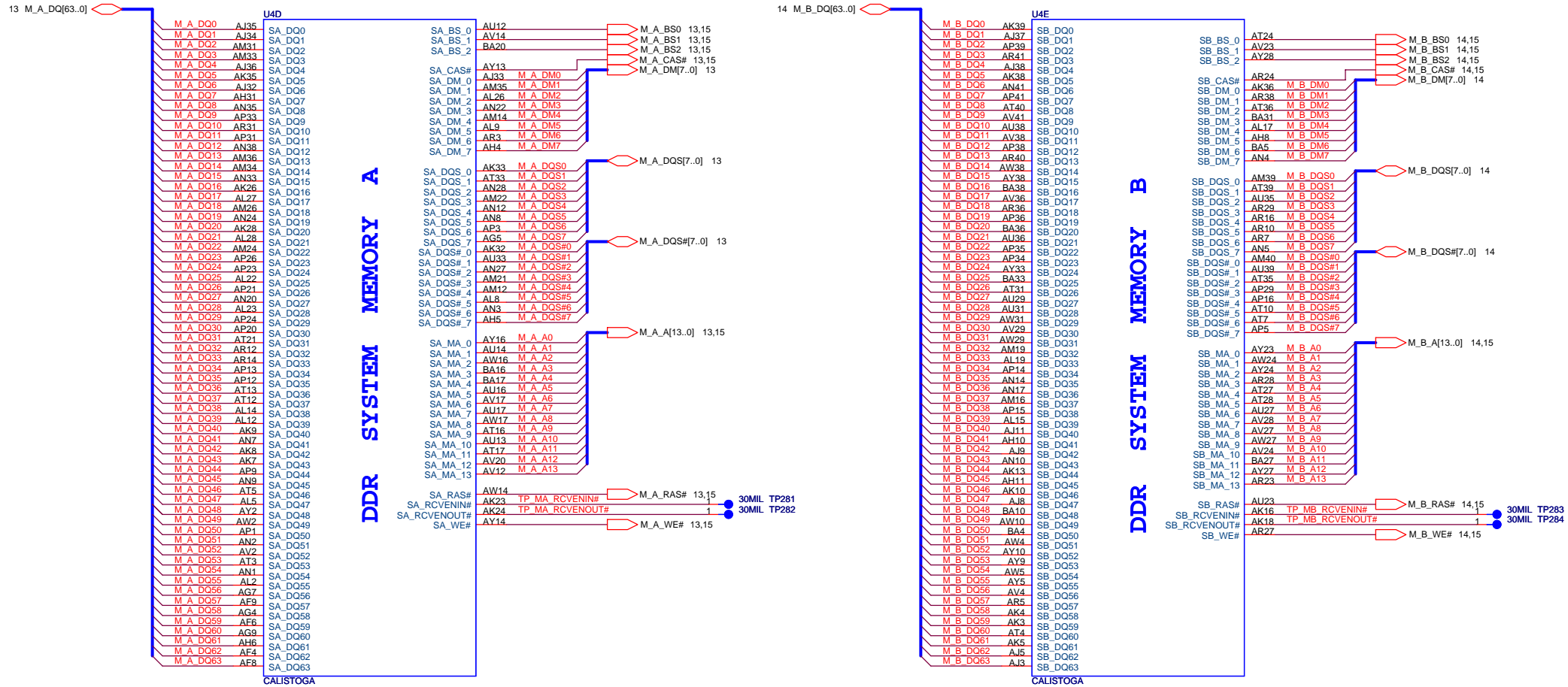
U4A	
H_D#0	F1
H_D#1	J1
H_D#2	H1
H_D#3	J6
H_D#4	H3
H_D#5	K2
H_D#6	G1
H_D#7	G2
H_D#8	K9
H_D#9	K1
H_D#10	K7
H_D#11	J8
H_D#12	H4
H_D#14	K13
H_D#15	G4
H_D#16	T10
H_D#17	W11
H_D#18	T3
H_D#19	U7
H_D#20	U9
H_D#21	U11
H_D#22	T11
H_D#23	W9
H_D#24	T1
H_D#25	T8
H_D#26	T4
H_D#27	W7
H_D#28	U5
H_D#29	T9
H_D#30	W6
H_D#31	T5
H_D#32	AB7
H_D#33	AA9
H_D#34	W4
H_D#35	W3
H_D#36	Y3
H_D#37	Y7
H_D#38	W5
H_D#39	Y10
H_D#40	AB8
H_D#41	W2
H_D#42	AA4
H_D#43	AA7
H_D#44	AA2
H_D#45	AA6
H_D#46	AA10
H_D#47	Y8
H_D#48	AA1
H_D#49	AB4
H_D#50	AC9
H_D#51	AB11
H_D#52	AC11
H_D#53	AB3
H_D#54	AC2
H_D#55	AD1
H_D#56	AD9
H_D#57	AC1
H_D#58	AD7
H_D#59	AC6
H_D#60	AB5
H_D#61	AD10
H_D#62	AD4
H_D#63	AC8
H_XRCOMP	E1
H_XSCOMP	E2
H_XSWING	E4
H_YRCOMP	Y1
H_YSCOMP	U1
H_YSWING	W1
H_CLKIN	AG2
H_CLKIN#	AG1

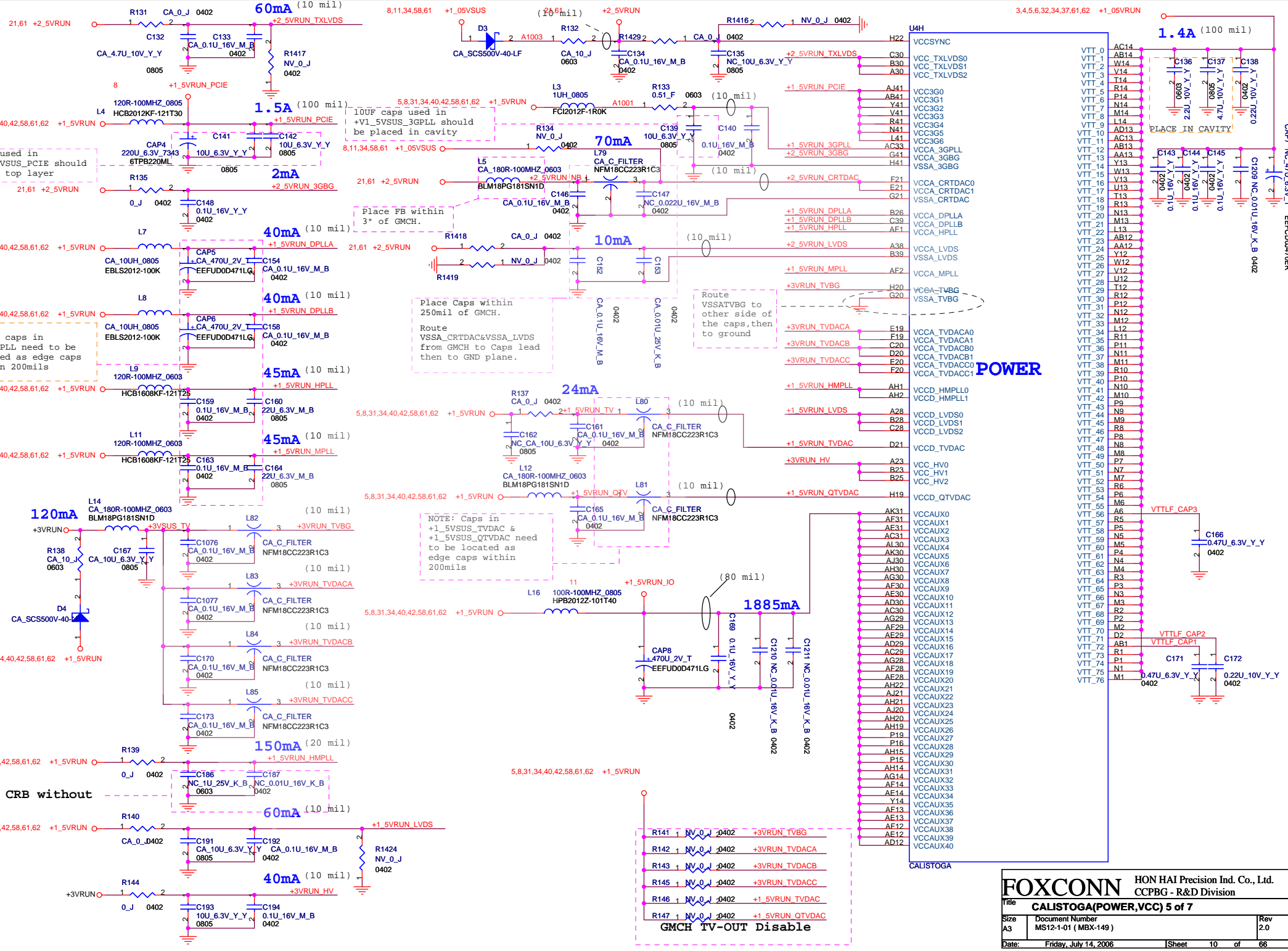
HOST











POWER

GMCH TV-OUT Disable

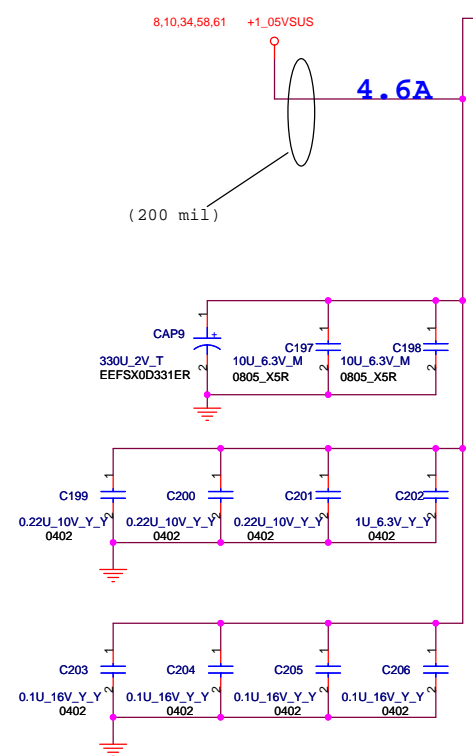
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Title: **CALISTOGA(POWER,VCC) 5 of 7**

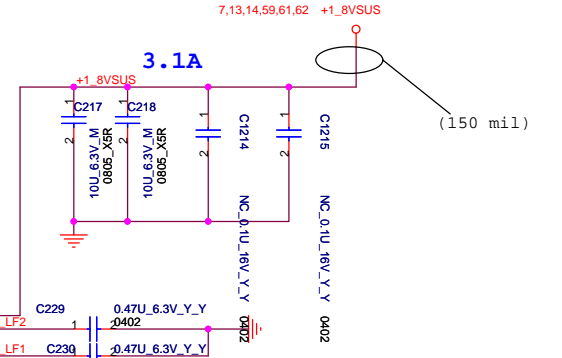
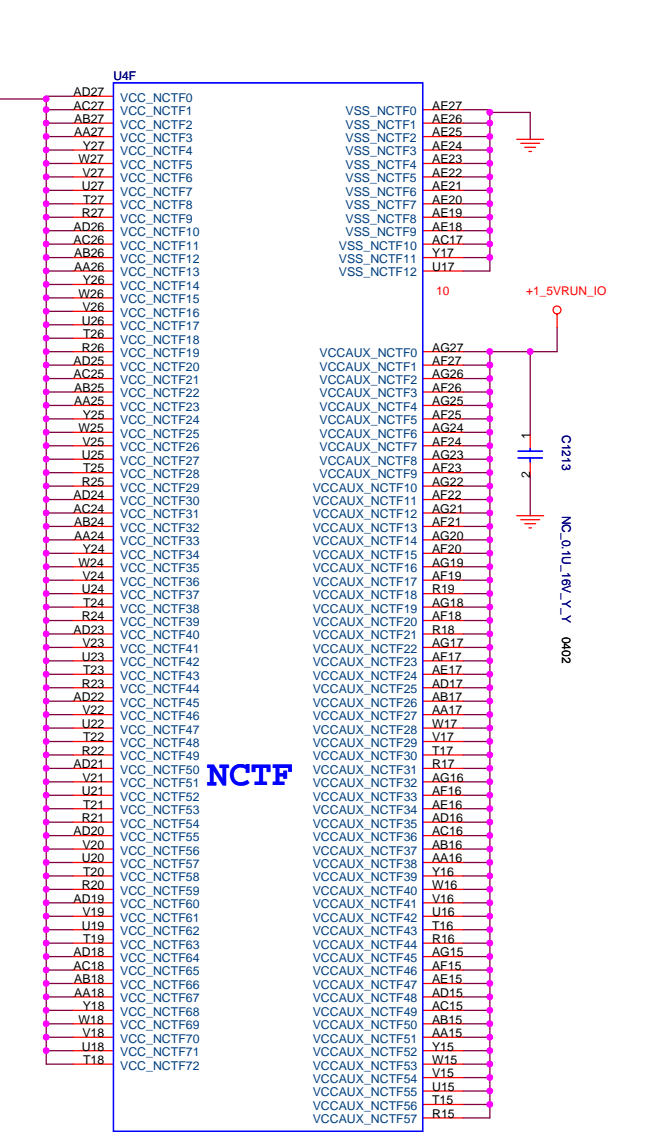
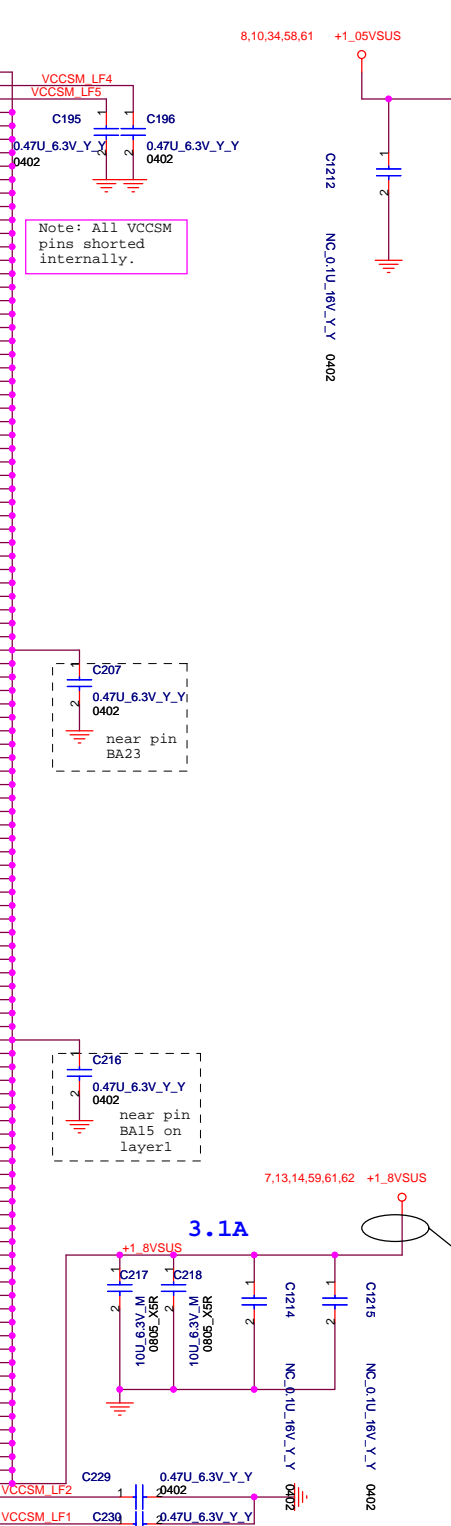
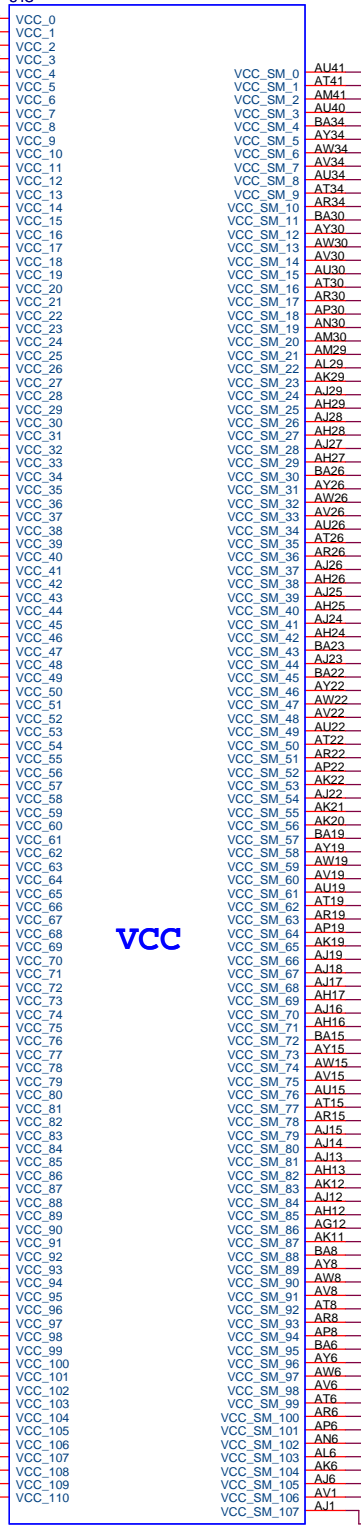
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- AA33 VCC_0
- W33 VCC_1
- P33 VCC_2
- L33 VCC_3
- J33 VCC_4
- AA32 VCC_5
- Y32 VCC_6
- W32 VCC_7
- L32 VCC_8
- J32 VCC_9
- AA31 VCC_10
- W31 VCC_11
- P31 VCC_12
- N31 VCC_13
- M31 VCC_14
- AA30 VCC_15
- Y30 VCC_16
- W30 VCC_17
- V30 VCC_18
- T30 VCC_19
- R30 VCC_20
- P31 VCC_21
- N31 VCC_22
- M31 VCC_23
- AA30 VCC_24
- Y30 VCC_25
- W30 VCC_26
- V30 VCC_27
- T30 VCC_28
- R30 VCC_29
- P30 VCC_30
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- AA29 VCC_34
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- V29 VCC_37
- T29 VCC_38
- R29 VCC_39
- P29 VCC_40
- M29 VCC_41
- L29 VCC_42
- AB28 VCC_43
- AA28 VCC_44
- Y28 VCC_45
- V28 VCC_46
- U28 VCC_47
- T28 VCC_48
- R28 VCC_49
- P28 VCC_50
- N28 VCC_51
- M28 VCC_52
- L28 VCC_53
- P27 VCC_54
- N27 VCC_55
- M27 VCC_56
- L27 VCC_57
- P26 VCC_58
- N26 VCC_59
- L26 VCC_60
- N25 VCC_61
- M25 VCC_62
- L25 VCC_63
- P24 VCC_64
- N24 VCC_65
- M24 VCC_66
- AB23 VCC_67
- AA23 VCC_68
- Y23 VCC_69
- P23 VCC_70
- N23 VCC_71
- M23 VCC_72
- L23 VCC_73
- AC22 VCC_74
- Y22 VCC_75
- W22 VCC_76
- P22 VCC_77
- N22 VCC_78
- M22 VCC_79
- L22 VCC_80
- AC21 VCC_81
- AA21 VCC_82
- W21 VCC_83
- N21 VCC_84
- M21 VCC_85
- L21 VCC_86
- AC20 VCC_87
- AB20 VCC_88
- Y20 VCC_89
- W20 VCC_90
- P20 VCC_91
- N20 VCC_92
- M20 VCC_93
- L20 VCC_94
- AB19 VCC_95
- AA19 VCC_96
- Y19 VCC_97
- N19 VCC_98
- M19 VCC_99
- L19 VCC_100
- N18 VCC_101
- M18 VCC_102
- L18 VCC_103
- P17 VCC_104
- N17 VCC_105
- M17 VCC_106
- N16 VCC_107
- M16 VCC_108
- N15 VCC_109
- L16 VCC_110



MCH_CFG_5 ← 1 ● 30MIL TP554

MCH_CFG_5
Low = DMIX2
High = DMIX4

MCH_CFG_18
Low = 1.05V(default)
High = 1.5V
(VCC_CORE Select)

MCH_CFG_18 ← 1 ● 30MIL TP555

MCH_CFG_6 ← 1 ● 30MIL TP556

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

MCH_CFG_19
Low = Normal(default)
High = LANES REVERSED
(DMI LANE REVERSAL)

MCH_CFG_19 ← 1 ● 30MIL TP558

MCH_CFG_7 ← 1 ● 30MIL TP557

MCH_CFG_7 (CPU Strap)
Low = RSVD
High = Mobile Yonah processor

MCH_CFG_20
Low = Only SDVO or PCIE x1 is operational (defaults)
High = SDVO and PCIE x1 are operating simultaneously via the PEG port
(PCIe Backward Interoperability mode)

MCH_CFG_9 ← 1 ● 30MIL TP559

MCH_CFG_9 (PCIe Graphics Lane)
Low = Reverse Lane operation
High = Normal operation

For layout convenience

MCH_CFG_10 ← 1 ● 30MIL TP560

MCH_CFG_10 (HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

MCH_CFG_20 ← 1 ● 30MIL TP561

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

MCH_CFG_11 ← 1 ● R162 NC 2.2K_J 0402

MCH_CFG_11 (PSB 4x CLK ENABLE)
Low = Calistoga
High = Reserved

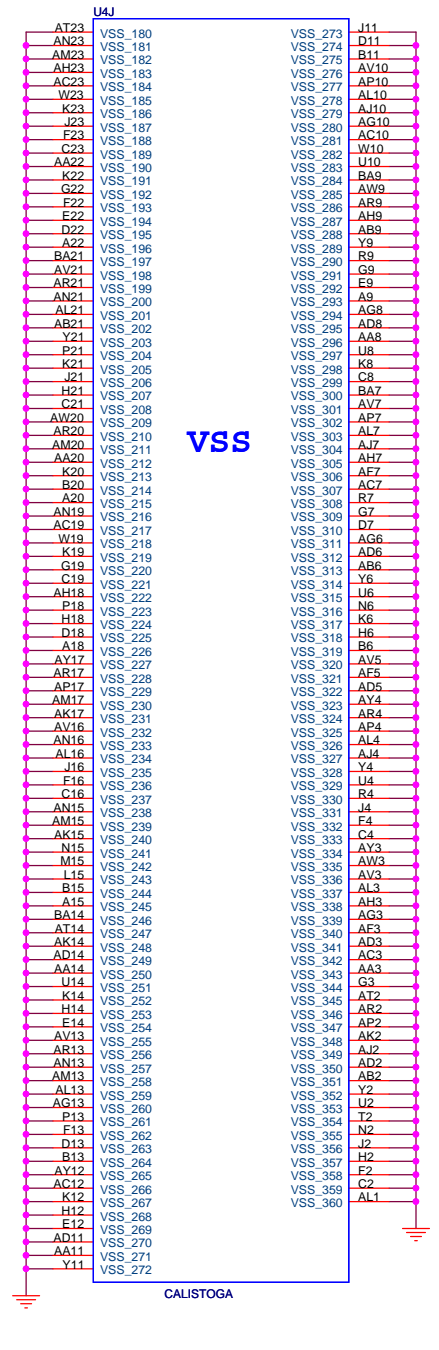
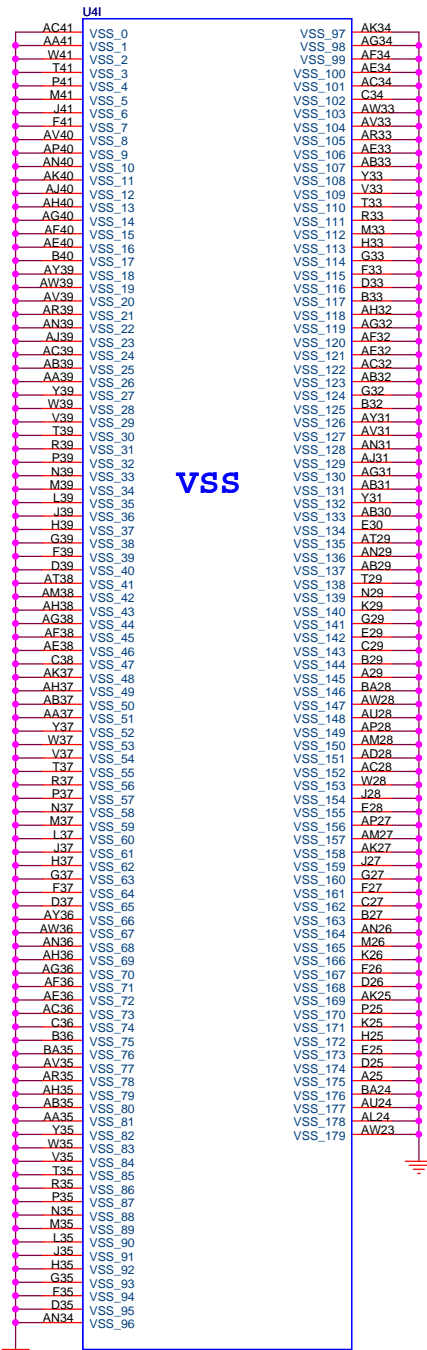
MCH_CFG_12 ← 1 ● 30MIL TP562

MCH_CFG_13 ← 1 ● 30MIL TP563

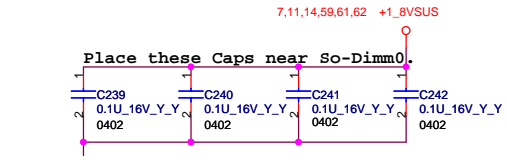
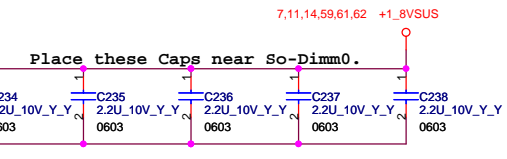
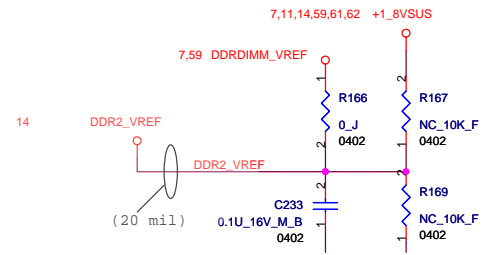
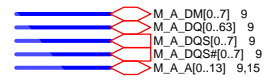
MCH_CFG_[13:12] (XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

MCH_CFG_16 ← 1 ●

MCH_CFG_16 (FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable



1.8V per DIMM=3.08A



0.1 uF and 2.2 uF placed close to VREF pins

Place these Caps near So-Dimm0.

Place these Caps near So-Dimm0.

PC4800 DDR2 SDRAM SO-DIMM (200P)

DIMM_0

SMBus Address: A0(W)/A1(R)

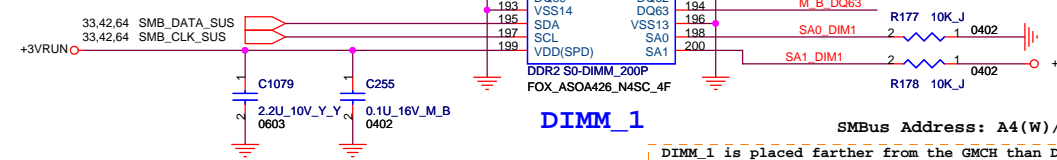
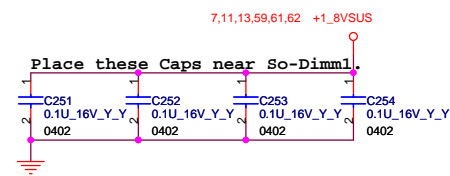
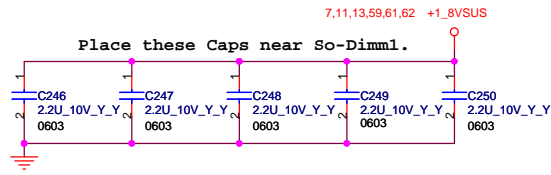
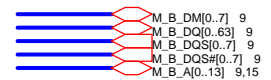
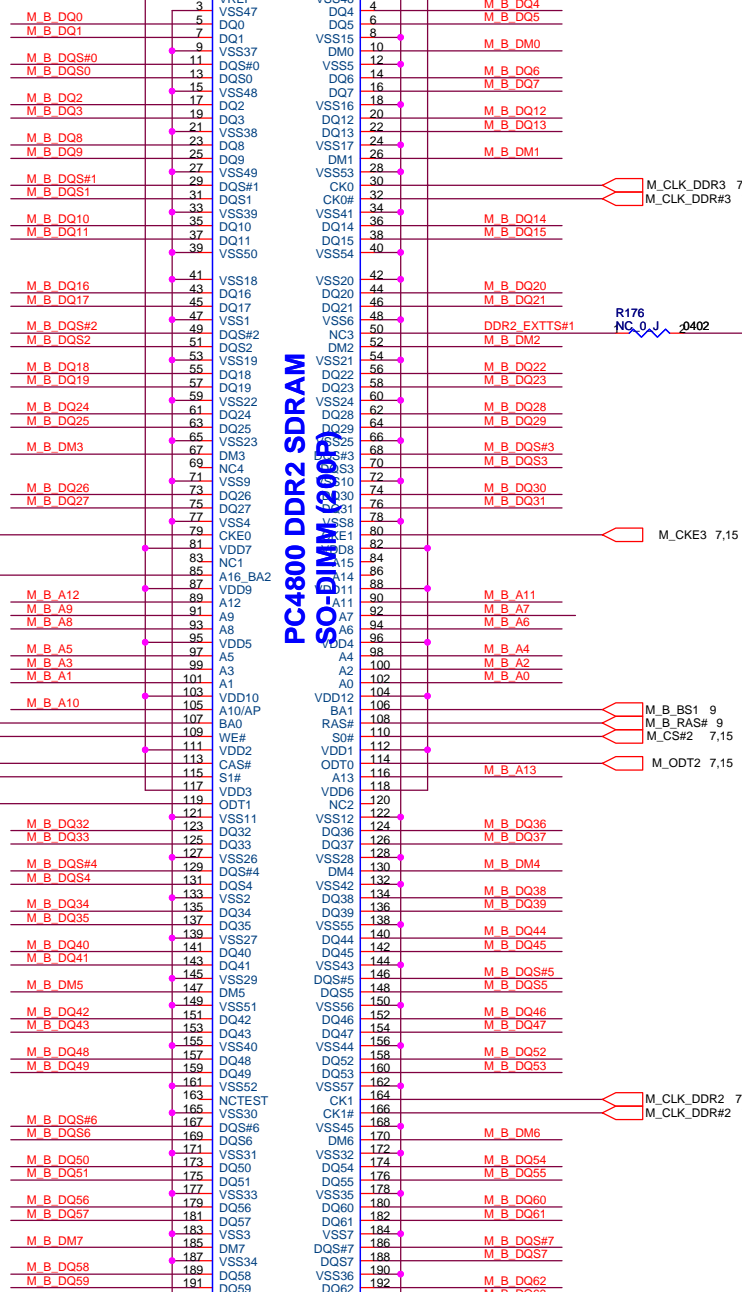
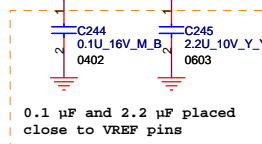
Place DIMM_0 near GMCH

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CCPBG - R&D Division

File: **DDR(II)SO-DIMM_0**

Size A3	Document Number MS12-1-01 (MBX-149)	Rev 2.0
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1.8V per DIMM=3.08A

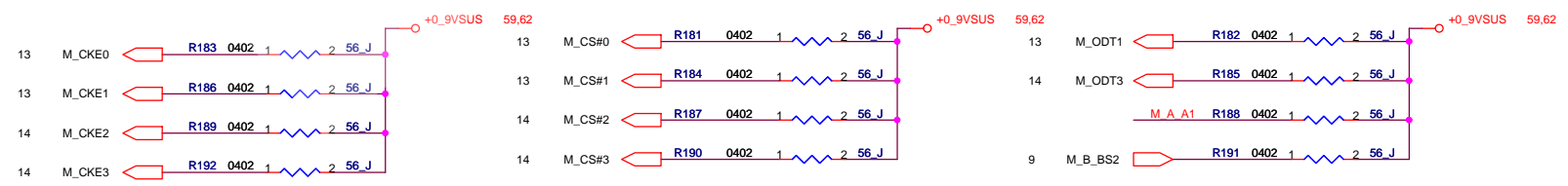
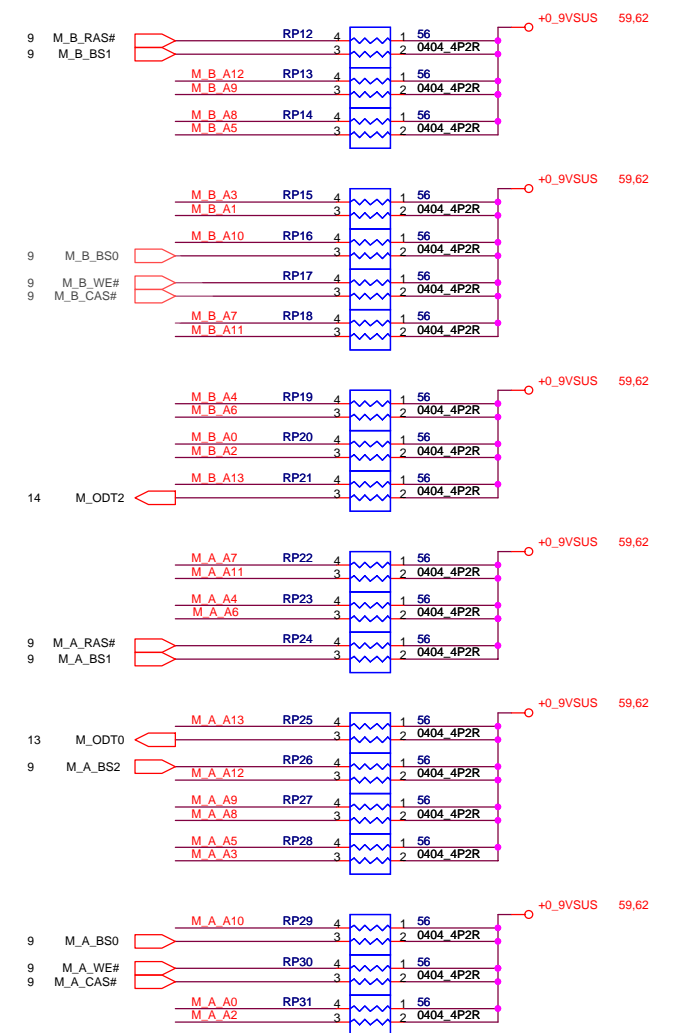
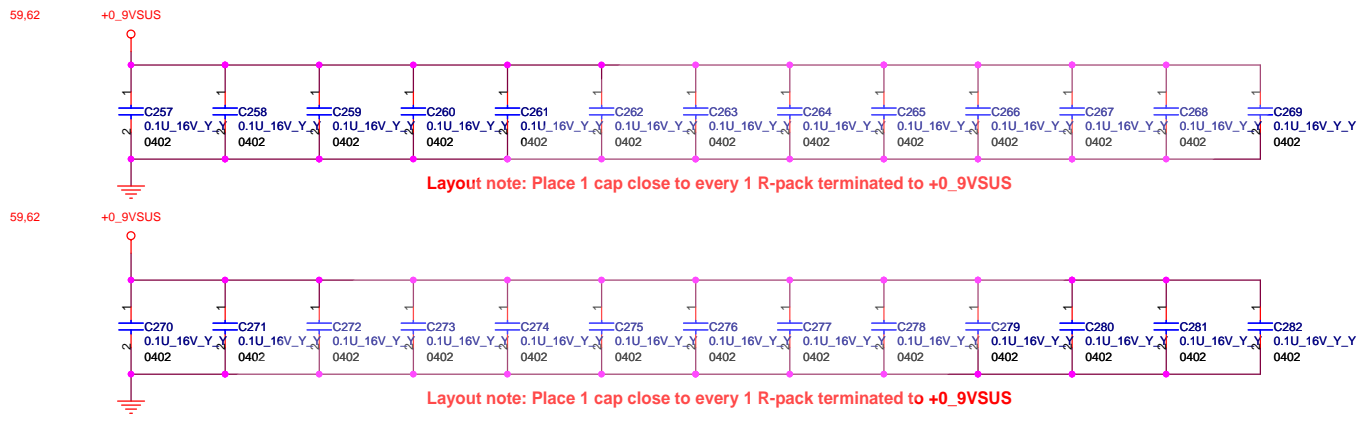


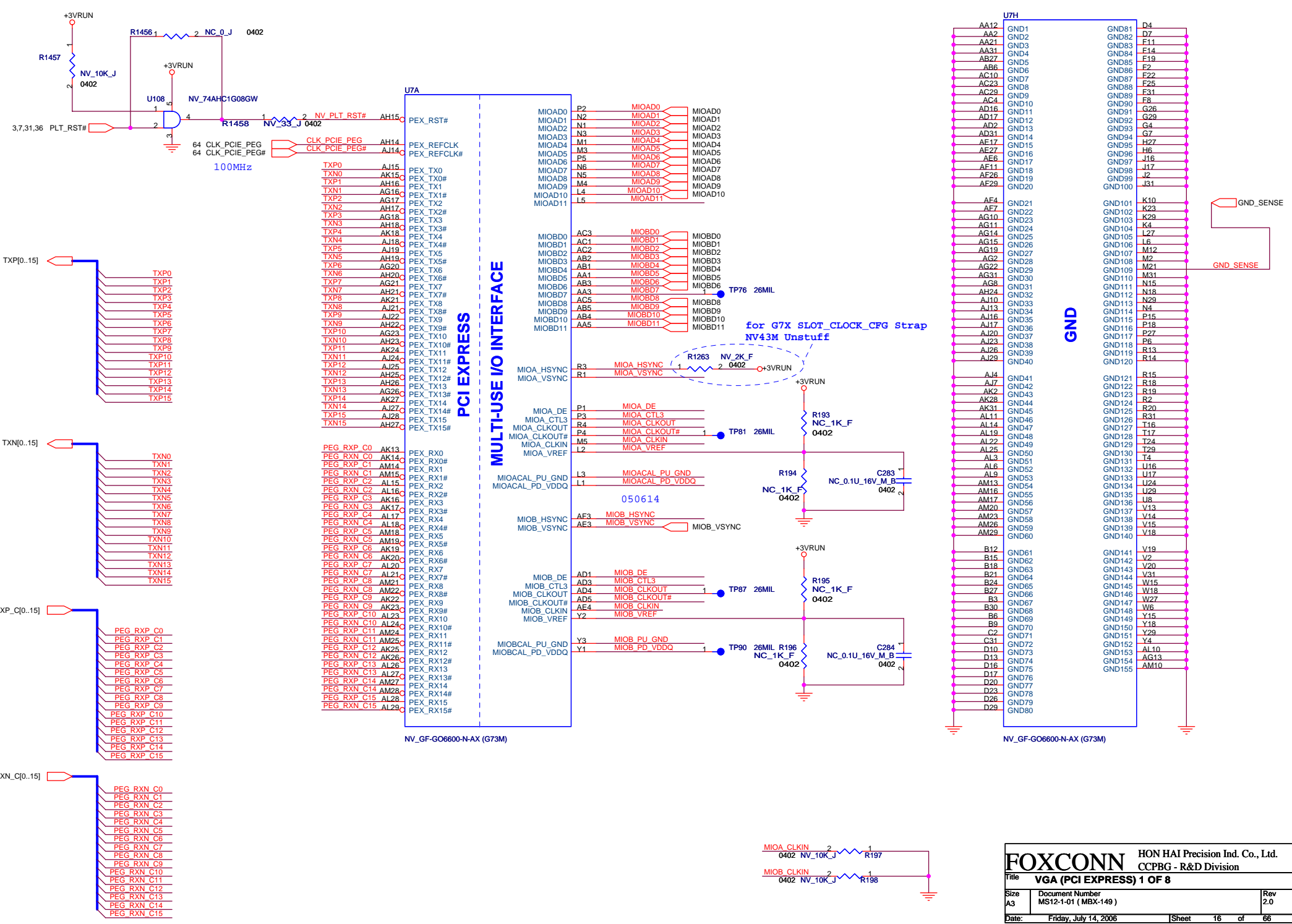
DIMM_1

SMBus Address: A4(W)/A5(R)

DIMM_1 is placed farther from the GMCH than DIMM_0

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
File: DDR(H)SO-DIMM_1		CCPBG - R&D Division	
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MULTI-USE I/O INTERFACE

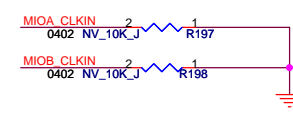
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PEX_REFCLK	AH14	PEX_REFCLK
PEX_REFCLK#	AJ14	PEX_REFCLK#
TXP0	AJ15	PEX_TX0
TXN0	AK15	PEX_TX0#
TXP1	AH16	PEX_TX1
TXN1	AG16	PEX_TX1#
TXP2	AG17	PEX_TX2
TXN2	AG18	PEX_TX2#
TXP3	AH17	PEX_TX3
TXN3	AH18	PEX_TX3#
TXP4	AK18	PEX_TX4
TXN4	AJ18	PEX_TX4#
TXP5	AJ19	PEX_TX5
TXN5	AH19	PEX_TX5#
TXP6	AC20	PEX_TX6
TXN6	AH20	PEX_TX6#
TXP7	AG21	PEX_TX7
TXN7	AH21	PEX_TX7#
TXP8	AK21	PEX_TX8
TXN8	AJ21	PEX_TX8#
TXP9	AH22	PEX_TX9
TXN9	AH23	PEX_TX9#
TXP10	AG23	PEX_TX10
TXN10	AH23	PEX_TX10#
TXP11	AK24	PEX_TX11
TXN11	AJ24	PEX_TX11#
TXP12	AJ25	PEX_TX12
TXN12	AH25	PEX_TX12#
TXP13	AH26	PEX_TX13
TXN13	AG26	PEX_TX13#
TXP14	AK27	PEX_TX14
TXN14	AJ27	PEX_TX14#
TXP15	AJ28	PEX_TX15
TXN15	AH28	PEX_TX15#
PEG_RXP_C0	AK13	PEX_RX0
PEG_RXN_C0	AK14	PEX_RX0#
PEG_RXP_C1	AM14	PEX_RX1
PEG_RXN_C1	AM15	PEX_RX1#
PEG_RXP_C2	AL15	PEX_RX2
PEG_RXN_C2	AL16	PEX_RX2#
PEG_RXP_C3	AK16	PEX_RX3
PEG_RXN_C3	AK17	PEX_RX3#
PEG_RXP_C4	AL17	PEX_RX4
PEG_RXN_C4	AL18	PEX_RX4#
PEG_RXP_C5	AM18	PEX_RX5
PEG_RXN_C5	AM19	PEX_RX5#
PEG_RXP_C6	AK19	PEX_RX6
PEG_RXN_C6	AK20	PEX_RX6#
PEG_RXP_C7	AL20	PEX_RX7
PEG_RXN_C7	AL21	PEX_RX7#
PEG_RXP_C8	AM21	PEX_RX8
PEG_RXN_C8	AM22	PEX_RX8#
PEG_RXP_C9	AK22	PEX_RX9
PEG_RXN_C9	AK23	PEX_RX9#
PEG_RXP_C10	AL23	PEX_RX10
PEG_RXN_C10	AL24	PEX_RX10#
PEG_RXP_C11	AM24	PEX_RX11
PEG_RXN_C11	AM25	PEX_RX11#
PEG_RXP_C12	AK25	PEX_RX12
PEG_RXN_C12	AK26	PEX_RX12#
PEG_RXP_C13	AL26	PEX_RX13
PEG_RXN_C13	AL27	PEX_RX13#
PEG_RXP_C14	AM27	PEX_RX14
PEG_RXN_C14	AM28	PEX_RX14#
PEG_RXP_C15	AL28	PEX_RX15
PEG_RXN_C15	AL29	PEX_RX15#

NV_GF-GO6600-N-AX (G73M)

GND

AA12	GND1	GND81	D4
AA2	GND2	GND82	D7
AA21	GND3	GND83	F11
AA31	GND4	GND84	F14
AB27	GND5	GND84	F19
AB6	GND6	GND85	F2
AC10	GND7	GND86	F22
AC23	GND8	GND87	F25
AC29	GND9	GND88	F31
AC4	GND10	GND89	F8
AD16	GND11	GND90	G26
AD17	GND12	GND91	G29
AD2	GND13	GND92	G4
AD31	GND14	GND93	G7
AE17	GND15	GND94	H27
AE27	GND16	GND95	H6
AE6	GND17	GND96	J16
AF11	GND18	GND97	J17
AF26	GND19	GND98	J2
AE29	GND20	GND99	J27
		GND100	J31
AF4	GND21	GND101	K10
AG10	GND22	GND102	K23
AG11	GND23	GND103	K29
AG14	GND24	GND104	K4
AG15	GND25	GND105	L27
AG19	GND26	GND106	L6
AG2	GND27	GND107	M12
AG22	GND28	GND108	M2
AG24	GND29	GND109	M21
AG8	GND30	GND110	M31
AH24	GND31	GND111	N15
AH25	GND32	GND112	N18
AJ10	GND33	GND113	N29
AJ13	GND34	GND114	N4
AJ16	GND35	GND115	N15
AJ17	GND36	GND116	P27
AJ20	GND37	GND117	P18
AJ23	GND38	GND118	P6
AJ26	GND39	GND119	R13
AJ29	GND40	GND120	R14
		GND121	R15
AJ4	GND41	GND122	R18
AJ7	GND42	GND123	R19
AK2	GND43	GND124	R2
AK28	GND44	GND125	R20
AK31	GND45	GND126	R31
AL11	GND46	GND127	T16
AL14	GND47	GND128	T17
AL19	GND48	GND129	T24
AL22	GND49	GND130	T29
AL25	GND50	GND131	T4
AL3	GND51	GND132	U16
AL6	GND52	GND133	U17
AL9	GND53	GND134	U24
AM13	GND54	GND135	U29
AM16	GND55	GND136	U8
AM20	GND56	GND137	V13
AM23	GND57	GND138	V14
AM26	GND58	GND139	V15
AM29	GND59	GND140	V18
		GND141	V19
B12	GND60	GND142	V2
B15	GND61	GND143	V20
B18	GND62	GND144	V31
B21	GND63	GND145	W15
B24	GND64	GND146	W18
B27	GND65	GND147	W27
B30	GND66	GND148	Y15
B6	GND67	GND149	Y18
B9	GND68	GND150	Y29
C2	GND69	GND151	Y4
C31	GND70	GND152	AL10
D10	GND71	GND153	AG13
D13	GND72	GND154	AM10
D16	GND73	GND155	
D17	GND74		
D20	GND75		
D23	GND76		
D26	GND77		
D29	GND78		
	GND79		
	GND80		

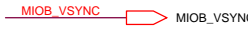
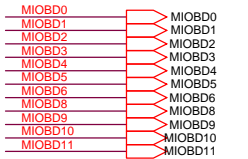
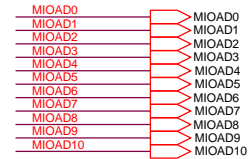
NV_GF-GO6600-N-AX (G73M)



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 CCPBG - R&D Division

Title: **VGA (PCI EXPRESS) 1 OF 8**

Size	Document Number	Rev
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TVMODE(NV43M)
NTSC (01)

MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC <---current setting
1	0	PAL
1	1	CRT

G72M/G73M/NV43M
RAM_CFG(3..0)
*0001 8MX32bit 1.8V
0100 4MX32bit 1.8V Samsung
0101 4MX32bit 1.8V Hynix

SUBVENDOR
*0 (USE SYSTEM BIOS)
1 (USE EXTERNAL ROM)

PANEL ID CONFIG
NC

MIOAD0 is used to set
the PCI Express PLL
termination enable.
DEFAULT "0"

3GIO_PADCFG[2:0]
*001 for NV43/NV44
010 for G7X/NV42

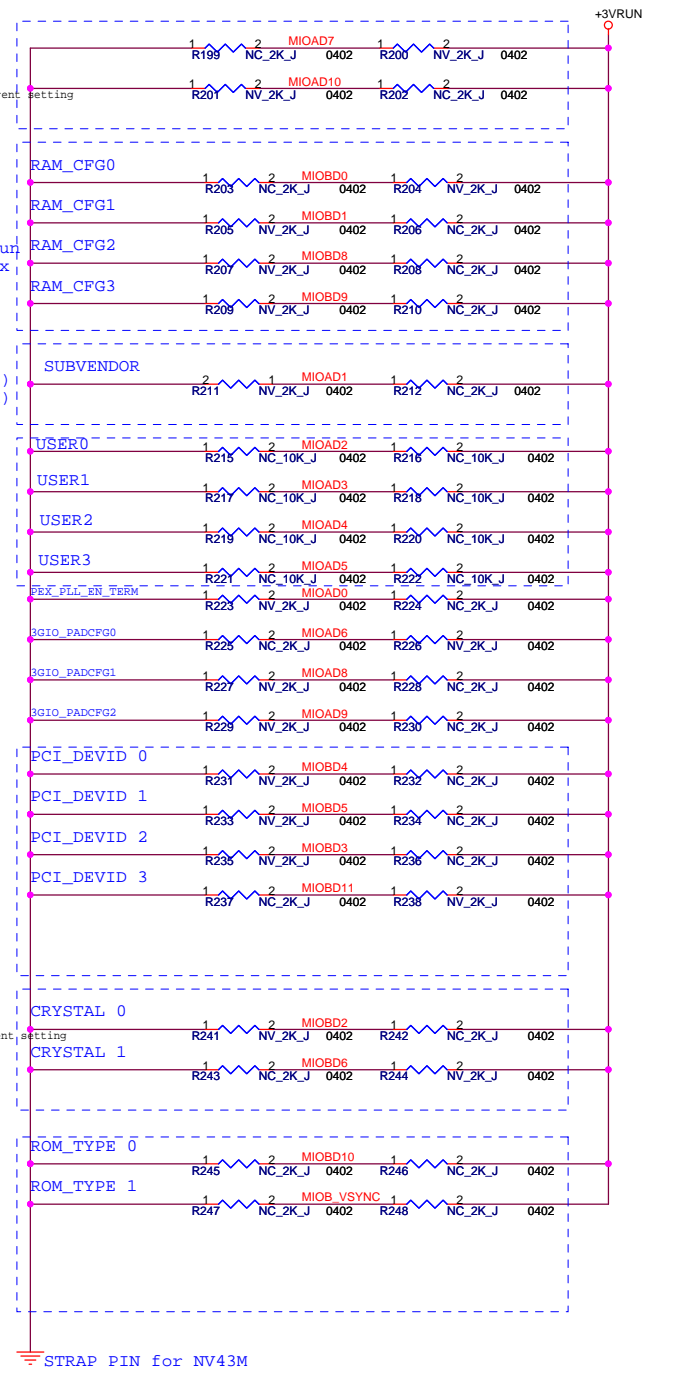
G72M/G73M/NV43M
PCI_DEVID[3:0]="1000"-->8

CRYSTAL(NV43M)
10 (27M Hz)

MIOBD6	MIOBD2	Crystal
1	0	27MHz <---current setting
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

ROM_TYPE(NV43M) NC

00 PARALLEL
01 SERIAL_AT25F
10 SERIAL_SST45VF
11 LPC

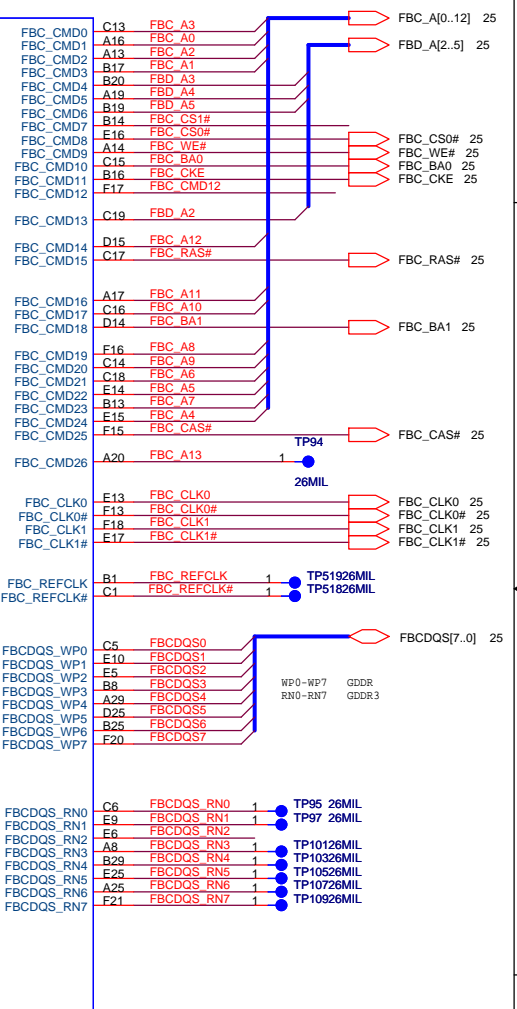
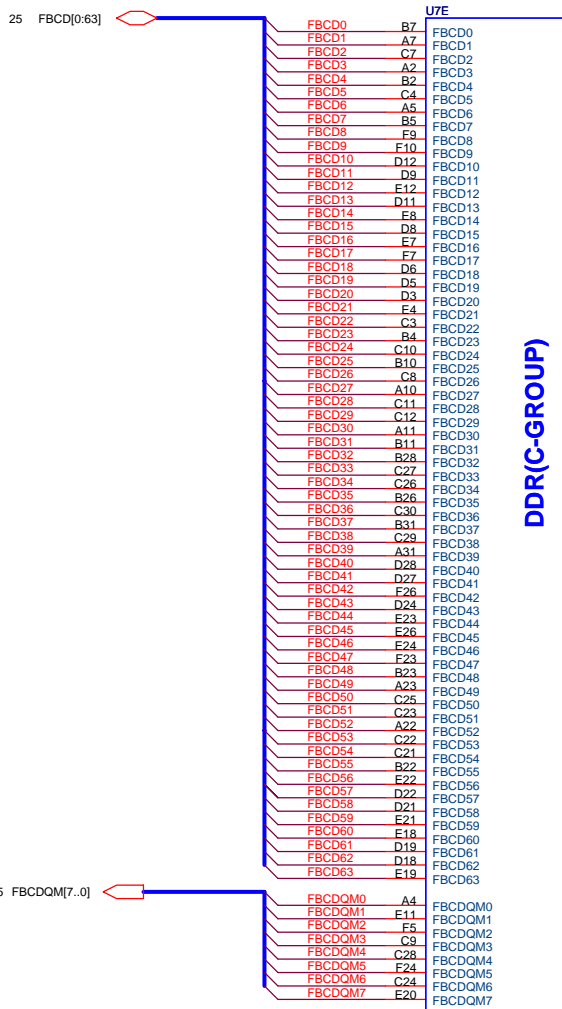
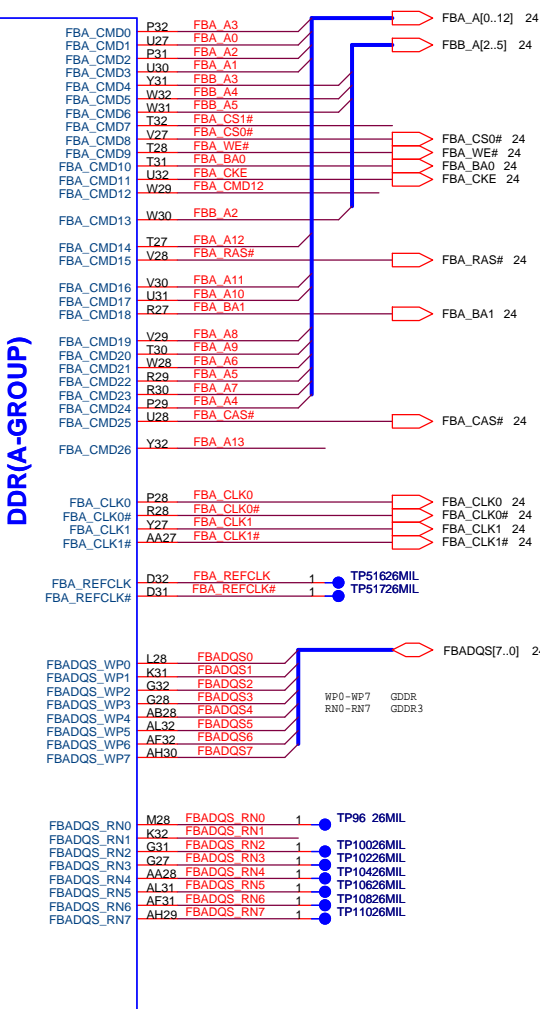
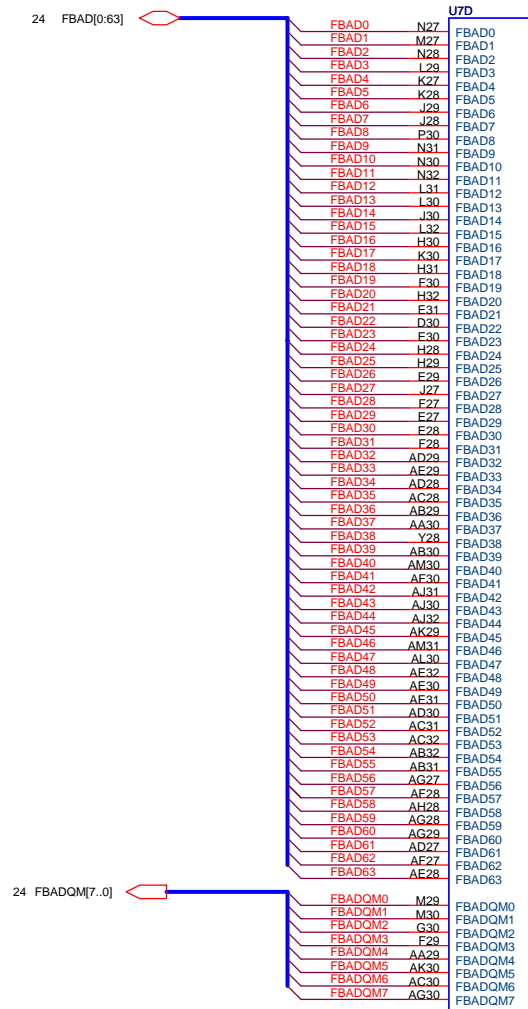


STRAP PIN for NV43M

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Title: **VGA (PCI-EXPRESS/STRAP) 2 OF 8**

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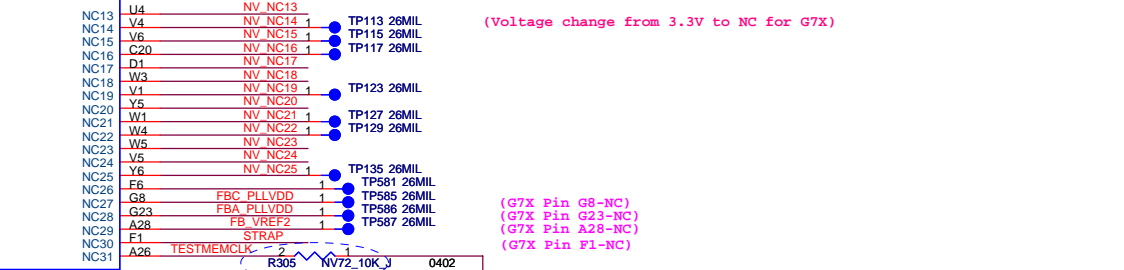
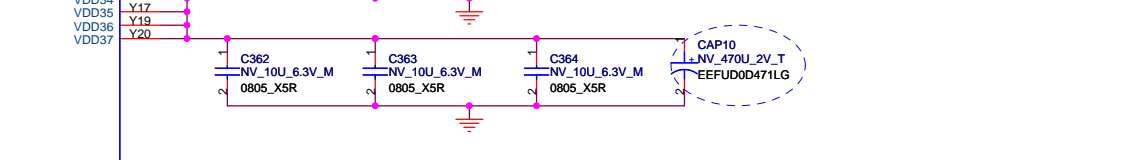
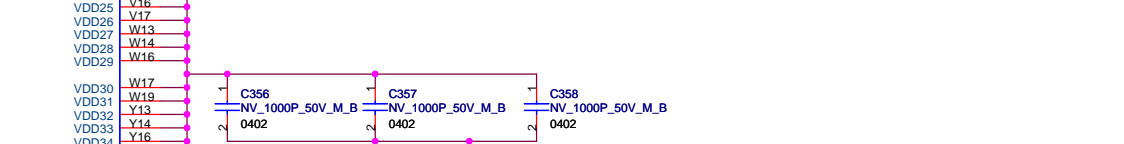
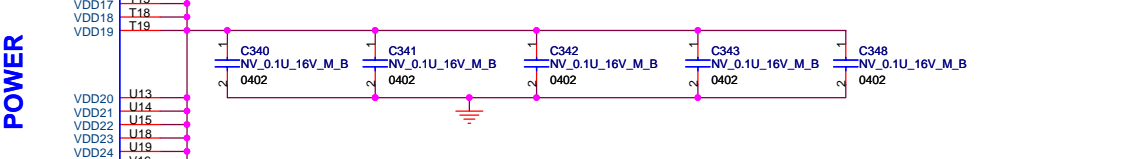
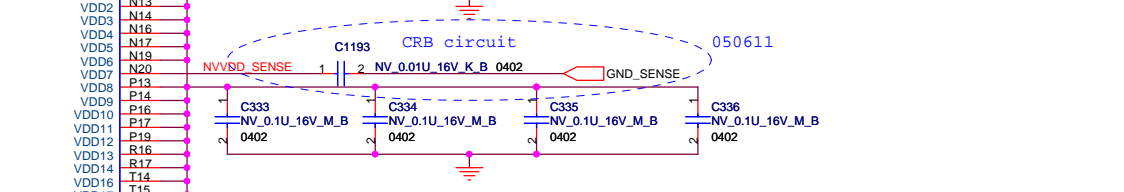
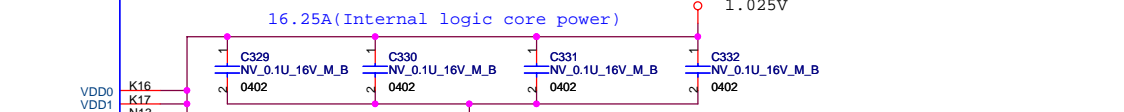
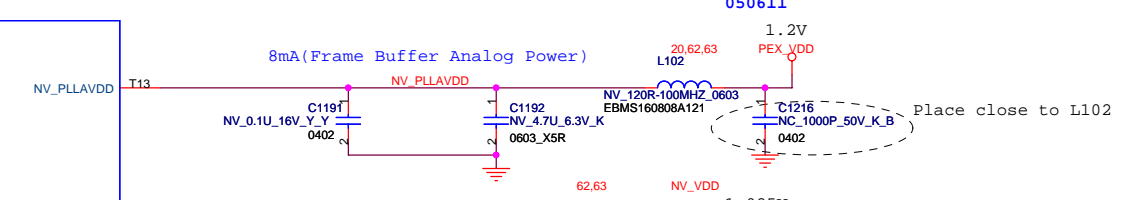
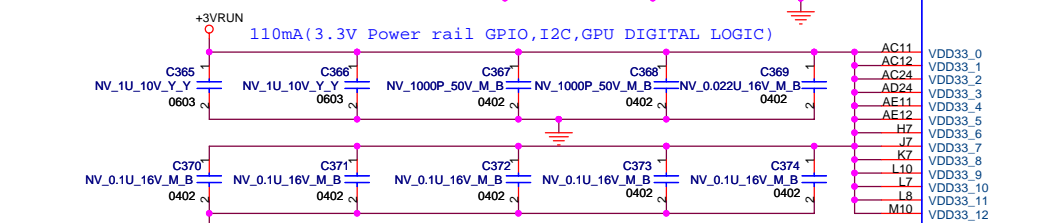
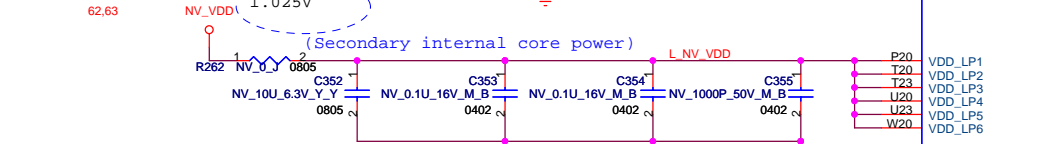
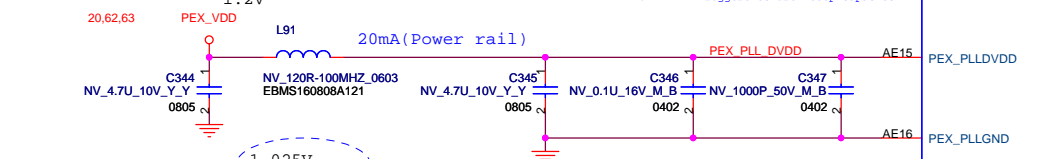
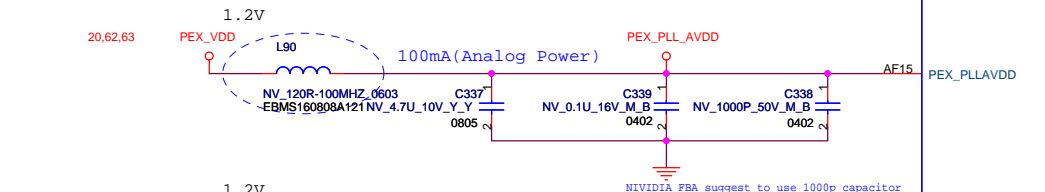
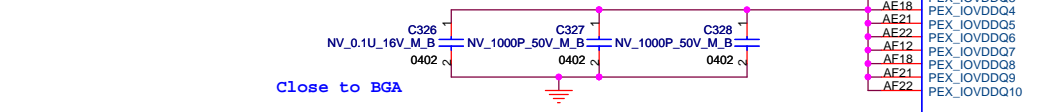
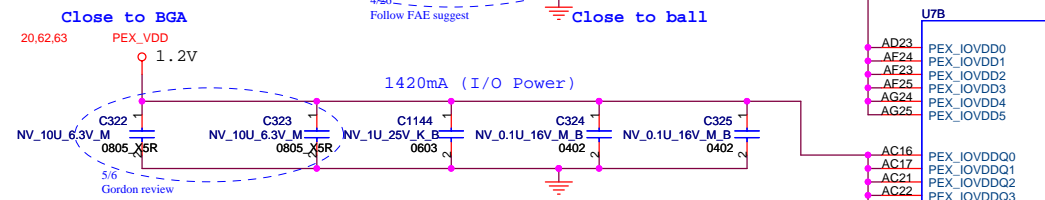
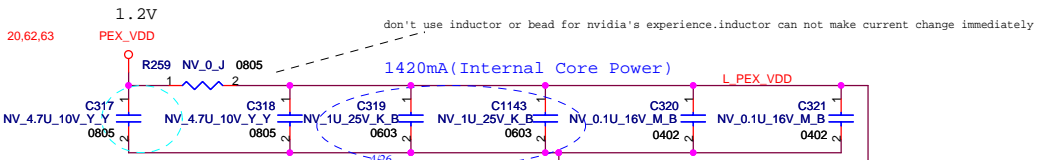


DDR(A-GROUP)

DDR(C-GROUP)

NV_GF-G06600-N-AX (G73M)

NV_GF-G06600-N-AX (G73M)



POWER

VDD0 K16

VDD1 K17

VDD2 N13

VDD3 N14

VDD4 N16

VDD5 N17

VDD6 N19

VDD7 N20

VDD8 P13

VDD9 P14

VDD10 P16

VDD11 P17

VDD12 P19

VDD13 R16

VDD14 T14

VDD16 T15

VDD17 T18

VDD18 T19

VDD19

VDD20 U13

VDD21 U14

VDD22 U15

VDD23 U18

VDD24 U19

VDD25 V16

VDD26 V17

VDD27 W13

VDD28 W14

VDD29 W16

VDD30 W17

VDD31 Y13

VDD32 Y14

VDD33 Y16

VDD34 Y17

VDD35 Y19

VDD36 Y19

VDD37 Y20

VDD LP1 P20

VDD LP2 T23

VDD LP3 U20

VDD LP4 U23

VDD LP5 W20

VDD LP6 W20

VDD33_0 AC11

VDD33_1 AC12

VDD33_2 AC24

VDD33_3 AD24

VDD33_4 AE11

VDD33_5 AE12

VDD33_6 HZ

VDD33_7 HZ

VDD33_8 K7

VDD33_9 L10

VDD33_10 L7

VDD33_11 L8

VDD33_12 M10

VDD33_0 VDD33_3_0

VDD33_1 VDD33_3_1

VDD33_2 VDD33_3_2

VDD33_3 VDD33_3_3

VDD33_4 VDD33_3_4

VDD33_5 VDD33_3_5

VDD33_6 VDD33_3_6

VDD33_7 VDD33_3_7

VDD33_8 VDD33_3_8

VDD33_9 VDD33_3_9

VDD33_10 VDD33_3_10

VDD33_11 VDD33_3_11

VDD33_12 VDD33_3_12

NV_GF-G06600-N-AX (G73M)

G73M Pin A26-NC

G72M Pin A26 need stuff R305 10K

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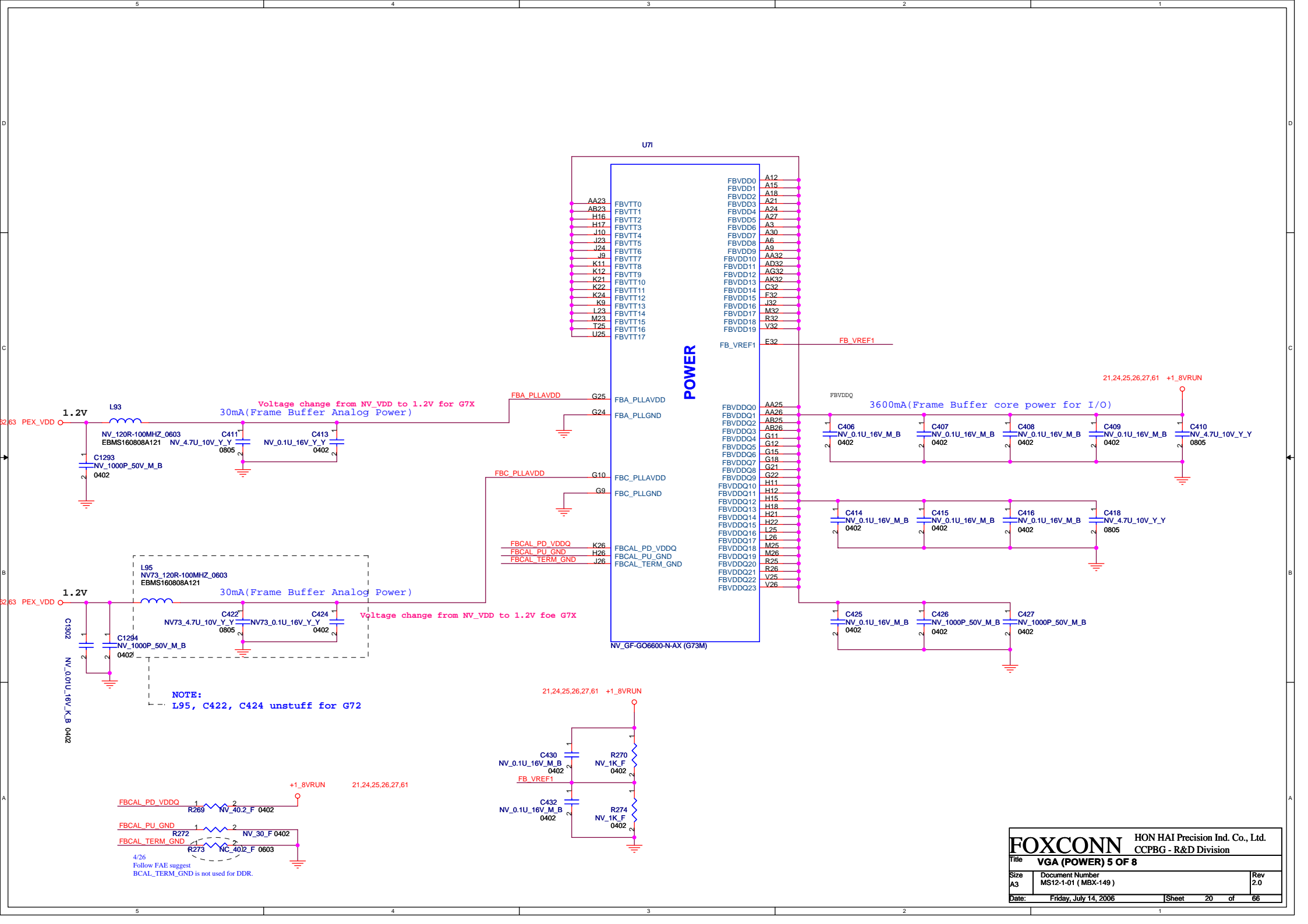
Title VGA (GDDR/I2C/ROM) 4 OF 8

Size Document Number

A3 MS12-1-01 (MBX-149)

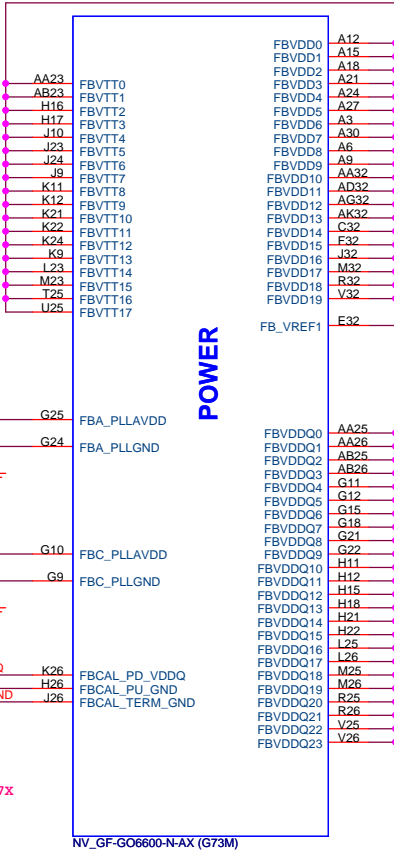
Date: Friday, July 14, 2006

Sheet 19 of 66



U71

POWER



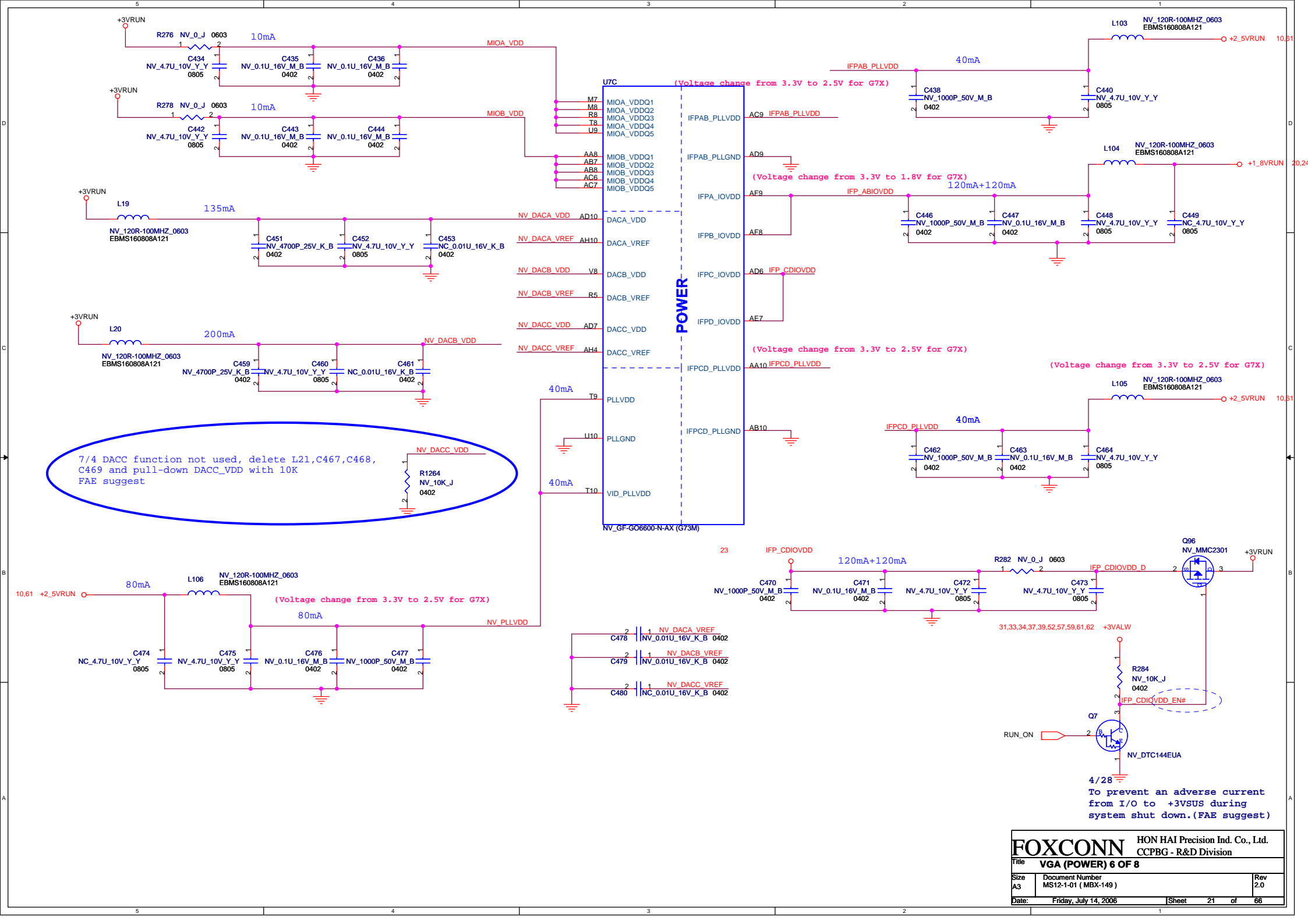
Voltage change from NV_VDD to 1.2V for G7X
30mA(Frame Buffer Analog Power)

3600mA(Frame Buffer core power for I/O)

Voltage change from NV_VDD to 1.2V for G7X

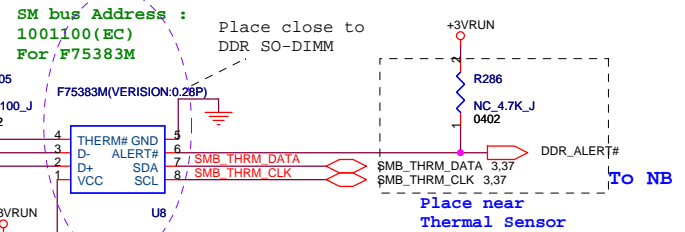
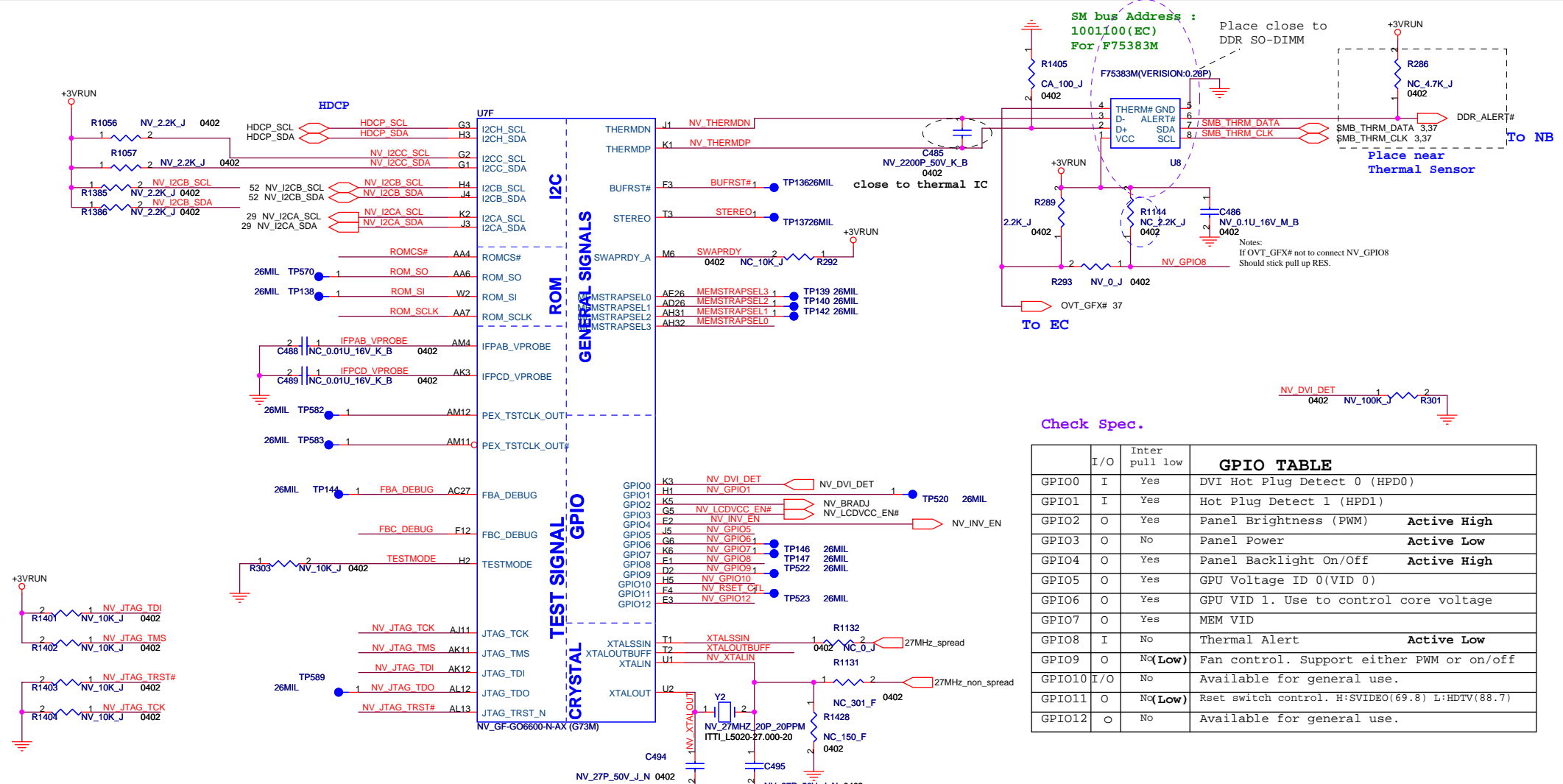
NOTE:
L95, C422, C424 unstuff for G72

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title VGA (POWER) 5 OF 8		
Size A3	Document Number MS12-1-01 (MBX-149)	Rev 2.0
Date: Friday, July 14, 2006	Sheet 20	of 66



7/4 DACB function not used, delete L21, C467, C468, C469 and pull-down DACB_VDD with 10K FAE suggest

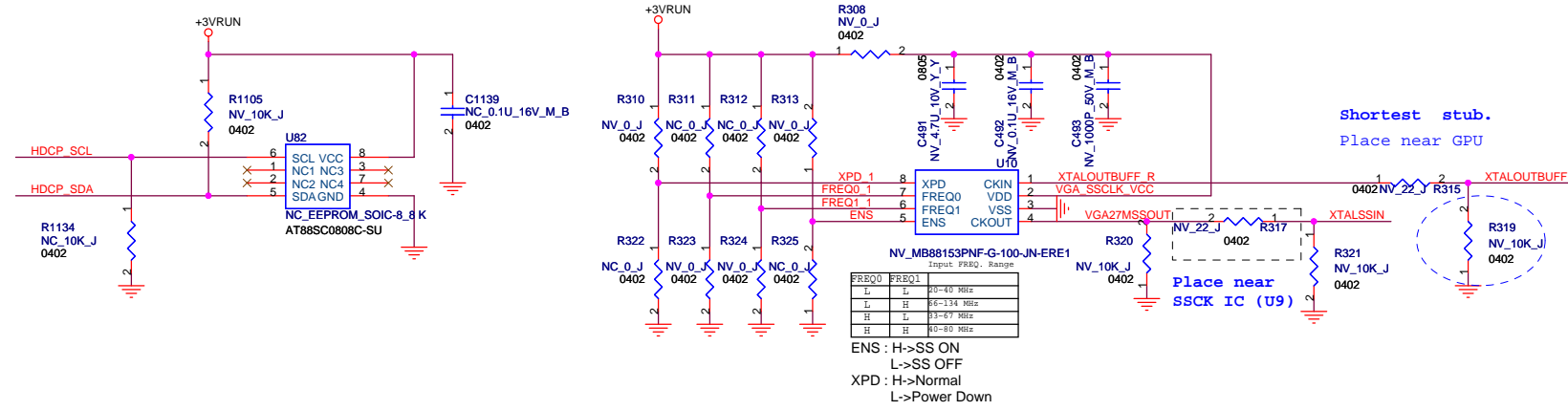
4/28
To prevent an adverse current from I/O to +3VSUS during system shut down. (FAE suggest)



Check Spec.

	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) Active High
GPIO3	O	No	Panel Power Active Low
GPIO4	O	Yes	Panel Backlight On/Off Active High
GPIO5	O	Yes	GPU Voltage ID 0 (VID 0)
GPIO6	O	Yes	GPU VID 1. Use to control core voltage
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert Active Low
GPIO9	O	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	O	No(Low)	Reset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

HDCP ROM



NV_MB88153PNF-G-100-JN-ERE1

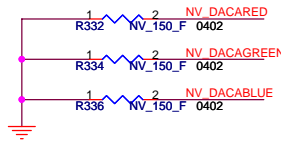
FREQ0	FREQ1	Input FREQ. Range
L	L	80-80 MHz
L	H	80-134 MHz
H	L	133-67 MHz
H	H	80-80 MHz

ENS : H->SS ON
L->SS OFF
XPD : H->Normal
L->Power Down

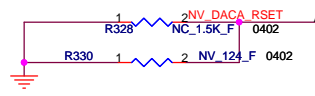
FOXCONN HON HAI Precision Ind. Co., Ltd.
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Title: **VGA (POWER) 7 OF 8**

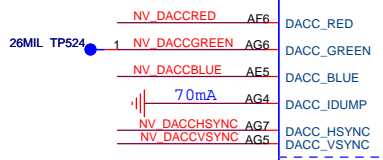
Size A3	Document Number MS12-1-01 (MBX-149)	Rev 2.0
Date: Friday, July 14, 2006	Sheet 22	of 66



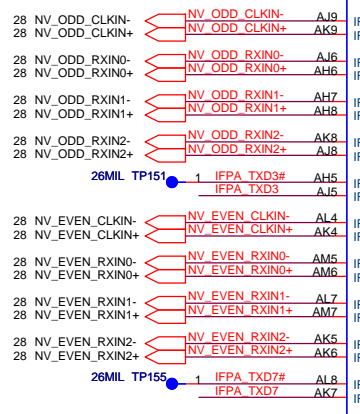
CLOSE TO GPU



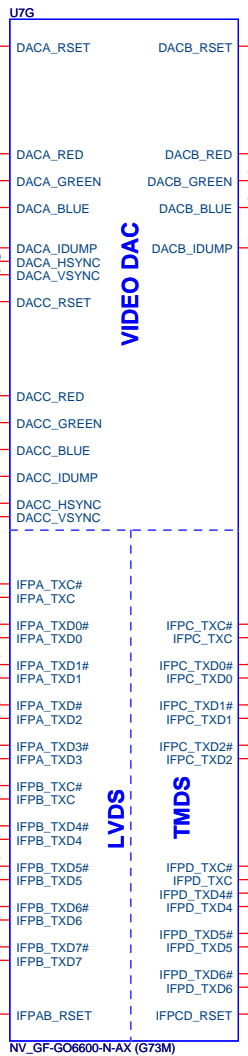
CLOSE TO GPU



DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDOCCLK			SCL
	VGA-DDOCDATA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CB
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDOCCLK			SCL
	DVI-DDOCDATA			SDA

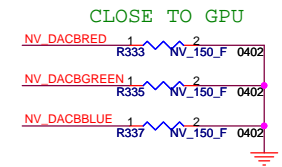


for G7X Unstuff (NC)

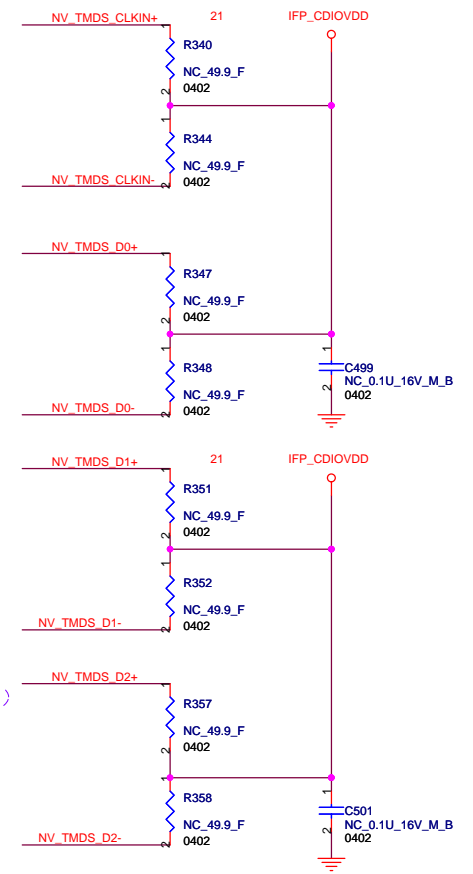


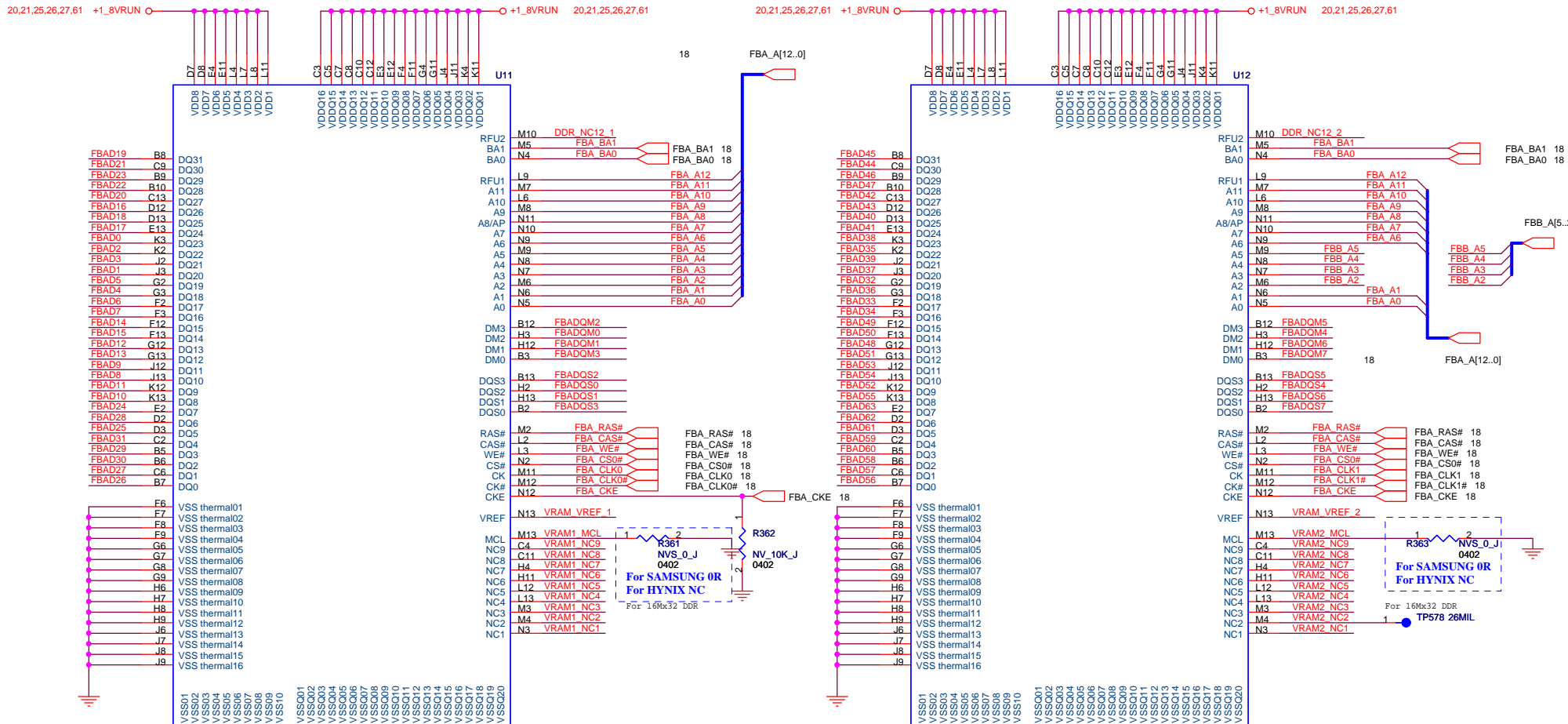
Place close to chipset

for G7X Unstuff (NC)



CLOSE TO GPU



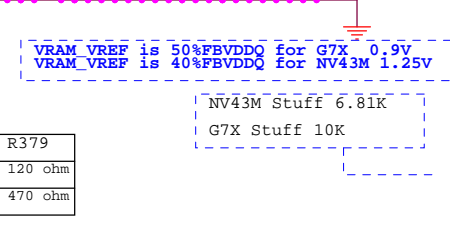
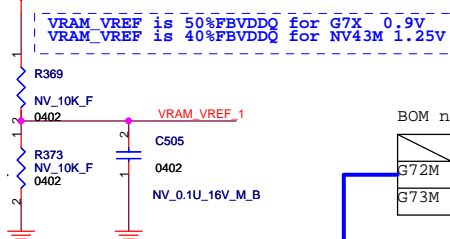


- F6 VSS thermal01
- F7 VSS thermal02
- F8 VSS thermal03
- F9 VSS thermal04
- G6 VSS thermal05
- G7 VSS thermal06
- G8 VSS thermal07
- G9 VSS thermal08
- H6 VSS thermal09
- H7 VSS thermal10
- H8 VSS thermal11
- H9 VSS thermal12
- J6 VSS thermal13
- J7 VSS thermal14
- J8 VSS thermal15
- J9 VSS thermal16

- VSS01
- VSS02
- VSS03
- VSS04
- VSS05
- VSS06
- VSS07
- VSS08
- VSS09
- VSS10
- VSS001
- VSS002
- VSS003
- VSS004
- VSS005
- VSS006
- VSS007
- VSS008
- VSS009
- VSS010
- VSS011
- VSS012
- VSS013
- VSS014
- VSS015
- VSS016
- VSS017
- VSS018
- VSS019
- VSS020

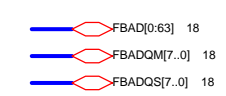
- M13 VRAM1 MCL
- C4 VRAM1 NC9
- C11 VRAM1 NC8
- H4 VRAM1 NC7
- H11 VRAM1 NC6
- L12 VRAM1 NC5
- L13 VRAM1 NC4
- M3 VRAM1 NC3
- M4 VRAM1 NC2
- NC2
- NC1

- VSS001
- VSS002
- VSS003
- VSS004
- VSS005
- VSS006
- VSS007
- VSS008
- VSS009
- VSS010
- VSS001
- VSS002
- VSS003
- VSS004
- VSS005
- VSS006
- VSS007
- VSS008
- VSS009
- VSS010
- VSS011
- VSS012
- VSS013
- VSS014
- VSS015
- VSS016
- VSS017
- VSS018
- VSS019
- VSS020



BOM notice:

R378	R378	R379
G72M	120 ohm	120 ohm
G73M	470 ohm	470 ohm



NV43M Stuff 6.81K
 G7X Stuff 10K

NV43M Stuff 6.81K
 G7X Stuff 10K

- VRAM1_NC8 1 TP160 26MIL
- VRAM1_NC7 1 TP161 26MIL
- VRAM1_NC6 1 TP162 26MIL
- VRAM1_NC4 1 TP165 26MIL
- VRAM1_NC3 1 TP167 26MIL
- VRAM1_NC1 1 TP170 26MIL

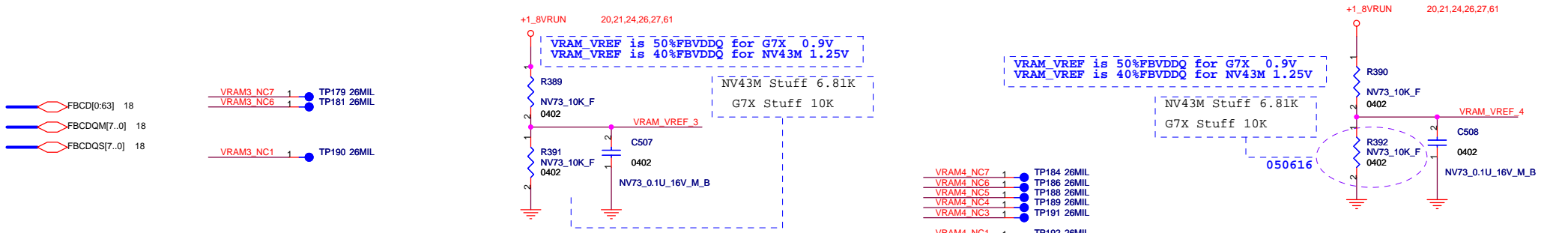
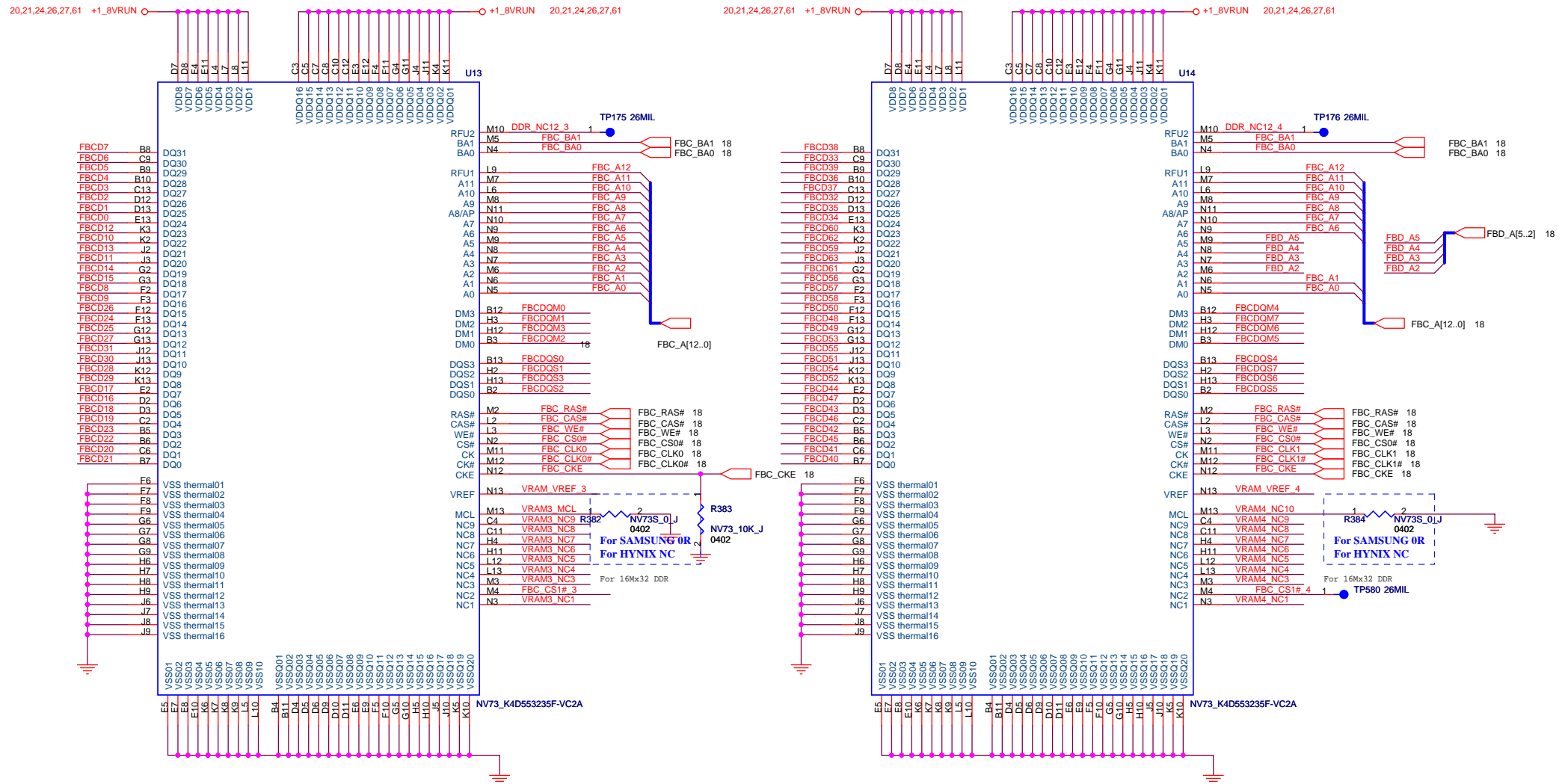
5/16
 FBCLK Termination follow design guide
 DG-01694-001_v01(page 42)100R->120R

- VRAM2_NC8 1 TP166 26MIL
- VRAM2_NC7 1 TP168 26MIL
- VRAM2_NC5 1 TP171 26MIL
- VRAM2_NC3 1 TP173 26MIL

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Title: **VRAM (GDDR) 1 OF 4**

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If use G72M, please unstuff U13, U14 and their related circuit

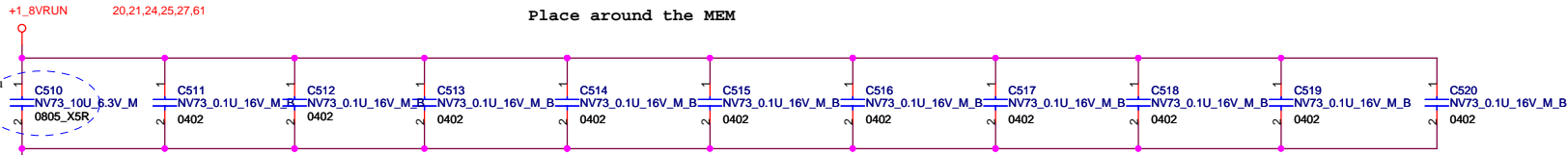
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

File: **VRAM (GDDR) 2 OF 4**

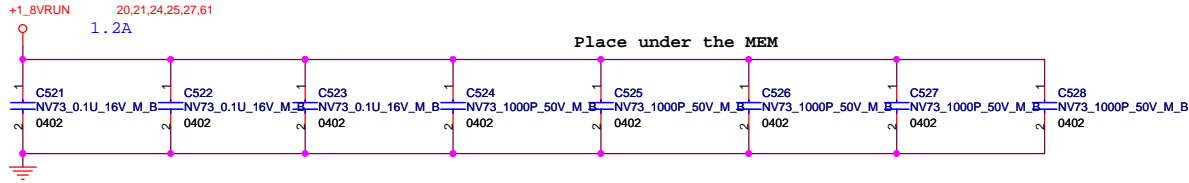
Size A3	Document Number MS12-1-01 (MBX-149)	Rev 2.0
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Decoupling for right MEMORY

Place around the MEM

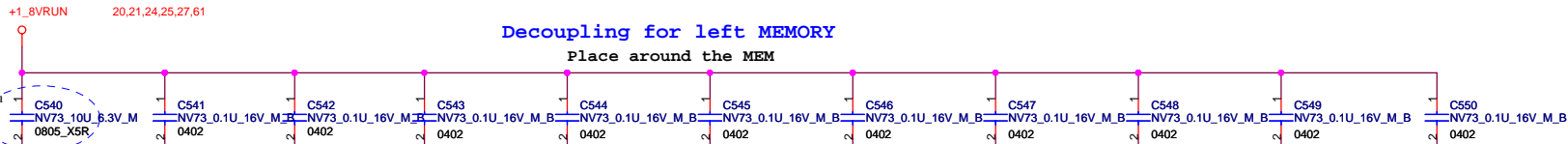


Place under the MEM

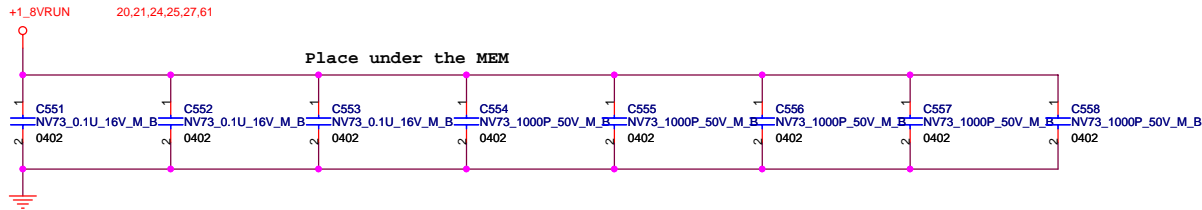


Decoupling for left MEMORY

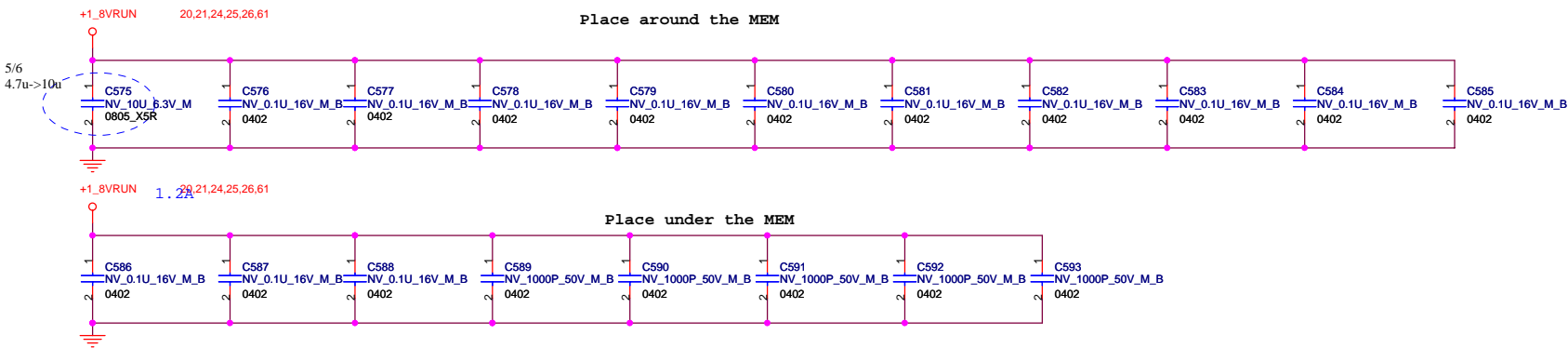
Place around the MEM



Place under the MEM

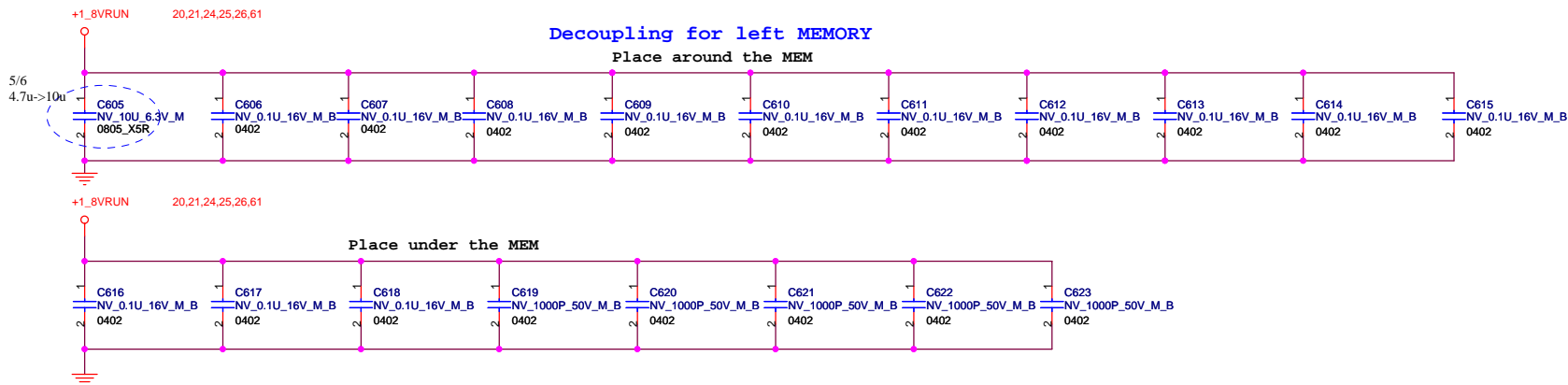


Decoupling for right MEMORY



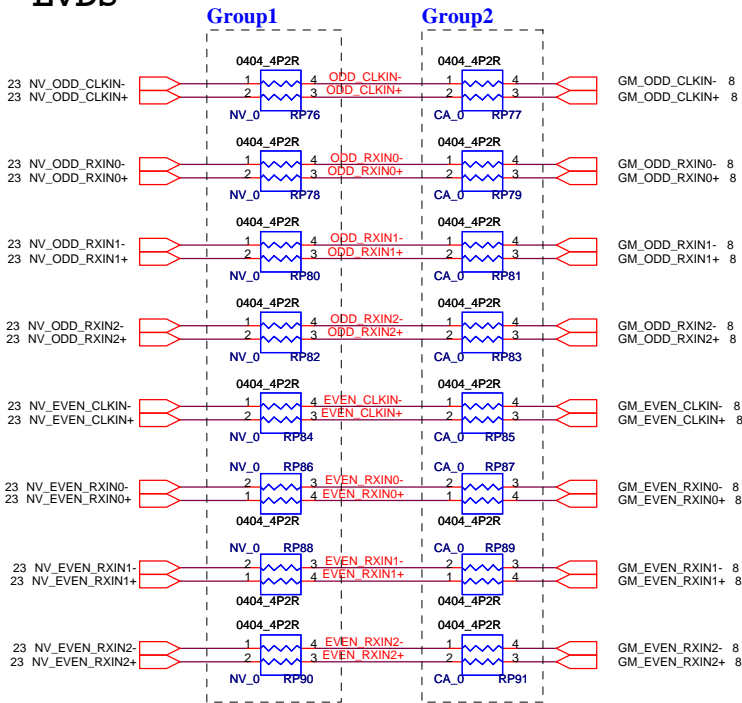
NO USE

Decoupling for left MEMORY

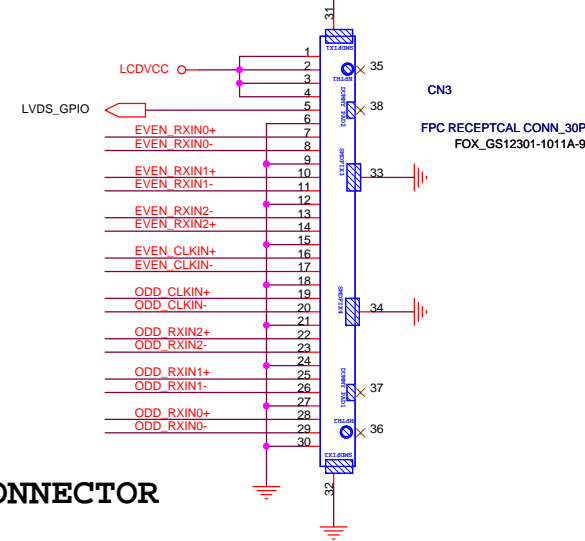


LVDS

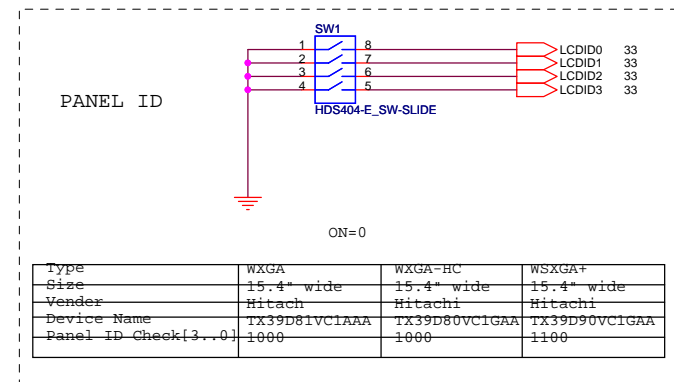
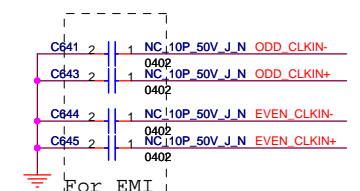
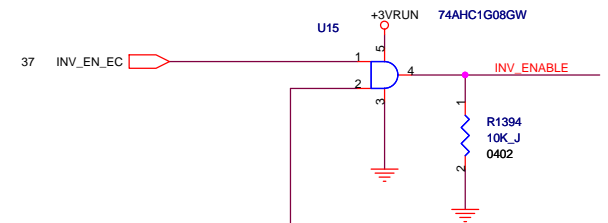
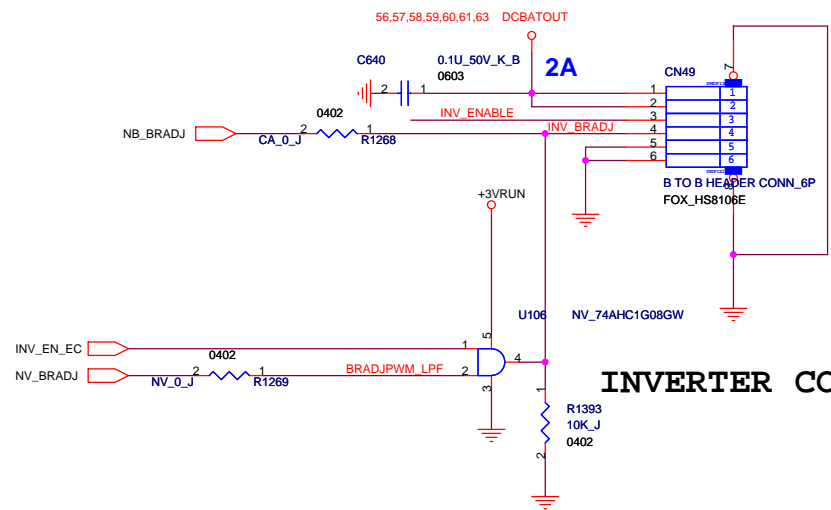
Group1, Group1 should be close



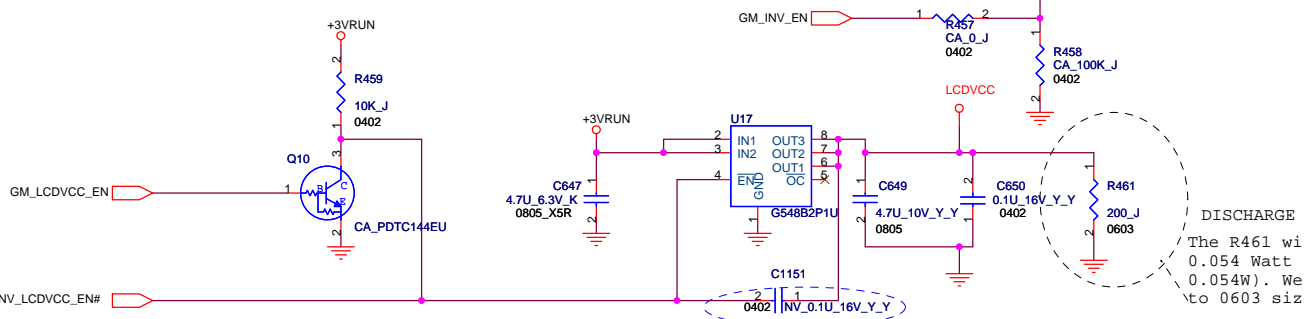
LVDS CONNECTOR



INVERTER CONNECTOR



Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	Hitachi	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC1GAA	TX39D90VC1GAA
Panel ID Check[3..0]	1000	1000	1100



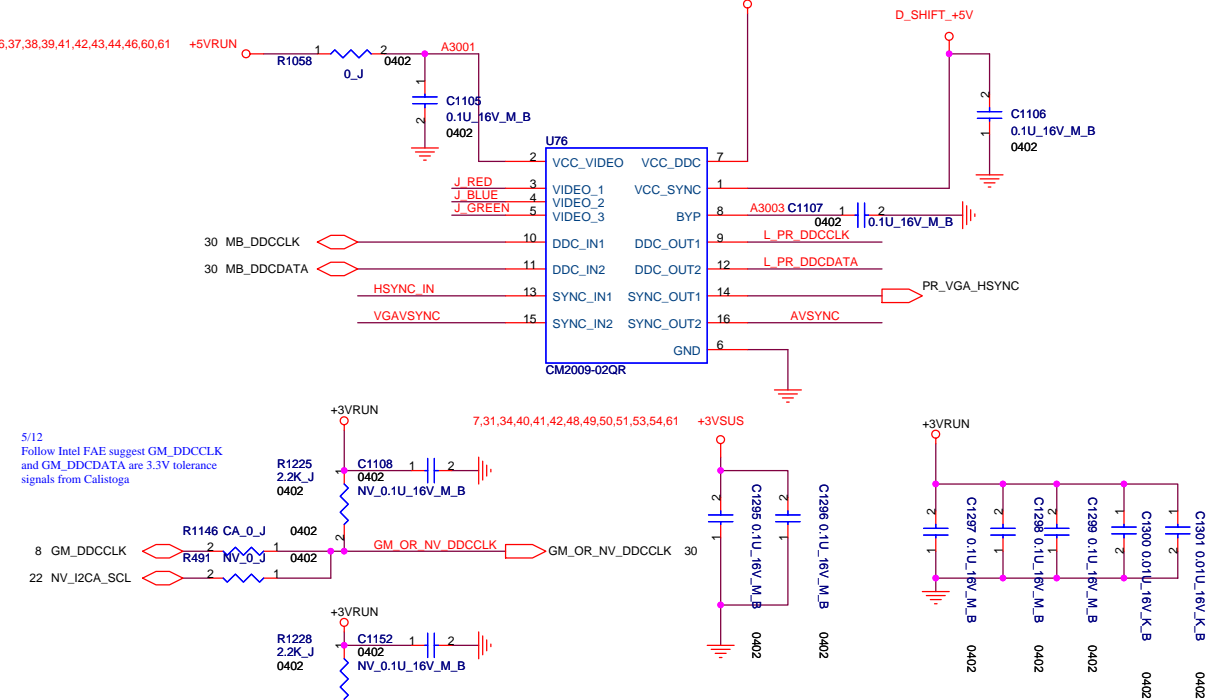
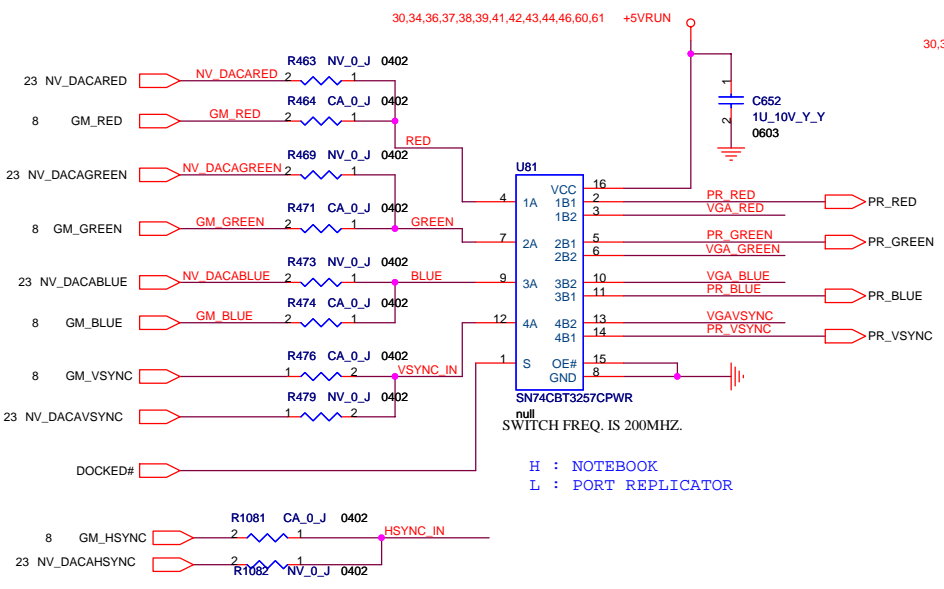
DISCHARGE
 The R461 will consume about 0.054 Watt ($3.3 \times 3.3 / 200 = 0.054W$). We changed resistor to 0603 size (1/8 Watt)

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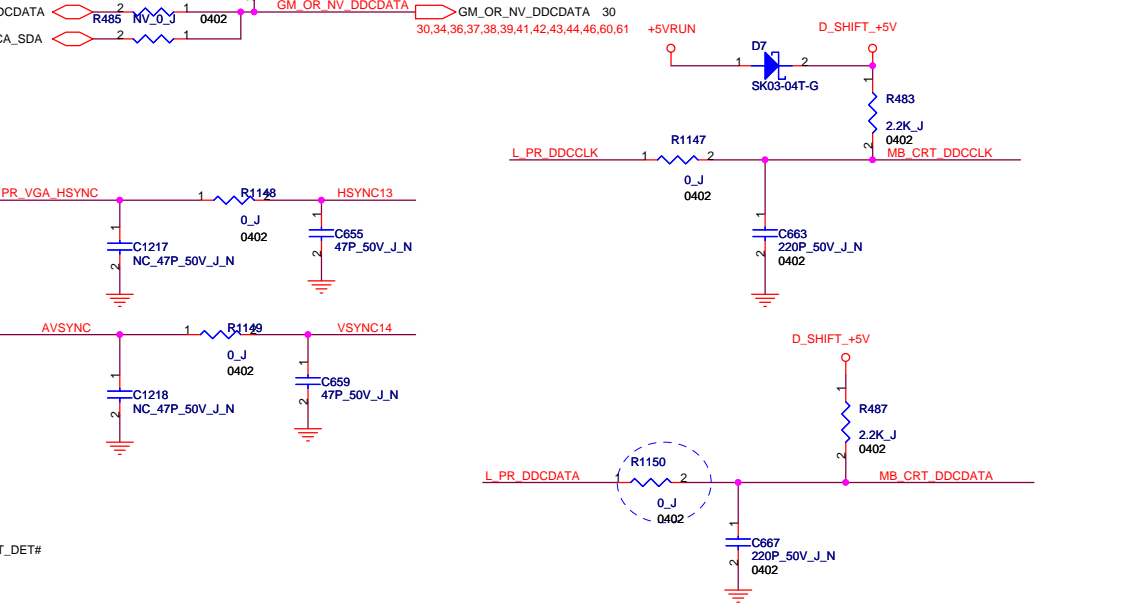
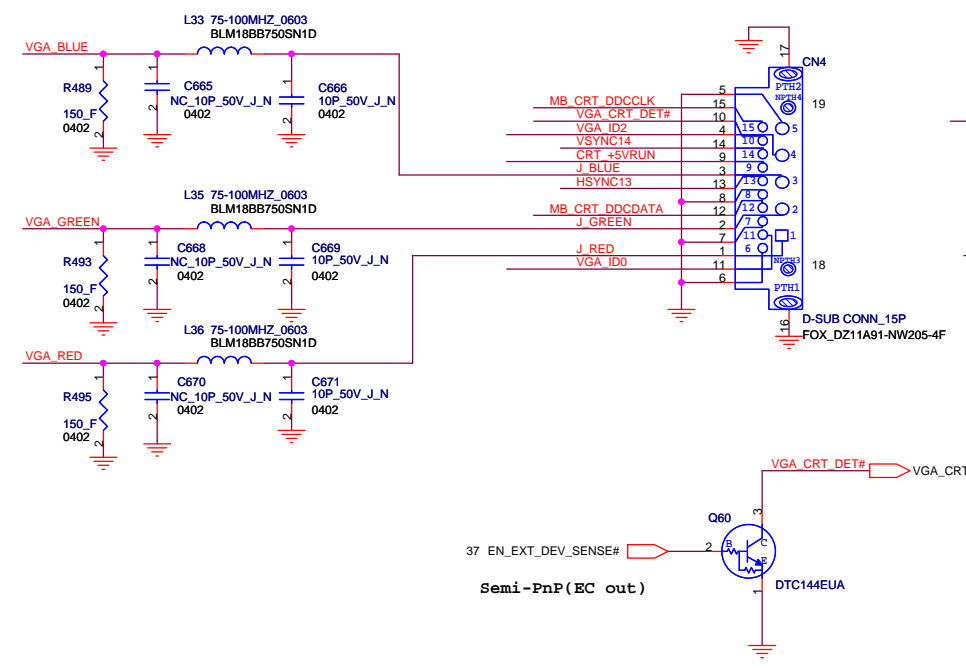
Title: **LVDS**

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CRT ANALOG SWITCH



CRT CONNECTOR

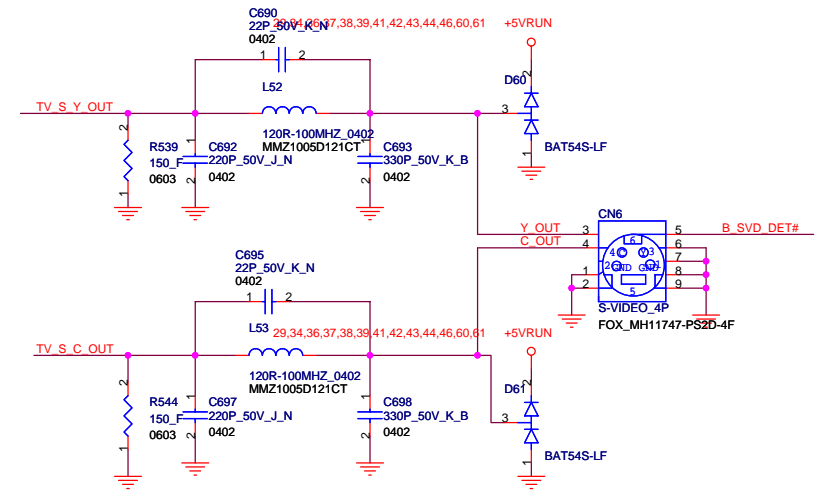
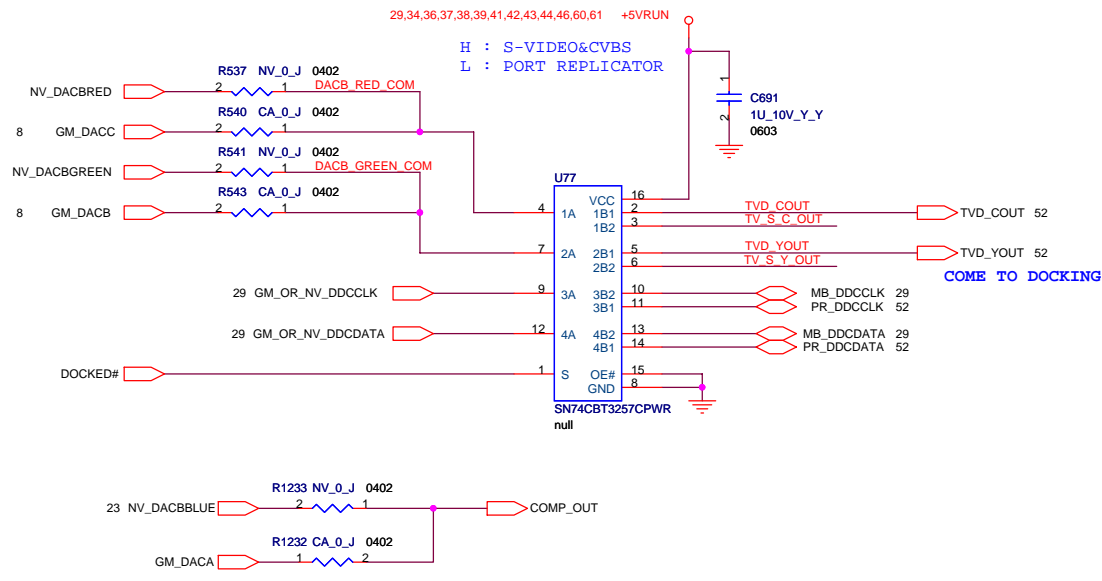


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title CRT		
Size A3	Document Number MS12-1-01 (MBX-149)	Rev 2.0
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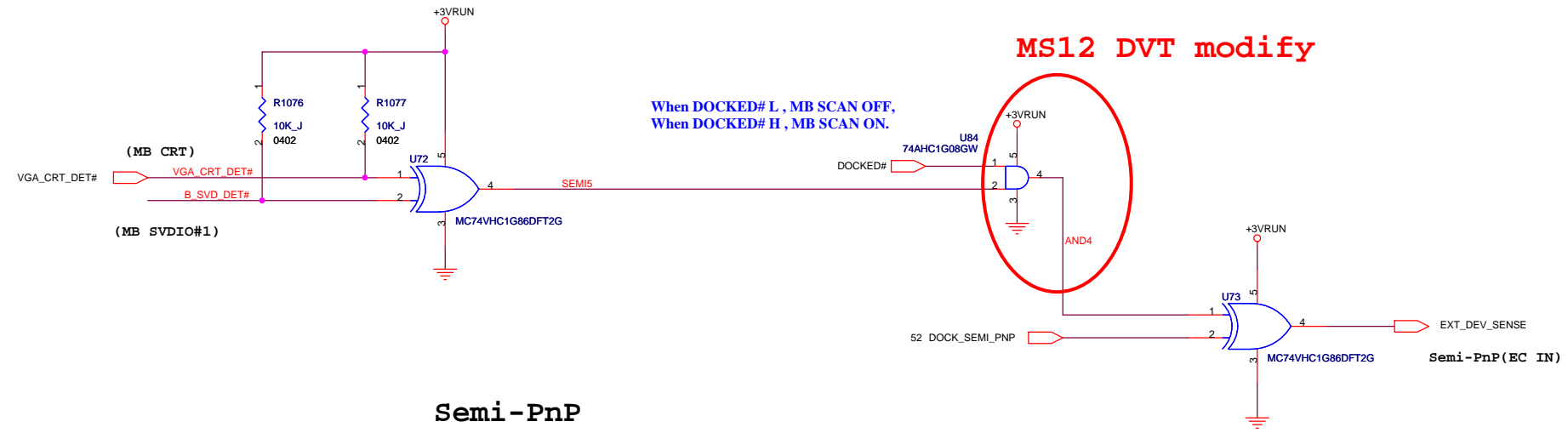
S-VIDEO

These component close to S-Video connector within 700 mil

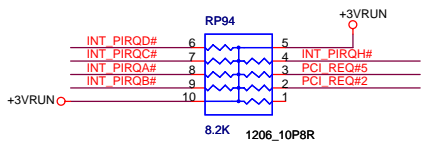
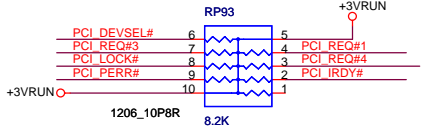
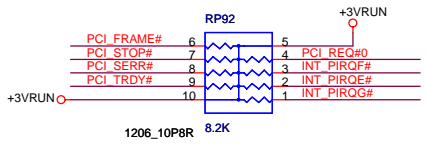
S-VIDEO ANALOG SWITCH



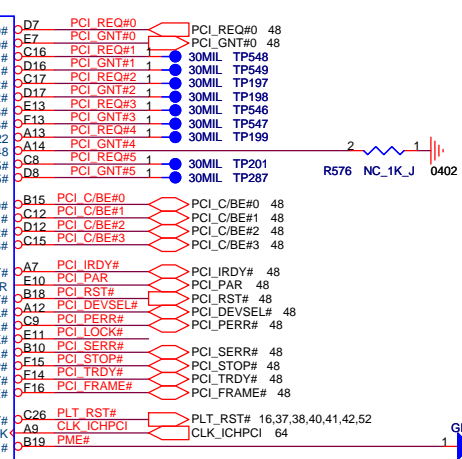
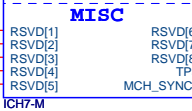
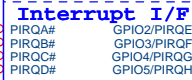
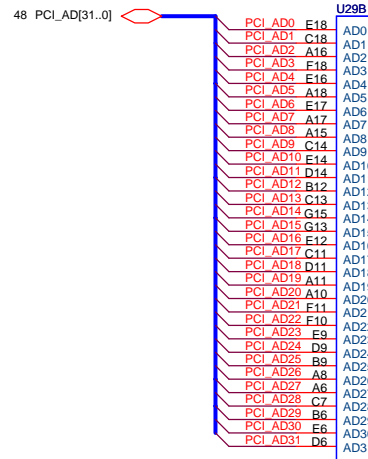
MS12 DVT modify



Semi-PnP

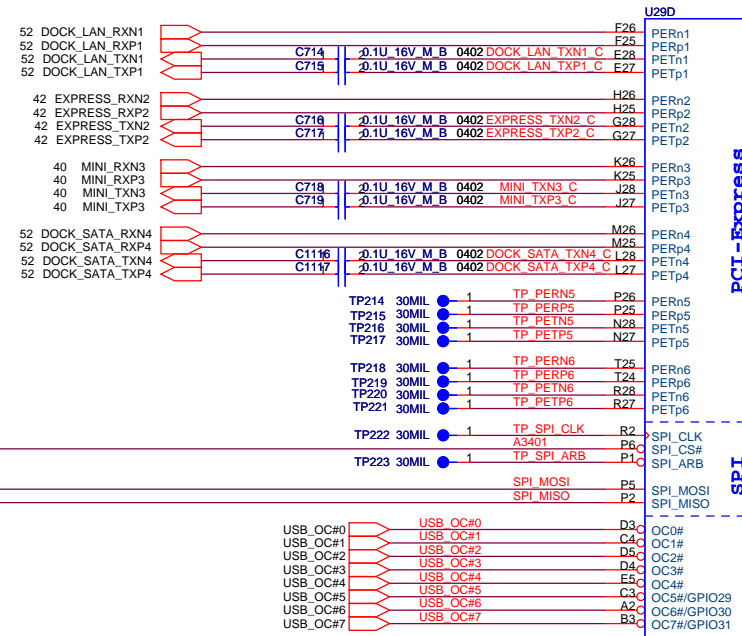
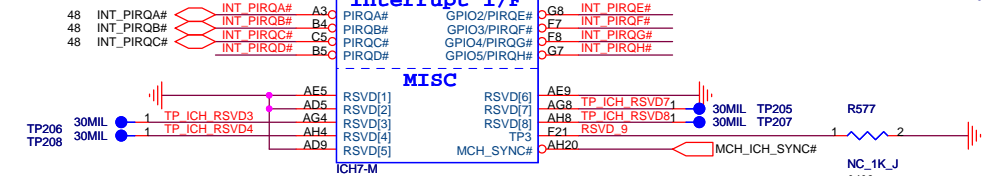


PCI Pullups

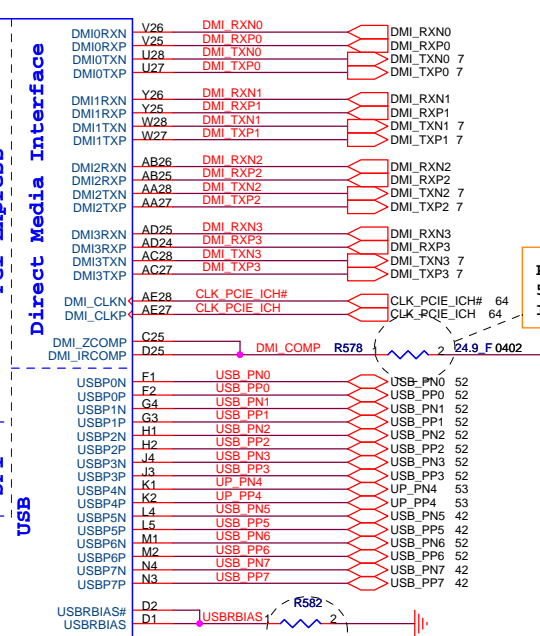
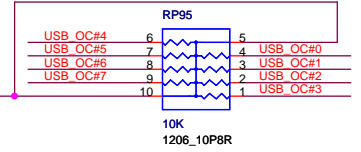
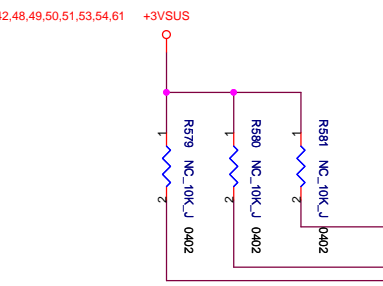


Strap for Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	H1	H1
PCI	H1	LOW



Place within 500 mils of ICH



Place within 500 mils of ICH and don't routing next to high speed signals

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Title: ICH7-M(PCI/DMI/USB/PCIE) 1/5

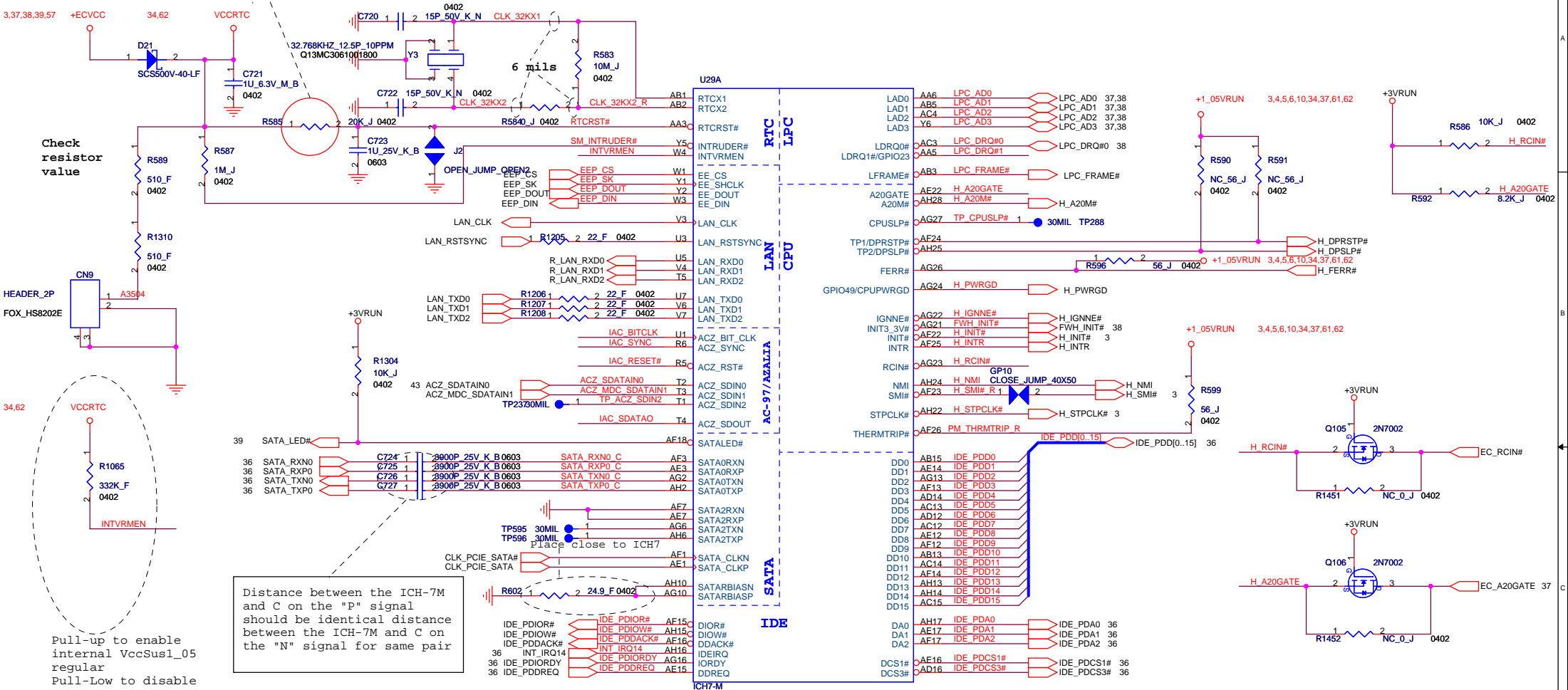
Size A3 Document Number MS12-1-01 (MBX-149) Rev 2.0

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RTRCRST#

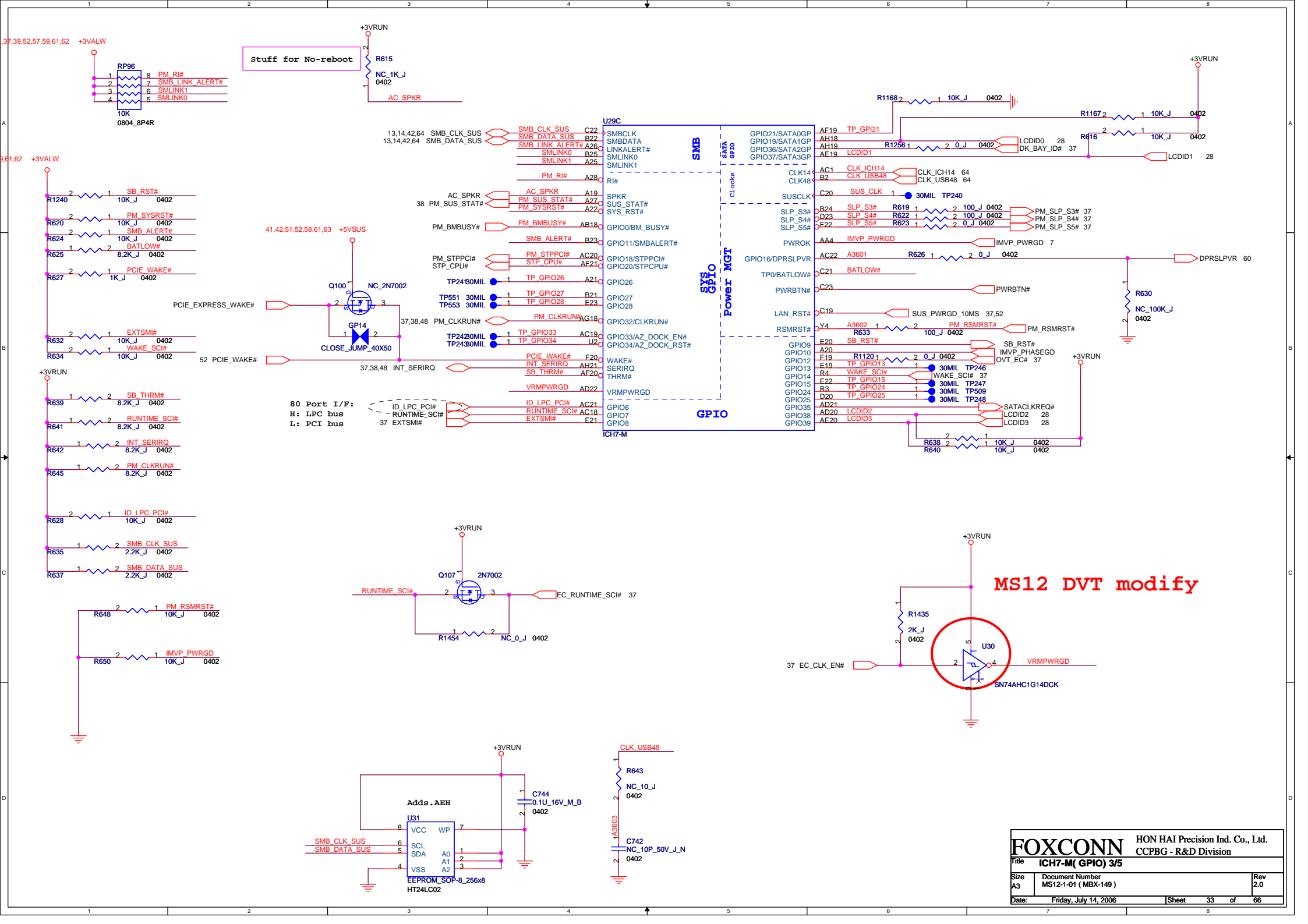
VccRTC
Min : 5ms

The traces inside this block should be wider.
No digital signals routed under XTAL



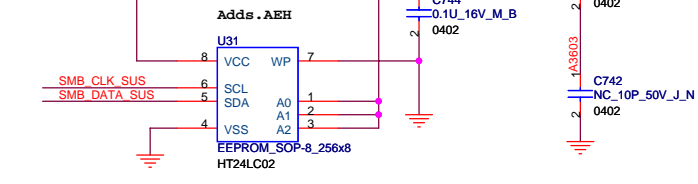
Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair

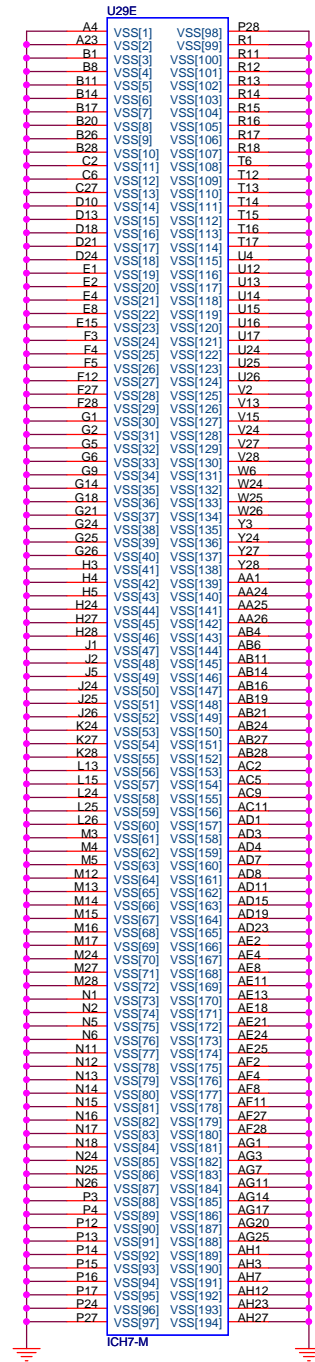
Pull-up to enable internal VccSus1_05 regular Pull-Low to disable



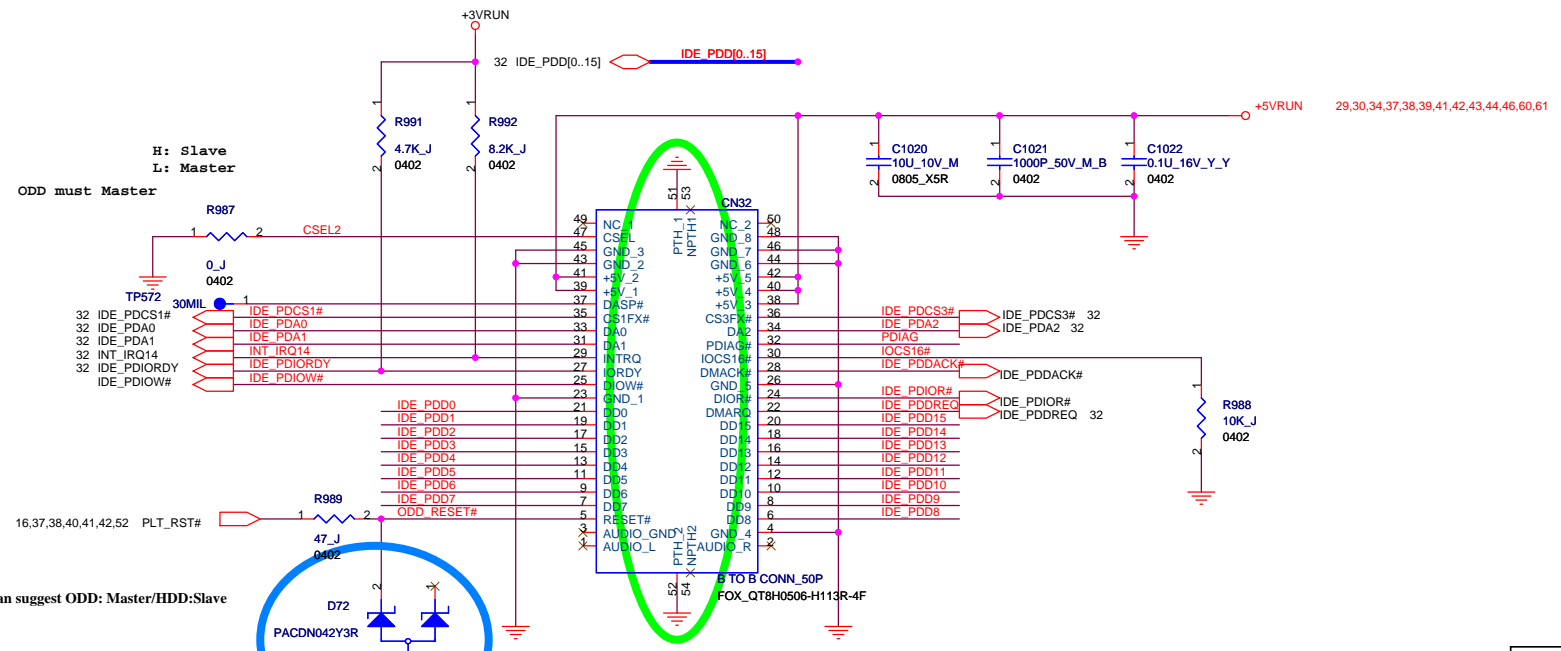
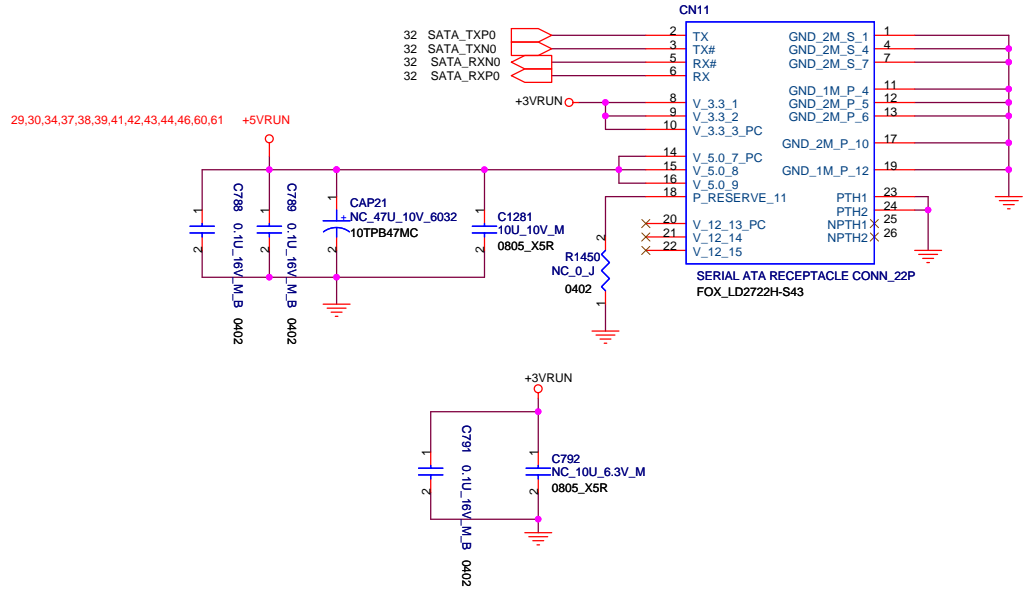
Stuff for No-reboot

MS12 DVT modify





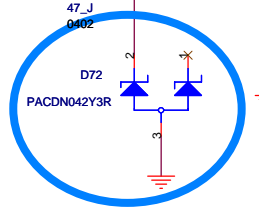
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Title ICH7-M(GND) 5/5			
Size	Document Number	Rev	
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H: Slave
L: Master
ODD must Master

4/17
Follow Adoi san suggest ODD: Master/HDD:Slave

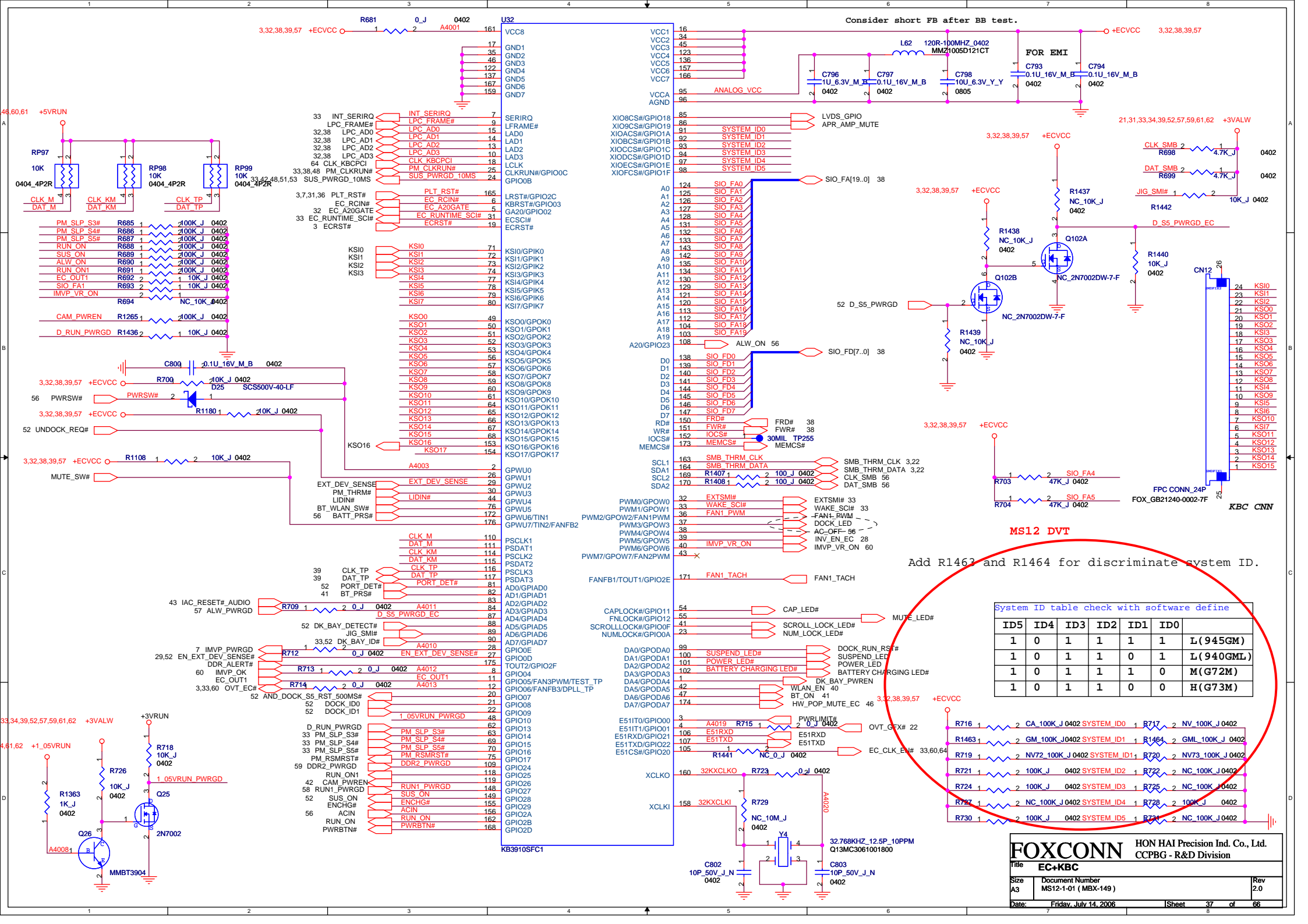
Modify for MP 07/11



CD-ROM CONN

6/13
MS12 PVT Modify footprint

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title SATA HDD/CD-ROM			
Size A3	Document Number MS12-1-01 (MBX-149)	Rev 2.0	
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Consider short FB after BB test.

FOR EMI

CLK SMB 2 1 4.7K_J 0402

DAT SMB 2 1 4.7K_J 0402

JIG SMIF 1 1 10K_J 0402

D S5_PWRGD EC

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

NC_10K_J 0402

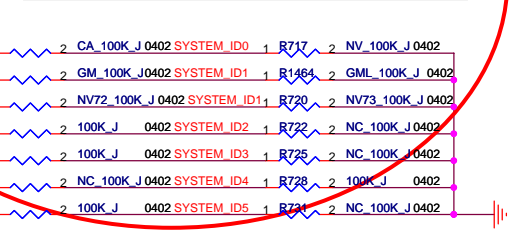
NC_2N7002DW-7-F

NC_10K_J 0402

NC_2N7002DW-7-F

System ID table check with software define

ID5	ID4	ID3	ID2	ID1	ID0	
1	0	1	1	1	1	L(945GM)
1	0	1	1	0	1	L(940GML)
1	0	1	1	1	0	M(G72M)
1	0	1	1	0	0	H(G73M)



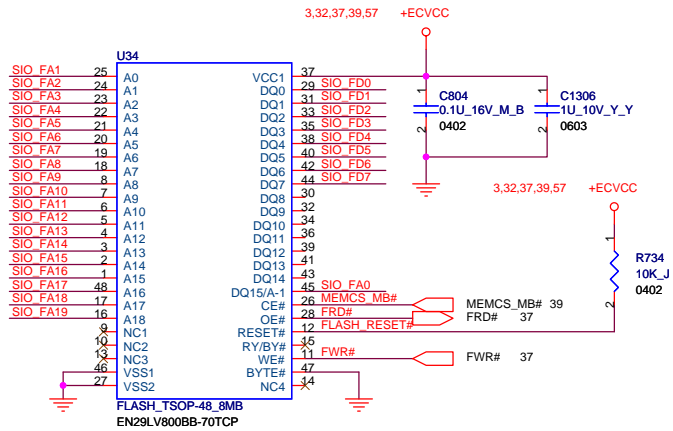
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

File: **EC+KBC**

Size: A3 Document Number: MS12-1-01 (MBX-149) Rev: 2.0

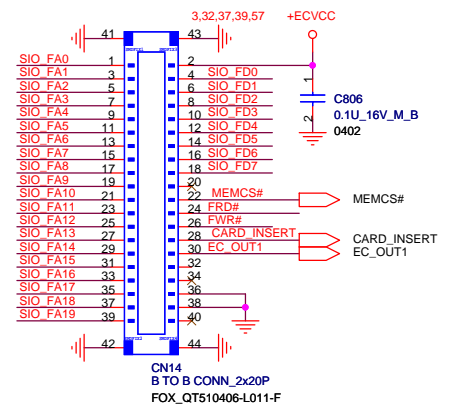
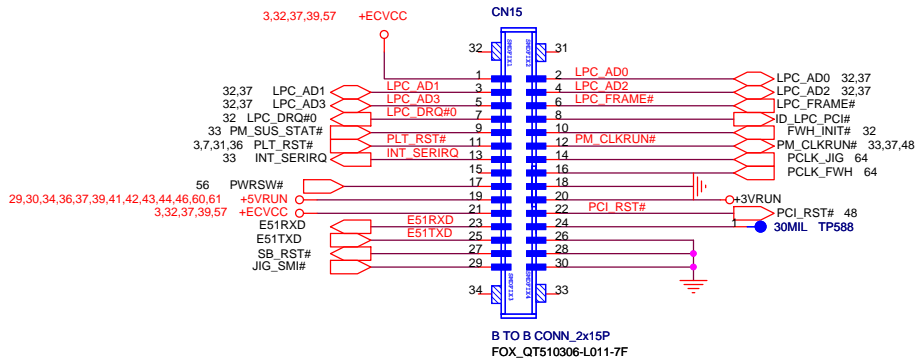
Date: Friday, July 14, 2006 Sheet: 37 of 66

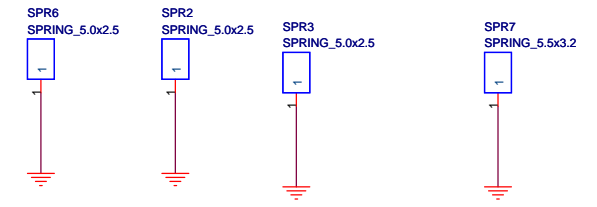
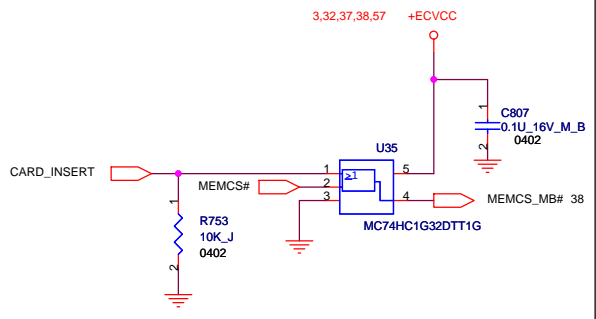
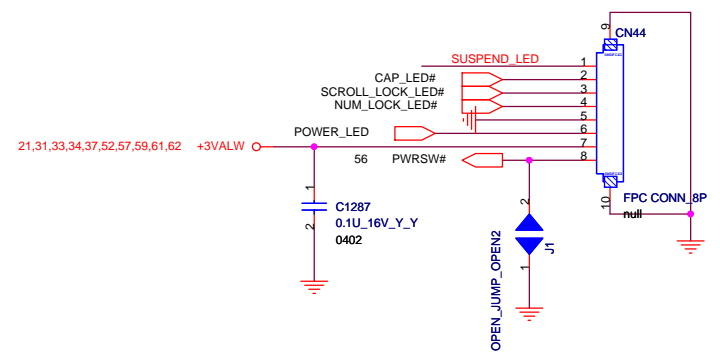
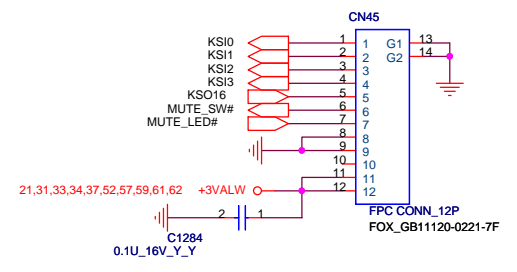
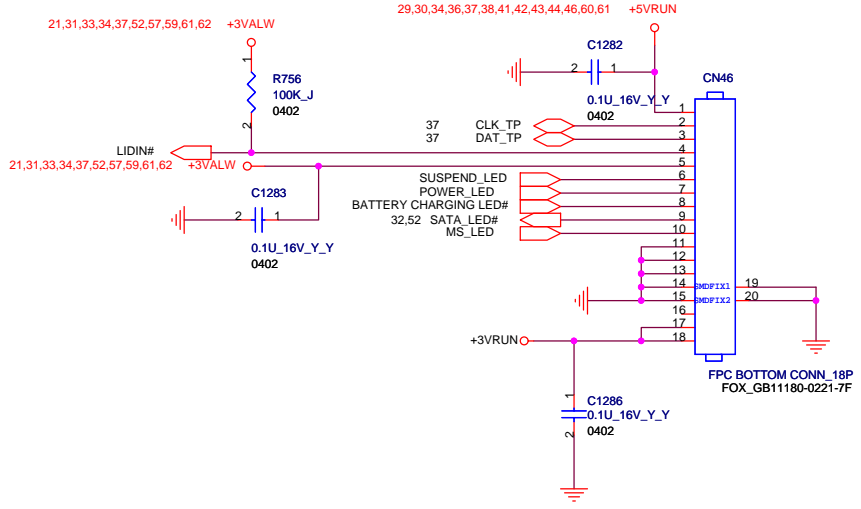
37 SIO_FA[19..0]
 37 SIO_FD[7..0]

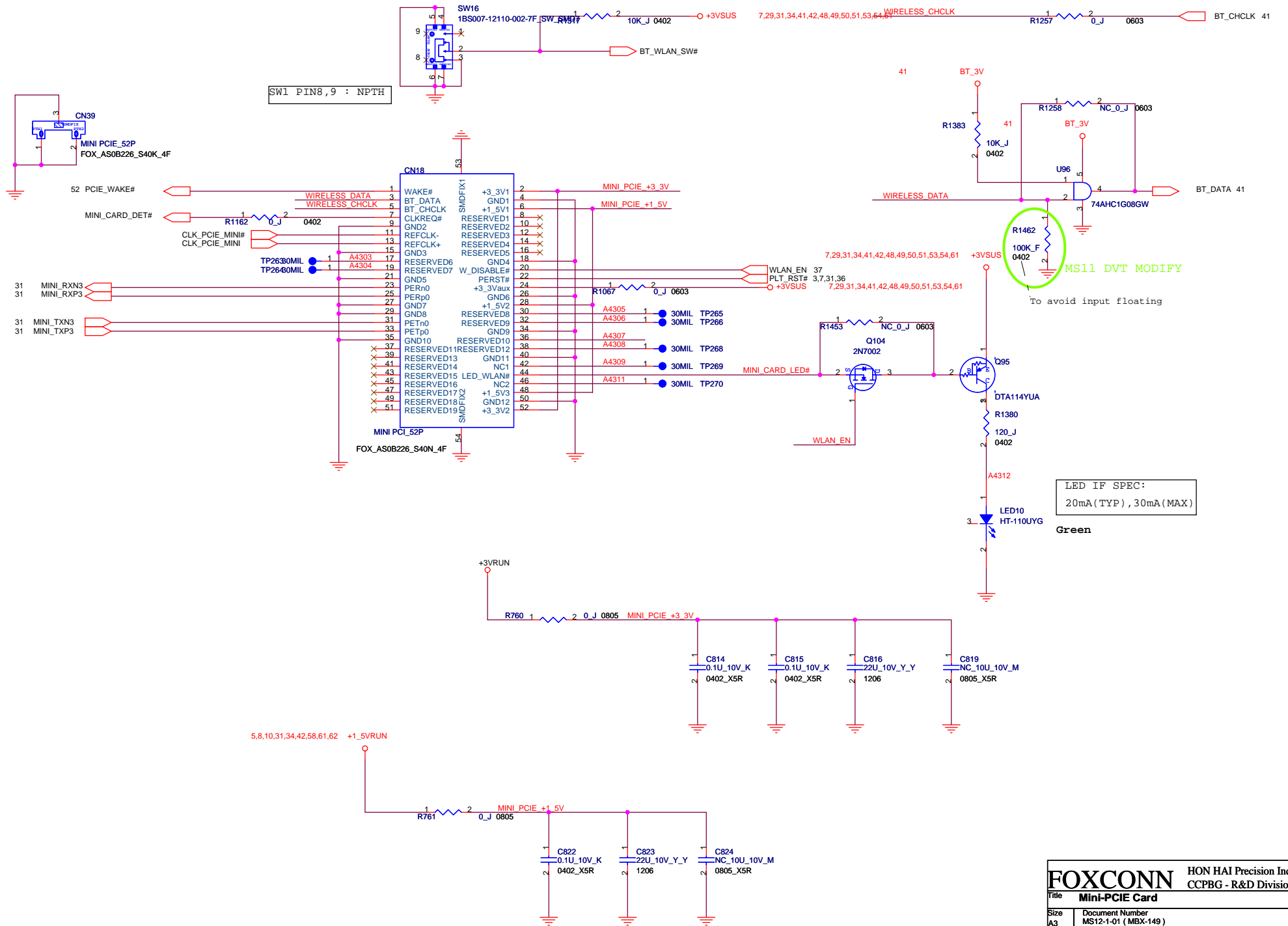


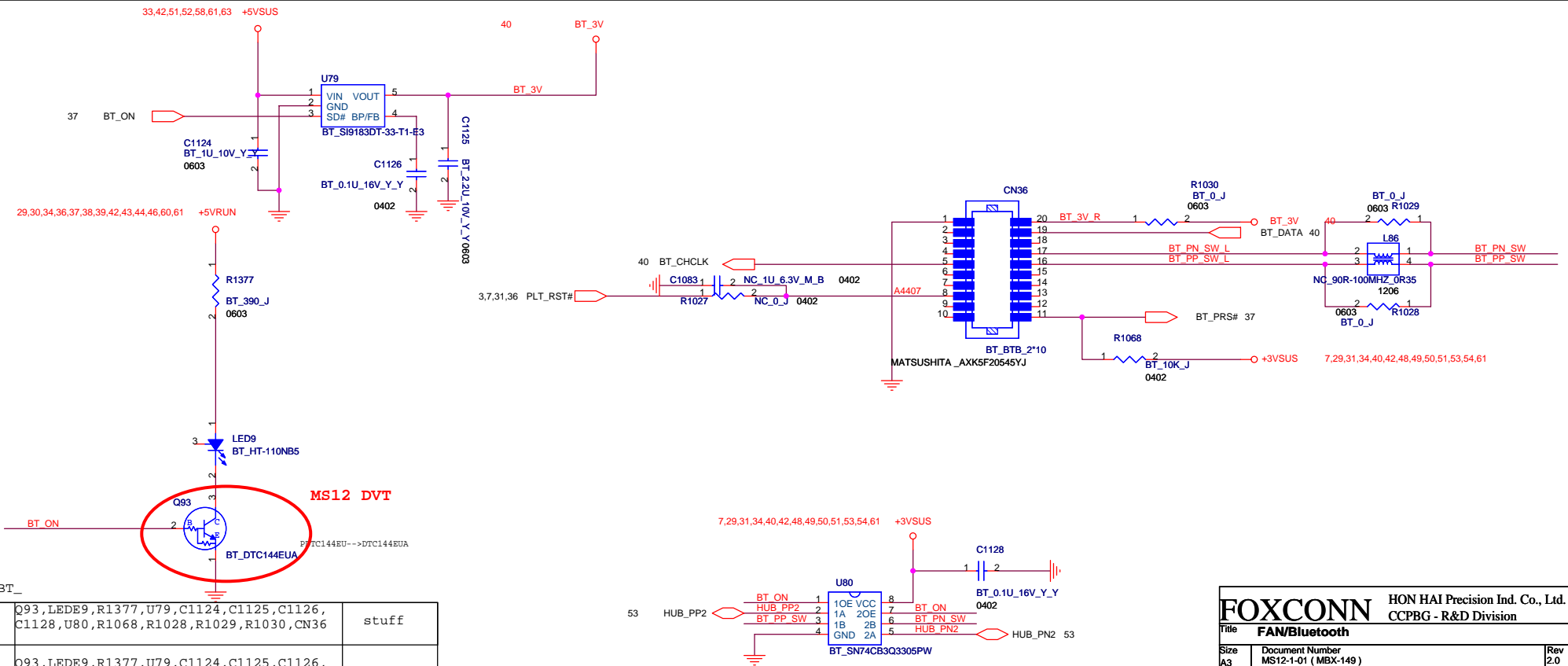
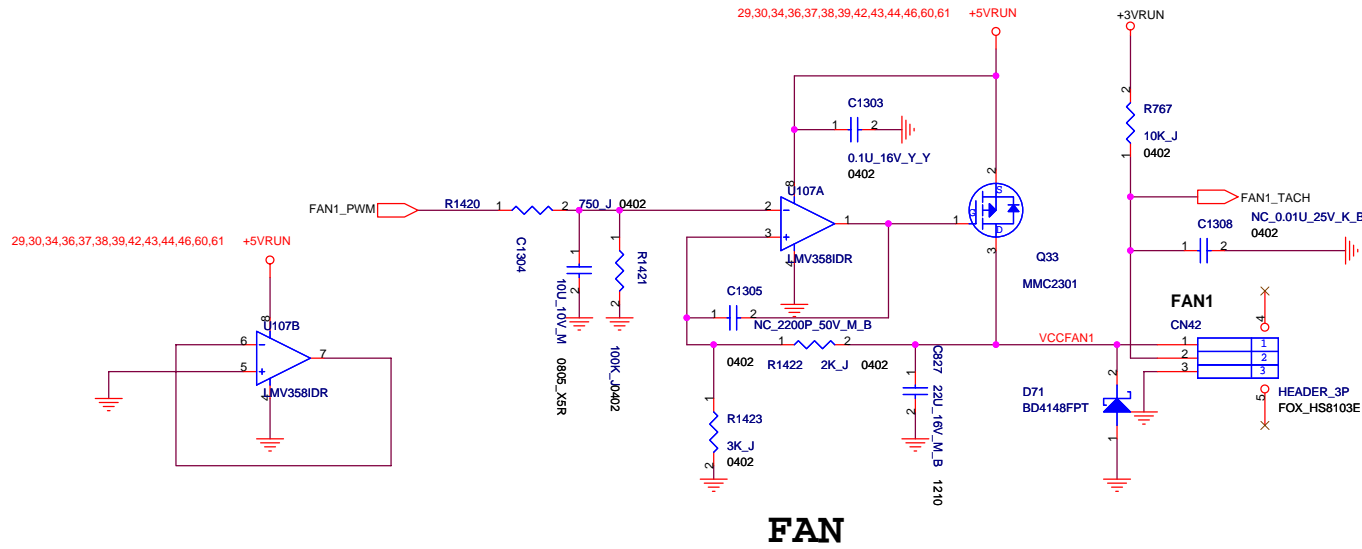
FLASH BIOS

JIG-120





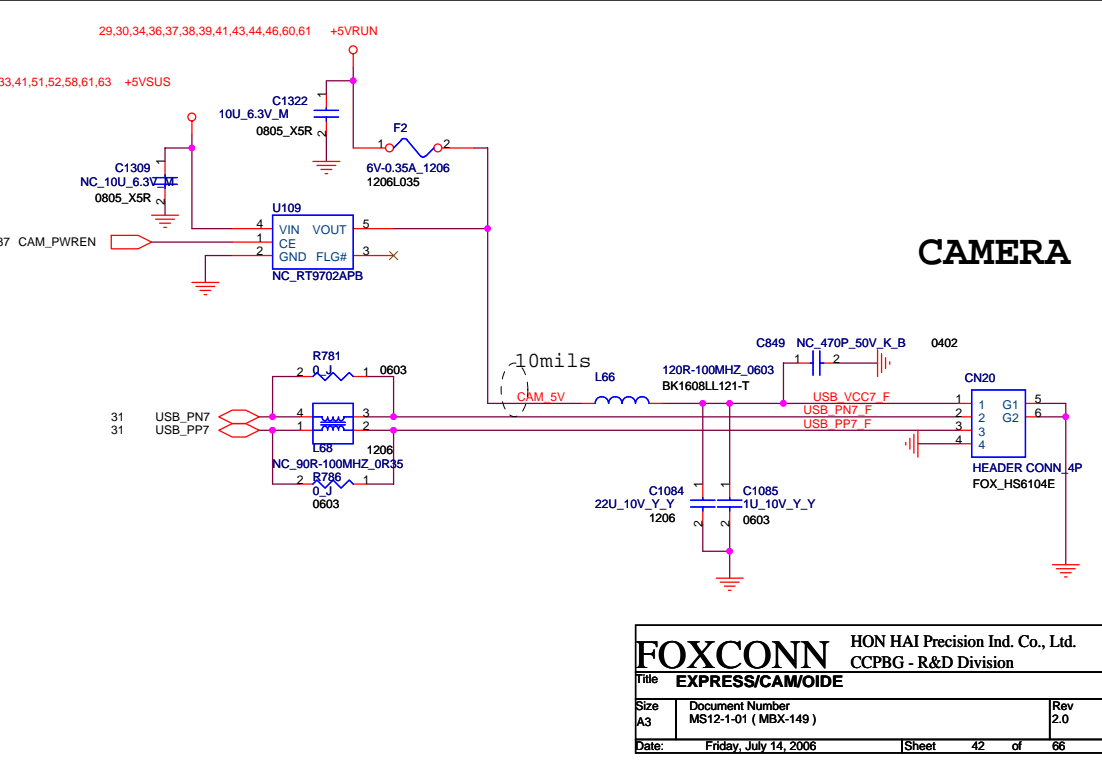
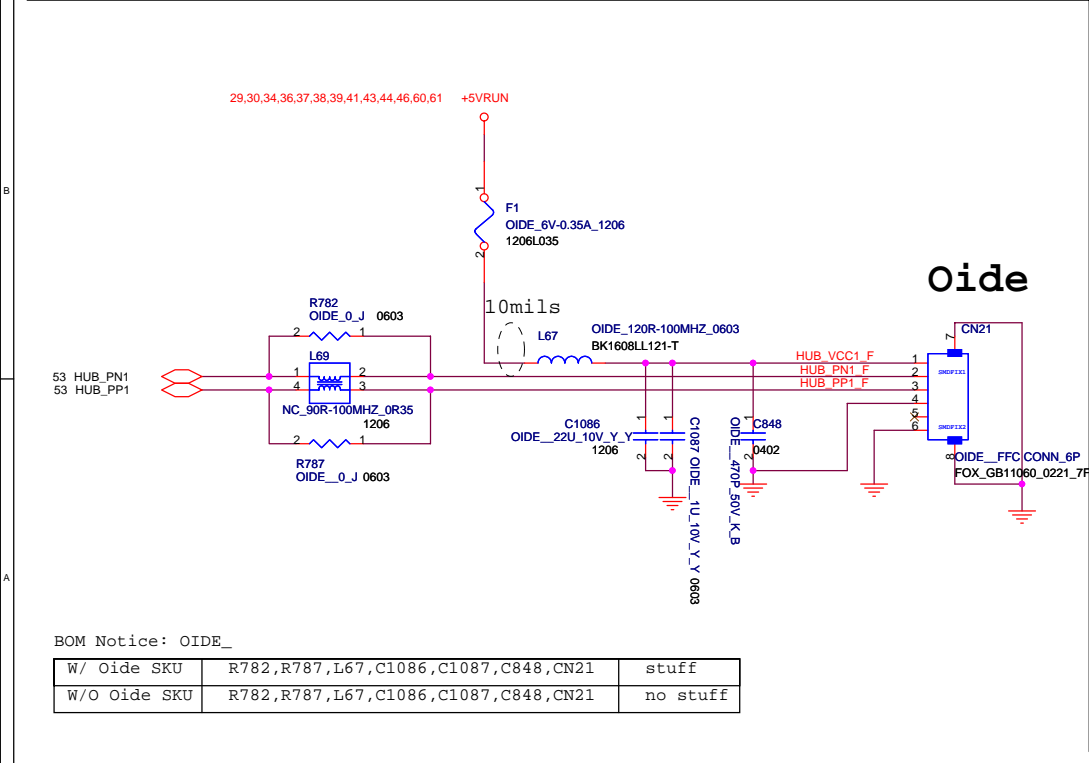
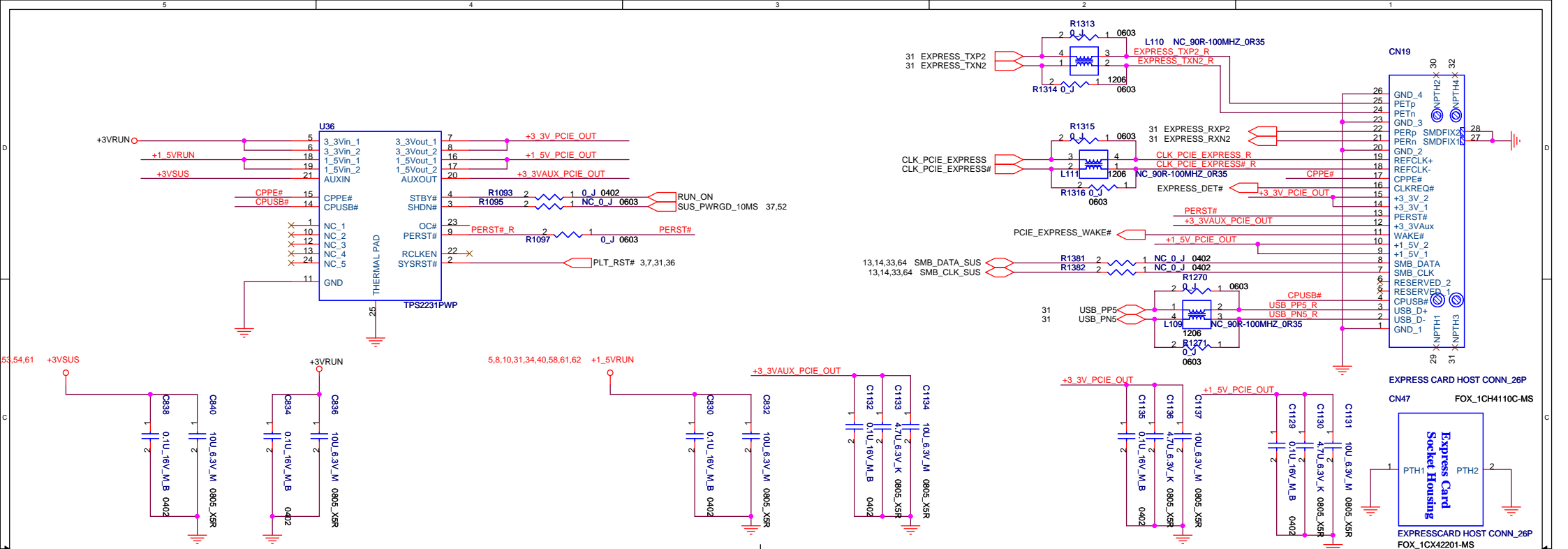




BOM Notice: BT_

W/ BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	stuff
W/O BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	no stuff

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
File		FAN/Bluetooth	
Size	Document Number	Rev	
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BOM Notice: OIDE_

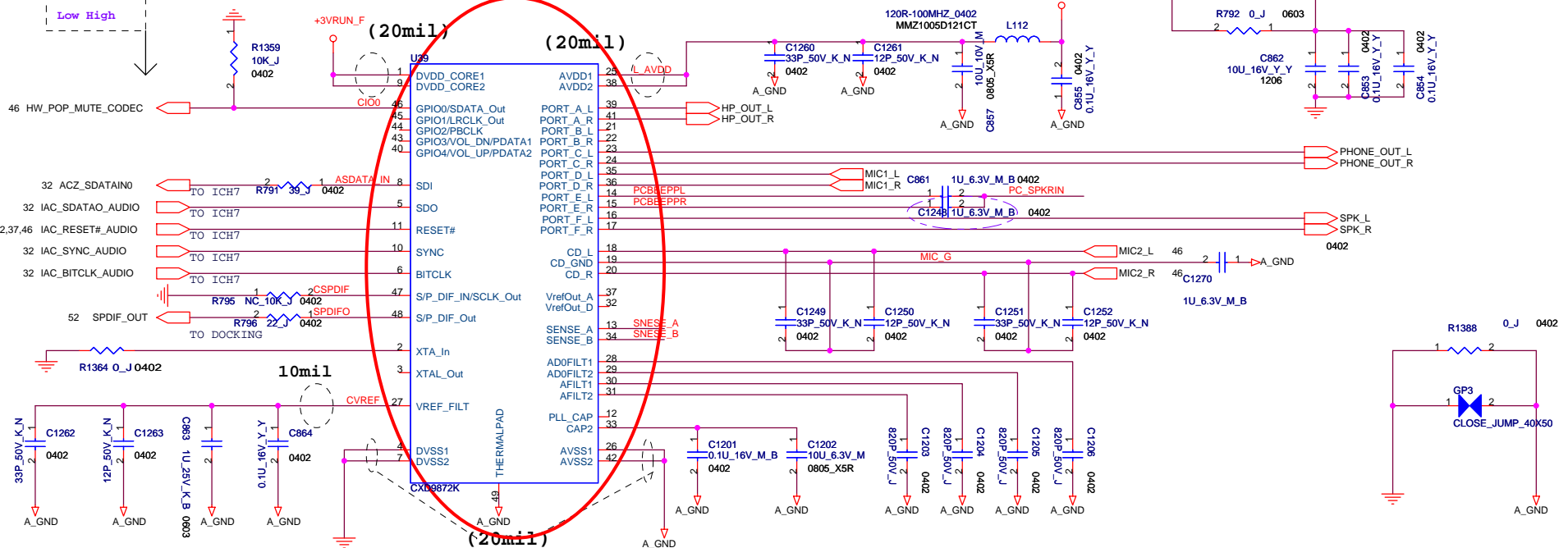
W/ Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	stuff
W/O Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	no stuff

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CCPBG - R&D Division

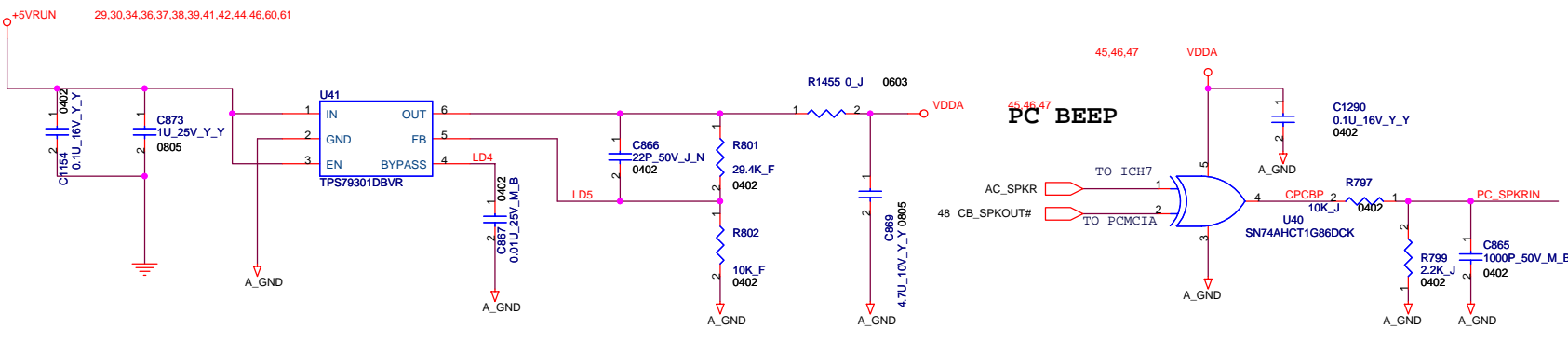
Title: **EXPRESS/CAM/OIDE**

Size A3	Document Number MS12-1-01 (MBX-149)	Rev 2.0
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If new codec part evaluate OK, pls change to ver:4th+



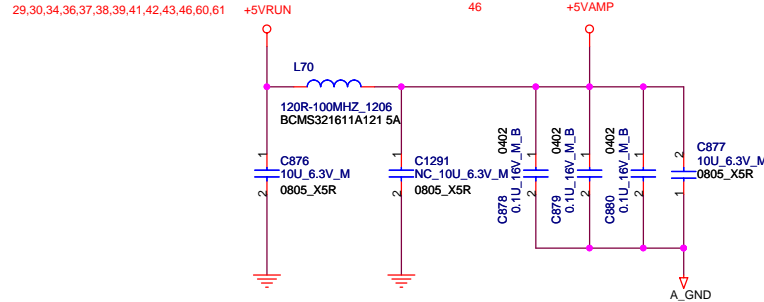
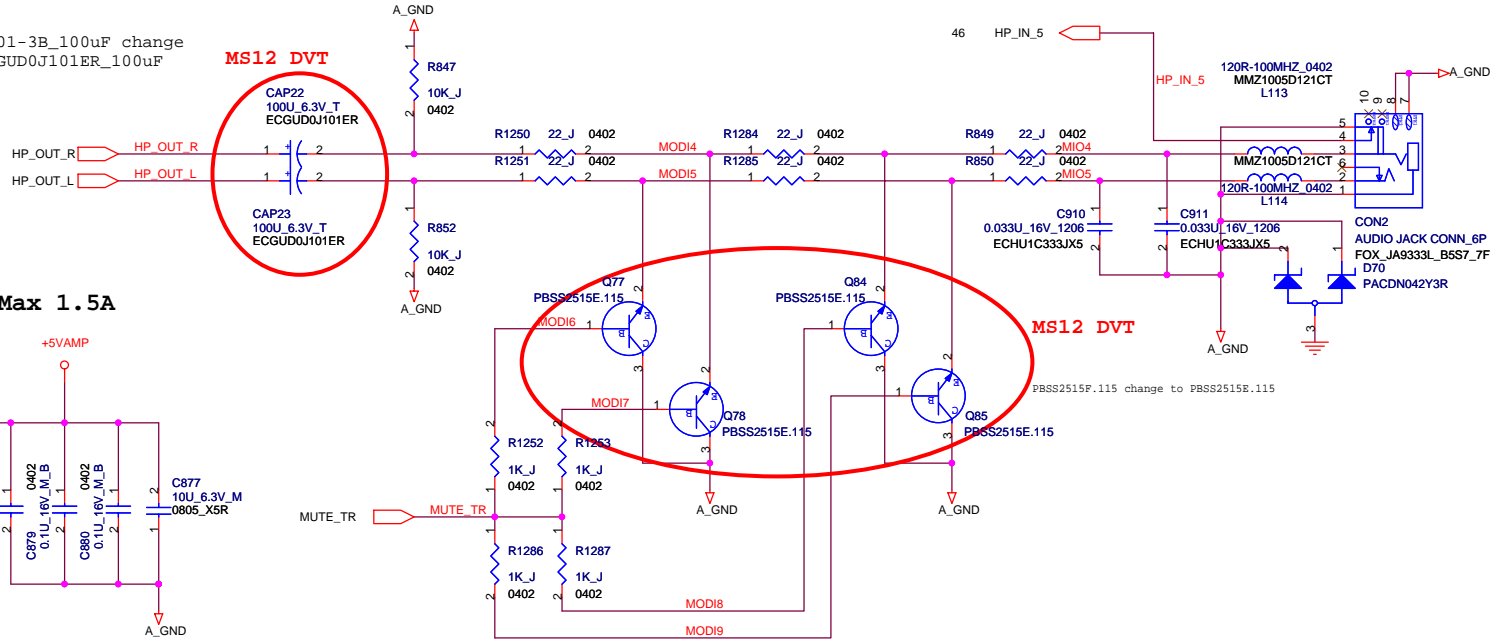
AUDIO POWER(Change to 4.75V/200mA)



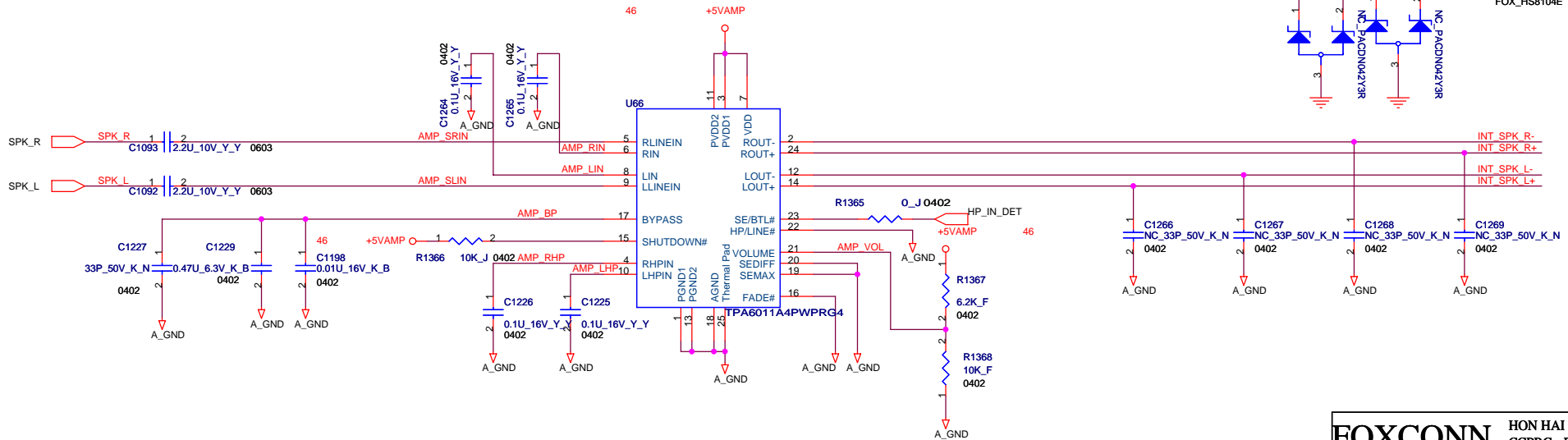
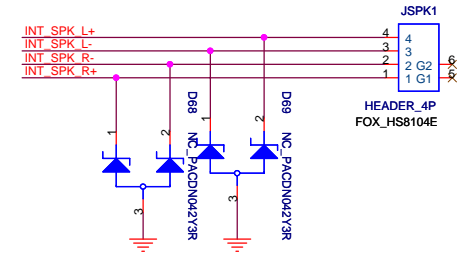
FOXCONN		
HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
File AUDIO(CODEC & POWER)		
Size	Document Number	Rev
A3	MS12-1-01 (MBX-149)	2.0
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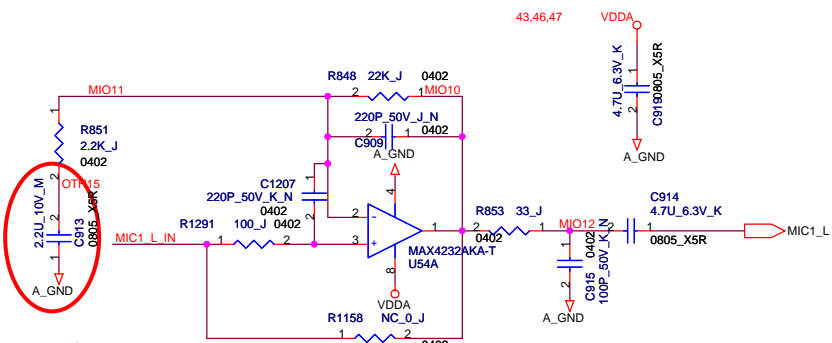
SE0J101-3B_100uF change to ECGUD0J101ER_100uF

MS12 DVT

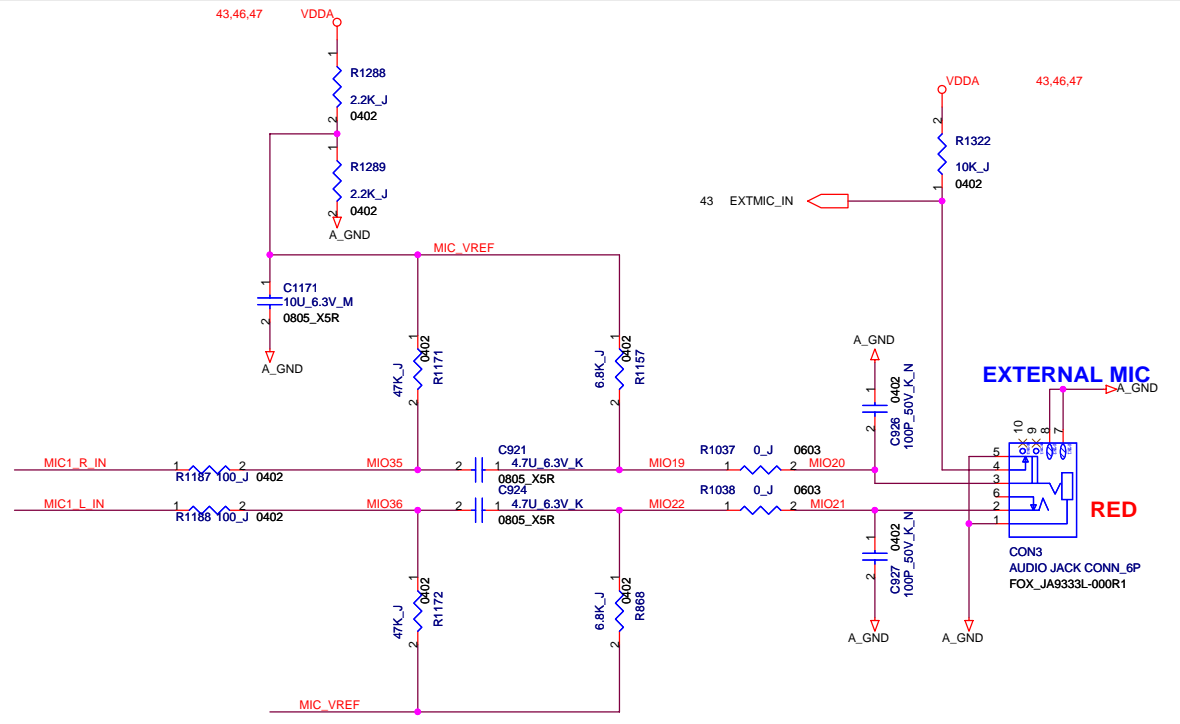
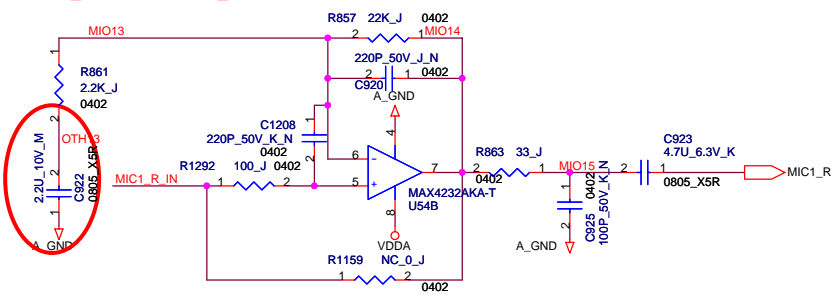


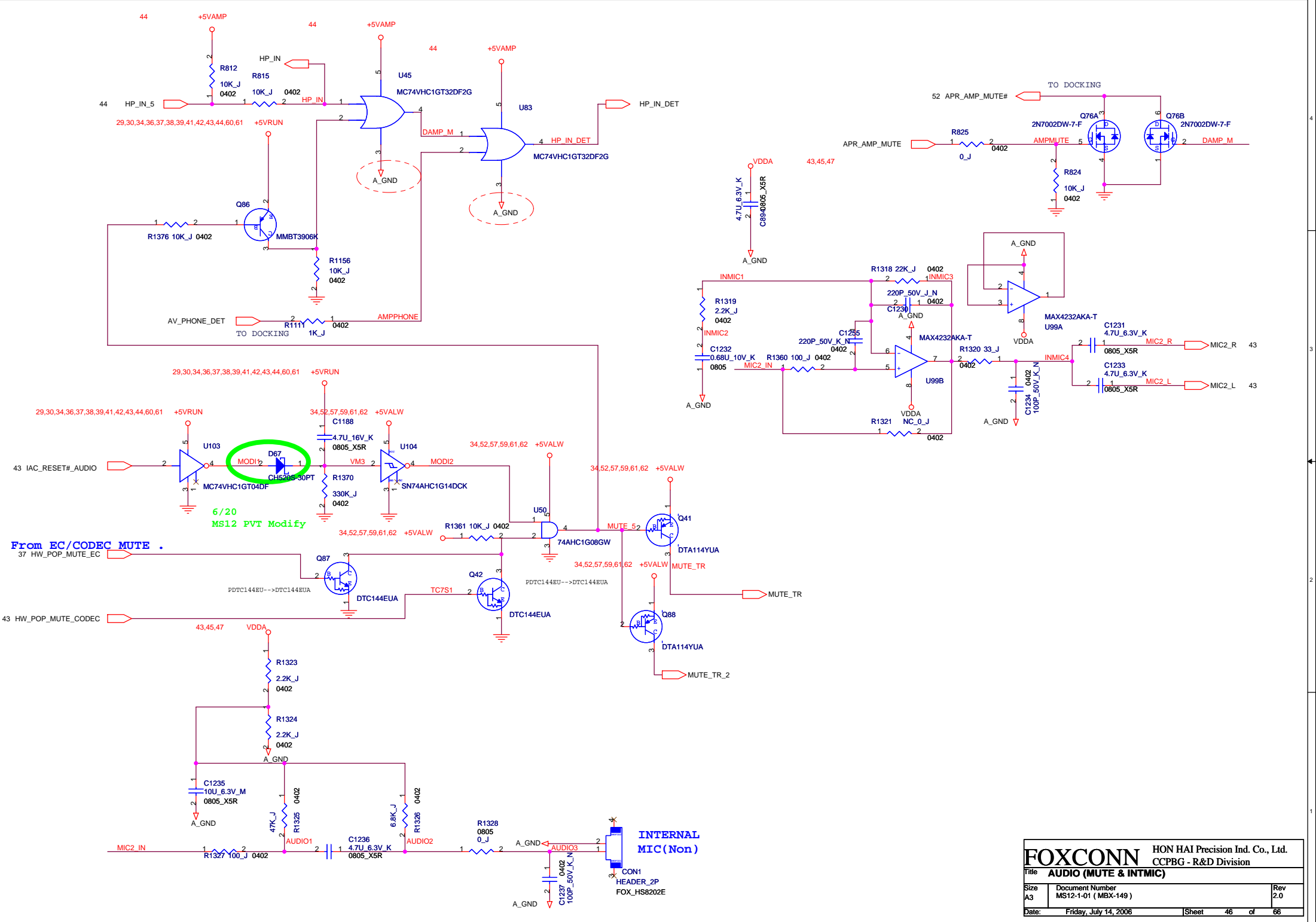
INTERNAL SPEAKER





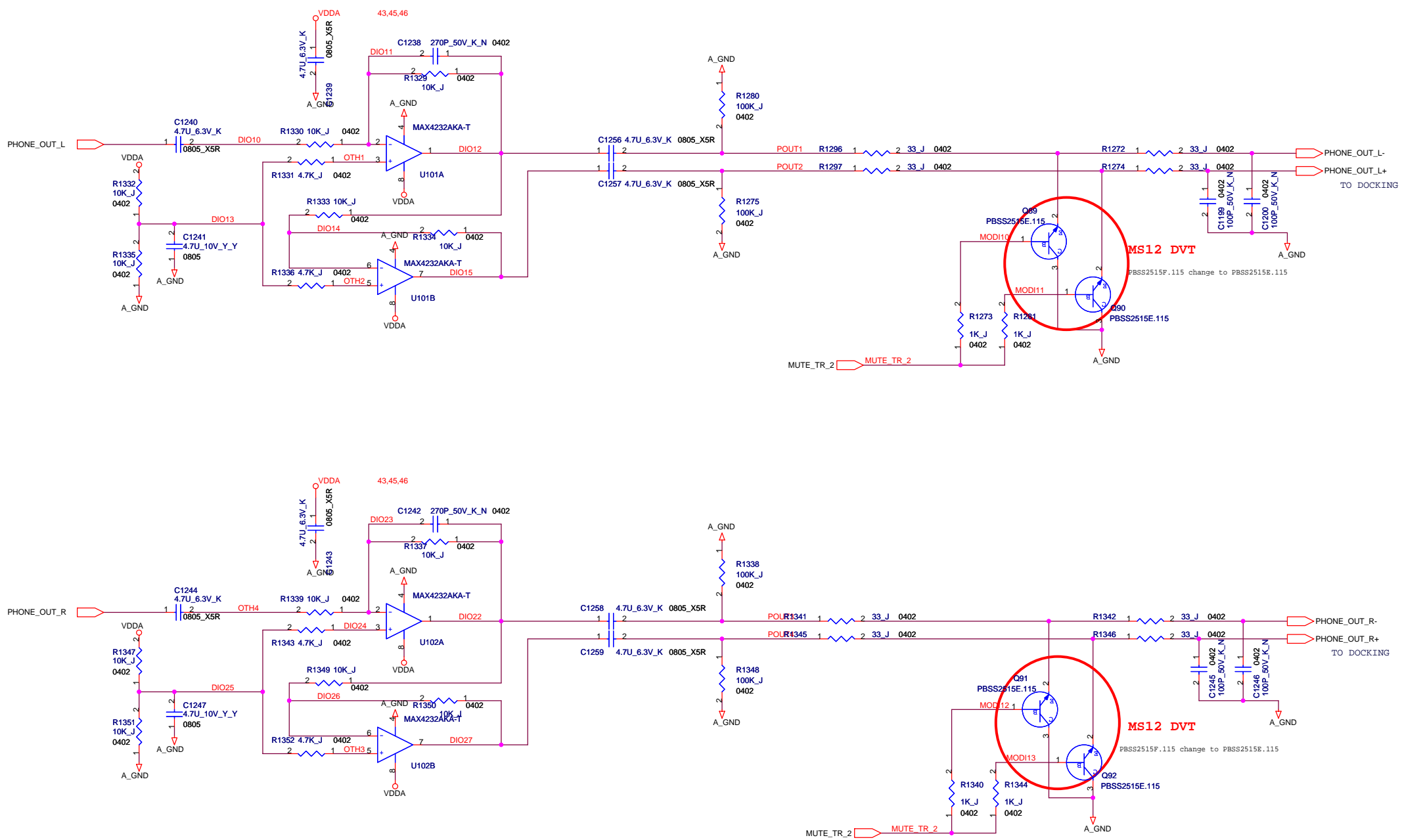
MS12 DVT
 2.2uF_16V ---> 2.2uF_10V

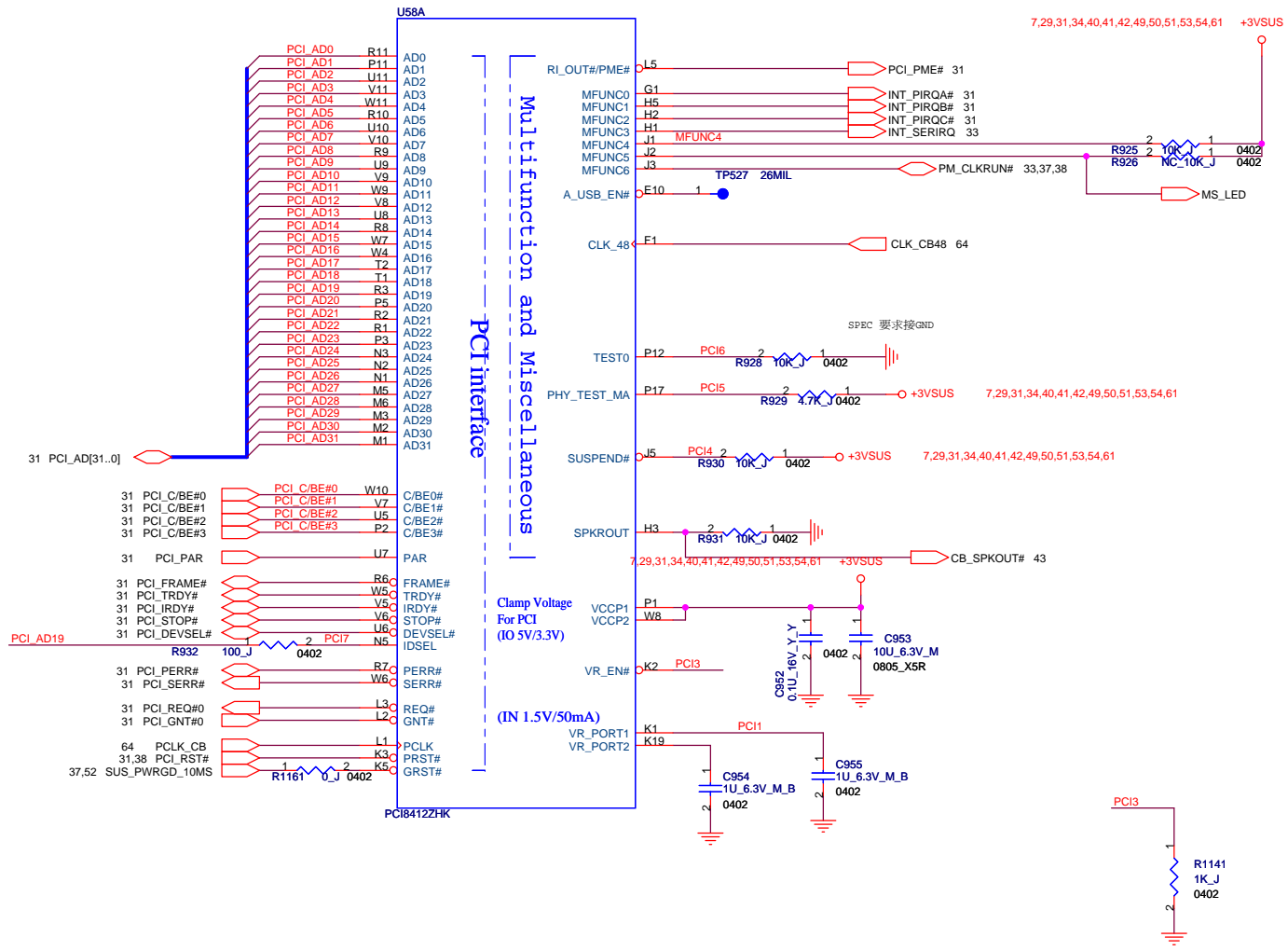




From EC/CODEC MUTE .

INTERNAL MIC (Non)





7.29,31,34,40,41,42,48,50,51,53,54,61 +3VSUS
 This array must be placed close to VDDPLL (Pin U19) They must be tied to a low-impedance GND.

This array must be placed close to AVDD (Pin P13,P14,U15) They must be tied to a low-impedance GND.

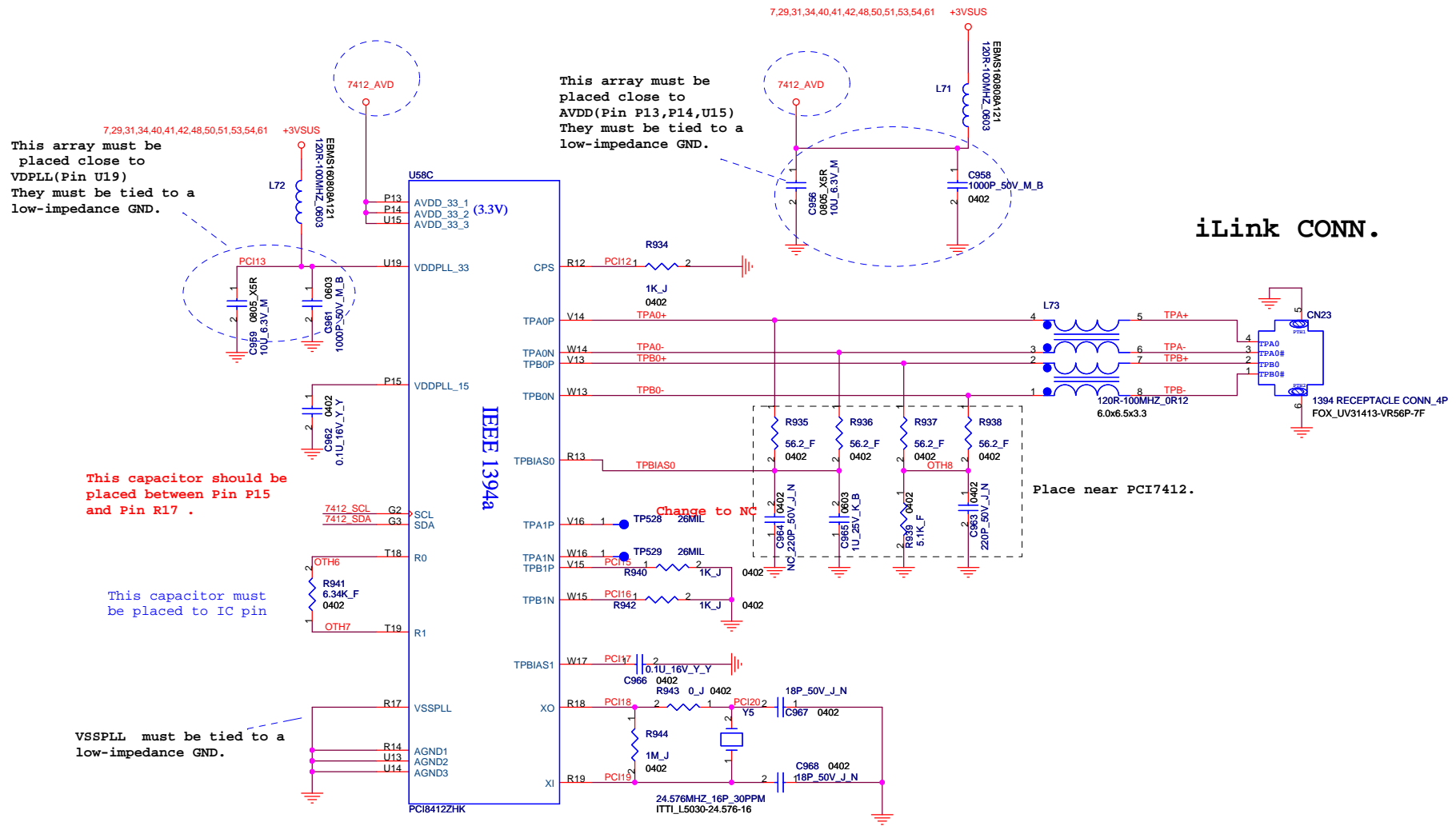
This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

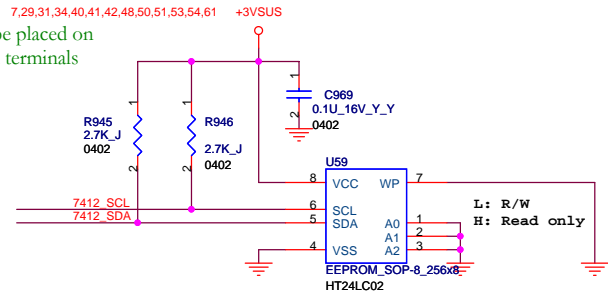
VSSPLL must be tied to a low-impedance GND.

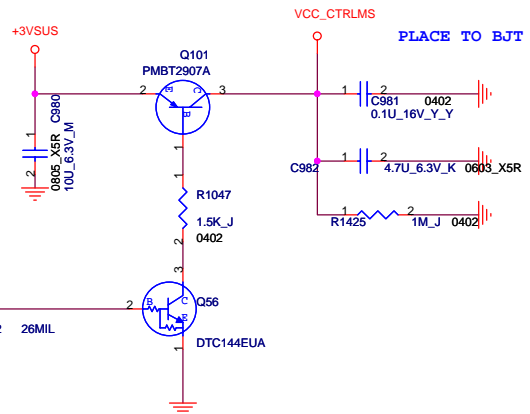
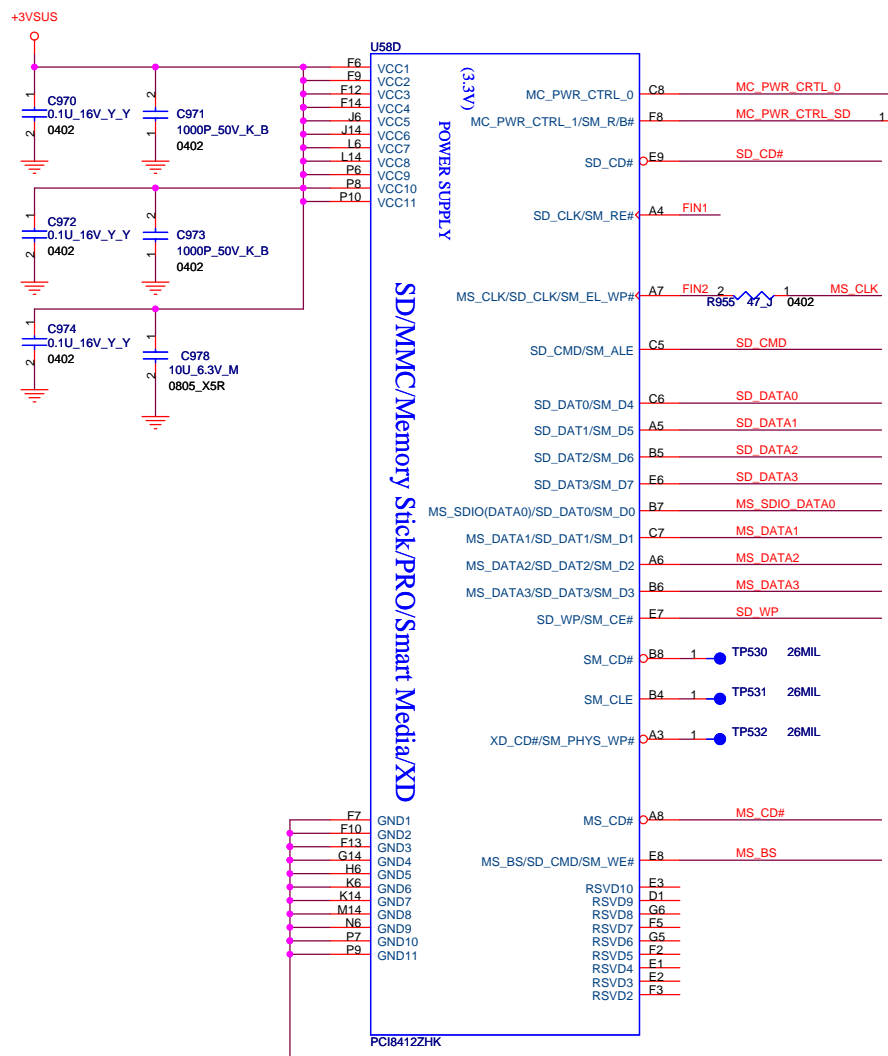
iLink CONN.

Place near PCI7412.

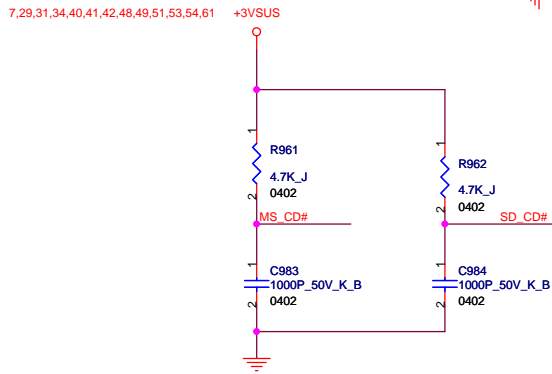
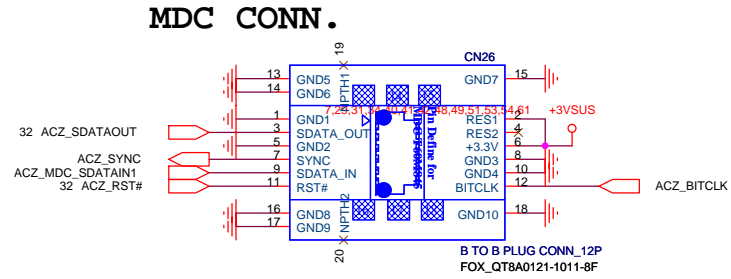
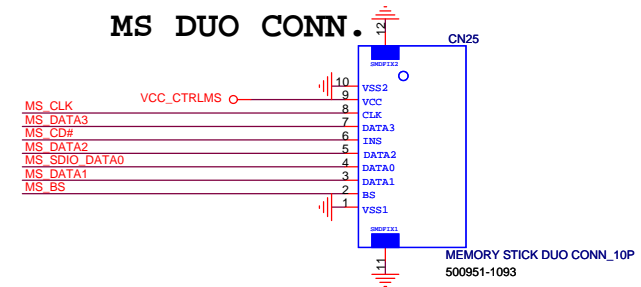


Resistors should be placed on the SCL and SDA terminals

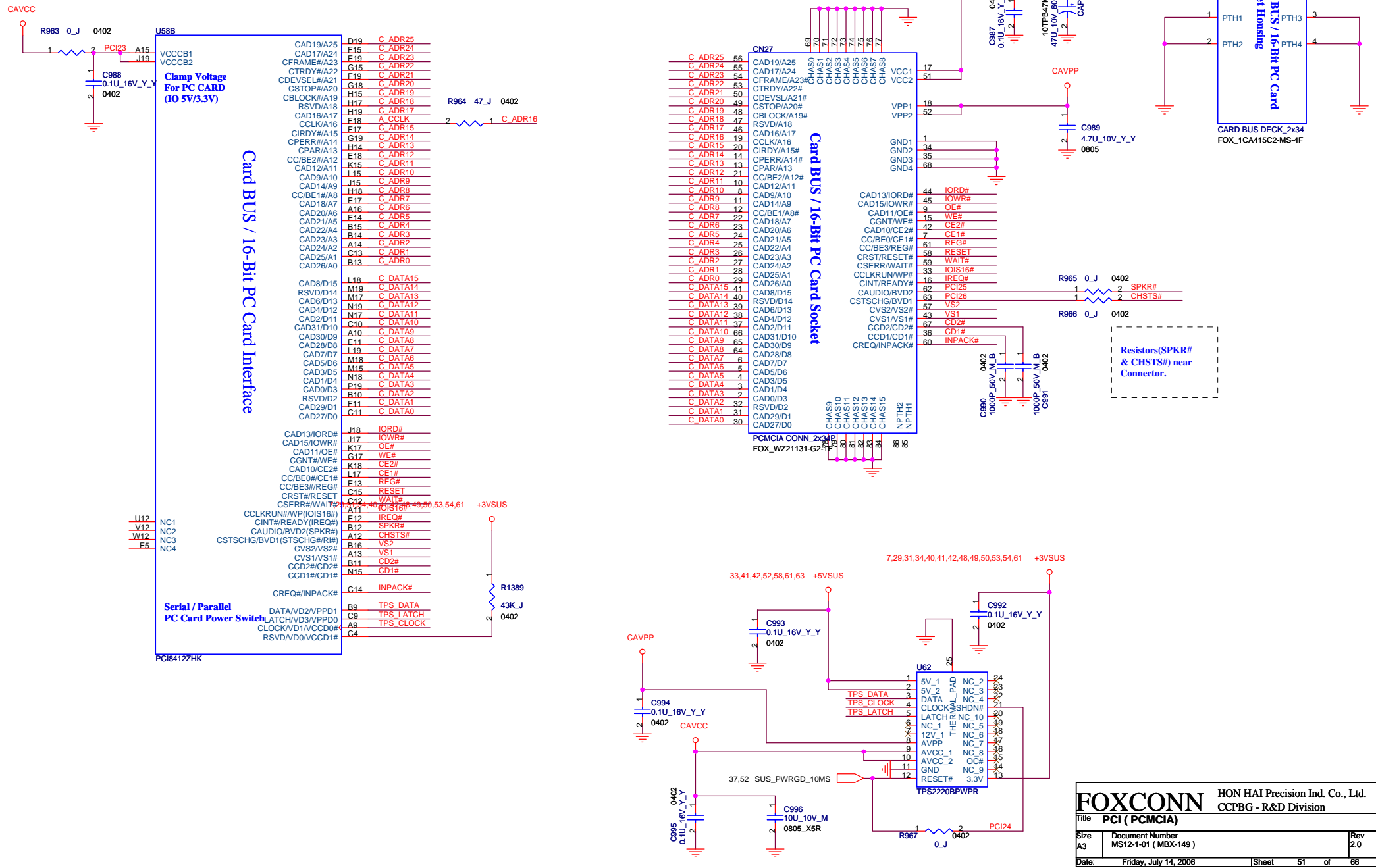




These capacitors should be closed to socket pin

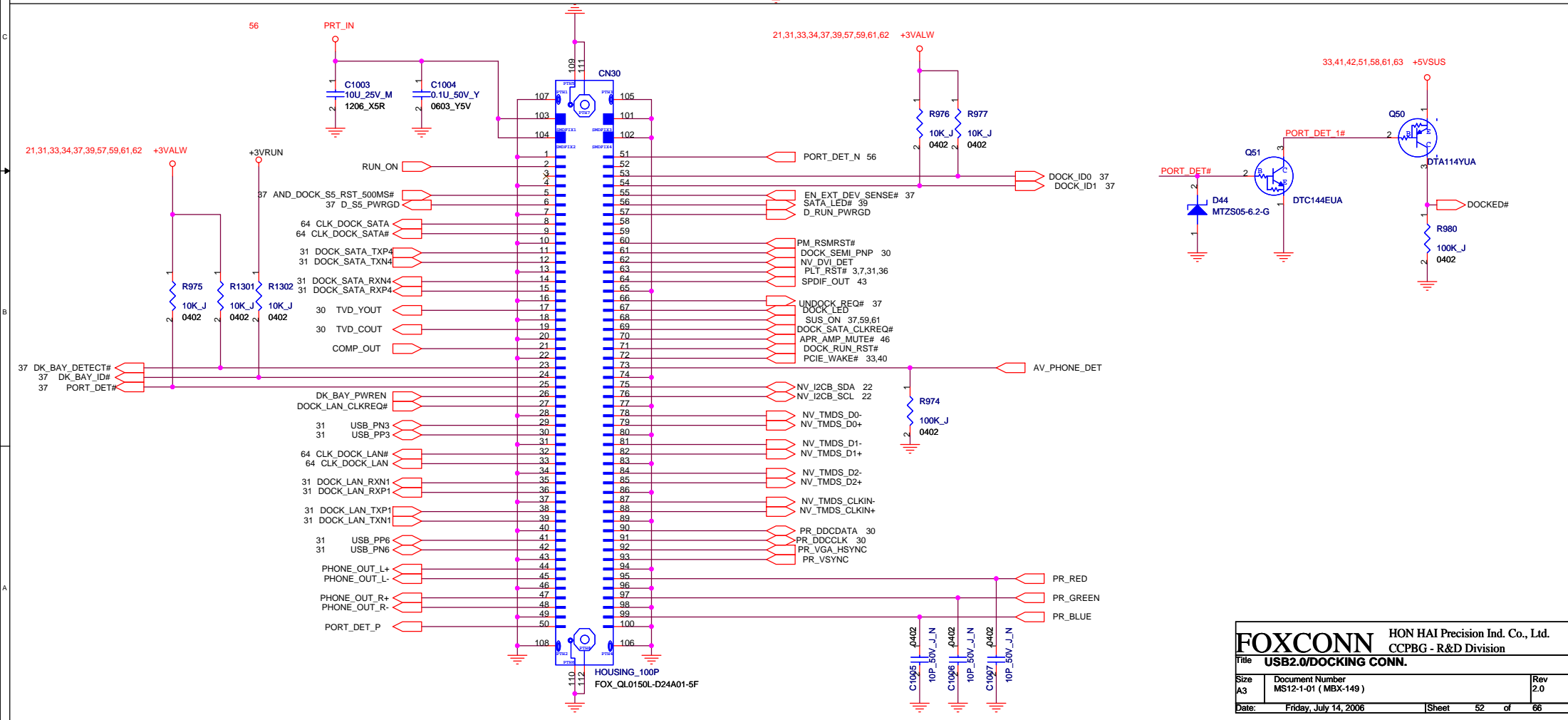
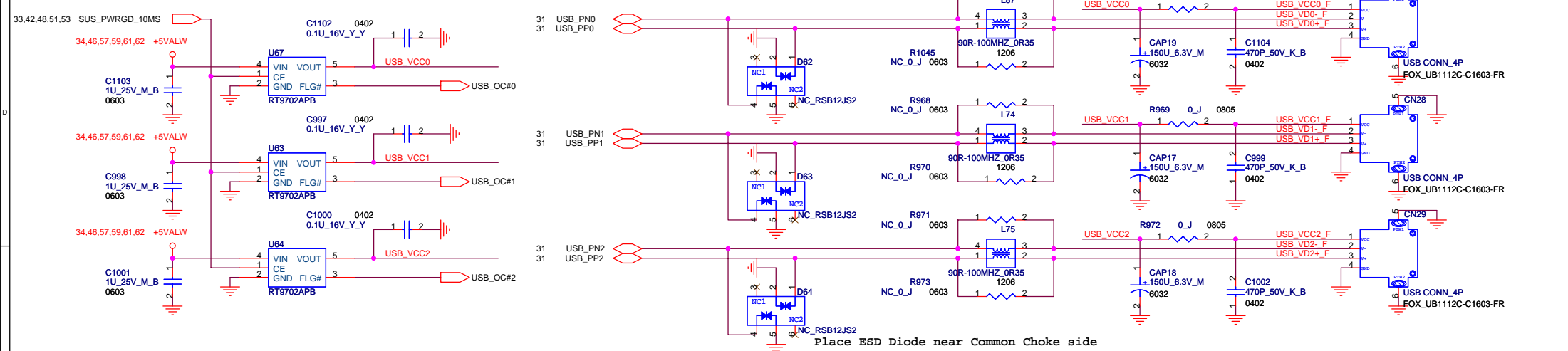


PCMCIA CONN.



FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title PCI (PCMCIA)		
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USB CONN X 3



BOM notice:

	R1243	R1244	R1247	R1248	R1459	R1460
BT + OIDE SKU	NC	NC	NC	NC	NC	NC
BT SKU	0 ohm	0 ohm	0 ohm	0 ohm	NC	NC
OIDE SKU	0 ohm	0 ohm	NC	NC	0 ohm	0 ohm

BOM notice:

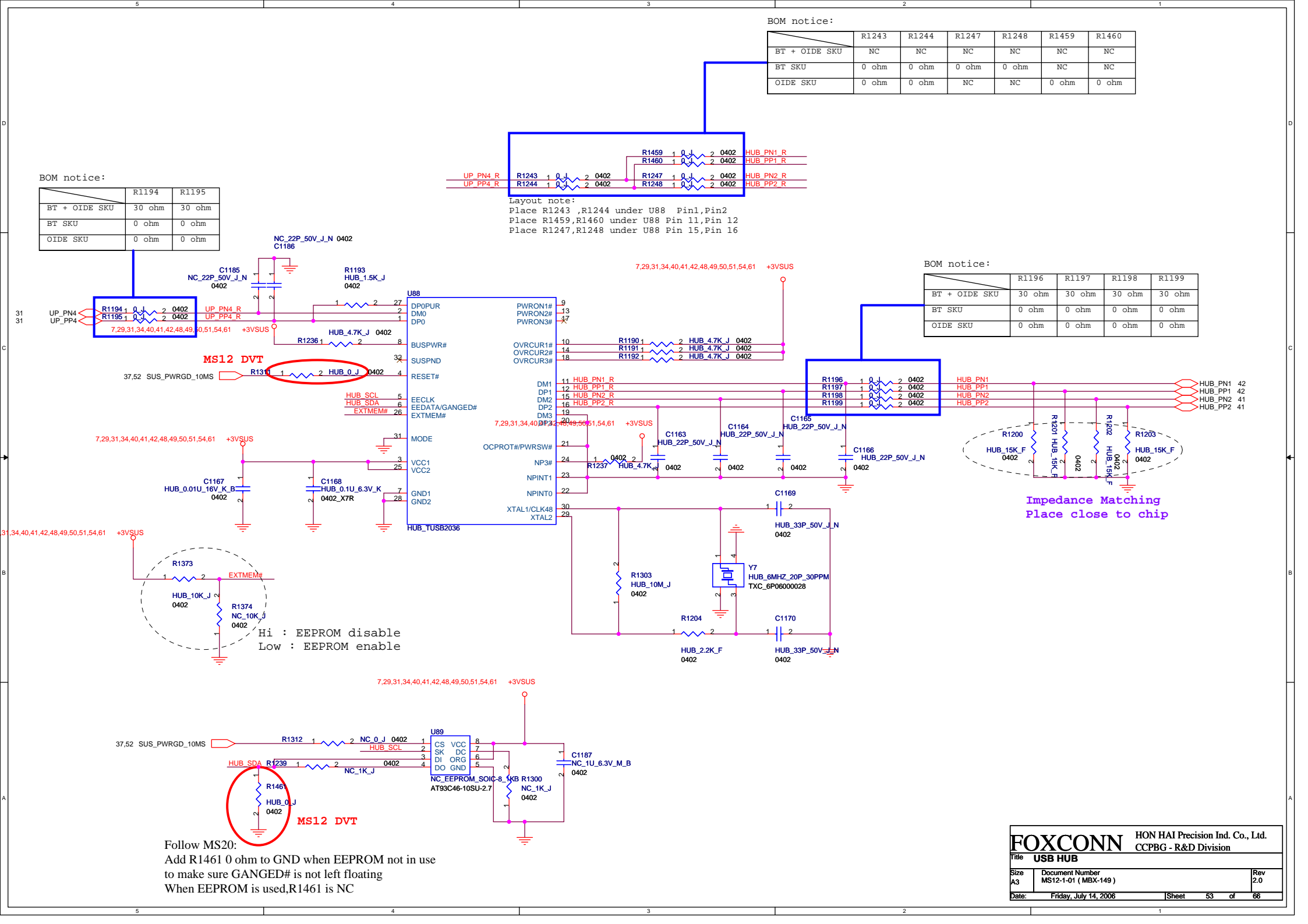
	R1194	R1195
BT + OIDE SKU	30 ohm	30 ohm
BT SKU	0 ohm	0 ohm
OIDE SKU	0 ohm	0 ohm

Layout note:

Place R1243 ,R1244 under U88 Pin1,Pin2
 Place R1459,R1460 under U88 Pin 11,Pin 12
 Place R1247,R1248 under U88 Pin 15,Pin 16

BOM notice:

	R1196	R1197	R1198	R1199
BT + OIDE SKU	30 ohm	30 ohm	30 ohm	30 ohm
BT SKU	0 ohm	0 ohm	0 ohm	0 ohm
OIDE SKU	0 ohm	0 ohm	0 ohm	0 ohm



Hi : EEPROM disable
 Low : EEPROM enable

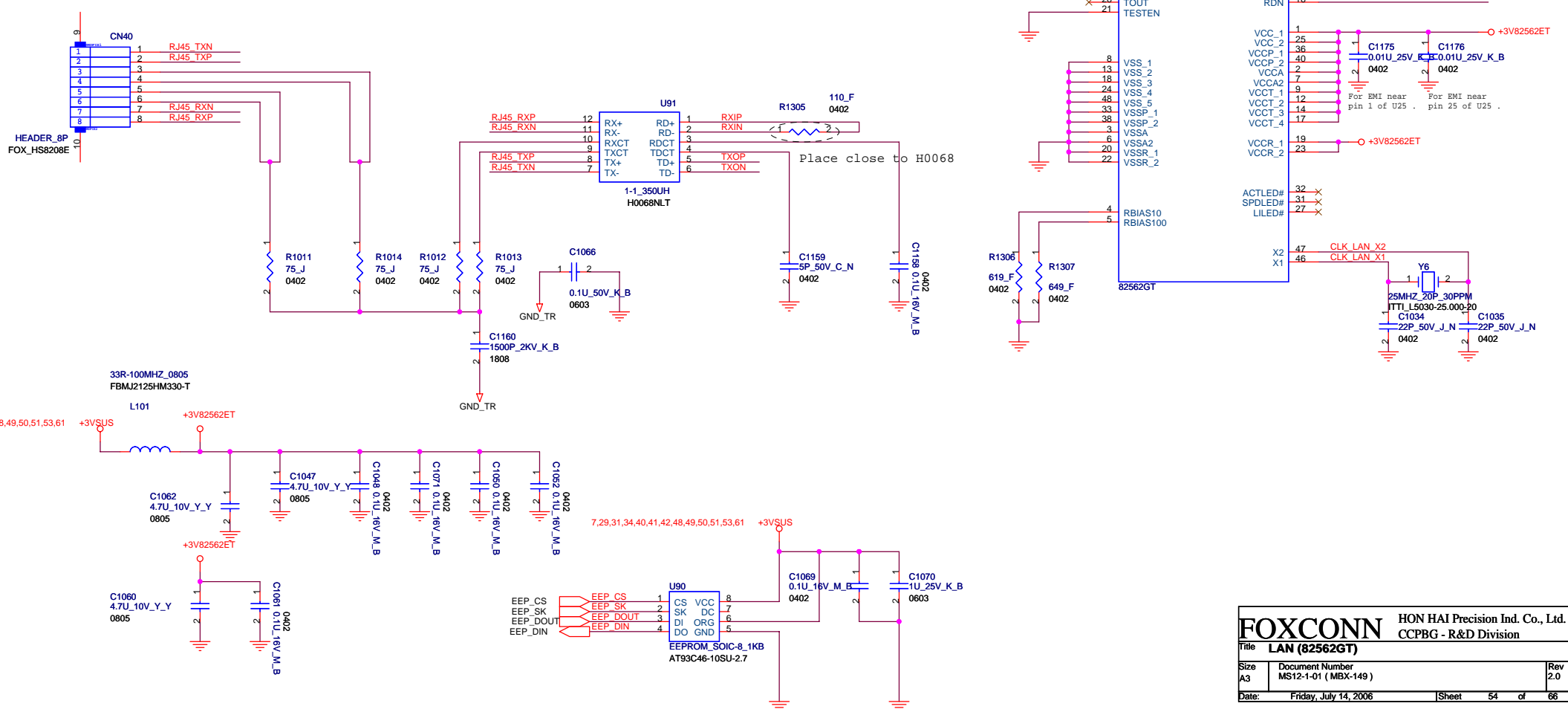
Impedance Matching
 Place close to chip

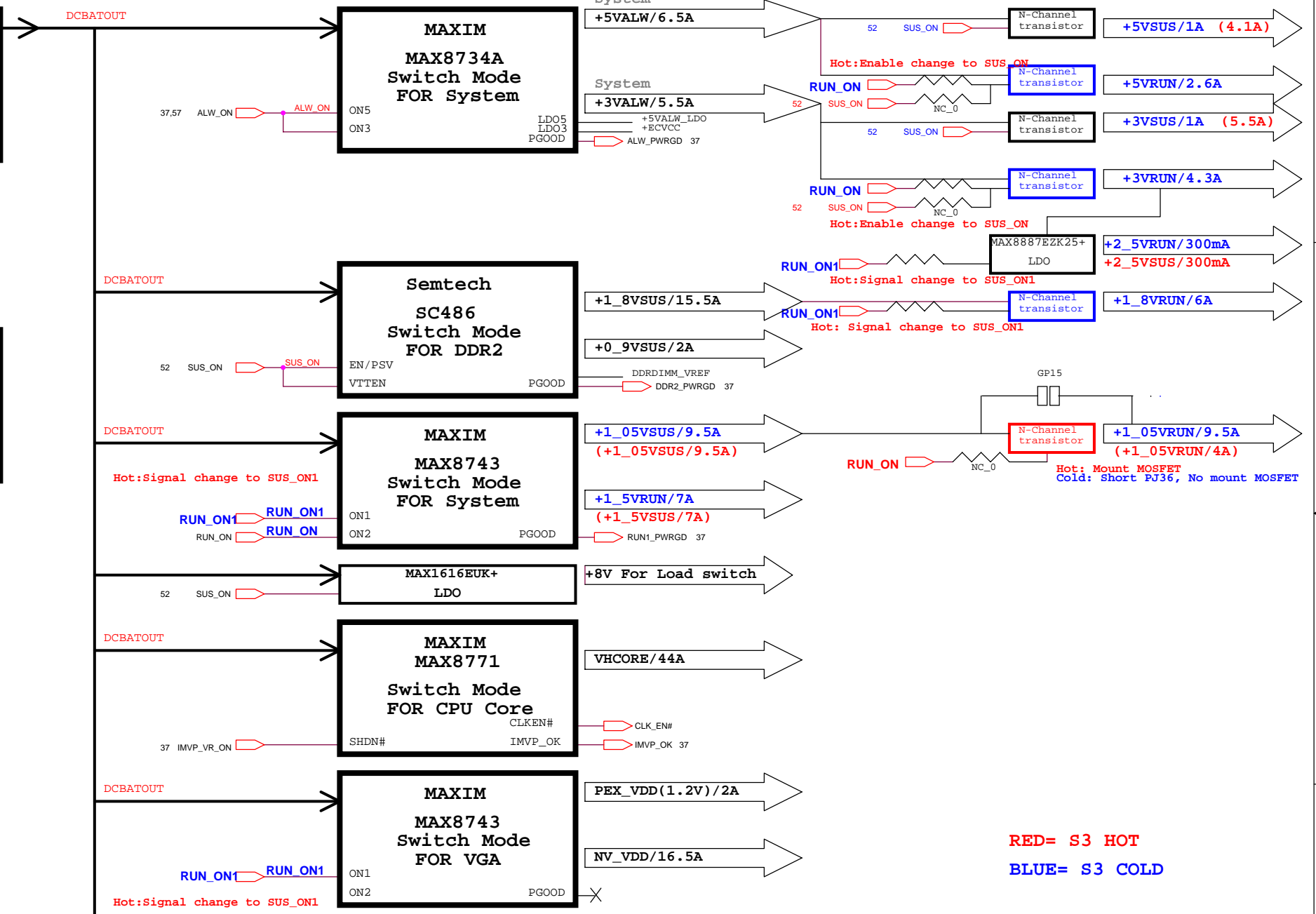
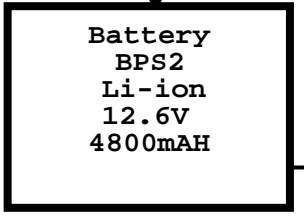
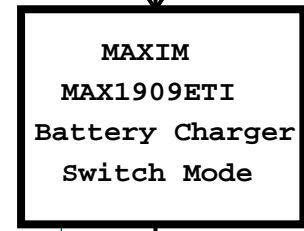
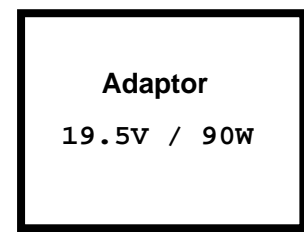
Follow MS20:
 Add R1461 0 ohm to GND when EEPROM not in use
 to make sure GANGED# is not left floating
 When EEPROM is used,R1461 is NC

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 CCPBG - R&D Division

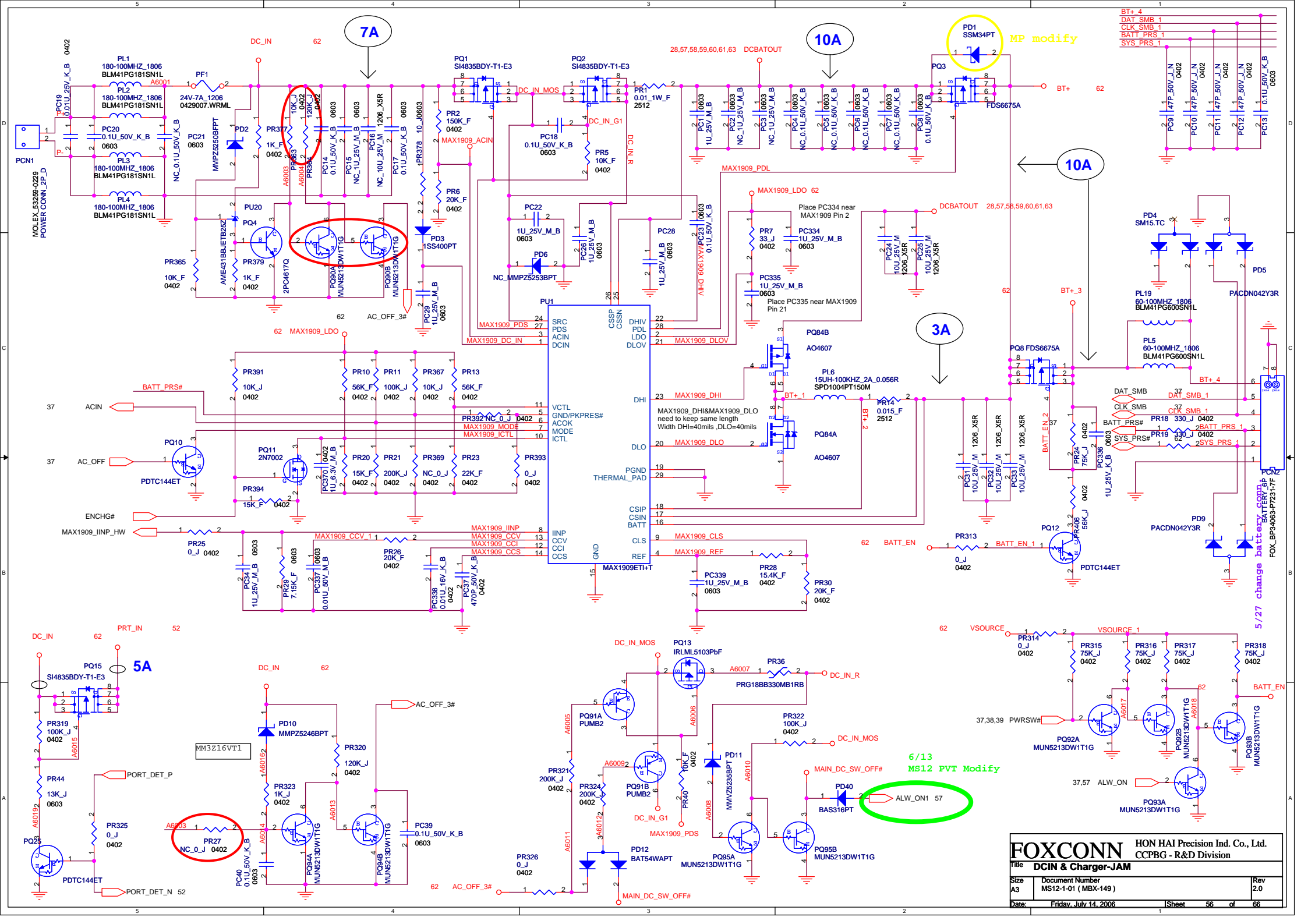
Title **USB HUB**

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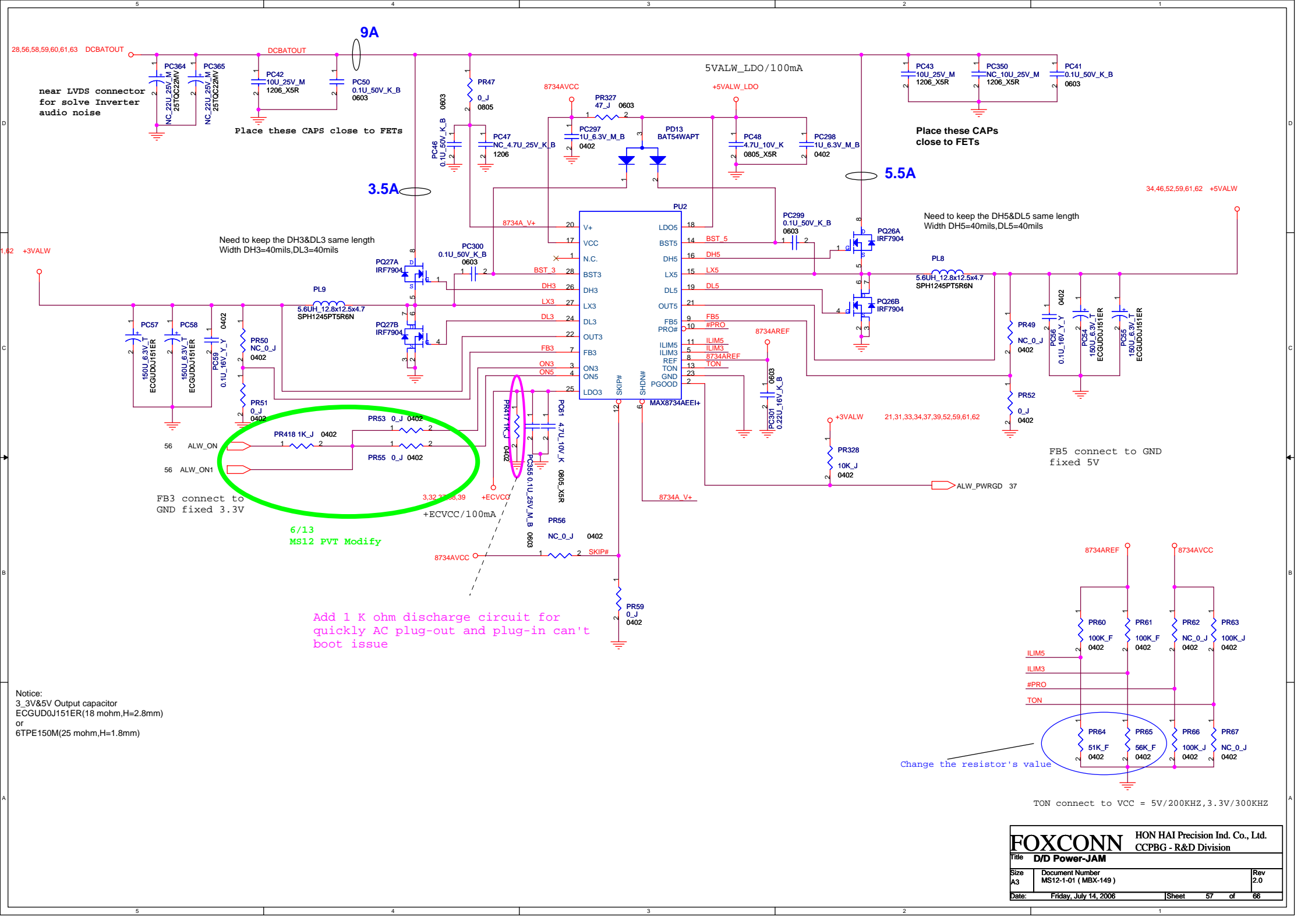




RED= S3 HOT
BLUE= S3 COLD



FOXCONN HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title DCIN & Charger-JAM	
Size A3	Document Number MS12-1-01 (MBX-149)
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near LVDS connector for solve Inverter audio noise

Place these CAPS close to FETs

Place these CAPS close to FETs

Need to keep the DH3&DL3 same length Width DH3=40mils,DL3=40mils

Need to keep the DH5&DL5 same length Width DH5=40mils,DL5=40mils

FB3 connect to GND fixed 3.3V

FB5 connect to GND fixed 5V

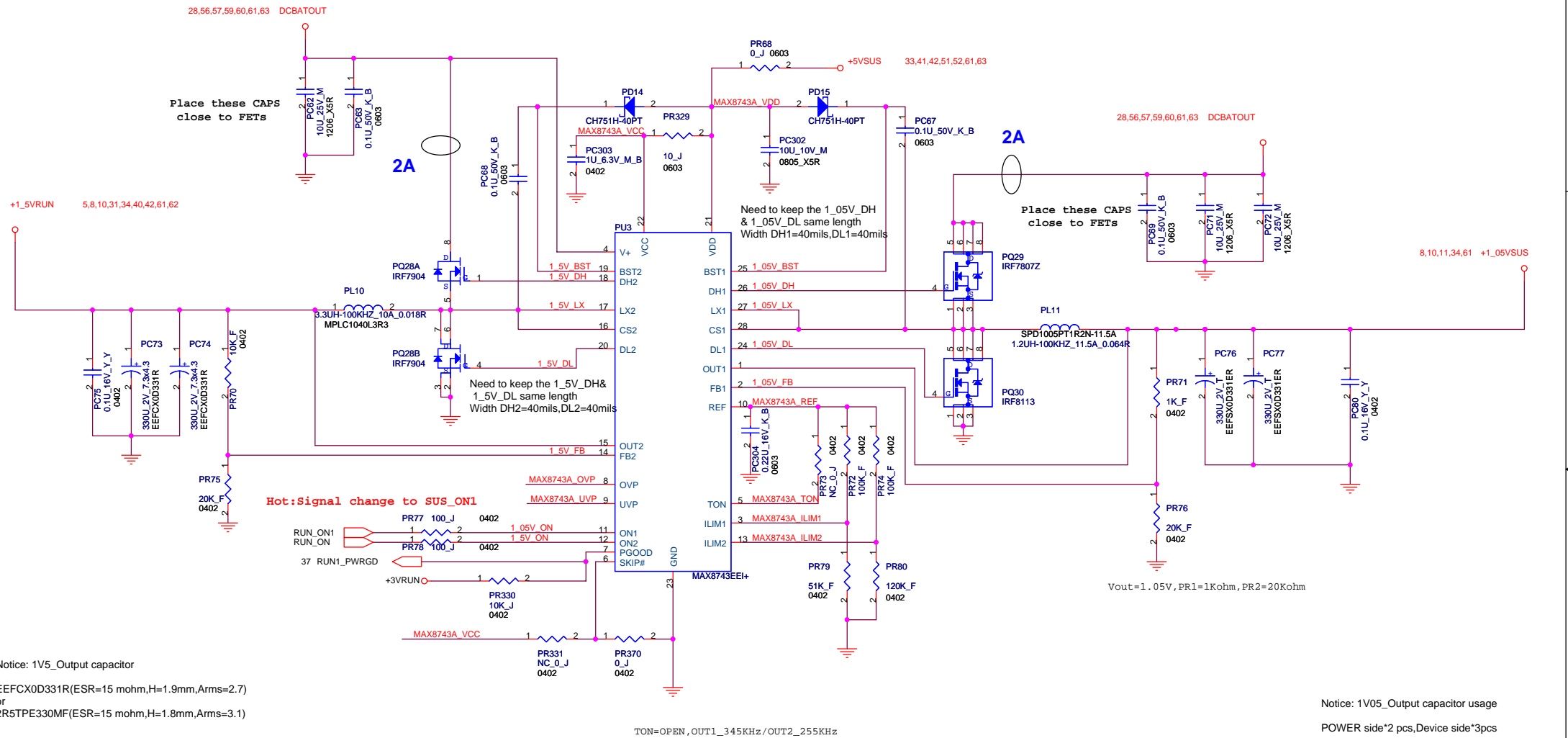
Add 1 K ohm discharge circuit for quickly AC plug-out and plug-in can't boot issue

Change the resistor's value

TON connect to VCC = 5V/200KHZ, 3.3V/300KHZ

FOXCONN HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
File D/D Power-JAM	
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Notice:
3_3V&5V Output capacitor
ECGUD0J151ER(18 mohm,H=2.8mm)
or
6TPE150M(25 mohm,H=1.8mm)



Place these CAPS close to FETs

Place these CAPS close to FETs

Hot:Signal change to SUS_ON1

Need to keep the 1.05V_DH & 1.05V_DL same length Width DH1=40mils, DL1=40mils

Need to keep the 1.5V_DH & 1.5V_DL same length Width DH2=40mils, DL2=40mils

TON=OPEN, OUT1_345KHz / OUT2_255KHz

Vout=1.05V, PR1=1Kohm, PR2=20Kohm

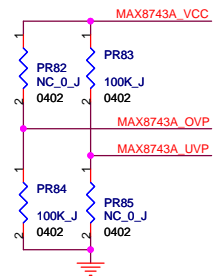
Notice: 1V5_Output capacitor

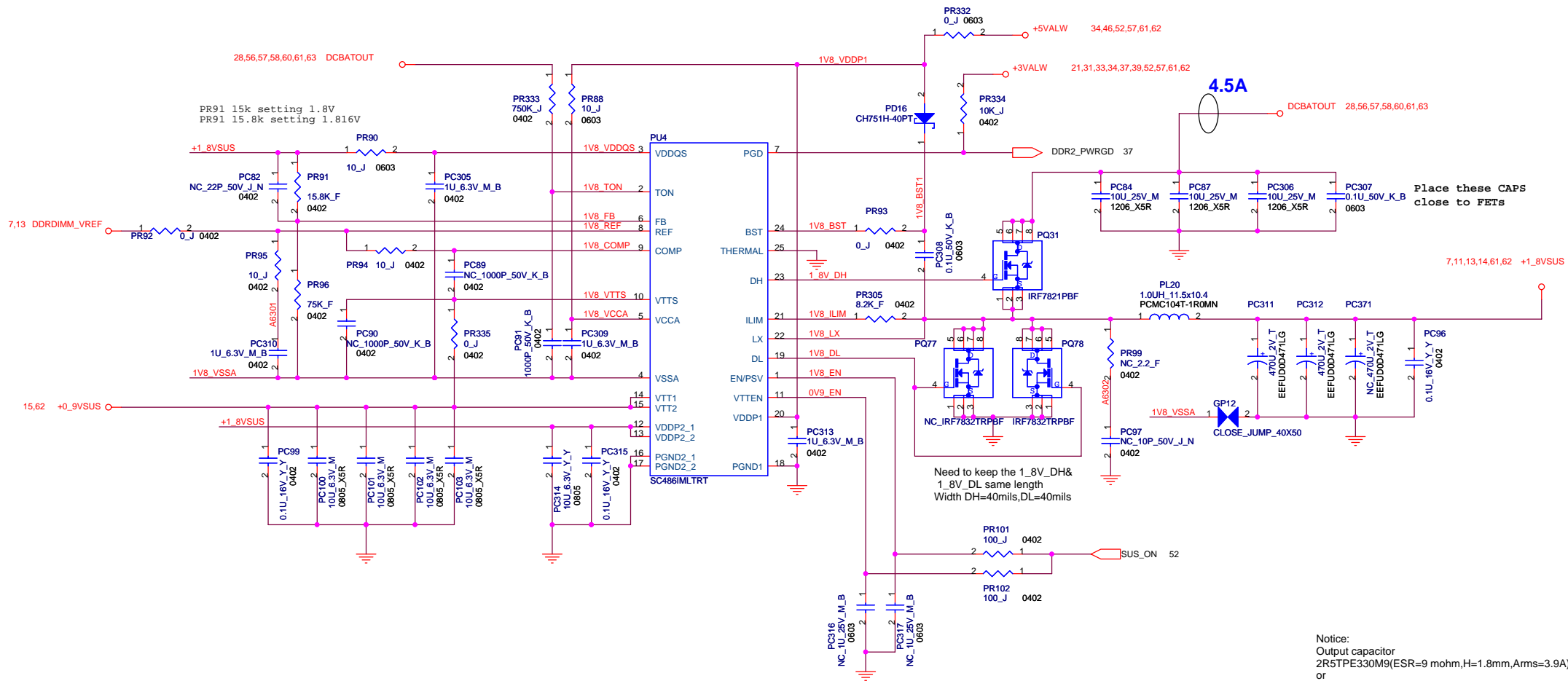
EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7)
or
2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1)

Notice: 1V05_Output capacitor usage

POWER side*2 pcs, Device side*3pcs

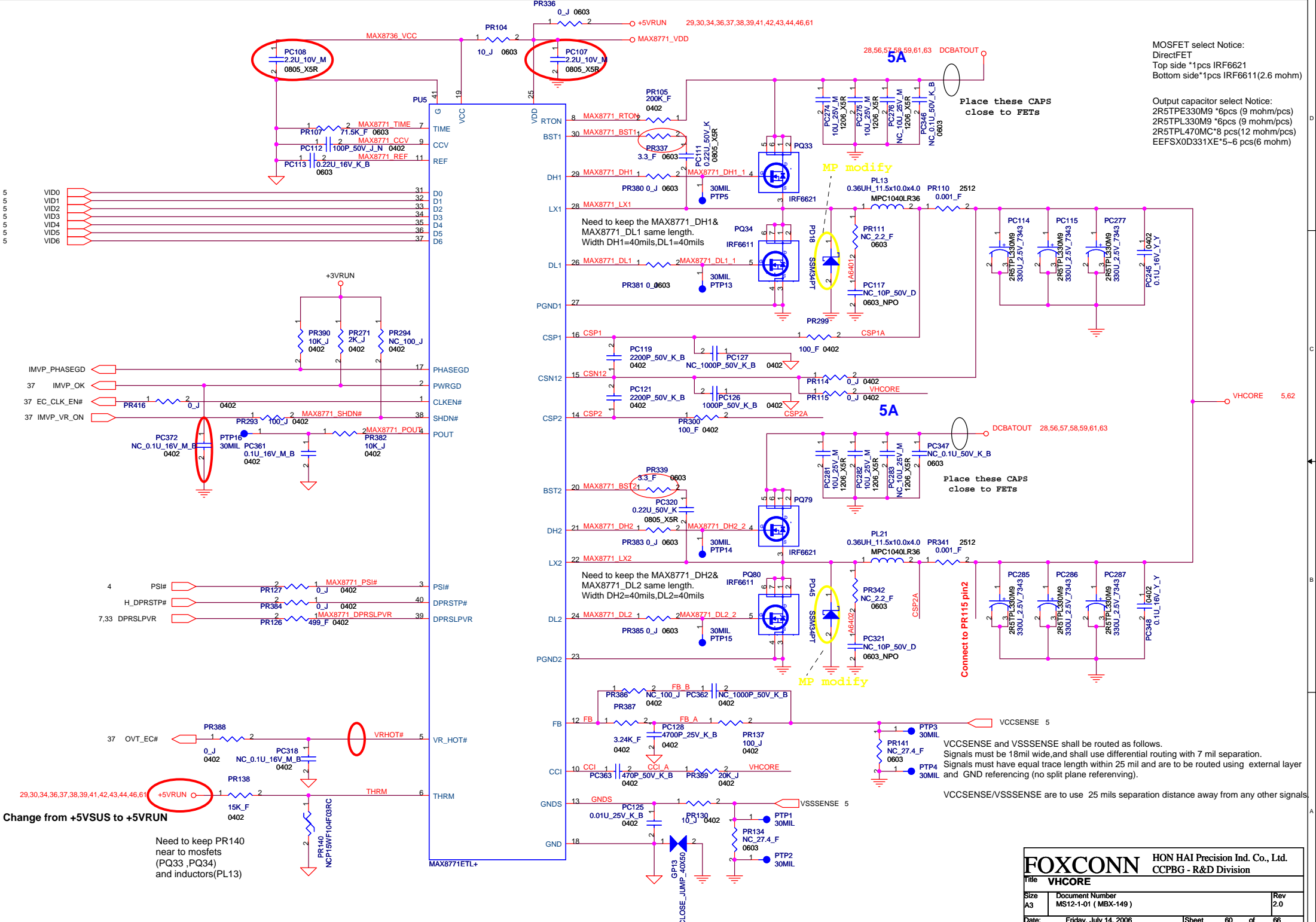
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
or
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)





Notice:
Output capacitor
2R5TPE330M9(ESR=9 mohm,H=1.8mm,Arms=3.9A)
or
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)

Bottom side MOSFET
IRF7832*1 pcs(4 mohm/pcs)
or
IRF7811*2 pcs(14 mohm/pcs)



MOSFET select Notice:
 DirectFET
 Top side *1pcs IRF6621
 Bottom side *1pcs IRF6611(2.6 mohm)

Output capacitor select Notice:
 2R5TPE330M9 *6pcs (9 mohm/pcs)
 2R5TPL330M9 *6pcs (9 mohm/pcs)
 2R5TPL470MC *8 pcs(12 mohm/pcs)
 EEFSXOD331XE*5-6 pcs(6 mohm)

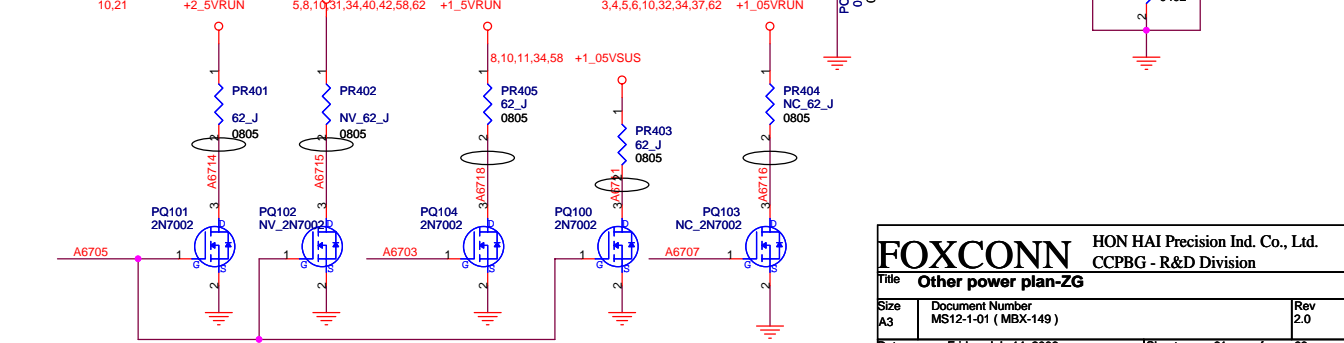
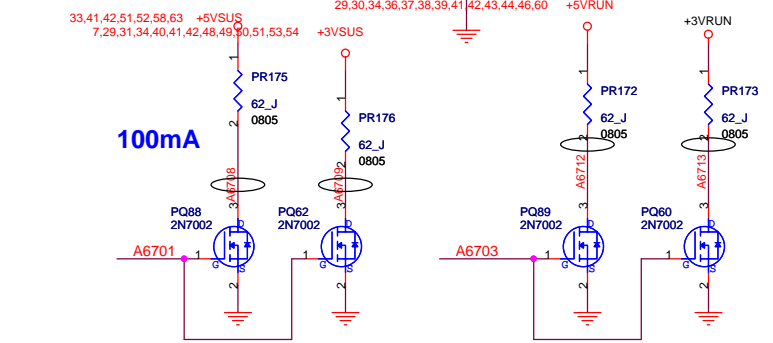
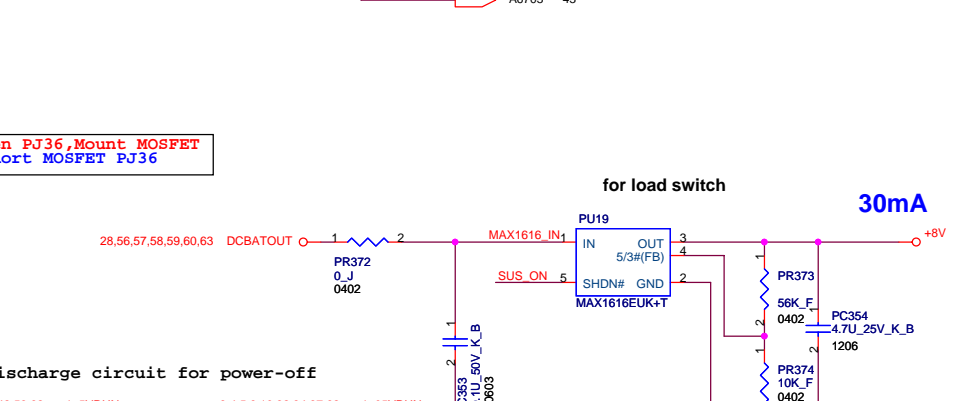
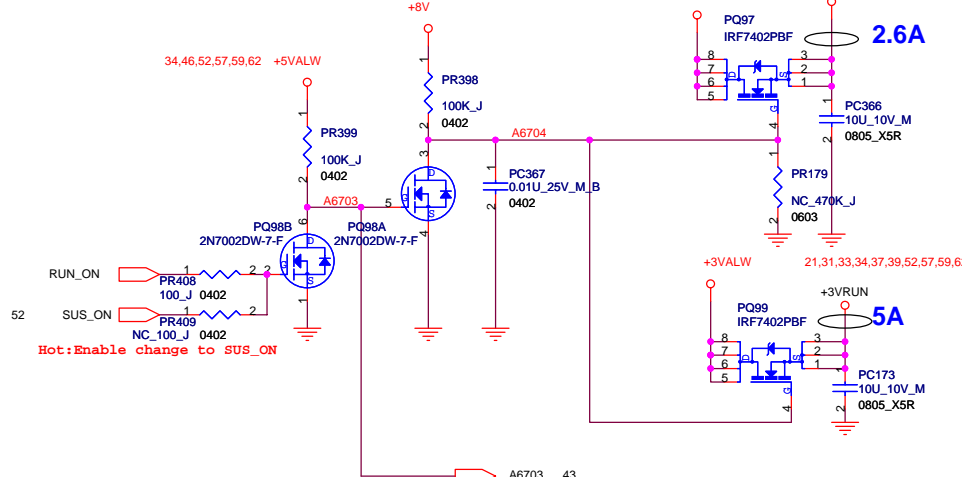
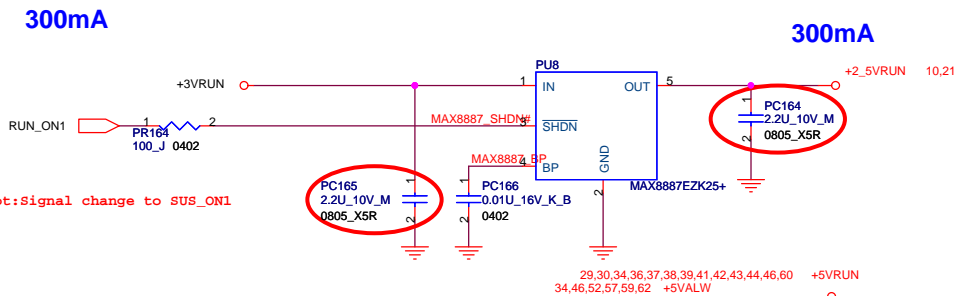
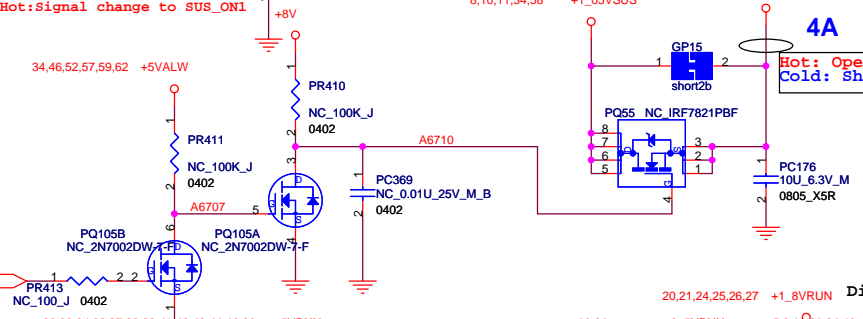
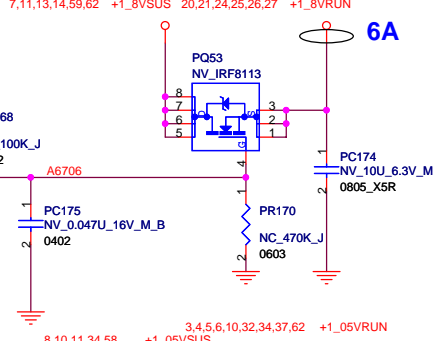
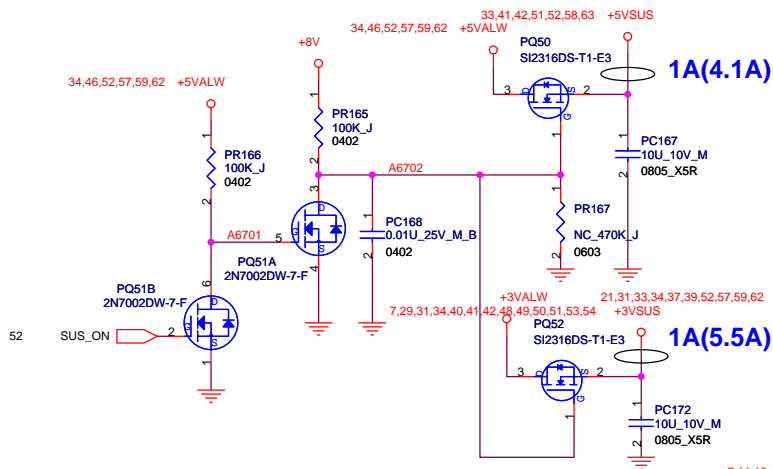
Change from +5VSUS to +5VRUN

Need to keep PR140 near to mosfets (PQ33, PQ34) and inductors(PL13)

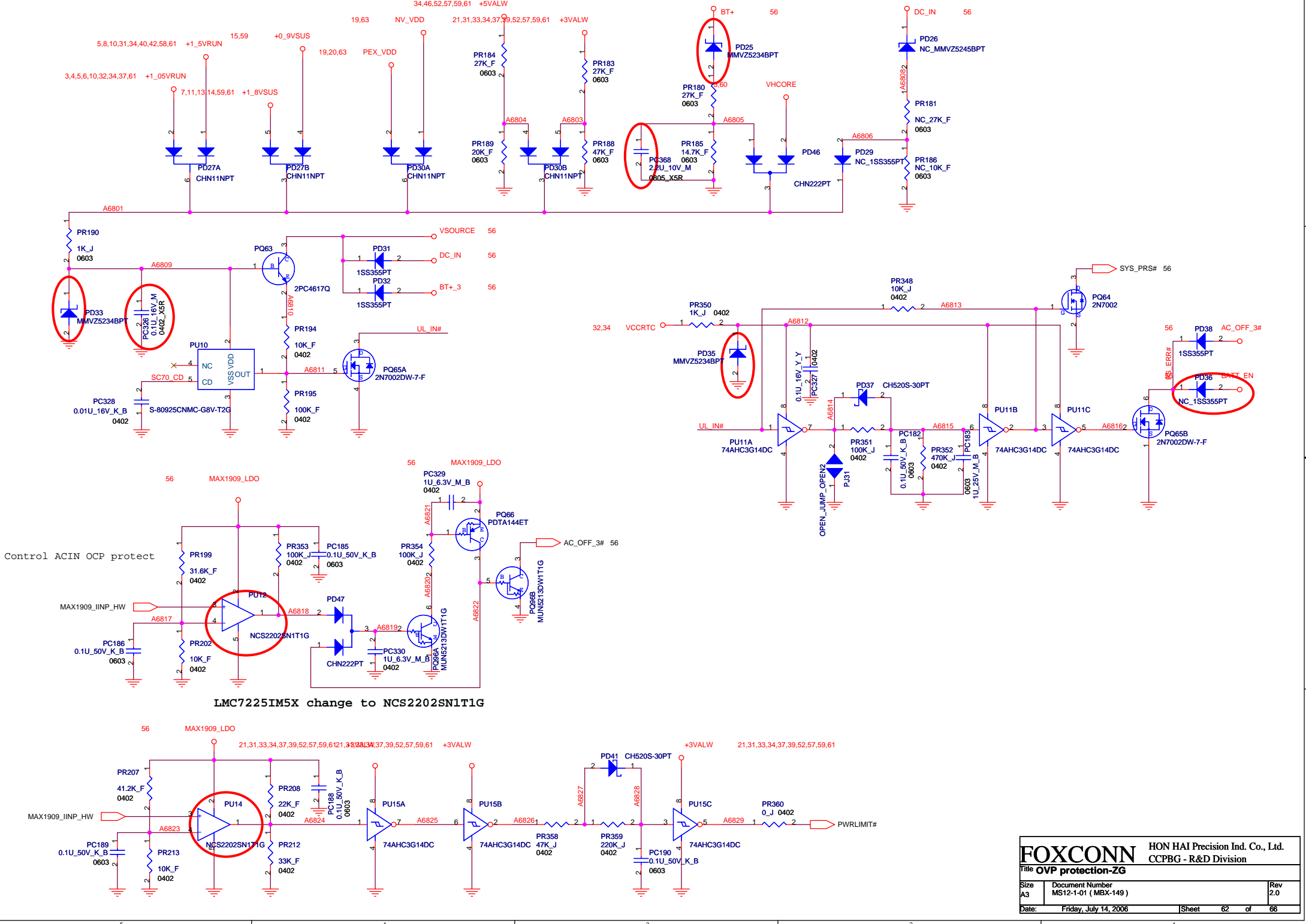
VCCSENSE and VSSSENSE shall be routed as follows.
 Signals must be 18mil wide, and shall use differential routing with 7 mil separation.
 Signals must have equal trace length within 25 mil and are to be routed using external layer and GND referencing (no split plane referencing).

VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

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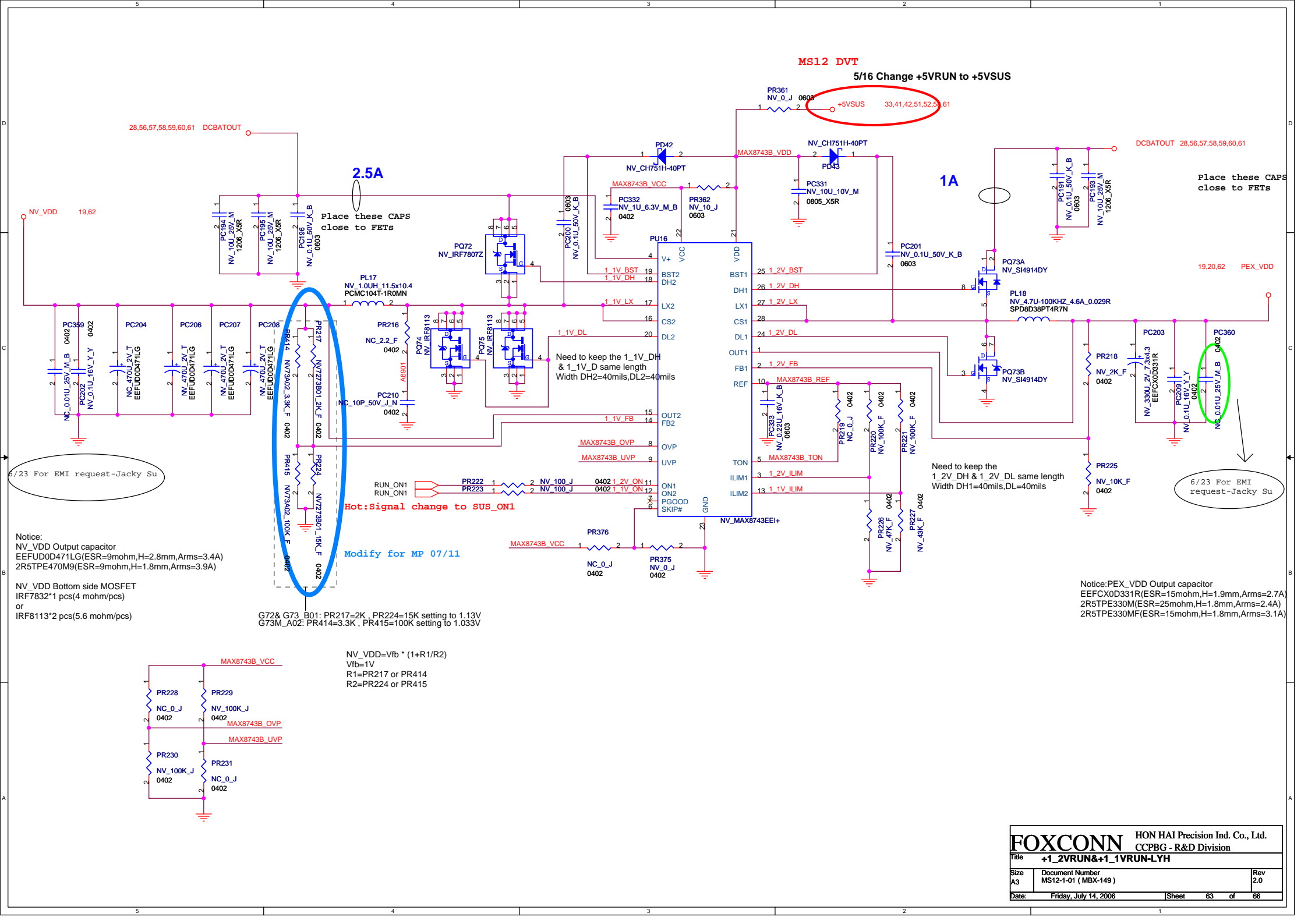
Hot: Open PJ36, Mount MOSFET
Cold: Short MOSFET PJ36



LMC7225IM5X change to NCS2202SN1T1G

MS12 DVT

5/16 Change +5VRUN to +5VSUS



28,56,57,58,59,60,61 DCBATOUT

NV_VDD 19,62

2.5A

Place these CAPS close to FETs

MAX8743B VDD

1A

DCBATOUT 28,56,57,58,59,60,61

Place these CAPS close to FETs

PEX_VDD 19,20,62

Need to keep the 1_1V_DH & 1_1V_D same length Width DH2=40mils, DL2=40mils

Need to keep the 1_2V_DH & 1_2V_DL same length Width DH1=40mils, DL=40mils

6/23 For EMI request-Jacky Su

6/23 For EMI request-Jacky Su

Notice: NV_VDD Output capacitor EEFUD0D471LG(ESR=9mohm,H=2.8mm,Arms=3.4A) 2R5TPE470M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

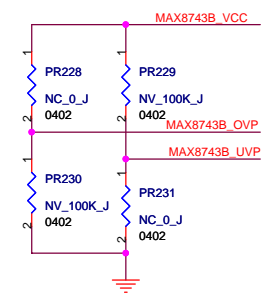
NV_VDD Bottom side MOSFET IRF7832*1 pcs(4 mohm/pcs) or IRF8113*2 pcs(5.6 mohm/pcs)

Modify for MP 07/11

G72& G73_B01: PR217=2K , PR224=15K setting to 1.13V G73M_A02: PR414=3.3K , PR415=100K setting to 1.033V

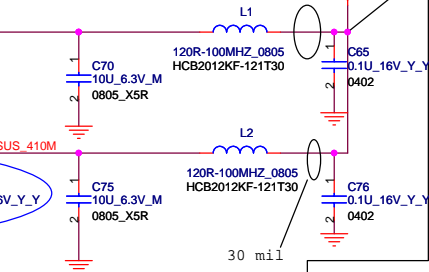
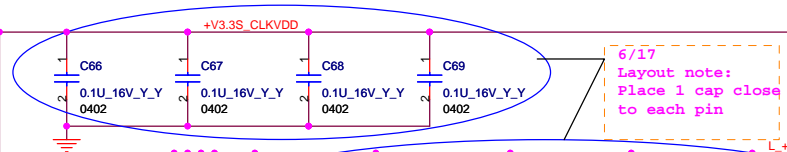
Notice:PEX_VDD Output capacitor EEFCD331R(ESR=15mohm,H=1.9mm,Arms=2.7A) 2R5TPE330M(ESR=25mohm,H=1.8mm,Arms=2.4A) 2R5TPE330MF(ESR=15mohm,H=1.8mm,Arms=3.1A)

NV_VDD=Vfb * (1+R1/R2)
 Vfb=1V
 R1=PR217 or PR414
 R2=PR224 or PR415



NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG
NC_10P_50V_E_N	2	1	

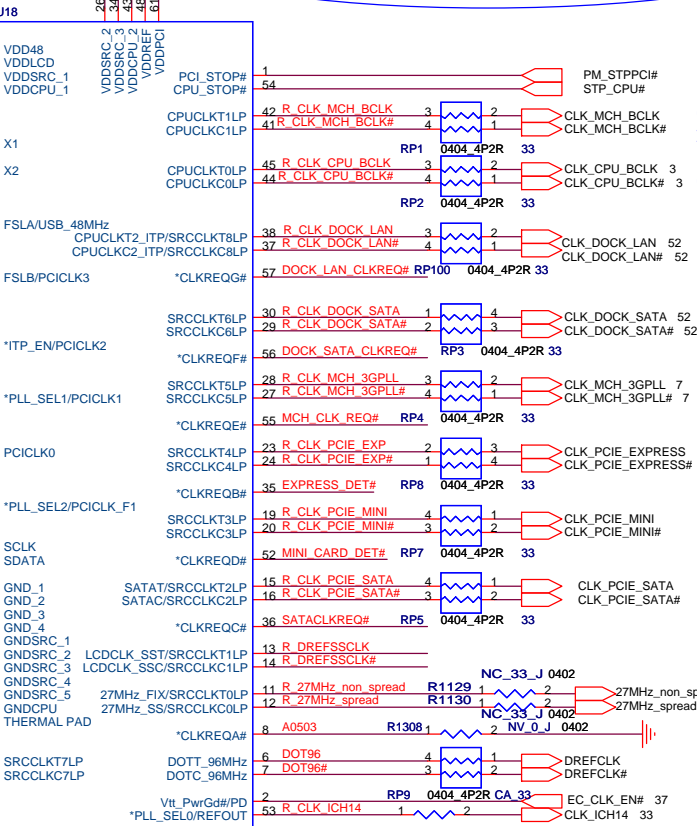
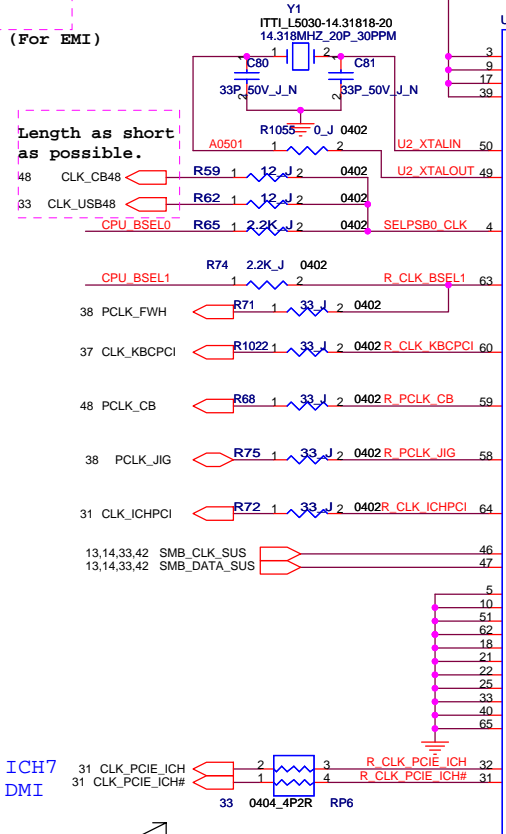
06/17
DEL 0 ohm resistor R38,R47,R50,
0.1u Cap C71 C64
10u Cap C72
Cap C78 changed to 0.1u



Pin Straps			
Pin 53/59/60/64 100K ohm pull-up		pin 11/12	
0	1	SRCCLK0	
		pin 15/16	(v)
0	1	SRCCLK0	SATA
		pin 37/38	(v)
0	1	SRCCLK8	CPU 2 ITP
		pin 13/14	(v)
0	1	LCDCLK SS (CA)	SRCCLK1 (NV)

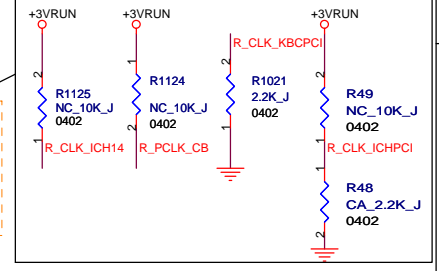
close to clk gen (For EMI)

Length as short as possible.

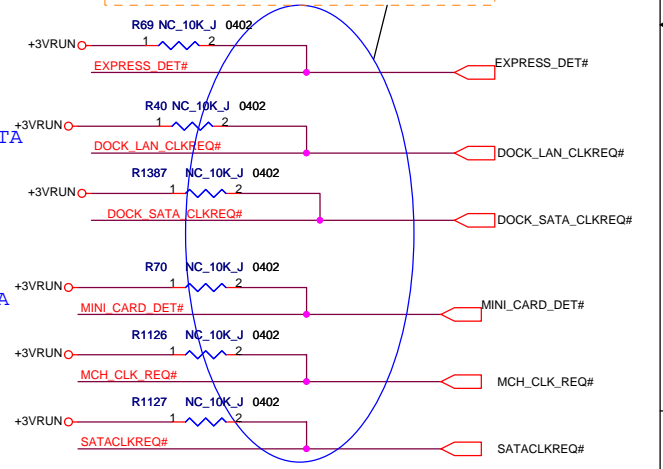


CALISTOGA Chip HOST
CPU

06/16
pin53/59/60/64 with internal pull-up resistor
No Stuff Pull-up Resistor (R1125,R1124,R49)
If EVT ok, del them in DVT
R1021/R48 changed to 2.2Kohm



06/09
CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor (R69,R40,R41,R70,R1126,R1127)
If EVT ok, del them in DVT



ICH7M SATA
Nvidia Graphic
CALISTOGA DOT96

CALISTOGA SSCK
Nvidia Graphic

06/17
CLK_PCIE_ICH changed to SRCCLK7
CLK_DOCK_LAN changed to SRCCLK8
SW Note: datasheet page13 Byte8.1 => SRCCLK7 should be configured as "Not Controlled"

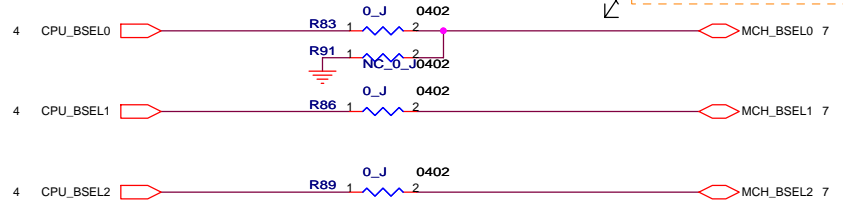
SM bus Address JCS9LPR321BKLF
1101001 (ICH7)
For clock generator

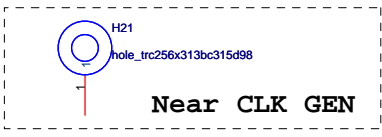
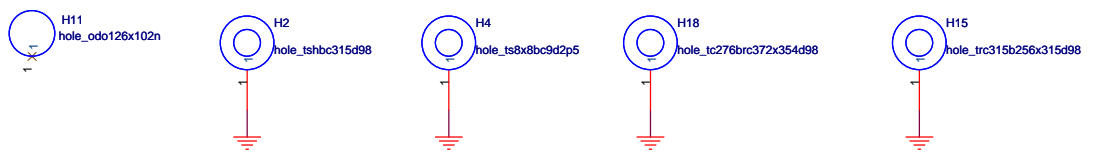
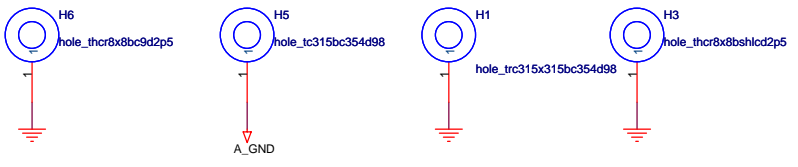
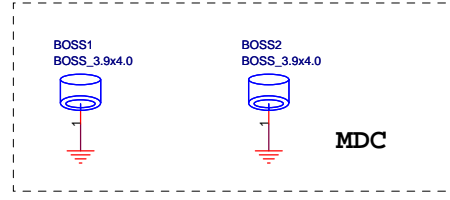
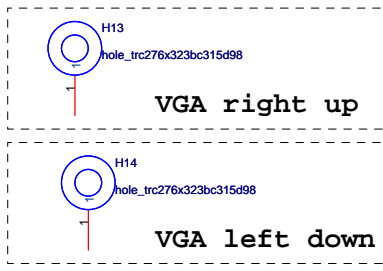
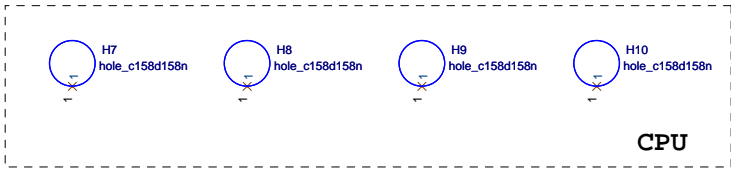
06/09
DEL pull-up resistor R80-82
pull-down resistor R85,R88
Del R84,R87,R90

06/16
ICS have recognized, FSLA/FSLB setting is different from CK410M spec. But MS10 will not use 100MHz, For test purpose, please move R91 from MCH_BSEL2 to MCH_BSEL0, and mount R89.

FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100 33
0	1	133	100 33
1	0	200	100 33
1	1	166	100 33





HISTORY

(2006/04/27 Initail REV 0.30)

- P.5 Change C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C17,C18,C19,C20,C21,C22,C23 from 22uF to 10uF for 22uF shortage.
- P.5 Change C1310,C1311,C1312,C1313,C1314,C1315,C1316,C1317,C1318,C1319,C1320,C1321 to mount for 22uF shortage.
- P.30 Change U84 from SN74AHC1G08DCK to 74AHC1G08GW for making BOM conveniently.
- P.33 Change U30 from 74AHC114GW to SN74AHC1G14DCK for making BOM conveniently.
- P.44 Change Q77,Q78,Q84,Q85 from PBSS2515F.115 to PBSS2525E.115.Because PBSS2515F.115 will be EOL.
- P.44 Change CAP22,CAP23 from SHOEI (SE0J101-3B) to Panasonic (ECGUD0J101ER).Because SE0J101-3B will be EOL.
- P.45 Change C913,C922 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- P.47 Change Q89,Q90,Q91,Q92 from PBSS2515F.115 to PBSS2525E.115.Because PBSS2515F.115 will be EOL.

Power modify

- P.56 Add PR27 , Change PR363/PR364/PQ90 to NC_ condition.Design change and can achieve the same function.
- P.60 Change PR138.1 from +5VSUS to +5VRUN.Keep the same power sequence with MAX8771 VDD.
- P.60 Delete PR338. Have reserved PR388, so can delete PR338.
- P.60 Add PC372 to avoid IMVP_OK signal 700mV pulse when power on.
- P.60 Change PC107/PC108 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- P.61 Change PC164/PC165 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- P.62 Change PU12,PU14 from LMC7225IM5X to NCS2202SNLT1G for LMC7225IM5X shortage.
- P.62 Change PC326 from 0.1U_16V_Y(Y5V) to 0.1U_16V_M (X5R).Because X5R speciality is more stable than Y5V.
- P.62 Change PD25,PD33,PD35 from MMHZ5234BPT to MMVZ5234BPT.Base on test result, MMVZ5234BPT is more stable than MMHZ5234BPT
- P.62 Change PD36 to NC_condition.When delete PD36, can also achieve the same function by SYS_PRS# signal.
- P.62 Change PC368 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- P.63 Change PR361.2 from +5VSUS to +5VRUN.To achieve more logical design and can save a little power consumption on S3 mode

(2006/05/05 System ID modify)

- P.37 Add R1463 and R1464 for making BOM conveniently.
- P.37 Change R719 from 100K_J to NV72_100K_J for making BOM conveniently.
- P.37 Change R724 from NC_100K_J to 100K_J for new System ID table.
- P.37 Change R725 from 100K_J to NC_100K_J for new System ID table.
- P.37 Change R727 from 100K_J to NC_100K_J for new System ID table.
- P.37 Change R728 from NC_100K_J to 100K_J for new System ID table.

(2006/05/8)

- P.41 Change Q93 from DTC144EUA to BT_DTC144EUA.
- P.53 Change R1311 from 0_J to HUB_0_J.
- P.53 Change R1461 from 0_J to HUB_0_J.

(2006/05/11)

- P.52 Change C1003 from 1210 to 1206/1210 dual layout package for MLCC shortage
- P.56 Change PC16, PC24, PC25, PC31, PC32, PC33 from 1210 to 1206/1210 dual layout package for MLCC shortage
- P.57 Change PC42, PC43, PC350 from 1210 to 1206/1210 dual layout package for MLCC shortage
- P.58 Change PC62, PC71, PC72 from 1206 to 1206/1210 dual layout package for MLCC shortage
- P.59 Change PC84, PC87, PC306 from 1210 to 1206/1210 dual layout package for MLCC shortage
- P.60 Change PC274, PC275, PC276, PC281, PC282, PC283 from 1206 to 1206/1210 dual layout package for MLCC shortage
- P.63 Change PC193, PC194, PC195 from 1206 to 1206/1210 dual layout package for MLCC shortage
- P.58 Change PR79 from 36K_F to 51K_F for MOSFET 2nd source OCP common setting.
- P.63 Change PR227 from NV_39_2K_F to NV_43K_F for MOSFET 2nd source OCP common setting.

(2006/05/16)

- P.63 Change PR361.2 from +5VRUN to +5VSUS.

(2006/05/18)

- P.56 Change PR27 from 0_J to NC_0_J.
- P.56 Change PR363 from NC_10K_J to 10K_J.
- P.56 Change PR364 from NC_120K_J to 120K_J.
- P.56 Change PQ90 from NC_MUN5213DW1T1G to MUN5213DW1T1G.

PVT MODIFY

(2006/06/13)

- P.36 Change CN32 footprint from FOXCONN_QT8H0506_H113R_4F to FOXCONN_QT8H0506_H113R_4F_MS12.
Modify footprint to avoid connector short.
- P.56 Change net(PD40 pin2) from ALW_ON to ALW_ON1.
- P.57 Change PR53, PR55 from 100_J to 0_J and add a resistor PR418(1K_J) for prevent EC damage when power protect occur.

(2006/06/16)

- P.5 Change C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C17,C18,C19,C20,C21,C22,C23 from 10uF to 22uF for BOM control.
- P.5 Change C1310,C1311,C1312,C1313,C1314,C1315,C1316,C1317,C1318,C1319,C1320,C1321 from mount to NC for BOM control.

(2006/06/20)

- P.46 Change D67 from ASKS02-03S-G to CH520S-30PT. Because ASKS02-03S-G will be EOL.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
History (1)			
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c			
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HISTORY

MP MODIFY

(2006/07/11)

P.36 Add D72 to avoid ESD fail for Pioneer SMDL K16VAD.

P.63 Change PR217 and PR224 head value from NV72_ to NV7273B01_. Because NV73M_B01 NVVDD need 1.1V.

P.63 Change PR414 and PR415 head value from NV73_ to NV73A02_. Because NV73M_A02 NVVDD still need 1.0V.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title History (1)		
Size c	Document Number MS12-1-01 (MBX-149)	Rev 2.0
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