

**Schematics Page Index (Title / Revision / Change Date)**

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48	Others power plane
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50	VGA Power(ATI_M82 XT-S)
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52	HOLE
53	CHANGELIST

BOM Control Table						
Value Prefix	CA_	AT_	DS_	ND_	LND_	HD_
UMA (W/ Dock)	v		v			
UMA (W/O Dock)	v			v	v	
M82 (W/ Dock)		v	v			
M82 (W/O Dock HDMI)		v		v		
M82 (w/dock W/ HDMI )		v	v			v

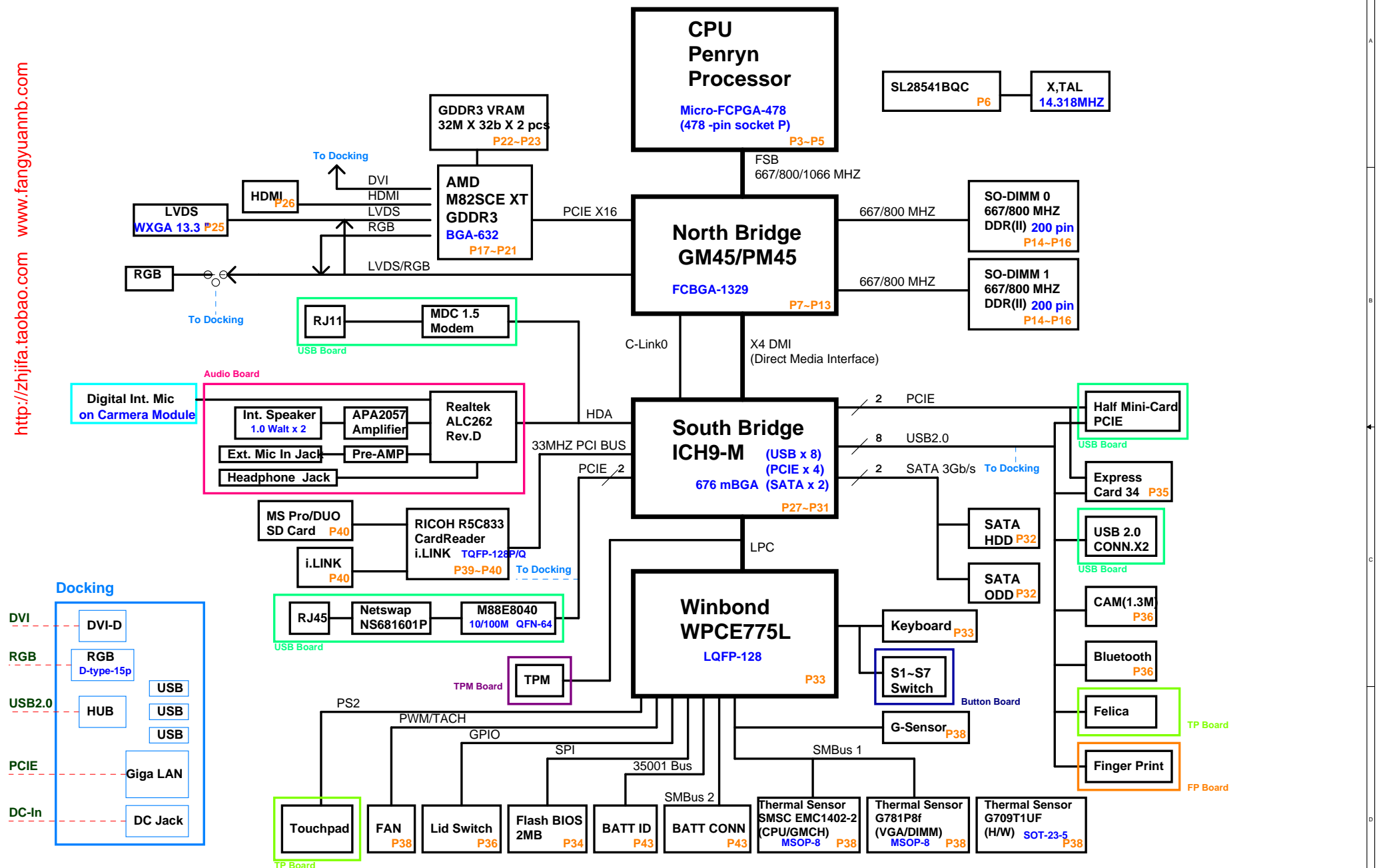
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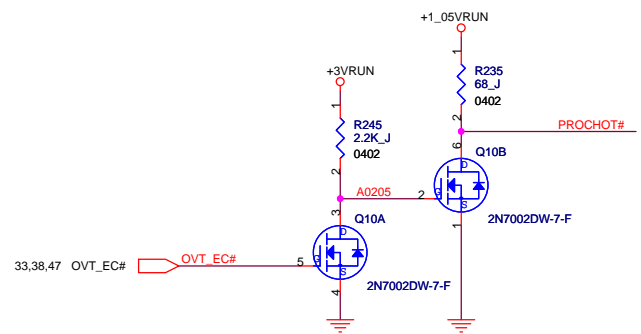
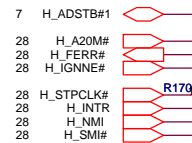
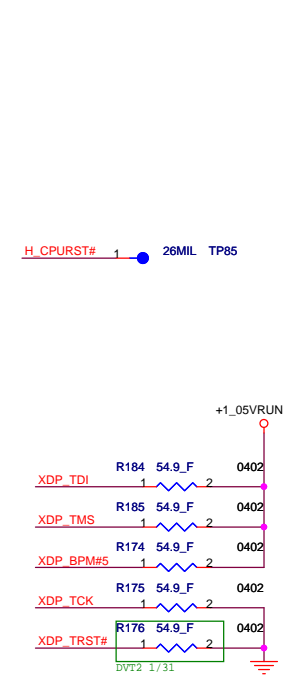
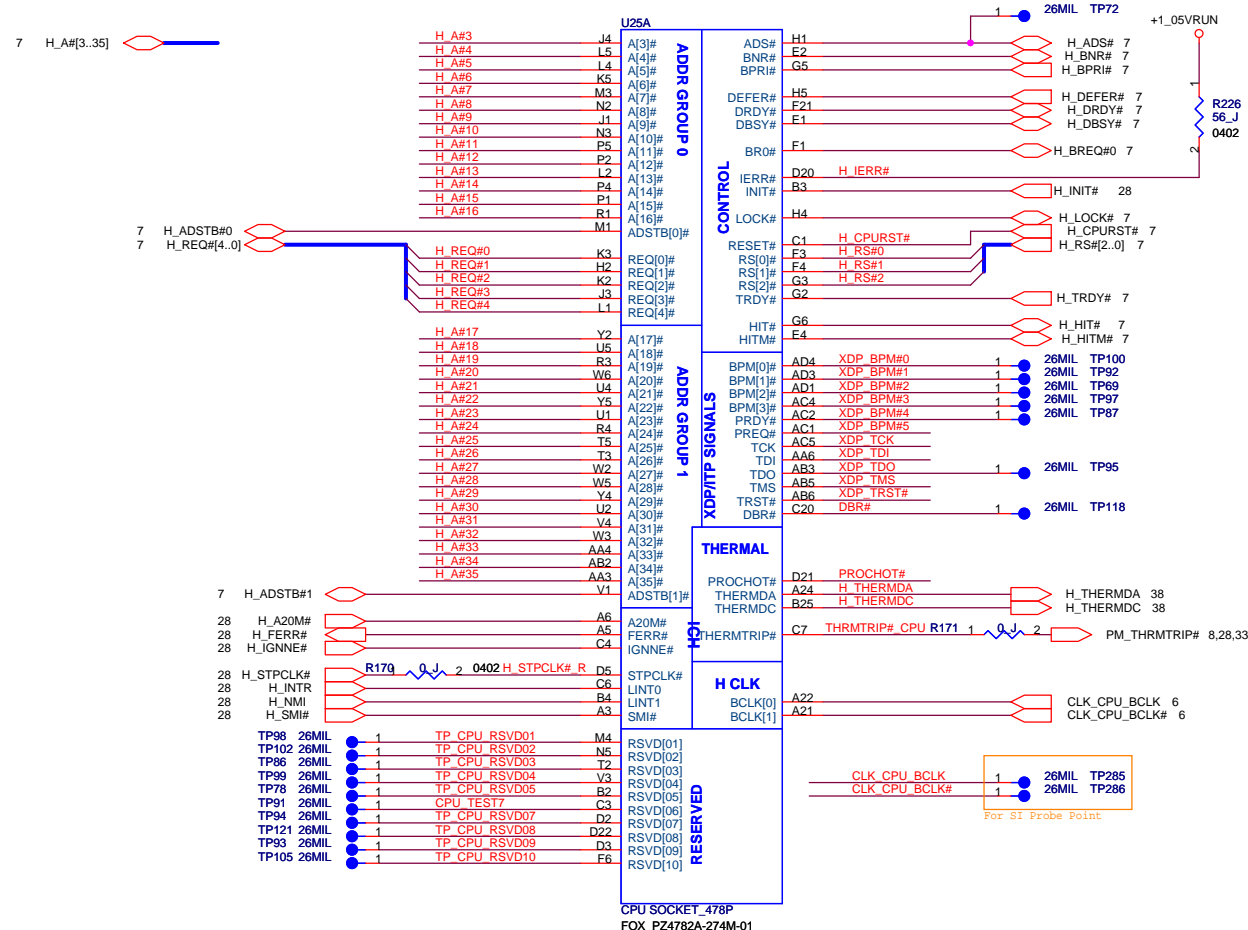
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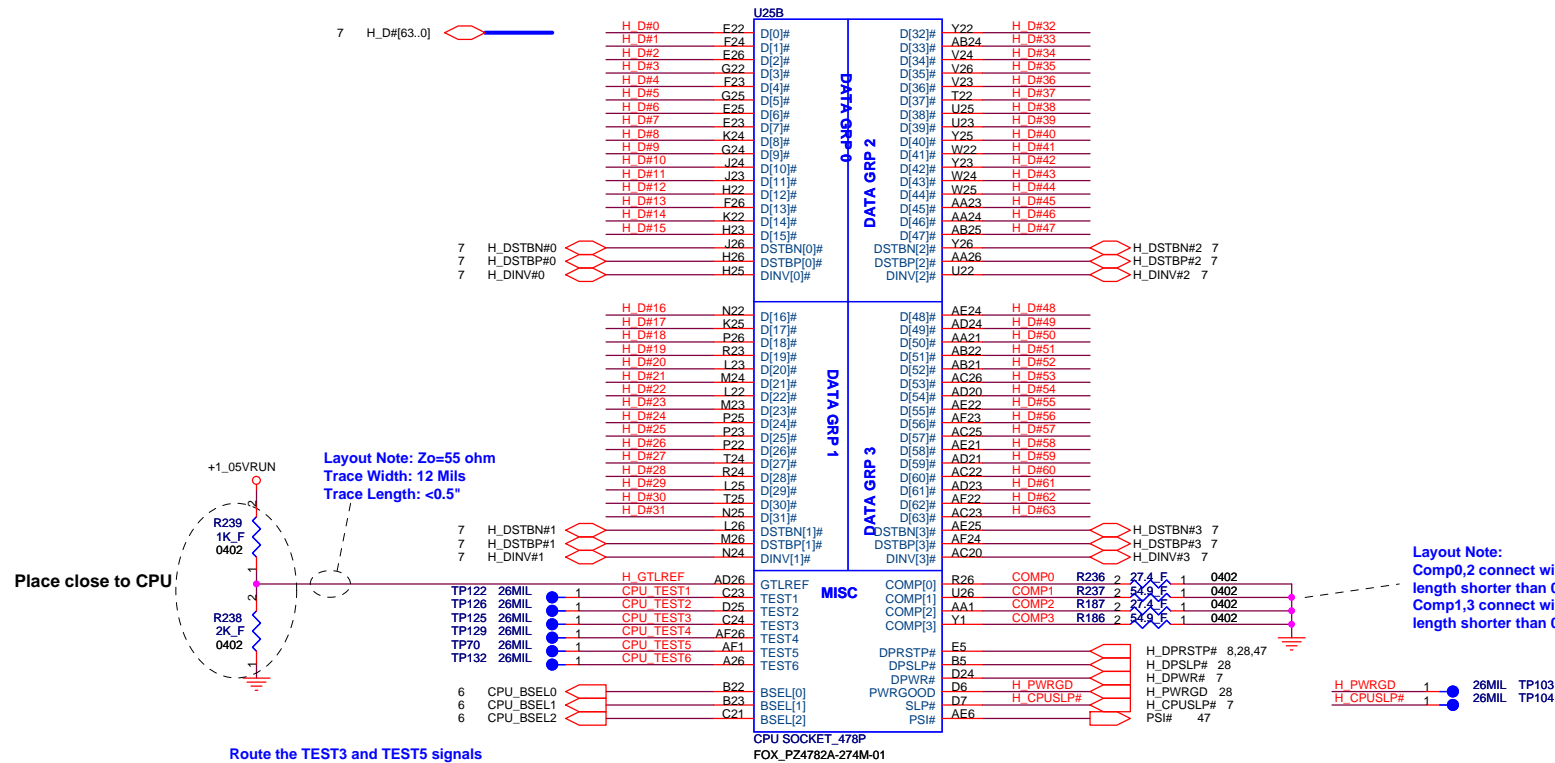
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Title <b>Index Page</b>			
Size	Document Number	Rev	
Custom	M750-1-01	1.0	
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# M750 (Montevina + M82SCE XT)

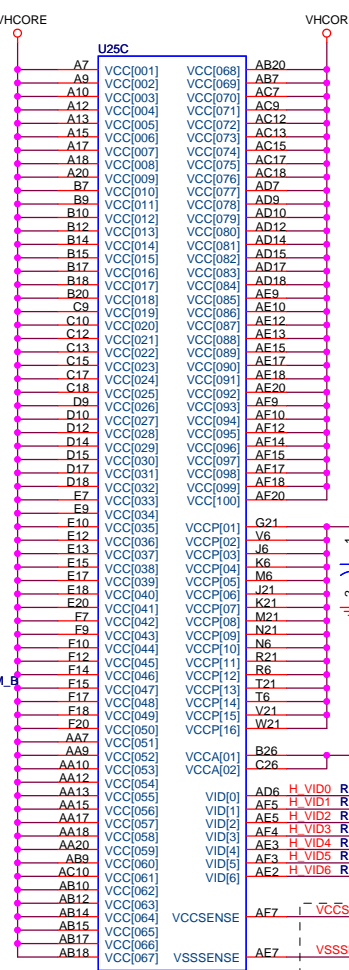
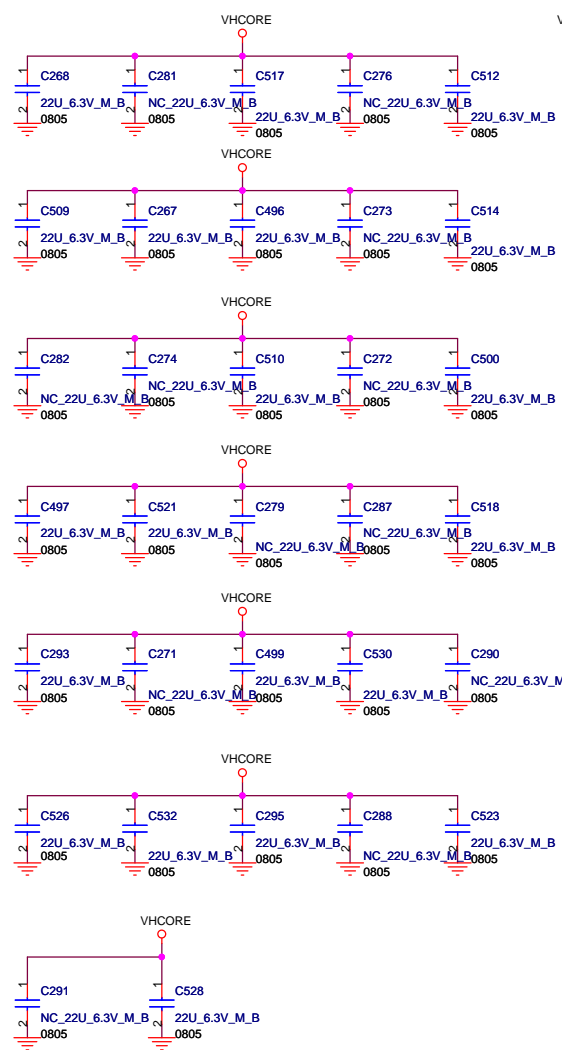
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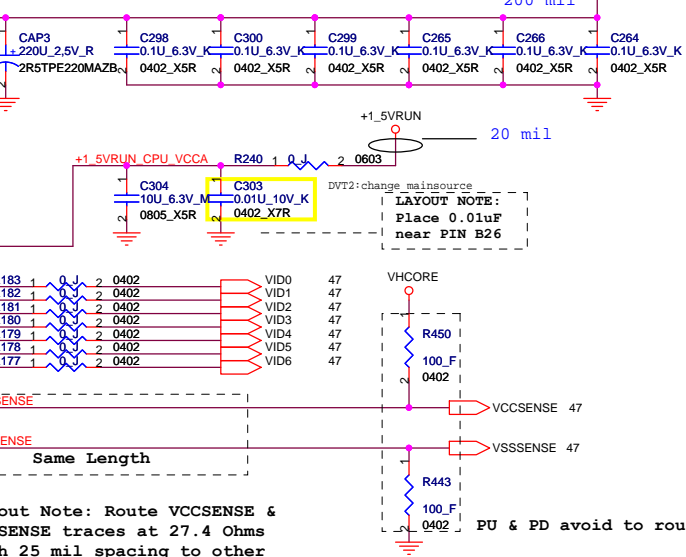




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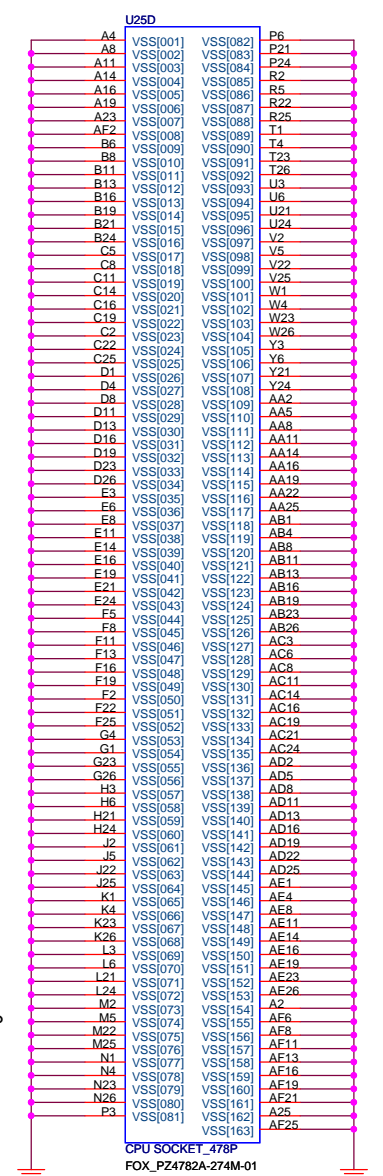
CPU\_VCCA---->0.13A  
CPU\_VCCP---->2.5A  
CPU\_VCC---->47A

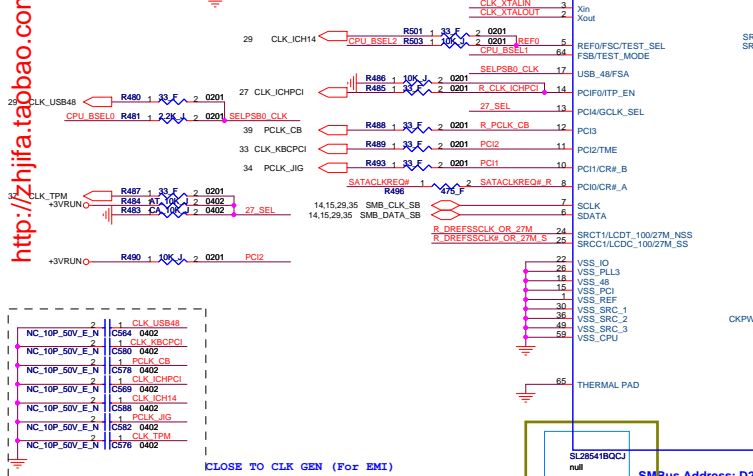
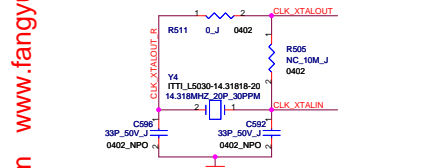
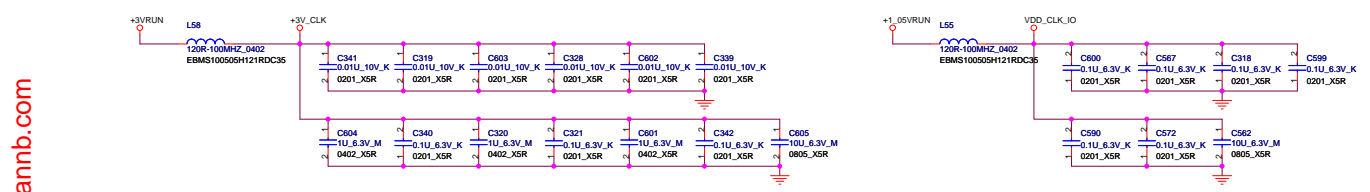


Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 2 inch of CPU.

Outer width=13 mil spacing=7 mil  
Inner width=13 mil spacing=7 mil  
Length match < 25 mil

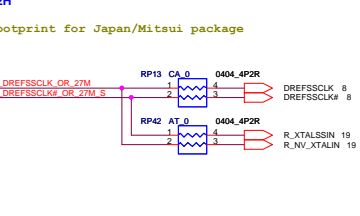
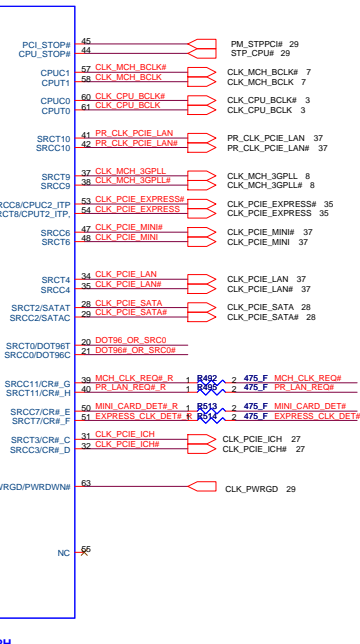
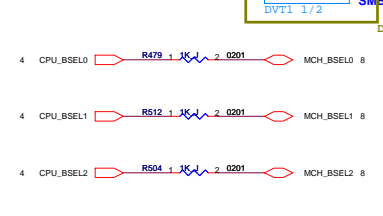
PU & PD avoid to route with stub



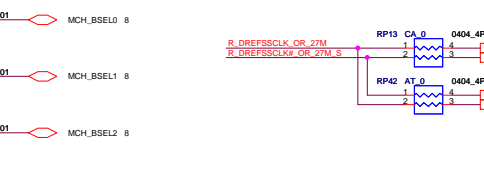
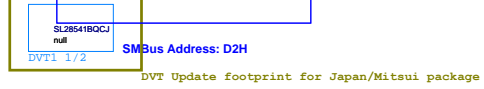
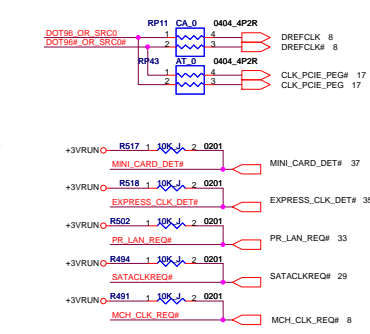


**FSB Frequency Table:**

FSLC	FSLB	FSLA	CPU SRC	PCI
0	0	0	266.66	100 33
0	0	1	133.33	100 33
0	1	0	200	100 33
0	1	1	166.66	100 33
1	0	0	333.33	100 33
1	0	1	100	100 33
1	1	0	400	100 33



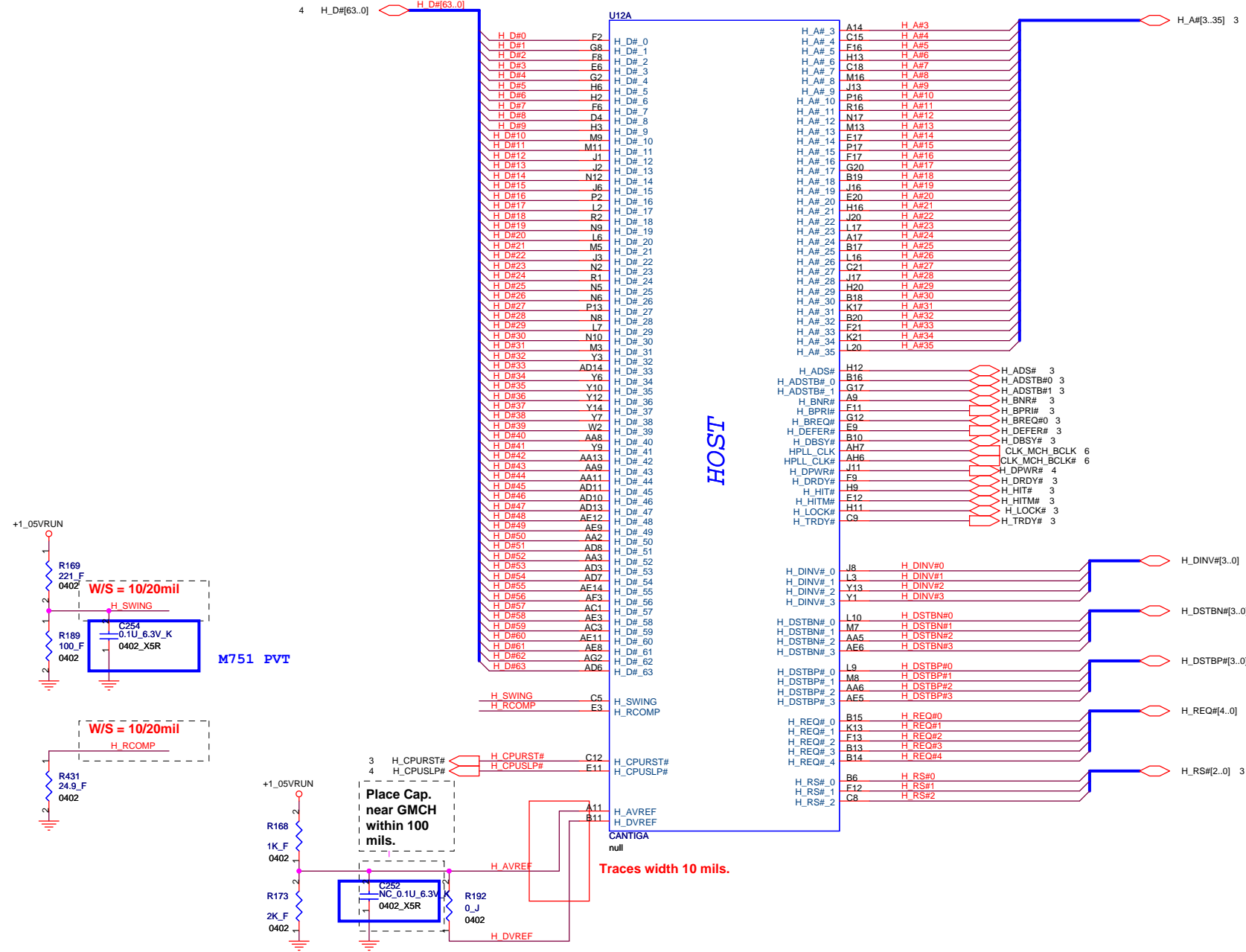
Clock Request	Clock Request Function
CR#A	SRC0, 2
CR#B	SRC1, 4
CR#C	SRC0, 2
CR#D	SRC1, 4
CR#E	SRC6
CR#F	SRC8
CR#G	SRC9
CR#H	SRC10



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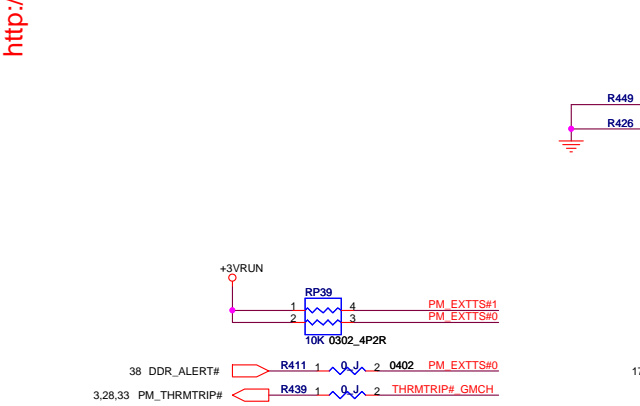
**CLOCK GEN**

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Size: \_\_\_\_\_  
A2: Document Number M750-1-01 Rev 1.0  
Date: Monday, June 23, 2008 Sheet 6 of 54

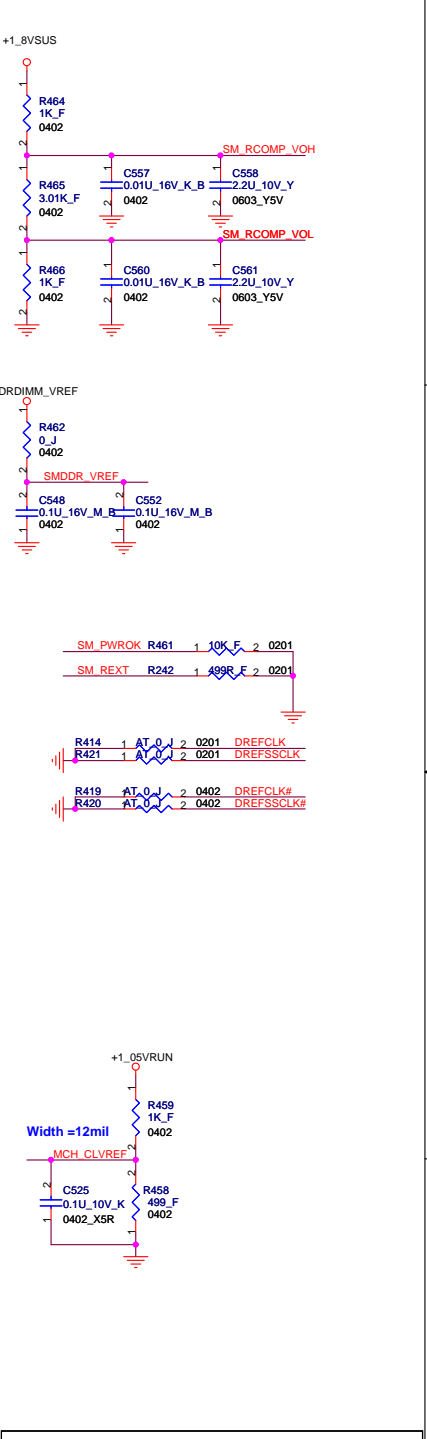
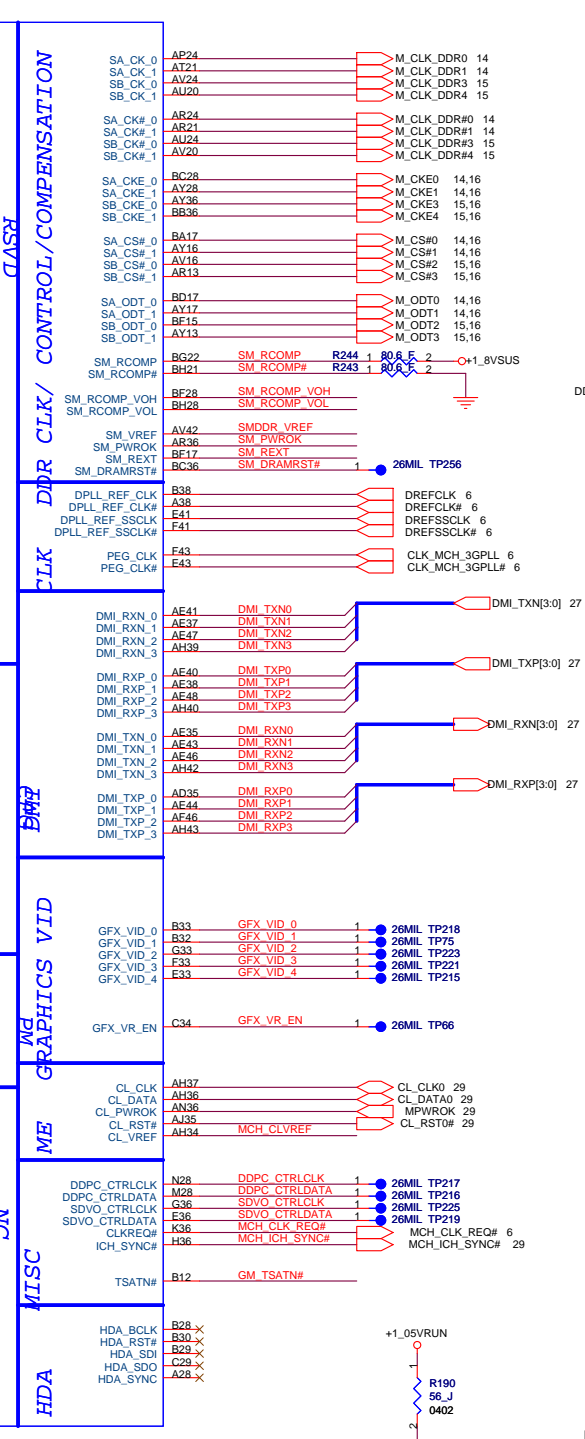




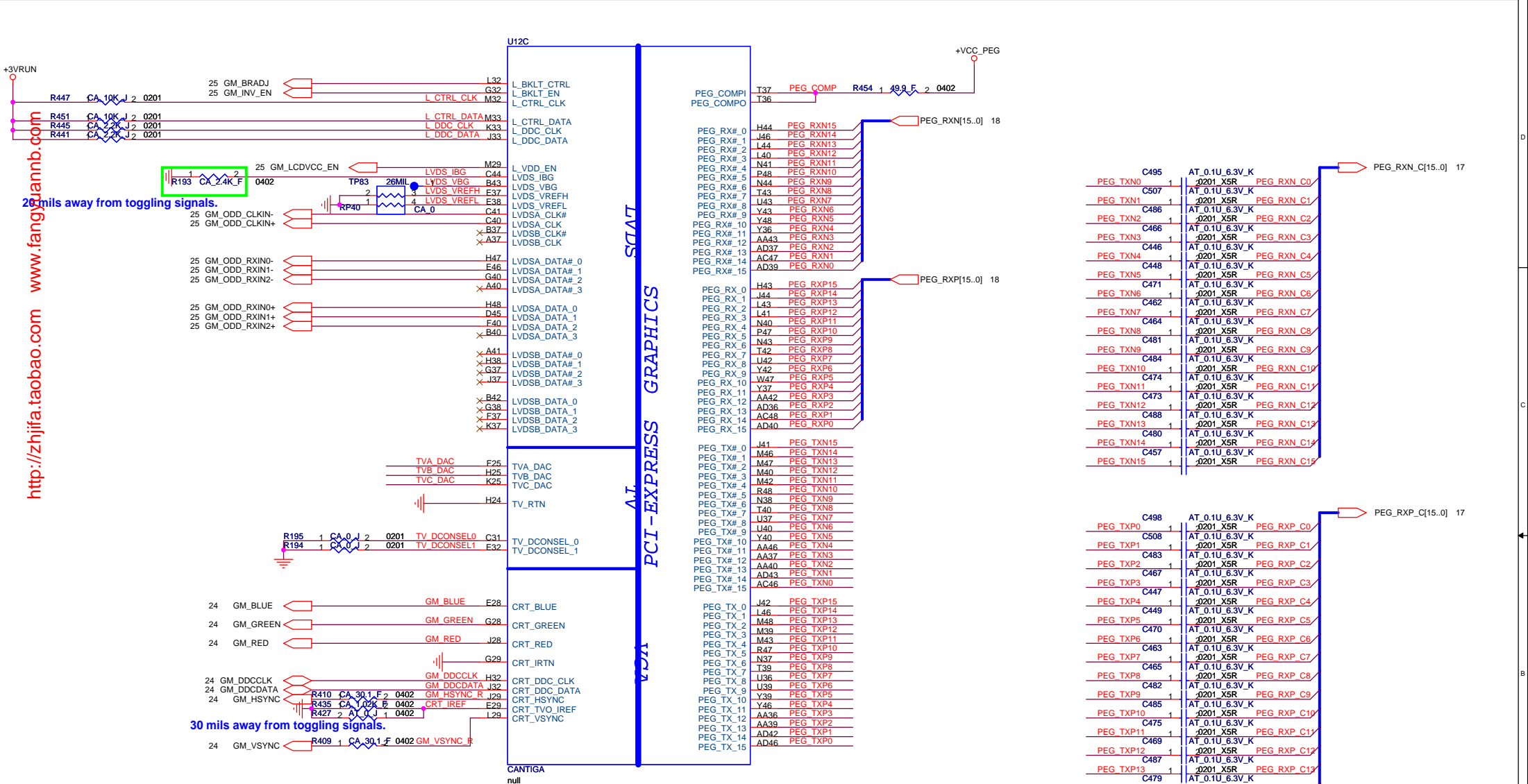
MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800 ; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Transport Layer Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Lane Reversed High = Normal operation
MCH_CFG_10 PCIe Loopback enable	Low = Enabled High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default). High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port



TP229 26MIL	1	MCH_RSVD 1	M36	RSVD1
TP235 26MIL	1	MCH_RSVD 2	N36	RSVD2
TP233 26MIL	1	MCH_RSVD 3	R33	RSVD3
TP240 26MIL	1	MCH_RSVD 4	T33	RSVD4
TP248 26MIL	1	MCH_RSVD 5	AH9	RSVD5
TP246 26MIL	1	MCH_RSVD 6	AH10	RSVD6
TP243 26MIL	1	MCH_RSVD 7	AH12	RSVD7
TP245 26MIL	1	MCH_RSVD 8	AH13	RSVD8
TP227 26MIL	1	MCH_RSVD 9	K12	RSVD9
TP250 26MIL	1	MCH_RSVD 10	AL34	RSVD10
TP244 26MIL	1	MCH_RSVD 11	AK34	RSVD11
TP252 26MIL	1	MCH_RSVD 12	AN35	RSVD12
TP253 26MIL	1	MCH_RSVD 13	AM35	RSVD13
TP241 26MIL	1	MCH_RSVD 14	T24	RSVD14
TP81 26MIL	1	MCH_RSVD 15	B31	RSVD15
TP65 26MIL	1	MCH_RSVD 16	B2	RSVD16
TP106 26MIL	1	MCH_RSVD 17	M1	RSVD17
TP254 26MIL	1	MCH_RSVD 20	AY21	RSVD20
TP140 26MIL	1	MCH_RSVD 22	BG23	RSVD22
TP255 26MIL	1	MCH_RSVD 23	BF23	RSVD23
TP142 26MIL	1	MCH_RSVD 24	BH18	RSVD24
TP144 26MIL	1	MCH_RSVD 25	BF18	RSVD25



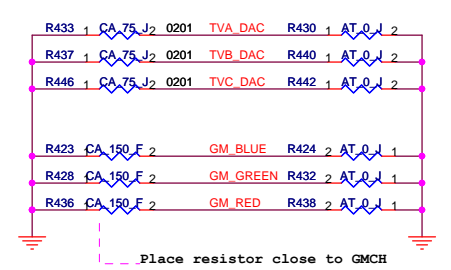
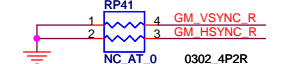




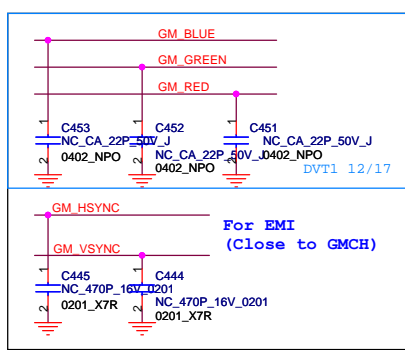
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25 mils away from toggling signals.

30 mils away from toggling signals.



Place resistor close to GMCH



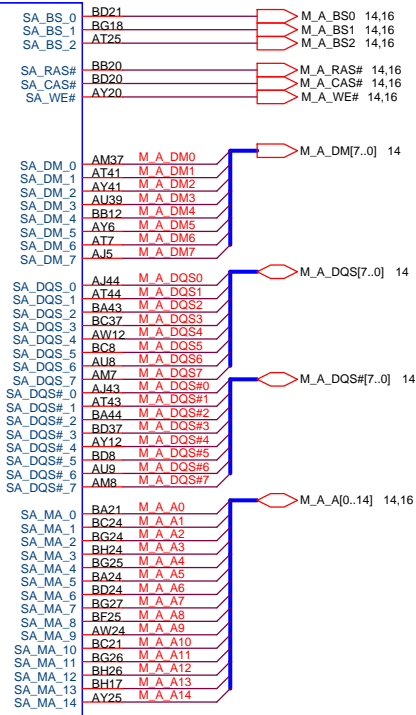
For EMI (Close to GMCH)

PEG_TXN0	C495	AT_0.1U_6.3V_K	PEG_RXN_C0	PEG_RXN_C[15..0]	17
PEG_TXN1	C507	AT_0.1U_6.3V_K	PEG_RXN_C1		
PEG_TXN2	C486	AT_0.1U_6.3V_K	PEG_RXN_C2		
PEG_TXN3	C466	AT_0.1U_6.3V_K	PEG_RXN_C3		
PEG_TXN4	C446	AT_0.1U_6.3V_K	PEG_RXN_C4		
PEG_TXN5	C448	AT_0.1U_6.3V_K	PEG_RXN_C5		
PEG_TXN6	C471	AT_0.1U_6.3V_K	PEG_RXN_C6		
PEG_TXN7	C462	AT_0.1U_6.3V_K	PEG_RXN_C7		
PEG_TXN8	C464	AT_0.1U_6.3V_K	PEG_RXN_C8		
PEG_TXN9	C481	AT_0.1U_6.3V_K	PEG_RXN_C9		
PEG_TXN10	C484	AT_0.1U_6.3V_K	PEG_RXN_C10		
PEG_TXN11	C474	AT_0.1U_6.3V_K	PEG_RXN_C11		
PEG_TXN12	C473	AT_0.1U_6.3V_K	PEG_RXN_C12		
PEG_TXN13	C488	AT_0.1U_6.3V_K	PEG_RXN_C13		
PEG_TXN14	C480	AT_0.1U_6.3V_K	PEG_RXN_C14		
PEG_TXN15	C457	AT_0.1U_6.3V_K	PEG_RXN_C15		

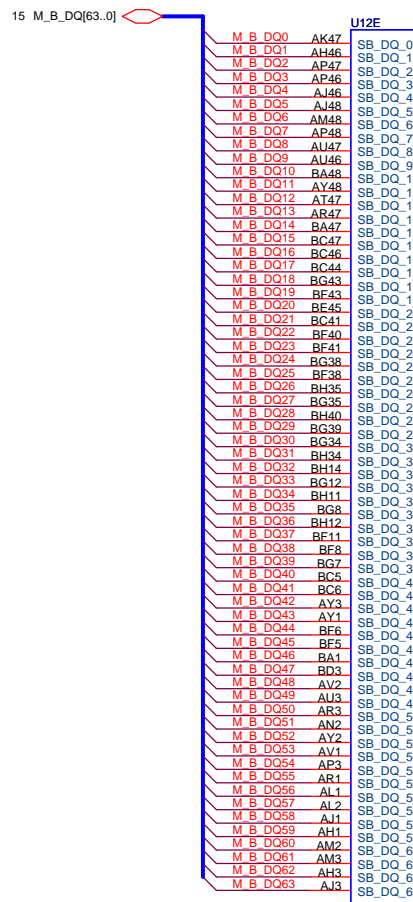
PEG_RXP0	C498	AT_0.1U_6.3V_K	PEG_RXP_C0	PEG_RXP_C[15..0]	17
PEG_RXP1	C508	AT_0.1U_6.3V_K	PEG_RXP_C1		
PEG_RXP2	C483	AT_0.1U_6.3V_K	PEG_RXP_C2		
PEG_RXP3	C467	AT_0.1U_6.3V_K	PEG_RXP_C3		
PEG_RXP4	C447	AT_0.1U_6.3V_K	PEG_RXP_C4		
PEG_RXP5	C449	AT_0.1U_6.3V_K	PEG_RXP_C5		
PEG_RXP6	C470	AT_0.1U_6.3V_K	PEG_RXP_C6		
PEG_RXP7	C463	AT_0.1U_6.3V_K	PEG_RXP_C7		
PEG_RXP8	C465	AT_0.1U_6.3V_K	PEG_RXP_C8		
PEG_RXP9	C482	AT_0.1U_6.3V_K	PEG_RXP_C9		
PEG_RXP10	C485	AT_0.1U_6.3V_K	PEG_RXP_C10		
PEG_RXP11	C475	AT_0.1U_6.3V_K	PEG_RXP_C11		
PEG_RXP12	C469	AT_0.1U_6.3V_K	PEG_RXP_C12		
PEG_RXP13	C487	AT_0.1U_6.3V_K	PEG_RXP_C13		
PEG_RXP14	C479	AT_0.1U_6.3V_K	PEG_RXP_C14		
PEG_RXP15	C456	AT_0.1U_6.3V_K	PEG_RXP_C15		



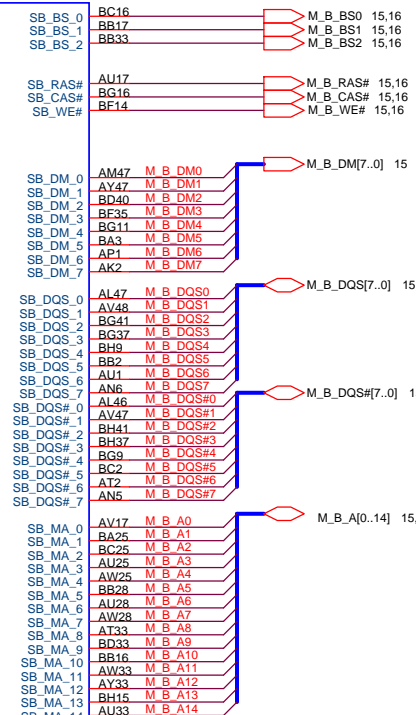
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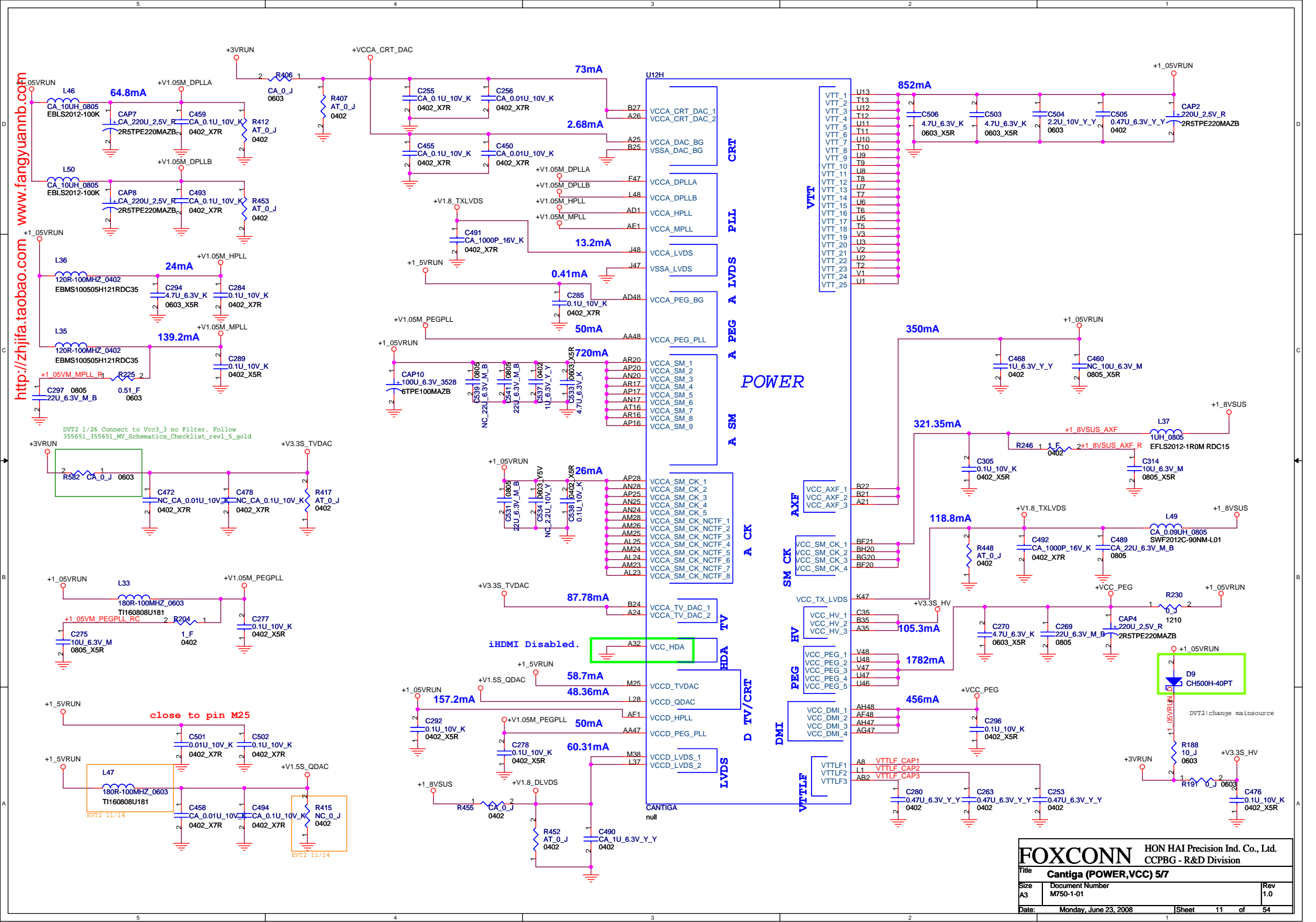
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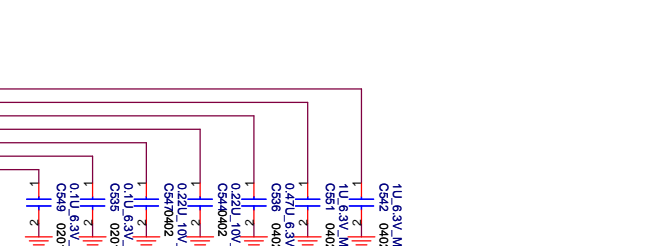
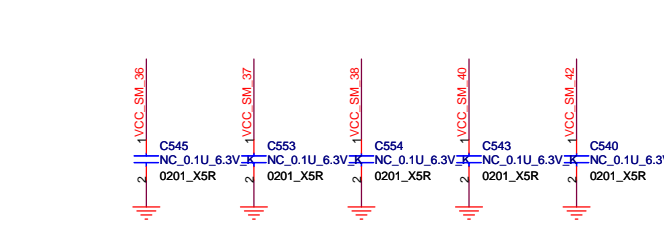
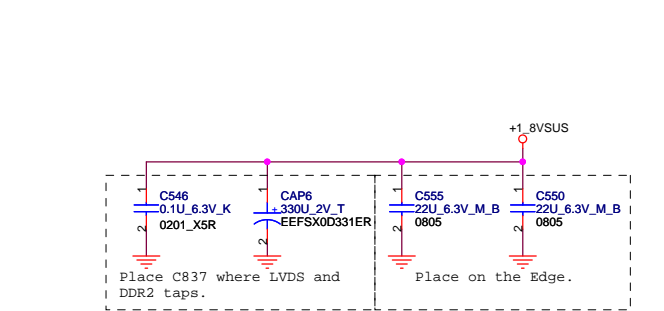
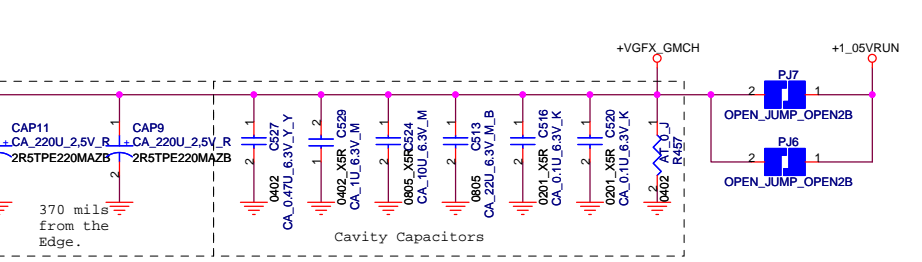
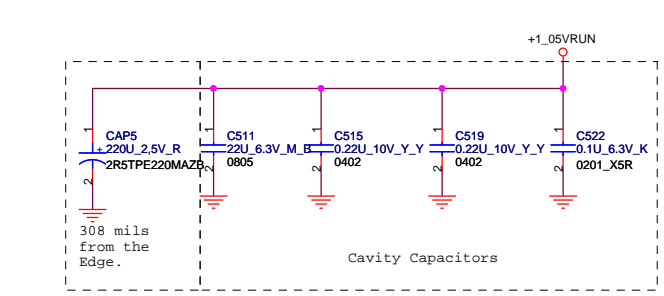
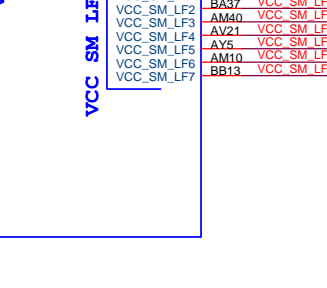
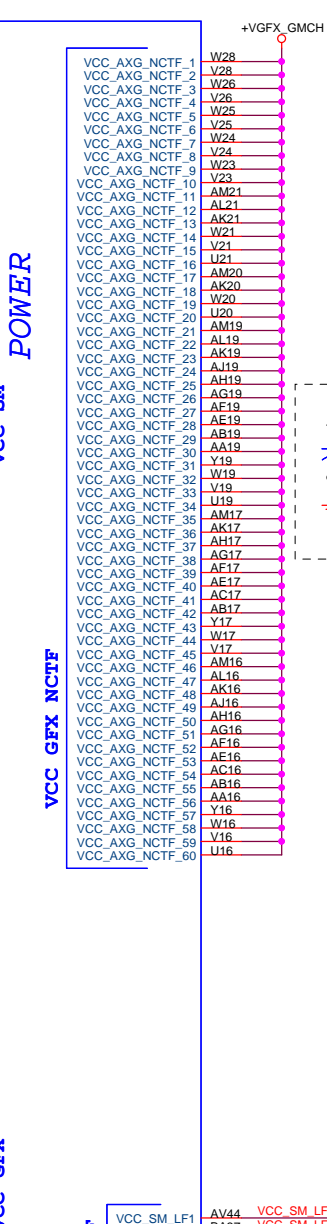
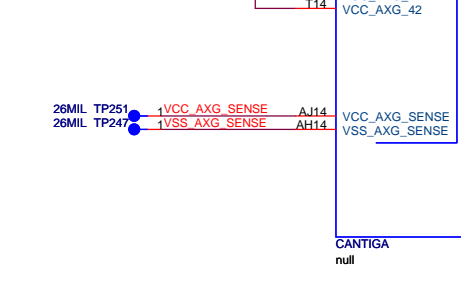
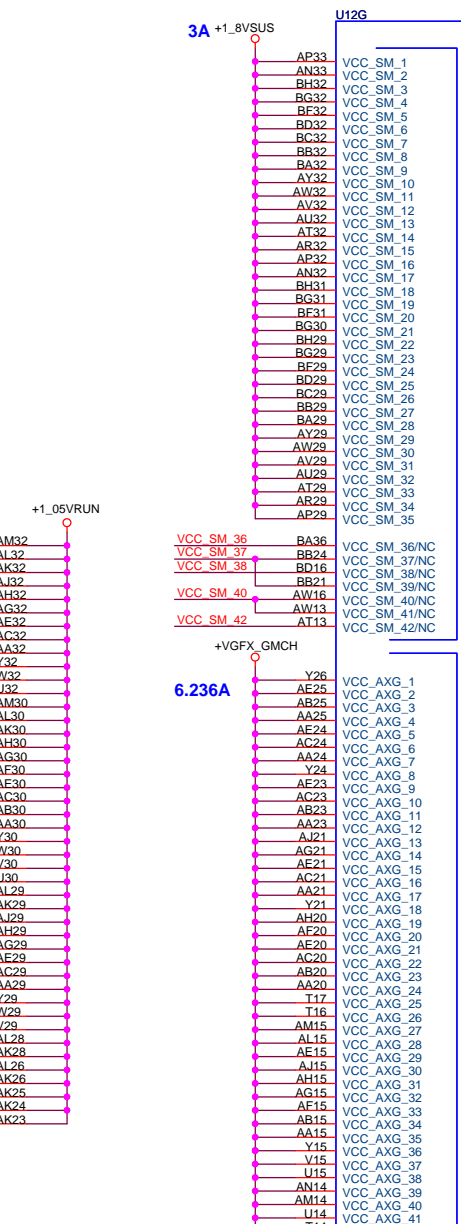
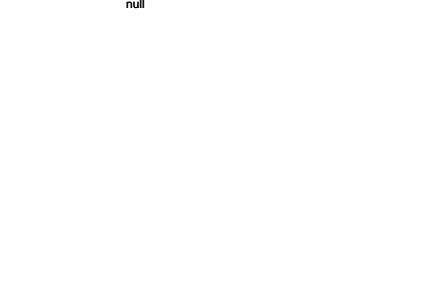
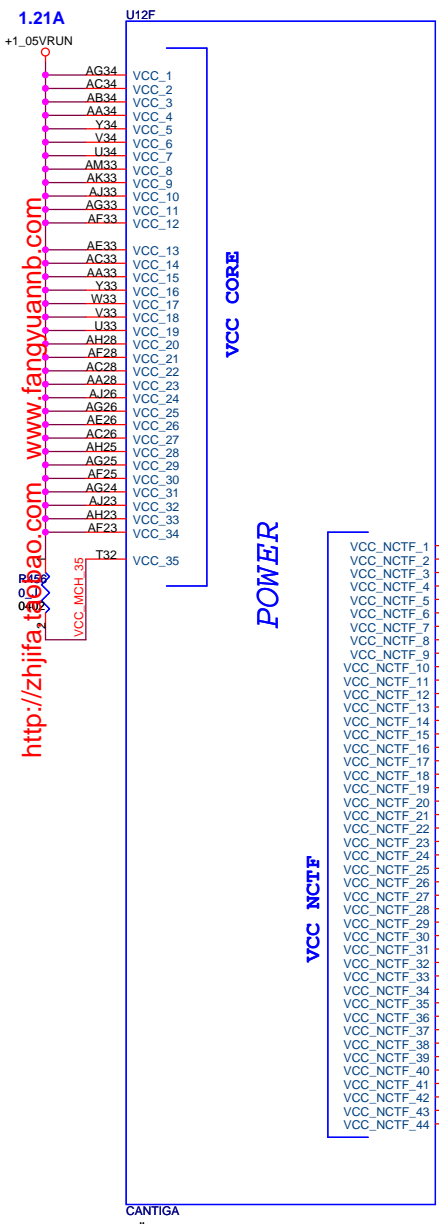
**DDR SYSTEM MEMORY B**



CANTIGA  
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U121		VSS	
ALJ48	VSS_1	VSS_100	AM36
AR48	VSS_2	VSS_101	AE36
AL48	VSS_3	VSS_102	P36
BB47	VSS_4	VSS_103	L36
AW47	VSS_5	VSS_104	J36
AN47	VSS_6	VSS_105	F36
AF47	VSS_7	VSS_106	AE21
AD47	VSS_8	VSS_107	AH35
AB47	VSS_9	VSS_108	AA35
Y47	VSS_10	VSS_109	Y35
T47	VSS_11	VSS_110	J21
L47	VSS_12	VSS_111	T35
G47	VSS_13	VSS_112	BG20
BD46	VSS_14	VSS_113	AM34
BA46	VSS_15	VSS_114	AJ34
AY46	VSS_16	VSS_115	AF34
AV46	VSS_17	VSS_116	AE34
AR46	VSS_18	VSS_117	W34
AM46	VSS_19	VSS_118	Y20
V46	VSS_20	VSS_119	B34
R46	VSS_21	VSS_120	A34
P46	VSS_22	VSS_121	BG33
H46	VSS_23	VSS_122	BC33
F46	VSS_24	VSS_123	BA33
BF44	VSS_25	VSS_124	AV33
AH44	VSS_26	VSS_125	AR33
AD44	VSS_27	VSS_126	AL33
AA44	VSS_28	VSS_127	AH33
Y44	VSS_29	VSS_128	AB33
U44	VSS_30	VSS_129	P33
T44	VSS_31	VSS_130	L33
M44	VSS_32	VSS_131	H33
F44	VSS_33	VSS_132	N32
BC43	VSS_34	VSS_133	HTZ
AV43	VSS_35	VSS_134	C32
AM43	VSS_36	VSS_135	A31
J43	VSS_37	VSS_136	AN29
C43	VSS_38	VSS_137	T29
BG42	VSS_39	VSS_138	N29
AY42	VSS_40	VSS_139	K29
AT42	VSS_41	VSS_140	H29
AN42	VSS_42	VSS_141	F29
AE42	VSS_43	VSS_142	G16
N42	VSS_44	VSS_143	A29
L42	VSS_45	VSS_144	BG28
BD41	VSS_46	VSS_145	BD28
BU41	VSS_47	VSS_146	BA28
AM41	VSS_48	VSS_147	AV28
AH41	VSS_49	VSS_148	A15
AD41	VSS_50	VSS_149	AT28
AA41	VSS_51	VSS_150	AR28
Y41	VSS_52	VSS_151	AJ28
U41	VSS_53	VSS_152	AG28
T41	VSS_54	VSS_153	AE28
M41	VSS_55	VSS_154	BC13
G41	VSS_56	VSS_155	AB28
B41	VSS_57	VSS_156	Y28
BG40	VSS_58	VSS_157	P28
BB40	VSS_59	VSS_158	K28
AV40	VSS_60	VSS_159	H28
AM40	VSS_61	VSS_160	F28
E40	VSS_62	VSS_161	C28
AT39	VSS_63	VSS_162	N13
AM39	VSS_64	VSS_163	L13
AJ39	VSS_65	VSS_164	G13
AE39	VSS_66	VSS_165	E13
N39	VSS_67	VSS_166	BF26
L39	VSS_68	VSS_167	AH26
B39	VSS_69	VSS_168	AF26
BH38	VSS_70	VSS_169	AB26
BC38	VSS_71	VSS_170	AA26
BA38	VSS_72	VSS_171	C26
AU38	VSS_73	VSS_172	B26
AH38	VSS_74	VSS_173	BH25
AD38	VSS_75	VSS_174	BD25
AA38	VSS_76	VSS_175	BB25
Y38	VSS_77	VSS_176	AV25
U38	VSS_78	VSS_177	AR25
T38	VSS_79	VSS_178	AC25
F38	VSS_80	VSS_179	Y25
C38	VSS_81	VSS_180	N25
BF37	VSS_82	VSS_181	L25
BB37	VSS_83	VSS_182	J25
AW37	VSS_84	VSS_183	G11
AT37	VSS_85	VSS_184	E25
AN37	VSS_86	VSS_185	BF24
AJ37	VSS_87	VSS_186	AD12
H37	VSS_88	VSS_187	AY24
C37	VSS_89	VSS_188	AT24
BG36	VSS_90	VSS_189	AJ24
BD36	VSS_91	VSS_190	AE10
AK15L	VSS_92	VSS_191	AA10
AU36	VSS_93	VSS_192	M10
	VSS_94	VSS_193	BF9
	VSS_95	VSS_194	BC9
	VSS_96	VSS_195	AN9
	VSS_97	VSS_196	AM9
	VSS_98	VSS_197	J24
	VSS_99	VSS_198	G24
		VSS_199	B9
			BH8
			BB8
			AV8
			AT8

CANTIGA null

U12J		VSS	
BG21	VSS_199	VSS_297	AH8
L12	VSS_200	VSS_298	Y8
AW21	VSS_201	VSS_299	LR
AU21	VSS_202	VSS_300	E8
AP21	VSS_203	VSS_301	B8
AN21	VSS_204	VSS_302	AY7
AH21	VSS_205	VSS_303	AU7
AE21	VSS_206	VSS_304	AN7
AB21	VSS_207	VSS_305	AJ7
R21	VSS_208	VSS_306	AE7
M21	VSS_209	VSS_307	AA7
J21	VSS_210	VSS_308	N7
G21	VSS_211	VSS_309	J7
BC20	VSS_212	VSS_310	BG6
BA20	VSS_213	VSS_311	BD6
AW20	VSS_214	VSS_312	AV6
AT20	VSS_215	VSS_313	AT6
AJ20	VSS_216	VSS_314	AM6
AG20	VSS_217	VSS_315	M6
W34	VSS_218	VSS_316	CS
Y20	VSS_219	VSS_317	BA5
N20	VSS_220	VSS_318	AH5
BG33	VSS_221	VSS_319	AD5
F20	VSS_222	VSS_320	Y5
C20	VSS_223	VSS_321	L5
AV33	VSS_224	VSS_322	J5
AR33	VSS_225	VSS_323	H5
AL33	VSS_226	VSS_324	F5
AH33	VSS_227	VSS_325	BE4
AB33	VSS_228		
P33	VSS_229	VSS_327	BC3
L33	VSS_230	VSS_328	AV3
H33	VSS_231	VSS_329	AL3
N32	VSS_232	VSS_330	R3
HTZ	VSS_233	VSS_331	P3
C32		VSS_332	F3
A31		VSS_333	BA2
AN29		VSS_334	AW2
T29		VSS_335	AU2
N29		VSS_336	AB2
K29		VSS_337	AP2
H29		VSS_338	AJ2
F29		VSS_339	AH2
G16		VSS_340	AE2
A29		VSS_341	AE2
BG28		VSS_342	AD2
BD28		VSS_343	AC2
BA28		VSS_344	Y2
AV28		VSS_345	M2
A15		VSS_346	K2
AT28		VSS_347	AM1
AR28		VSS_348	AA1
AJ28		VSS_349	H1
AG28		VSS_350	
AE28			
BC13			
AB28			
Y28			
P28			
K28		VSS_351	U24
H28		VSS_352	U28
F28		VSS_353	U25
C28		VSS_354	U29
N13			
L13			
G13			
E13			
BF26			
AH26			
AF26			
AB26			
AA26			
C26			
B26			
BH25			
BD25			
BB25			
AV25			
AR25			
AC25			
Y25			
N25			
L25			
J25			
G11			
E25			
BF24			
AD12			
AY24			
AT24			
AJ24			
AE10			
AA10			
M10			
BF9			
BC9			
AN9			
AM9			
J24			
G24			
B9			
BH8			
BB8			
AV8			
AT8			

CANTIGA null

VSS

VSS NCTF

VSS SCB

NC

VSS_NCTF_1	AF32
VSS_NCTF_2	AB32
VSS_NCTF_3	V32
VSS_NCTF_4	AJ30
VSS_NCTF_5	AM29
VSS_NCTF_6	AB29
VSS_NCTF_7	U26
VSS_NCTF_8	U23
VSS_NCTF_9	AL20
VSS_NCTF_10	V20
VSS_NCTF_11	AC19
VSS_NCTF_12	AL17
VSS_NCTF_13	AJ17
VSS_NCTF_14	P1
VSS_NCTF_15	AA17
VSS_NCTF_16	U17
VSS_SCB_1	BH48
VSS_SCB_2	BH1
VSS_SCB_3	A48
VSS_SCB_4	C1
VSS_SCB_5	A3
NC_26	E1
NC_27	D2
NC_28	C3
NC_29	B4
NC_30	A5
NC_31	A6
NC_32	A43
NC_33	A44
NC_34	B45
NC_35	C46
NC_36	D47
NC_37	B47
NC_38	A46
NC_39	F48
NC_40	E48
NC_41	C48
NC_42	B48

26MIL	TP89
26MIL	TP63
26MIL	TP64
26MIL	TP62
26MIL	TP61
26MIL	TP60
26MIL	TP73
26MIL	TP71
26MIL	TP84
26MIL	TP82
26MIL	TP90
26MIL	TP79
26MIL	TP88
26MIL	TP101
26MIL	TP96
26MIL	TP67
26MIL	TP80

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **Cantiga (VSS) 777**

Size: A3	Document Number: M750-1-01	Rev: 1.0
Date: Monday, June 23, 2008	Sheet: 13	of: 54

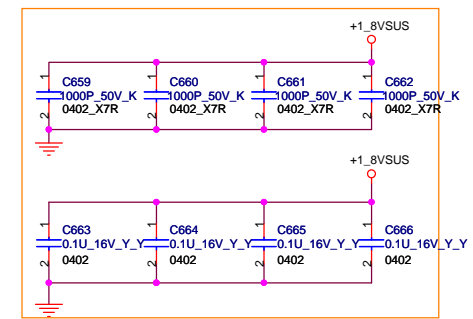
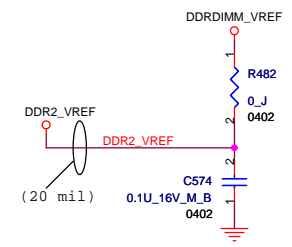
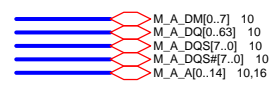


C573  
0.1U\_16V\_M\_B  
0402

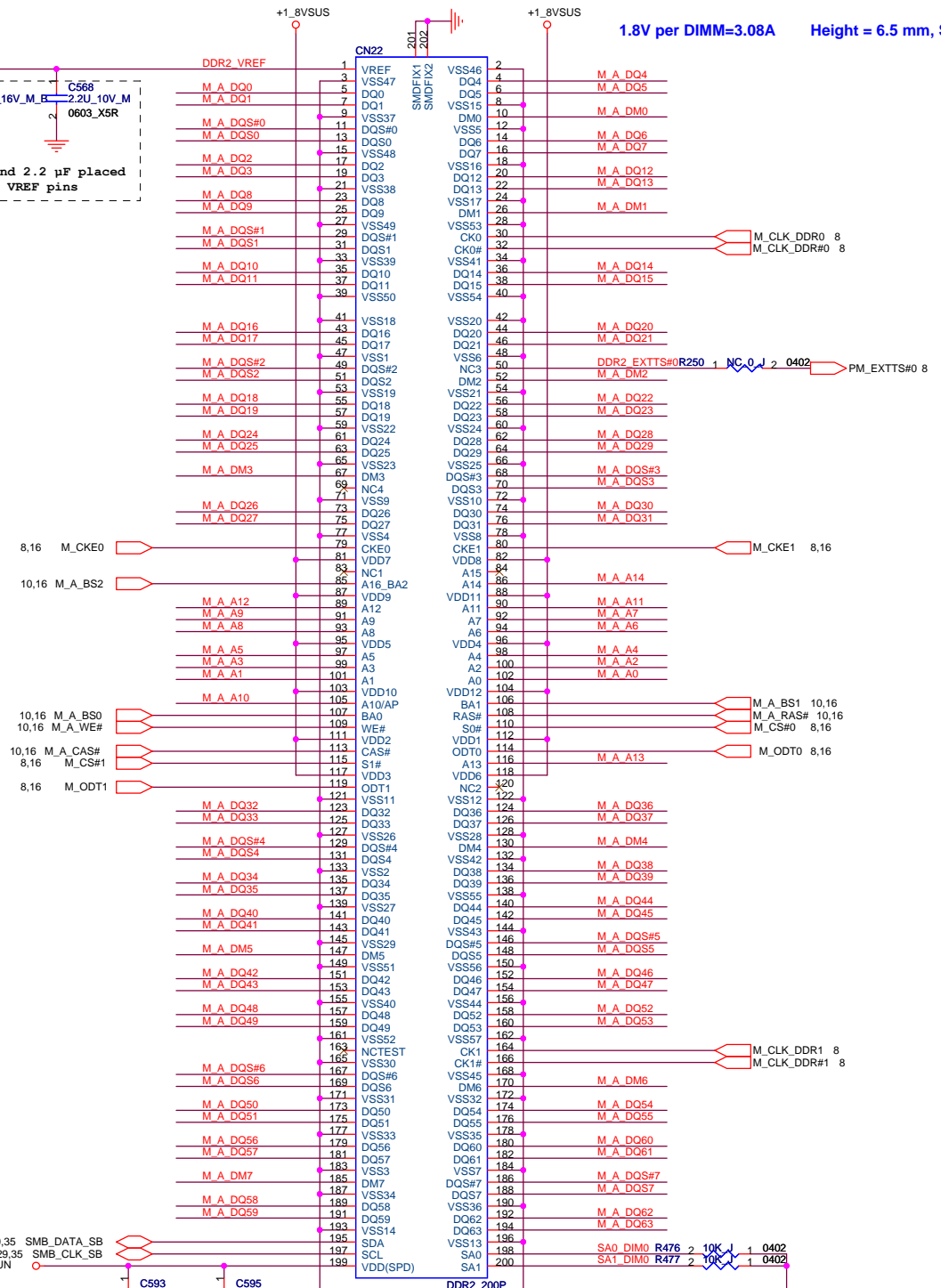
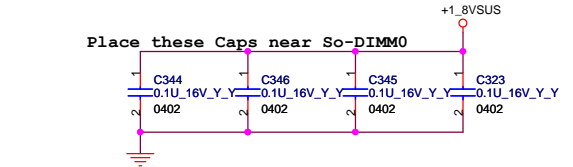
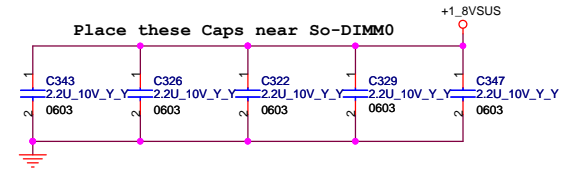
C568  
2.2U\_10V\_M  
0603\_X5R

0.1  $\mu$ F and 2.2  $\mu$ F placed close to VREF pins

1.8V per DIMM=3.08A Height = 6.5 mm, Standard Type

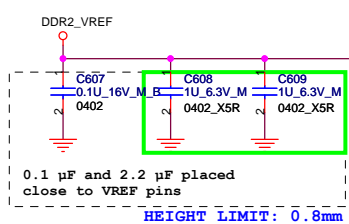


EVT2 11/09 Reserved For EMI. Place around +1.8VSUS plane.

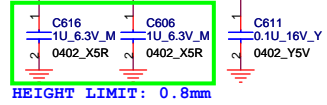
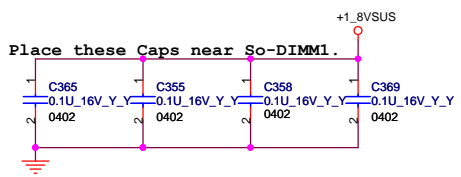
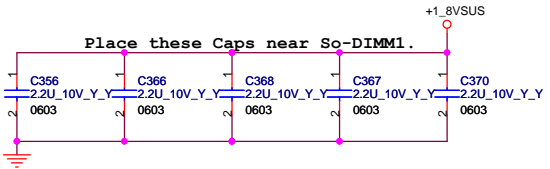
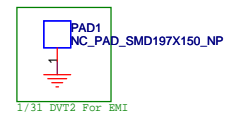
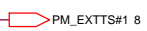
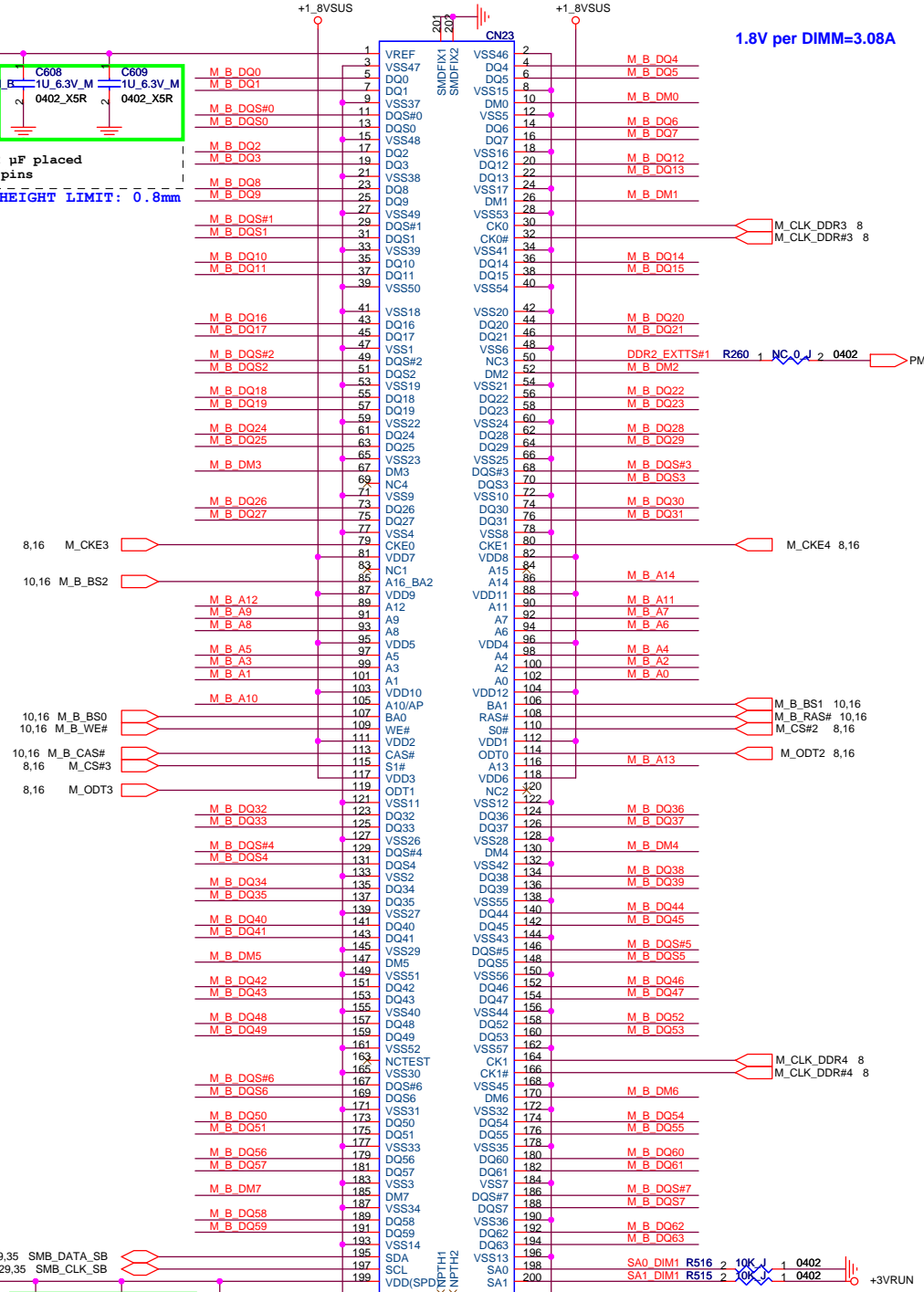
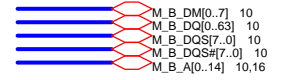


SMBus Address: A0H(W)/A1H(R)  
Place DIMM\_0 near GMCH

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>DDR(H)SO-DIMM_0</b>		CCPBG - R&D Division	
Size A3	Document Number M750-1-01	Rev 1.0	
Date: Monday, June 23, 2008	Sheet 14	of 54	

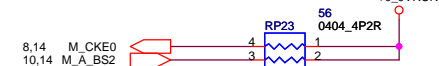
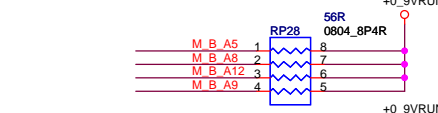
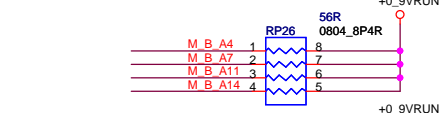
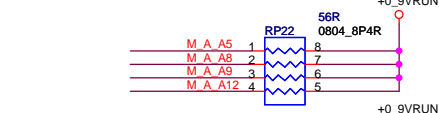
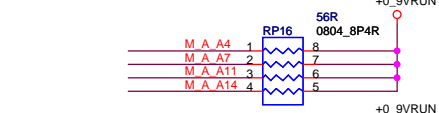
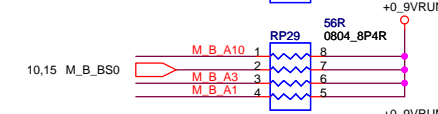
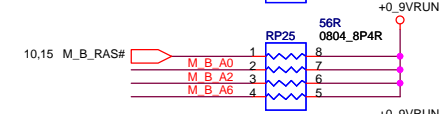
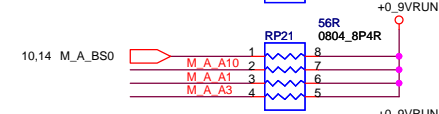
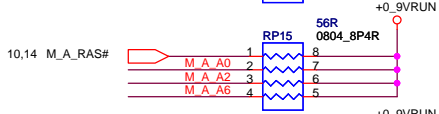
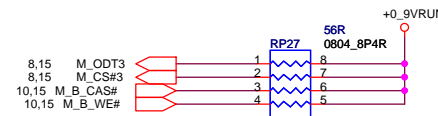
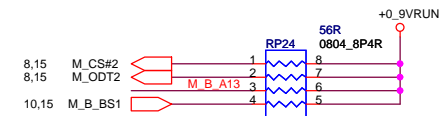
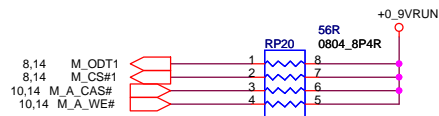
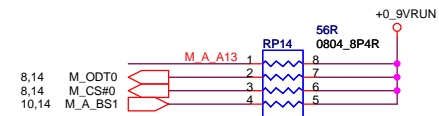
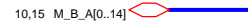
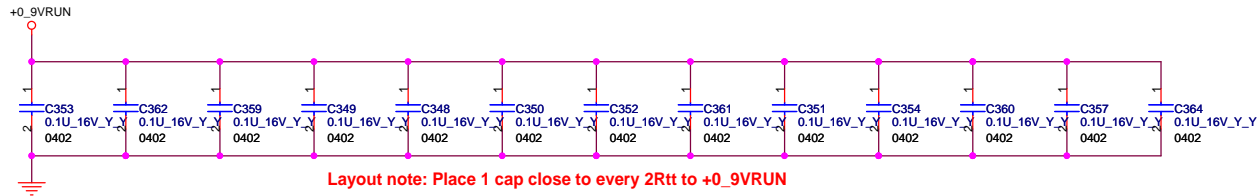
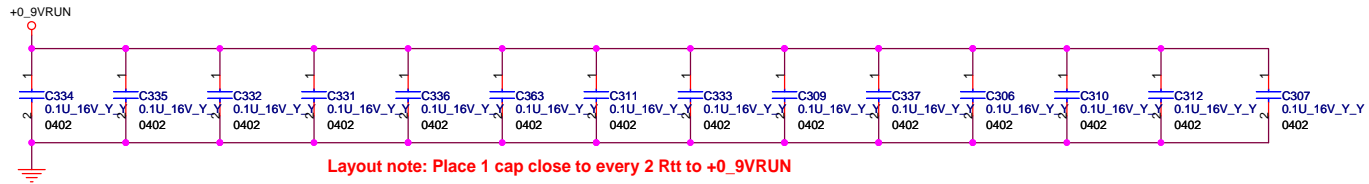


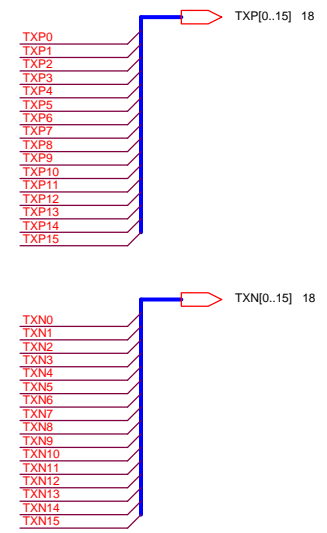
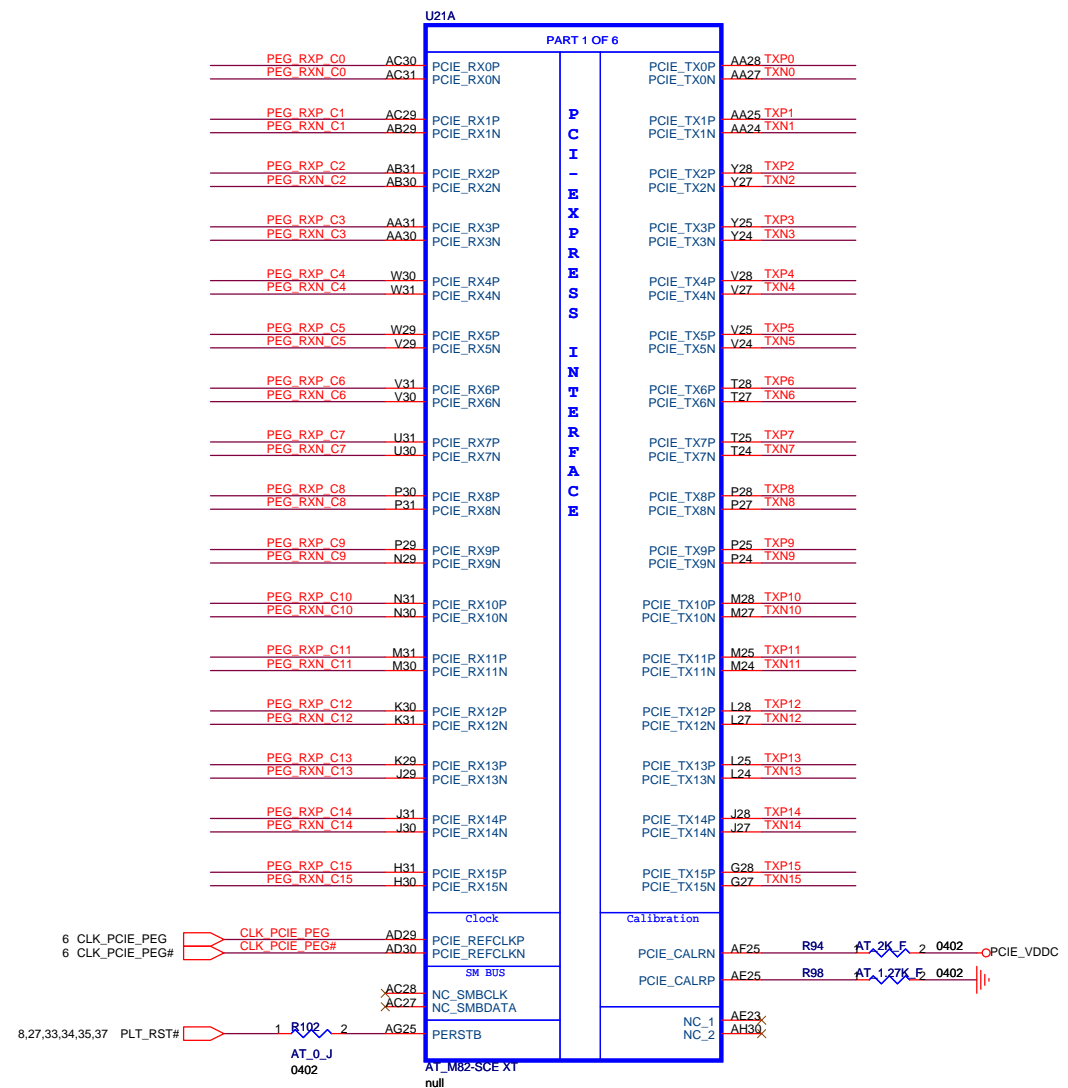
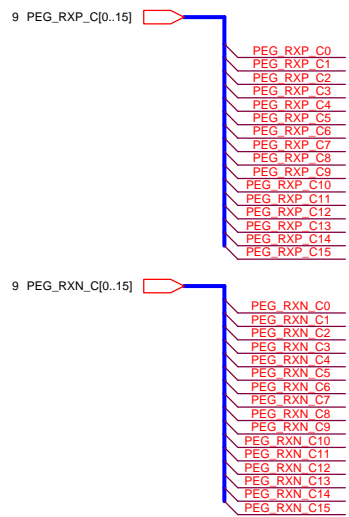
1.8V per DIMM=3.08A Height = 5.2mm, Reversed Type

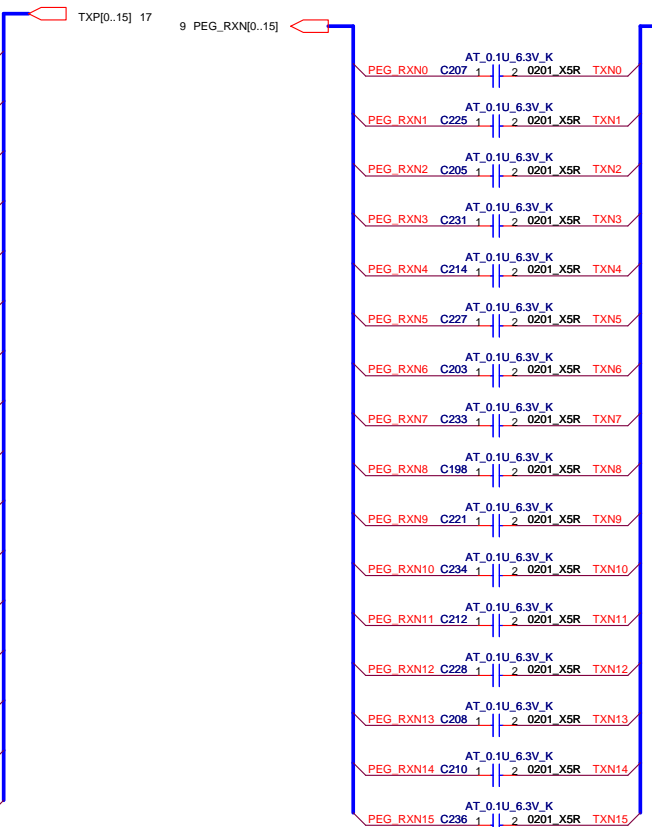
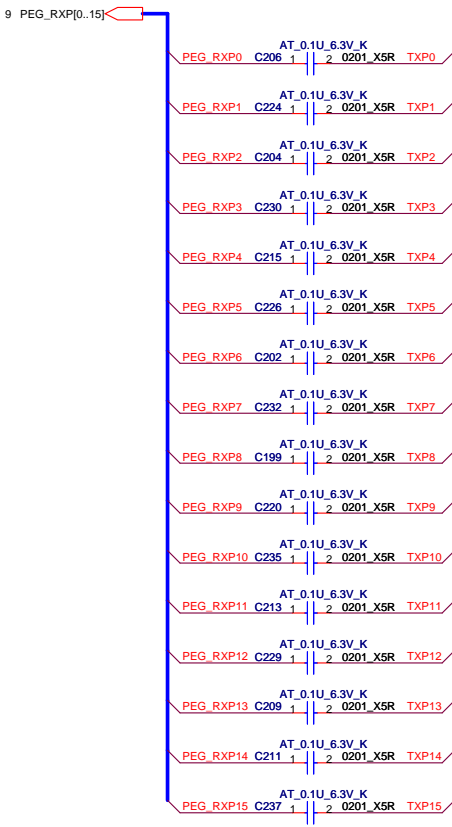


DDR2 SO-DIMM\_2x100P  
FOX\_AS0A426\_N2RN\_7F  
SMBus Address: A4(W)/A5(R)  
DIMM\_1 is placed farther from the GMCH than DIMM\_0







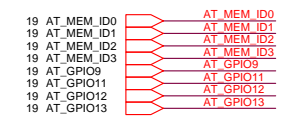
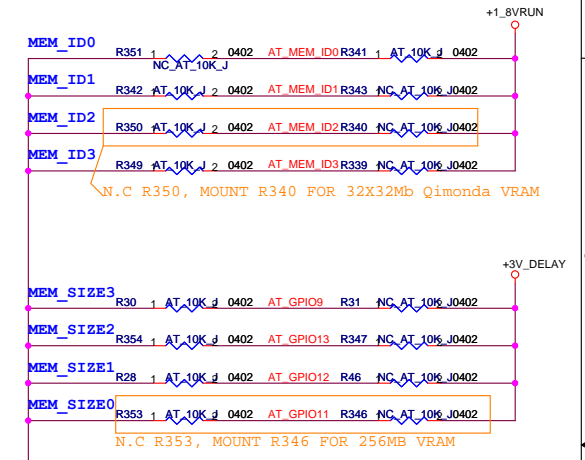


Strap for GDDR3-136ball  
 ATL\_DVPDATA[23 : 20 ]

0001 16Mx32 Qimonda  
 0010 16Mx32 Hynix  
 0011 16Mx32 Samsung  
 0101 32Mx32 Qimonda  
 0110 32Mx32 Hynix  
 0111 32Mx32 Samsung

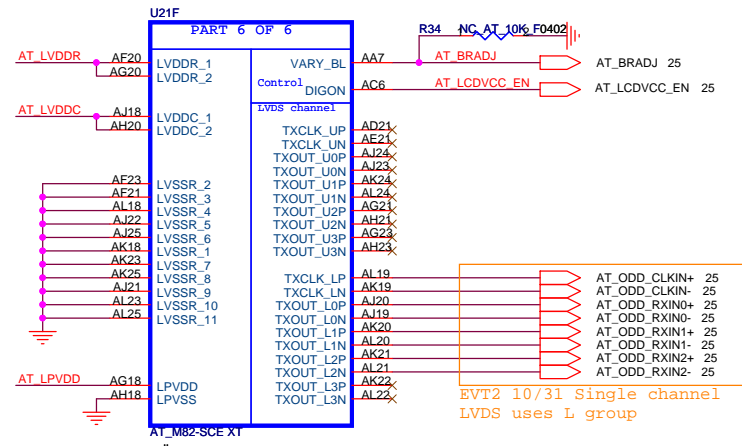
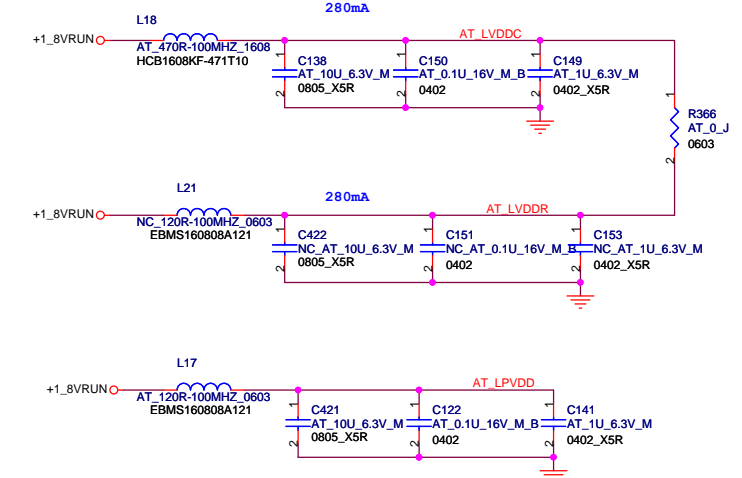
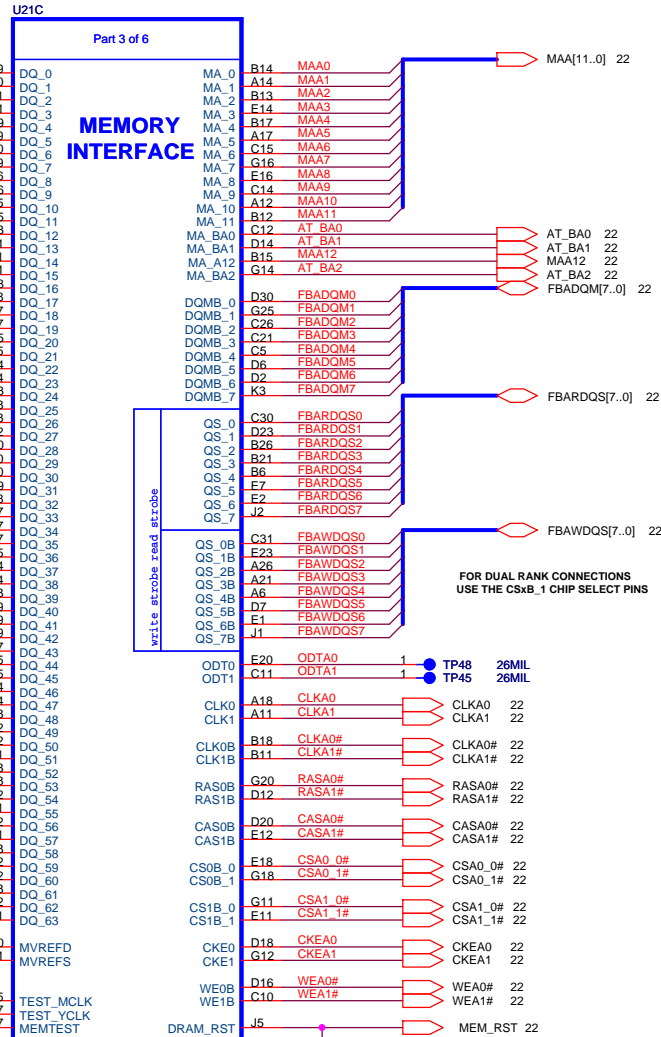
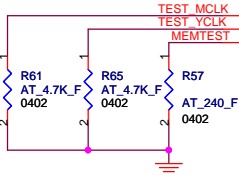
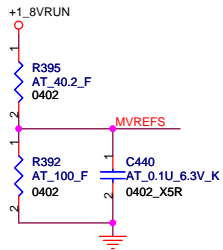
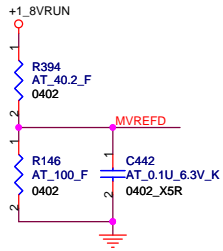
If no ROM attached, GPIO[9:13:12:11]  
 CONFIG(3:0)  
 controls the memory aperture size.

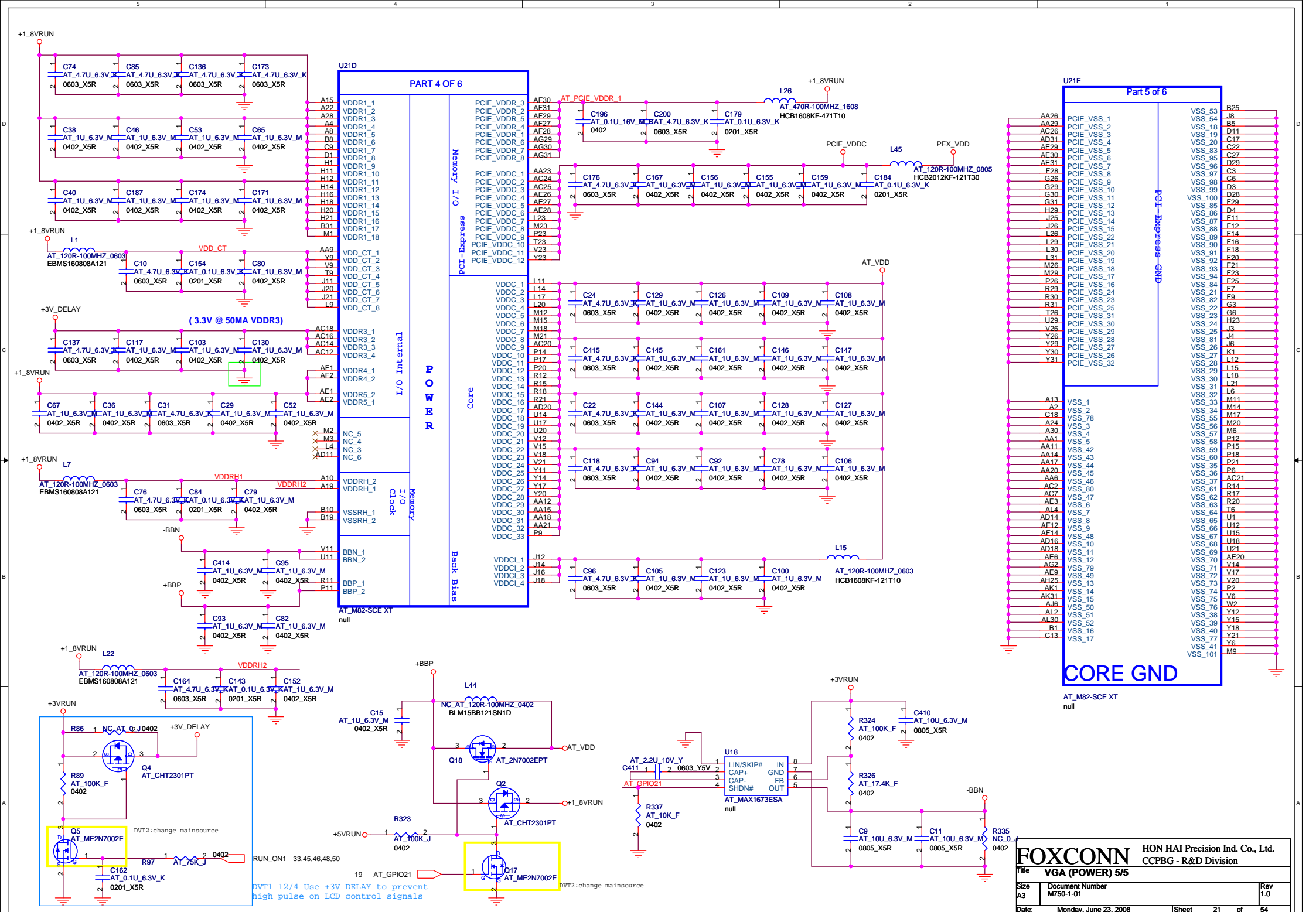
128MB	X000
256MB	X001
64MB	X010
32MB	X011
512MB	X100
1GB	X101
2GB	X110
4GB	X111

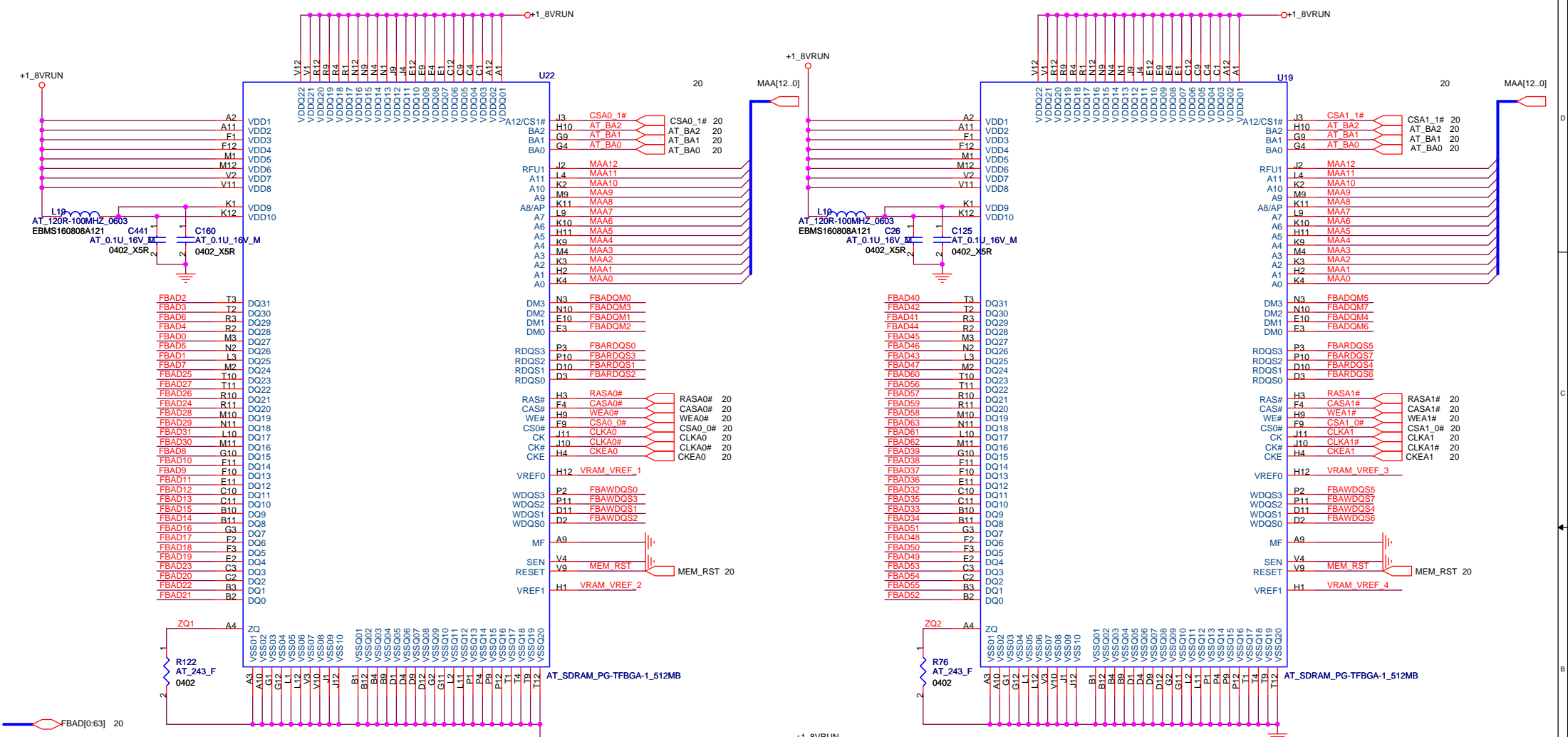




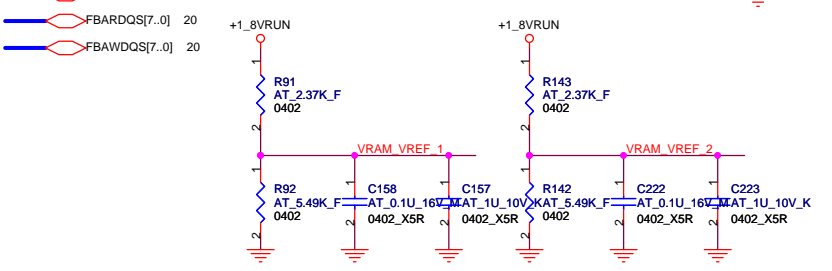
PLACE MVREF DIVIDERS  
AND CAPS CLOSE TO ASIC





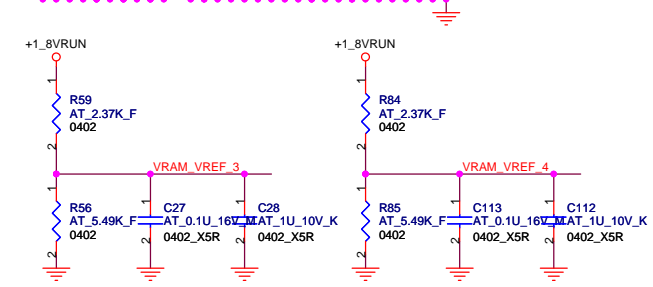


- FBAD[0:63] 20
- FBADQM[7:0] 20
- FBARDQS[7:0] 20
- FBAWDQS[7:0] 20



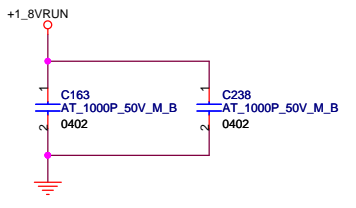
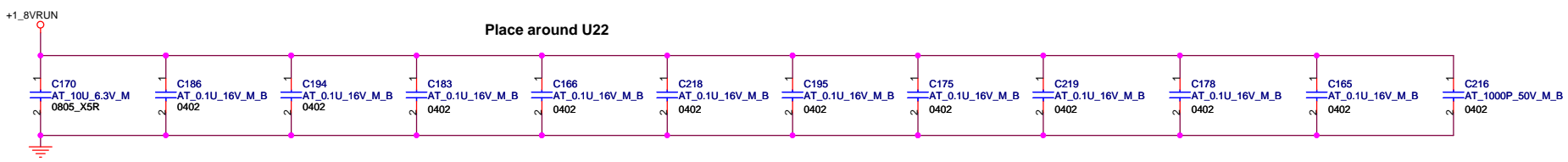
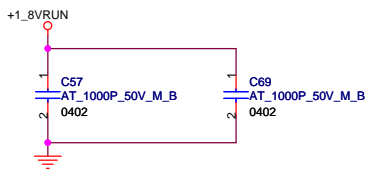
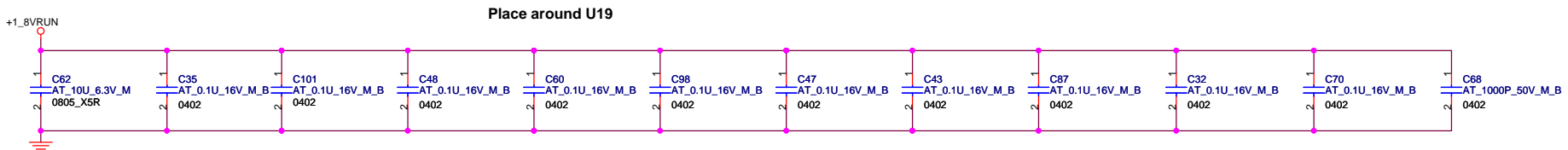
VRAM\_VREF is 70%VDDQ for GDDR3

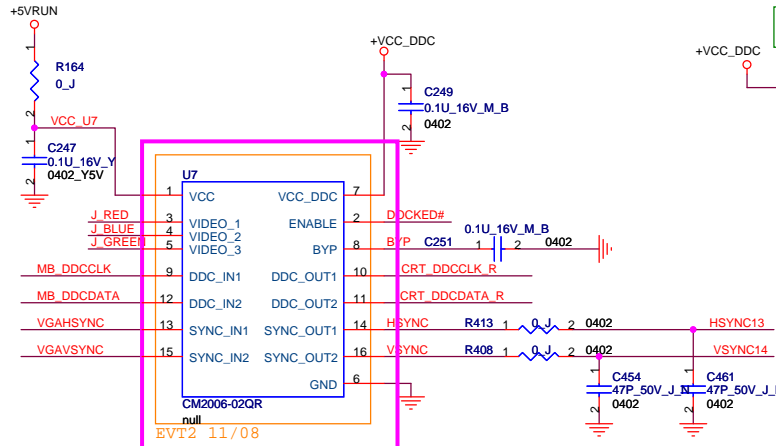
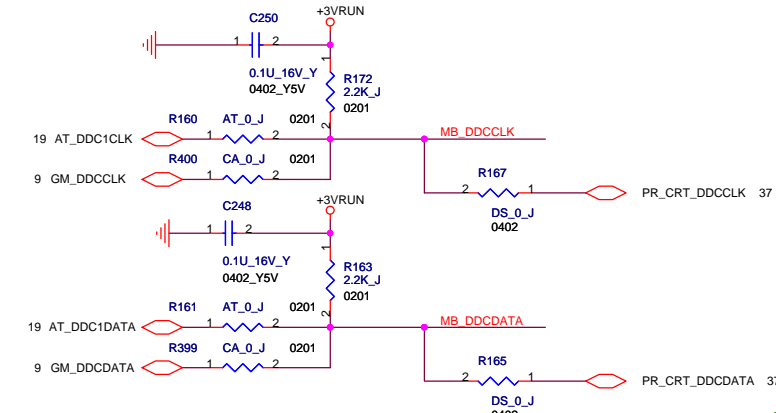
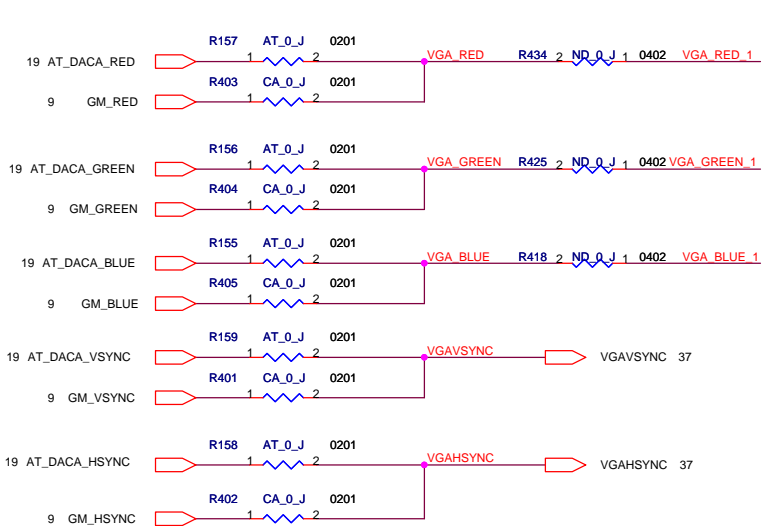
- RASA0# R130 AT 120 2 0402
- RASA1# R83 AT 20 2 0402
- CASA0# R120 AT 20 2 0402
- CASA1# R75 AT 20 2 0402
- WEA0# R117 AT 20 2 0402
- WEA1# R69 AT 20 2 0402
- CSA0 0#R118 AT 20 2 0402
- CSA1 0#R70 AT 20 2 0402
- CKEA0 R119 AT 20 2 0402
- CKEA1 R73 AT 20 2 0402
- CLKA0 R99 AT 20 2 0402
- CLKA0# R105 AT 20 2 0402
- CLKA1# R63 AT 20 2 0402
- CLKA1# R67 AT 20 2 0402
- CSA0 1#R133 AT 20 2 0402
- CSA1 1#R68 AT 20 2 0402



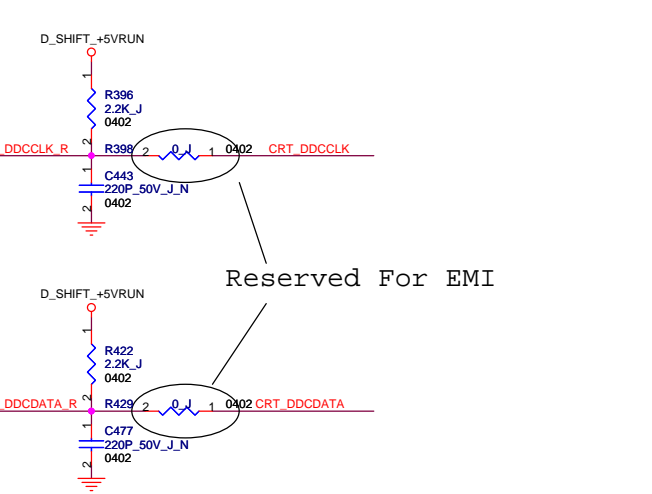
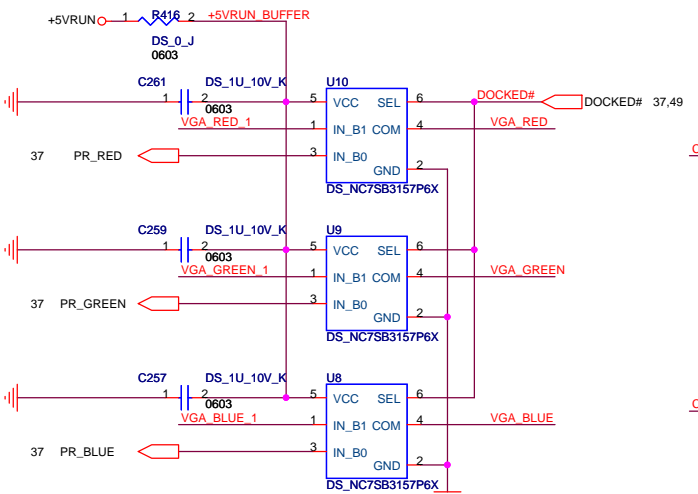
VRAM\_VREF is 70%VDDQ for GDDR3



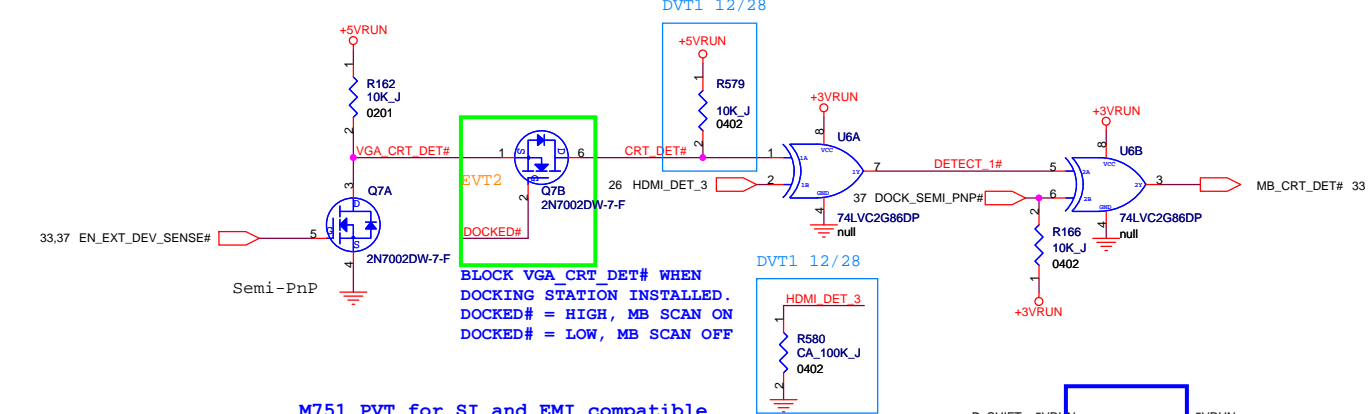




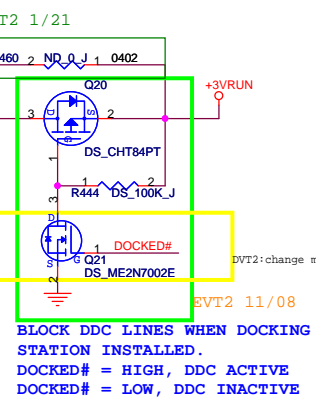
PVT update symbol to CM2006-02QR



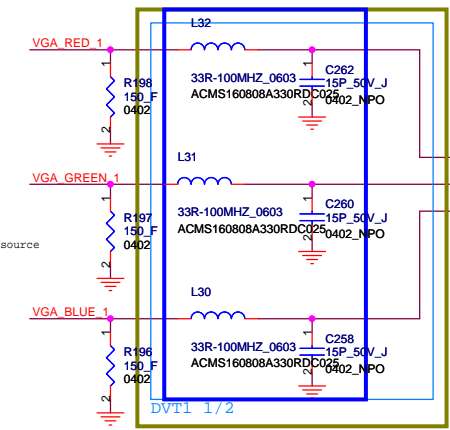
Reserved For EMI



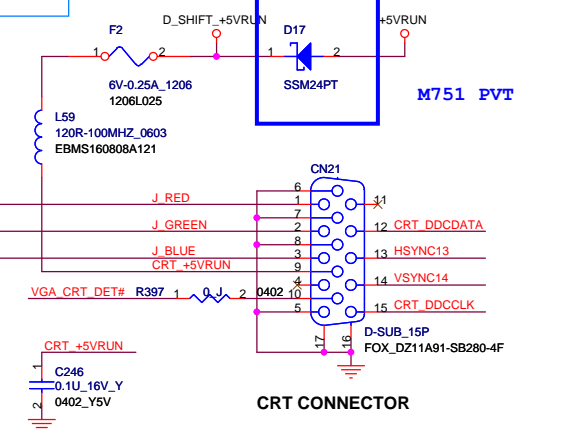
M751 PVT for SI and EMI compatible



BLOCK DDC LINES WHEN DOCKING STATION INSTALLED.  
DOCKED# = HIGH, DDC ACTIVE  
DOCKED# = LOW, DDC INACTIVE



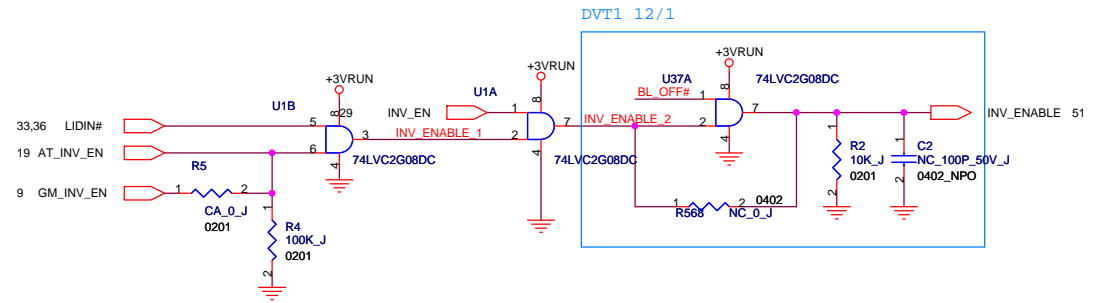
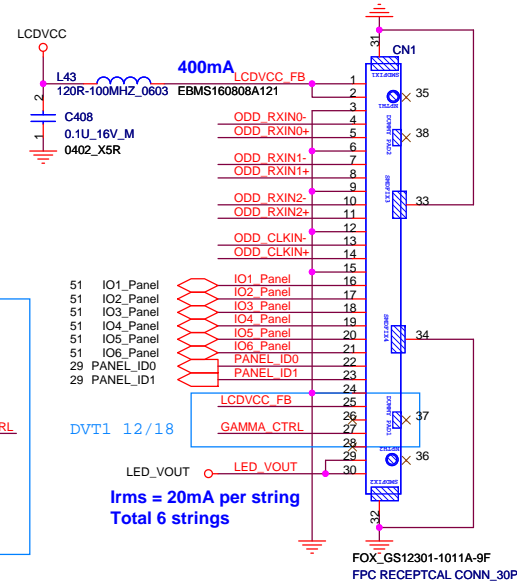
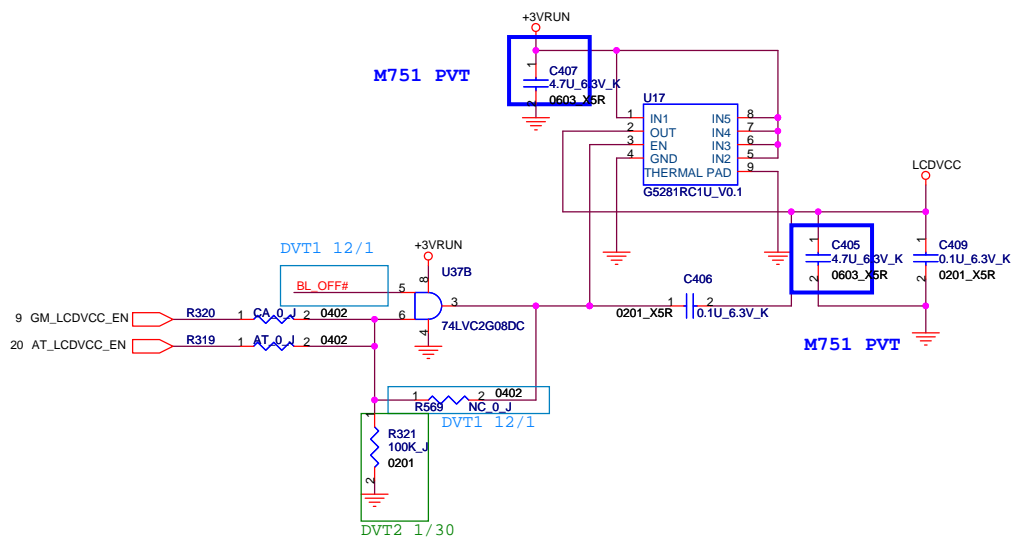
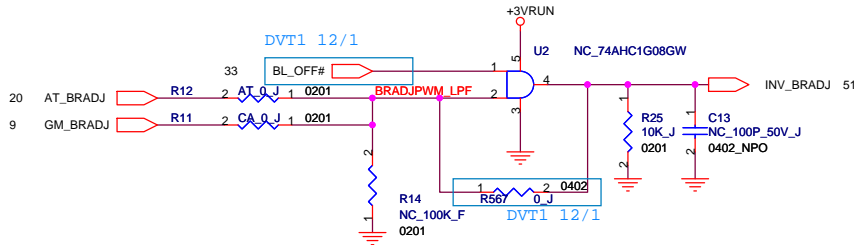
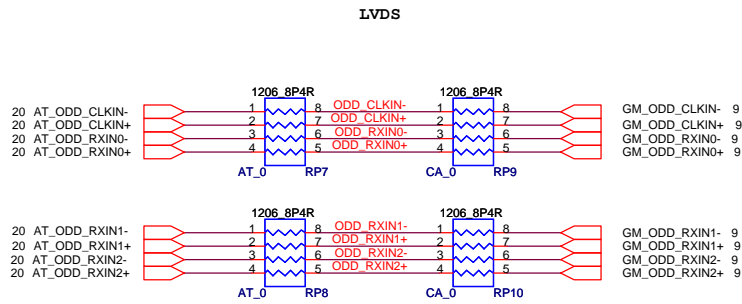
M751 DVT changed for EMI

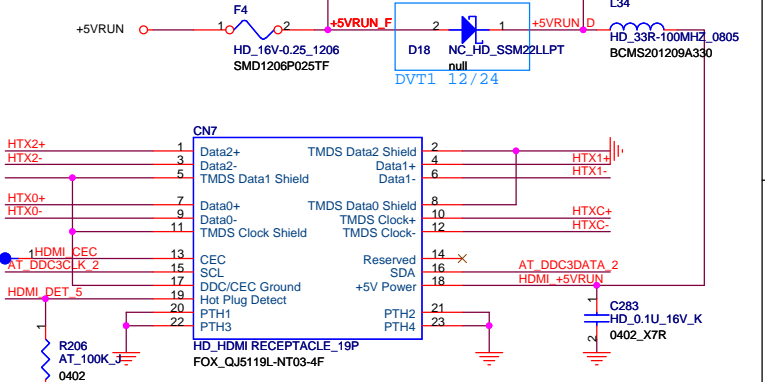
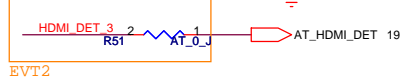
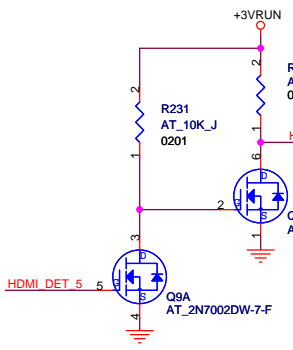
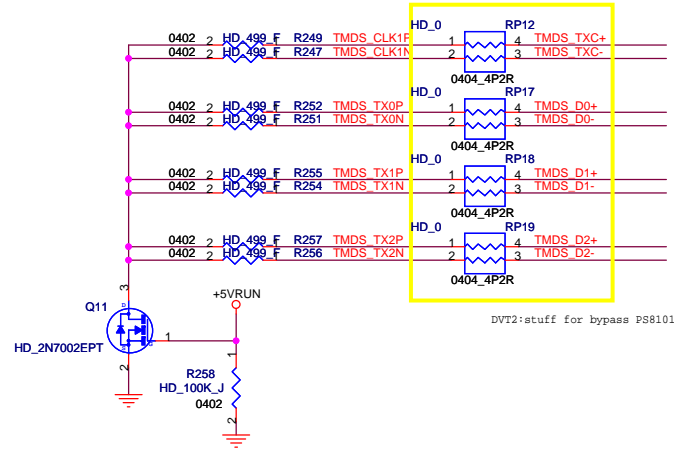
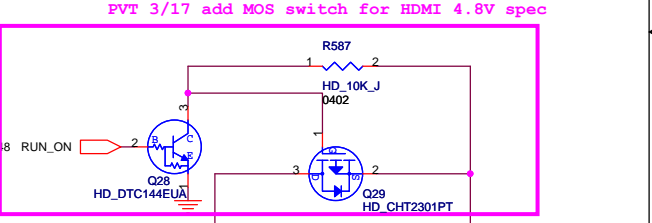
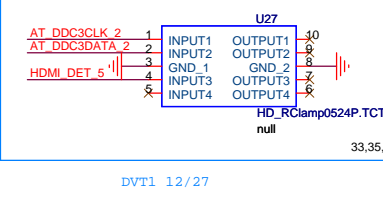
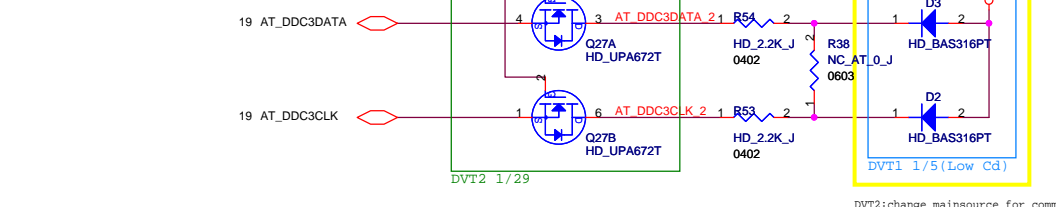
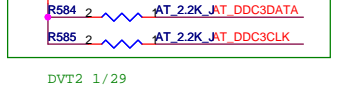
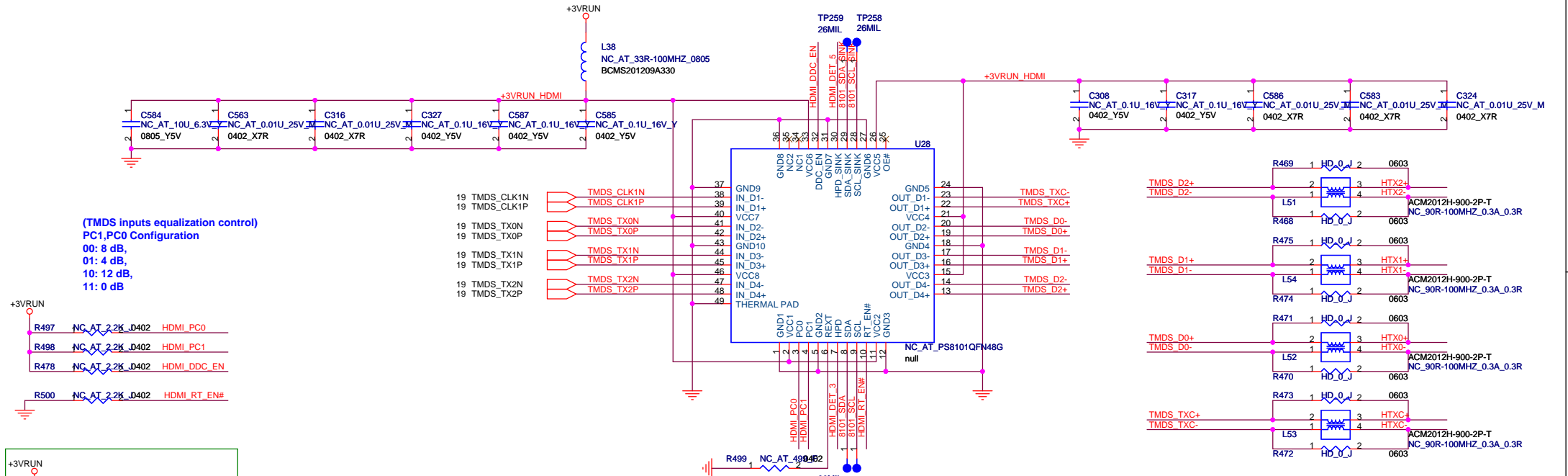


M751 PVT

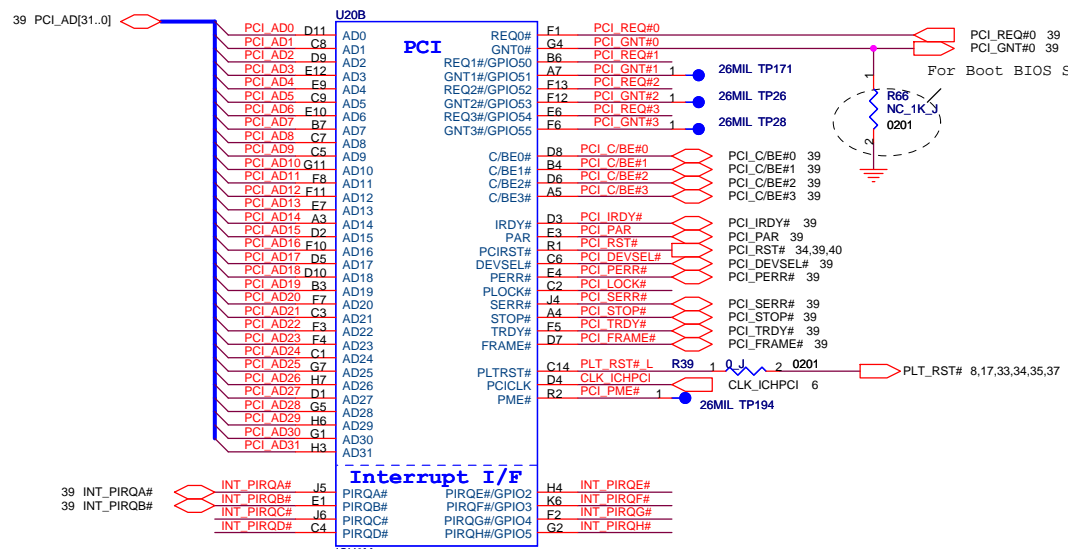
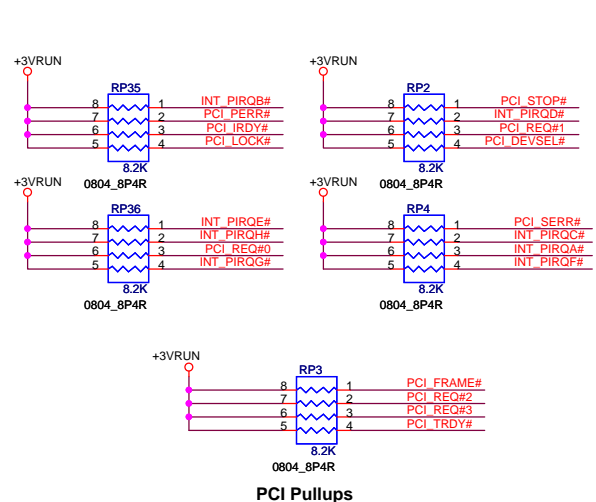
CRT CONNECTOR

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
File	<b>CRT</b>	
Size	Document Number	Rev
A3	M750-1-01	1.0
Date:	Thursday, June 26, 2008	Sheet 24 of 54



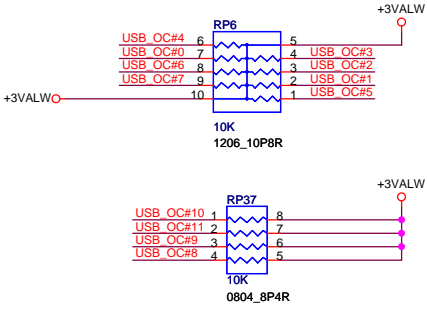
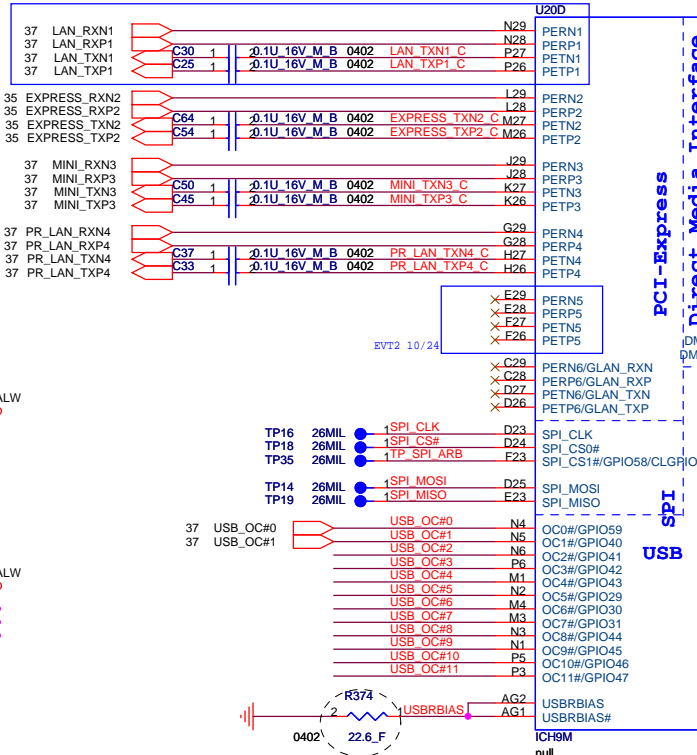


<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	<b>HDMI</b>	
Size	Document Number	Rev
A3	M750-1-01	1.0
Date	Monday, June 23, 2008	Sheet 26 of 54

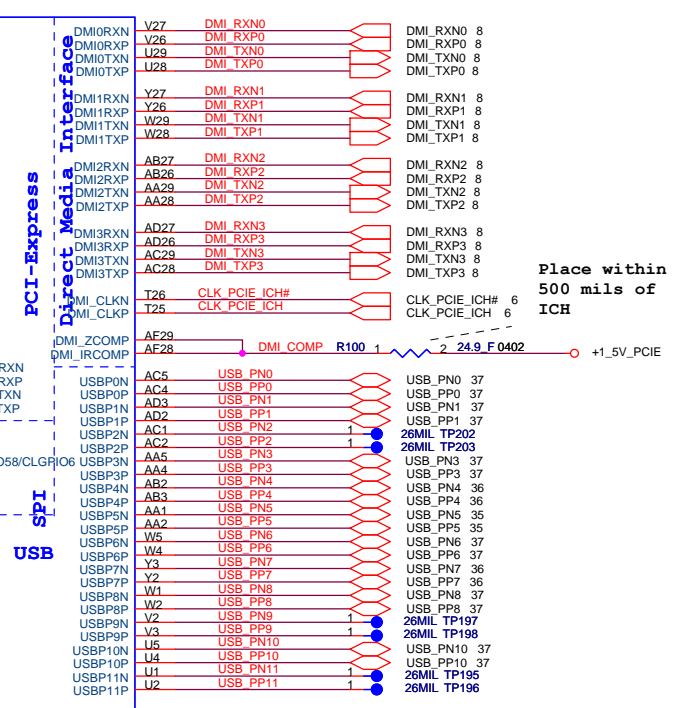


**Strap for Boot-BIOS**

	GNT#	SPI_CS#
JPC(Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI

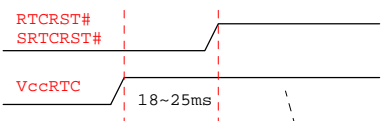


Place within 500 mils of ICH and don't route next to high speed signals



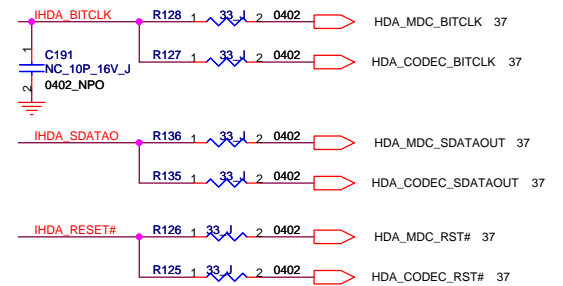
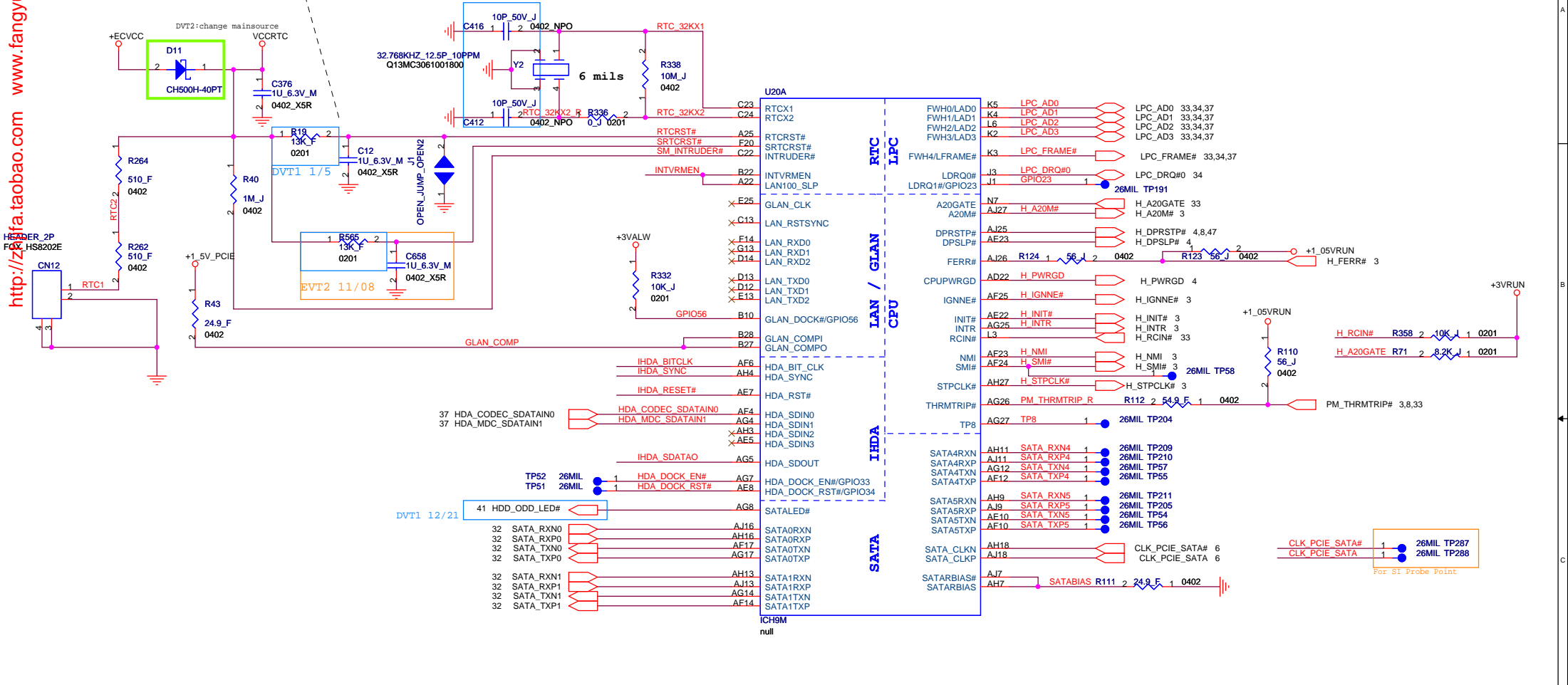
USB PORT	Function
PORT-0	SIDE-1
PORT-1	SIDE-2
PORT-2	x
PORT-3	Docking Hub
PORT-4	Bluetooth
PORT-5	ExpressCard
PORT-6	FingerPrint
PORT-7	Camera
PORT-8	Felica
PORT-9	x
PORT-10	Wimax
PORT-11	x

Place within 500 mils of ICH



Internal VRM enabled for VccSus1_05, VccSus1_5, VccCl1_5, VccLAN1_05 and VccCl1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)

The traces inside this block should be wider.  
DVT1 12/23

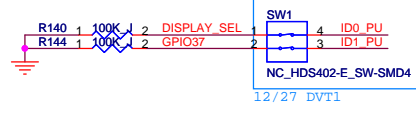
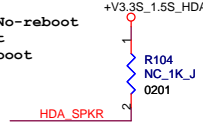
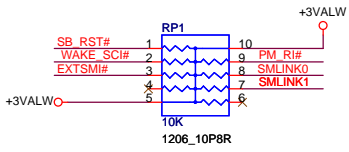


Stuff for No-reboot  
Low=Default  
High=No-reboot

SYSTEM ID0-3

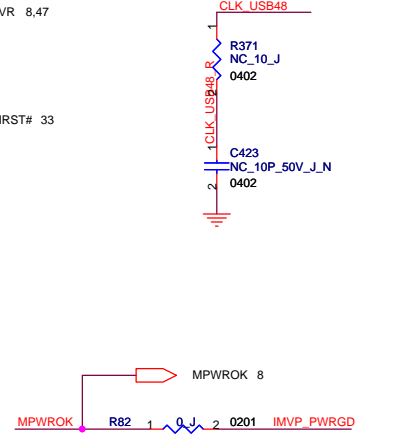
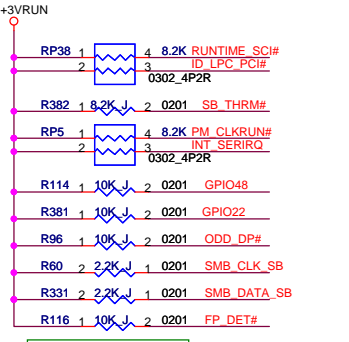
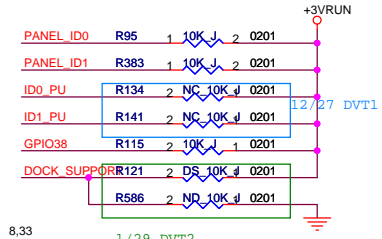
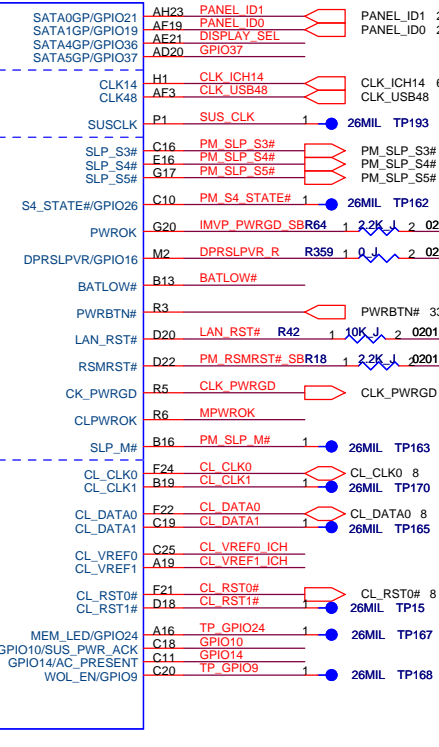
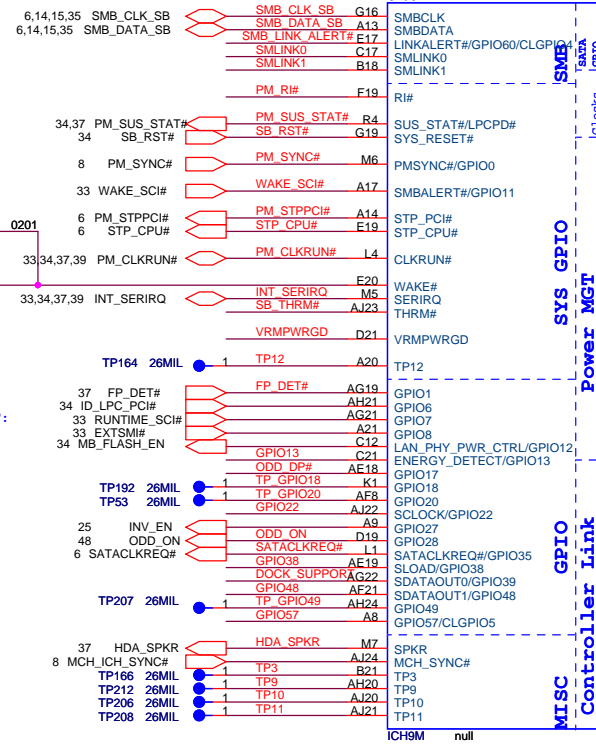
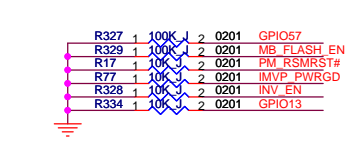
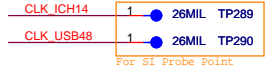
SW1: DISPLAY OUTOUT SELECTION  
(FOR DEBUG ONLY)

Dock Support  
Selection

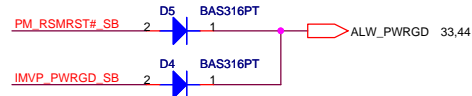
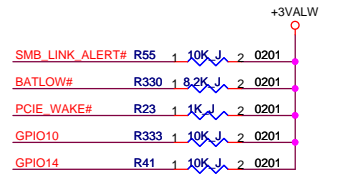
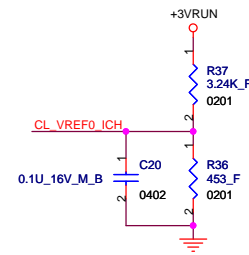
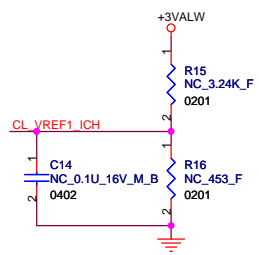
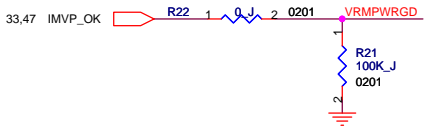
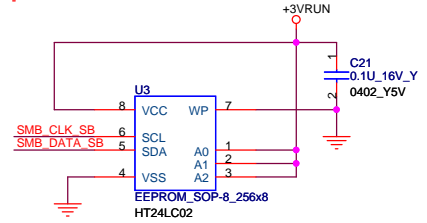


DISPLAY_SEL	
0	CRT
1	LVDS

	Dock Support
0	Not Support
1	Support



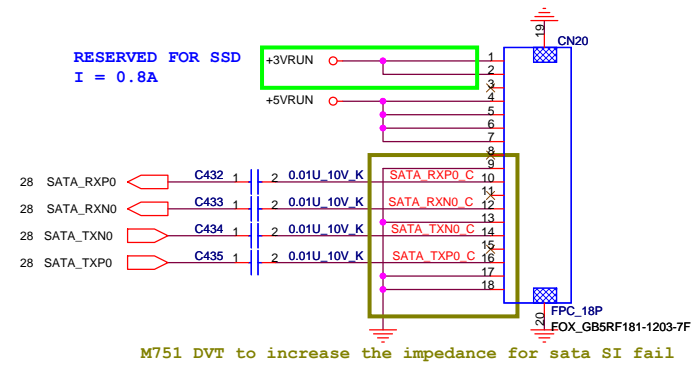
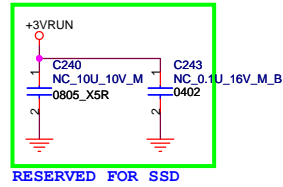
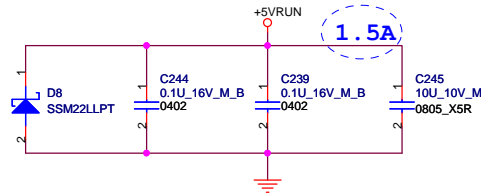
DVT2 1/26 If G3 -> S5 WOL is not supported, GPIO9/WOL\_EN can be connected to ground.



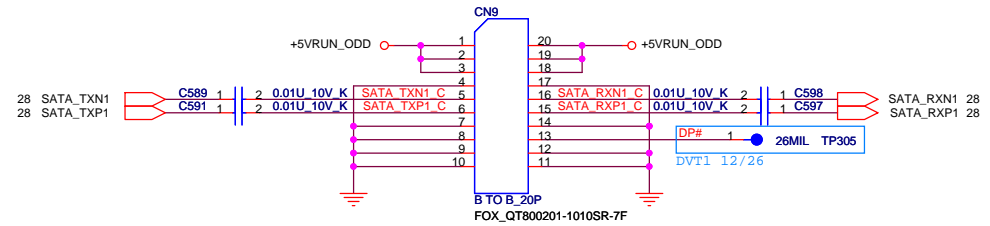
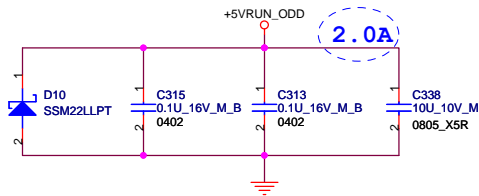




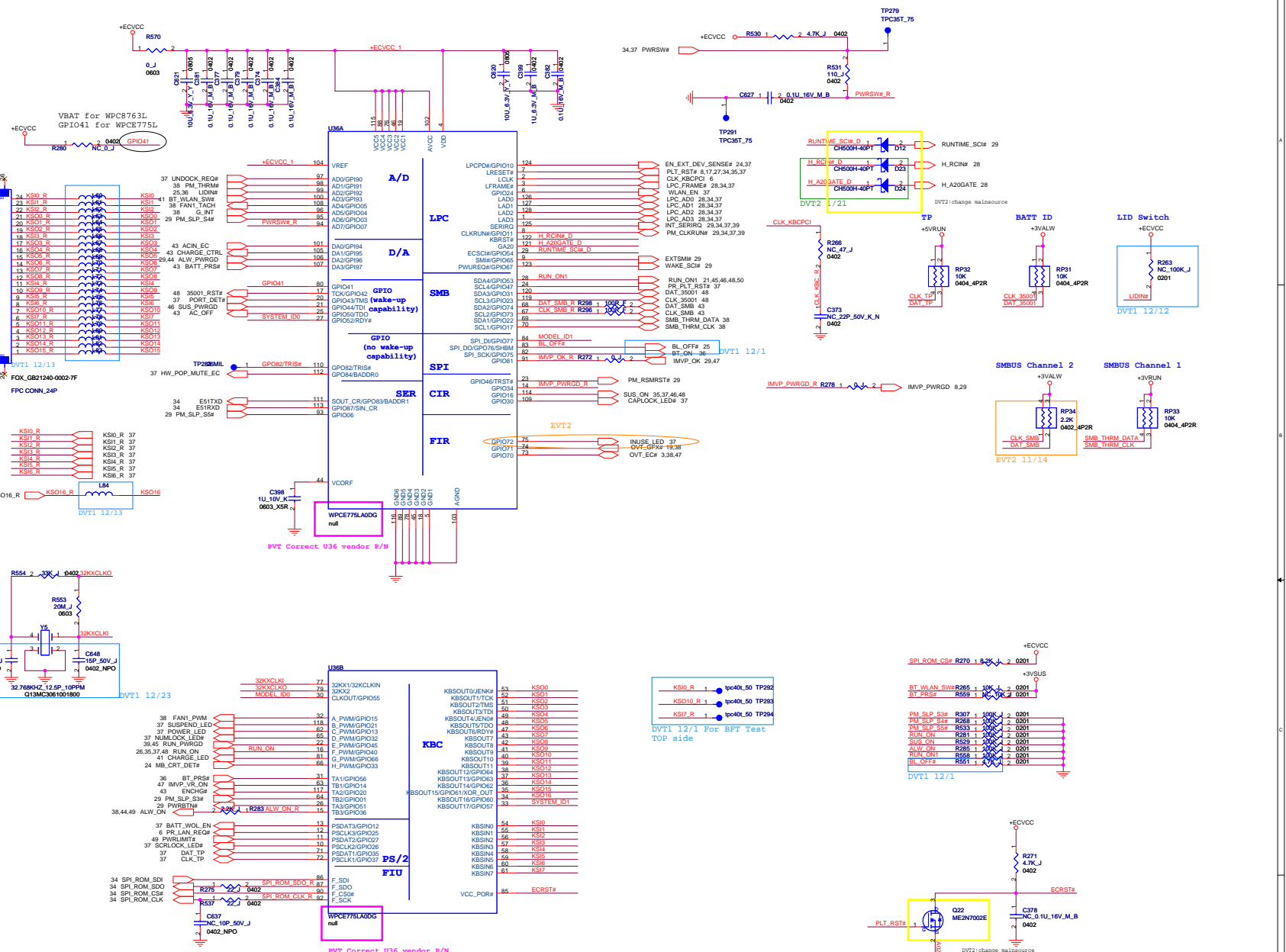
U20E		
AA26	VSS[001]	VSS[107]
AA27	VSS[002]	VSS[108]
AA3	VSS[003]	VSS[109]
AA6	VSS[004]	VSS[110]
AB1	VSS[005]	VSS[111]
AA23	VSS[006]	VSS[112]
AB28	VSS[007]	VSS[113]
AB29	VSS[008]	VSS[114]
AB4	VSS[009]	VSS[115]
AB5	VSS[010]	VSS[116]
AC17	VSS[011]	VSS[117]
AC26	VSS[012]	VSS[118]
AC27	VSS[013]	VSS[119]
AC3	VSS[014]	VSS[120]
AD1	VSS[015]	VSS[121]
AD10	VSS[016]	VSS[122]
AD12	VSS[017]	VSS[123]
AD13	VSS[018]	VSS[124]
AD14	VSS[019]	VSS[125]
AD17	VSS[020]	VSS[126]
AD18	VSS[021]	VSS[127]
AD21	VSS[022]	VSS[128]
AD28	VSS[023]	VSS[129]
AD29	VSS[024]	VSS[130]
AD4	VSS[025]	VSS[131]
AD5	VSS[026]	VSS[132]
AD6	VSS[027]	VSS[133]
AD7	VSS[028]	VSS[134]
AD9	VSS[029]	VSS[135]
AE12	VSS[030]	VSS[136]
AE13	VSS[031]	VSS[137]
AE14	VSS[032]	VSS[138]
AE16	VSS[033]	VSS[139]
AE17	VSS[034]	VSS[140]
AE2	VSS[035]	VSS[141]
AE20	VSS[036]	VSS[142]
AE24	VSS[037]	VSS[143]
AE3	VSS[038]	VSS[144]
AE4	VSS[039]	VSS[145]
AE6	VSS[040]	VSS[146]
AE9	VSS[041]	VSS[147]
AF13	VSS[042]	VSS[148]
AF16	VSS[043]	VSS[149]
AF18	VSS[044]	VSS[150]
AF22	VSS[045]	VSS[151]
AH26	VSS[046]	VSS[152]
AF26	VSS[047]	VSS[153]
AF27	VSS[048]	VSS[154]
AF5	VSS[049]	VSS[155]
AF7	VSS[050]	VSS[156]
AF9	VSS[051]	VSS[157]
AG13	VSS[052]	VSS[158]
AG18	VSS[053]	VSS[159]
AG18	VSS[054]	VSS[160]
AG20	VSS[055]	VSS[161]
AG23	VSS[056]	VSS[162]
AG3	VSS[057]	VSS[163]
AG6	VSS[058]	VSS[164]
AG9	VSS[059]	VSS[165]
AH12	VSS[060]	VSS[166]
AH14	VSS[061]	VSS[167]
AH17	VSS[062]	VSS[168]
AH19	VSS[063]	VSS[169]
AH2	VSS[064]	VSS[170]
AH22	VSS[065]	VSS[171]
AH25	VSS[066]	VSS[172]
AH28	VSS[067]	VSS[173]
AH5	VSS[068]	VSS[174]
AH8	VSS[069]	VSS[175]
AJ12	VSS[070]	VSS[176]
AJ14	VSS[071]	VSS[177]
AJ17	VSS[072]	VSS[178]
AJ8	VSS[073]	VSS[179]
B11	VSS[074]	VSS[180]
B14	VSS[075]	VSS[181]
B17	VSS[076]	VSS[182]
B2	VSS[077]	VSS[183]
B20	VSS[078]	VSS[184]
B23	VSS[079]	VSS[185]
B5	VSS[080]	VSS[186]
B8	VSS[081]	VSS[187]
C26	VSS[082]	VSS[188]
C27	VSS[083]	VSS[189]
E11	VSS[084]	VSS[190]
E14	VSS[085]	VSS[191]
E18	VSS[086]	VSS[192]
E2	VSS[087]	VSS[193]
E21	VSS[088]	VSS[194]
E24	VSS[089]	VSS[195]
E5	VSS[090]	VSS[196]
E8	VSS[091]	VSS[197]
F16	VSS[092]	VSS[198]
F28	VSS[093]	VSS[199]
F29	VSS[094]	VSS[200]
G12	VSS[095]	VSS[201]
G14	VSS[096]	VSS[202]
G18	VSS[097]	VSS[203]
G21	VSS[098]	VSS[204]
G24	VSS[099]	VSS[205]
G26	VSS[100]	VSS[206]
G27	VSS[101]	VSS[207]
G8	VSS[102]	VSS[208]
H2	VSS[103]	VSS[209]
H23	VSS[104]	VSS[210]
H28	VSS[105]	VSS[211]
H29	VSS[106]	VSS[212]
	VSS_NCTF[01]	A1
	VSS_NCTF[02]	A2
	VSS_NCTF[03]	A28
	VSS_NCTF[04]	A29
	VSS_NCTF[05]	AH1
	VSS_NCTF[06]	AH29
	VSS_NCTF[07]	AJ1
	VSS_NCTF[08]	AJ2
	VSS_NCTF[09]	AJ28
	VSS_NCTF[10]	AJ29
	VSS_NCTF[11]	B1
	VSS_NCTF[12]	B29
	ICH9M	
	null	



### SATA HDD CONN



### SATA ODD CONN

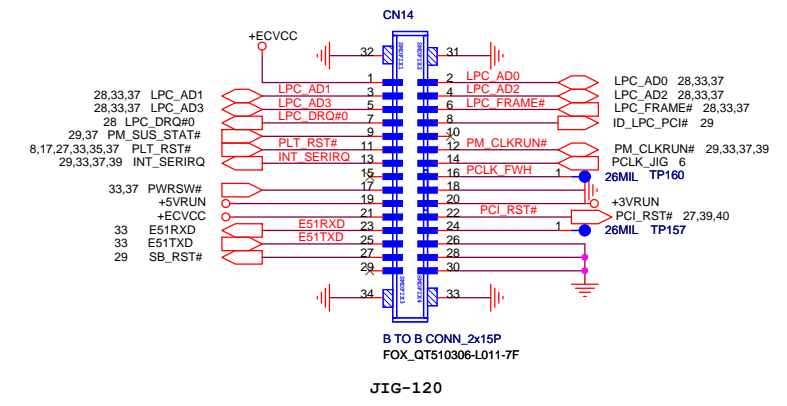
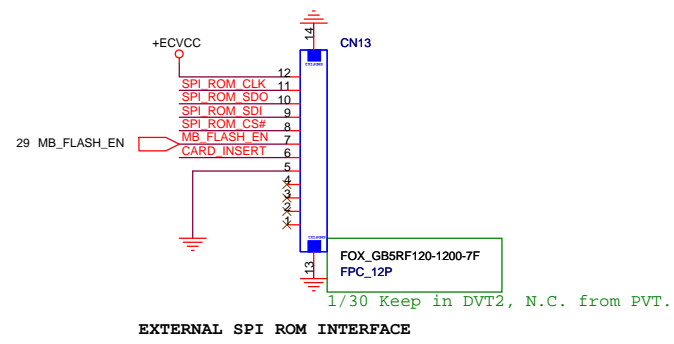
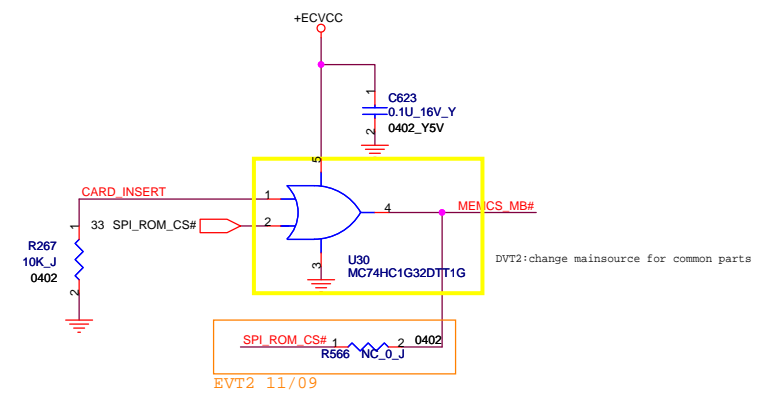
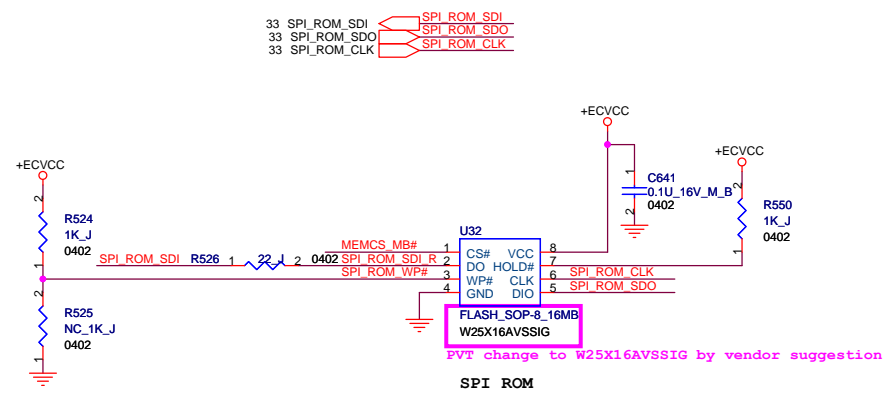


**MODEL ID0-1**

ID1	ID0	Sku	MODEL
0	0	UMA	
0	1	DISCRETE	M750

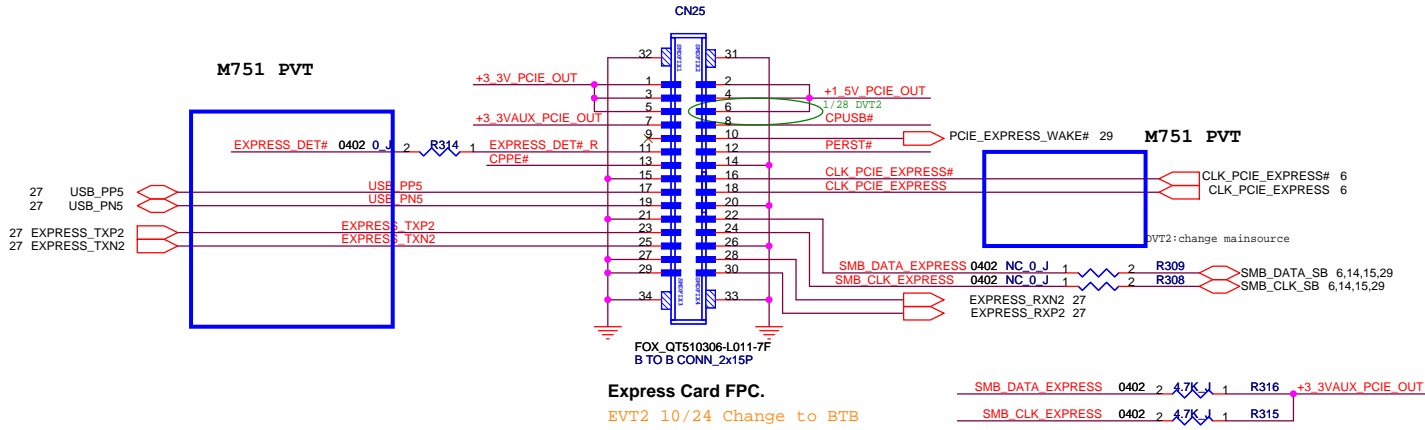
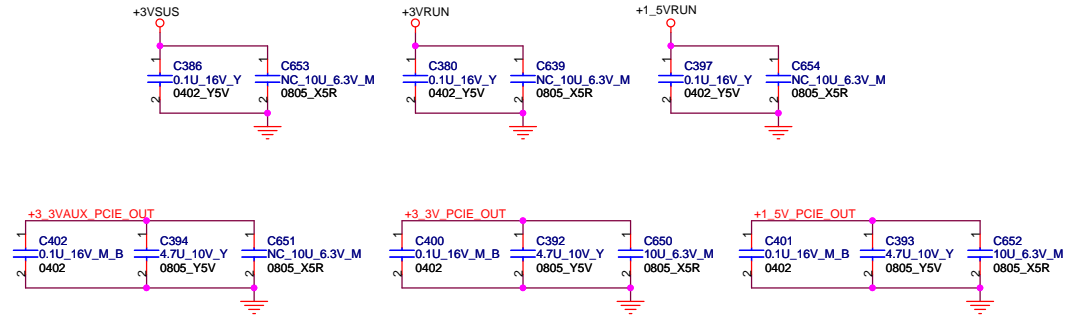
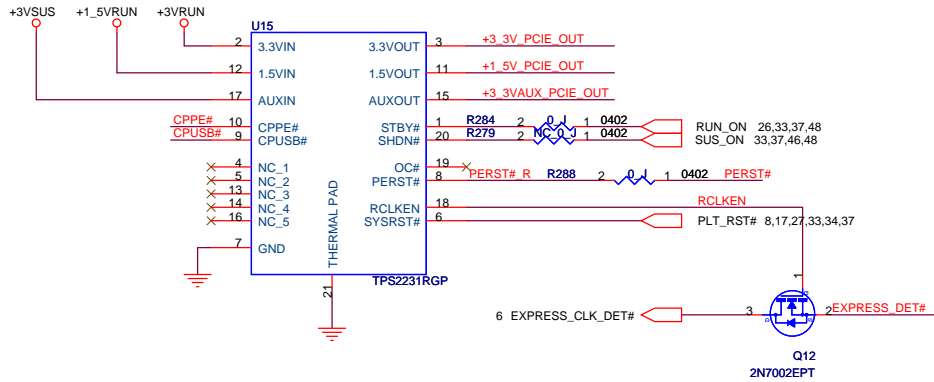
**SYSTEM ID0-1**

ID1	ID0	MODEL
0	0	M750
0	1	M751
1	0	M752



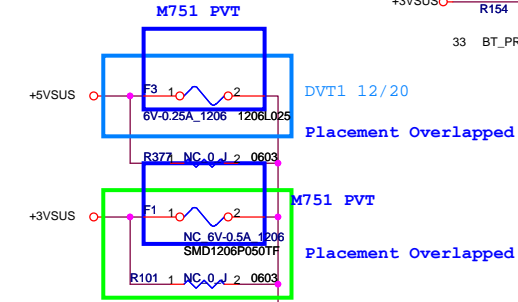
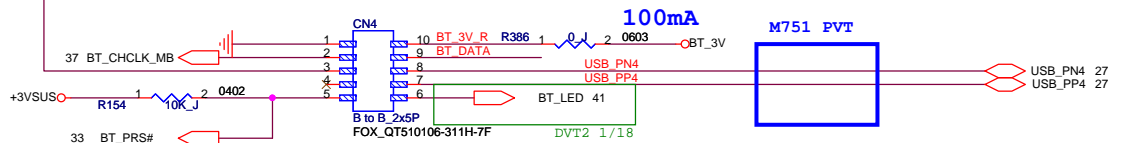
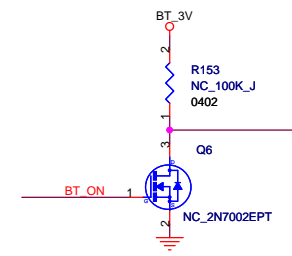
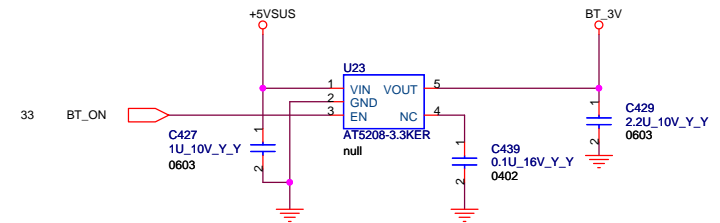
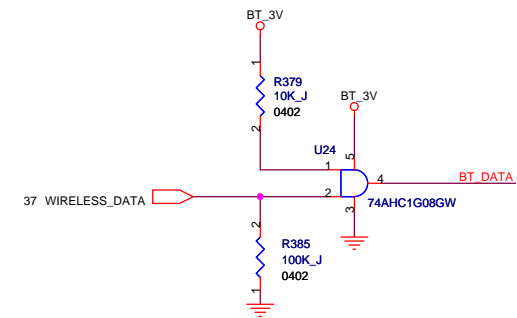
+1\_5V=>0.65A  
 +3\_3VAux=>0.275A  
 +3\_3V=>1.3A

Express Card Power Switch

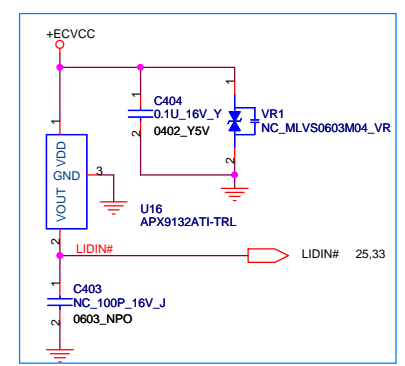
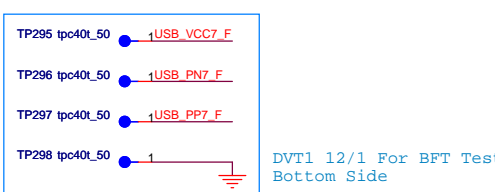
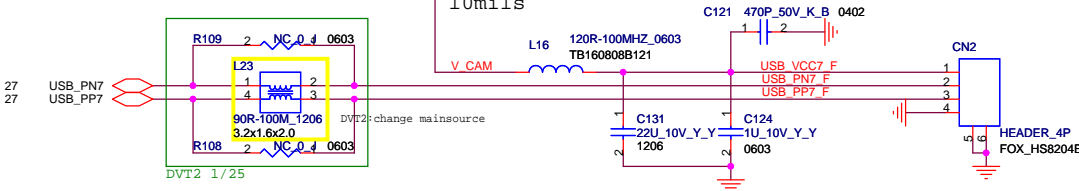


Express Card FPC.  
 EVT2 10/24 Change to BTB

http://zhjifa.taobao.com www.fangyuannb.com

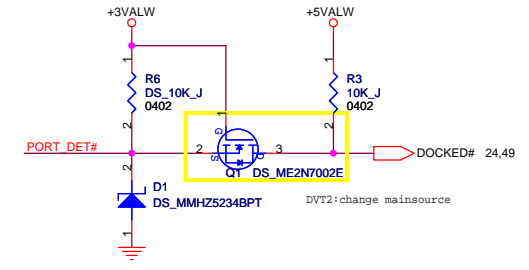
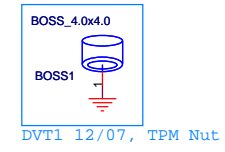
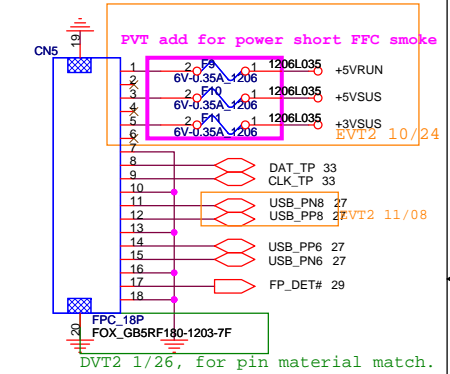
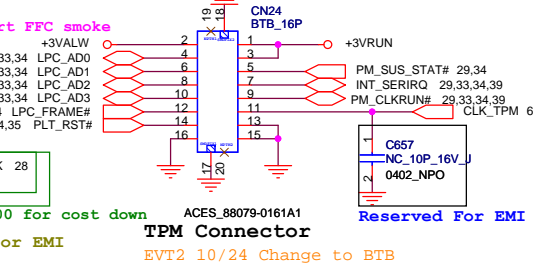
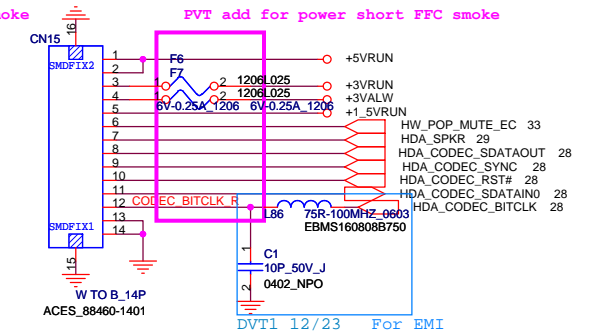
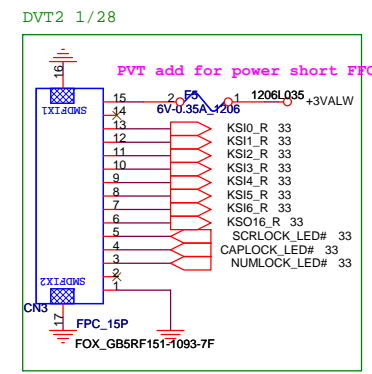
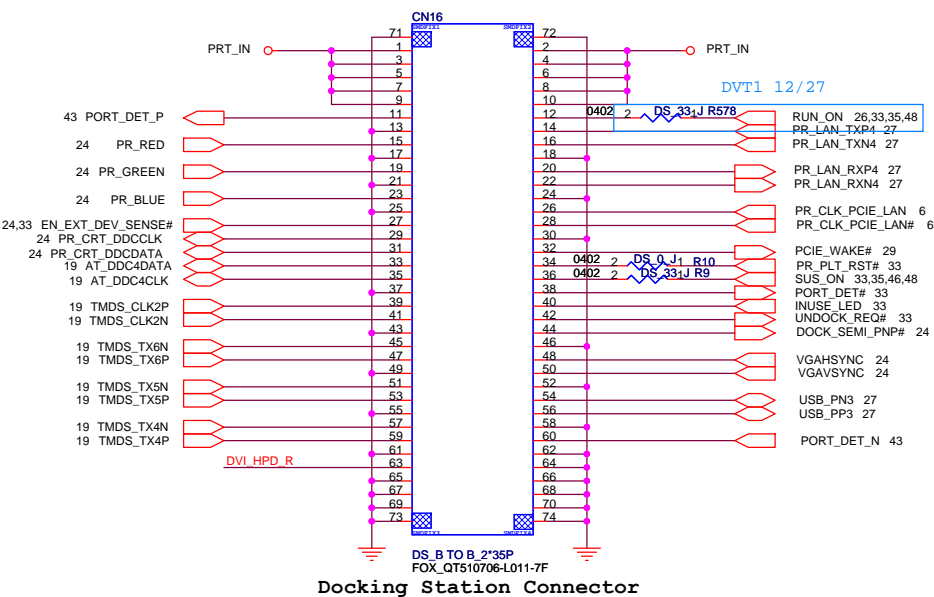
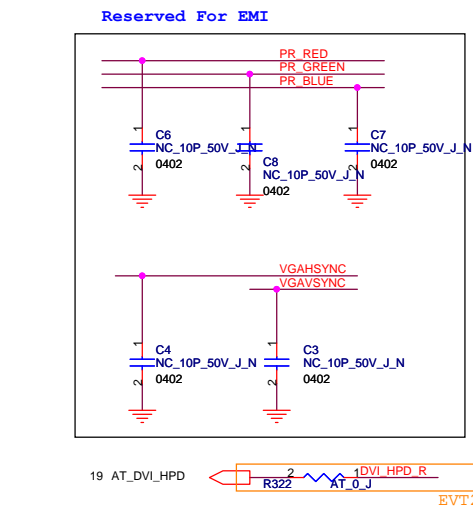
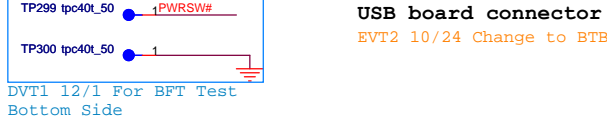
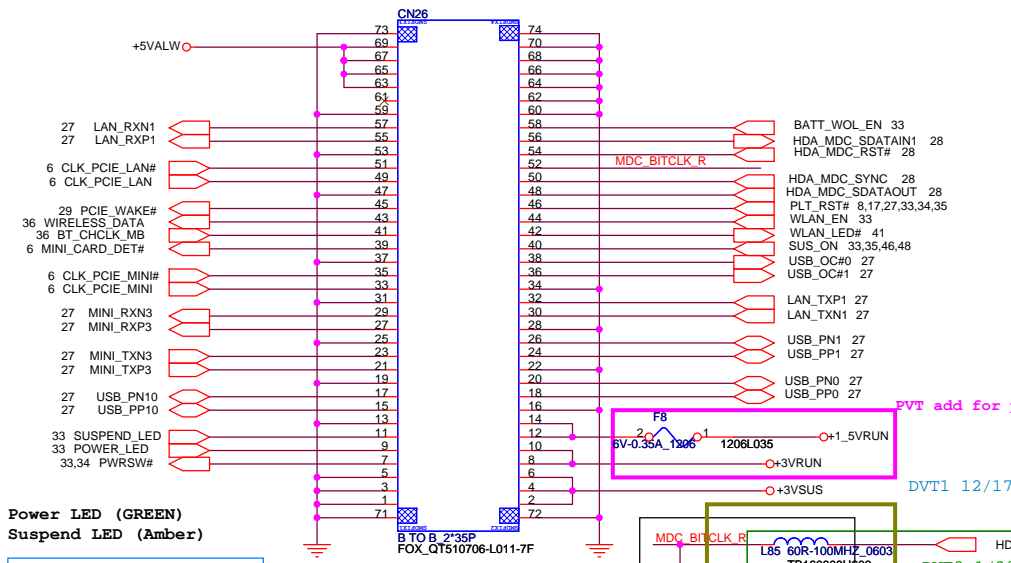


**CAMERA CONN.**



**LID Switch**

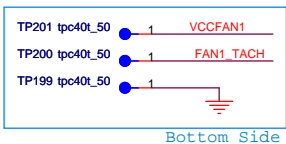
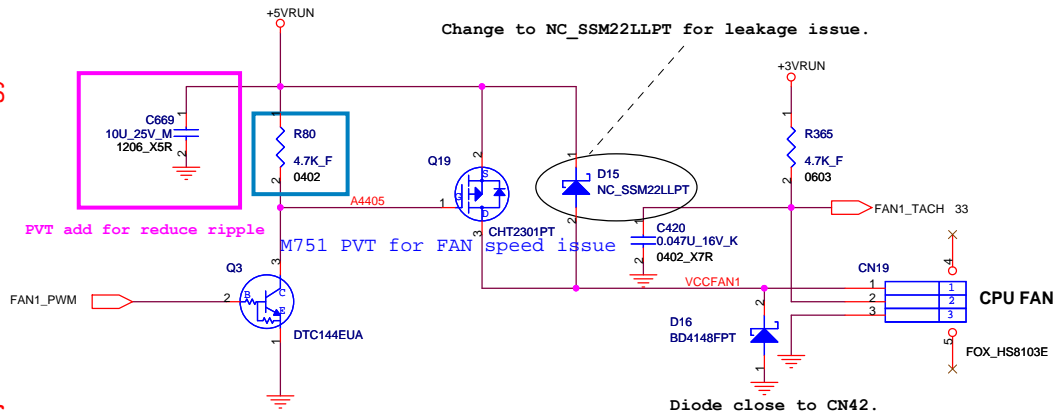




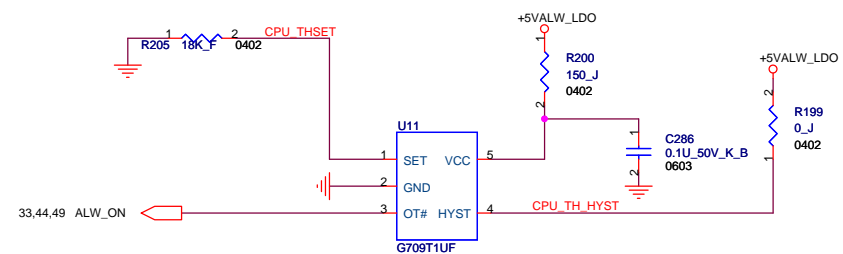
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		CCPBG - R&D Division	
<b>Title DB connector &amp; Docking</b>			
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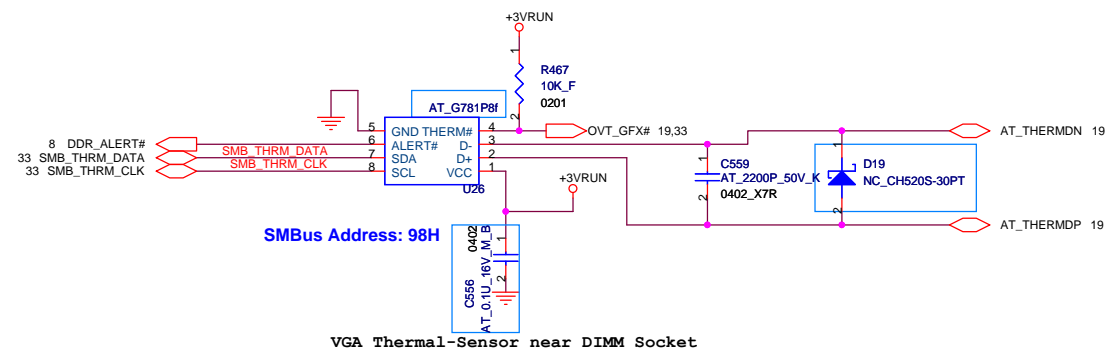
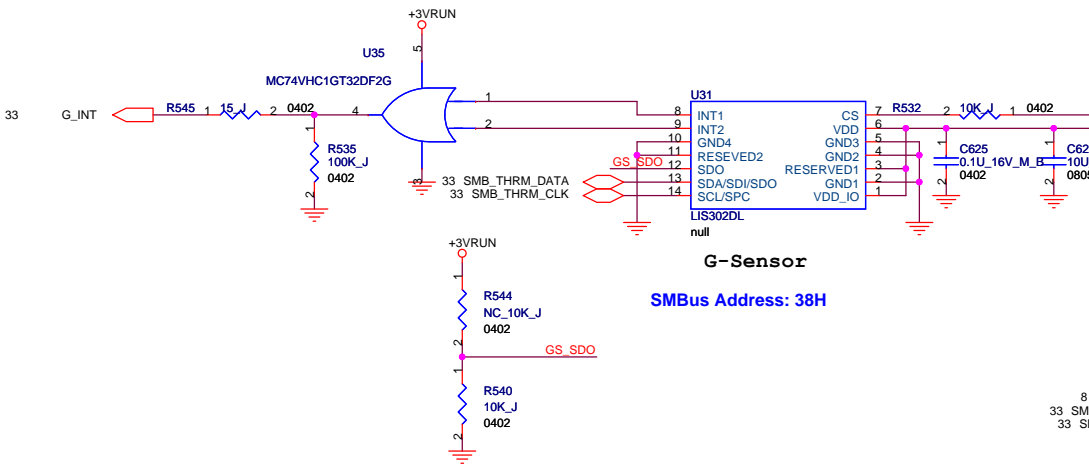
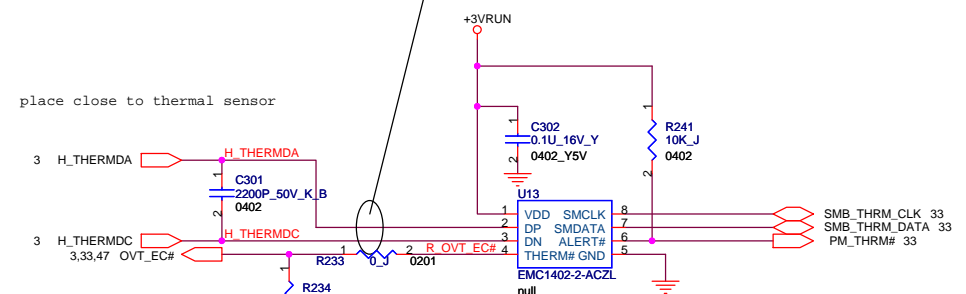
Change to NC\_SSM22LLPT for leakage issue.

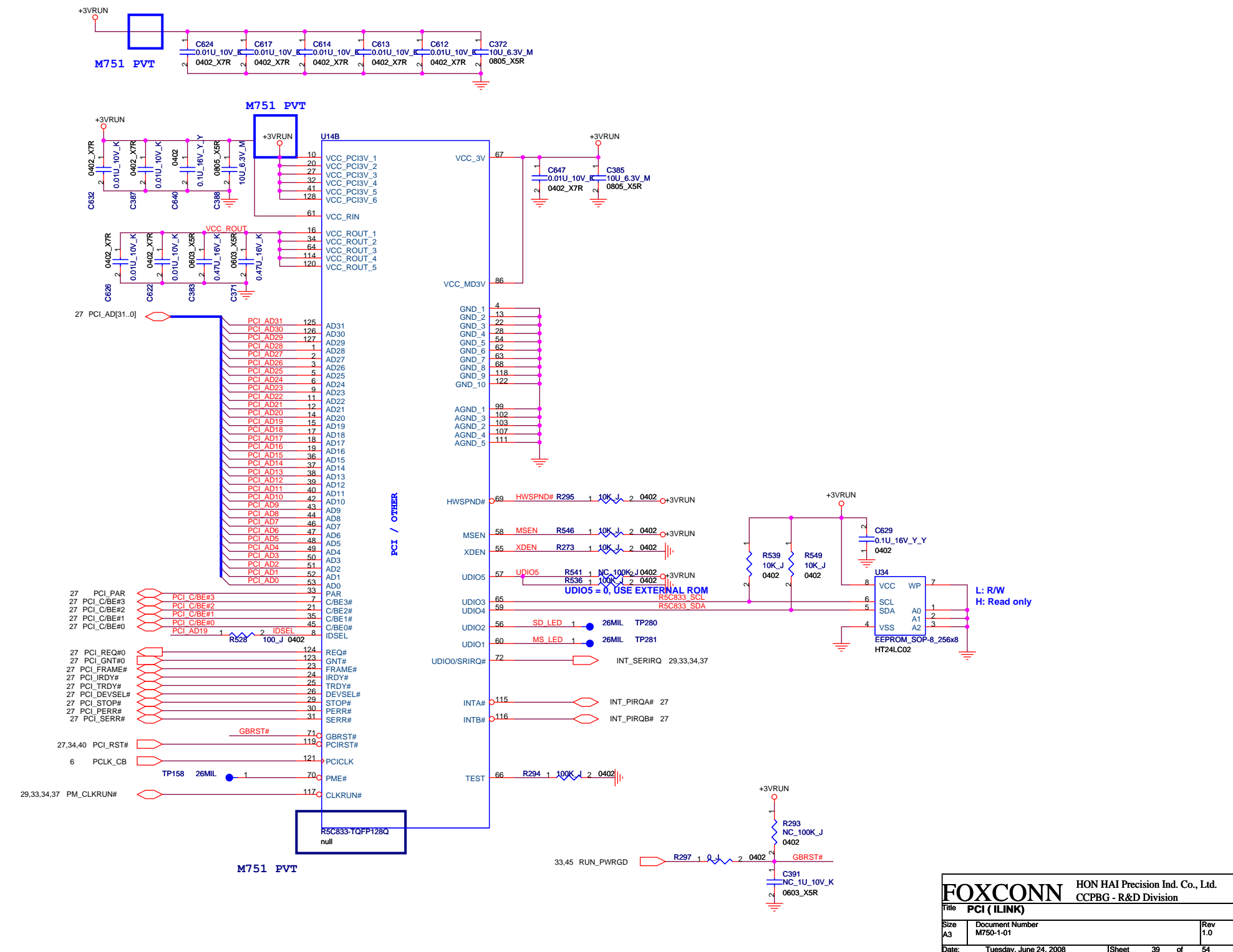


HW THERMAL PROTECTION

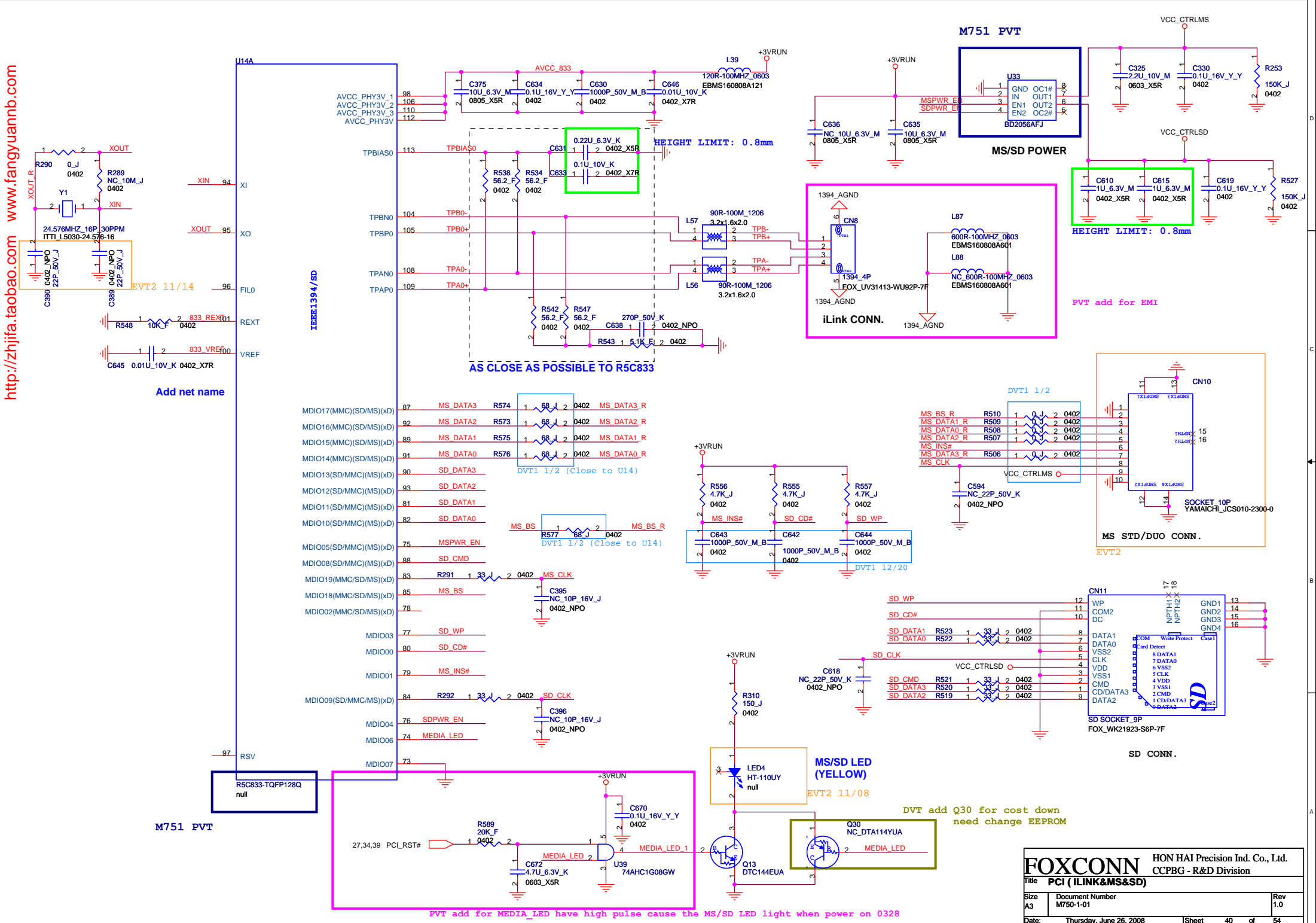


W/S:10/10 (microstrip)





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Add net name

AS CLOSE AS POSSIBLE TO R5CB33

HEIGHT LIMIT: 0.8mm

HEIGHT LIMIT: 0.8mm

PVT add for EMI

SOCKET\_10P YAMAICHI\_JCS010-2300-0

MS STD/DUO CONN.

SD CONN.

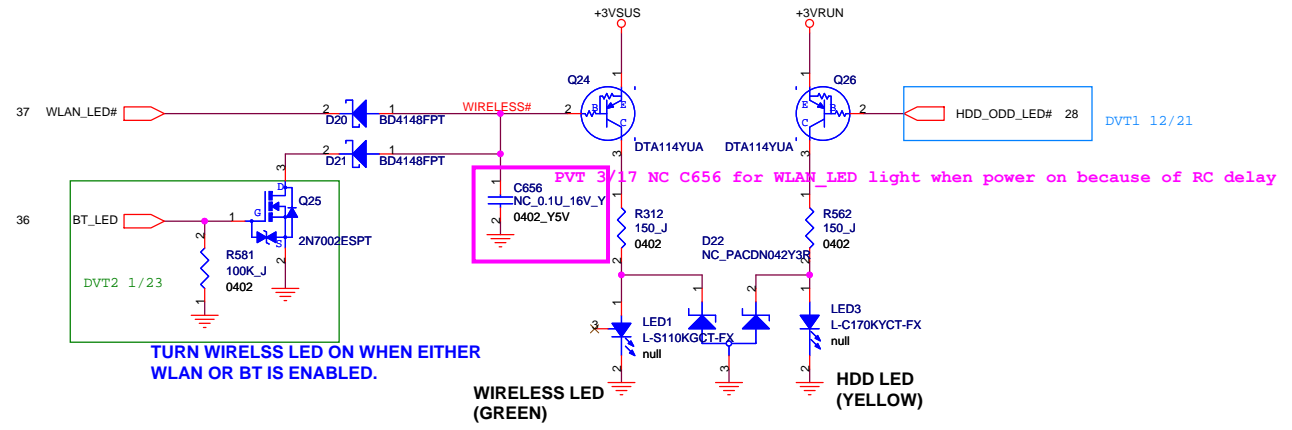
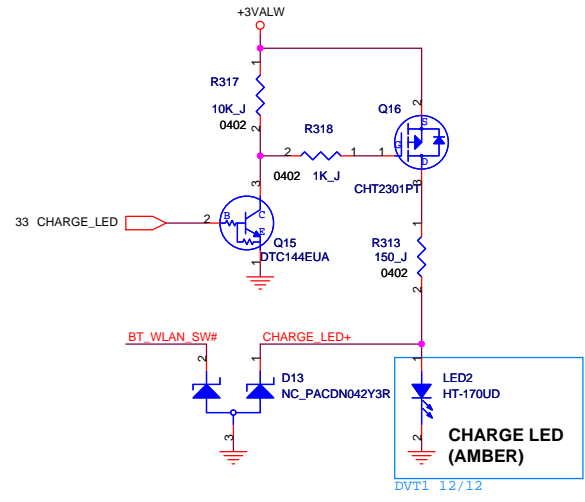
DVT add Q30 for cost down need change EEPROM

PVT add for MEDIA\_LED have high pulse cause the MS/SD LED light when power on Q328

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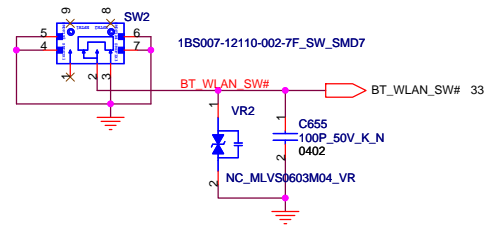
Title: **PCI (iLINK&MS&SD)**

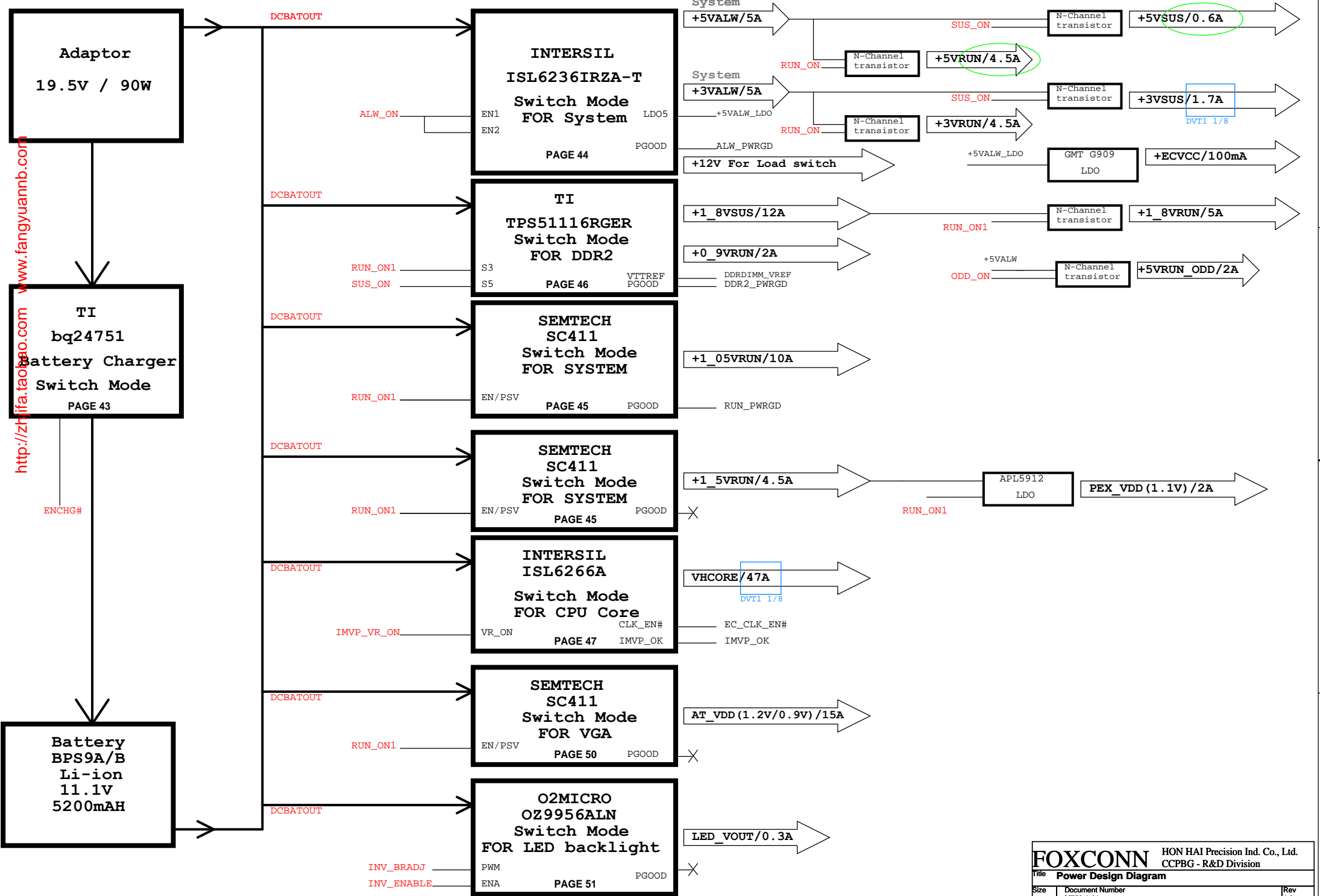
Size A3	Document Number M750-1-01	Rev 1.0
Date: Thursday, June 26, 2008	Sheet 40	of 54



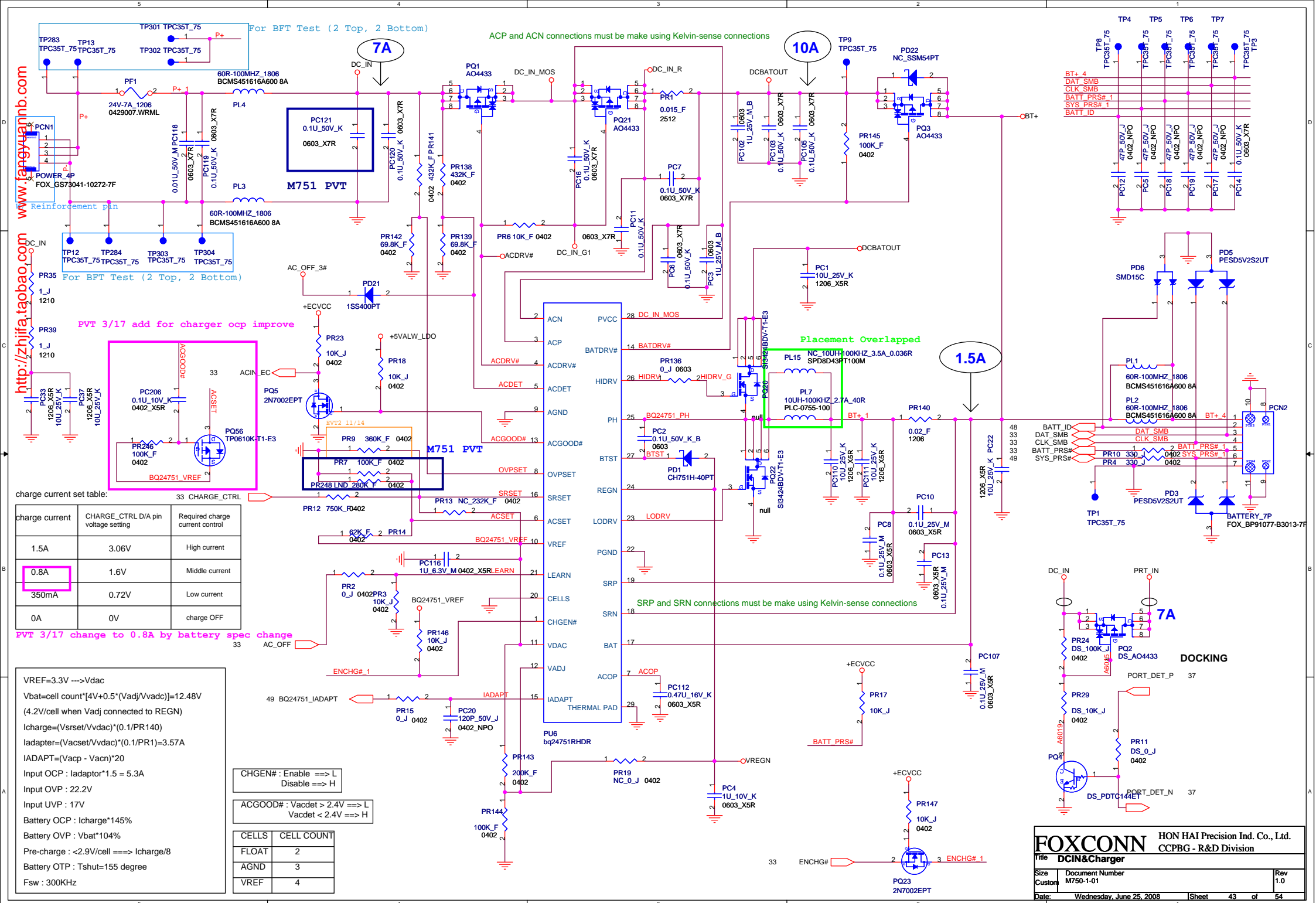
TURN WIRELESS LED ON WHEN EITHER WLAN OR BT IS ENABLED.

**WLAN/BT ON/OFF SWITCH**





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For BFT Test (2 Top, 2 Bottom)

ACP and ACN connections must be make using Kelvin-sense connections

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Reinforcement plan

charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V ==> Vdac  
 $V_{bat} = cell\ count * [4V + 0.5 * (V_{adj} / V_{vdac})] = 12.48V$   
 (4.2V/cell when Vadj connected to REGN)  
 $I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR140)$   
 $I_{adaptor} = (V_{acset} / V_{vdac}) * (0.1 / PR1) = 3.57A$   
 $IADAPT = (V_{acp} - V_{vacn}) * 20$   
 Input OCP :  $I_{adaptor} * 1.5 = 5.3A$   
 Input OVP : 22.2V  
 Input UVP : 17V  
 Battery OCP :  $I_{charge} * 145\%$   
 Battery OVP :  $2.9V * 104\%$   
 Pre-charge :  $< 2.9V / cell ==> I_{charge} / 8$   
 Battery OTP :  $T_{shut} = 155\text{ degree}$   
 $F_{sw} = 300KHz$

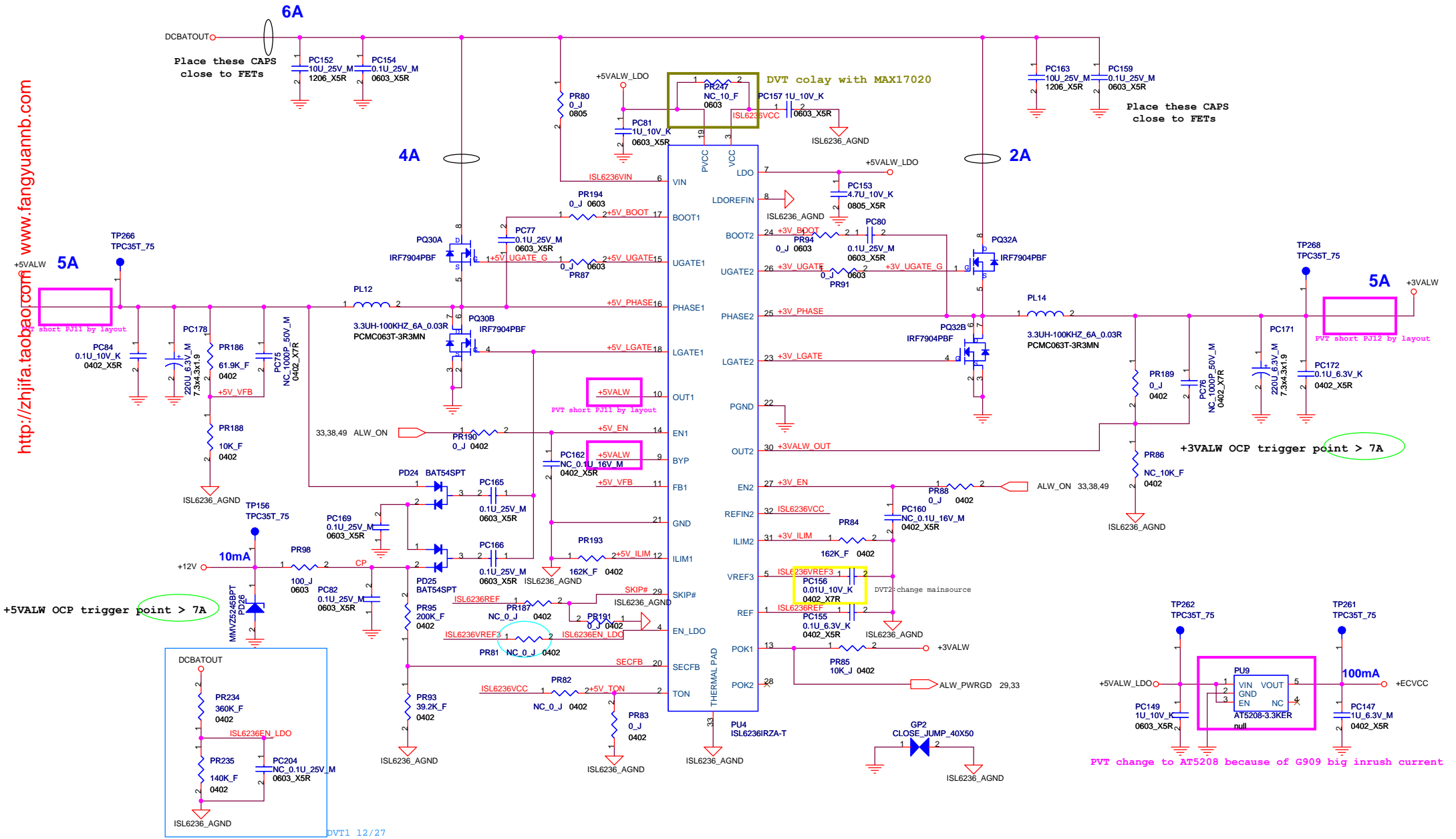
CHGEN# : Enable ==> L  
 Disable ==> H

ACGOOD# : Vdac > 2.4V ==> L  
 Vdac < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4



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TON	Operating Freqence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = VOUT(VIN - VOUT) / (VIN * F * ILIR * ILOAD(MAX))$$

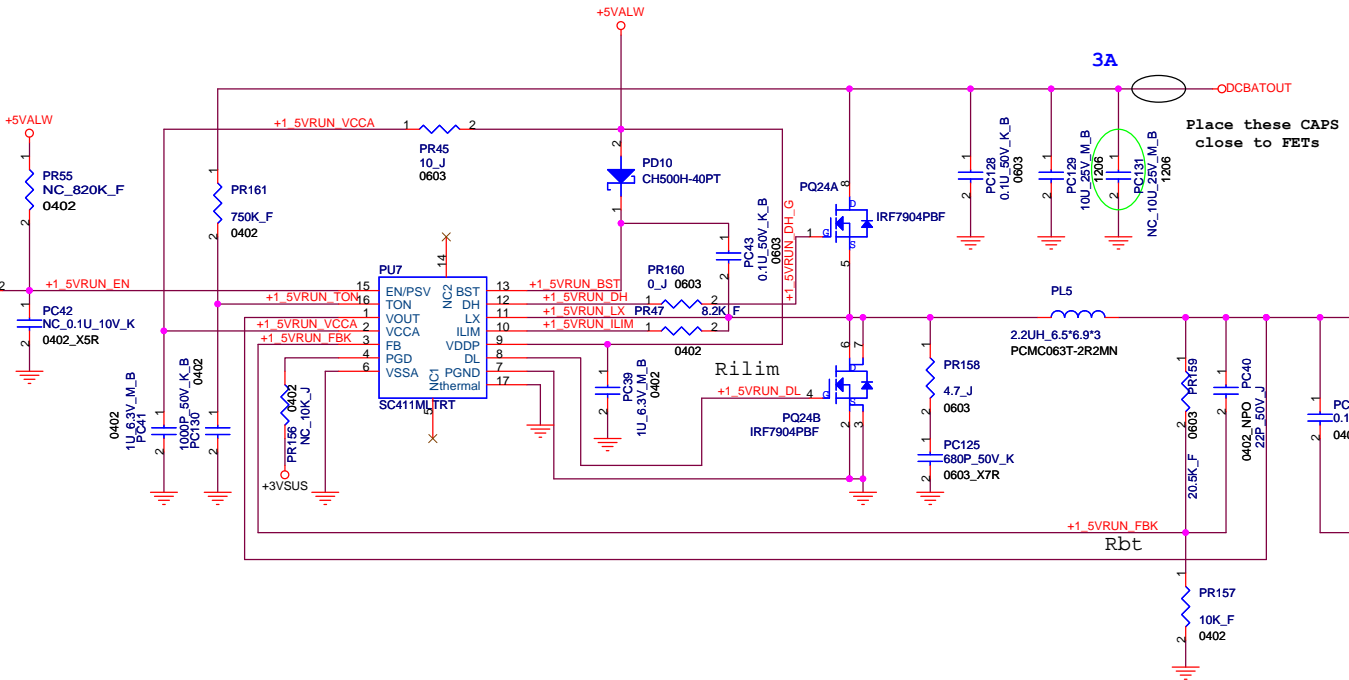
$$Rocp = (Iocp - Iripple/2) * (10 * Rds(on)) / 5u$$

$$+5VALW = ((PR186 / PR188) + 1) * VFB1$$

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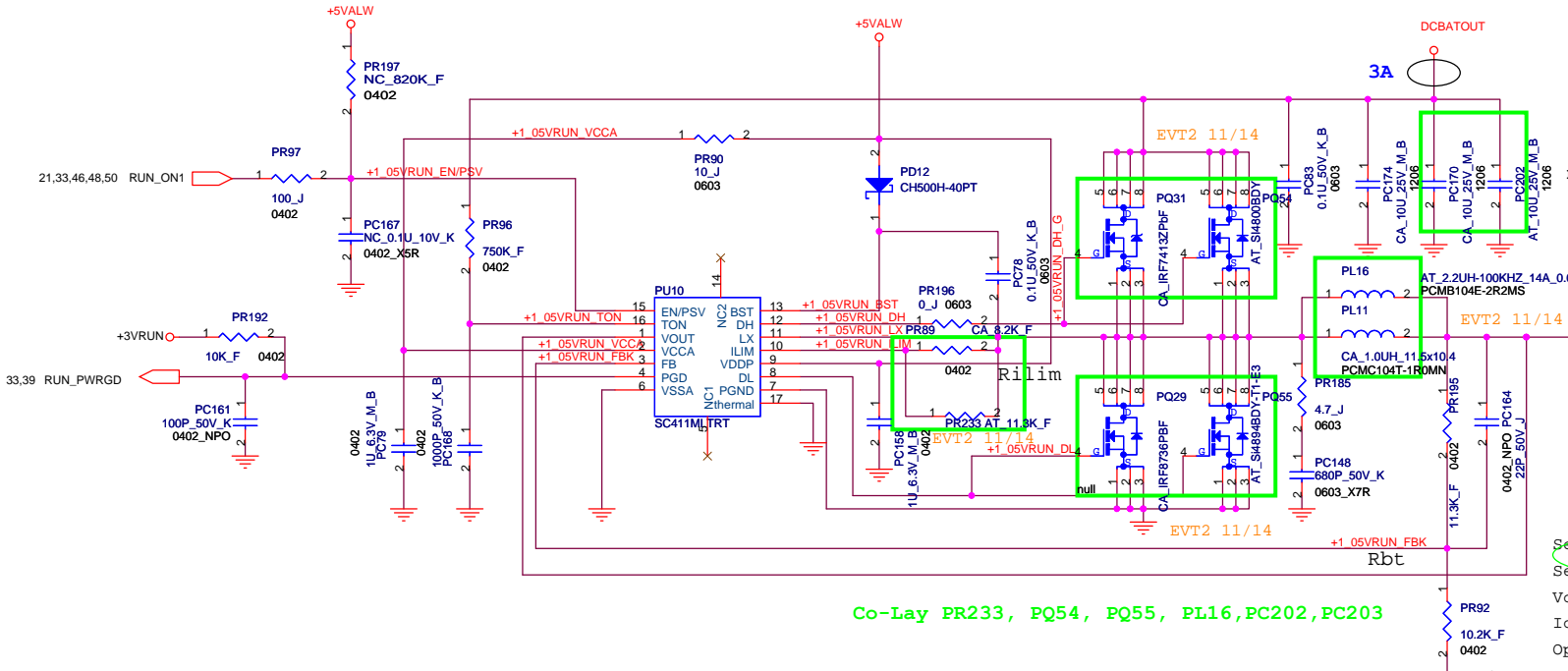
Title: **SYS Power (+3.3V/+5V)**

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4.5A  
PVT short PJ3 by layout

Setting OCP trigger point > 6.8A  
 $V_o = (1 + (PR159/PR157)) * 0.5 = 1.525V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10uA * PR47) / R_{dson}$   
 Operating Frequency : 345KHz  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%

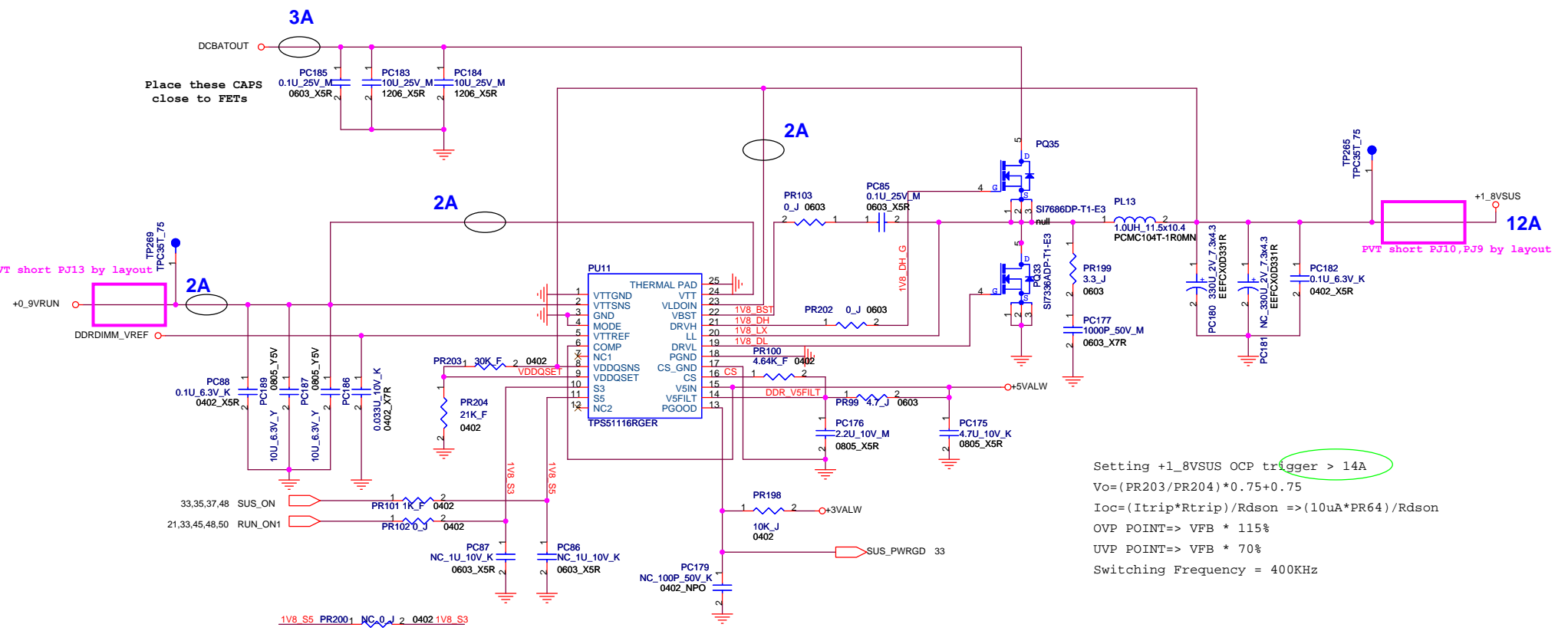


3A  
PVT short PJ8 by layout

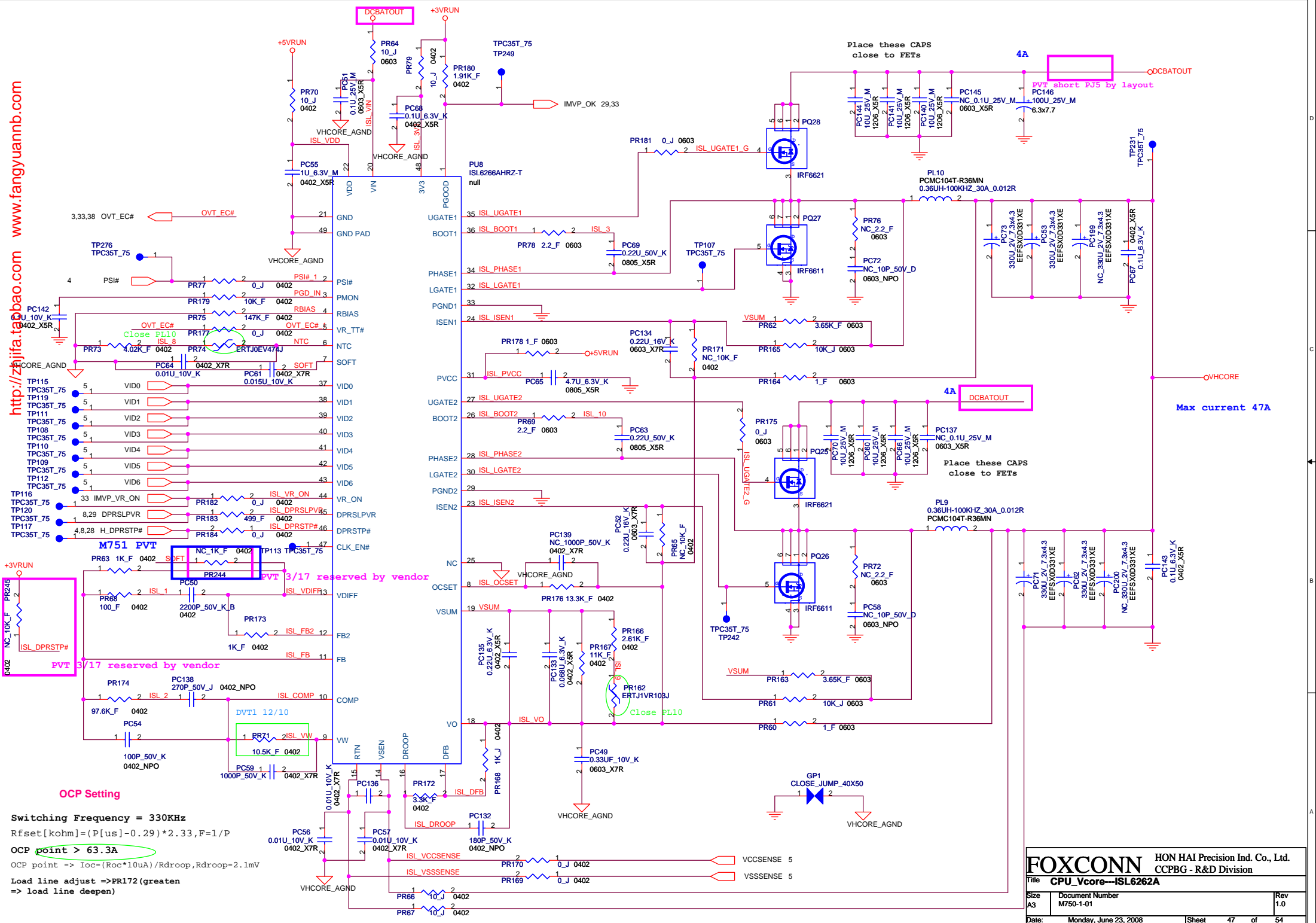
H version 5A  
L version 10A  
 Setting +1.05V H version OCP trigger point > 7A  
 Setting +1.05V L version OCP trigger point > 12A  
 $V_o = (1 + (PR195/PR92)) * 0.5 = 1.054V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10uA * PR89) / R_{dson}$   
 Operating Frequency : 345KHz  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%

Co-Lay PR233, PQ54, PQ55, PL16, PC202, PC203

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Setting +1\_8VSUS OCP trigger > 14A  
 $V_o = (PR203/PR204) * 0.75 + 0.75$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} => (10uA * PR64) / R_{dson}$   
 OVP POINT=> VFB \* 115%  
 UVP POINT=> VFB \* 70%  
 Switching Frequency = 400KHz



- TP276 TPC35T\_75
- TP115 TPC35T\_75
- TP119 TPC35T\_75
- TP111 TPC35T\_75
- TP108 TPC35T\_75
- TP110 TPC35T\_75
- TP109 TPC35T\_75
- TP112 TPC35T\_75
- TP116 TPC35T\_75
- TP120 TPC35T\_75
- TP117 TPC35T\_75
- TP118 TPC35T\_75
- TP121 TPC35T\_75
- TP122 TPC35T\_75
- TP123 TPC35T\_75
- TP124 TPC35T\_75
- TP125 TPC35T\_75
- TP126 TPC35T\_75
- TP127 TPC35T\_75
- TP128 TPC35T\_75
- TP129 TPC35T\_75
- TP130 TPC35T\_75
- TP131 TPC35T\_75
- TP132 TPC35T\_75
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- TP136 TPC35T\_75
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- TP246 TPC35T\_75
- TP247 TPC35T\_75
- TP248 TPC35T\_75
- TP249 TPC35T\_75
- TP250 TPC35T\_75

**OCP Setting**

Switching Frequency = 330KHz

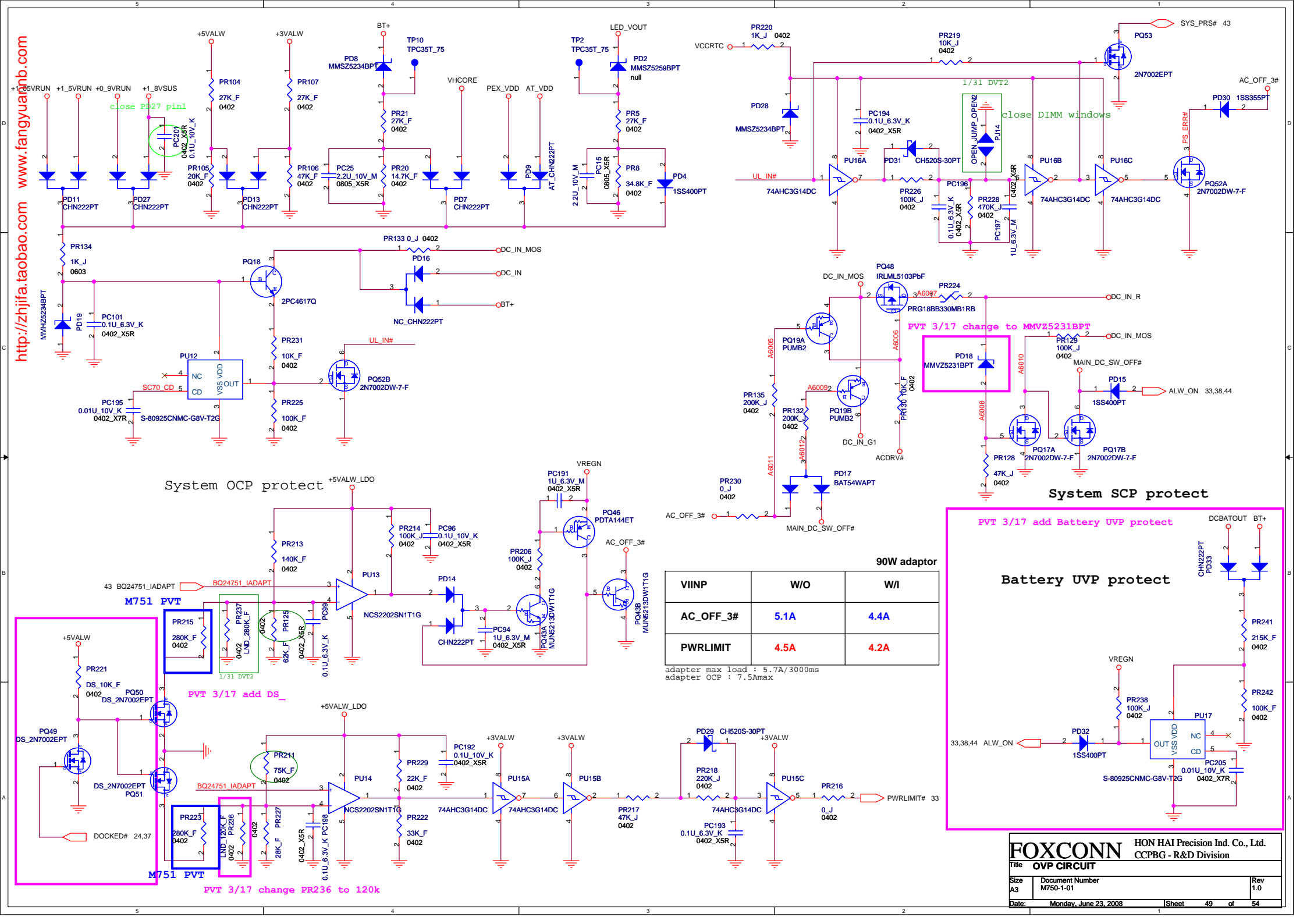
$$R_{fset}[kohm] = (P_{us} - 0.29) * 2.33, F = 1/P$$

OCP point > 63.3A

OCP point =>  $I_{oc} = (R_{oc} * 10uA) / R_{droop}, R_{droop} = 2.1mV$

Load line adjust => PR172(greaten => load line deepen)





**System OCP protect**

**System SCP protect**

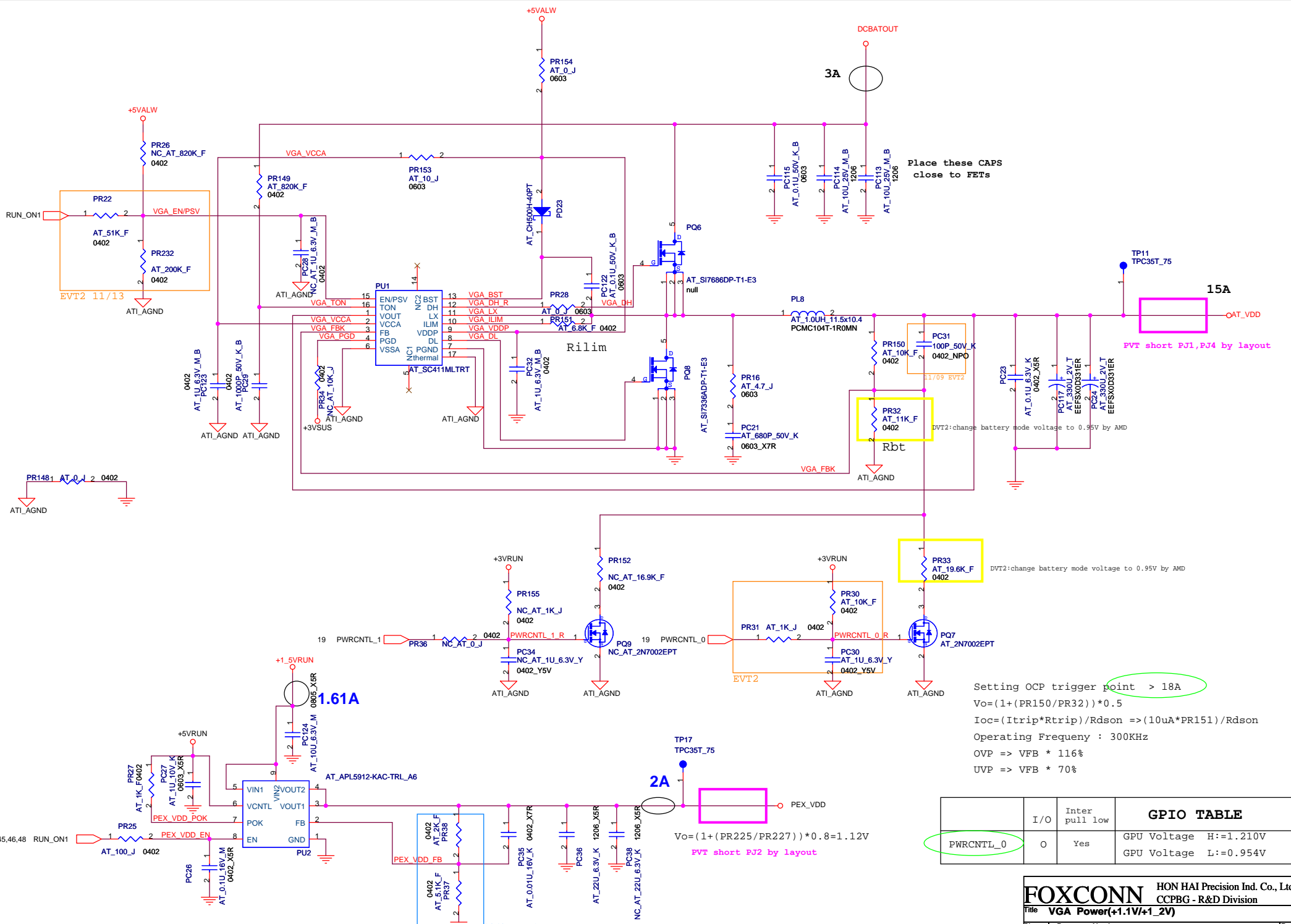
**PVT 3/17 add Battery UVP protect**

**Battery UVP protect**

**90W adaptor**

VIINP	W/O	W/I
AC_OFF_3#	5.1A	4.4A
PWRLIMIT	4.5A	4.2A

adapter max load : 5.7A/3000ms  
 adapter OCP : 7.5Amax



Place these CAPS close to FETs

PVT short PJ1, PJ4 by layout

Setting OCP trigger point > 18A

$$V_o = (1 + (PR150 / PR32)) * 0.5$$

$$I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR151) / R_{dson}$$

$$\text{Operating Frequency} = 300\text{KHz}$$

$$\text{OVP} \Rightarrow V_{FB} * 116\%$$

$$\text{UVP} \Rightarrow V_{FB} * 70\%$$

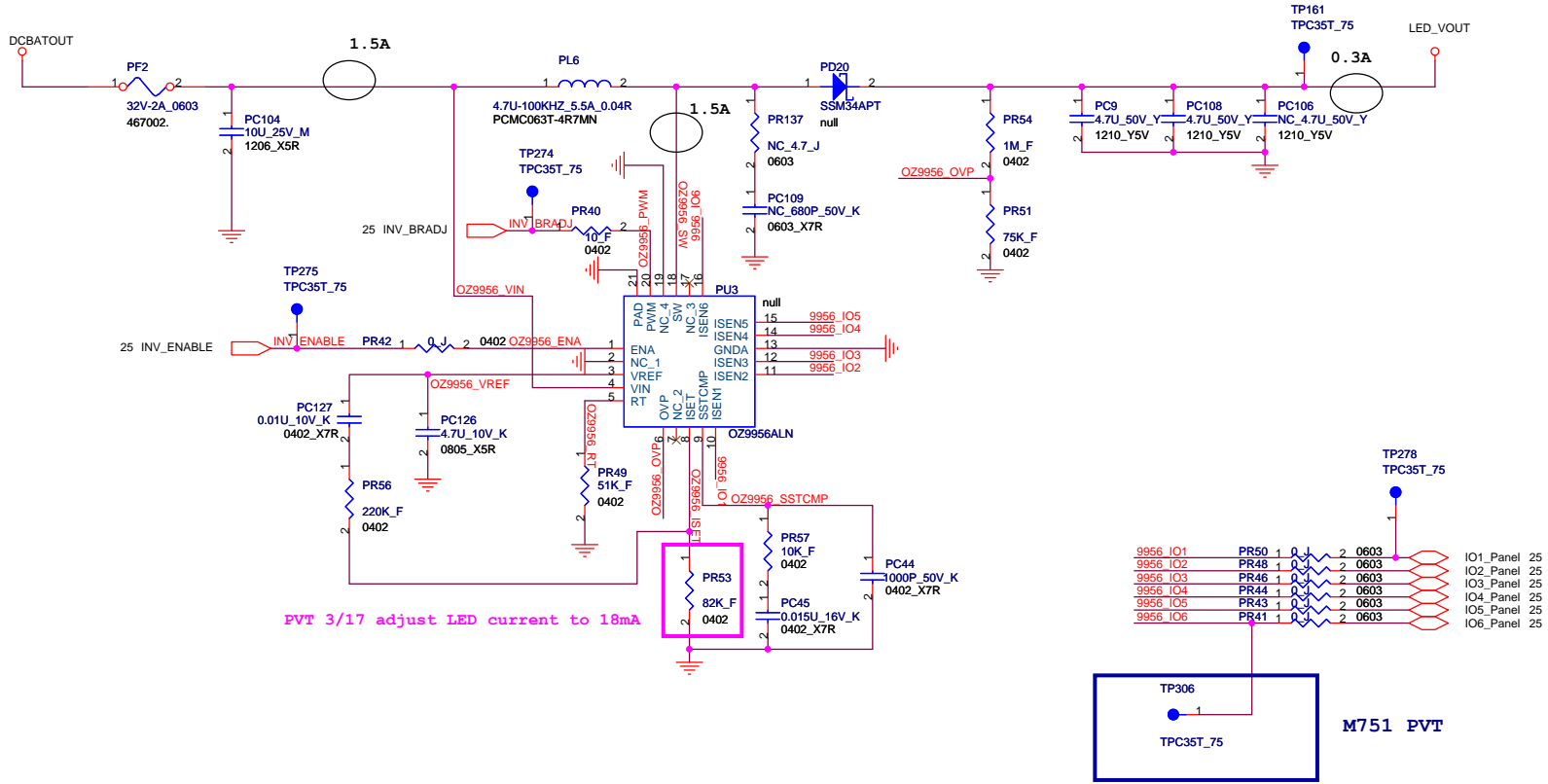
GPIO TABLE		
I/O	Inter pull low	
PWRCNTL_0	Yes	GPU Voltage H: =1.210V GPU Voltage L: =0.954V

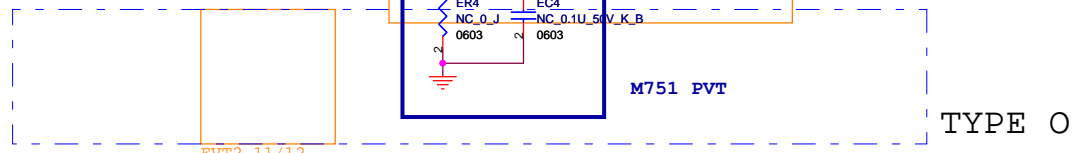
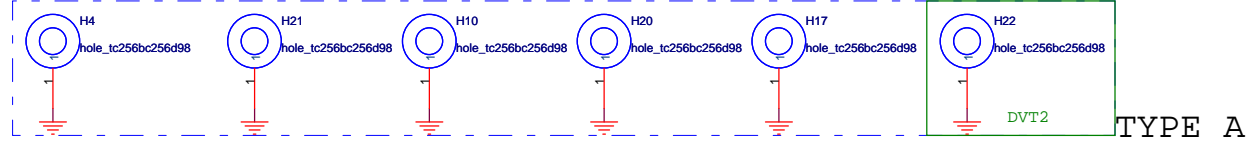
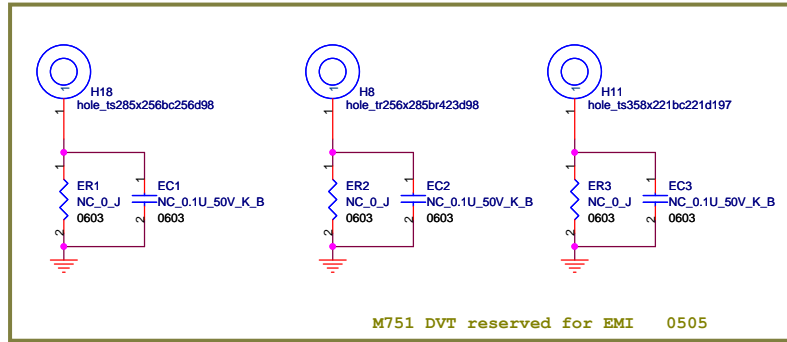
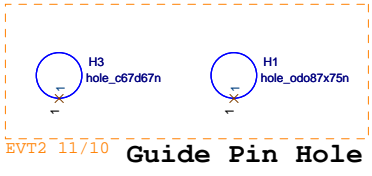
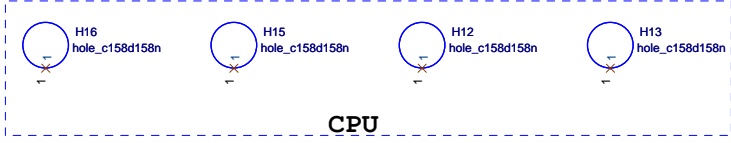
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Title: **VGA Power(+1.1V/+1.2V)**

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Mainboard

10/12  
Change color of MS/SD/HDD LED.  
Mount R419, R414, R420, R421.  
10/13  
SYSTEM\_ID, MODEL\_ID definition update.  
10/20  
CPU 22pF CAP N.C. parts location change.  
N.C. R101 For EVT2 (Use +5V type camera module)  
10/24  
Move PCI Express pair of LAN from port5 to port1.  
10/29  
Change PR9 to 422K.  
Add PL15 and PL7 co-lay.  
Modify charge current setting table.  
Mount PR83.  
PL11 change to 1uH.  
Add TP276 test point.  
Add PC201 0.1uF and close to PD27 pin1.  
Change PL6 to 4.7uH and add TP274,TP275 test points.  
10/30  
Refer to PUR suggestoin to change component source.  
Add NC\_PR232  
Change PR30 to 10K and PR31 to 1K.  
Mount PC30  
Add TP278 test point.  
10/31  
Refer to PUR suggestoin to change component source.  
Swap LVDS group of ATI M82.  
11/02  
Change "\*" to net "EN\_EXT\_DEV\_SENSE" for low active.  
Modify MB Semi-PNP circuit.  
11/03  
Inverse HDMI pairs polarity(DVI pairs inversed on docking side).  
11/04  
Change USB board connector.  
Combine MS/SD LED to one(MEDIA\_LED).  
11/05  
N.C. R377, Mount F3.  
Change INUSE\_LED to GPIO72.  
Change MS slot to YMAIICHI JCS010-2300-0.  
11/06  
Change part of CN16/CN26.(Height Change)  
Change netname of "SD\_WP#" to "SD\_WP".  
Change PR143 to 200Kohm.  
Update charge current setting table.  
Reserve BATT\_WOL\_EN for LAN wake up enable/disable in battery mode.  
11/07  
C453, C452, C451,C426, C425, C424 change size to 0402.  
Mount PR158, PC125 and PR185, PC148 and PR199, PC177 and PR16, PC21.  
N.C. PR36.  
Change C188 from 0.1uF to 0.47uF.  
11/08  
Swap USB\_PP8/PN8 for ease of routing.  
Change button board connector to WBF31326-F04TR.  
Change MS/SD LED to side view, yellow color.  
Change U7 from CM2009 to CM2006.  
Update VCC\_DDC power isolation circuit.  
Add R565,C658 for SRTCST#.  
11/09  
Change PC31 from 22p to 100p.  
Reserve R566 for removal of Ext. SPI Conn on DVT.  
Reverse Button Brd CN pin assignment.  
Add EMI Cap C659-C666 on +1\_8VSUS.  
11/10  
Delete guide pin hole H9, H22.  
N.C. F3, mount P1. (Use +3VSUS for camera power on EVT2).  
11/11  
Change pin assignment of Express CN.  
11/12  
Change PTH hole size. (H11)  
Add TP283,TP284.  
Change net name "ISL\_VSSSENSE\_" to "ISL\_VSSSENSE".  
11/13  
Add TP285-290 for SI probe point.  
Change type of H14,H19.  
Change PR22#51K, PR232#200k.  
11/14  
Tune crystal accuracy, change C390/C389/C416/C412 to 22PF,C648/C649 to 18PF.  
Change PR6#360K.(Charge Current Control)  
Co-Lay PR233, PQ54, PQ55, PL16.  
Change RP34 to 2.2K for SI.  
N.C. R415, mount L47 on H model.  
11/19  
N.C. R559 (Double pull up on BT\_PRS#)  
11/23  
Change camera power to +5VSUS.  
DVT1 12/01  
Swap DVI bus polarity.  
Route RUN\_ON to docking station CN.  
Add logic gate(U37) to prevent panel flash when boot up.  
Add R567, bypass brightness control signal.  
Use +3V\_DELAY(Q4) to prevent M82 high pulse on LCD control signals.  
12/07  
Change DC-IN CN(PCN1, With Reinforcement Pin).  
Add TPM Nut (BOSS1)  
Change Button Board CN (CN3) to 15 pin.  
Add R570 for power consumption measurement.  
12/12  
Change U6 from Quad to Dual XOR gate.  
Change EMI Caps C424-C426, C451-453 to 10pF.  
Change color of LED2(Charge LED) to Amber.  
Change U16 from MR-sensor to Hall-sensor. (N.C. R263)  
12/13  
Change damping resistors of keyboard matrix to 120ohm Ferrite bead.(For EMI)  
12/17  
Change C451,C452,C453,C424,C425,C451 to 22pF. (For EMI)  
Add one more +3VSUS (CN26) for WLAN module to cover 1500mA(peak)/1100mA(normal) requirement.  
12/18  
Add one more LCDVCC pin (CN1) for panel to improve voltage drop.  
Add optional resistors(R571,R572) for gamma control.  
Reduce LED\_VOUT from 6 pins to 2 pins.  
12/20  
Change net "BL\_OFF" to "BL\_OFF#".  
Add R573-577 to improve MS signal overshoot/undershoot.  
Mount C642-644.  
Change F3 to 0.25A.  
12/21  
Change Net "HDD\_LED#" to "HDD\_ODD\_LED#"  
12/23  
Change C412/C416 from 22pF to 10pF.  
Change C648,C649 from 18pF to 15pF.  
Mount U26(VGA Thermal Sensor) on H model only.  
Add 75 ohm bead, 10pF capacitor on HDA\_MDC\_BITCLK/HDA\_CODEC\_BITCLK for EMI.  
12/24  
Update H2/H6/H7/H8 footprint.  
Delete R563, R564 (CR1\_GND).  
Change D17, D18 to SSM22 to reduce voltage drop.  
Change pull up voltage of R360/R361 to +3VRUN. (Only Strap/GPIO pin connected to +3V\_DELAY)  
N.C. C403 (Not necessary for ESD)  
12/26  
Delete ODD\_DP# connection to ICH9M.  
12/27  
Add PC204 for noise filtering.  
Add R578 for protection.  
Change U27 from RClamp0514 to RClamp0524.  
N.C. SW1, R134,R141  
Change TP285-290 for SI probe point.  
Change PR38 to 2K, PR37 to 5.1K.  
12/28  
N.C. U4 shunt regulator to reduce S4 consumption.  
Mount R131, N.C. R129.  
Reserve LDO (U38) for 1.5V type VCCSUSHDA.  
Add R579,R580 to avoid floating on input pin.  
1/2  
N.C. C451-453, C424-426.  
N.C. PC204.  
Add prefix AT\_ on R322, R51.  
Change damping resistor value of MS card.  
(R573-577 from 33 to 68 ohm)  
(R506-510 from 33 to 0 ohm)  
Change L30-32 to 27mH inductor.  
Change C258,260,262 to 2.2pF.  
Change revision of clock generator(U29) to Rev.B  
1/5  
Change D2/D3 to low capacitance type.  
Fine tune delay timing. Change R19/R565 to 13K.  
1/8  
Update power design spec.  
VCore: 47A, +3VSUS: 1.7A.  
DVT2  
1/15  
Update power budget of VCCHDA,VCCSUSHDA,VCCDMI,VCC1\_5\_A  
Add GND pin on C130.2  
1/21  
Add BT\_LED on CM4.6  
Update WIRELESS LED circuit. Page41.  
1/21  
Add screw hole H22.  
Add D23, D24 for leakage issue when EC initialization.  
Add R460 for Non-Dock Sku.  
1/23  
PQ12 change to SI3424BDV-T1-E3.  
PR125 change to 62Kohm  
PR215 change to 205Kohm  
PR211 change to 75Kohm  
PR223 change to 154Kohm  
Add PR237 ND\_280Kohm , PR236 ND\_154Kohm for Non-Dock sku.  
Add pull down resistor (R581) on BT\_LED.  
1/25  
Mount L23, N.C. R108, R109 for EMI.  
Change L86 from 75R to 10R for SI.  
For Docking sku, add prefix DS\_ on value of C257,C259,C261,CN16 D1, PQ2, PQ4, PR11, PR24, PR29, Q1, Q20, Q21, R6, R9, R10, R165, R167, R416 R444, R578, U8, U9, U10.  
1/26  
Change R176 from 54.9 to 649 Ohm.  
Del L48, Add R582, R583 (N.C.)  
Change C413 from 0.1uF to 1uF.  
Change CN5 from Gold plated to TIN plated.  
1/28  
Mount R555, R556, R557.  
Add +1.5V\_PCIE\_OUT on CN25.6 to reduce voltage drop.  
Change CN3 from WBF31526-F04TR to GBSRF151-1093-7F.  
(Vendor naming rule change, same part.  
layout footprint pin reversed)  
1/29  
Add R584, R585, Q27 to solve DDC capacitance issue.  
Add R586 for identification of Dock support.  
1/30  
Change L86 back to 75R, change L85 from 75R to 10R.  
Mount CN13 for software debug on DVT2.  
N.C. R572.  
Move R321 to U37B.6  
1/31  
Move PJ14 to PR226.2  
Change R176 back to 54.9 ohm.  
Add prefix LND on PR36, PR237 for Non-Dock skue for LOW model.  
Add PAD1 for EMI Grounding.  
0218  
M750  
change U30 from NC7832M5X(14-NC7832M-5X00) to MC74HC1G32DTT1G(14-MC74HC1-G300)  
change D2,D3 from BAS316(16-BAS3160-0000) to BAS316PT(16-BAS316P-T000) for common parts  
change D6,D7,D9,D11,D12,D14,D23,D24 from 16-SC5500V-4000 to CH5500V-40PT(16-CH5500V-40P00) for common parts  
change Q1,Q5,Q17,Q21,Q22 from 17-2N7002P-T000 to ME2N7002E(17-ME2N700-2E00) for common parts  
change Q23 from 17-MMBT390-4001 to PMBT3904.215(17-PMBT390-4200) for common parts  
change C303,PC156 from 0.01U,6.3V,K(1C-2B20103-R100) to 0.01U,10V,K(1C-2B20103-K200) for common parts  
change L23,L28,L40,L41,L42 from 90R-100MHZ\_0R35(1L-FDLW315-N900) to 90R-100M\_1206(1L-FWCM321-6F00) for common parts  
change C19,C17 from Y5V to X5R tolerance  
change PR32 to 11K, PR33 to 19.6k to set the battery mode voltage to 0.95V by AMD for battery mode dual display  
0318 PVT  
NC C656 for WLAN\_LED light when power on because of RC delay  
update battery identify (CPU5) P/N to R500500DN100NS by vendor  
update U7 symbol to CM2006-02QR  
modify R345 value to HD\_ for BOM change of disable HDAudio in 128MB SKU  
remove PU11,PU12,PU3,PU8,PU10,PU9,PU13,PU5 and short by layout  
correct U36 vendor P/N to WPCB775LAADG  
change U32 to W25X16AVSSIG by vendor suggestion  
add PQ56,PC206,PR246 for charger ocp improve by M760 battery OCP issue  
modify P43 charge current table ,middle current change from 1A to 0.8A  
add PR244 and PR245(dummy directly) for intersil ISL6266A found C4 hang at the other company  
add UVP circuit (PU17,PR238,PD32,PC205,PR242,PR241,PD33)  
change PR236 to 120Kohm for power limit point improved  
change PQ50,PQ51,PQ49,PR221 value title to DS.  
change PR53 to 82Kohm for LED backlight current modify  
add R587,Q28,Q29 for improve HDMI voltage drop  
0326  
Short R31,R32,P34 by layout  
add C669 for reduce fan power source ripple  
add L87,L88 for EMI  
add U39,C670 for MS/SD abnormal behavior  
0327  
change PU9 to AT5208 because of G909 big inrush current  
0328  
NC R389,R393,Y3,C436,C437,C241,C242,L29,U5,R152 for use AMD internal SS  
add R589,C672 for MS/SD led abnormal when power on  
NC R389,R393,Y3,C436,C437,C241,C242,L29,U5,R152 for use AMD internal SS  
add R589,C672 for MS/SD led abnormal when power on  
reserve R588 for reduce G-sensor power ripple  
0402  
add F5-F11 for power short  
0403  
change PR241 from 232K to 215K for UVP circuit improve  
0408  
NC R348,R356,R357 for using AMD internal SS  
change R378 value to HD\_ for HDMI disable

M751 DVT  
0505  
Reserve EC1,EC2,EC3, ER1,ER2,ER3 for Hynix 1GB EMI  
change HDD sata CN20 pin define to increase the impedance for SATA SI  
0506  
reselect PR247 for colay with MAX17020  
Update U29 footprint for Japan/Mitsui package  
change L85 to 60ohm for EMI  
NC C5 for EMI  
0508  
add Q30 for MS/SD LED cost down  
M751 DVT  
0618  
Page 2: Change L30,L31,L32 to 33ohm and change C258,C260,C262 to 15PF for SI issue  
Page 4: chang C405 C407 to 1C-2B30475-K100 for PUR request  
Page 7: NC R561,Mount R560 ,keep system ID the same as M750  
Page 8: NC F1 ,mount F3,for 5v Camera moudle  
Page 38:Change R80 to 4.7k from 10k , for FAN speed issue  
Page 4 : NC Q30 ,Mount U39 Q13 C672 C670 R589 for mor Request  
Page 49: NC PR244 ,Vendor suggestion and it is related with DC4  
Page 49:1.FR14 change to 62Kohm , co-lay PR248 LND 56.6Kohm with PR7.  
2. PR215 205Kohm change to 280Kohm  
3. PR223 154Kohm change to 280Kohm  
Page 24: change D17 to 16-SSM24AP-T000' for leakage issue  
Page 27: Change C254,C252 rating to 6.3v for cost down  
Page 35: del R301,R302,R303,R304,R305,R306,L40,L41,L42 for cost down  
Page 36: del R147 H150 L28 for cost down  
Page 38: del R261 for cost down,change U14 version  
Page 39: Change CN6 to 1N-0024000-F170 for pur request  
Page 39: add ER4 EC4 for EMI Issue  
0625  
Page 23: .PC121 change from 0.1uF/25V to 0.1uF/50V(1C-2B30104-K000)  
Page 24 : change ER4 EC4 to 0603 for EMI request  
Page 45: modify the U33 F/N to 15-BD2056A-FJ00 for CE update component library  
Page 45: resume CN6 main source 1N-0024000-M170, for 2nd source layout issue  
Page 45: change D17 to 16-SSM24PT-0000 For design change  
Page 47: add one test point in PR41 pin1.

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