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P. Leader	Check by	Design by

Project Code & Schematics Subject: MS21 MP Main Board

(TYPE 2)

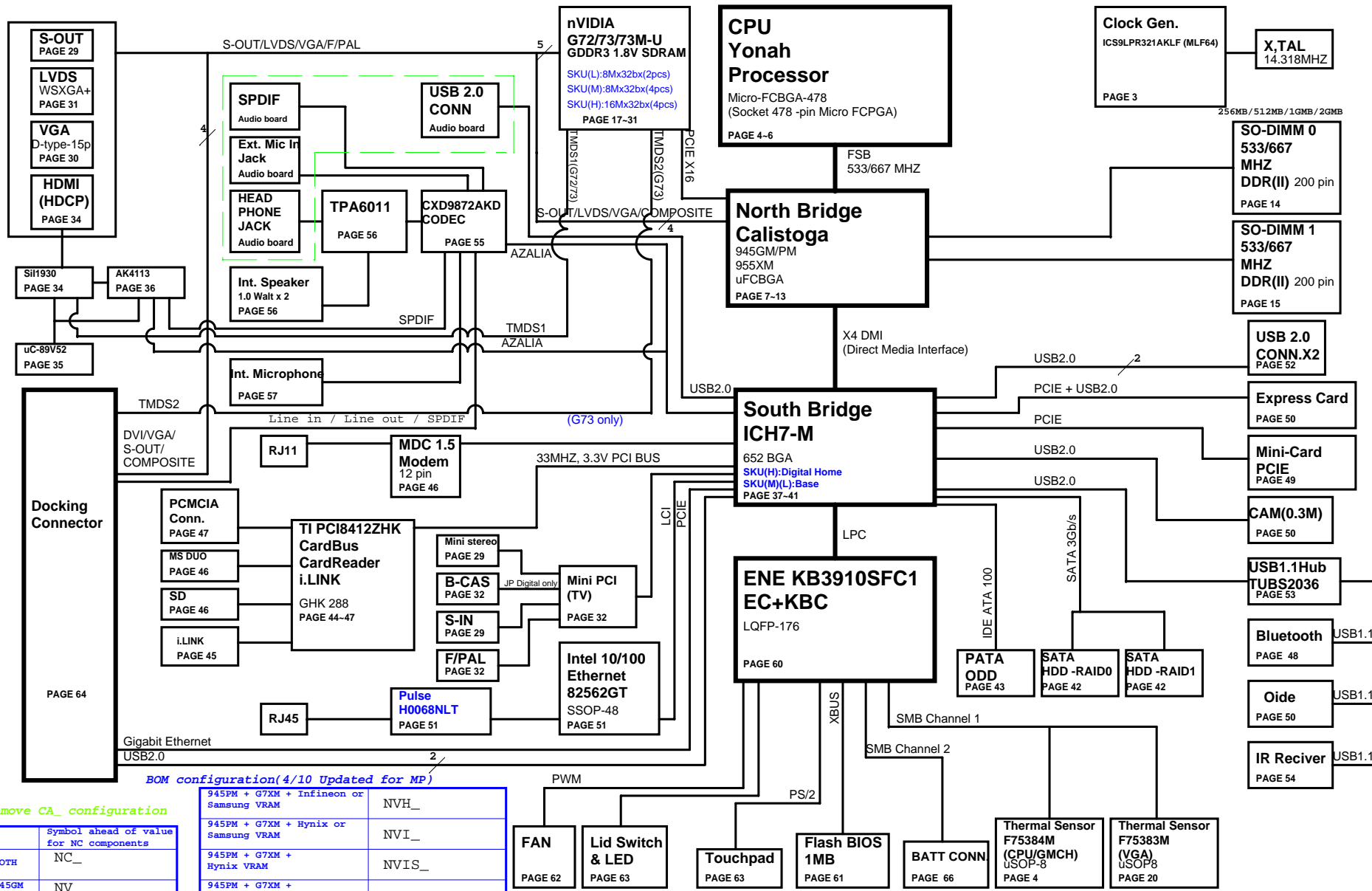
PCB P/N: 1P-0068100-8011 (FUBAI)
1P-0068500-8011 (Hannstar)

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MS21(CALISTOGA PM+Gfx Block Diagram)

Red texts:
New modified



Remove CA_configuration

Symbol	Value
BOTH	NC_
945GM	NV_
945PM + G72M	NV73_
945PM + G73M	NV72_
945PM + G72M or G73M-U	NV73Only_

Configuration	Value
945PM + G7XM + Infineon or Samsung VRAM	NVH_
945PM + G7XM + Hynix or Samsung VRAM	NVI_
945PM + G7XM + Hynix VRAM	NVIS_
945PM + G7XM + Infineon VRAM	NVHS_
945PM + G72M or G73M	NV16M_, NV73U_
945PM + G73M-U	NV8M_, NV7273_
*JP Digital TV Tuner SKU & No Tuner SKU not stick	JDTVNC_

BOM configuration(4/10 Updated for MP)

NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_MINI
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG
NC_10P_50V_E_N	2	1	PCLK_JIG

close to terminal side (For EMI)

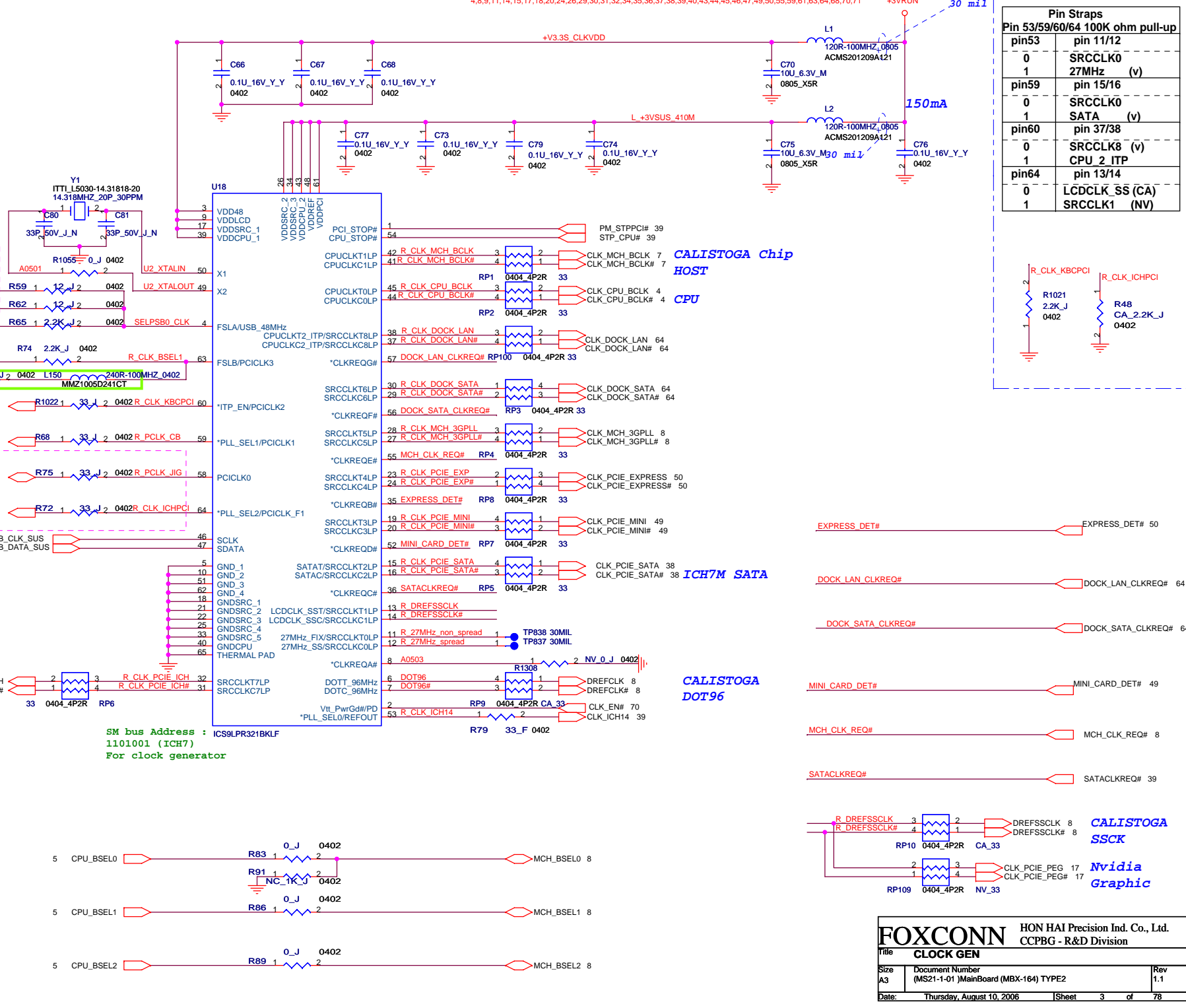
Length as short as possible.

This dumping resistor and FB should be placed close to U18, update for MOR requirement on12/23.

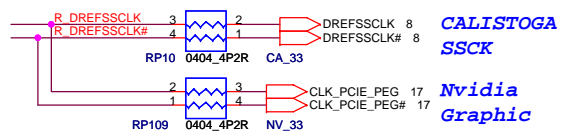
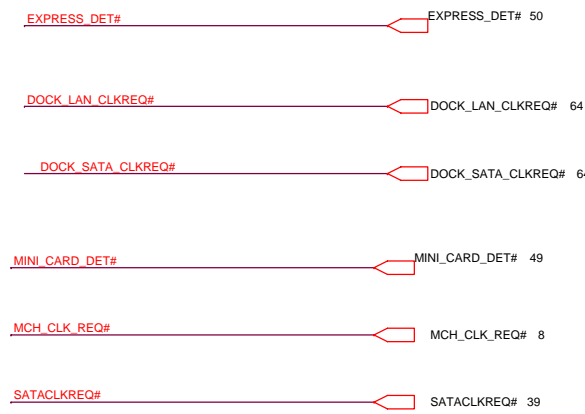
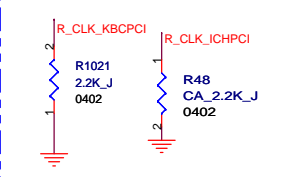
ICH7 DMI

FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100
0	1	133	100
1	0	200	100
1	1	166	100



Pin Straps	
Pin 53/59/60/64 100K ohm pull-up	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin 59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin 60	pin 37/38
0	SRCCLK8 (v)
1	CPU 2 ITP
pin 64	pin 13/14
0	LDCCLK_SS (CA)
1	SRCCLK1 (NV)

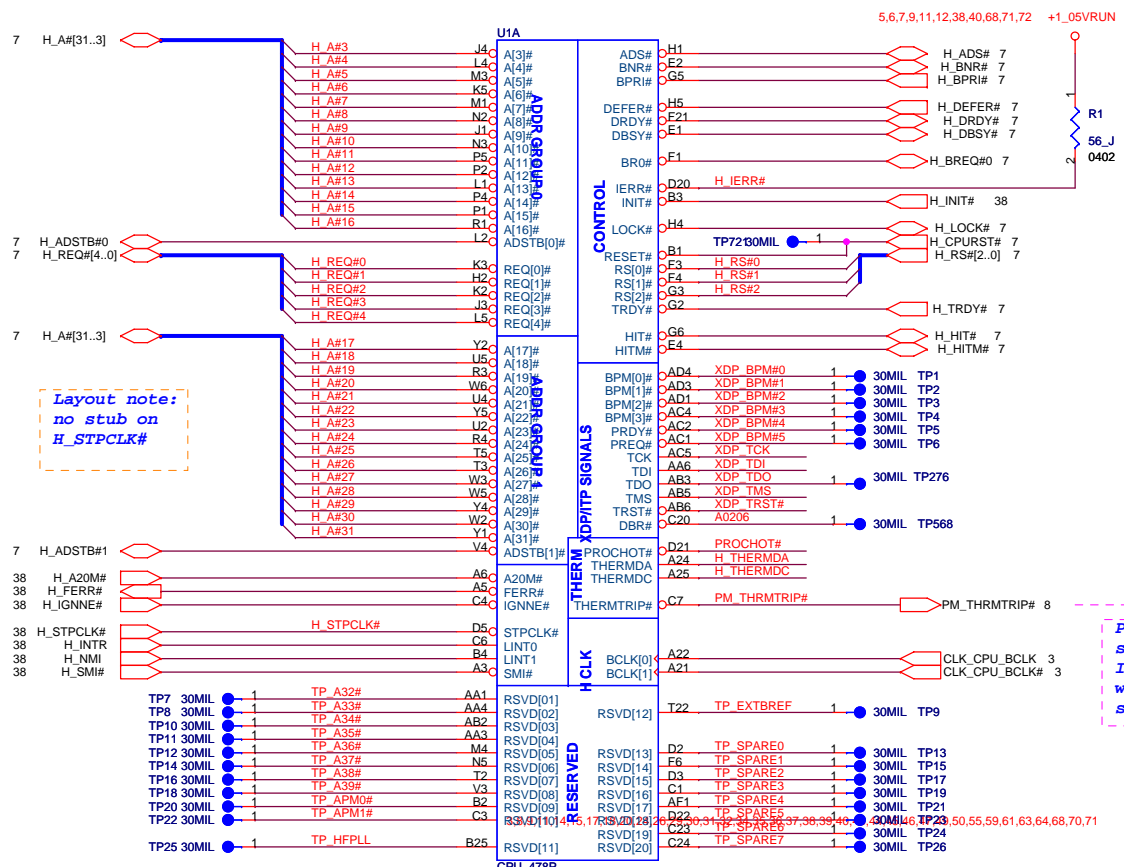


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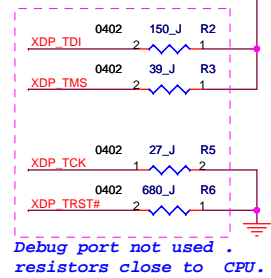
File: **CLOCK_GEN**

Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
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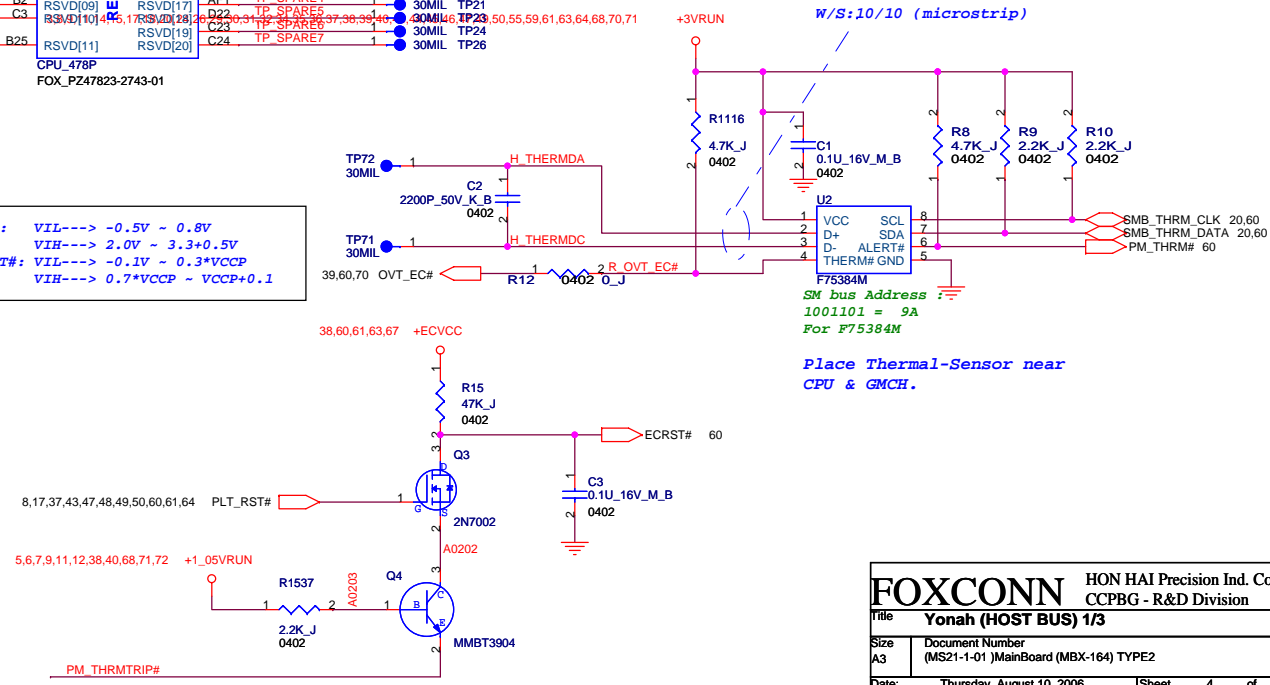
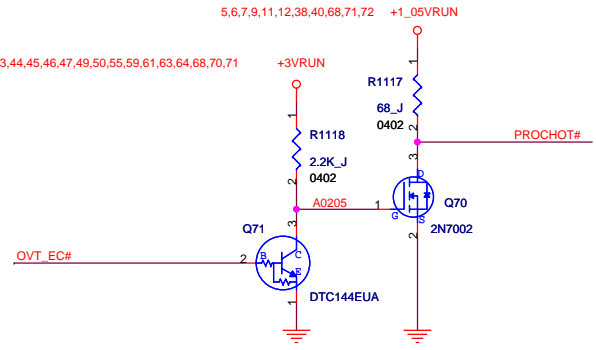
Layout note:
no stub on
H_STPCLK#



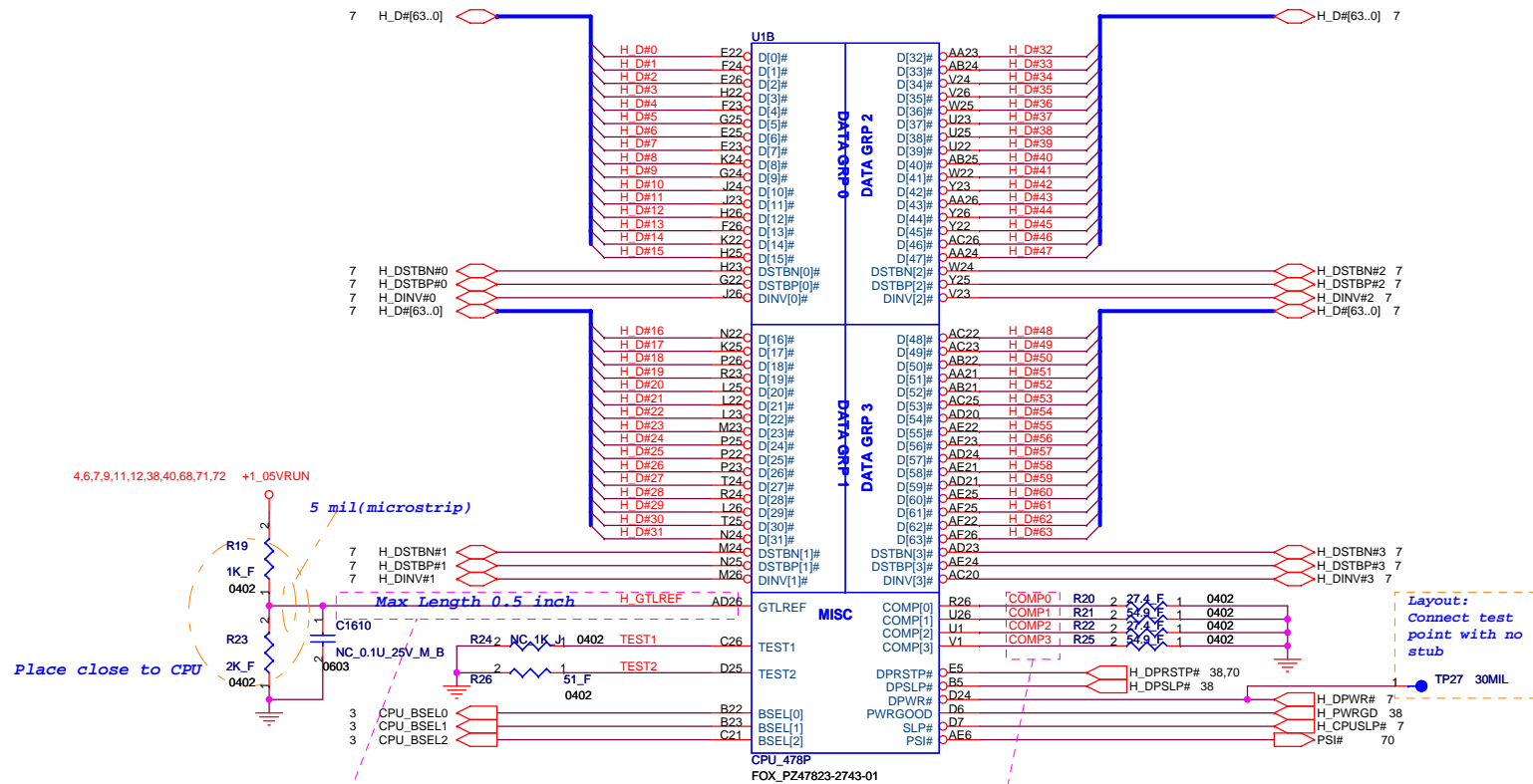
PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)

A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL----> -0.5V - 0.8V
VIH----> 2.0V - 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V - 0.3*VCCP
VIH----> 0.7*VCCP - VCCP+0.1



Place Thermal-Sensor near
CPU & GMCH.



4,6,7,9,11,12,38,40,68,71,72 +1_05VRUN

5 mil(microstrip)

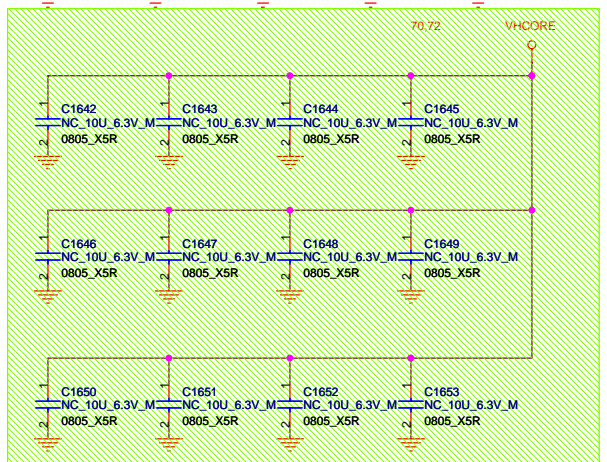
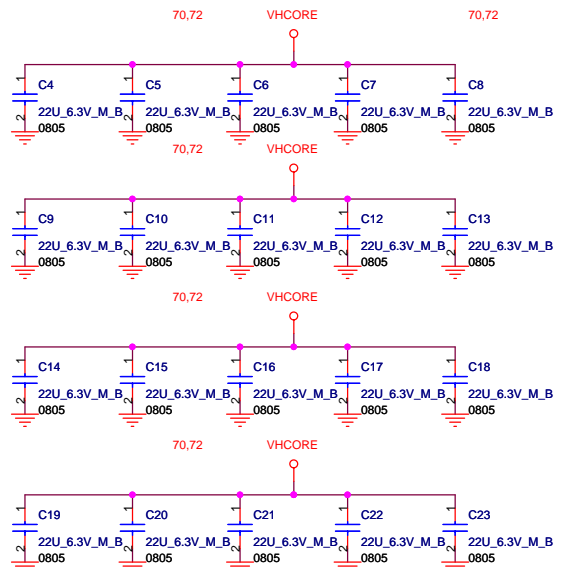
Max Length 0.5 inch

Place close to CPU

Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make
trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make
trace length shorter then 0.5".

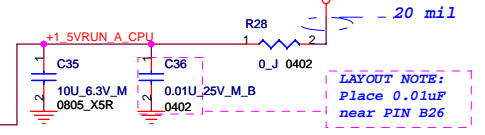
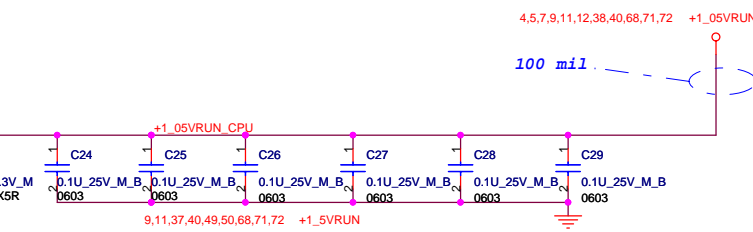
Layout:
Connect test
point with no
stub



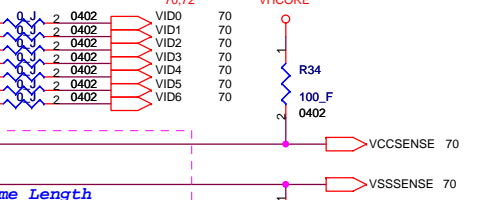
Backup 10uF capacitors for 22uF shortage.

U1C		U1D	
A7	VCC[001]	A4	VSS[001]
A9	VCC[002]	A8	VSS[002]
A10	VCC[003]	A11	VSS[003]
A12	VCC[004]	A14	VSS[004]
A13	VCC[005]	A16	VSS[005]
A15	VCC[006]	A19	VSS[006]
A17	VCC[007]	A23	VSS[007]
A18	VCC[008]	A26	VSS[008]
A20	VCC[009]	B6	VSS[009]
B7	VCC[010]	B9	VSS[010]
B9	VCC[011]	B11	VSS[011]
B10	VCC[012]	B13	VSS[012]
B12	VCC[013]	B16	VSS[013]
B14	VCC[014]	B19	VSS[014]
B15	VCC[015]	B21	VSS[015]
B17	VCC[016]	B24	VSS[016]
B18	VCC[017]	C5	VSS[017]
B20	VCC[018]	C8	VSS[018]
C9	VCC[019]	C11	VSS[019]
C10	VCC[020]	C14	VSS[020]
C12	VCC[021]	C16	VSS[021]
C13	VCC[022]	C19	VSS[022]
C15	VCC[023]	C22	VSS[023]
C17	VCC[024]	C25	VSS[024]
C18	VCC[025]	C27	VSS[025]
D9	VCC[026]	C28	VSS[026]
D10	VCC[027]	C29	VSS[027]
D12	VCC[028]	D1	VSS[028]
D14	VCC[029]	D4	VSS[029]
D15	VCC[030]	D8	VSS[030]
D17	VCC[031]	D11	VSS[031]
D18	VCC[032]	D13	VSS[032]
E7	VCC[033]	D19	VSS[033]
E9	VCC[034]	D23	VSS[034]
E10	VCC[035]	D26	VSS[035]
E13	VCC[036]	E3	VSS[036]
E15	VCC[037]	E6	VSS[037]
E17	VCC[038]	E8	VSS[038]
E18	VCC[039]	E11	VSS[039]
E20	VCC[040]	E14	VSS[040]
F7	VCC[041]	E16	VSS[041]
F9	VCC[042]	E19	VSS[042]
F10	VCC[043]	E21	VSS[043]
F12	VCC[044]	E24	VSS[044]
F14	VCC[045]	F8	VSS[045]
F15	VCC[046]	F11	VSS[046]
F17	VCC[047]	F13	VSS[047]
F18	VCC[048]	F16	VSS[048]
F20	VCC[049]	F19	VSS[049]
AA7	VCC[050]	F2	VSS[050]
AA9	VCC[051]	F22	VSS[051]
AA10	VCC[052]	F25	VSS[052]
AA12	VCC[053]	G4	VSS[053]
AA13	VCC[054]	G1	VSS[054]
AA15	VCC[055]	G23	VSS[055]
AA17	VCC[056]	G26	VSS[056]
AA18	VCC[057]	H3	VSS[057]
AA20	VCC[058]	H6	VSS[058]
AB9	VCC[059]	H21	VSS[059]
AC10	VCC[060]	H24	VSS[060]
AB10	VCC[061]	J2	VSS[061]
AB12	VCC[062]	N5	VSS[062]
AB14	VCC[063]	J25	VSS[063]
AB15	VCC[064]	K1	VSS[064]
AB17	VCC[065]	K4	VSS[065]
AB18	VCC[066]	K23	VSS[066]
	VCC[067]	K26	VSS[067]
		L3	VSS[068]
		L6	VSS[069]
		L21	VSS[070]
		L24	VSS[071]
		M2	VSS[072]
		M5	VSS[073]
		M22	VSS[074]
		M25	VSS[075]
		N1	VSS[076]
		N4	VSS[077]
		N23	VSS[078]
		N26	VSS[079]
		P3	VSS[080]
			VSS[081]
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			VSS[162]

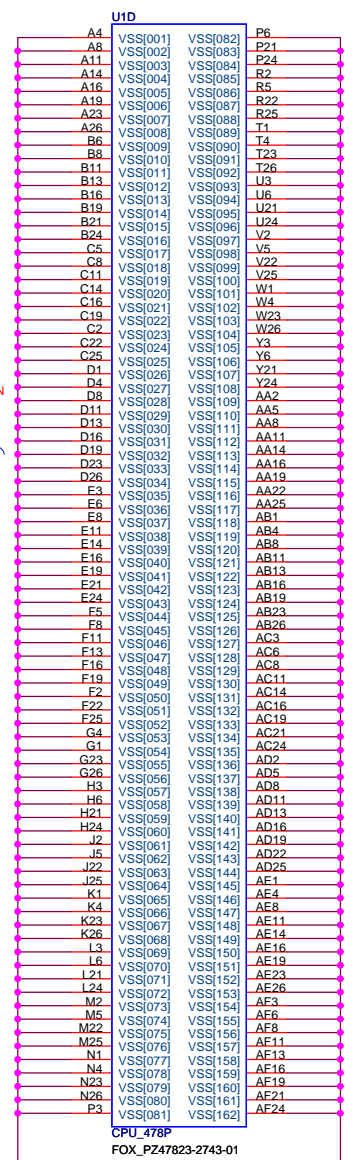
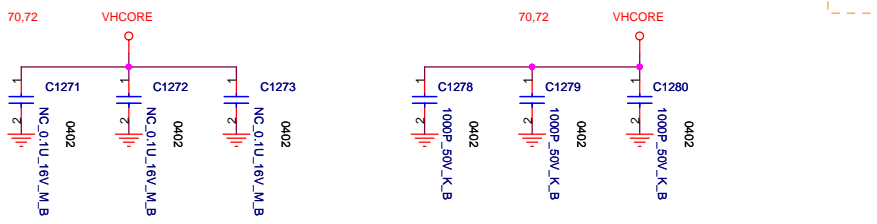
CPU_VCCA----->120mA
 CPU_VCCP----->2.5A
 CPU_VCC----->44A

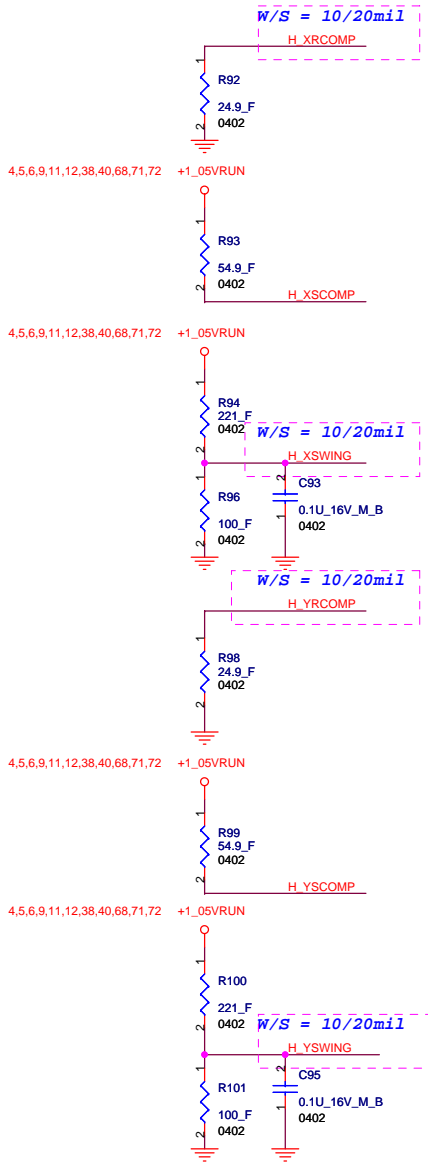


LAYOUT NOTE:
 Place 0.01uF near PIN B26



Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
 width=18 mil spacing=7 mil

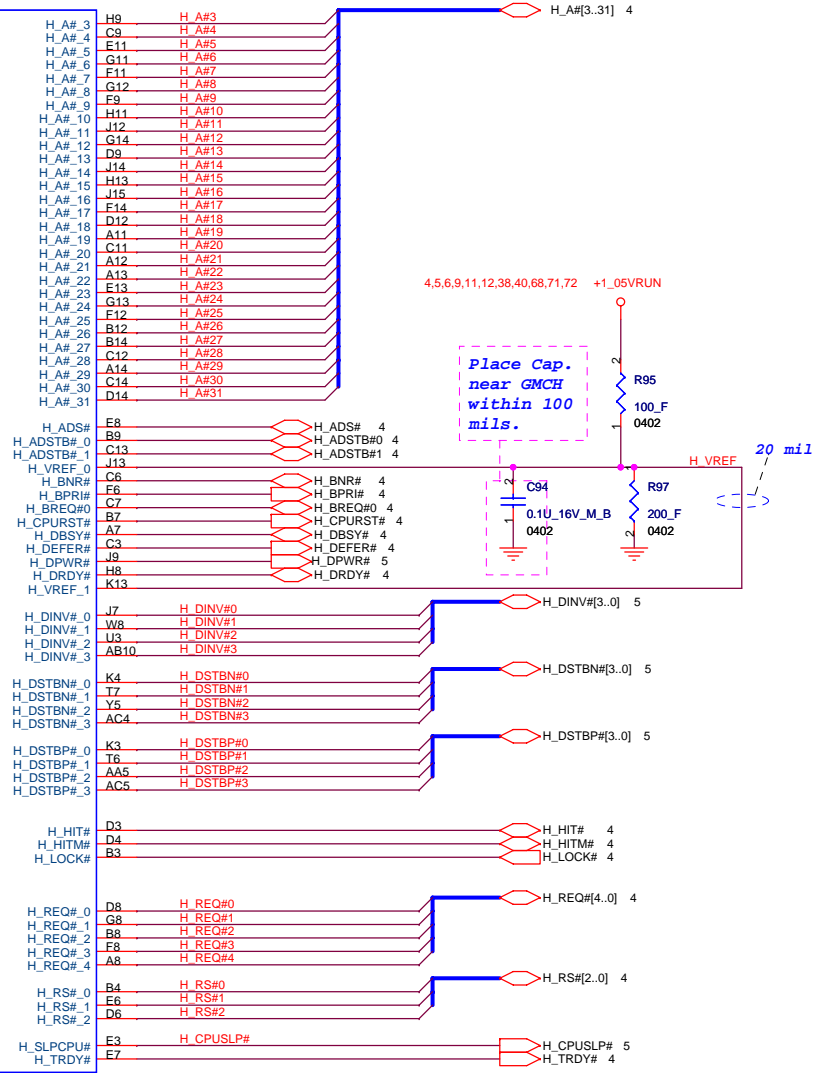




5 H_D#[63..0] H_D#[63..0]

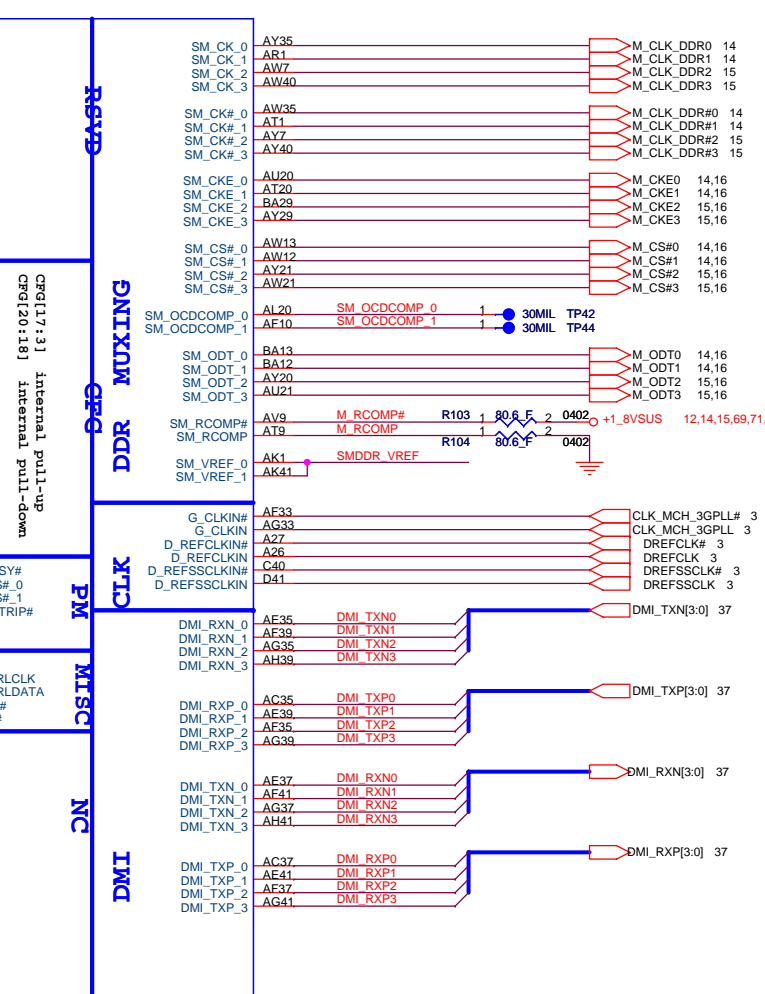
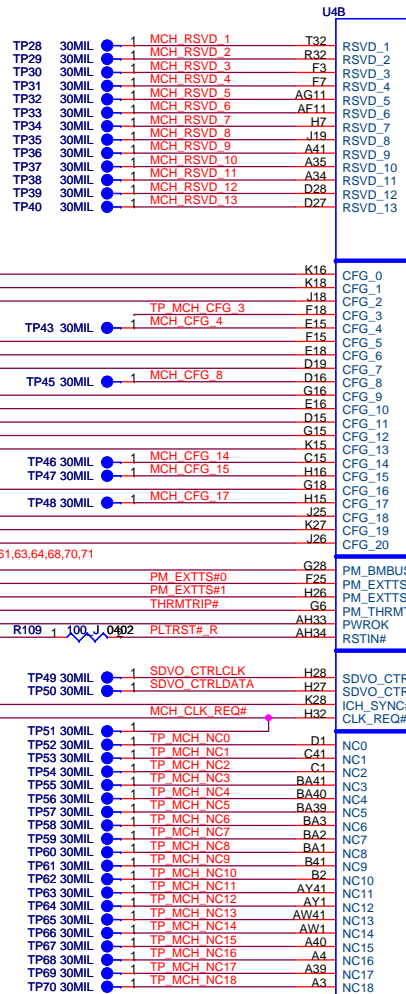
U4A	
H_D#0	F1
H_D#1	J1
H_D#2	H1
H_D#3	J6
H_D#4	H3
H_D#5	K2
H_D#6	G1
H_D#7	G2
H_D#8	K9
H_D#9	K1
H_D#10	K7
H_D#11	J8
H_D#12	H4
H_D#14	K11
H_D#15	G4
H_D#16	T10
H_D#17	W11
H_D#18	T3
H_D#19	U9
H_D#20	U7
H_D#21	U11
H_D#22	T11
H_D#23	W9
H_D#24	T1
H_D#25	T4
H_D#26	T4
H_D#27	W7
H_D#28	U5
H_D#29	T9
H_D#30	W6
H_D#31	T5
H_D#32	AB7
H_D#33	AA9
H_D#34	W4
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H_D#40	AB8
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H_D#42	AA4
H_D#43	AA7
H_D#44	AA2
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H_D#46	AA10
H_D#47	Y8
H_D#48	AA1
H_D#49	AB4
H_D#50	AC9
H_D#51	AB11
H_D#52	AC11
H_D#53	AB3
H_D#54	AC2
H_D#55	AD1
H_D#56	AD9
H_D#57	AC1
H_D#58	AD7
H_D#59	AC6
H_D#60	AB5
H_D#61	AD10
H_D#62	AD4
H_D#63	AC8
H_D#_0	H_D#_0
H_D#_1	H_D#_1
H_D#_2	H_D#_2
H_D#_3	H_D#_3
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H_D#_26	H_D#_26
H_D#_27	H_D#_27
H_D#_28	H_D#_28
H_D#_29	H_D#_29
H_D#_30	H_D#_30
H_D#_31	H_D#_31
H_D#_32	H_D#_32
H_D#_33	H_D#_33
H_D#_34	H_D#_34
H_D#_35	H_D#_35
H_D#_36	H_D#_36
H_D#_37	H_D#_37
H_D#_38	H_D#_38
H_D#_39	H_D#_39
H_D#_40	H_D#_40
H_D#_41	H_D#_41
H_D#_42	H_D#_42
H_D#_43	H_D#_43
H_D#_44	H_D#_44
H_D#_45	H_D#_45
H_D#_46	H_D#_46
H_D#_47	H_D#_47
H_D#_48	H_D#_48
H_D#_49	H_D#_49
H_D#_50	H_D#_50
H_D#_51	H_D#_51
H_D#_52	H_D#_52
H_D#_53	H_D#_53
H_D#_54	H_D#_54
H_D#_55	H_D#_55
H_D#_56	H_D#_56
H_D#_57	H_D#_57
H_D#_58	H_D#_58
H_D#_59	H_D#_59
H_D#_60	H_D#_60
H_D#_61	H_D#_61
H_D#_62	H_D#_62
H_D#_63	H_D#_63
H_XRCOMP	E1
H_XSCOMP	E2
H_XSWING	E4
H_YRCOMP	Y1
H_YSCOMP	U1
H_YSWING	W1
H_CLKIN	AG2
H_CLKIN#	AG1

HOST

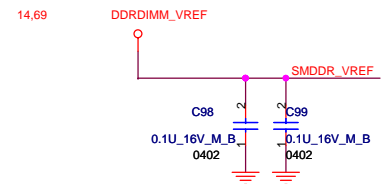
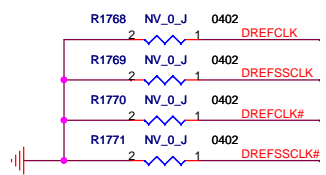
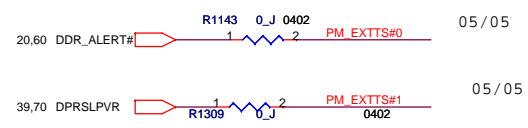


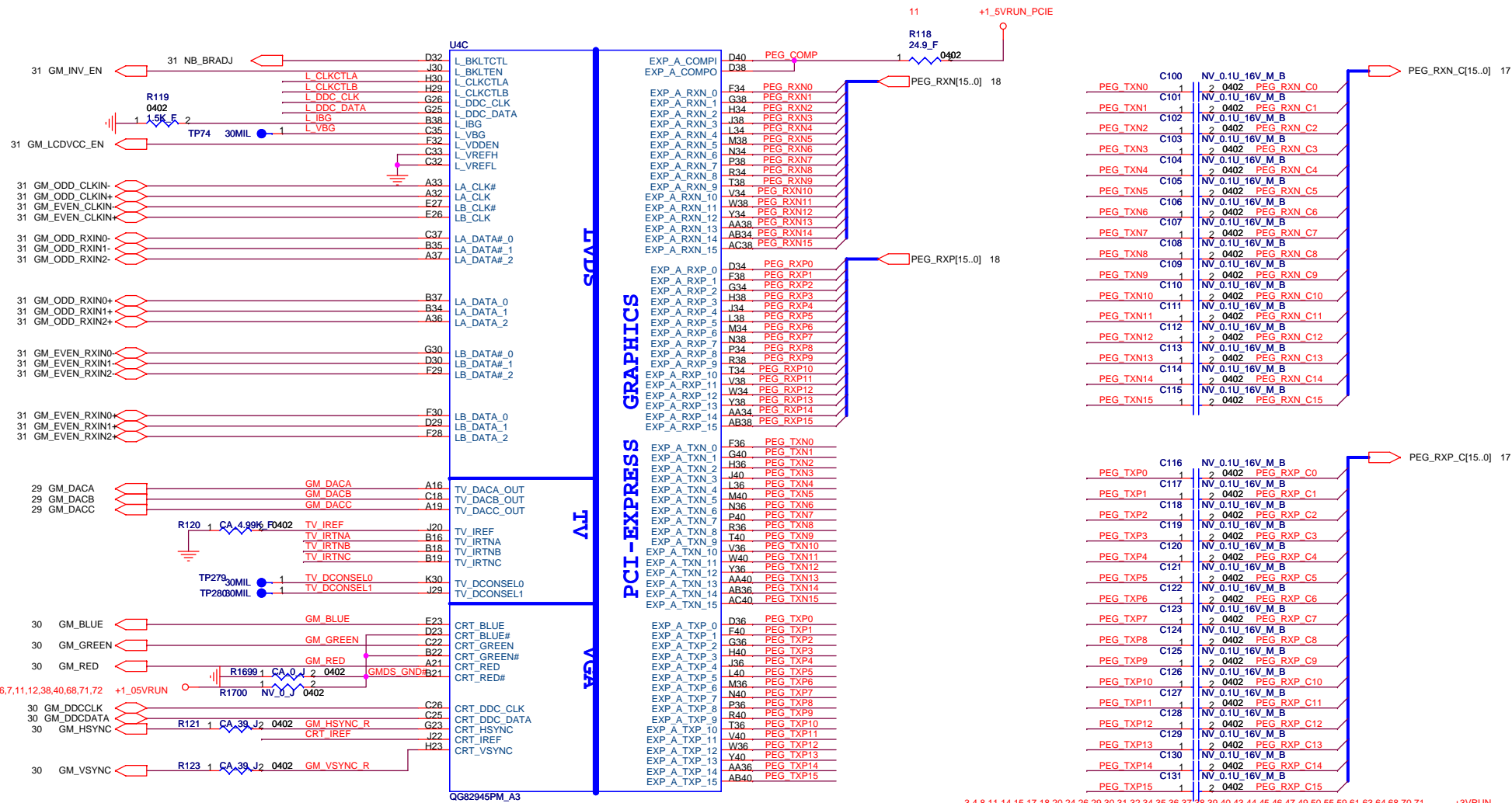
3 CLK_MCH_BCLK
3 CLK_MCH_BCLK#

QG82945PM_A3



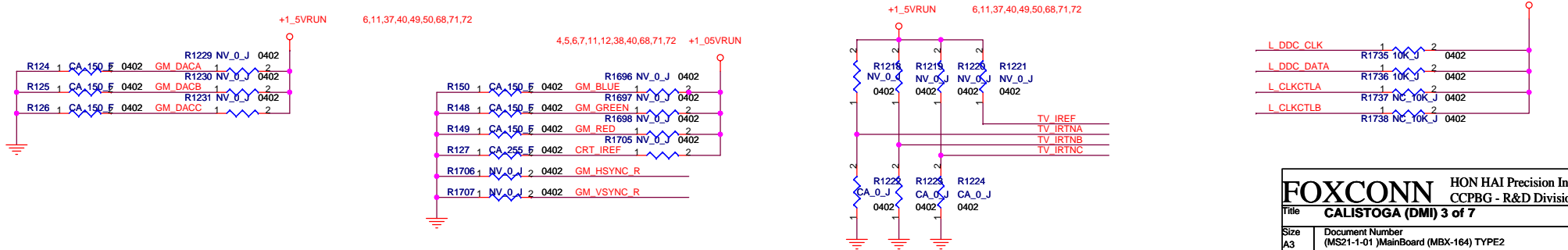
5/5 Remove R110 for PM_EXTTs#1 back up pull up res.
 ICH7 (DPRSLPVR) already have internal pull up





Signal Name	GM Pin	UMC Pin	Component
PEG_TXN0	C100	NV_01U_16V_M_B	2 0402 PEG_RXN C0
PEG_TXN1	C101	NV_01U_16V_M_B	2 0402 PEG_RXN C1
PEG_TXN2	C102	NV_01U_16V_M_B	2 0402 PEG_RXN C2
PEG_TXN3	C103	NV_01U_16V_M_B	2 0402 PEG_RXN C3
PEG_TXN4	C104	NV_01U_16V_M_B	2 0402 PEG_RXN C4
PEG_TXN5	C105	NV_01U_16V_M_B	2 0402 PEG_RXN C5
PEG_TXN6	C106	NV_01U_16V_M_B	2 0402 PEG_RXN C6
PEG_TXN7	C107	NV_01U_16V_M_B	2 0402 PEG_RXN C7
PEG_TXN8	C108	NV_01U_16V_M_B	2 0402 PEG_RXN C8
PEG_TXN9	C109	NV_01U_16V_M_B	2 0402 PEG_RXN C9
PEG_TXN10	C110	NV_01U_16V_M_B	2 0402 PEG_RXN C10
PEG_TXN11	C111	NV_01U_16V_M_B	2 0402 PEG_RXN C11
PEG_TXN12	C112	NV_01U_16V_M_B	2 0402 PEG_RXN C12
PEG_TXN13	C113	NV_01U_16V_M_B	2 0402 PEG_RXN C13
PEG_TXN14	C114	NV_01U_16V_M_B	2 0402 PEG_RXN C14
PEG_TXN15	C115	NV_01U_16V_M_B	2 0402 PEG_RXN C15

Signal Name	GM Pin	UMC Pin	Component
PEG_TXP0	C116	NV_01U_16V_M_B	2 0402 PEG_RXP C0
PEG_TXP1	C117	NV_01U_16V_M_B	2 0402 PEG_RXP C1
PEG_TXP2	C118	NV_01U_16V_M_B	2 0402 PEG_RXP C2
PEG_TXP3	C119	NV_01U_16V_M_B	2 0402 PEG_RXP C3
PEG_TXP4	C120	NV_01U_16V_M_B	2 0402 PEG_RXP C4
PEG_TXP5	C121	NV_01U_16V_M_B	2 0402 PEG_RXP C5
PEG_TXP6	C122	NV_01U_16V_M_B	2 0402 PEG_RXP C6
PEG_TXP7	C123	NV_01U_16V_M_B	2 0402 PEG_RXP C7
PEG_TXP8	C124	NV_01U_16V_M_B	2 0402 PEG_RXP C8
PEG_TXP9	C125	NV_01U_16V_M_B	2 0402 PEG_RXP C9
PEG_TXP10	C126	NV_01U_16V_M_B	2 0402 PEG_RXP C10
PEG_TXP11	C127	NV_01U_16V_M_B	2 0402 PEG_RXP C11
PEG_TXP12	C128	NV_01U_16V_M_B	2 0402 PEG_RXP C12
PEG_TXP13	C129	NV_01U_16V_M_B	2 0402 PEG_RXP C13
PEG_TXP14	C130	NV_01U_16V_M_B	2 0402 PEG_RXP C14
PEG_TXP15	C131	NV_01U_16V_M_B	2 0402 PEG_RXP C15



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CCPBG - R&D Division

Title: **CALISTOGA (DMI) 3 of 7**

Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 9 of 78	

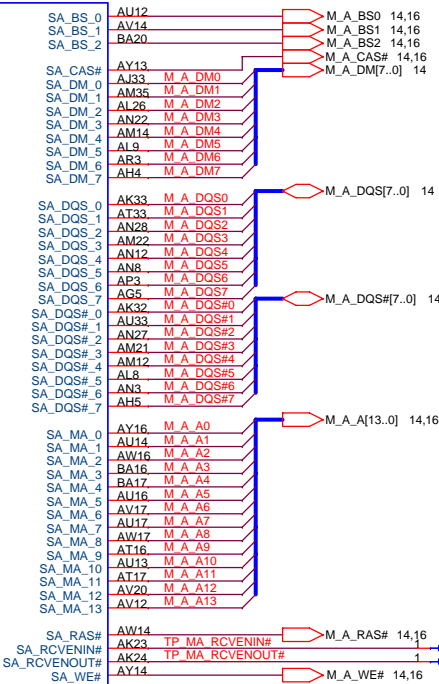
14 M_A_DQ[63.0]



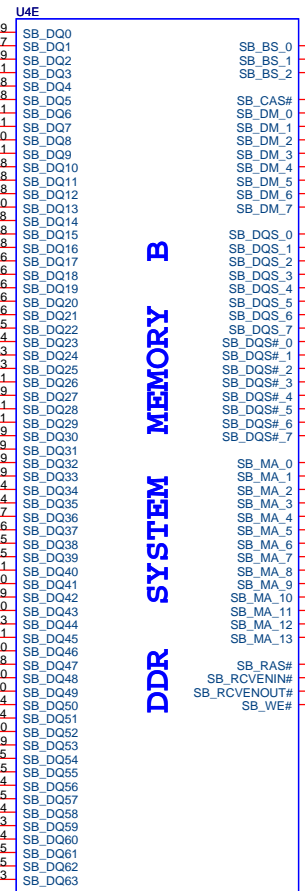
U4D

DDR SYSTEM MEMORY A

QG82945PM_A3



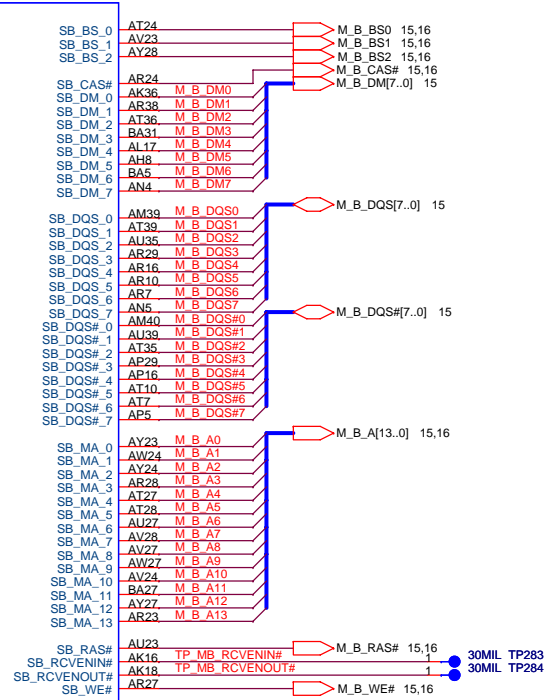
15 M_B_DQ[63.0]

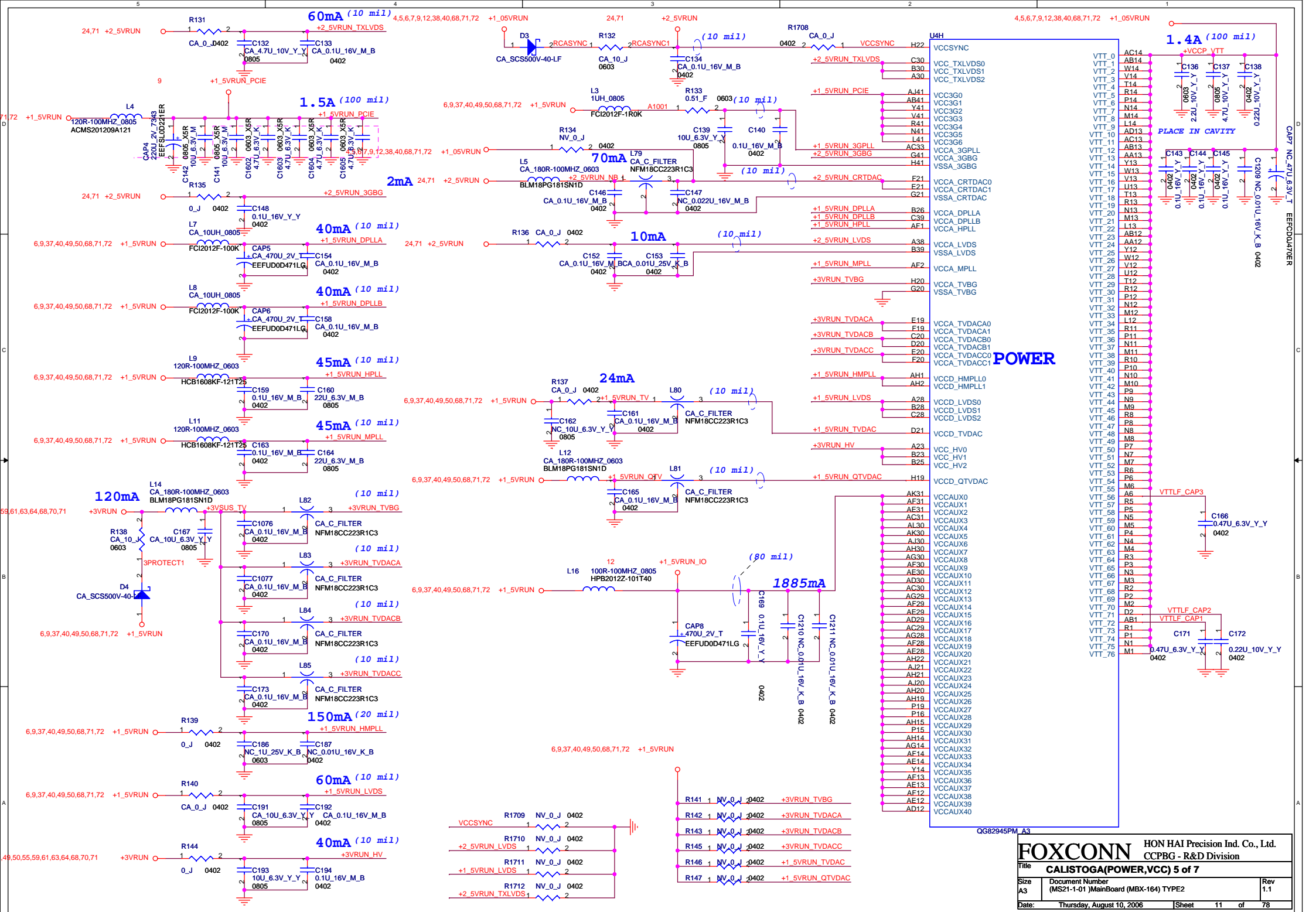


U4E

DDR SYSTEM MEMORY B

QG82945PM_A3

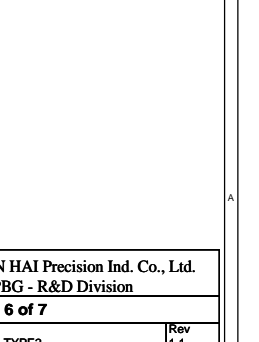
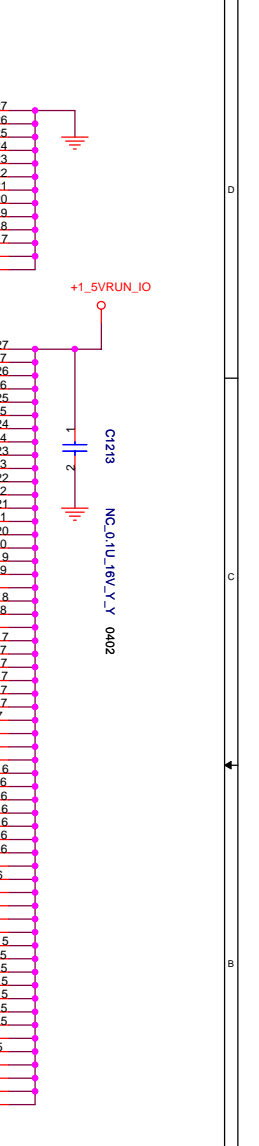
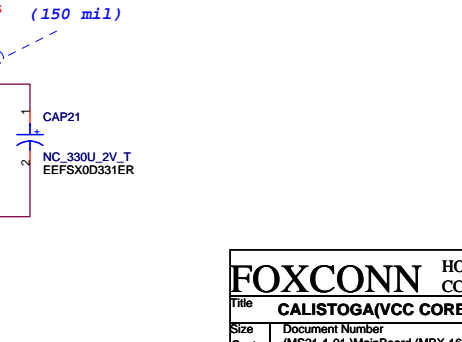
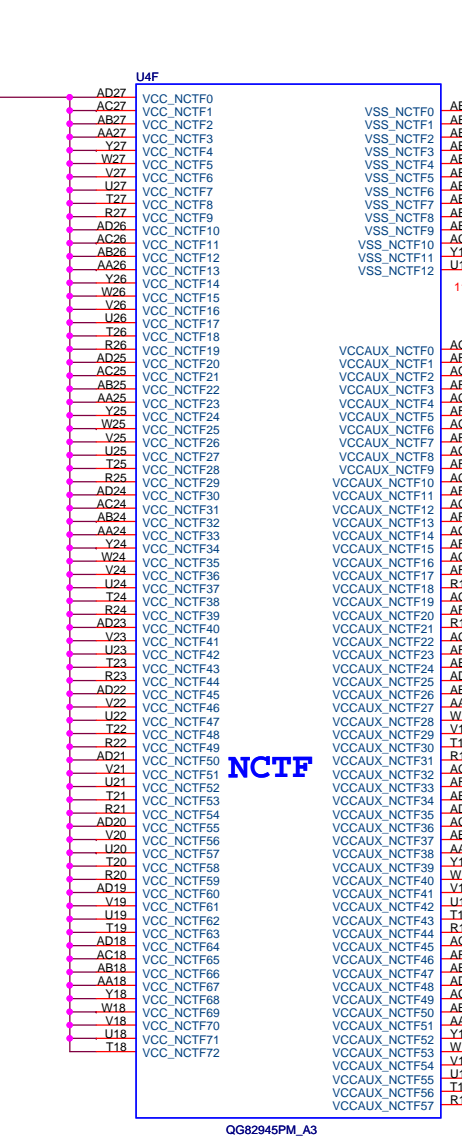
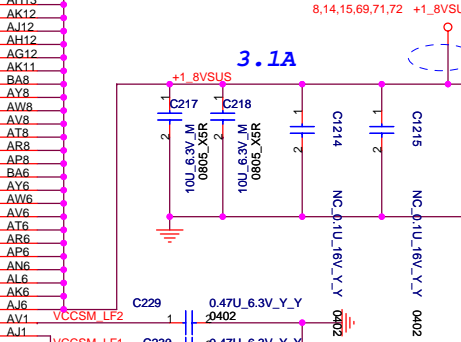
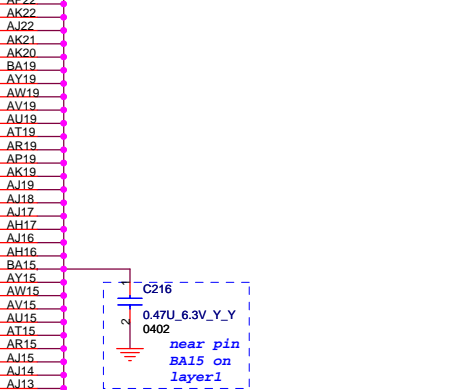
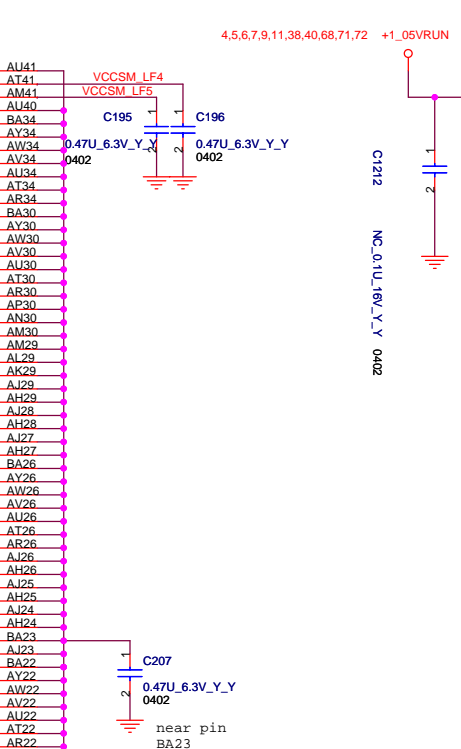
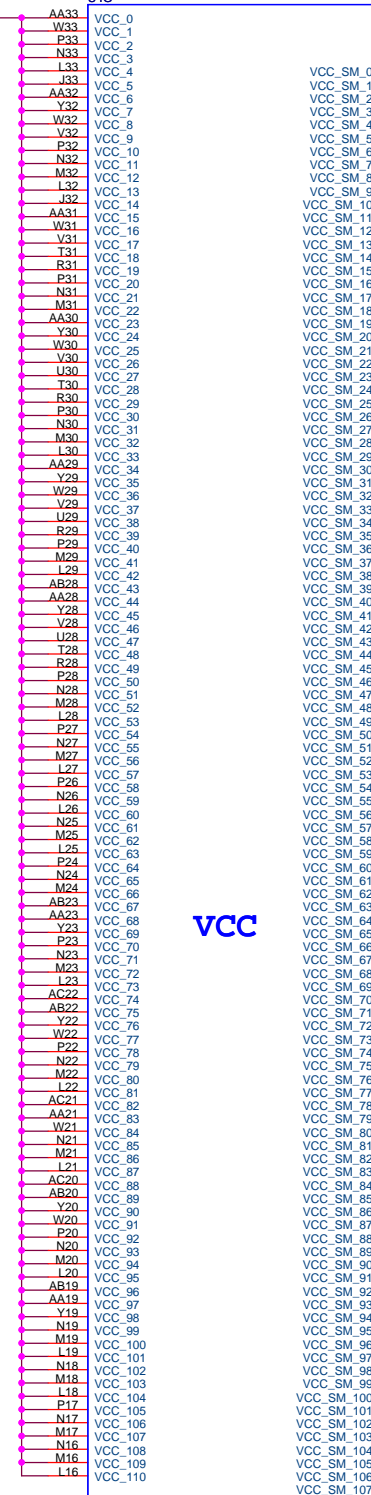
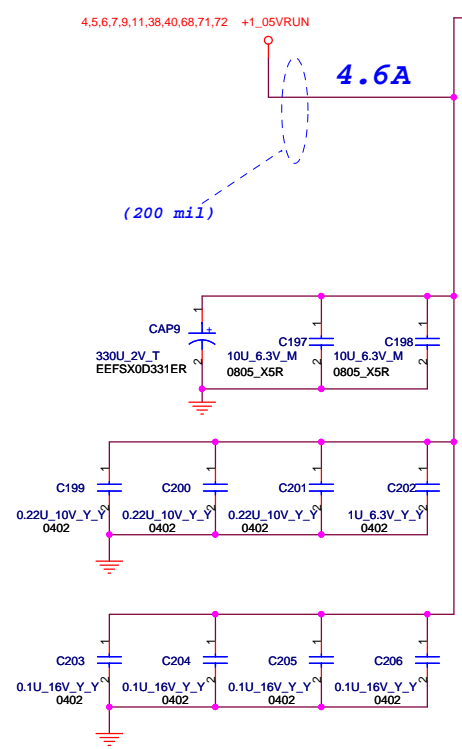




FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **CALISTOGA(POWER,VCC) 5 of 7**

Size	Document Number	Rev
A3	(MS21-01)MainBoard (MBX-164) TYPE2	1.1
Date:	Thursday, August 10, 2006	Sheet 11 of 78



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CALISTOGA(VCC CORE) 6 of 7	
Size	Document Number	Rev	
Custom	(MS21-1-01) MainBoard (MBX-164) TYPE2	1.1	
Date:	Thursday, August 10, 2006	Sheet	12 of 78

8 MCH_CFG_5 ← 1 ● 30MIL TP554

MCH_CFG_5
Low = DMIX2
High = DMIX4

8 MCH_CFG_6 ← 1 ● 30MIL TP556

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

MCH_CFG_18
Low = 1.05V(default)
High = 1.5V
(VCC_CORE Select)

8 MCH_CFG_18 ← 1 ● 30MIL TP555

MCH_CFG_19
Low = Normal(default)
High = LANES REVERSED
(DMI LANE REVERSAL)

8 MCH_CFG_19 ← 1 ● 30MIL TP558

8 TP_MCH_CFG_7 ← TP_MCH_CFG_7

MCH_CFG_7
(CPU Strap)
Low = RSVD
High = Mobile Yonah processor

8 MCH_CFG_9 ← 1 ● 30MIL TP559

MCH_CFG_9
(PCIe Graphics Lane)
Low = Reverse Lane
High = Normal operation
For layout convenience

MCH_CFG_20
Low = Only SDVO or PCIE x1 is operational (defaults)
High = SDVO and PCIE x1 are operating simultaneously via the PEG port
(PCIe Backward Interoperability mode)

8 MCH_CFG_20 ← 1 ● 30MIL TP561

8 MCH_CFG_10 ← 1 ● 30MIL TP560

MCH_CFG_10
(HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

8 MCH_CFG_11 ← 1 ● R162 NC 2.2K Ω 0402

MCH_CFG_11
(PSB 4x CLK ENABLE)
Low = Calistoga
High = Reserved

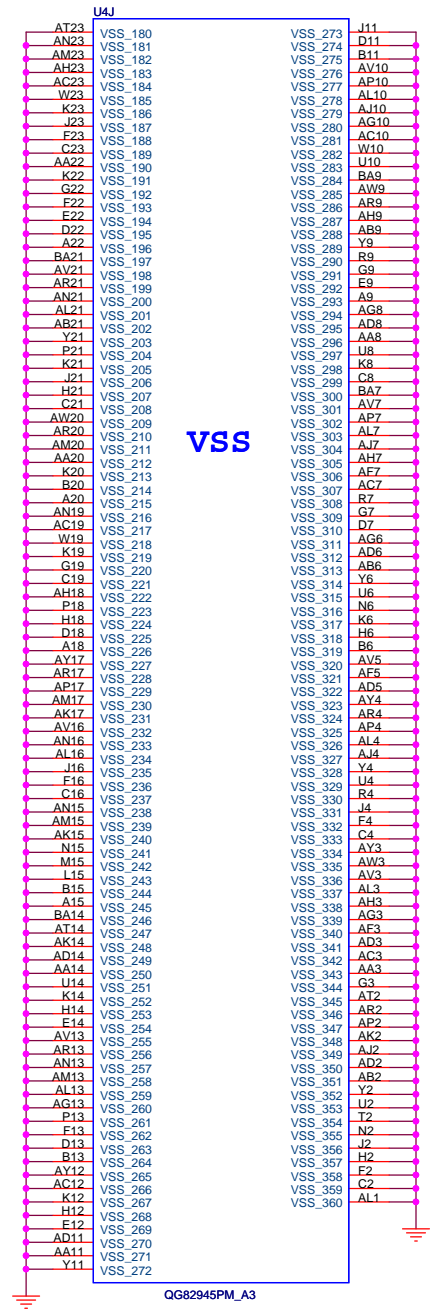
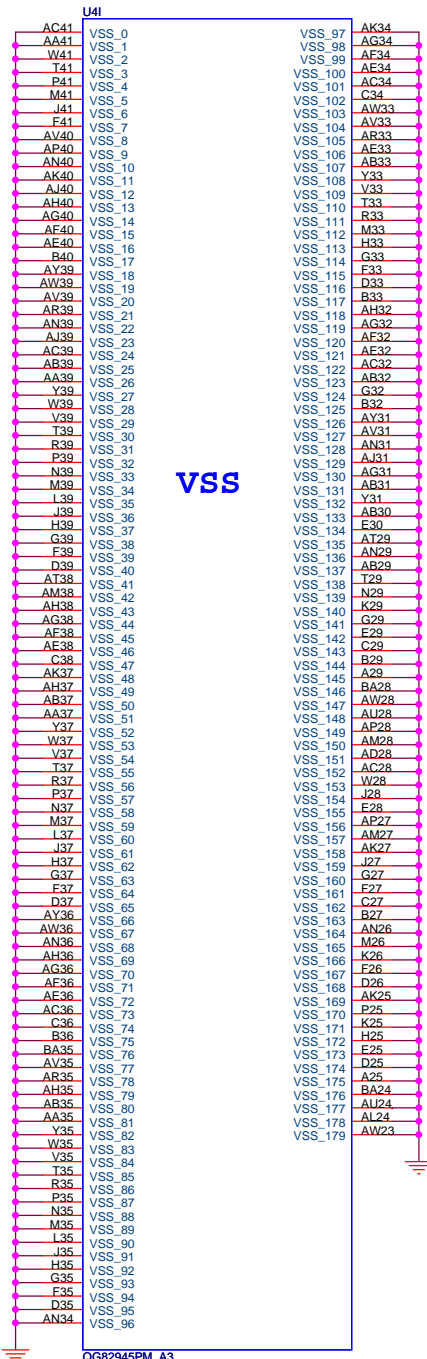
8 MCH_CFG_12 ← 1 ● 30MIL TP562

8 MCH_CFG_13 ← 1 ● 30MIL TP563

MCH_CFG [13:12]
(XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

8 MCH_CFG_16 ← 1 ● 30MIL TP564

MCH_CFG_16
(FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable

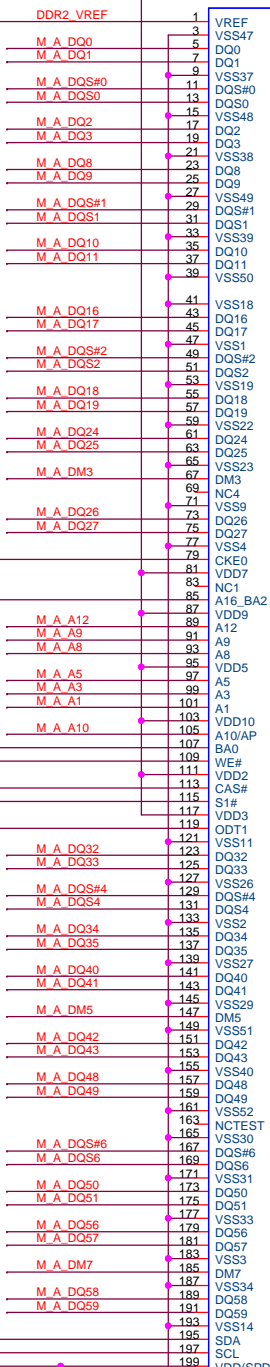
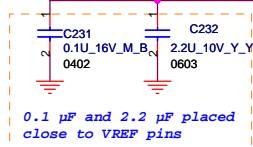


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title: CALISTOGA(VSS) 7 of 7
Size: Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2 Rev 1.1
Date: Thursday, August 10, 2006 Sheet 13 of 78

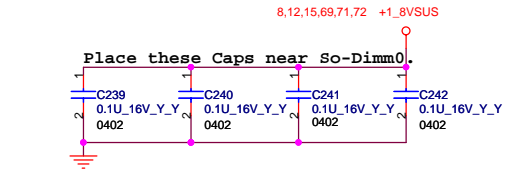
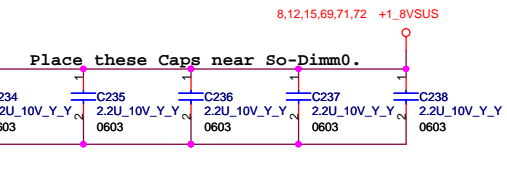
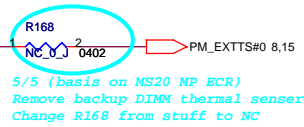
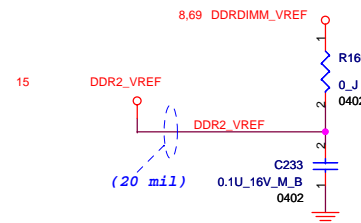
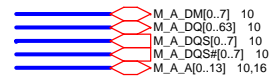
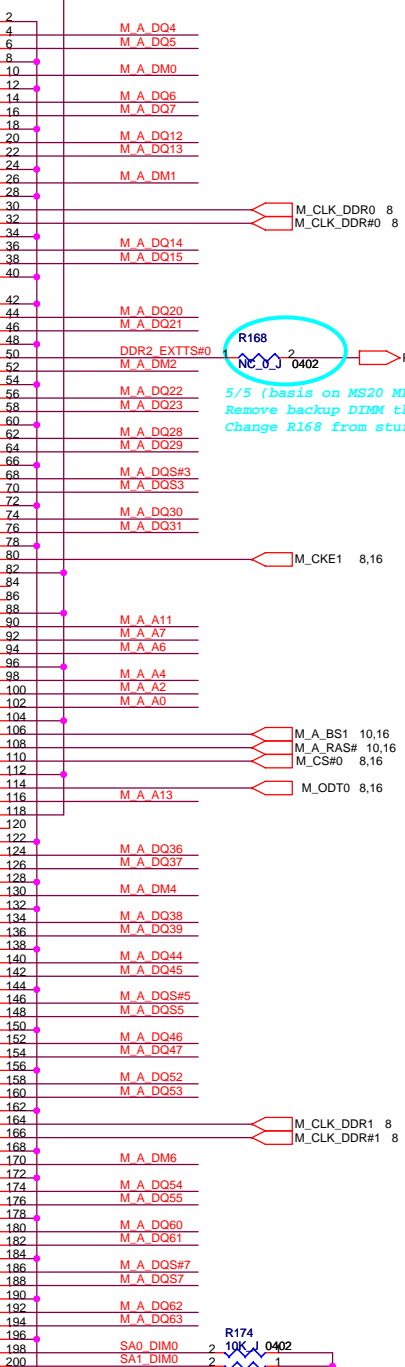
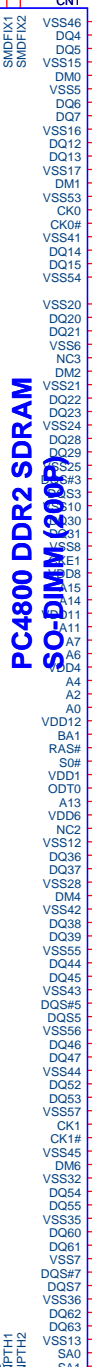
8,12,15,69,71,72 +1_8VSUS

+1_8VSUS 8,12,15,69,71,72

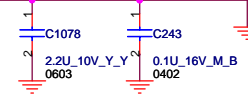
1.8V per DIMM=3.08A



PC4800 DDR2 SDRAM SO-DIMM (200P)



3,15,39,50 SMB_DATA_SUS
3,15,39,50 SMB_CLK_SUS
+3VRUN

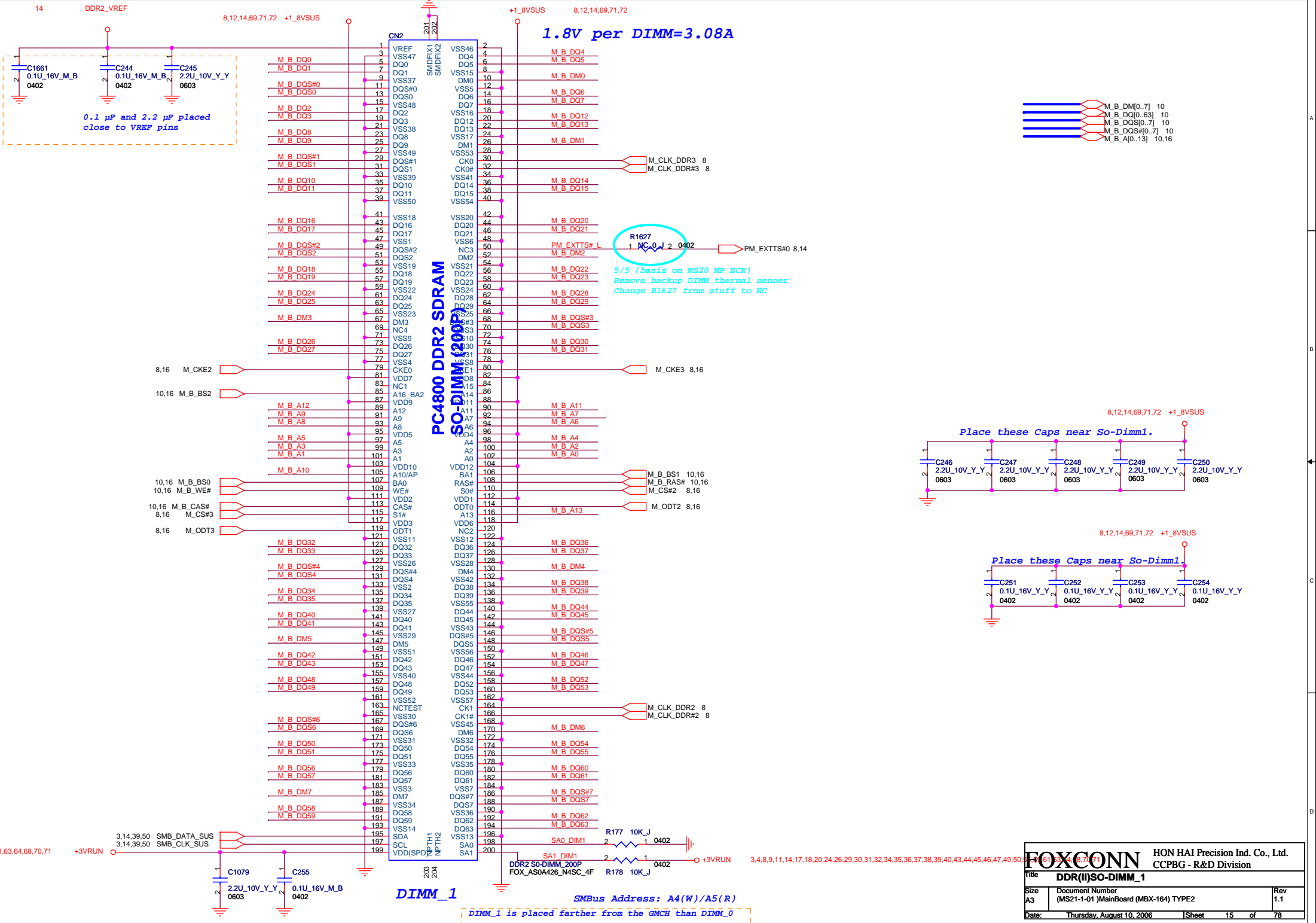


DIMM_0

DDR2 SO-DIMM_200P
FOX_AS0A426_N4RC_4F
SMBus Address: A0(W)/A1(R)

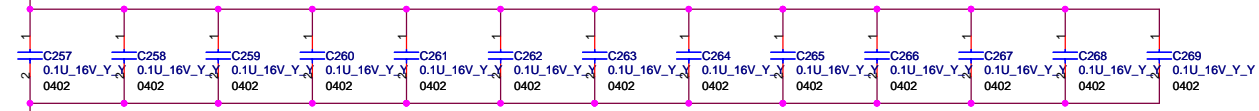
Place DIMM_0 near GMCH

FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title DDR(II)SO-DIMM_0		
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 14	of 78



69.72

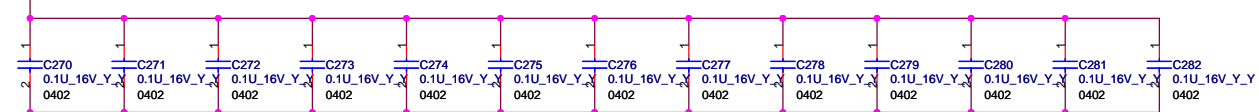
+0_9VSUS



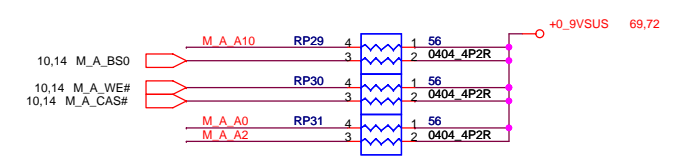
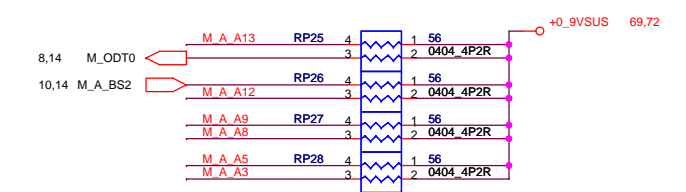
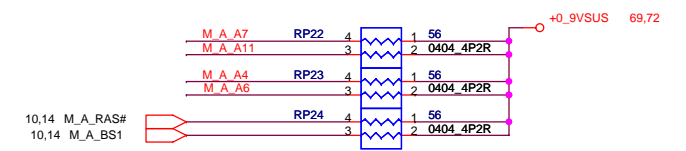
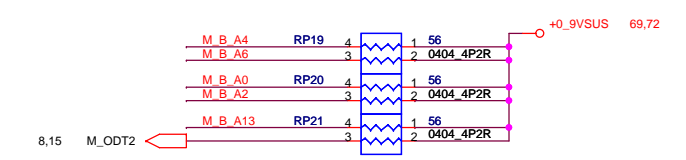
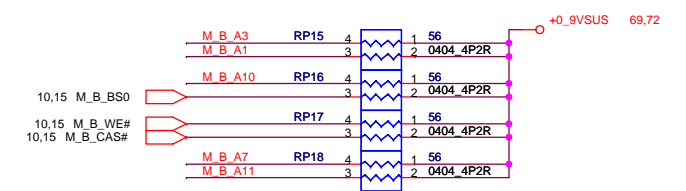
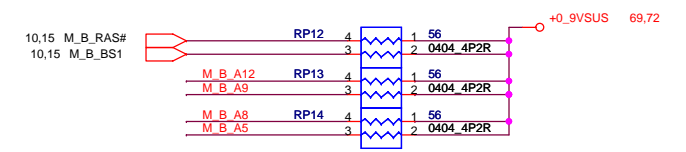
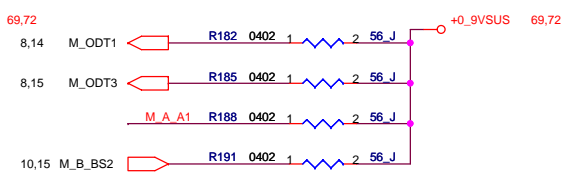
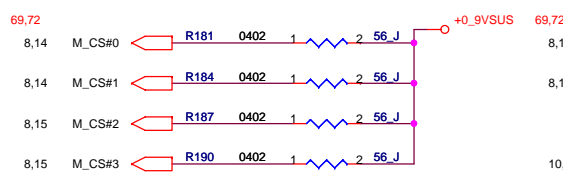
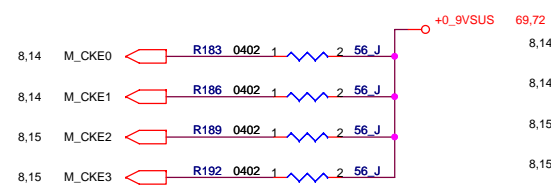
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

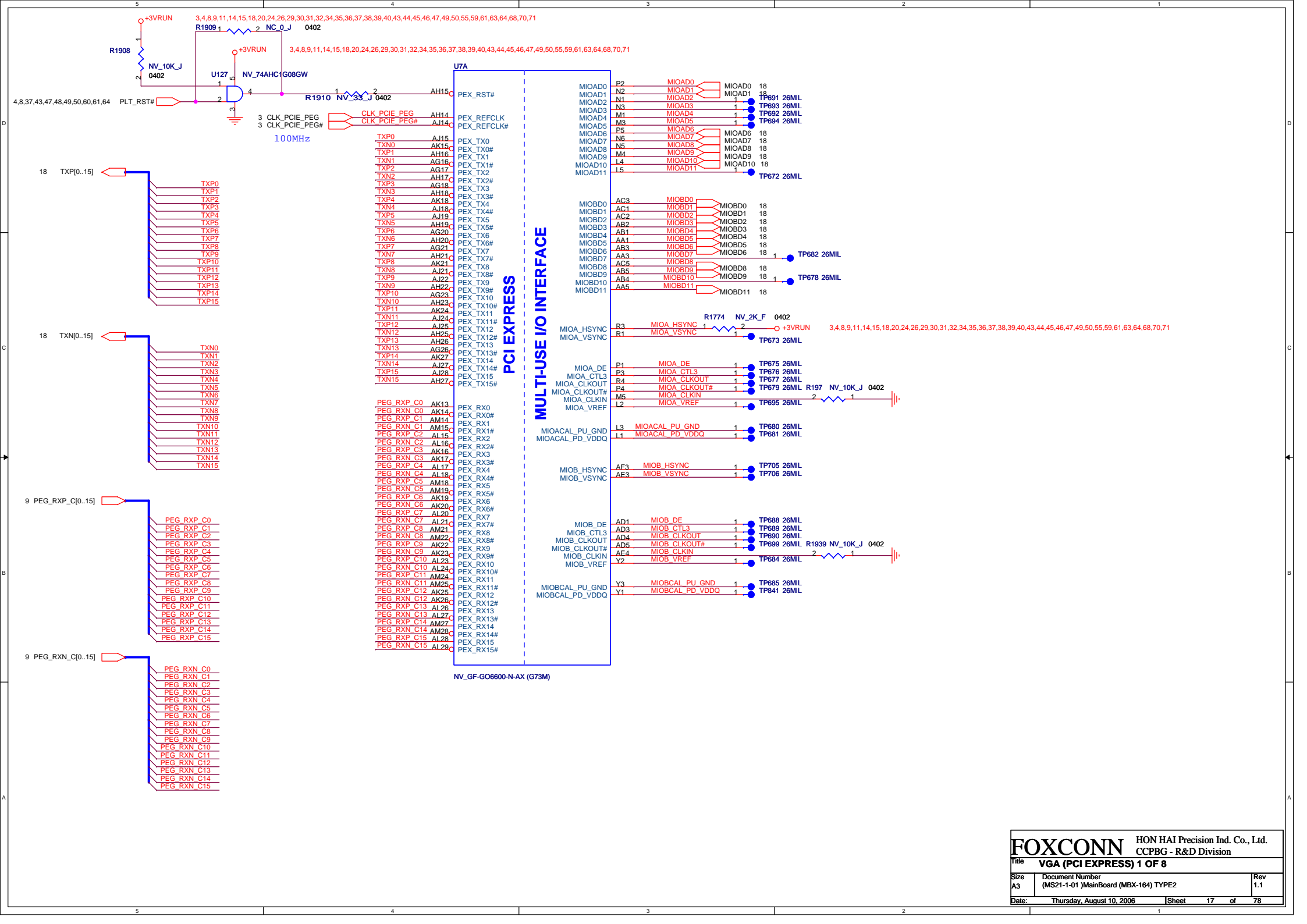
69.72

+0_9VSUS



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS





3,4,8,9,11,14,15,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71

3,4,8,9,11,14,15,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71

4,8,37,43,47,48,49,50,60,61,64

3 CLK_PCIE_PEG#

3 CLK_PCIE_PEG#

100MHz

18 TXP[0..15]

TXP0 AK15C

TXP1 AH16C

TXP2 AG16C

TXP3 AH17C

TXP4 AG17C

TXP5 AH18C

TXP6 AG18C

TXP7 AH19C

TXP8 AG20C

TXP9 AH20C

TXP10 AG21C

TXP11 AH21C

TXP12 AG22C

TXP13 AH22C

TXP14 AG23C

TXP15 AH23C

18 TXN[0..15]

TXN0 AK15C

TXN1 AH16C

TXN2 AG16C

TXN3 AH17C

TXN4 AG17C

TXN5 AH18C

TXN6 AG18C

TXN7 AH19C

TXN8 AG20C

TXN9 AH20C

TXN10 AG21C

TXN11 AH21C

TXN12 AG22C

TXN13 AH22C

TXN14 AG23C

TXN15 AH23C

9 PEG_RXP_C[0..15]

PEG_RXP_C0 AK13C

PEG_RXP_C1 AM14C

PEG_RXP_C2 AL15C

PEG_RXP_C3 AK16C

PEG_RXP_C4 AL17C

PEG_RXP_C5 AM18C

PEG_RXP_C6 AK19C

PEG_RXP_C7 AL20C

PEG_RXP_C8 AM21C

PEG_RXP_C9 AM22C

PEG_RXP_C10 AL23C

PEG_RXP_C11 AL24C

PEG_RXP_C12 AM25C

PEG_RXP_C13 AK26C

PEG_RXP_C14 AL27C

PEG_RXP_C15 AM28C

9 PEG_RXN_C[0..15]

PEG_RXN_C0 AL29C

PEG_RXN_C1 AL28C

PEG_RXN_C2 AM28C

PEG_RXN_C3 AL27C

PEG_RXN_C4 AL26C

PEG_RXN_C5 AL25C

PEG_RXN_C6 AL24C

PEG_RXN_C7 AM24C

PEG_RXN_C8 AL23C

PEG_RXN_C9 AM23C

PEG_RXN_C10 AL22C

PEG_RXN_C11 AM22C

PEG_RXN_C12 AL21C

PEG_RXN_C13 AM21C

PEG_RXN_C14 AL20C

PEG_RXN_C15 AM20C

PCI EXPRESS

MULTI-USE I/O INTERFACE

U7A

PEX_RST#

PEX_REFCLK

PEX_REFCLK#

PEX_TX0#

PEX_TX0#

PEX_TX1#

PEX_TX1#

PEX_TX2#

PEX_TX2#

PEX_TX3#

PEX_TX3#

PEX_TX4#

PEX_TX4#

PEX_TX5#

PEX_TX5#

PEX_TX6#

PEX_TX6#

PEX_TX7#

PEX_TX7#

PEX_TX8#

PEX_TX8#

PEX_TX9#

PEX_TX9#

PEX_TX10#

PEX_TX10#

PEX_TX11#

PEX_TX11#

PEX_TX12#

PEX_TX12#

PEX_TX13#

PEX_TX13#

PEX_TX14#

PEX_TX14#

PEX_TX15#

PEX_TX15#

PEX_RX0#

PEX_RX0#

PEX_RX1#

PEX_RX1#

PEX_RX2#

PEX_RX2#

PEX_RX3#

PEX_RX3#

PEX_RX4#

PEX_RX4#

PEX_RX5#

PEX_RX5#

PEX_RX6#

PEX_RX6#

PEX_RX7#

PEX_RX7#

PEX_RX8#

PEX_RX8#

PEX_RX9#

PEX_RX9#

PEX_RX10#

PEX_RX10#

PEX_RX11#

PEX_RX11#

PEX_RX12#

PEX_RX12#

PEX_RX13#

PEX_RX13#

PEX_RX14#

PEX_RX14#

PEX_RX15#

PEX_RX15#

MIOAD0

MIOAD1

MIOAD2

MIOAD3

MIOAD4

MIOAD5

MIOAD6

MIOAD7

MIOAD8

MIOAD9

MIOAD10

MIOAD11

MIOBD0

MIOBD1

MIOBD2

MIOBD3

MIOBD4

MIOBD5

MIOBD6

MIOBD7

MIOBD8

MIOBD9

MIOBD10

MIOBD11

MIOA_HSYNC

MIOA_VSYNC

MIOA_DE

MIOA_CTL3

MIOA_CLKOUT

MIOA_CLKOUT#

MIOA_CLKIN

MIOA_VREF

MIOACAL_PU_GND

MIOACAL_PD_VDDQ

MIOB_HSYNC

MIOB_VSYNC

MIOB_DE

MIOB_CTL3

MIOB_CLKOUT

MIOB_CLKOUT#

MIOB_CLKIN

MIOB_VREF

MIOBCAL_PU_GND

MIOBCAL_PD_VDDQ

TP691 26MIL

TP693 26MIL

TP692 26MIL

TP694 26MIL

TP672 26MIL

TP682 26MIL

TP678 26MIL

TP673 26MIL

TP675 26MIL

TP676 26MIL

TP677 26MIL

TP679 26MIL

TP695 26MIL

TP680 26MIL

TP681 26MIL

TP705 26MIL

TP706 26MIL

TP688 26MIL

TP689 26MIL

TP690 26MIL

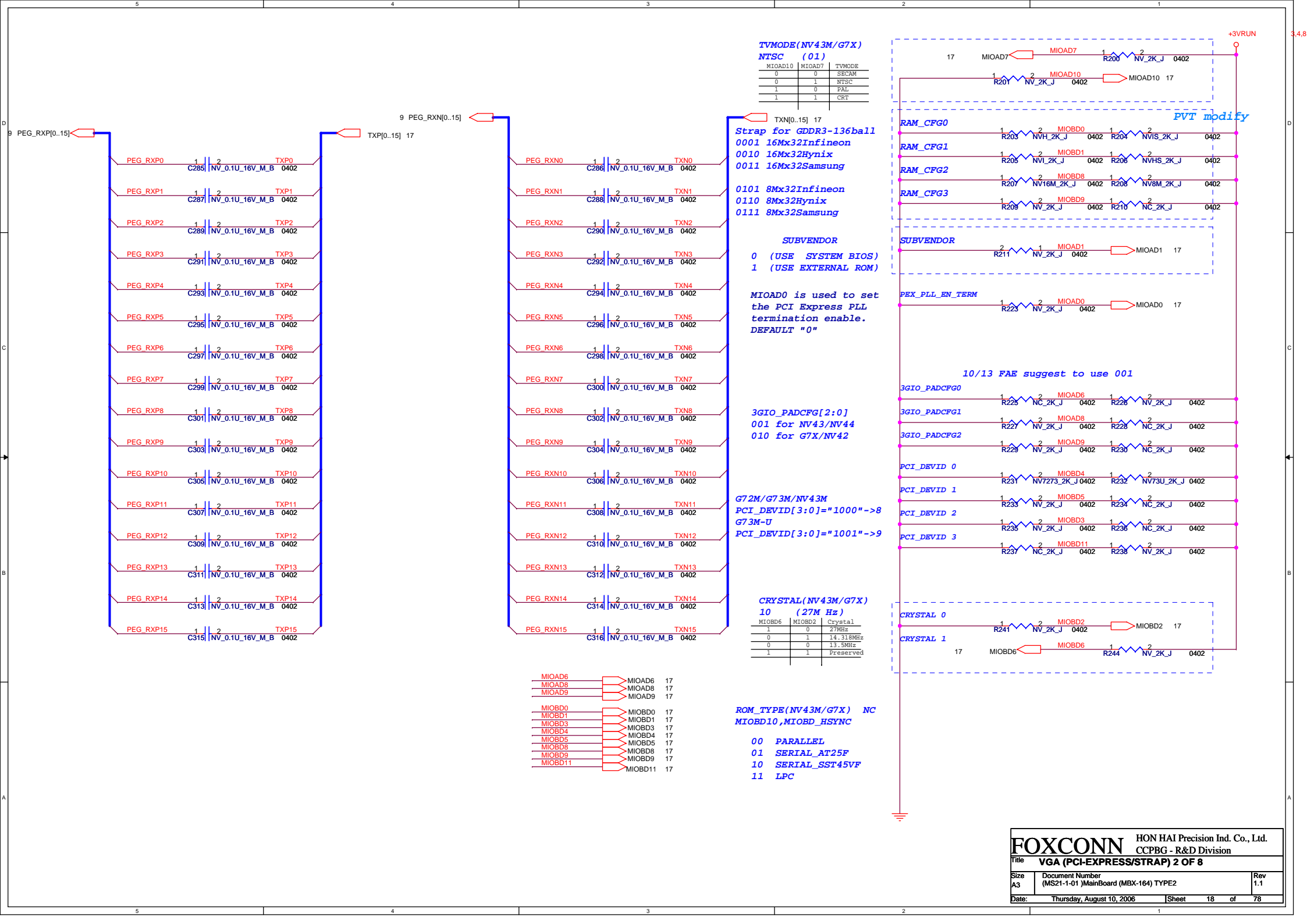
TP699 26MIL

TP684 26MIL

TP685 26MIL

TP684 26MIL

NV_GF-GO6600-N-AX (G73M)



**TVMODE(NV43M/G7X)
NTSC (01)**

MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

Strap for GDDR3-136ball
 0001 16Mx32Infineon
 0010 16Mx32Hynix
 0011 16Mx32Samsung

0101 8Mx32Infineon
 0110 8Mx32Hynix
 0111 8Mx32Samsung

SUBVENDOR

0 (USE SYSTEM BIOS)
 1 (USE EXTERNAL ROM)

MIOAD0 is used to set
 the PCI Express PLL
 termination enable.
 DEFAULT "0"

3GIO_PADCFG[2:0]
 001 for NV43/NV44
 010 for G7X/NV42

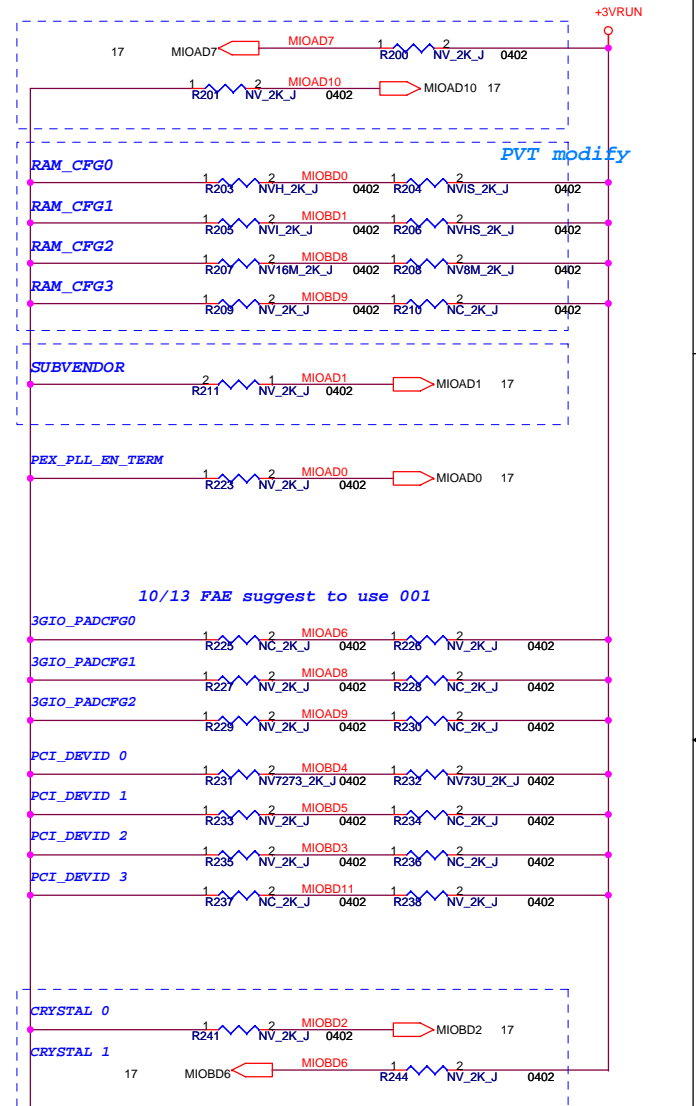
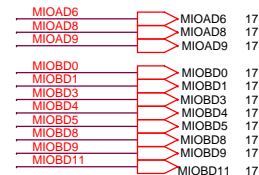
G72M/G73M/NV43M
 PCI_DEVID[3:0]="1000"-->8
 G73M-U
 PCI_DEVID[3:0]="1001"-->9

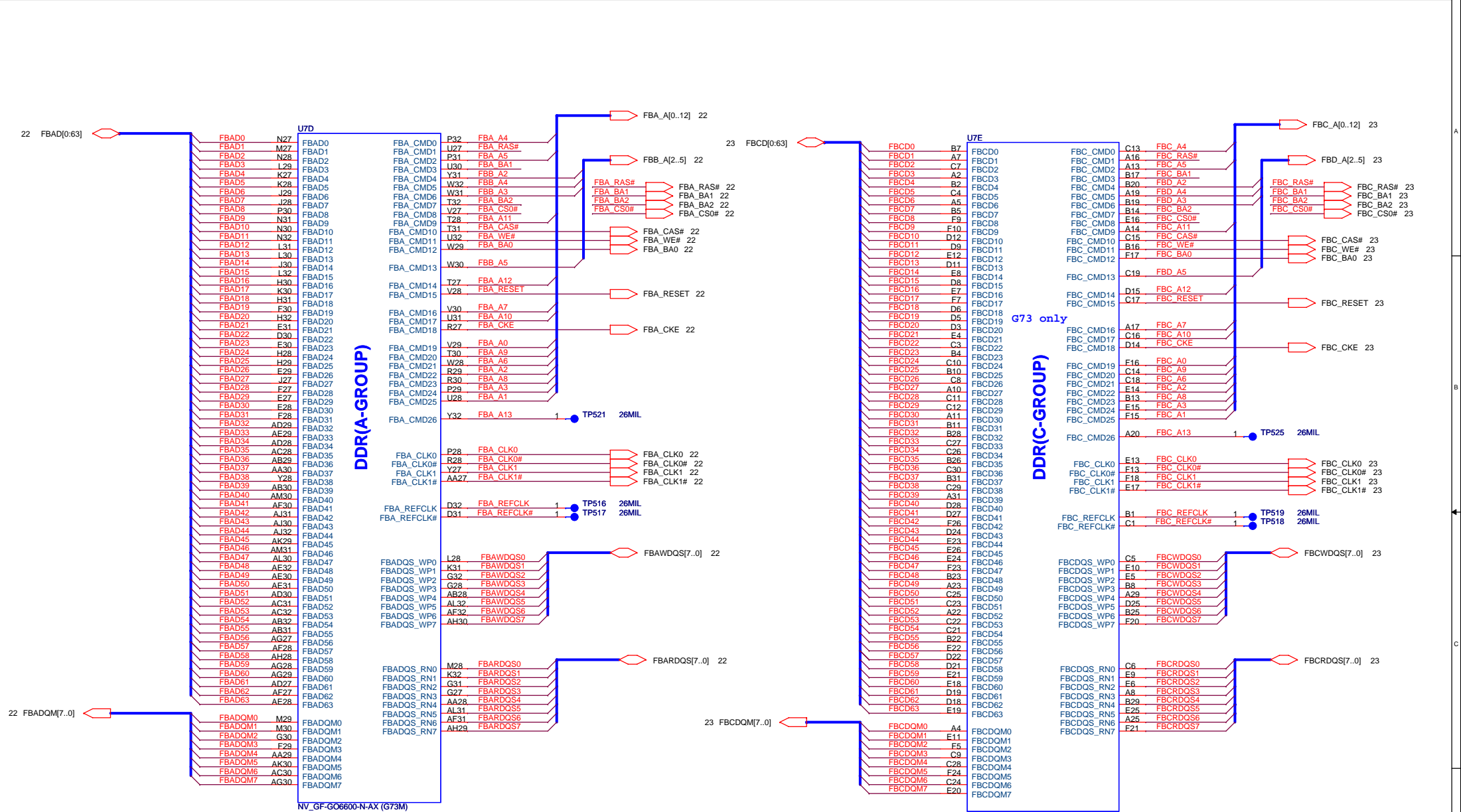
**CRYSTAL(NV43M/G7X)
10 (27M Hz)**

MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

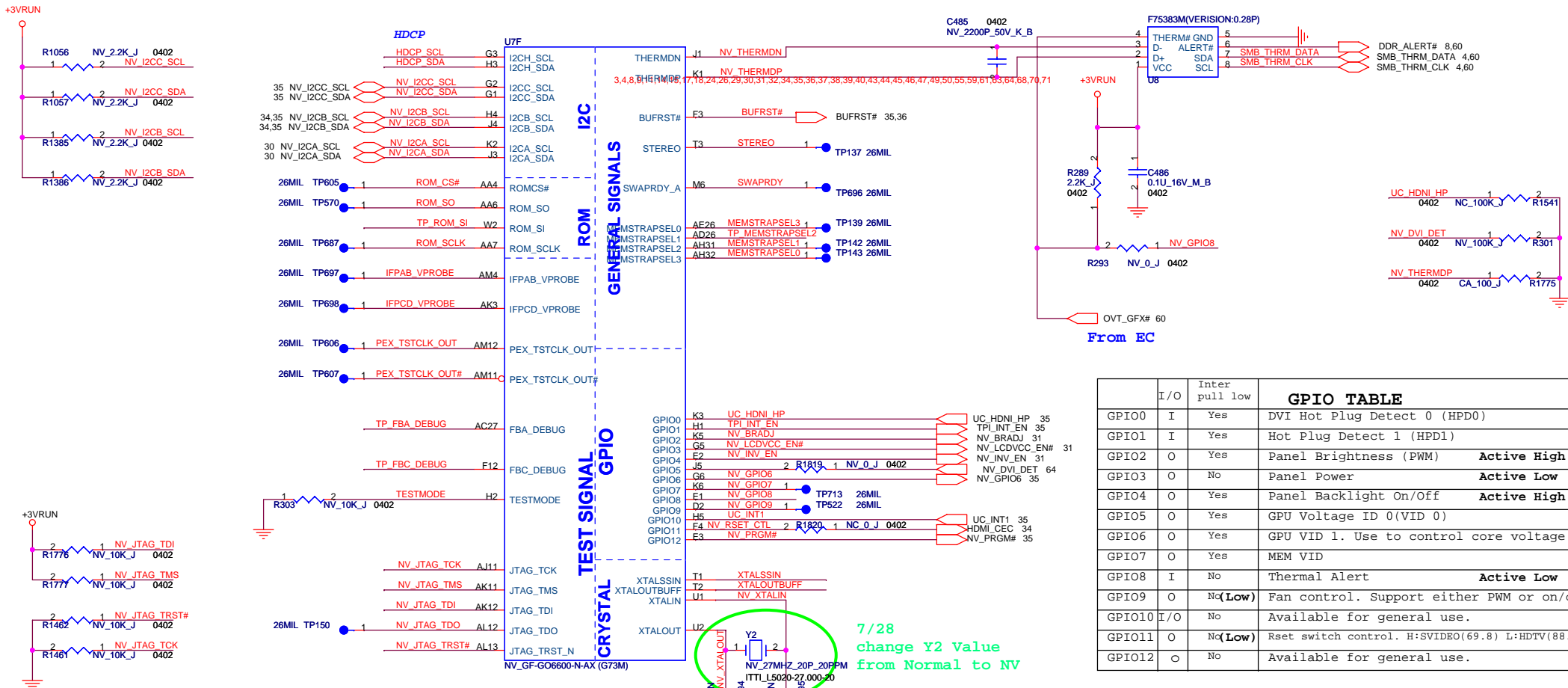
ROM_TYPE(NV43M/G7X) NC
 MIOBD10, MIOBD_HSYNC

00 PARALLEL
 01 SERIAL_AT25F
 10 SERIAL_SST45VF
 11 LPC





SM bus Address :
1001100(BC)
For F75383M



	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) Active High
GPIO3	O	No	Panel Power Active Low
GPIO4	O	Yes	Panel Backlight On/Off Active High
GPIO5	O	Yes	GPU Voltage ID 0(VID 0)
GPIO6	O	Yes	GPU VID 1. Use to control core voltage
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert Active Low
GPIO9	O	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	O	No(Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

7/28
change Y2 Value
from Normal to NV

SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

SPREAD SPECTRUM SETTING FOR P1819B

SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

0 = connect to GND
M = unconnected
1 = connect directly to VDD

nVidia support Down -1.25%

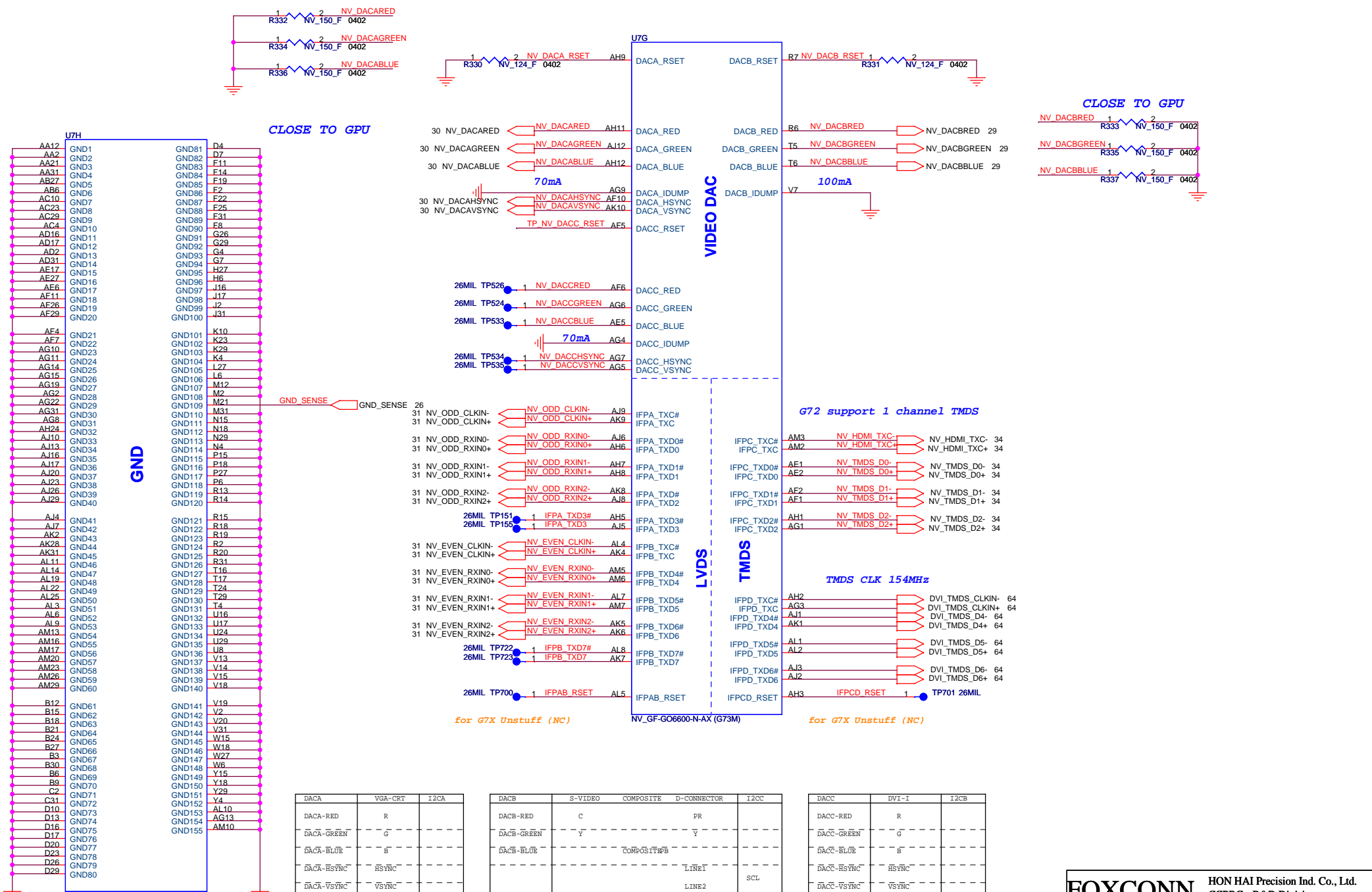
This chip can use MK1726 or P1819B

R316 place near GPU
R317 place near spectrum chip

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CCPBG - R&D Division

Title: **VGA (POWER) 7 OF 8**

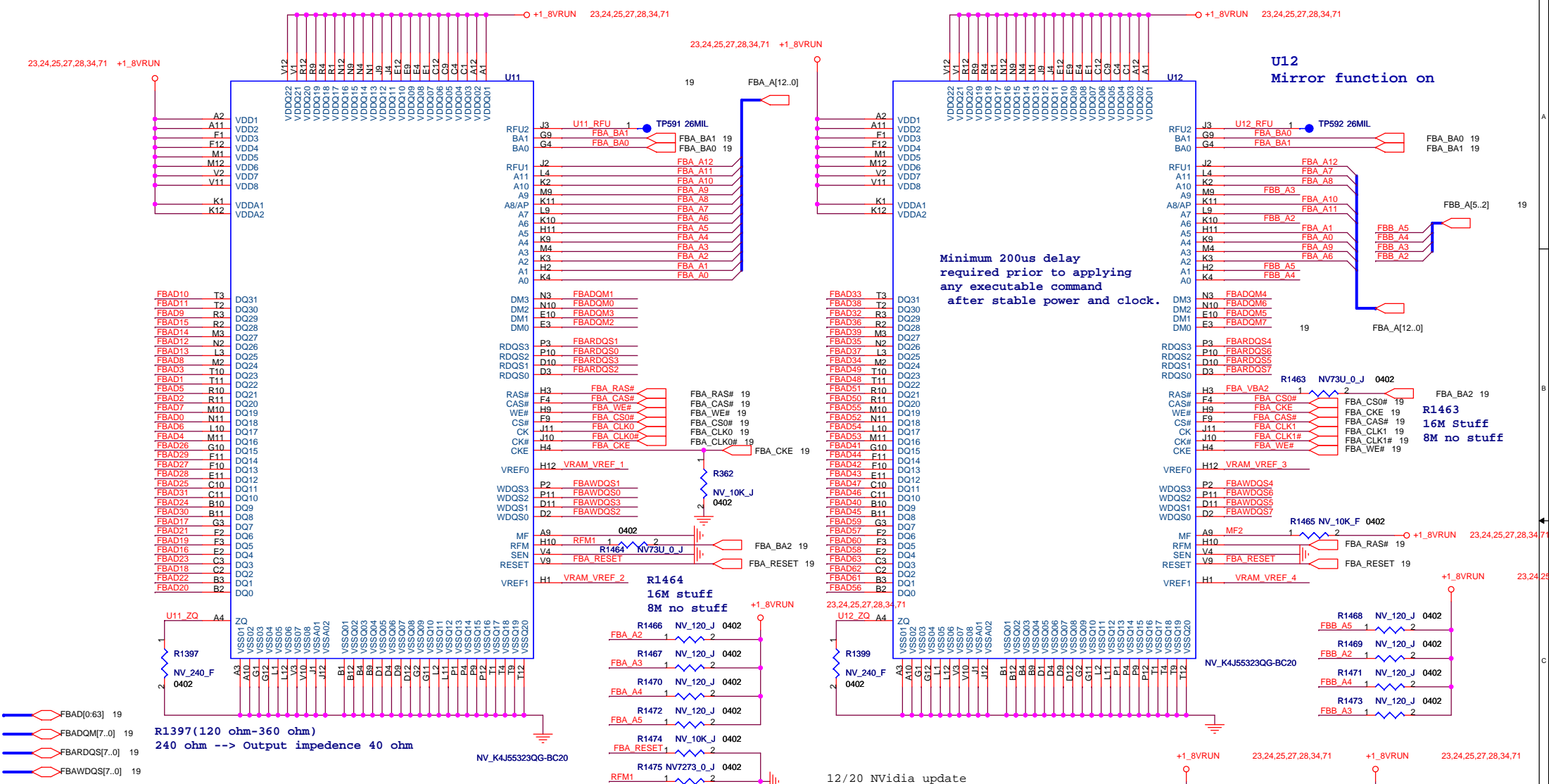
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 20 of 78	



DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA

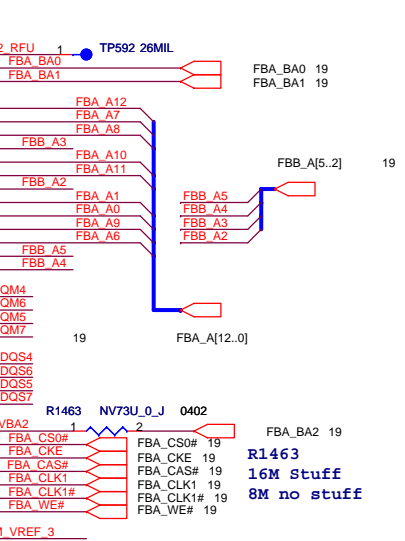
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CB
DACB-RED	C		FR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	

DACC	DVI-I	I2CB
DACC-RED	R	
DACC-GREEN	G	
DACC-BLUE	B	
DACC-HSYNC	HSYNC	
DACC-VSYNC	VSYNC	
	DVI-DDCCLK	SCL
	DVI-DDCDATA	SDA



Minimum 200us delay required prior to applying any executable command after stable power and clock.

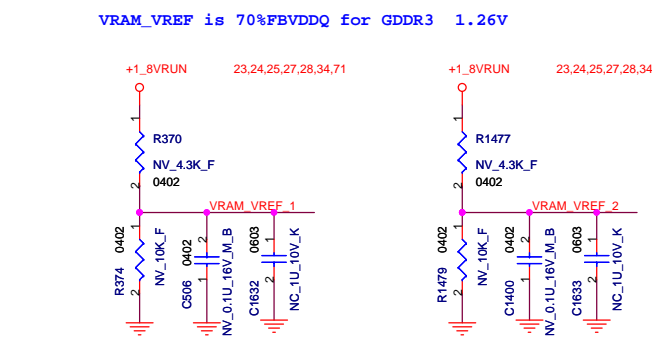
U12 Mirror function on



R1463 16M Stuff 8M no stuff

FBAD[0:63] 19
 FBADQM[7..0] 19
 FBARDQS[7..0] 19
 FBAWDQS[7..0] 19

R1397(120 ohm-360 ohm)
 240 ohm --> Output impedance 40 ohm



R1464 16M stuff 8M no stuff

R1465 NV_120_J 0402

R1466 NV_120_J 0402

R1467 NV_120_J 0402

R1470 NV_120_J 0402

R1472 NV_120_J 0402

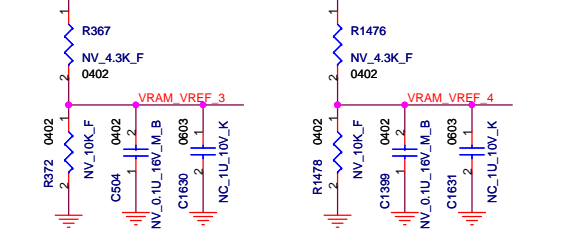
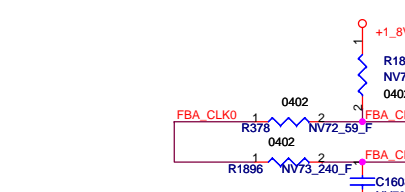
R1474 NV_10K_J 0402

R1475 NV723_0_J 0402

RFM1

12/20 Nvidia update

	DDR3(G72M)	DDR3(G73M)(G73M-U)
R378,R380	60 ohm	240 ohm
R,C 1890	0 ohm	0.01uF



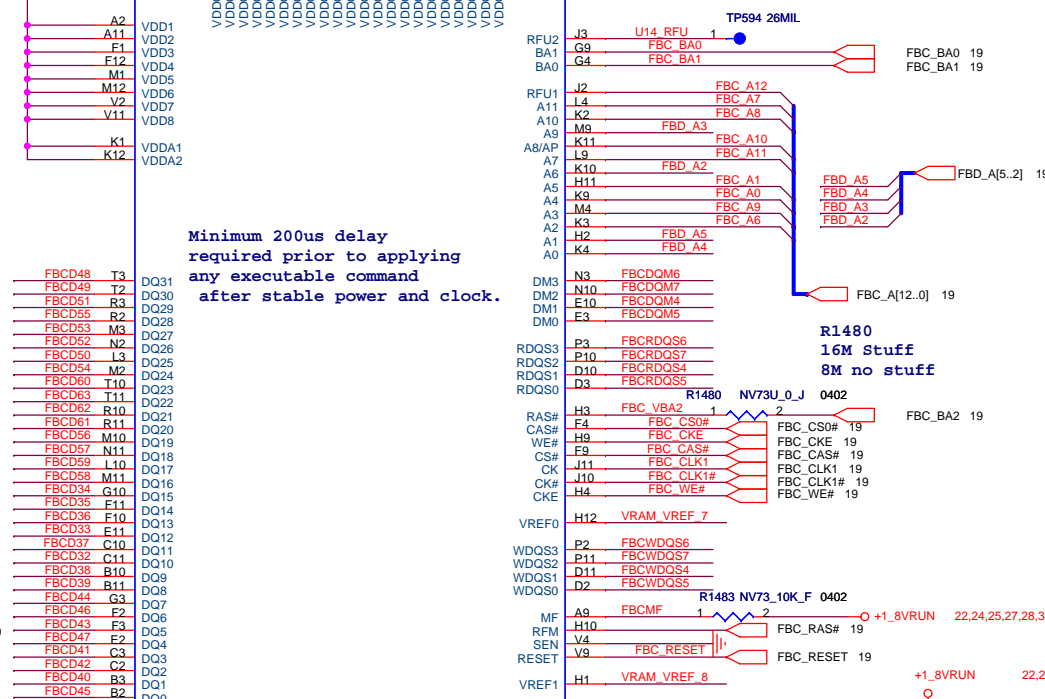
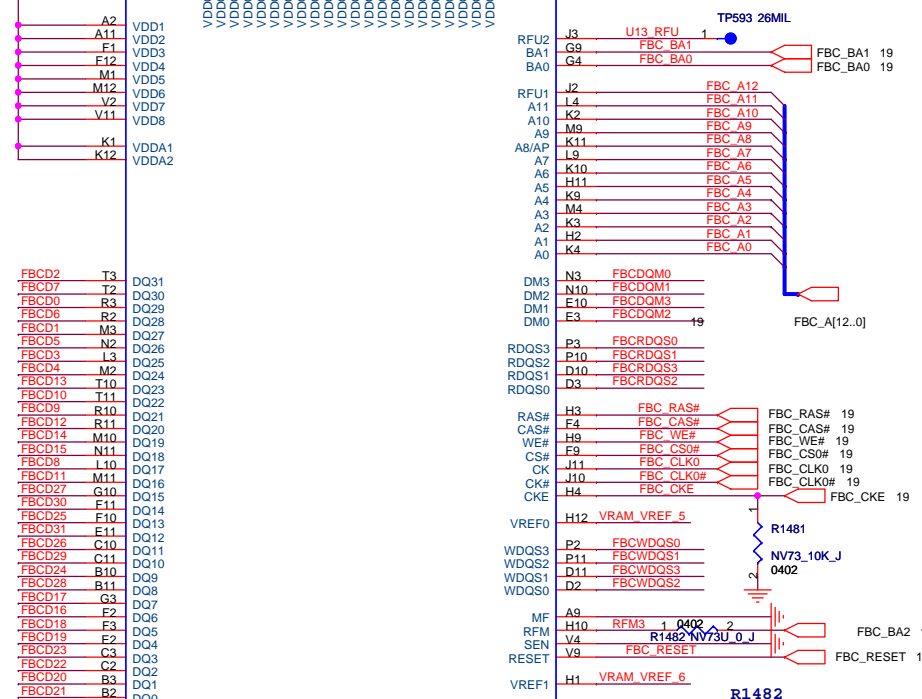
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22.24.25.27.28.34.71 +1_8VRUN

22.24.25.27.28.34.71 +1_8VRUN

+1_8VRUN 22.24.25.27.28.34.71

U14
Mirror function on



Minimum 200us delay
required prior to applying
any executable command
after stable power and clock.

R1480
16M Stuff
8M no stuff

- FBCD[0:63] 19
- FBCDQM[7..0] 19
- FBCRDQS[7..0] 19
- FBCWDQS[7..0] 19

R1414(120 ohm-360 ohm)
240 ohm --> Output impedance 40 ohm

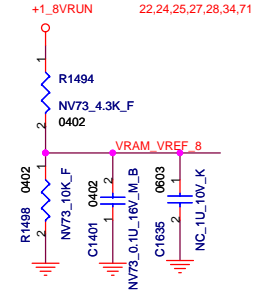
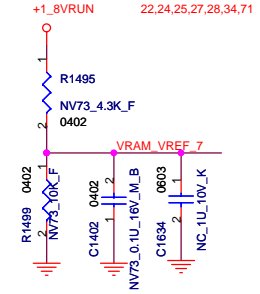
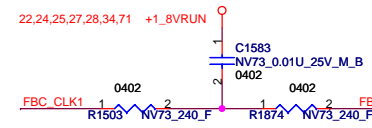
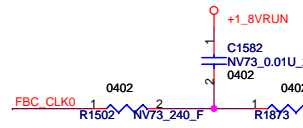
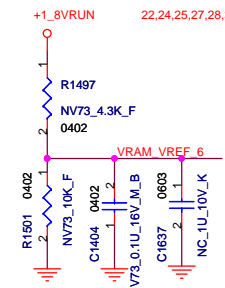
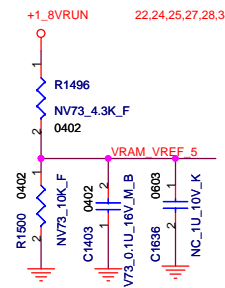
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

R1493
8M Stuff
16M no stuff

040506
R1493 change part name (G73Only_ ->NV73Only_)
to meet BOM configuration
*PVT already modify(special noties V0.6)

11/3 nVidia update

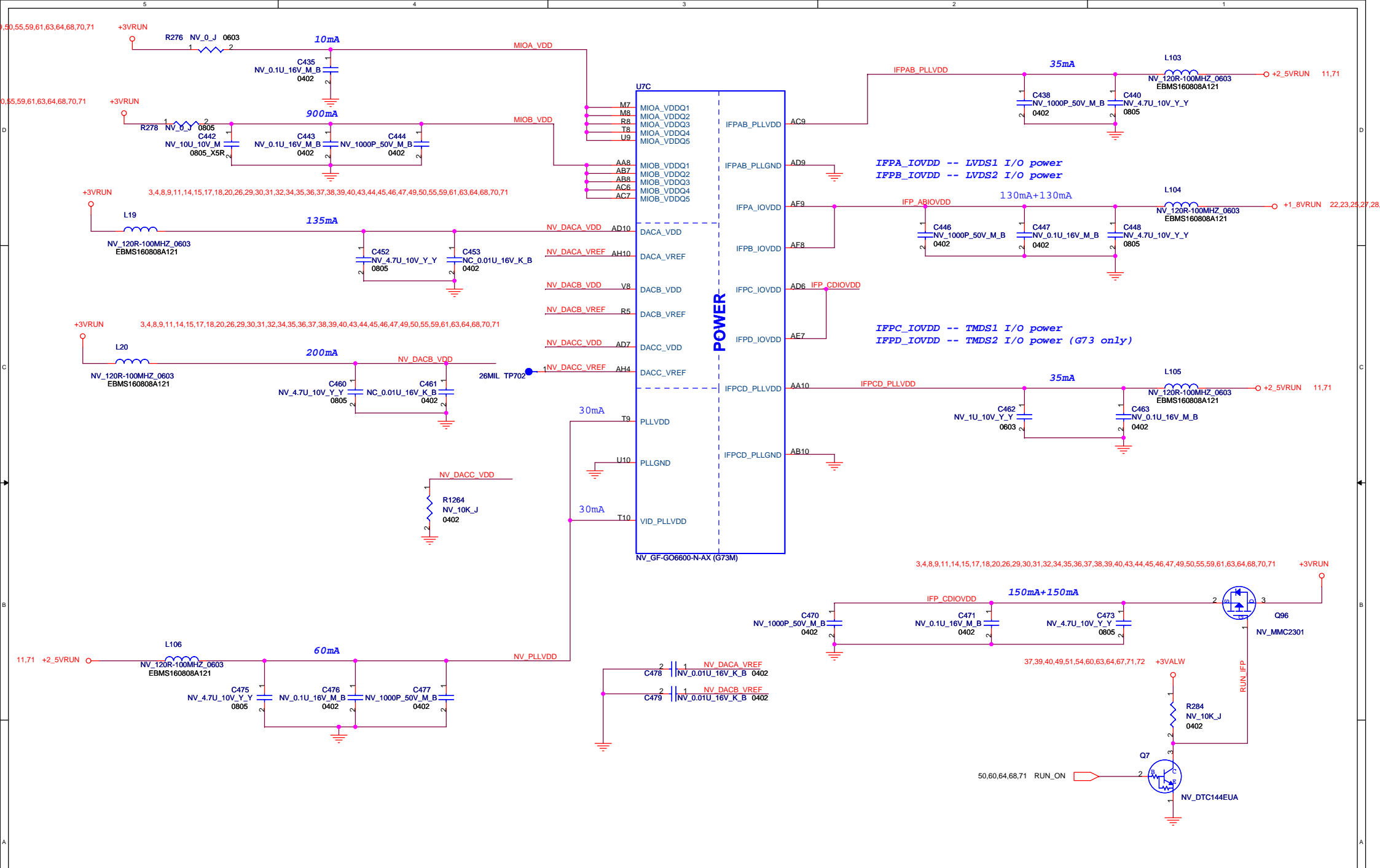
	DDR3 (G72M)	DDR3 (G73M) (G73M-U)
R1502,R1873	40 ohm	240 ohm
R1503,R1874		
C1582,C1583	0 ohm	0.01uF



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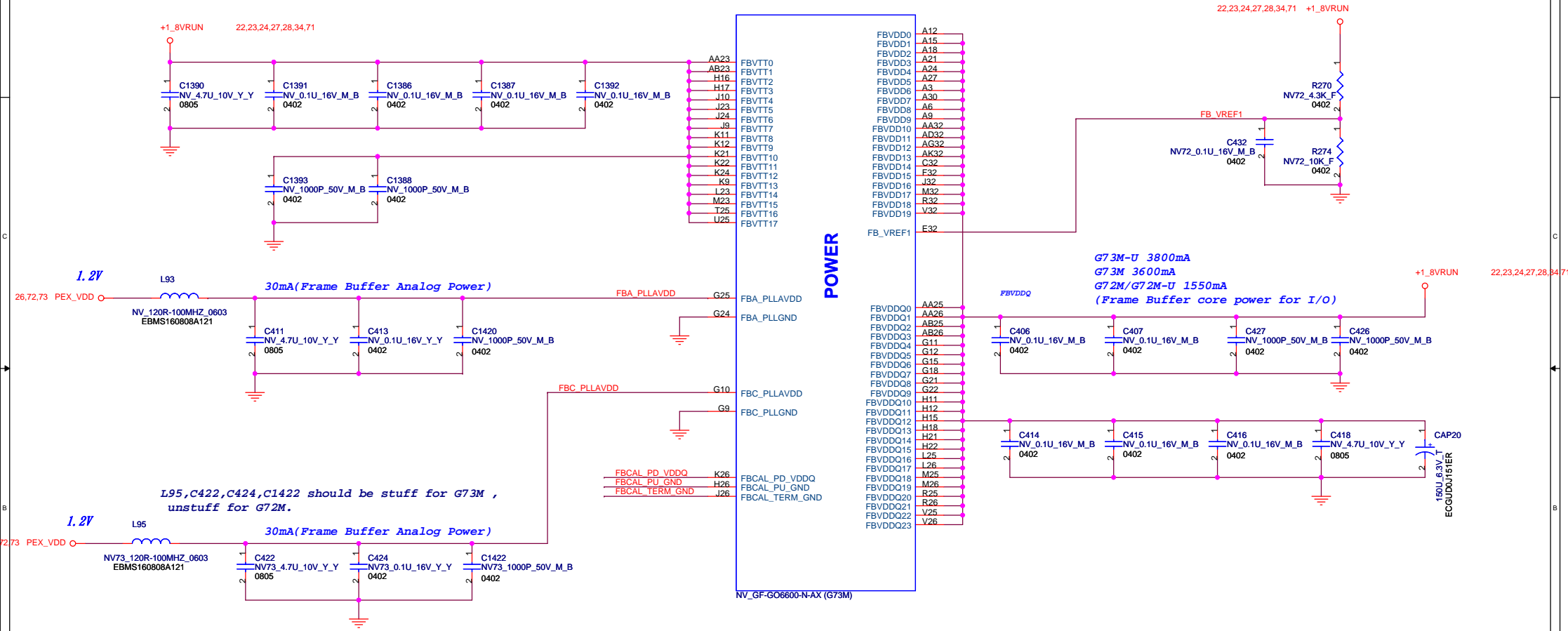
Title: **VRAM (GDDR) 1 OF 4**

Size A3	Document Number (MS21-1-01)MainBoard (MBX-164) TYPE2	Rev 1.1
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For GDDR3 FBVTT require decoupling capacitor,FBVDD don't require them.

U71

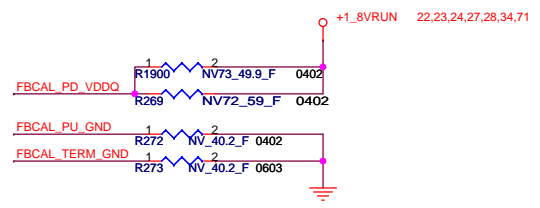


POWER

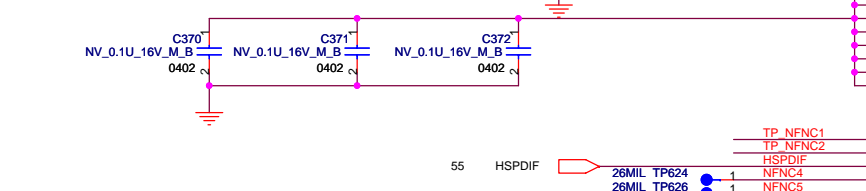
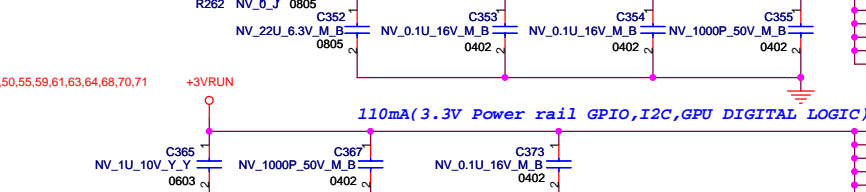
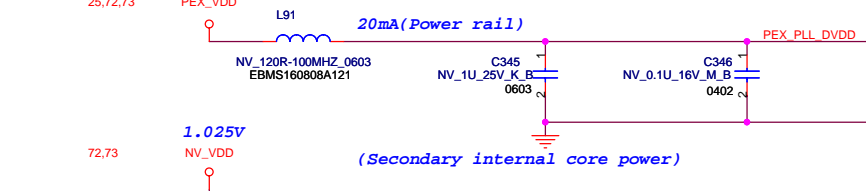
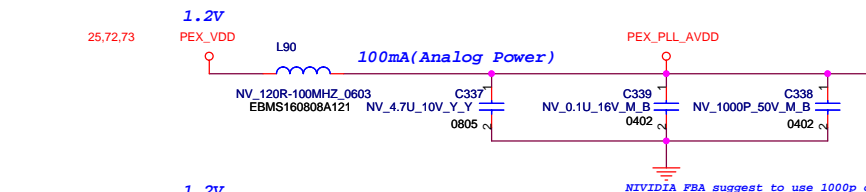
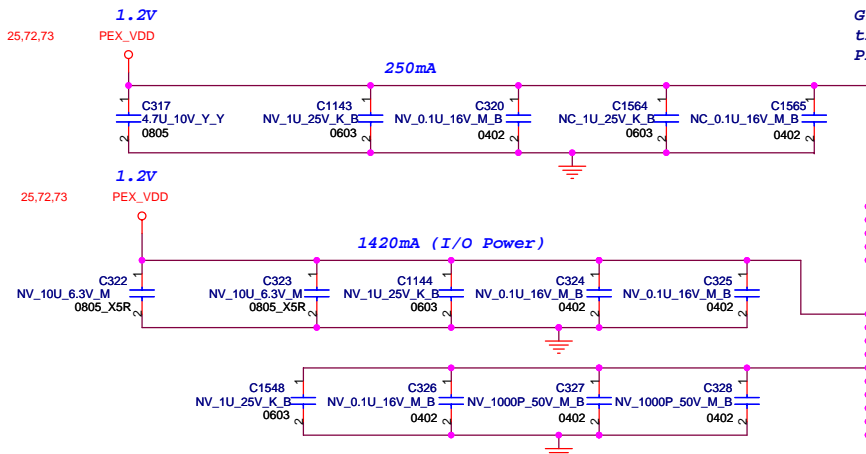
G73M-U 3800mA
 G73M 3600mA
 G72M/G72M-U 1550mA
 (Frame Buffer core power for I/O)

11/3 nVidia update

	DDR1	DDR3(G72M)	DDR3(G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm



G3 design guide require that PEX_IOVDD/Q directly connect to PEX_VDD on page 16.



- U7B
- AD23 PEX_IOVDD0
 - AF24 PEX_IOVDD1
 - AE23 PEX_IOVDD2
 - AF25 PEX_IOVDD3
 - AG24 PEX_IOVDD4
 - AG25 PEX_IOVDD5
 - AC16 PEX_IOVDDQ0
 - AC17 PEX_IOVDDQ1
 - AC21 PEX_IOVDDQ2
 - AC22 PEX_IOVDDQ3
 - AE18 PEX_IOVDDQ4
 - AE21 PEX_IOVDDQ5
 - AE22 PEX_IOVDDQ6
 - AE12 PEX_IOVDDQ7
 - AF18 PEX_IOVDDQ8
 - AF21 PEX_IOVDDQ9
 - AF22 PEX_IOVDDQ10

- AE15 PEX_PLLAVDD
- AE15 PEX_PLLDVDD
- AE16 PEX_PLLGND

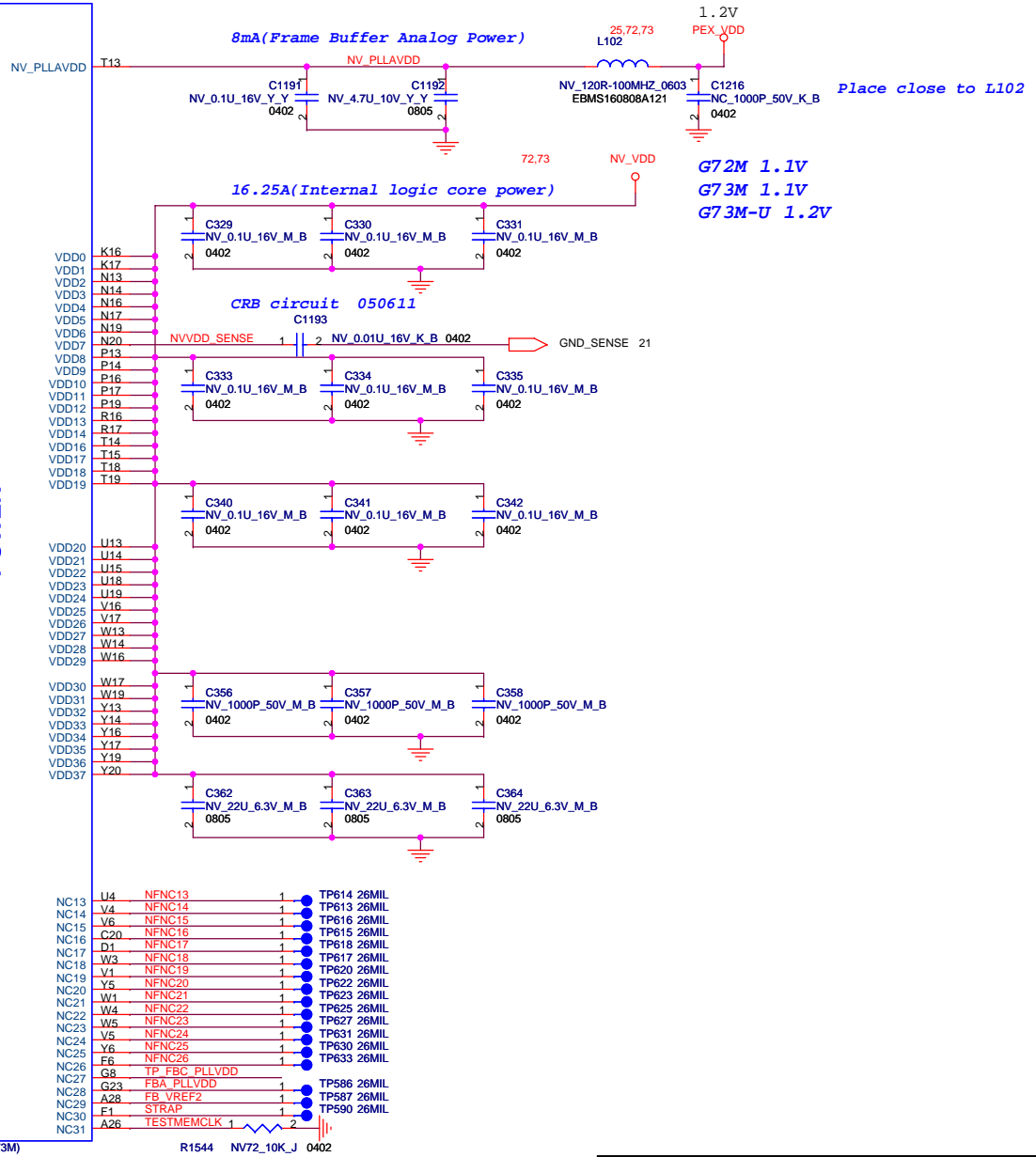
- VDD_LP1
- VDD_LP2
- VDD_LP3
- VDD_LP4
- VDD_LP5
- VDD_LP6

- VDD33_0
- VDD33_1
- VDD33_2
- VDD33_3
- VDD33_4
- VDD33_5
- VDD33_6
- VDD33_7
- VDD33_8
- VDD33_9
- VDD33_10
- VDD33_11
- VDD33_12

- NC1
- NC2
- NC3
- NC4
- NC5
- NC6
- NC7
- NC8
- NC9
- NC10
- NC11
- NC12

NV_GF-G06600-N-AX (G73M)

POWER



1.2V PEX_VDD

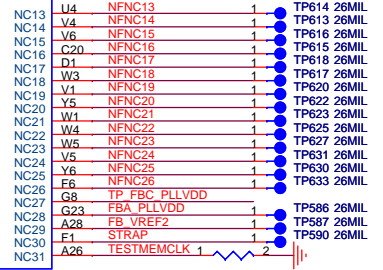
Place close to L102

25.72,73

72.73

NV_VDD

G72M 1.1V
G73M 1.1V
G73M-U 1.2V



R1544 NV72_10K_J 0402

G73M Pin A26-NC
G72M Pin A26 need stuff R305 10K

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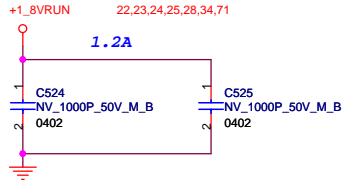
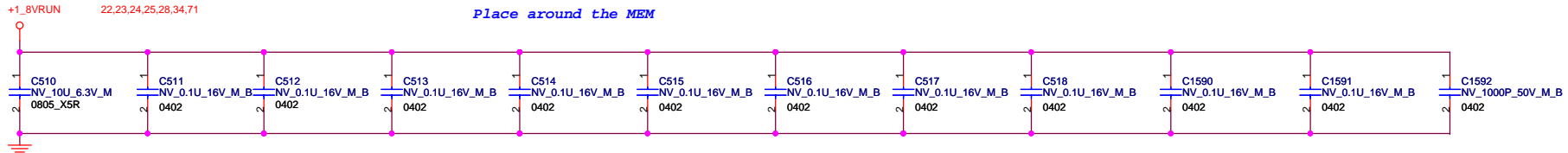
Title **VGA (GDDR/12C/ROM) 4 OF 8**

Size Document Number Rev 1.1
A3 (MS21-1-01)MainBoard (MBX-164) TYPE2

Date: Thursday, August 10, 2006 Sheet 26 of 78

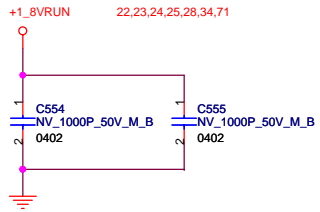
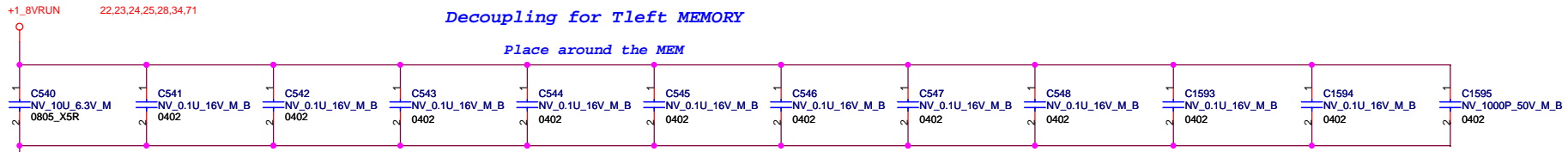
Decoupling for Tright MEMORY

Place around the MEM



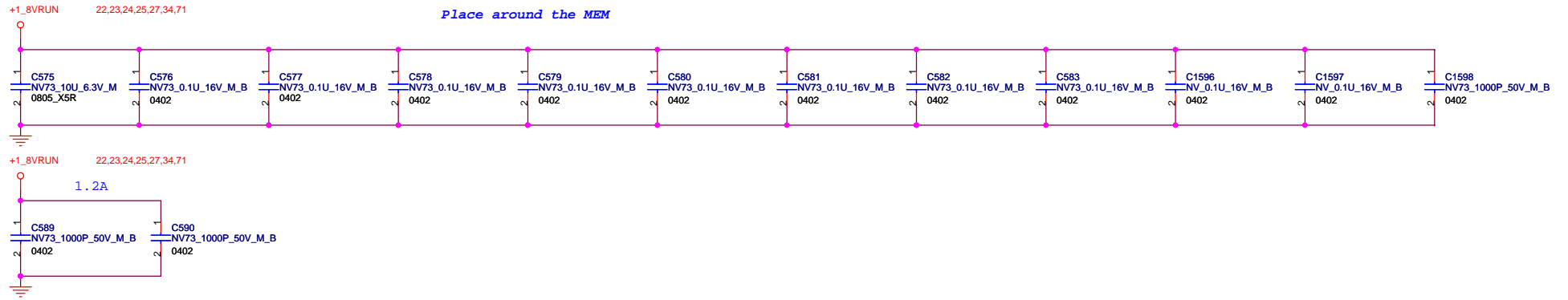
Decoupling for Tleft MEMORY

Place around the MEM



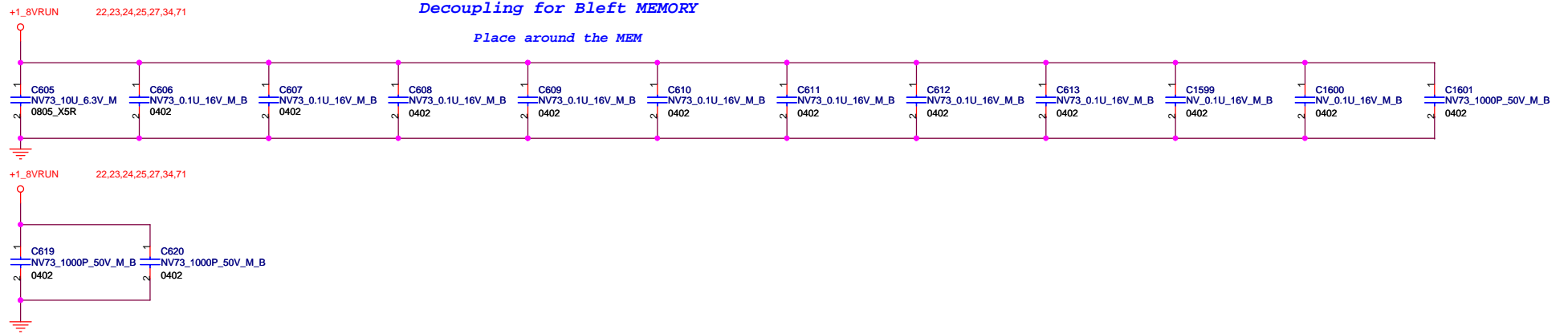
Decoupling for Bright MEMORY

Place around the MEM



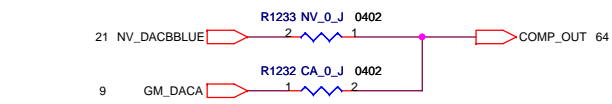
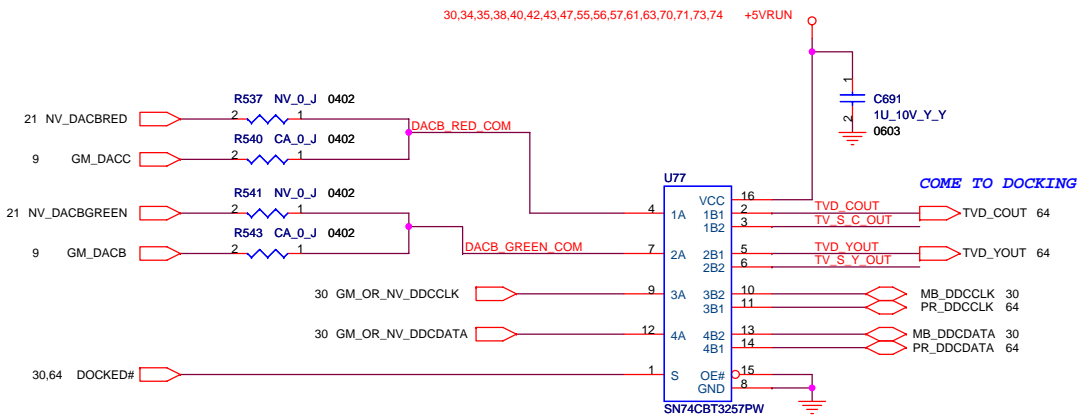
Decoupling for Bleft MEMORY

Place around the MEM

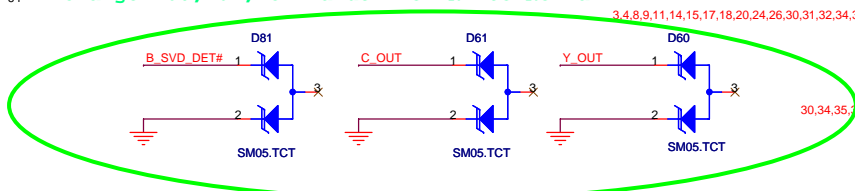


S-VIDEO ANALOG SWITCH

H : S-VIDEO&CVBS
L : PORT REPLICATOR

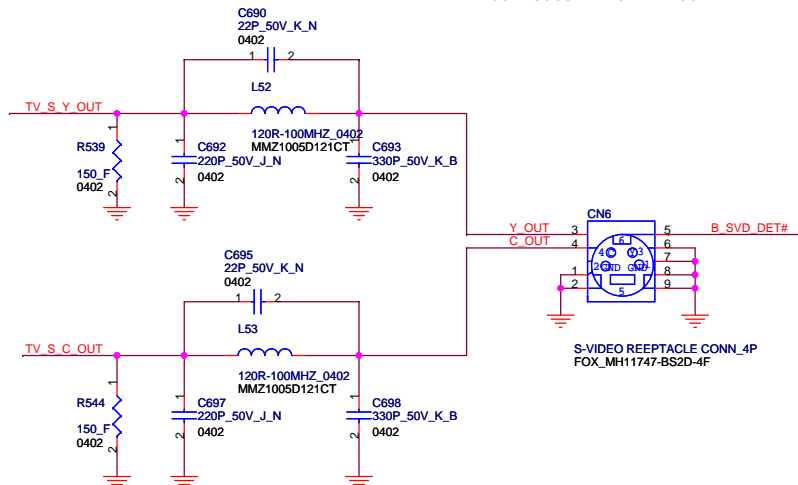


2006/8/7
change D60,D61,D81 Value from NV to Normal



S-VIDEO

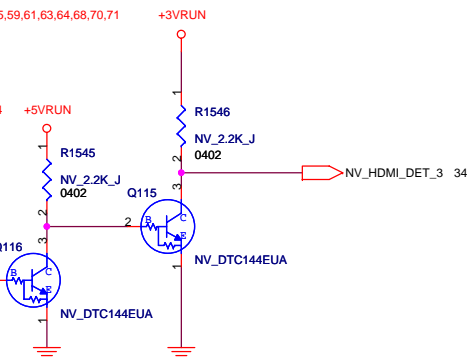
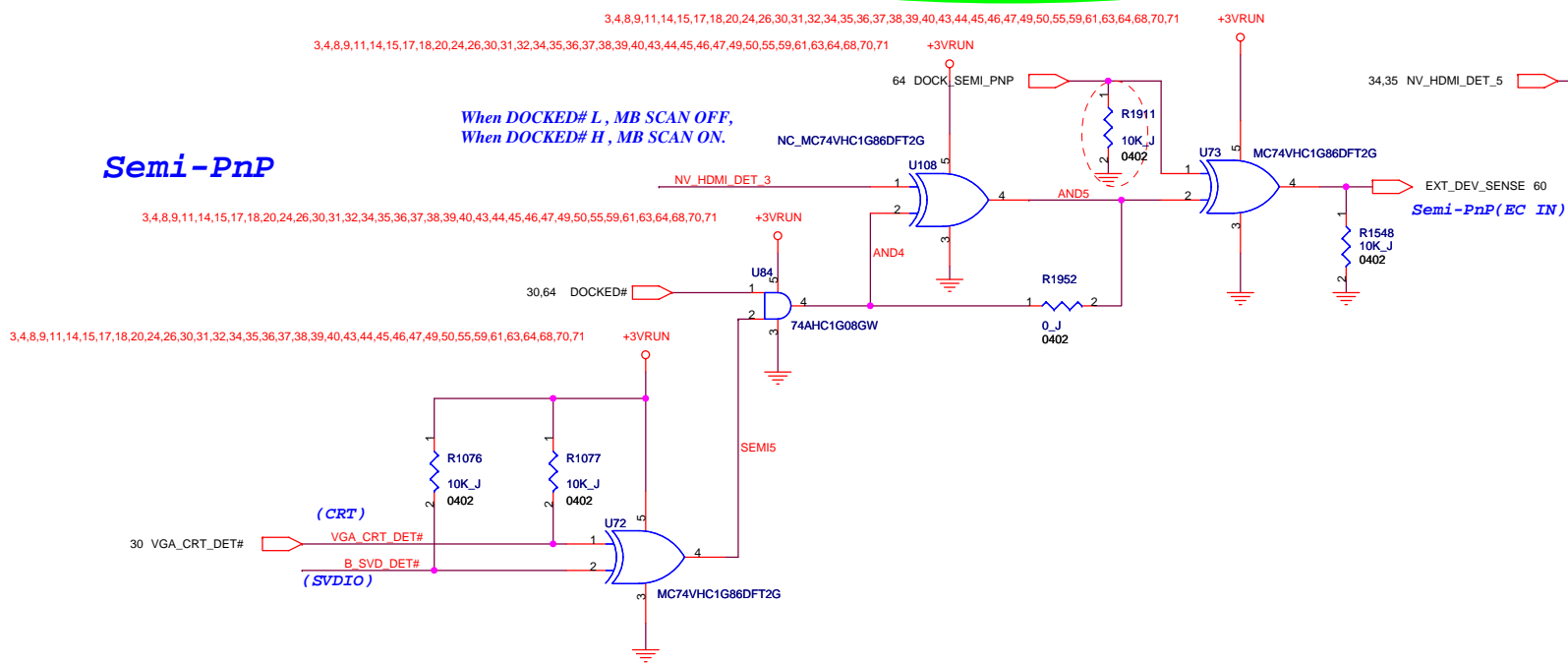
These component close to S-Video connector within 700 mil



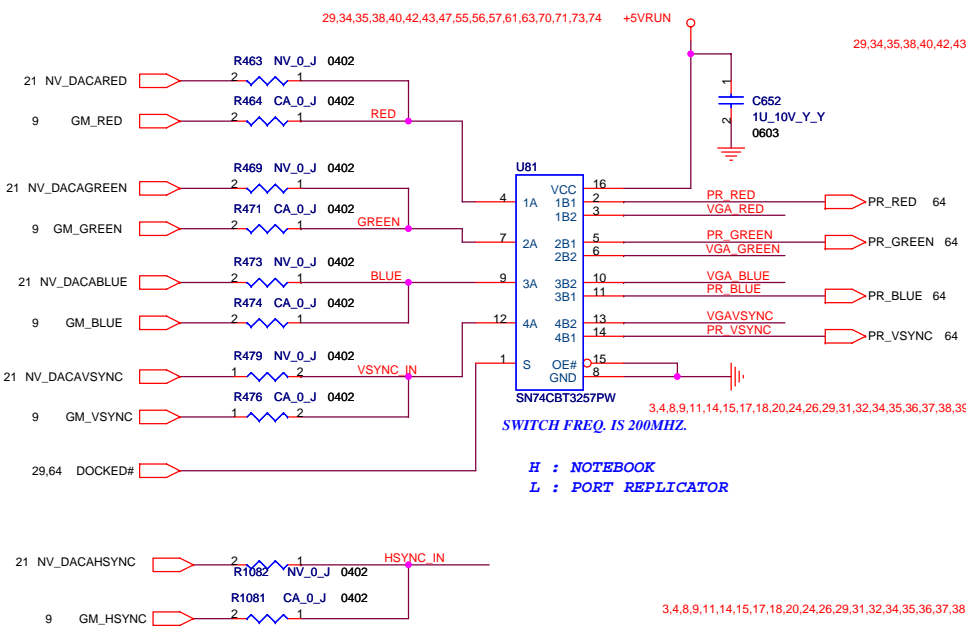
3,4,8,9,11,14,15,17,18,20,24,26,30,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71
3,4,8,9,11,14,15,17,18,20,24,26,30,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71

Semi-PnP

When DOCKED# L, MB SCAN OFF,
When DOCKED# H, MB SCAN ON.



CRT ANALOG SWITCH

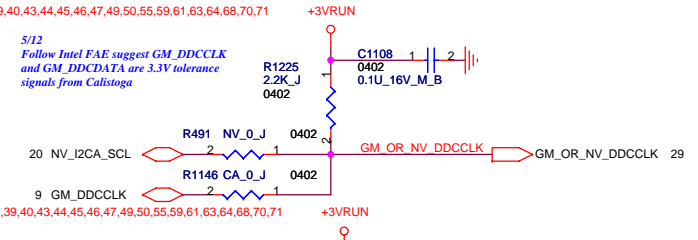


H : NOTEBOOK
L : PORT REPLICATOR

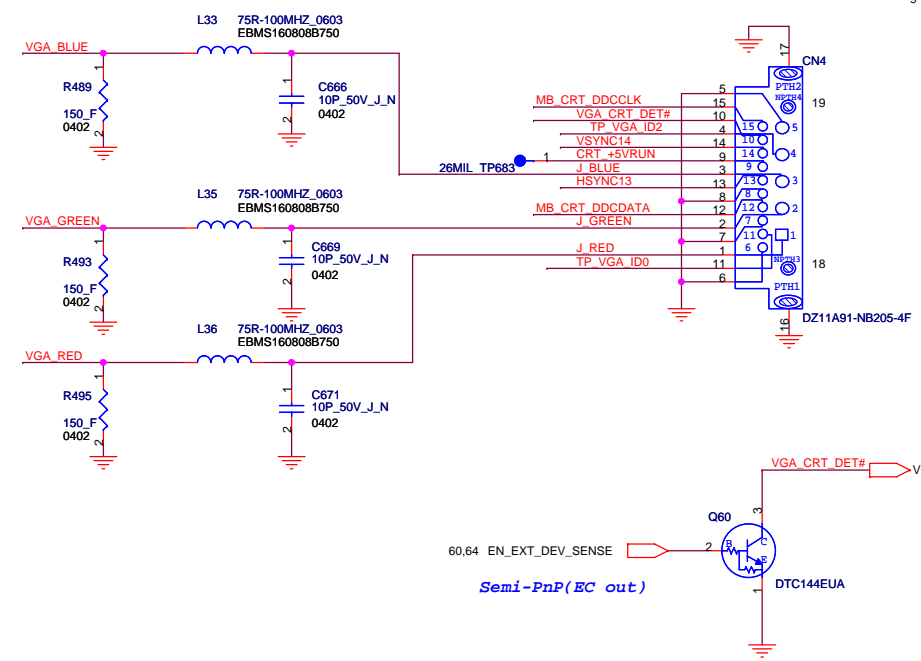
SWITCH FREQ. IS 200MHZ.

3,4,8,9,11,14,15,17,18,20,24,26,29,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71

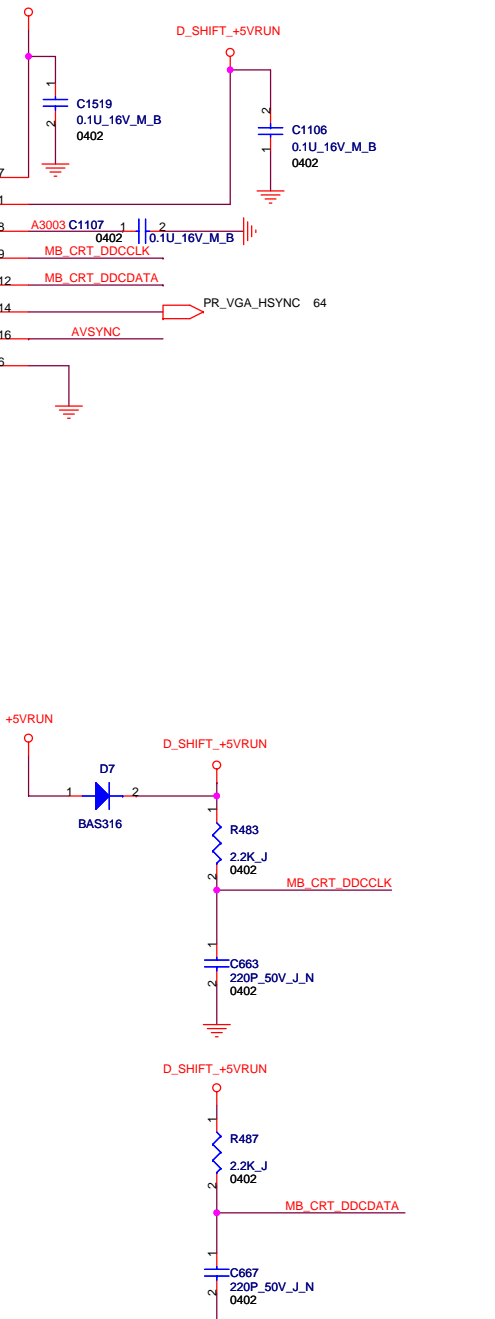
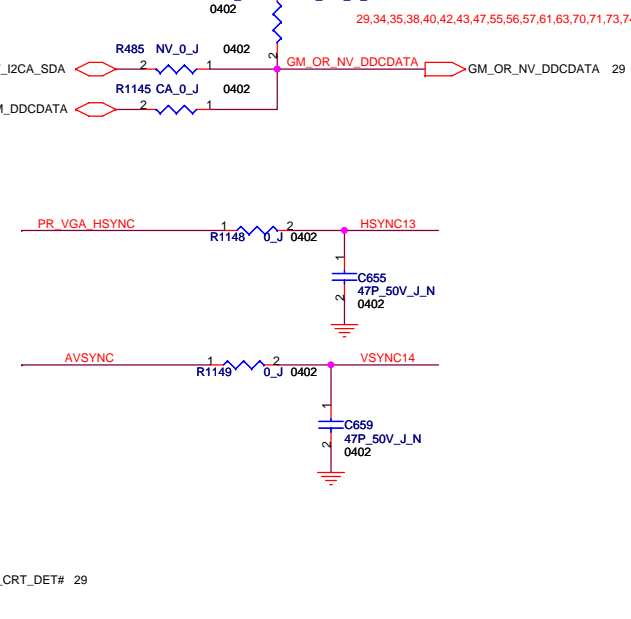
5/12
Follow Intel FAE suggest GM_DDCCLK and GM_DDCDATA are 3.3V tolerance signals from Callstoga



CRT CONNECTOR



Semi-PnP(EC out)

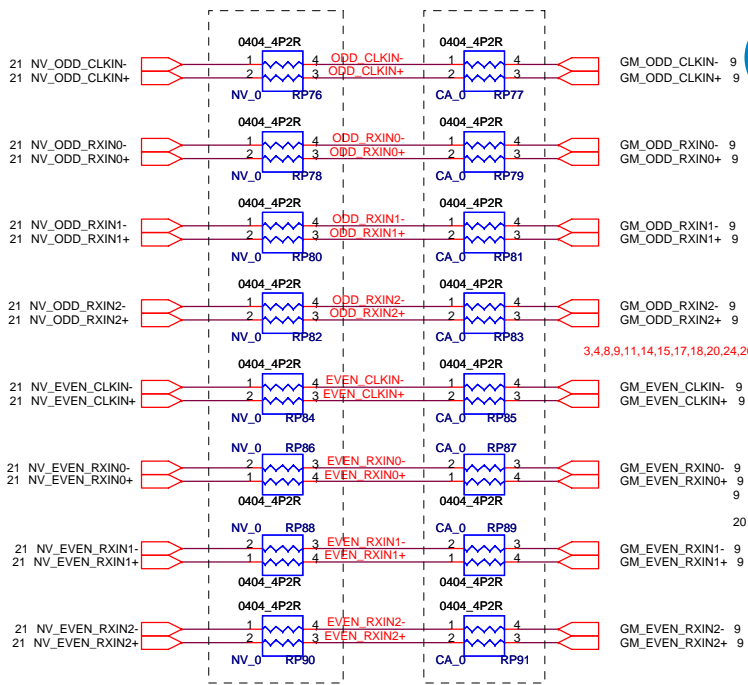


FOXCONN HON HAI Precision Ind. Co., Ltd.		CCPBG - R&D Division	
Title	CRT		
Size	Document Number	Rev	
A3	(MS21-1-01) MainBoard (MBX-164) TYPE2	1.1	
Date:	Thursday, August 10, 2006	Sheet	30 of 78

LVDS

Group1

Group2

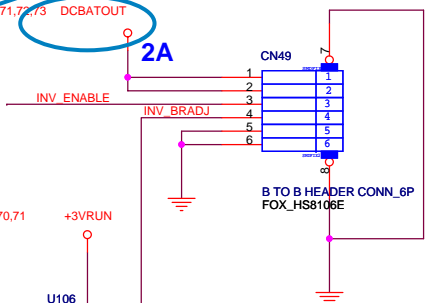
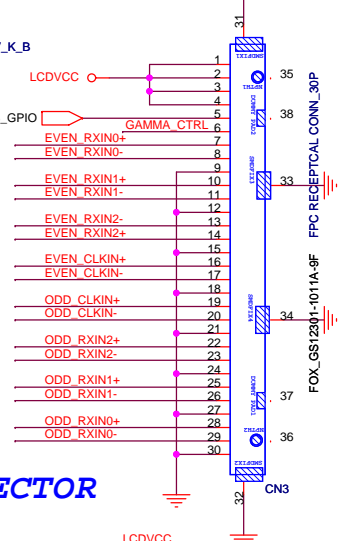


2006/6/26
 (Del inverter boost circuit, after change, the inverter circuit is the same with MS20 MP)
 Detail change list
 Delete PR426&PR427 and change C604-1, C1557-1, C1558-1, CN49pin1, pin2 net name INVERTER_VCC to net DCBATOUT.

Place C640 and C1558 close to CN49.

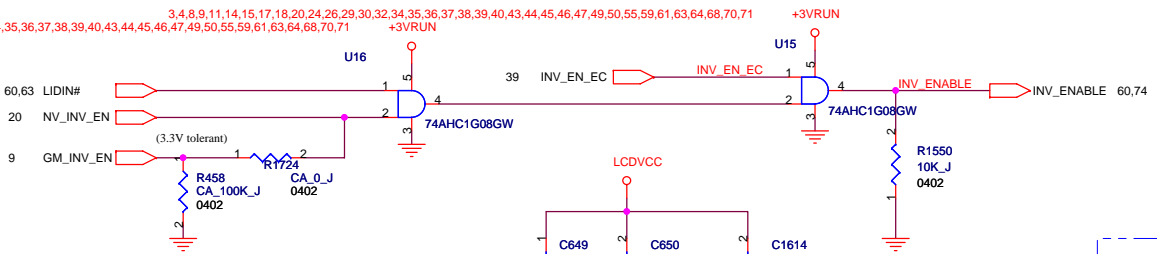
66,67,68,69,70,71,72,73 DCBATOUT

LVDS CONNECTOR



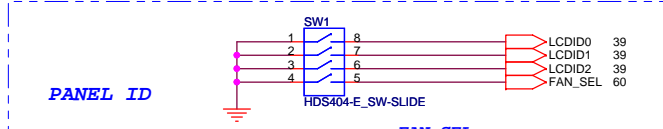
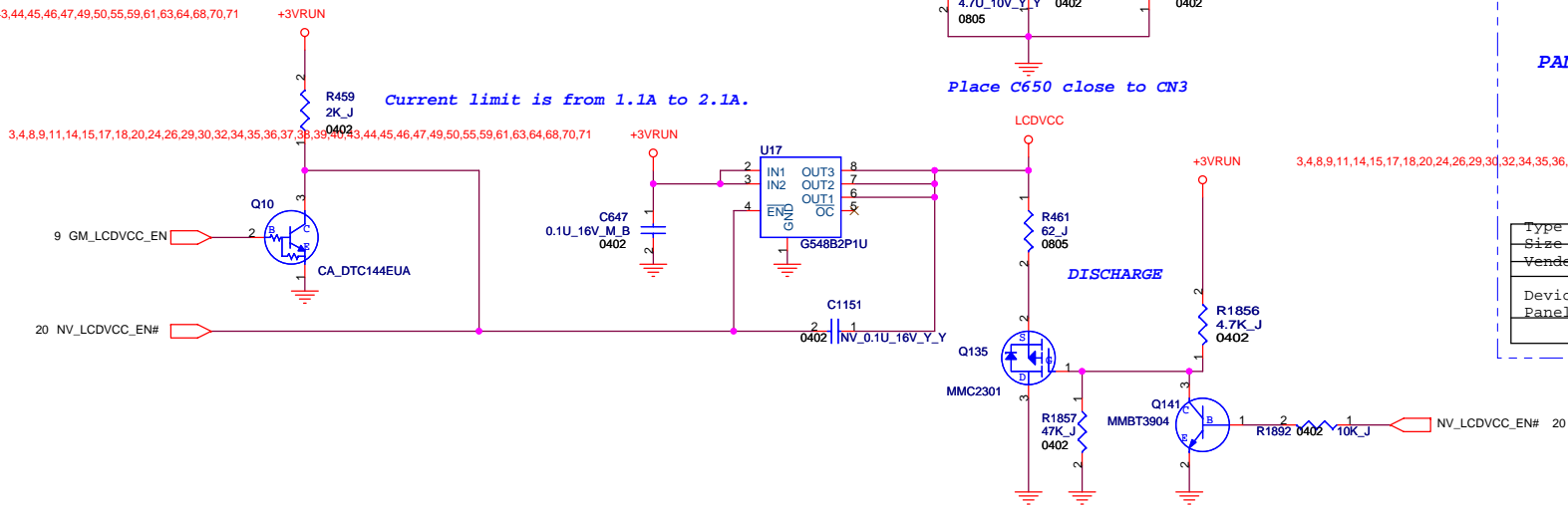
INVERTER CONNECTOR

U106, U15, U16 can use ON (MC74VHC1G08DF2G)
 H.H. PN: 14-MC74VHC-1G04



Place C650 close to CN3

Current limit is from 1.1A to 2.1A.



FAN_SEL:
 H: Foxconn FAN
 L: MOR cooling unit

Type	WXGA+	WXGA+	WUXGA
Size	17" wide	17" wide	17" wide
Vender	LG-PHILIPS	LG-PHILIPS	SHARE
Device Name	LP171WP7-1LA1	LP171WX2-A4K3	LQ170M1LA04
Panel ID Check[3..0]	0001	0010	0100

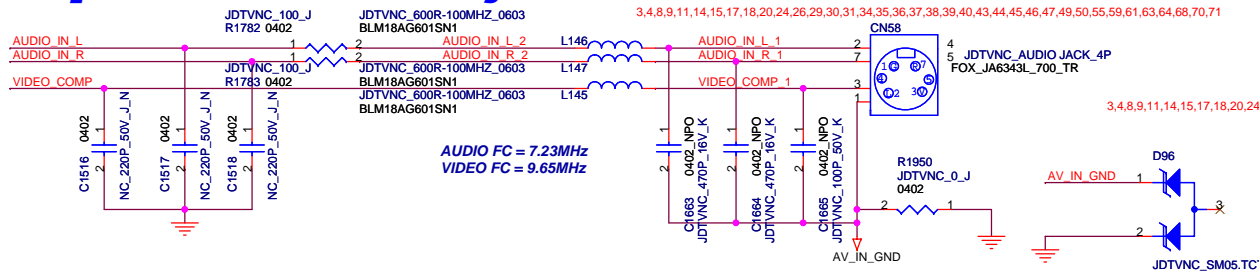
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **LVDS**

Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
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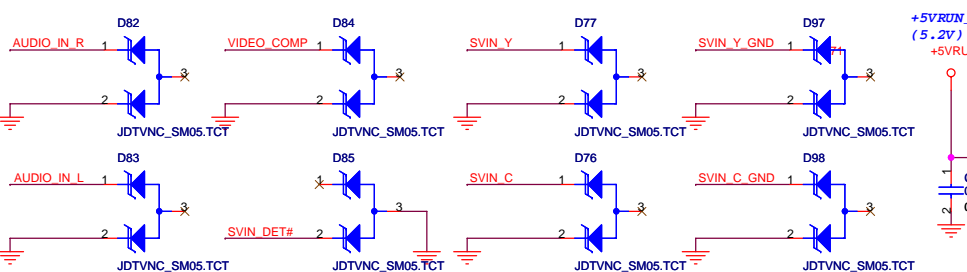
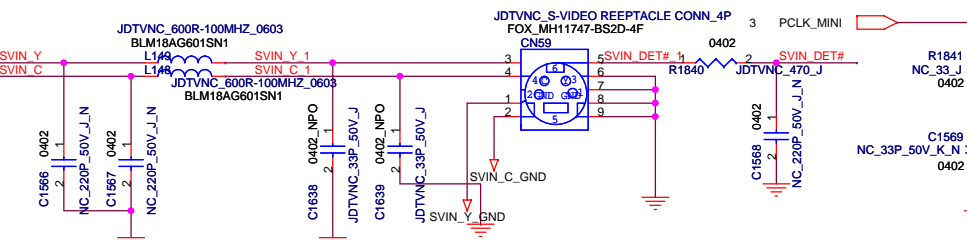
Date: Thursday, August 10, 2006 Sheet 31 of 78

Special mini stereo jack



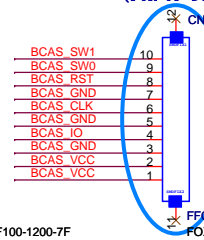
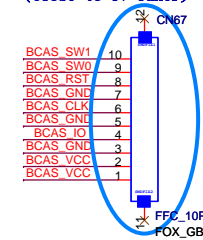
040406 Modify BOM roul
 (1)Mini PCI socket circuit group change part neam from TV_ to normal.
 (2)Special mini stereo jack and S-VIDEO in group change part name from TV_ to JDTVNC_
 (JP digital tuner sku & No tuner SKU NOT stuff)

S-VIDEO IN



B-CAS connentor (Close to TV Tuner)

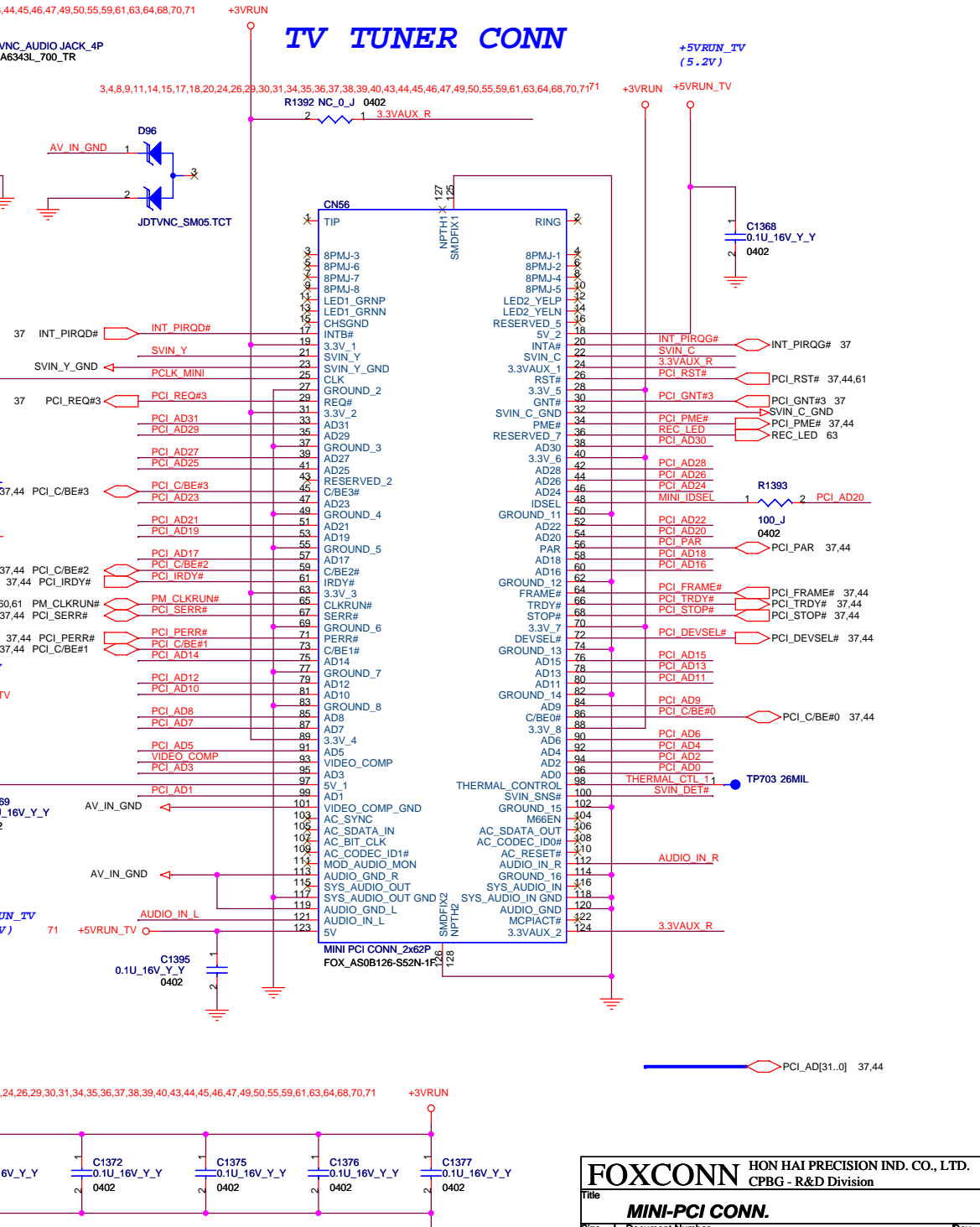
FFC CONNECT TO TV TUNER BOARD (FOR JP DIAGITAL)



BFT Test Pad

BCAS SW1	1	TP725	tpc32l_100
BCAS SW0	1	TP727	tpc32l_100
BCAS RST	1	TP726	tpc32l_100
BCAS SW1	1	TP728	tpc32l_100
BCAS SW0	1	TP729	tpc32l_100
BCAS RST	1	TP731	tpc32l_100
BCAS SW1	1	TP730	tpc32l_100

TV TUNER CONN



TV-TUNER not support CLKRUN

CN66, CN67 Change from MOLEX to FOXCONN

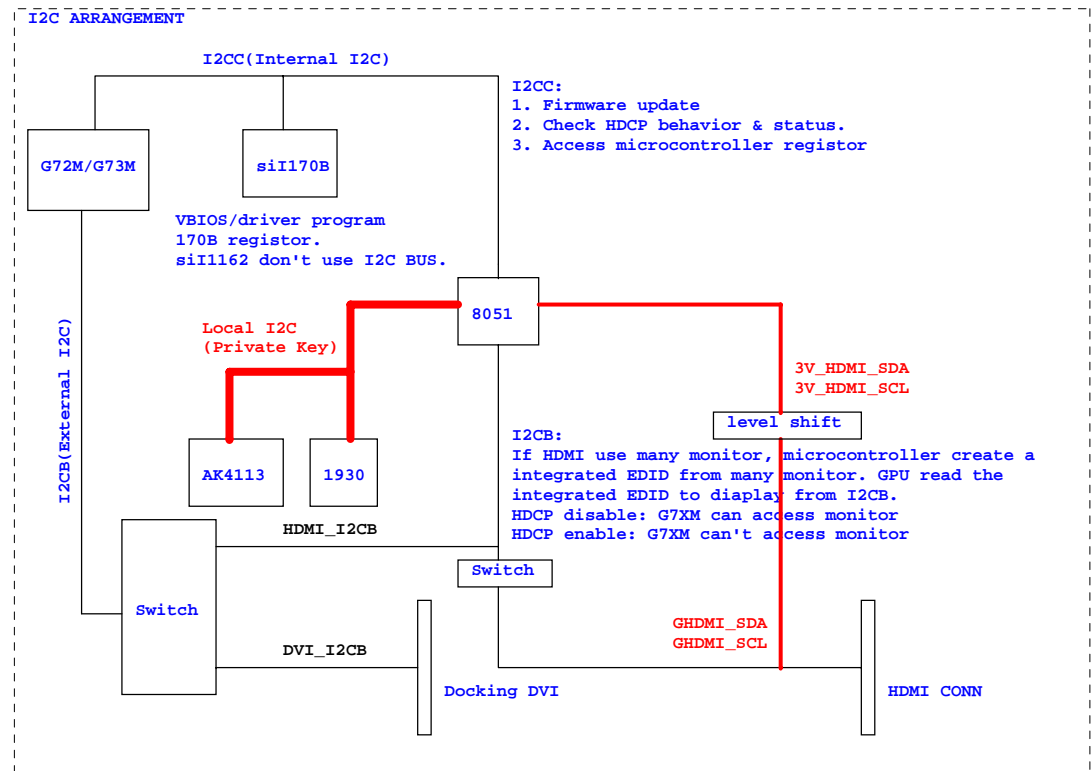
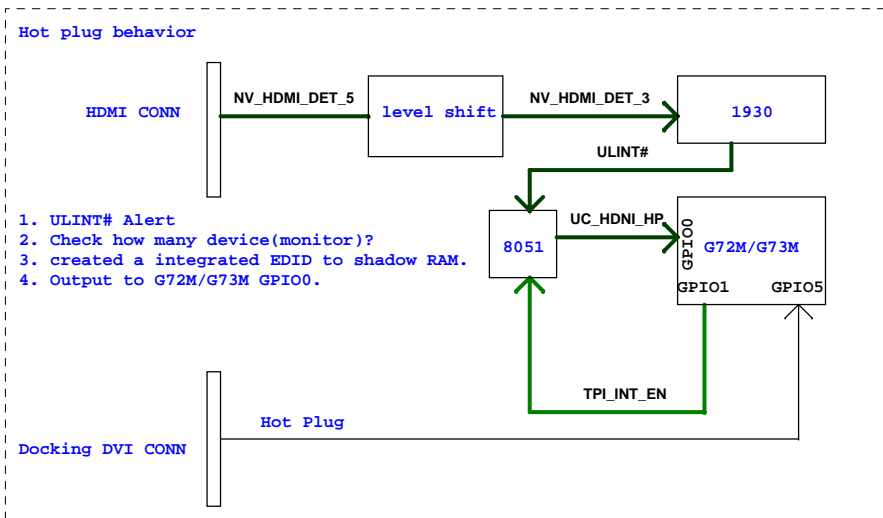
FOXCONN HON HAI PRECISION IND. CO., LTD.
 CPBG - R&D Division

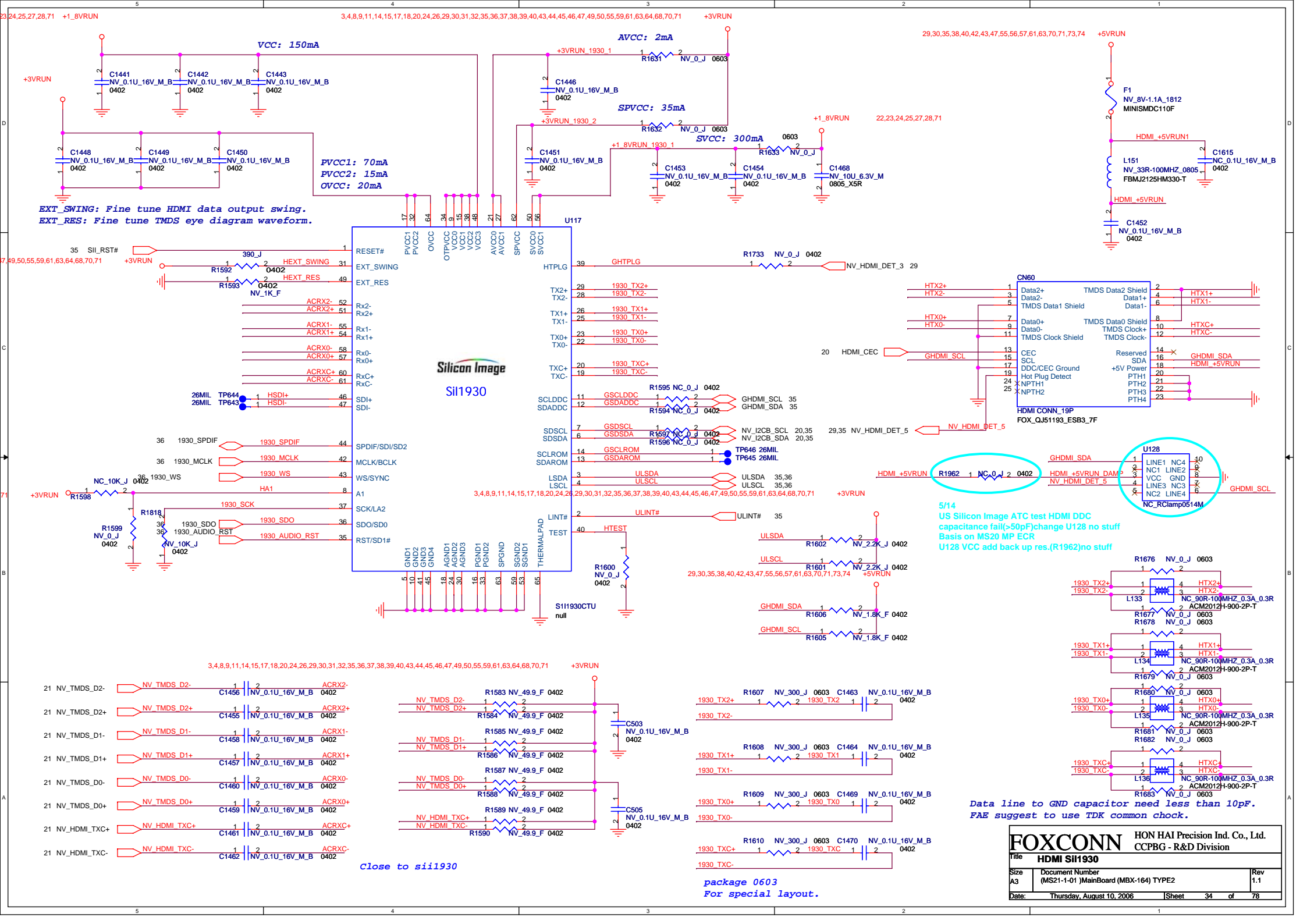
Title: **MINI-PCI CONN.**

Size: 43 Document Number: (MS21-1-01) MainBoard (MBX-164) TYPE2 Rev: 1.1

Date: Thursday, August 10, 2006 Sheet: 32 of 78

Hot plug behavior & I2C ARRANGEMENT block diagram





EXT_SWING: Fine tune HDMI data output swing.
 EXT_RES: Fine tune TMDS eye diagram waveform.

PVCC1: 70mA
 PVCC2: 15mA
 OVCC: 20mA



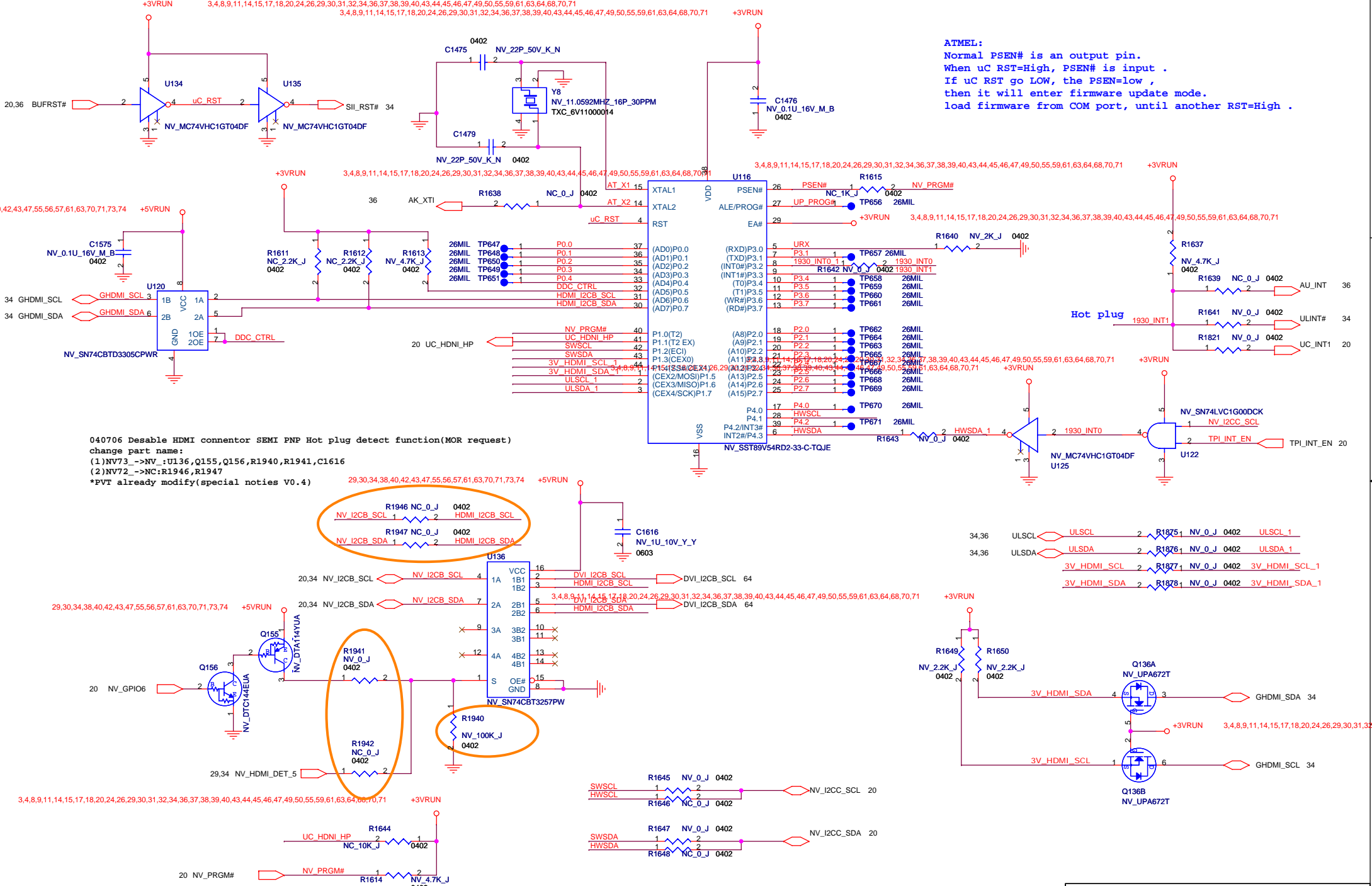
5/14
 US Silicon Image ATC test HDMI DDC
 capacitance fail(>50pF)change U128 no stuff
 Basis on MS20 MP ECR
 U128 VCC add back up res.(R1962)no stuff

Data line to GND capacitor need less than 10pF.
 FAE suggest to use TDK common chock.

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title HDMI SiI1930		
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 34	of 78

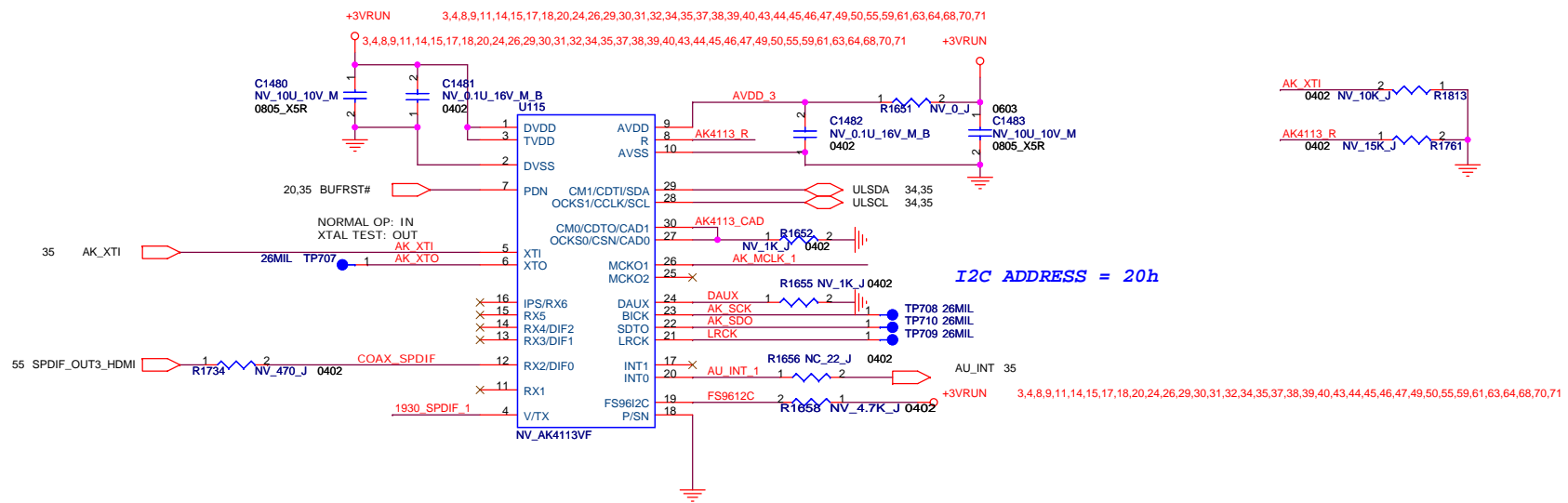
Close to sii1930

package 0603
 For special layout.

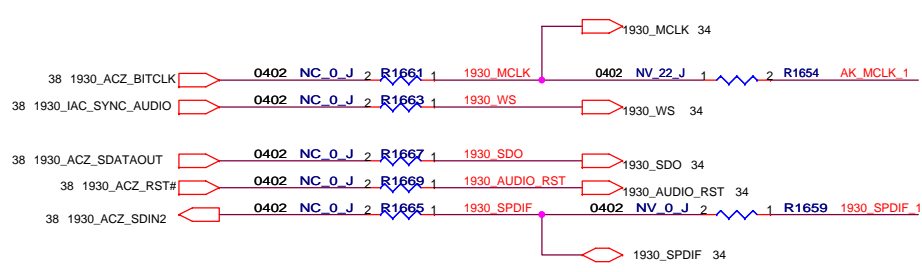


ATMEL:
 Normal PSEN# is an output pin.
 When uC RST=High, PSEN# is input .
 If uC RST go LOW, the PSEN=low ,
 then it will enter firmware update mode.
 load firmware from COM port, until another RST=High .

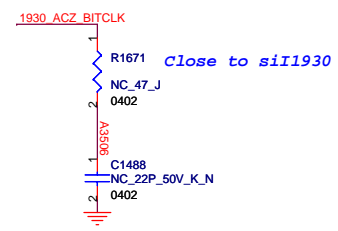
040706 Desable HDMI connentor SEMI PNP Hot plug detect function(MOR request)
 change part name:
 (1)NV73_ ->NV :U136,Q155,Q156,R1940,R1941,C1616
 (2)NV72_ ->NC:R1946,R1947
 *PVT already modify(special noties V0.4)

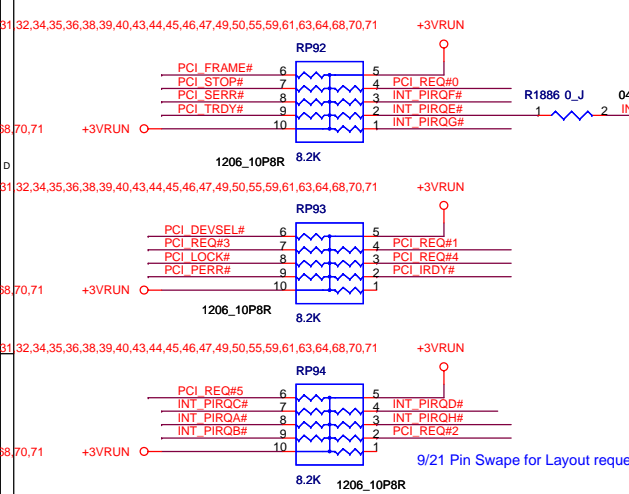


I2C ADDRESS = 20h

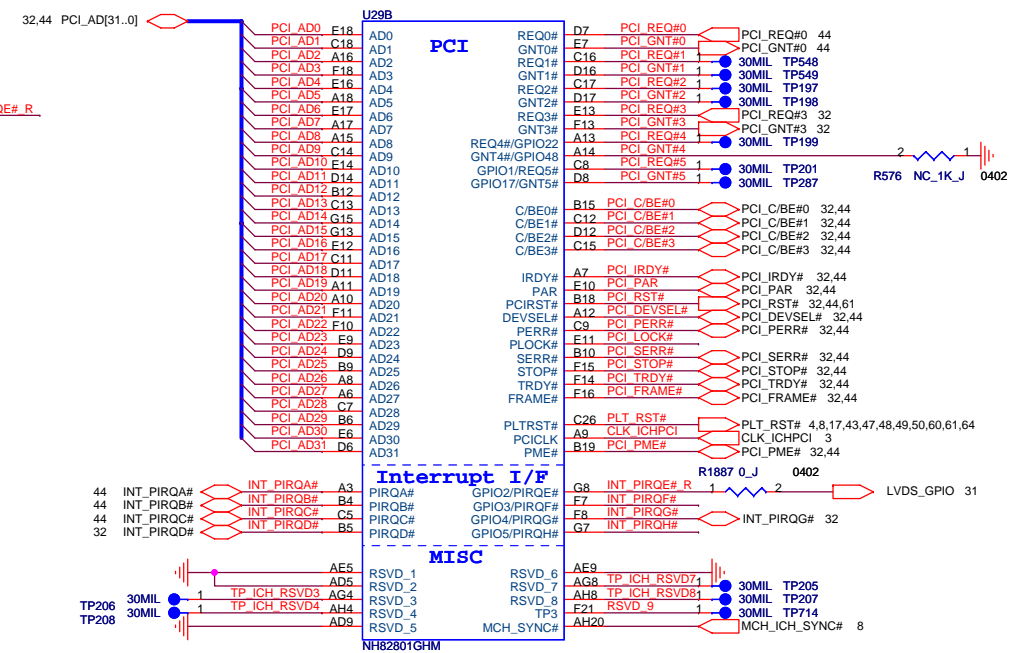


SPIDIF: AK4113-->Sil1930
Azalia: ICH7-->Sil1930



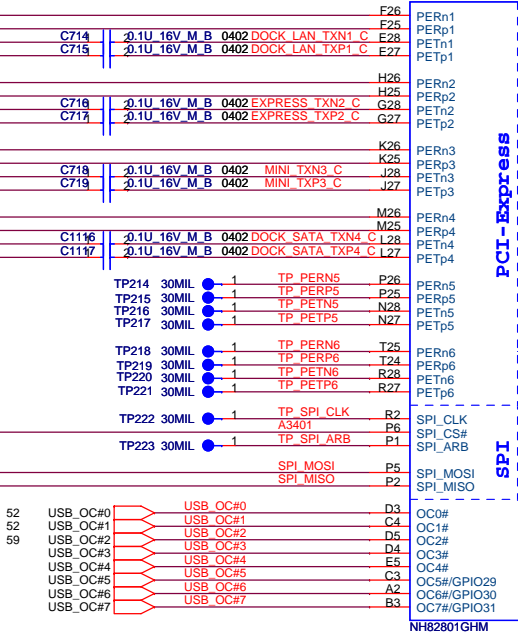
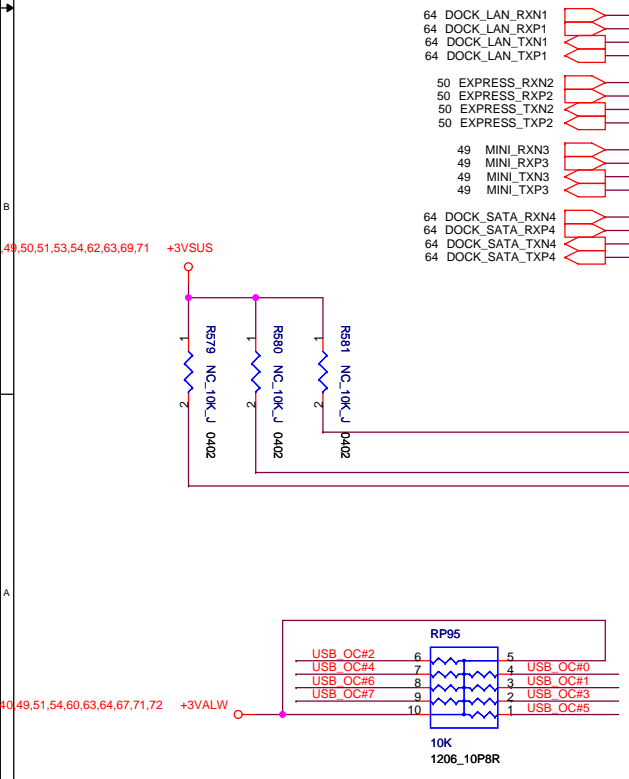


PCI Pullups



Strap for Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	HI	HI
PCI	HI	LOW



Direct Media Interface

SPI

USB

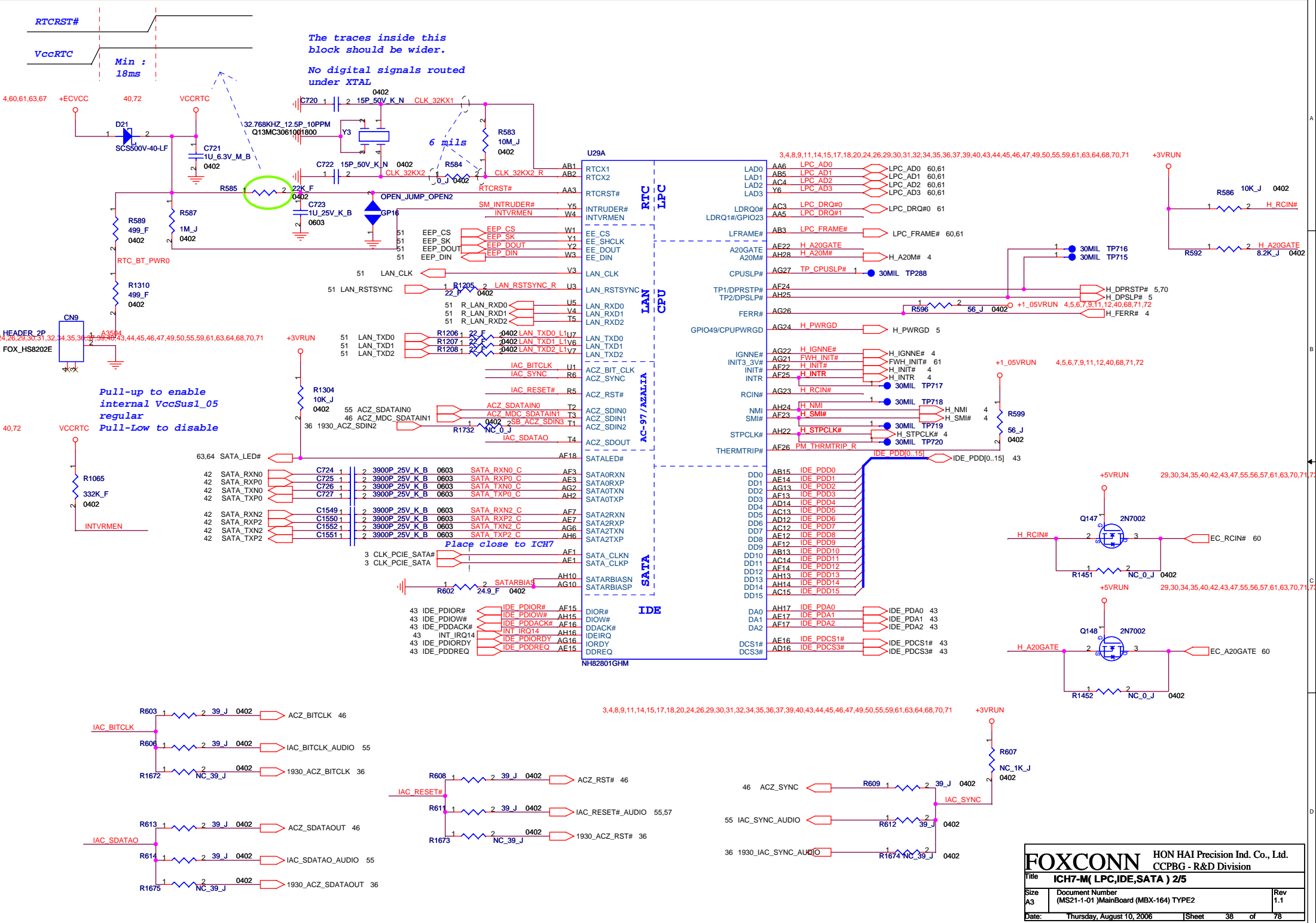
Place within 500 mils of ICH

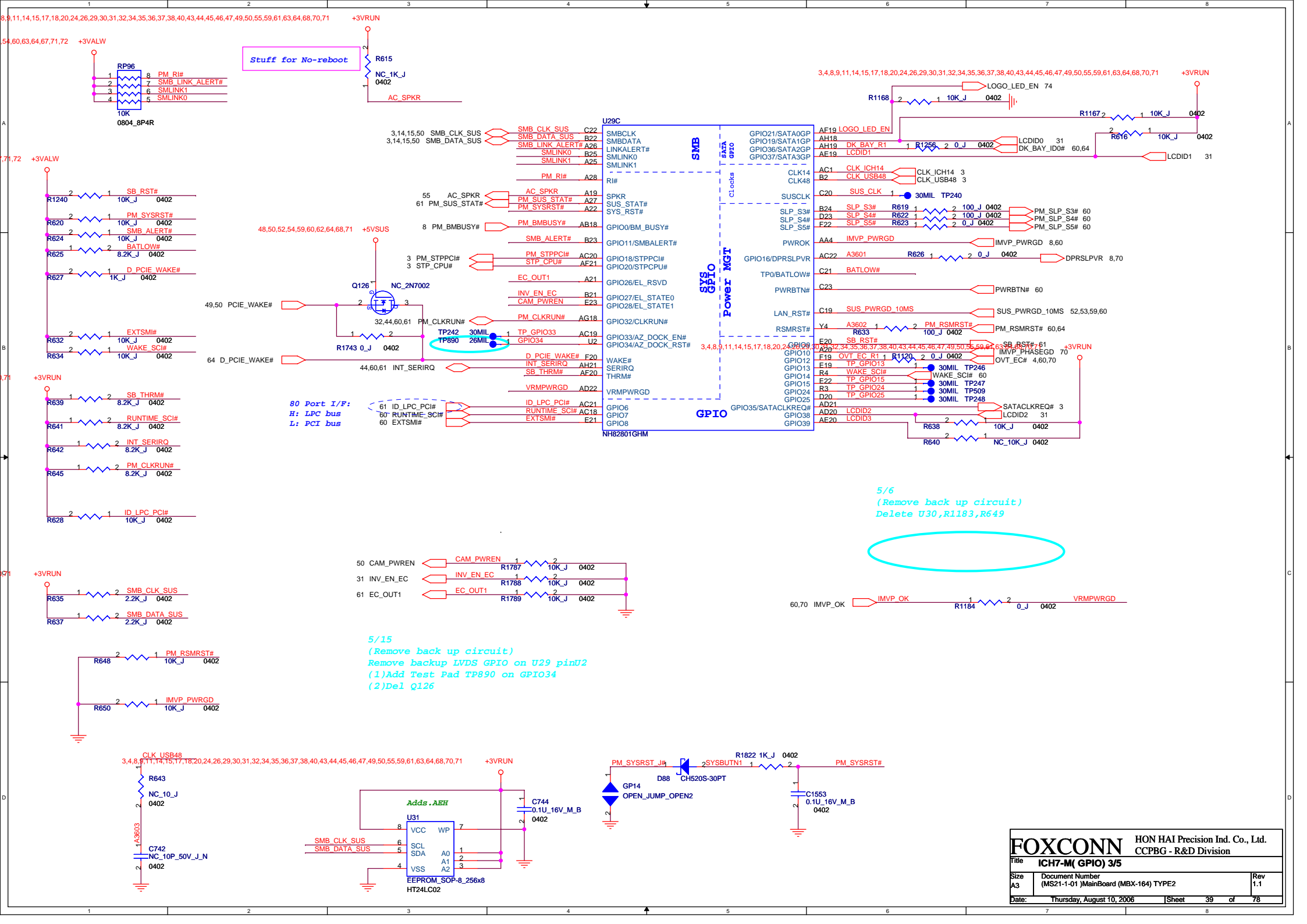
Place within 500 mils of ICH and don't routing next to high speed signals

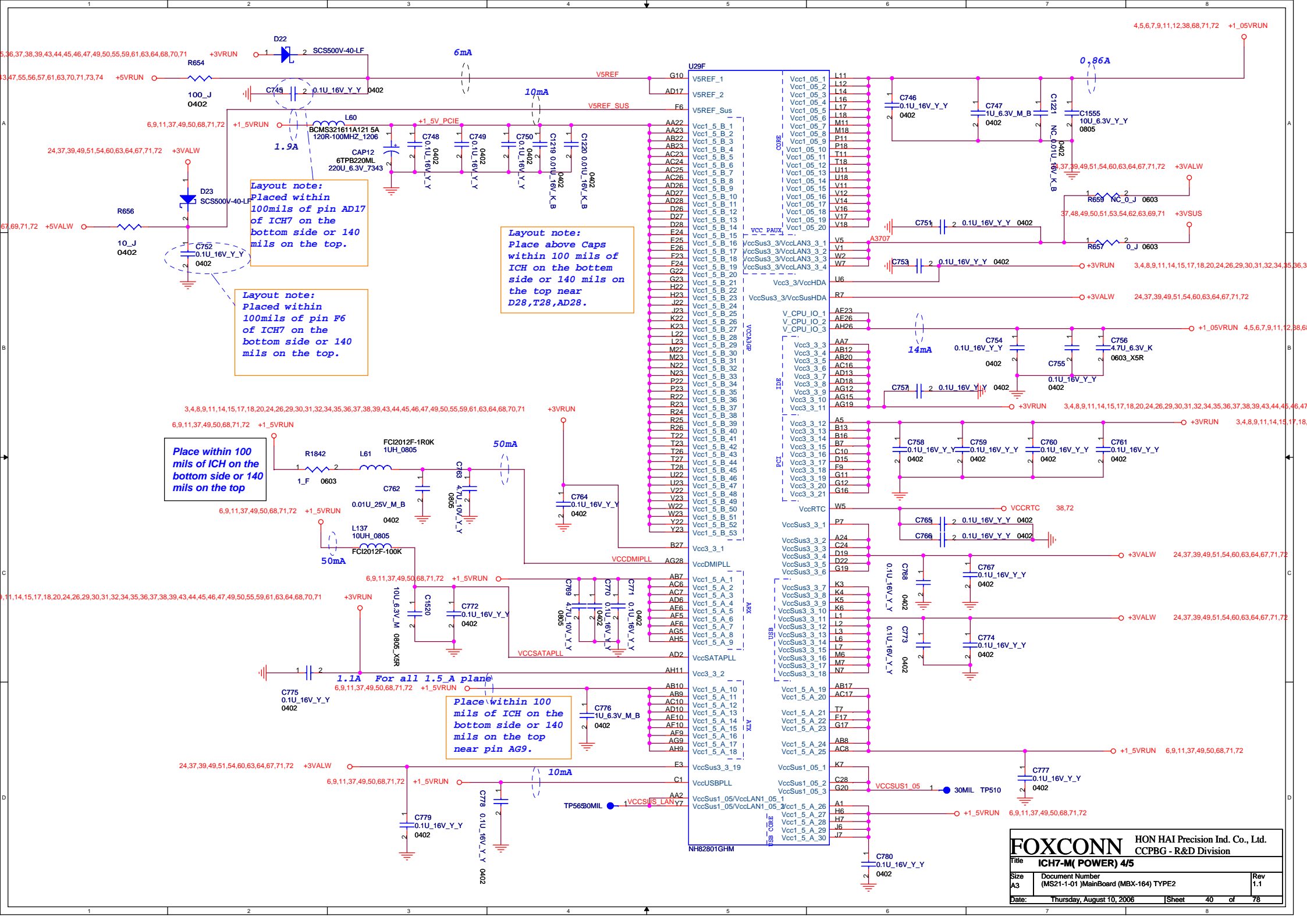
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **ICH7-M(PC/DMI/USB/PCIE) 1/5**

Size A3	Document Number (MS21-1-01)MainBoard (MBX-164) TYPE2	Rev 1.1
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Layout note:
Placed within 100mils of pin AD17 on the bottom side or 140 mils on the top.

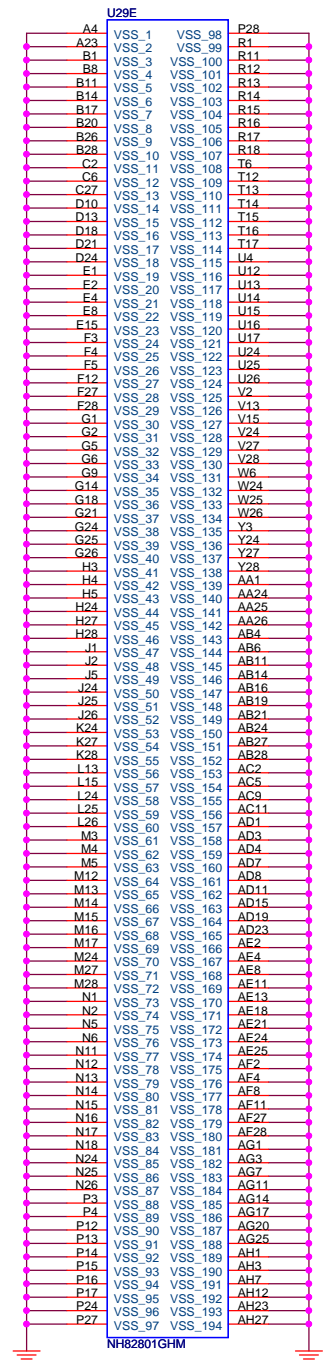
Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28.

Place within 100 mils of ICH on the bottom side or 140 mils on the top

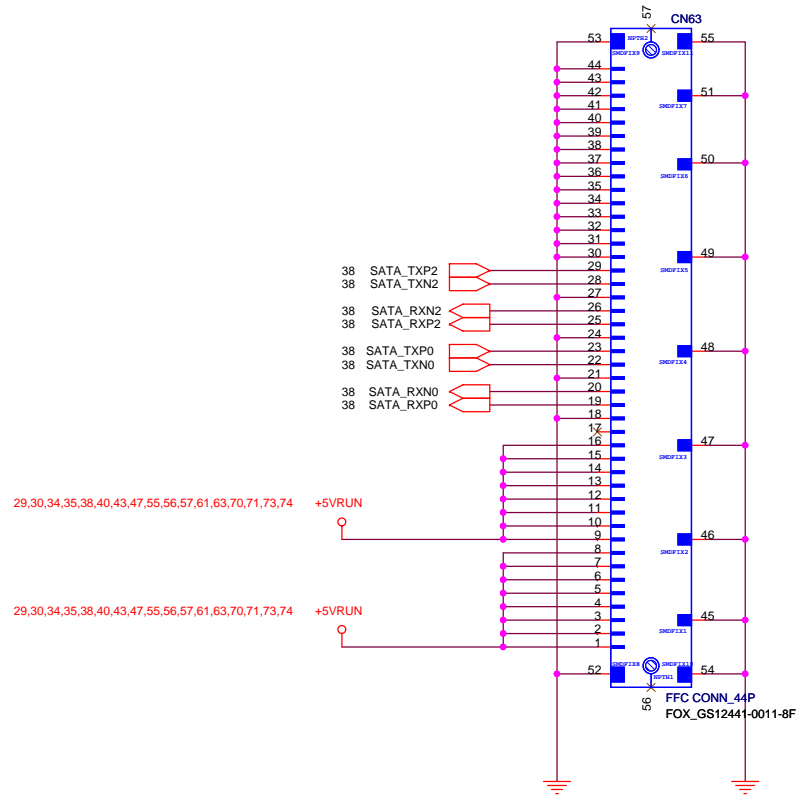
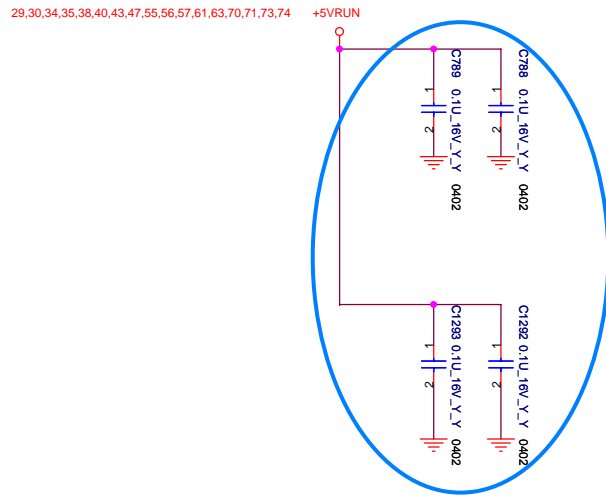
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.

AA22	Vcc1_5_B_1
AA23	Vcc1_5_B_2
AB22	Vcc1_5_B_3
AB23	Vcc1_5_B_4
AC23	Vcc1_5_B_5
AC24	Vcc1_5_B_6
AC25	Vcc1_5_B_7
AC26	Vcc1_5_B_8
AD25	Vcc1_5_B_9
AD27	Vcc1_5_B_10
AD28	Vcc1_5_B_11
D26	Vcc1_5_B_12
D27	Vcc1_5_B_13
D28	Vcc1_5_B_14
E24	Vcc1_5_B_15
E25	Vcc1_5_B_16
F23	Vcc1_5_B_17
F24	Vcc1_5_B_18
G22	Vcc1_5_B_19
G23	Vcc1_5_B_20
H22	Vcc1_5_B_21
H23	Vcc1_5_B_22
J22	Vcc1_5_B_23
J23	Vcc1_5_B_24
K22	Vcc1_5_B_25
K23	Vcc1_5_B_26
L22	Vcc1_5_B_27
L23	Vcc1_5_B_28
M23	Vcc1_5_B_29
N22	Vcc1_5_B_30
N23	Vcc1_5_B_31
P22	Vcc1_5_B_32
P23	Vcc1_5_B_33
R22	Vcc1_5_B_34
R23	Vcc1_5_B_35
R24	Vcc1_5_B_36
R25	Vcc1_5_B_37
T22	Vcc1_5_B_38
T23	Vcc1_5_B_39
T26	Vcc1_5_B_40
T27	Vcc1_5_B_41
T28	Vcc1_5_B_42
U22	Vcc1_5_B_43
U23	Vcc1_5_B_44
V23	Vcc1_5_B_45
W22	Vcc1_5_B_46
W23	Vcc1_5_B_47
Y22	Vcc1_5_B_48
Y23	Vcc1_5_B_49
Y24	Vcc1_5_B_50
Y25	Vcc1_5_B_51
Y26	Vcc1_5_B_52
Y27	Vcc1_5_B_53
AB7	Vcc1_5_A_1
AC6	Vcc1_5_A_2
AC7	Vcc1_5_A_3
AD6	Vcc1_5_A_4
AE6	Vcc1_5_A_5
AF6	Vcc1_5_A_6
AG5	Vcc1_5_A_7
AH5	Vcc1_5_A_8
AB10	Vcc1_5_A_10
AC10	Vcc1_5_A_11
AD10	Vcc1_5_A_12
AE10	Vcc1_5_A_13
AF10	Vcc1_5_A_14
AG9	Vcc1_5_A_15
AH9	Vcc1_5_A_16
AB17	Vcc1_5_A_19
AC17	Vcc1_5_A_20
T7	Vcc1_5_A_21
F17	Vcc1_5_A_22
G17	Vcc1_5_A_23
AB8	Vcc1_5_A_24
AC8	Vcc1_5_A_25
K7	Vcc1_5_A_26
C28	Vcc1_5_A_27
G20	Vcc1_5_A_28
A1	Vcc1_5_A_29
H6	Vcc1_5_A_30
H7	Vcc1_5_A_31
J6	Vcc1_5_A_32
J7	Vcc1_5_A_33



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title ICH7-M(GND) 5/5			
Size	Document Number	Rev	
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Date:	Thursday, August 10, 2006	Sheet	41 of 78

5/6
 For power droup cause 0.16V voltage loss Issue
 (1)F7,F8,F19,F20 no stuff
 (2)Co-layout normal open gap GP17-GP18 with fuse
 5/27 Delete SATA HDD Fuse backup circuit
 (1)Remove F7,F8,F19,F20 Pad
 (2)Remove GP17-GP18 open gap



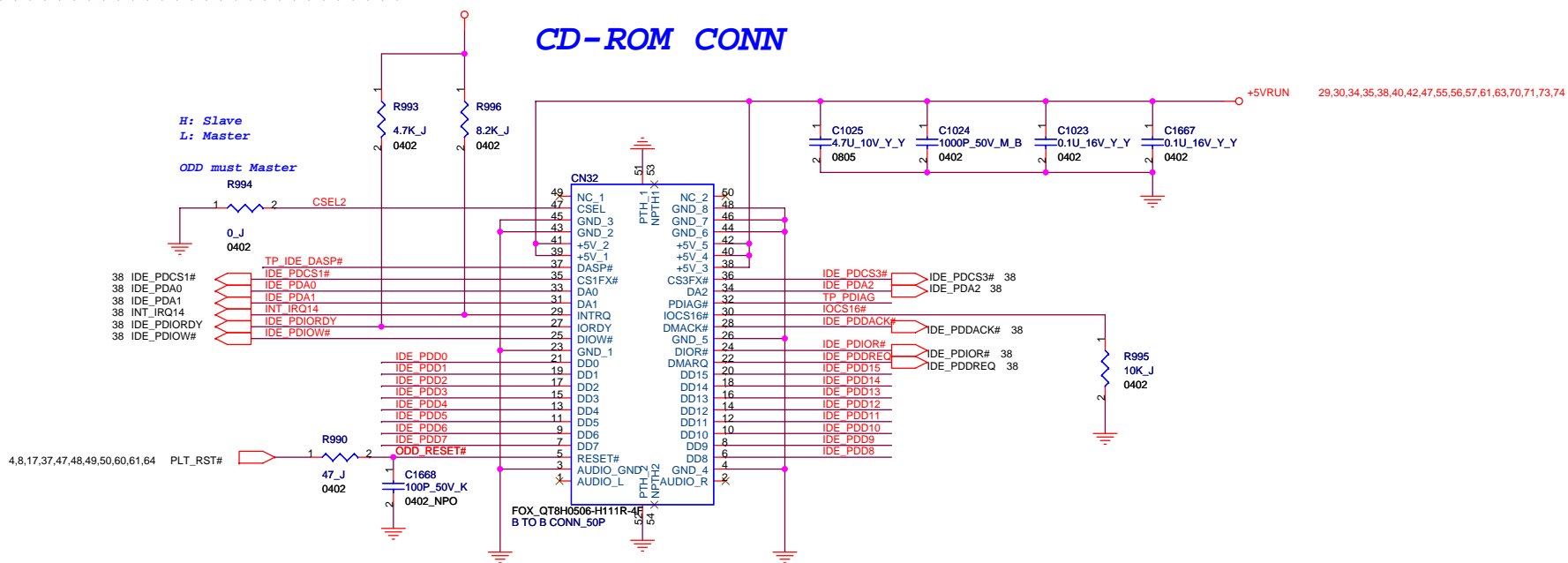
3,4,8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,44,45,46,47,49,50,55,59,61,63,64,68,70,71

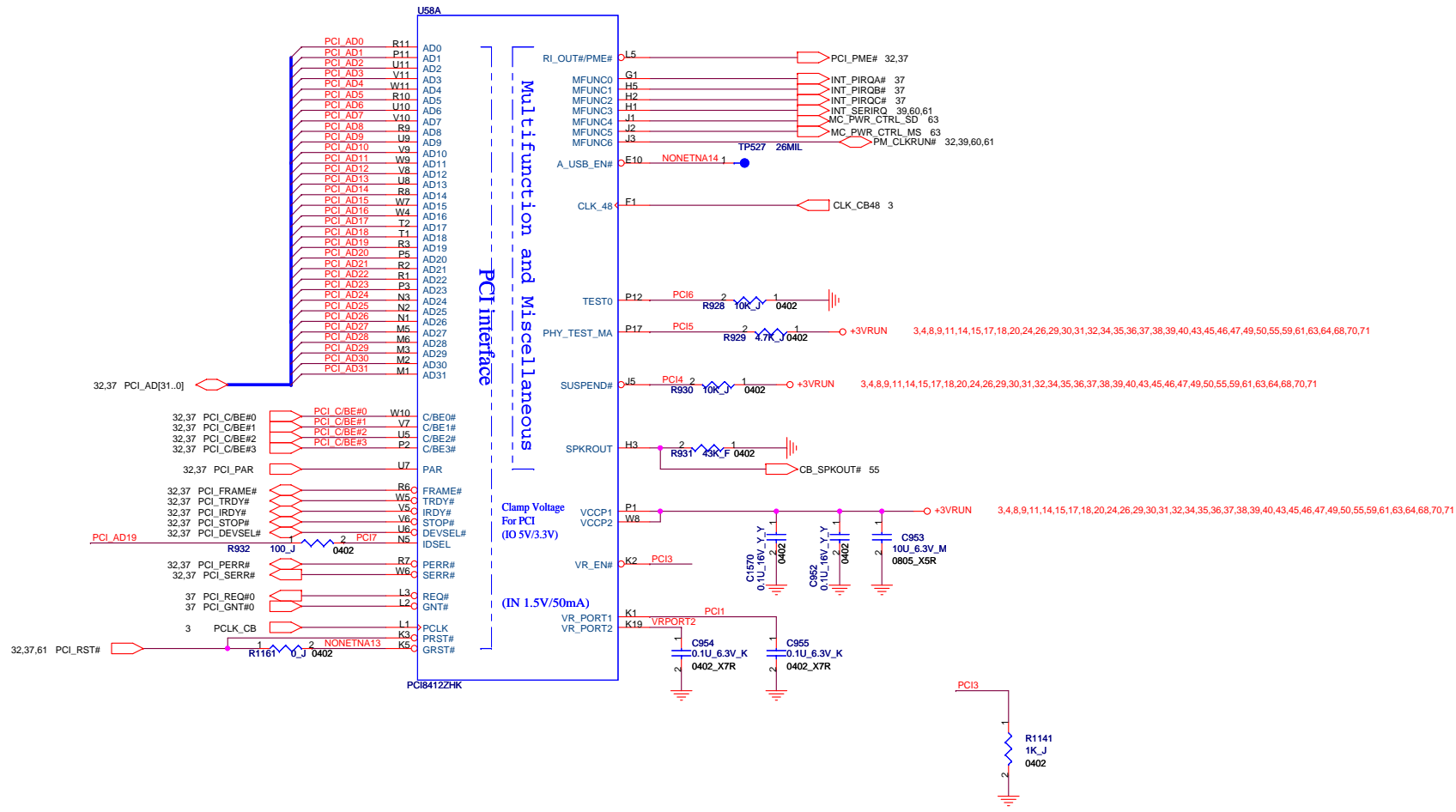
38 IDE_PDD[0..15] IDE_PDD[0..15]

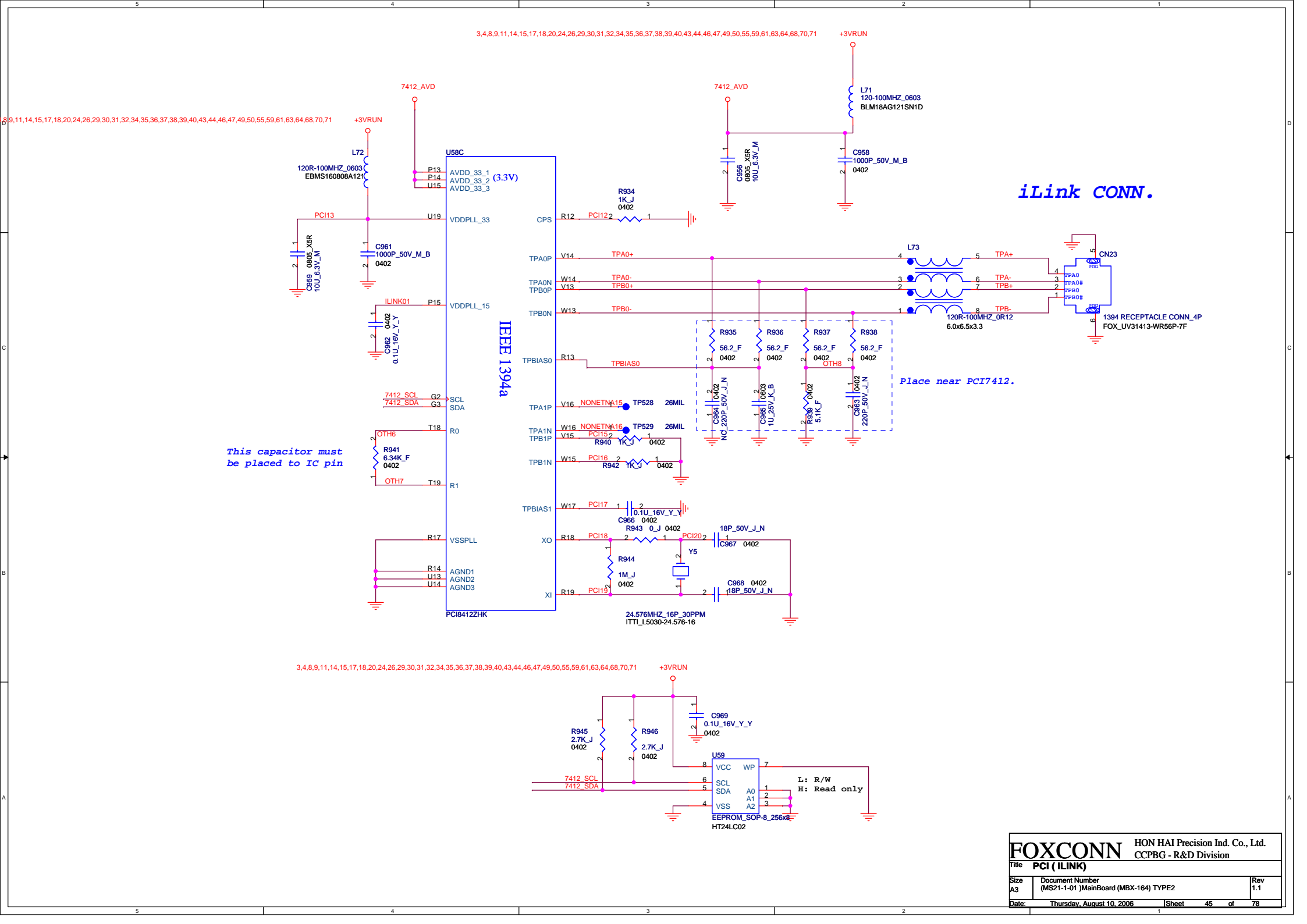
+3VRUN

CD-ROM CONN

+5VRUN 29,30,34,35,38,40,42,47,55,56,57,61,63,70,71,73,74





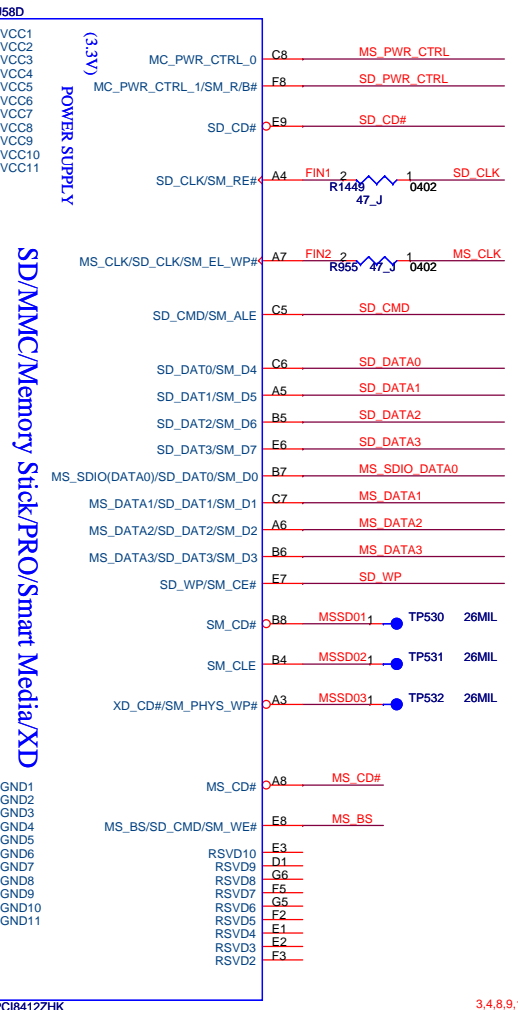
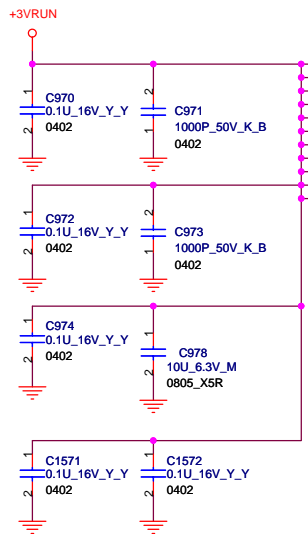


This capacitor must be placed to IC pin

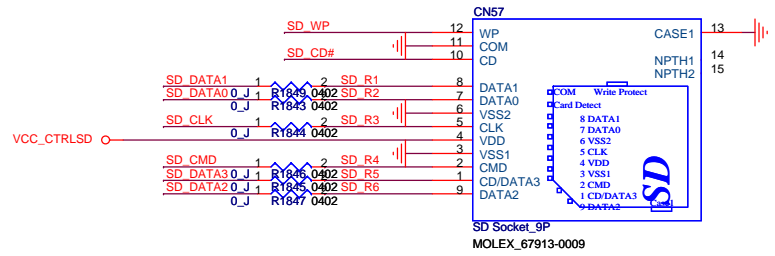
Place near PCI7412.

iLink CONN.

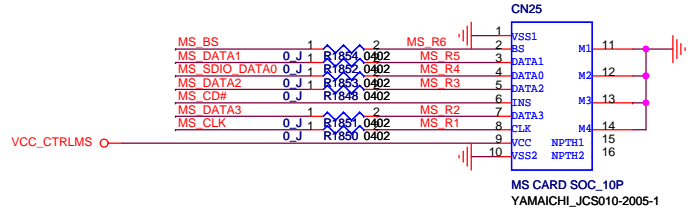
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title PCI (iLINK)			
Size A3	Document Number (MS21-1-01)MainBoard (MBX-164) TYPE2	Rev 1.1	
Date: Thursday, August 10, 2006	Sheet 45	of 78	



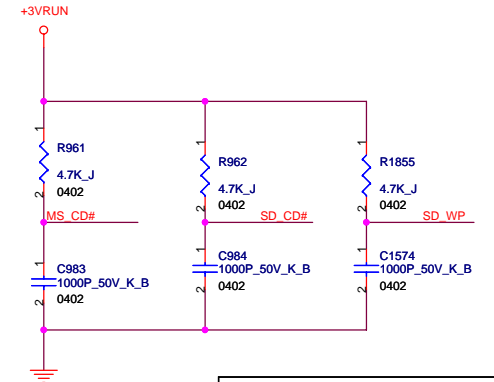
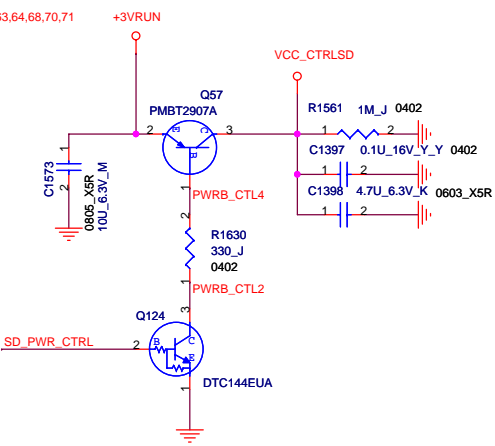
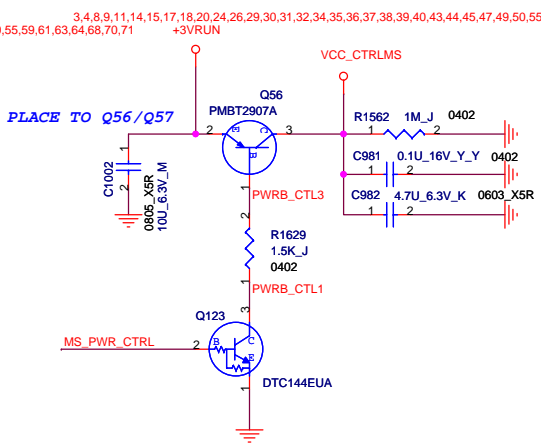
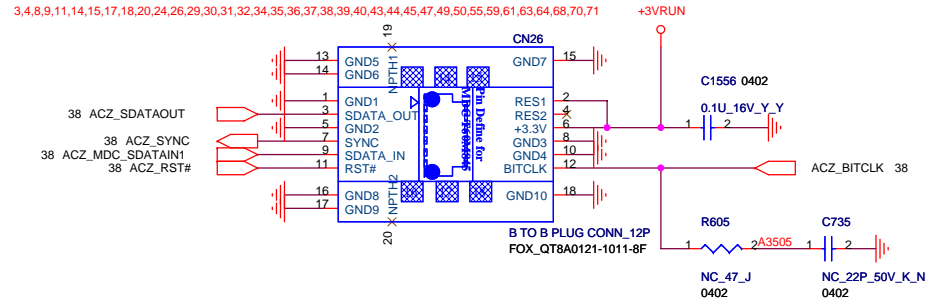
SD CONN.



MS STD/DUO CONN.



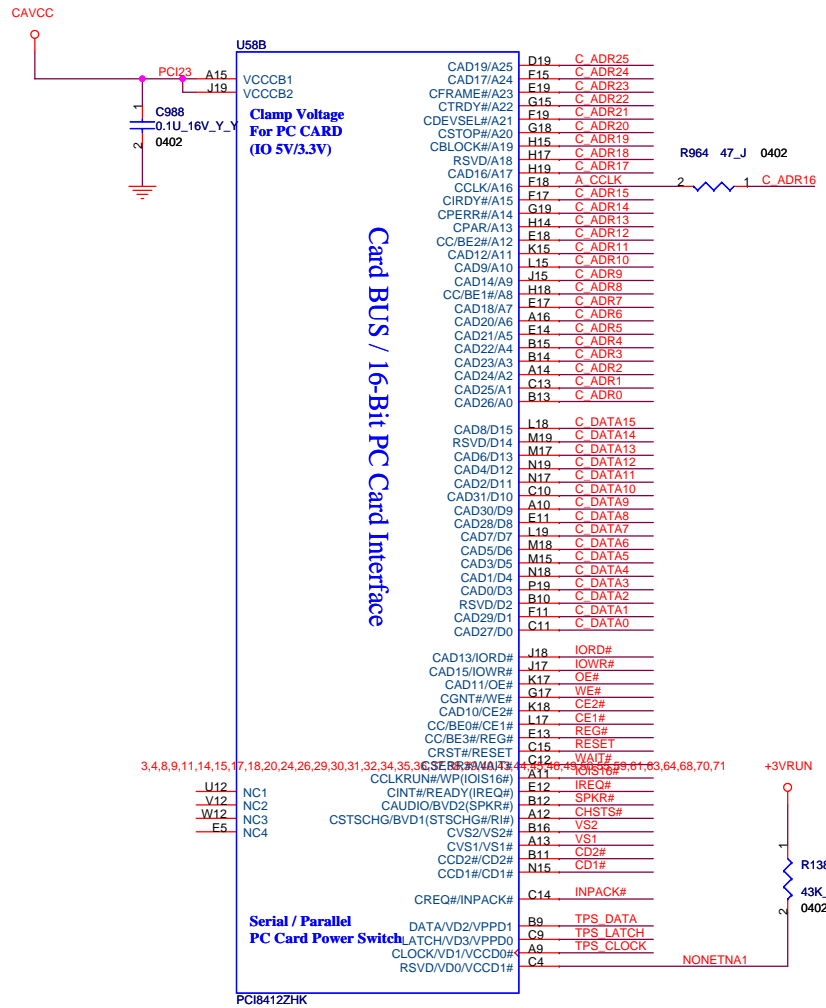
MDC CONN.



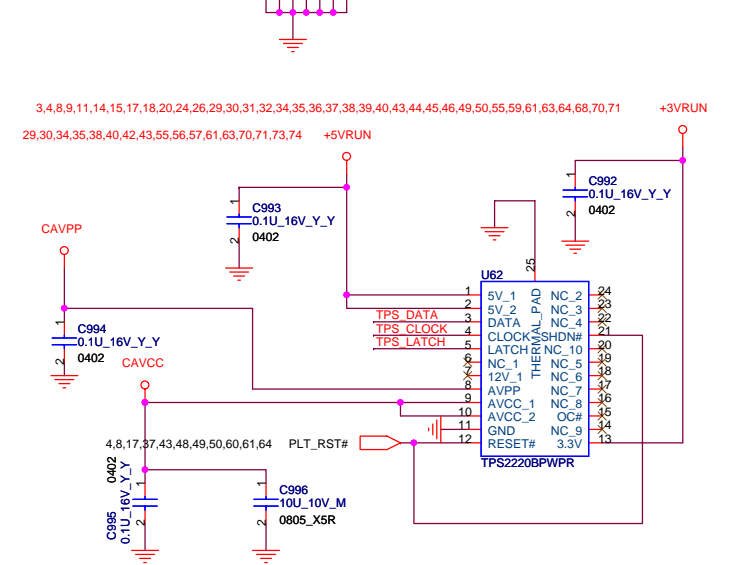
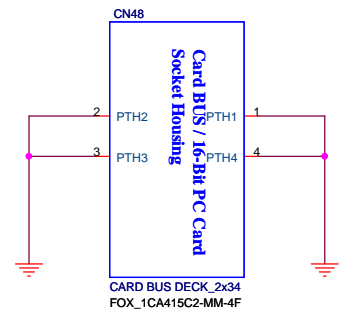
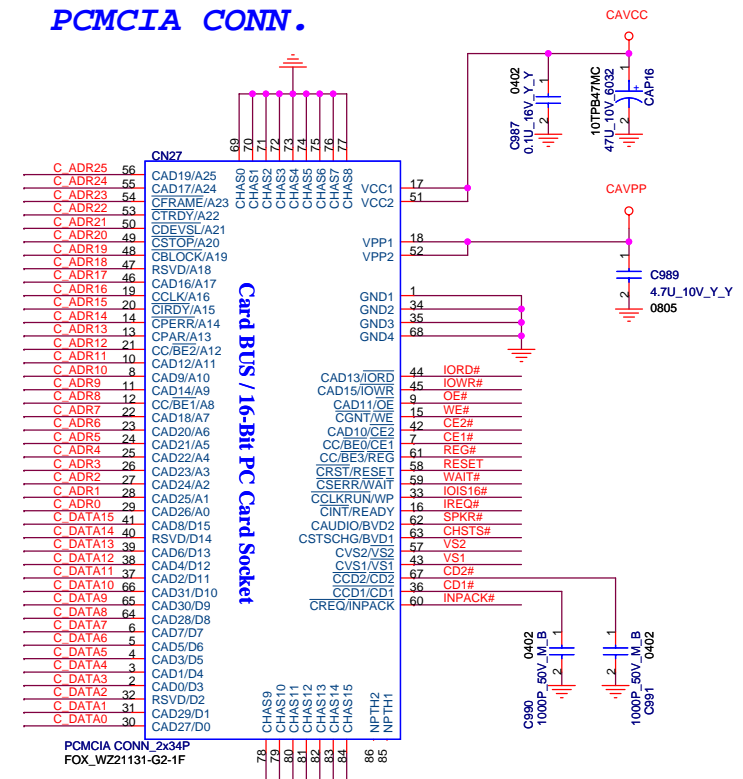
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

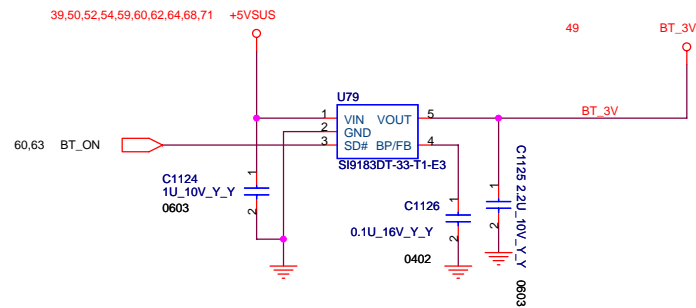
Title: **PCI (MS-DUO/MDC)**

Size: A3	Document Number: (MS21-1-01)MainBoard (MBX-164) TYPE2	Rev: 1.1
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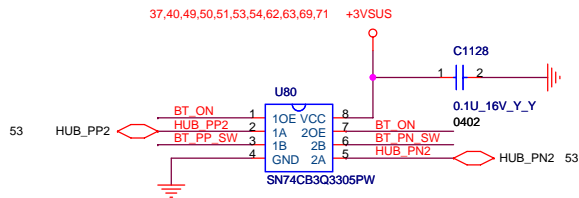
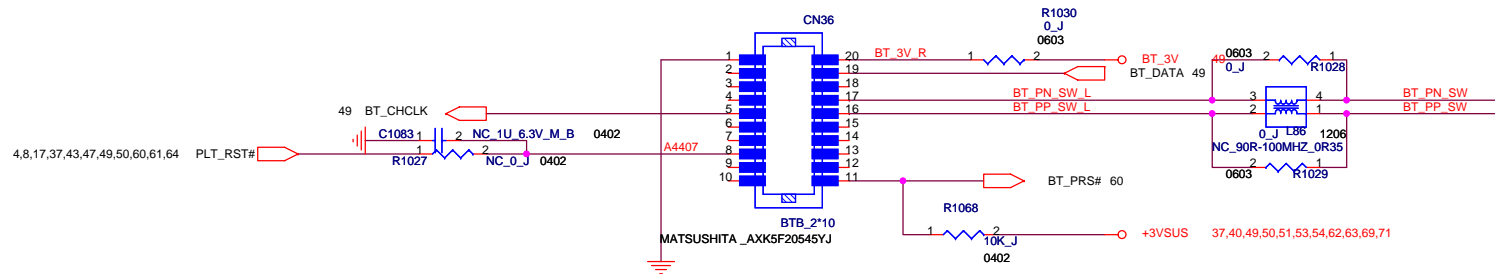


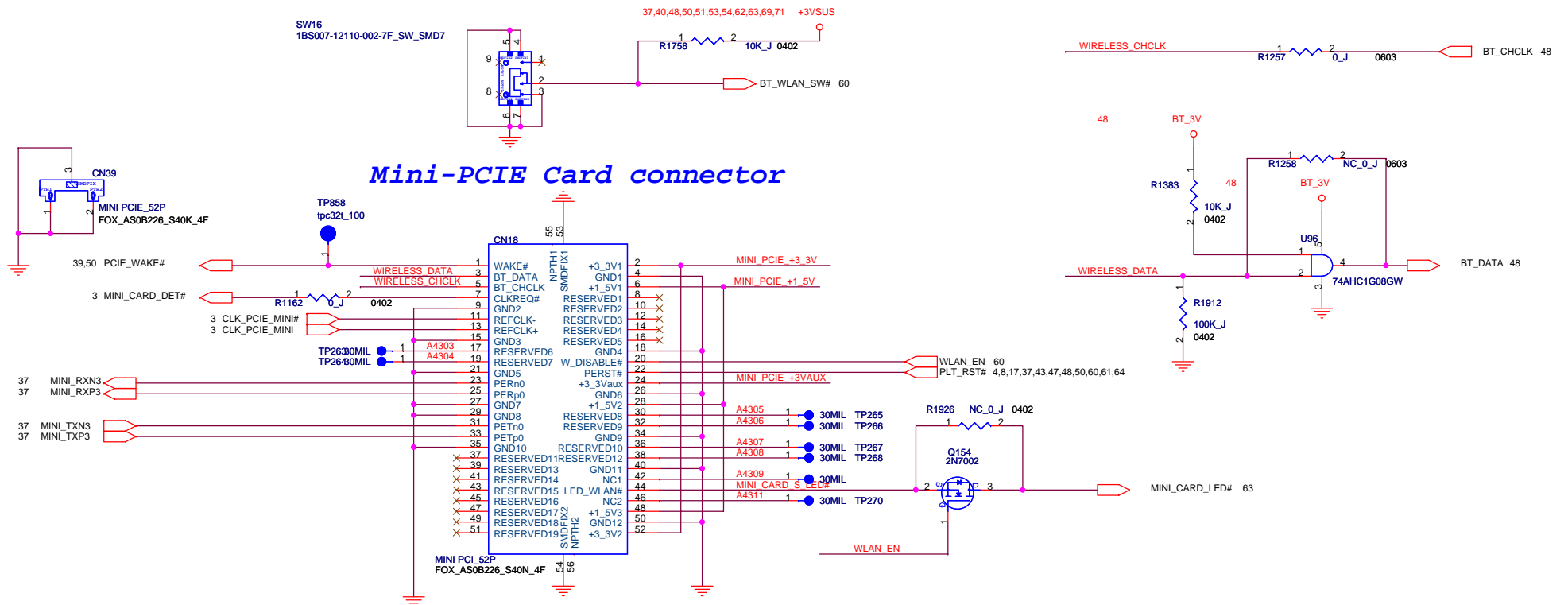
PCMCIA CONN.



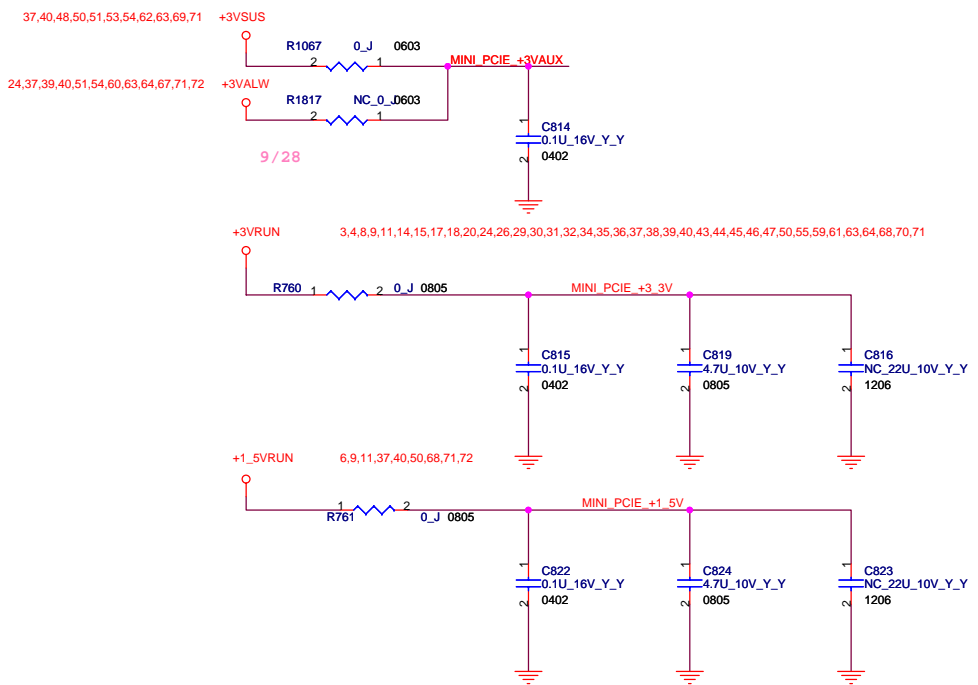


Bluetooth connector





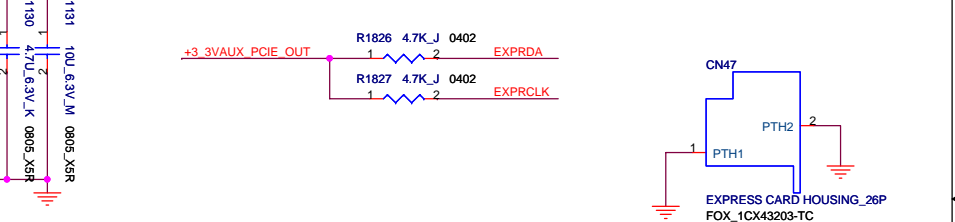
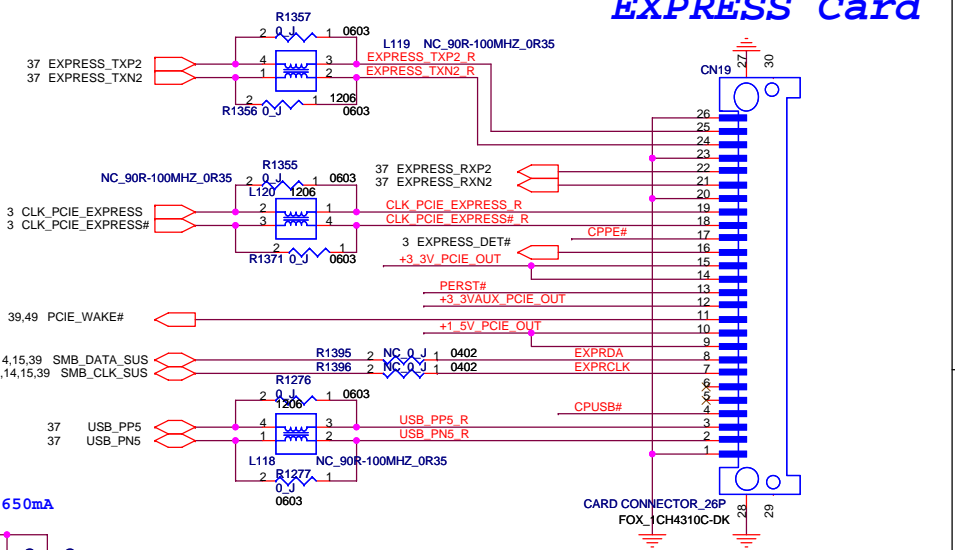
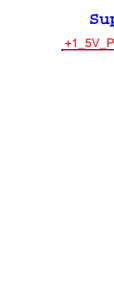
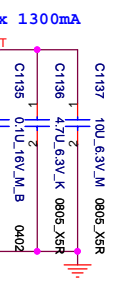
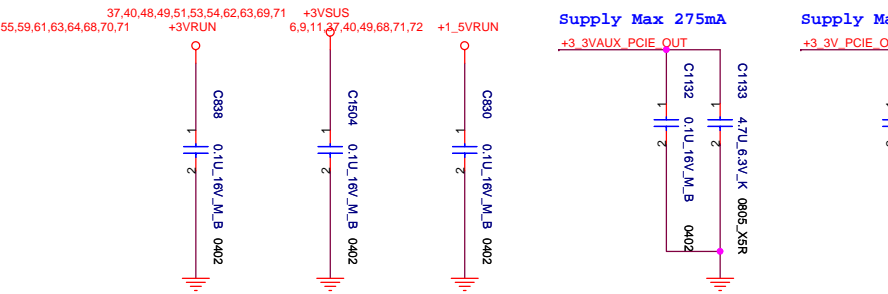
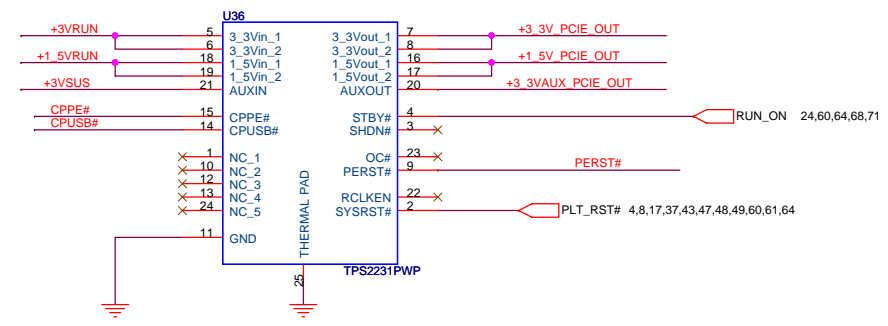
Mini-PCIE Card connector



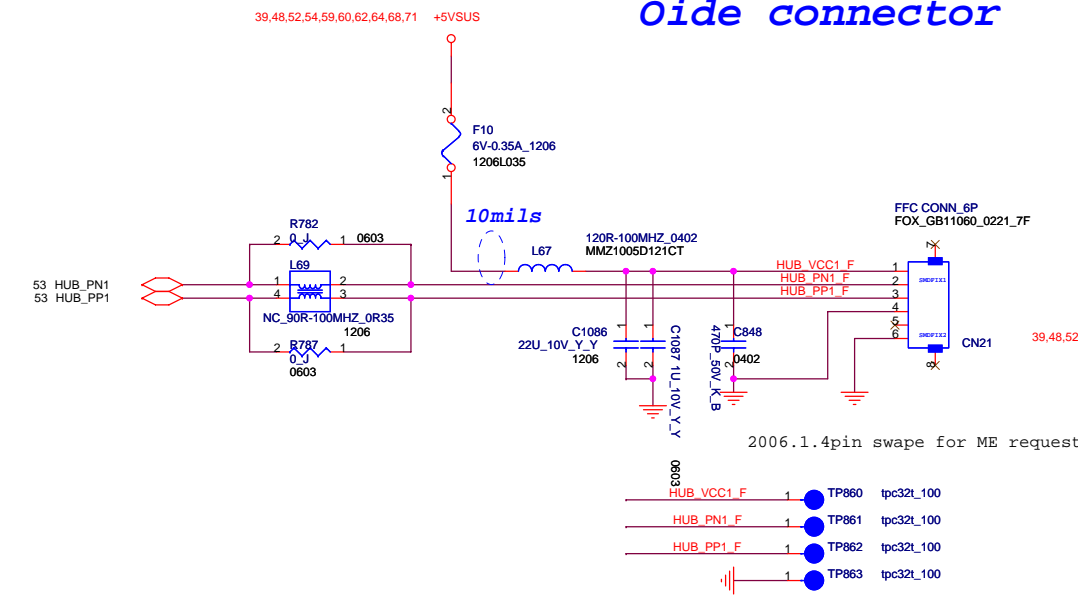
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Mini-PCIE Card		
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 49	of 78

EXPRESS Card

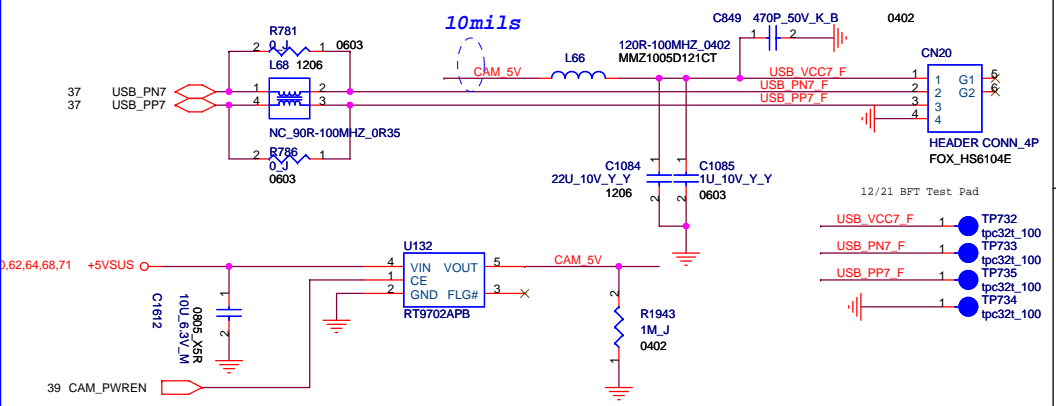
VOLTAGE INPUTS ⁽¹⁾					LOGIC INPUTS					VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT					
Off	x	x	x	x	x	Off	Off	Off				OFF	
On	x	x	0	x	x	GND	GND	GND				Shutdown	
On	x	x	1	x	1	GND	GND	GND				No Card	
On	On	On	1	0	0	On	Off	Off				Standby	
On	On	On	1	1	0	On	On	On				Card Inserted	



Oide connector



CAMERA connector

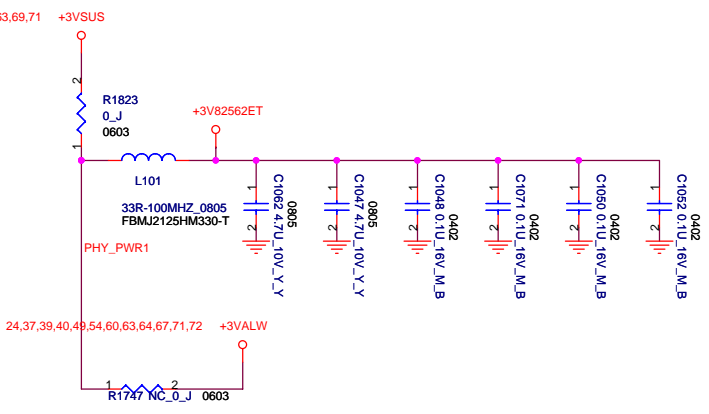
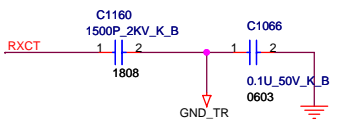
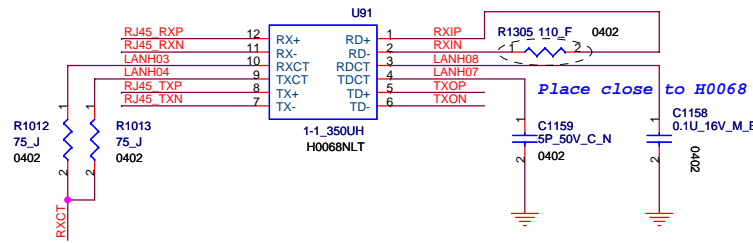
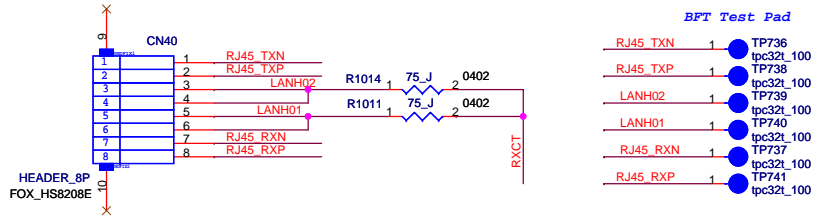


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

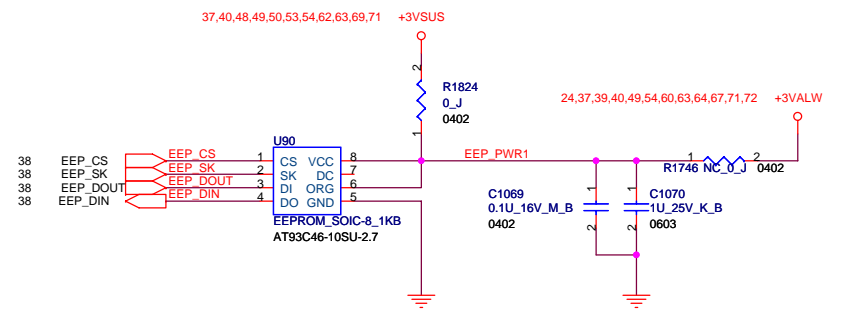
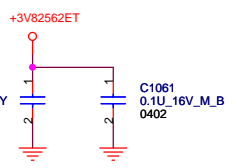
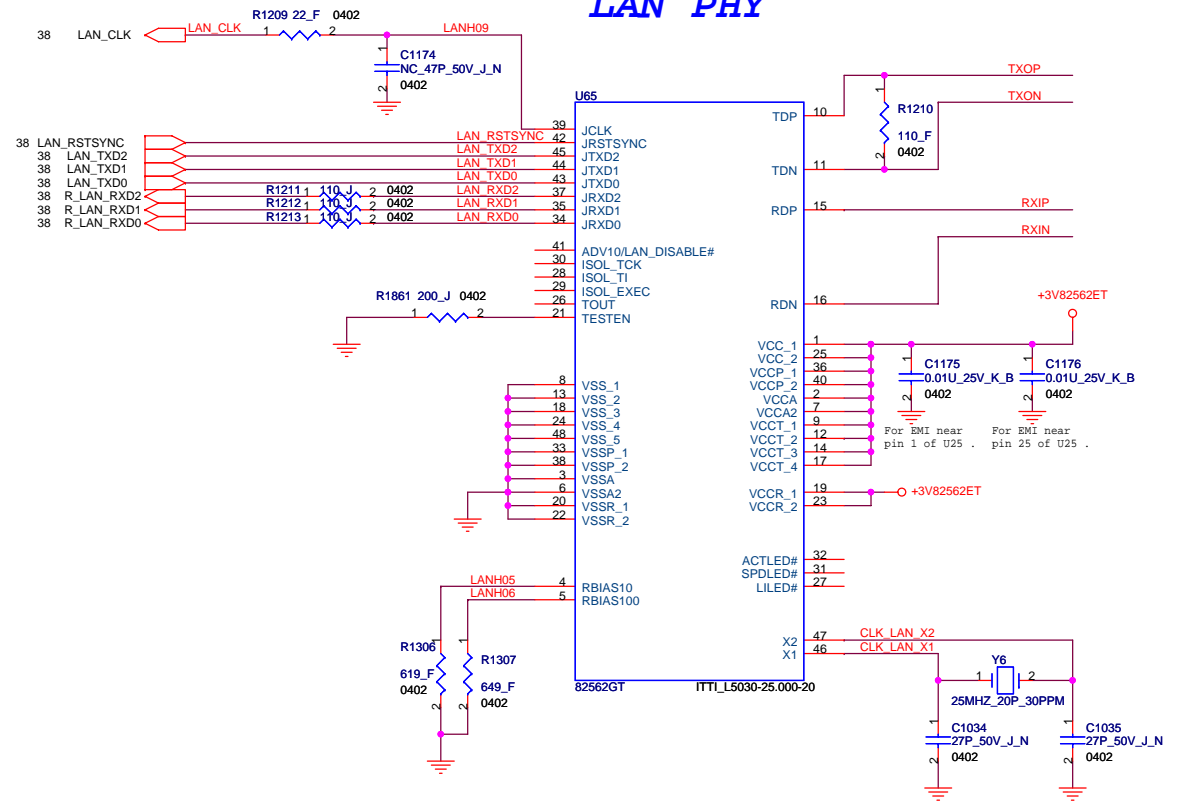
Title: **EXPRESS/CAM/OIDE**

Size: A3	Document Number: (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev: 1.1
Date: Thursday, August 10, 2006	Sheet: 50	of: 78

LAN connector

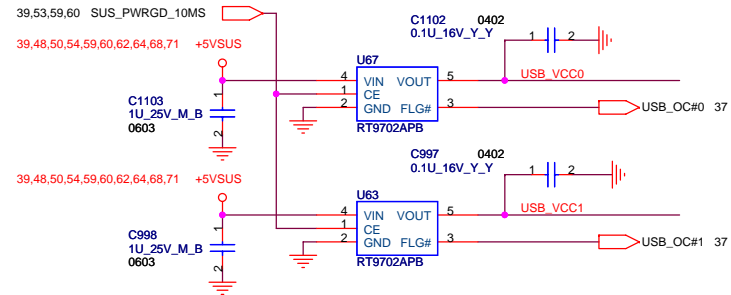
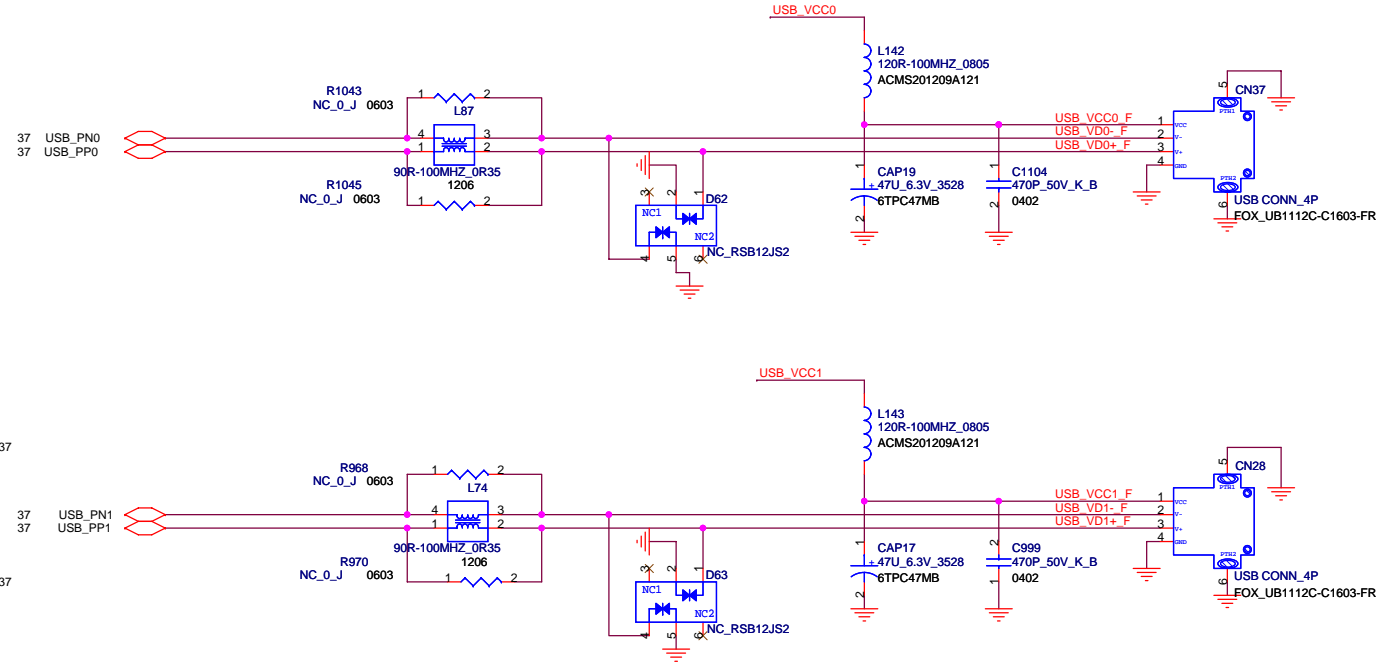


LAN PHY



Default for S3 waking up event ,
backup for S4 waking up event

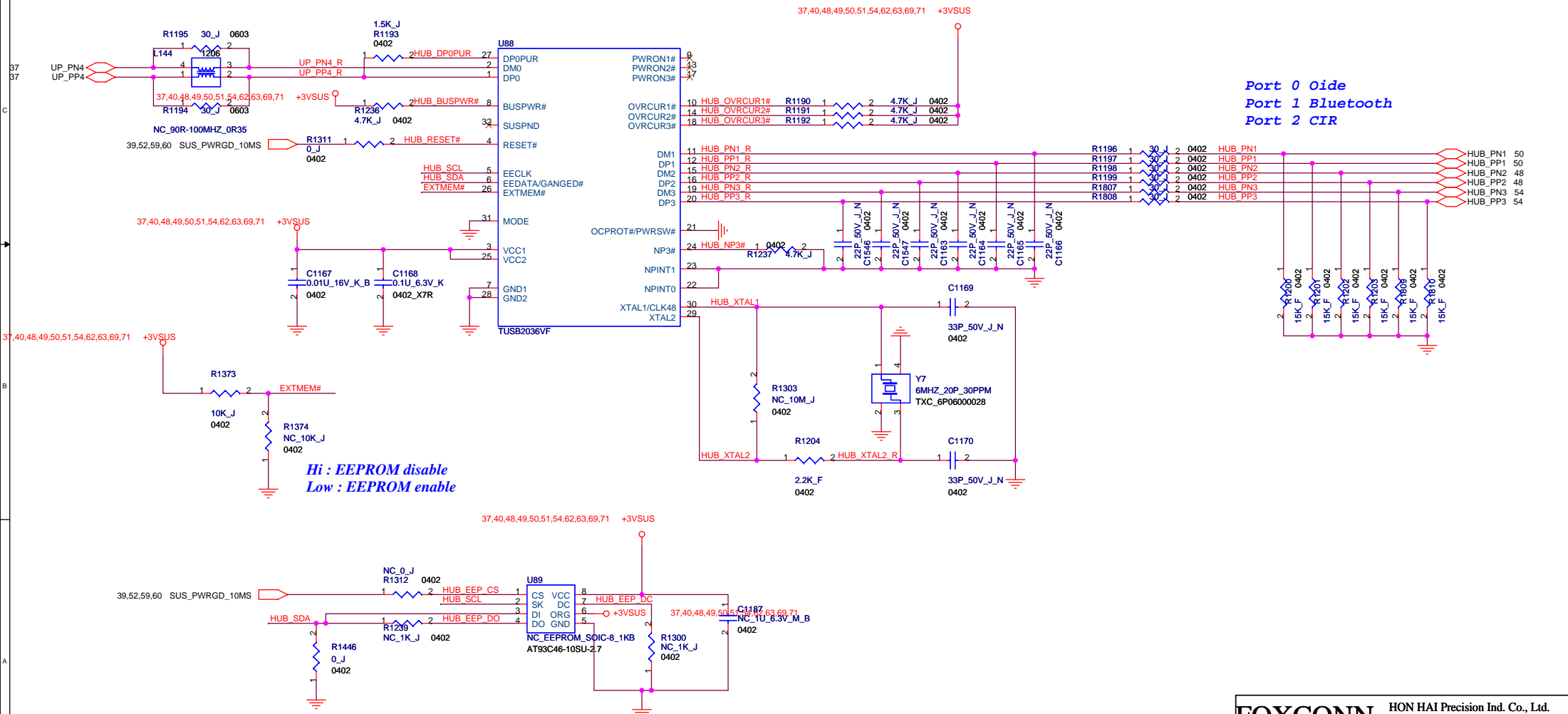
USB connector #2



FOXCONN		HON HAI Precision Ind. Co., Ltd.
		CCPBG - R&D Division
Title USB2.0/DOCKING CONN.		
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 52	of 78

Application design in datasheet 27 ohm;
but 30ohm is also in range of USB Spec.

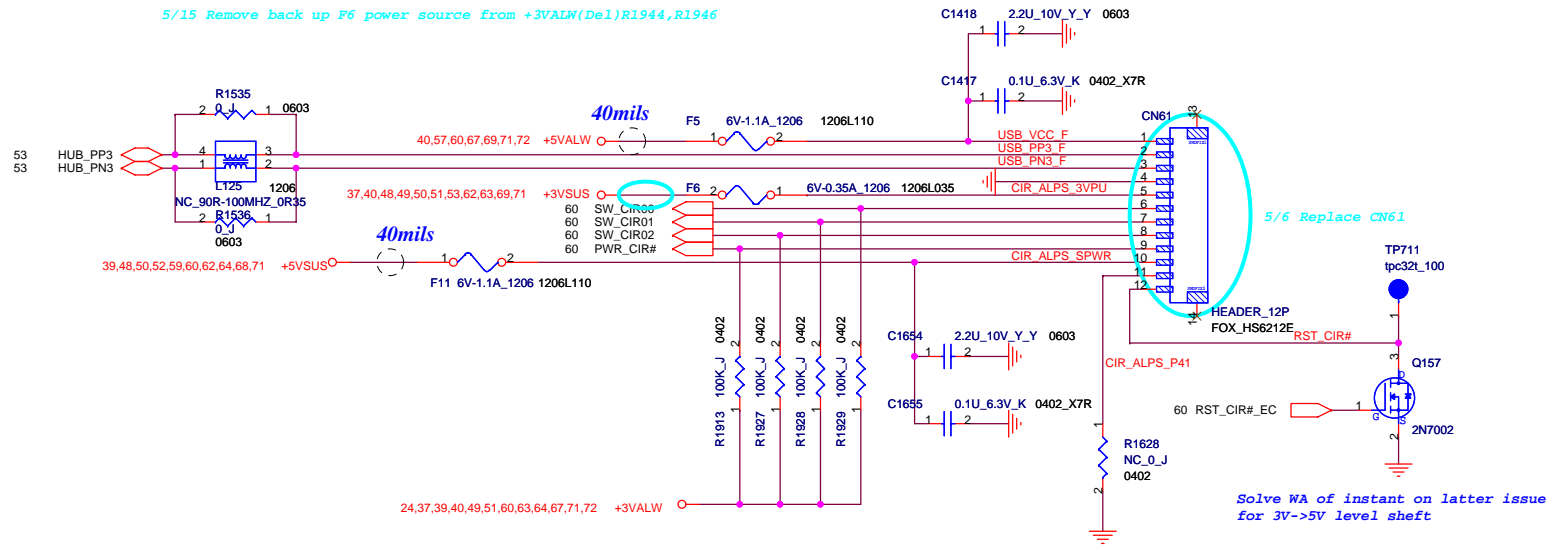
USB 1.1 HUB



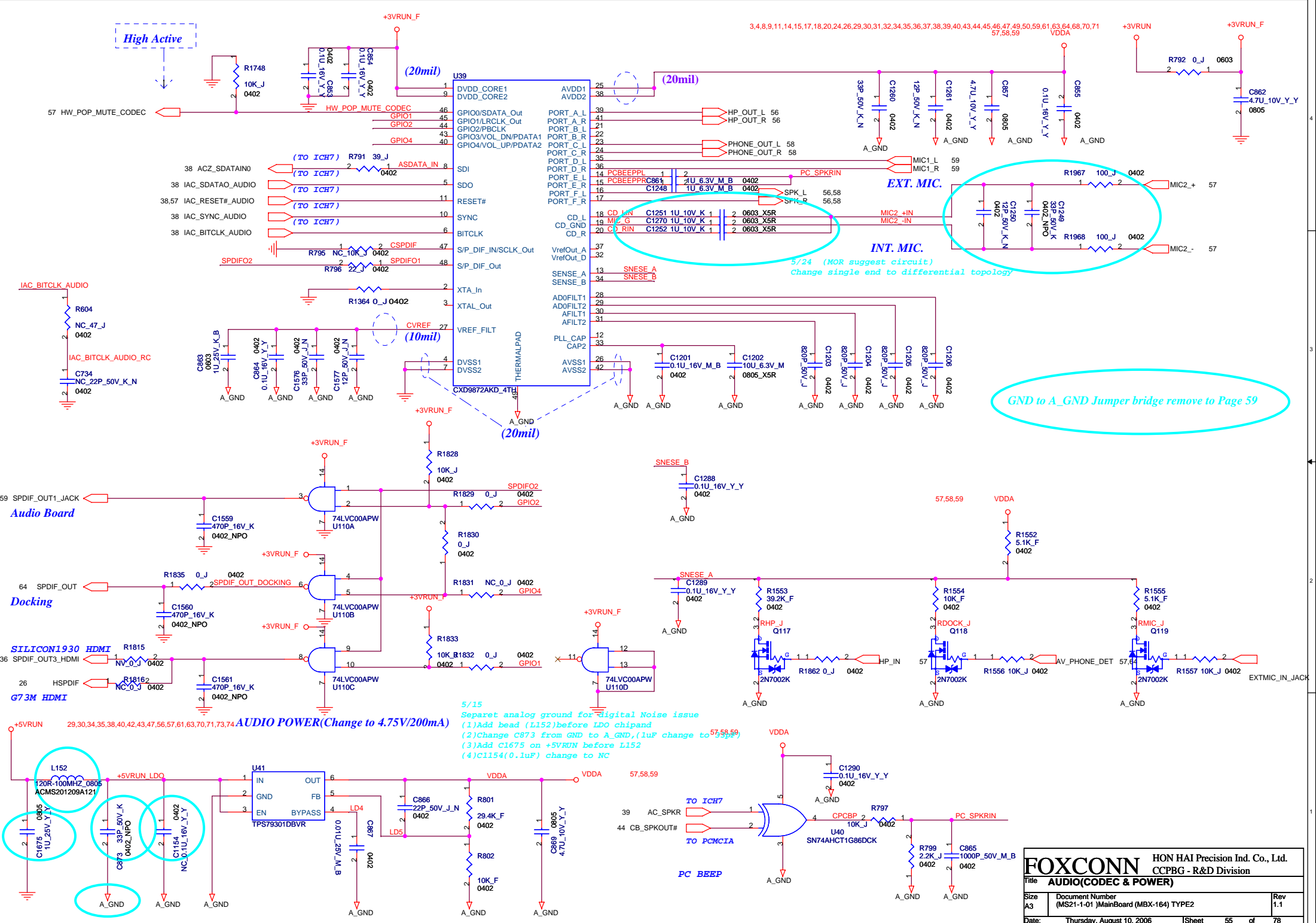
Port 0 Oide
Port 1 Bluetooth
Port 2 CIR

Hi : EEPROM disable
Low : EEPROM enable

IR Receiver connector



USB_VCC_F	1	TP847
USB_PP3_F	1	tpc321_100
USB_PP3_F	1	TP848
USB_PP3_F	1	tpc321_100
USB_PN3_F	1	TP849
USB_PN3_F	1	tpc321_100
CIR_ALPS_3VPU	1	TP850
CIR_ALPS_3VPU	1	tpc321_100
SW_CIR00	1	TP851
SW_CIR00	1	tpc321_100
SW_CIR01	1	TP852
SW_CIR01	1	tpc321_100
SW_CIR02	1	TP853
SW_CIR02	1	tpc321_100
PWR_CIR#	1	TP854
PWR_CIR#	1	tpc321_100
CIR_ALPS_SPWR	1	TP855
CIR_ALPS_SPWR	1	tpc321_100
CIR_ALPS_SPWR	1	TP856
CIR_ALPS_SPWR	1	tpc321_100



High Active

(20mil)

(20mil)

GND to A_GND Jumper bridge remove to Page 59

57 HW_POP_MUTE_CODEC

HW POP MUTE CODEC
GPIO1
GPIO2
GPIO4

38 ACZ_SDATAIN0
38 IAC_SDATAO_AUDIO
38.57 IAC_RESET#_AUDIO
38 IAC_SYNC_AUDIO
38 IAC_BITCLK_AUDIO

IAC_BITCLK_AUDIO
IAC_BITCLK_AUDIO_RC

59 SPDIF_OUT1_JACK
Audio Board

64 SPDIF_OUT
Docking

SILICON1930 HDMI
G73M HDMI

+5VRUN AUDIO POWER(Change to 4.75V/200mA)

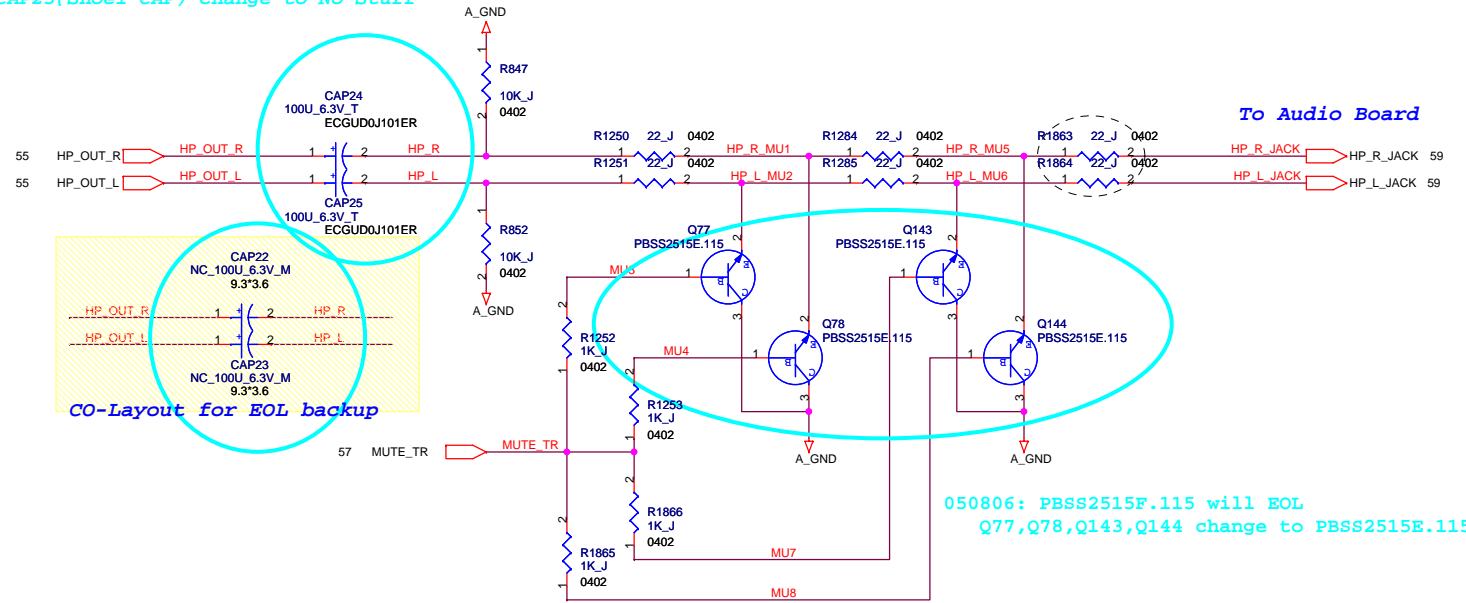
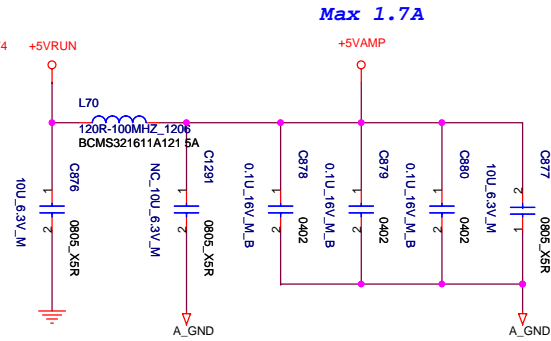
5/15 Separate analog ground for digital noise issue
(1) Add bead (L152) before LDO chipand
(2) Change C873 from GND to A_GND, (1uF change to 57.58.59)
(3) Add C1675 on +5VRUN before L152
(4) C1154(0.1uF) change to NC

SNESE_B
C1288
0.1U_16V_Y_Y
0402

SNESE_A
C1289
0.1U_16V_Y_Y
0402

PC BEEP
TO ICH7
TO PCMCIA

050806: Shoei CAP will EOL
 CAP24,CAP25(SP CAP) change to Stuff
 CAP22,CAP23(Shoei CAP) change to No Stuff

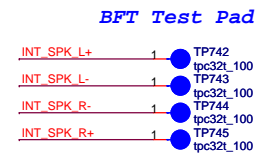
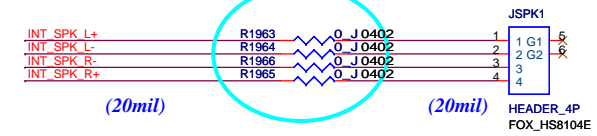
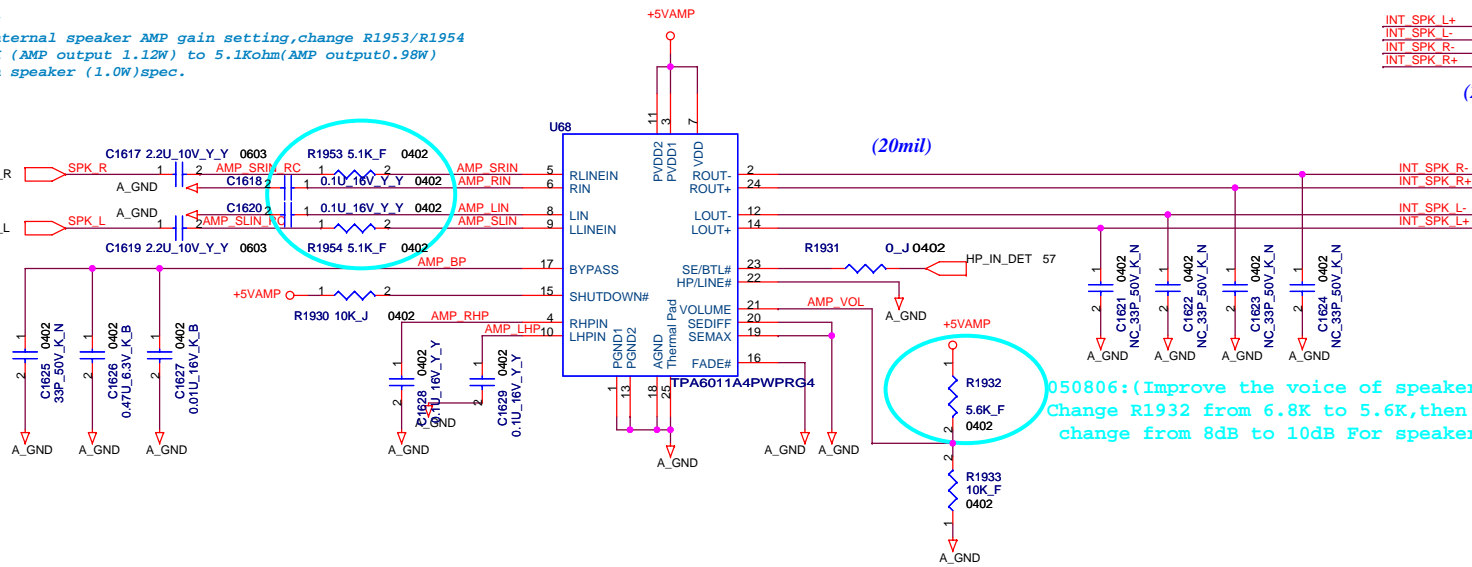


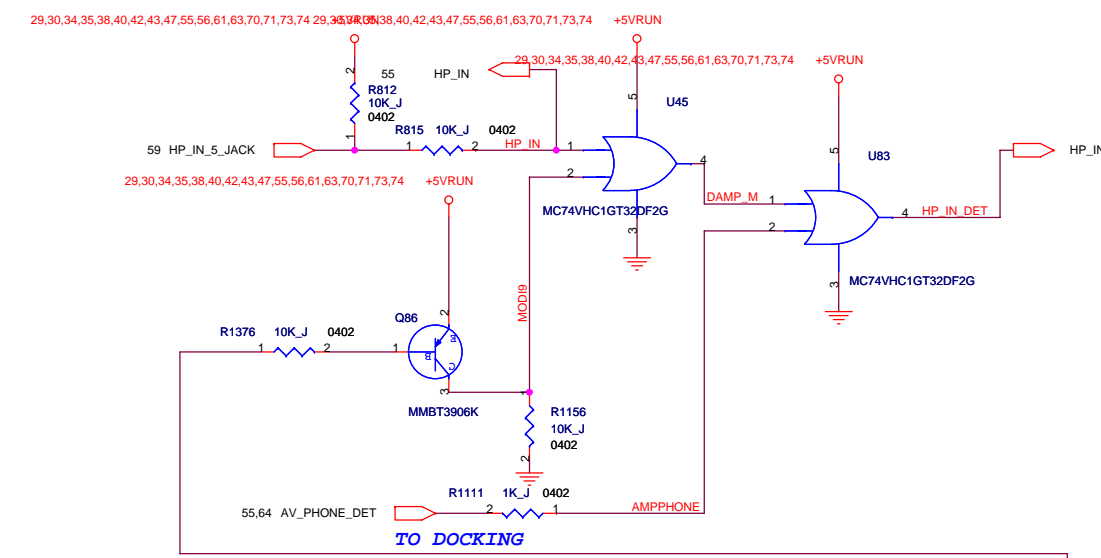
INTERNAL SPEAKER

050806:(Improve the voice of speaker up to 0.94W).
 Add damping Resistors R1953 on AMP_SRIN,R1954 on AMP_SLIN
 then speaker amp output won't be distorted.
 For speaker loudness issue.

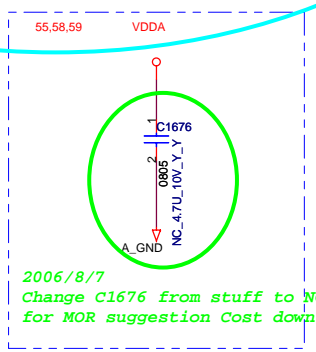
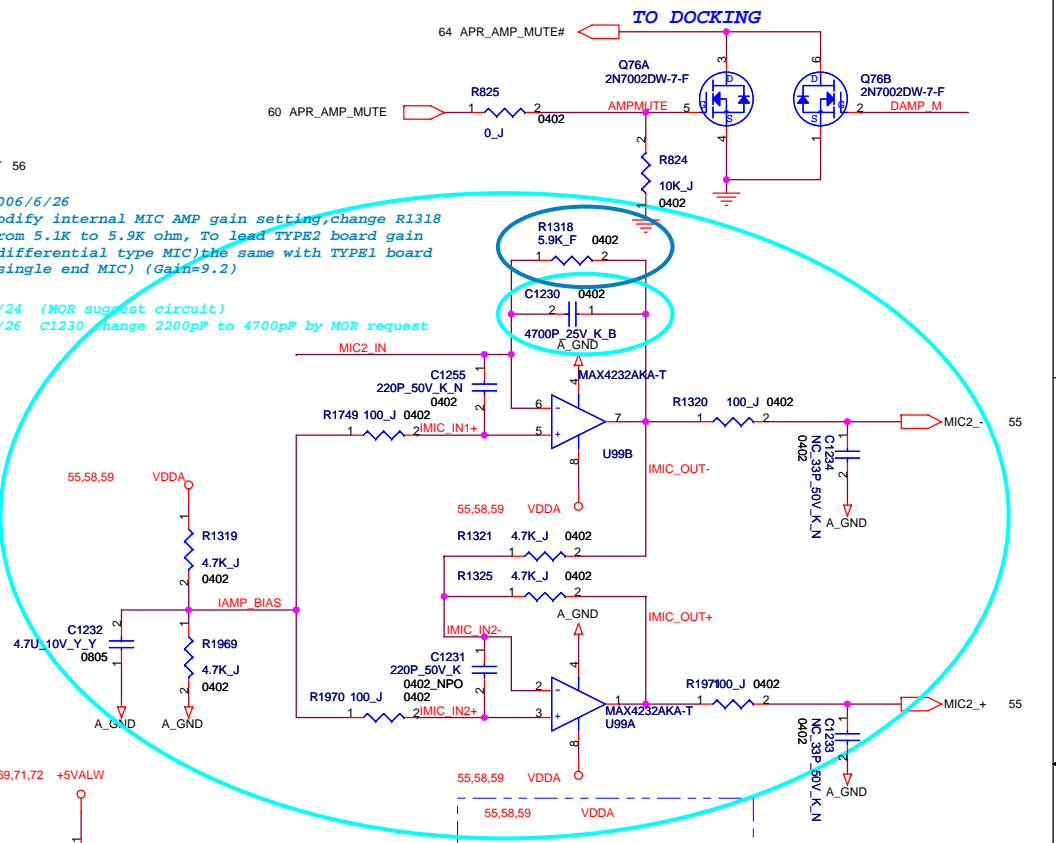
050806:(Improve the voice of speaker up to 0.94W).
 EMI team confirm whether
 it is ok to use 0ohm resistor replacing bead

2006/6/26
 Modify internal speaker AMP gain setting,change R1953/R1954
 from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98W)
 to fit in speaker (1.0W)spec.

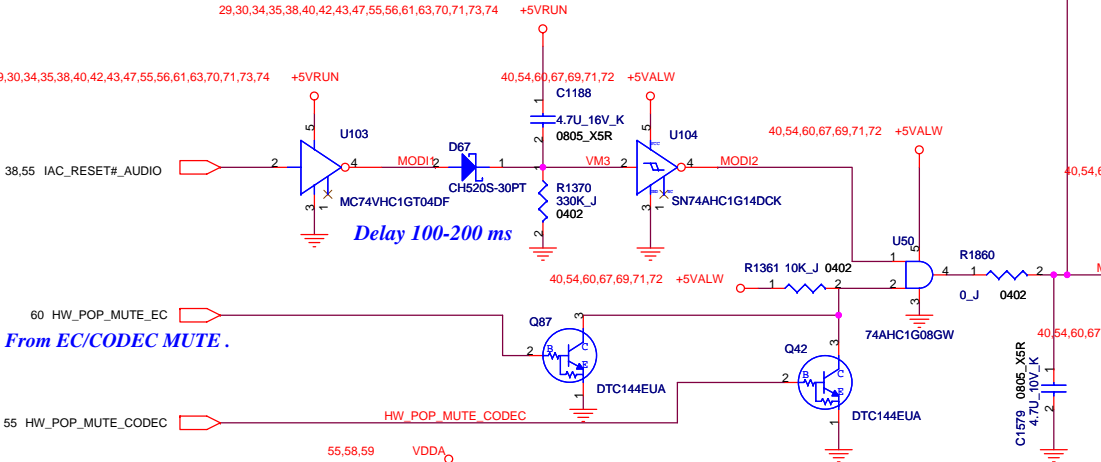




2006/6/26
 Modify internal MIC AMP gain setting, change R1318 from 5.1K to 5.9K ohm, To lead TYPE2 board gain (differential type MIC) the same with TYPE1 board (single end MIC) (Gain=9.2)
 5/24 (MOR suggest circuit)
 5/26 C1230 change 2200pF to 4700pF by MOR request



2006/8/7
 Change C1676 from stuff to NC for MOR suggestion Cost down request.

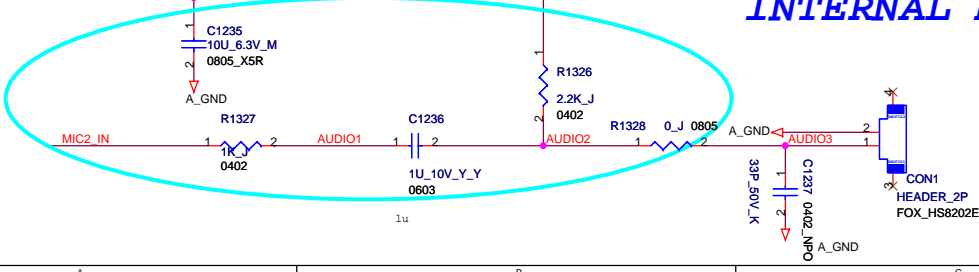


Delay 100-200 ms

From EC/CODEC MUTE.

5/24 (MOR suggest circuit)
 C1237 change from 100pF to 33pF (GPRS noise)
 R1326 change from 7.5Kohm to 2.2K (Mic datasheet suggest)
 R1327 change from 100ohm to 1K
 R1236 change from 4.7u to 1u

INTERNAL MIC(Non)

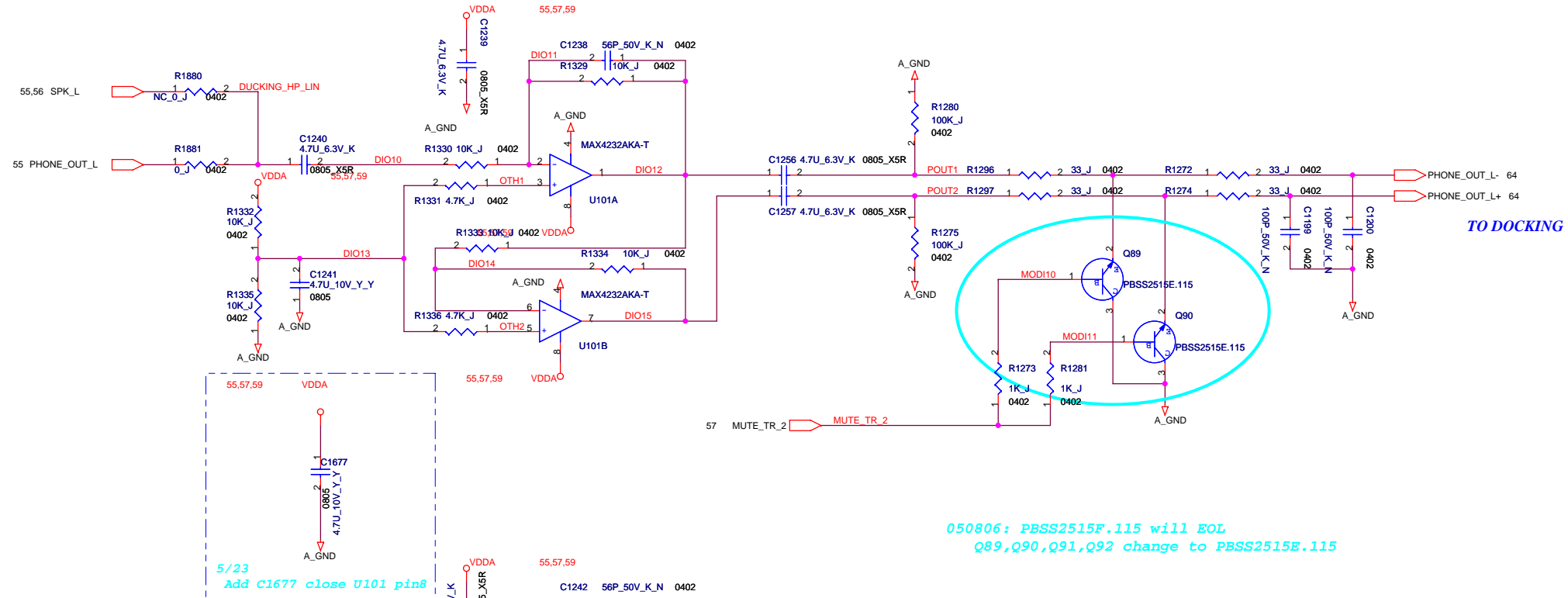


BFT Test Pad



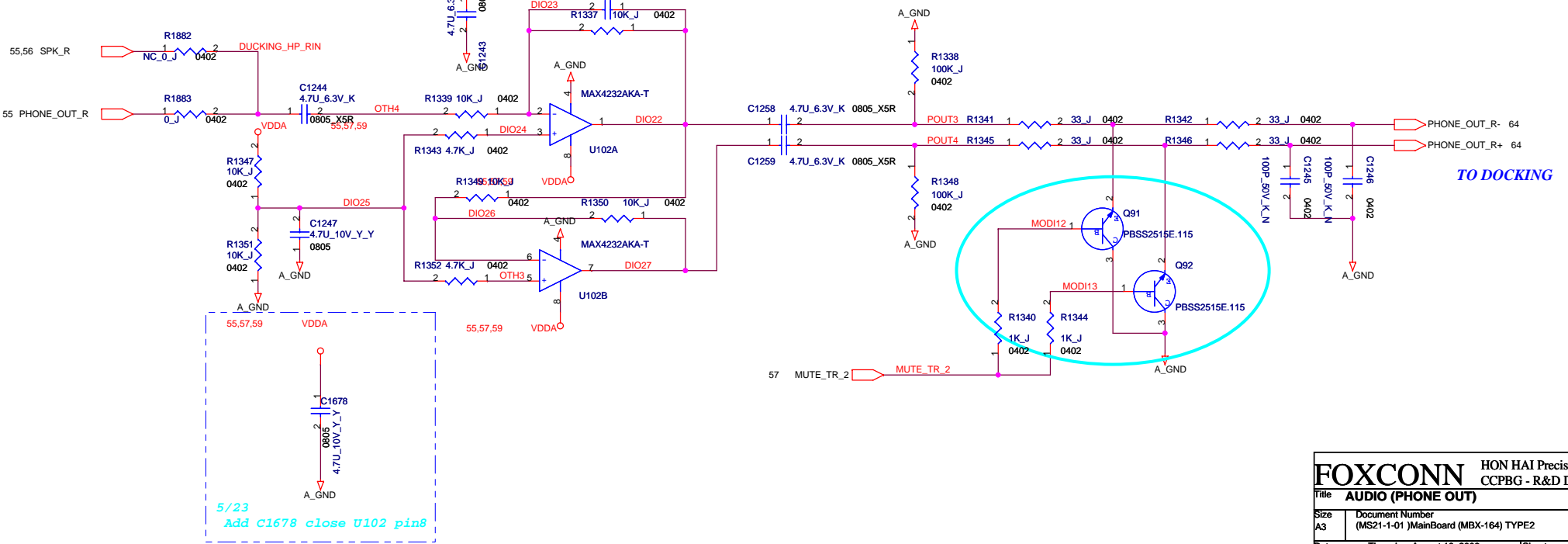
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title AUDIO (MUTE & INTMIC)		
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
Date: Thursday, August 10, 2006	Sheet 57	of 78

PHONE OUT



5/23
Add C1677 close U101 pin8

050806: PBSS2515F.115 will EOL
Q89,Q90,Q91,Q92 change to PBSS2515E.115

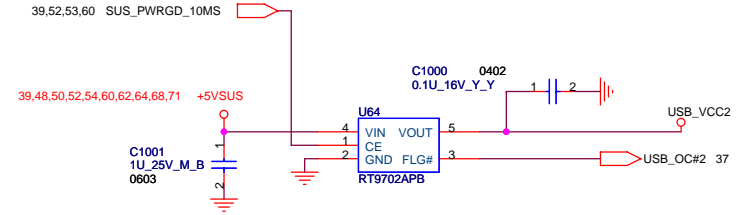
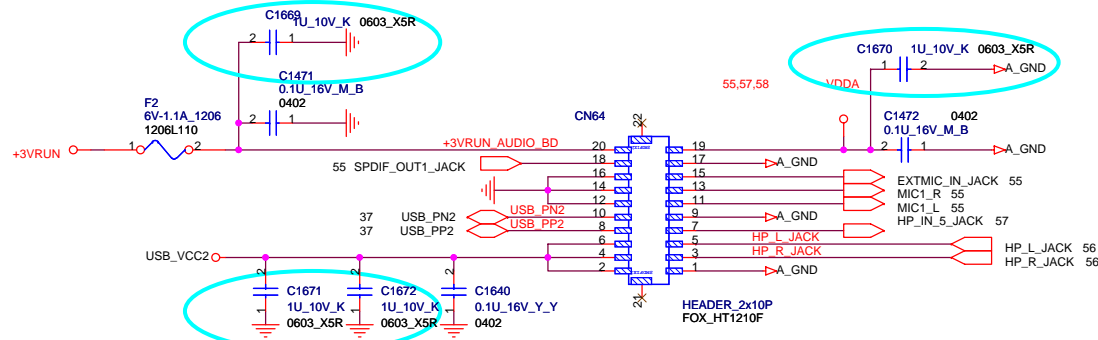


5/23
Add C1678 close U102 pin8

Audio Board connector

050806: (To improve SNR issue)

Add 1uF capacitors close CN64 :C1671,C1672 on USB_VCC2,
C1669 on +3VRUN_AUDIO_BD, and C1670 on VDDA .



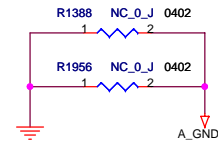
5/6

Separate analog ground for digital Noise issue:

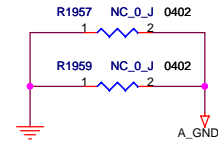
- (1) Remove GP3 (Close Jumper) not bridge between GND and A_GND
- (2) Backup two jumper resistors for bridge between GND and A_GND (C1388, C1966 on Screw hole H3, C1957, C1959 on screw hole H5)
- (3) Isolate screw hole H4, add 100pF capacitors C1673, C1674 for EMI, Zener diode D100 for ESD
- (4) Add jumper resistor for Return patch R1955 close L70 (+5VAMP) & R1958 close U41 (+5VRUN) & R1960 close codec.

Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

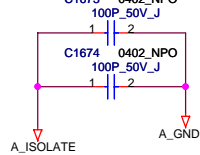


Close screw hole H5

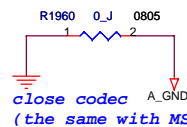
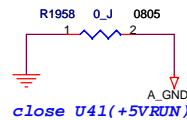


Isolate screw hole H4, and add EMI/ESD solution

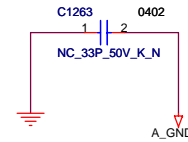
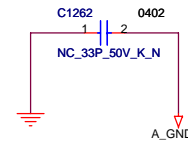
EMI



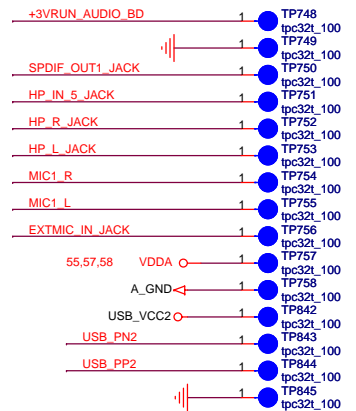
Add jumper resistor for Return patch

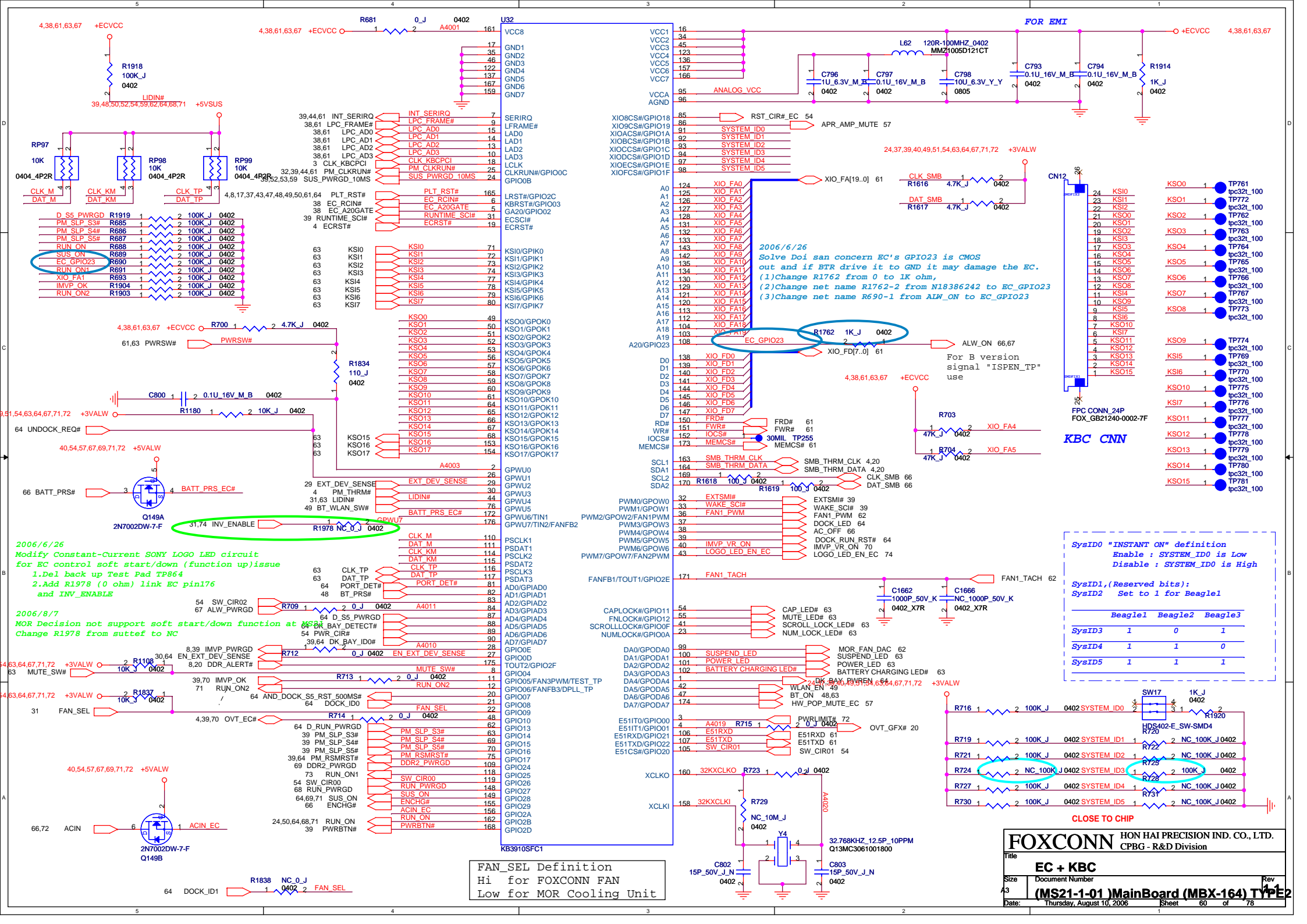


Original EMI back up solution to continue with MS20 (bridge between GND and A_GND)



BFT Test Pad





- | | | | | | | | | | | |
|---|---|---|------------|-------|-------|---|------|------|------|------|
| D | S | D | SS | PWRGD | R1919 | 1 | 2 | 100K | J | 0402 |
| | | | PM_SLP_S3# | R685 | 1 | 2 | 100K | J | 0402 | |
| | | | PM_SLP_S4# | R686 | 1 | 2 | 100K | J | 0402 | |
| | | | PM_SLP_S5# | R687 | 1 | 2 | 100K | J | 0402 | |
| | | | RUN_ON | R688 | 1 | 2 | 100K | J | 0402 | |
| | | | SUS_ON | R689 | 1 | 2 | 100K | J | 0402 | |
| | | | EC_GPIO23 | R690 | 1 | 2 | 100K | J | 0402 | |
| | | | RUN_ON1 | R691 | 1 | 2 | 100K | J | 0402 | |
| | | | XIO_FAT1 | R693 | 1 | 2 | 100K | J | 0402 | |
| | | | IMVP_OK | R1904 | 1 | 2 | 100K | J | 0402 | |
| | | | RUN_ON2 | R1903 | 1 | 2 | 100K | J | 0402 | |

2006/6/26
 Modify Constant-Current SONY LOGO LED circuit for EC control soft start/down (function up/issue)
 1.Del back up Test Pad TP864
 2.Add R1978 (0 ohm) link EC pin176 and INV_ENABLE

2006/8/7
 MOR Decision not support soft start/down function at BAY DETECT#
 Change R1978 from suttef to NC

2006/6/26
 Solve Doi sun concern EC's GPIO23 is CMOS out and if BTR drive it to GND it may damage the EC.
 (1)Change R1762 from 0 to 10 ohm
 (2)Change net name R1762-2 from N18386242 to EC_GPIO23
 (3)Change net name R690-1 from ALW_ON to EC_GPIO23

FAN_SEL Definition
 Hi for FOXCONN FAN
 Low for MOR Cooling Unit

SysID0 "INSTANT ON" definition
 Enable : SYSTEM_ID0 is Low
 Disable : SYSTEM_ID0 is High

SysID1,(Reserved bits):
 SysID2 Set to 1 for Beagle1

	Beagle1	Beagle2	Beagle3
SysID3	1	0	1
SysID4	1	1	0
SysID5	1	1	1

FOXCONN HON HAI PRECISION IND. CO., LTD.
 CPBG - R&D Division

Title: **EC + KBC**

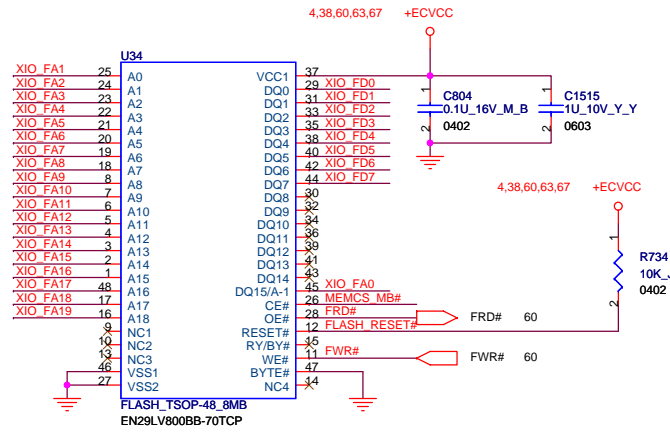
Size: **(MS21-1-01) MainBoard (MBX-164) TYPE2**

Date: Thursday, August 10, 2006
 Sheet: 60 of 78

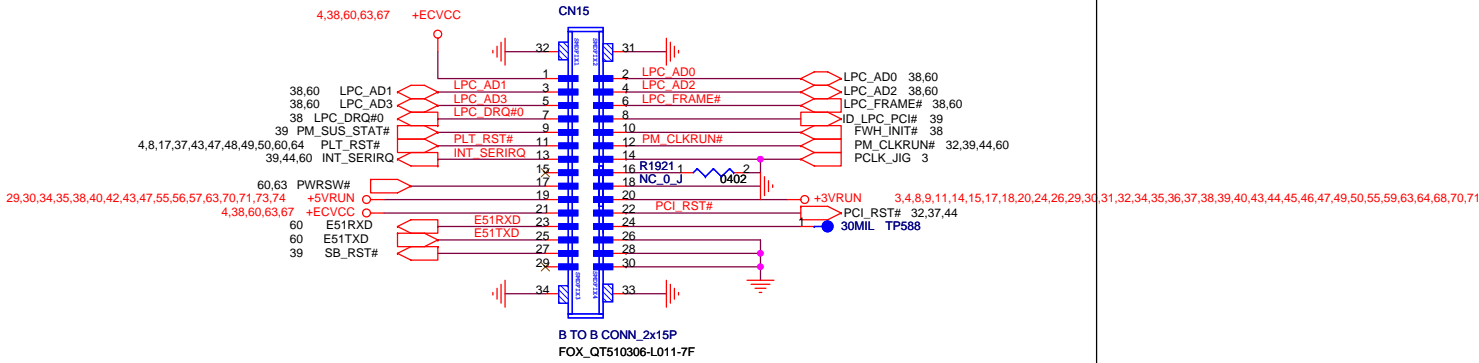
FAN_SEL Definition
 Hi for FOXCONN FAN
 Low for MOR Cooling Unit

FLASH BIOS

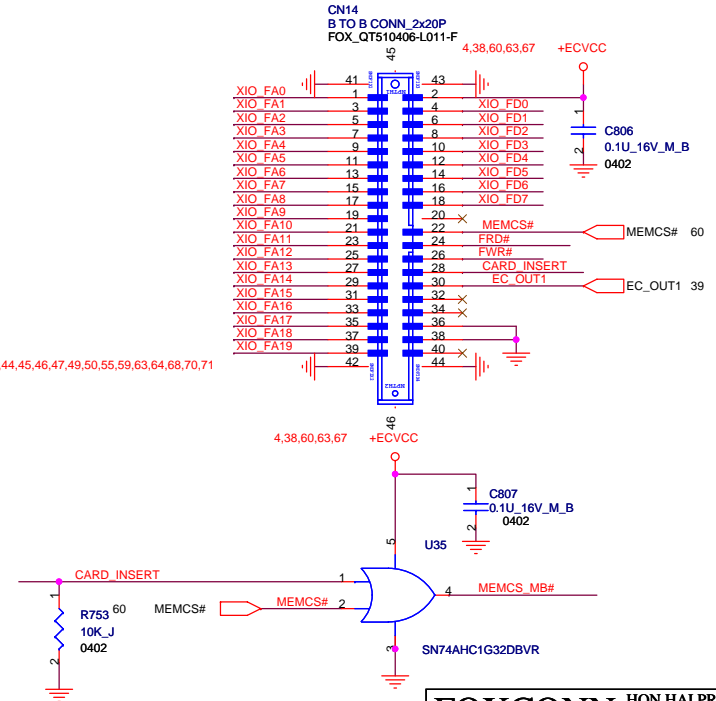
60 XIO_FA[19..0]
60 XIO_FD[7..0]



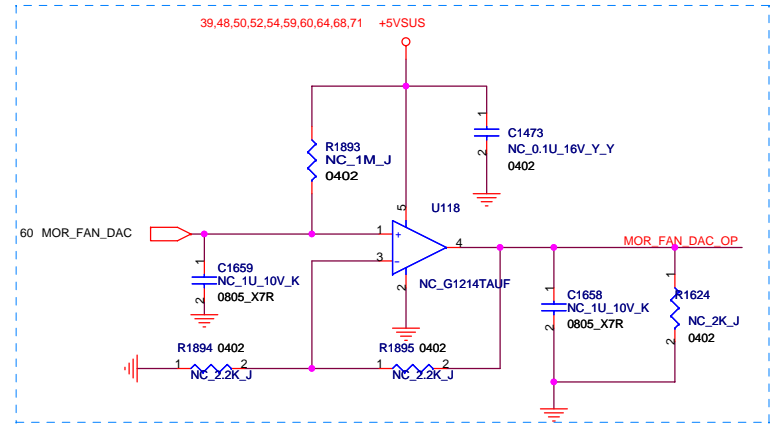
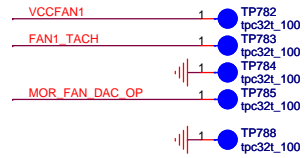
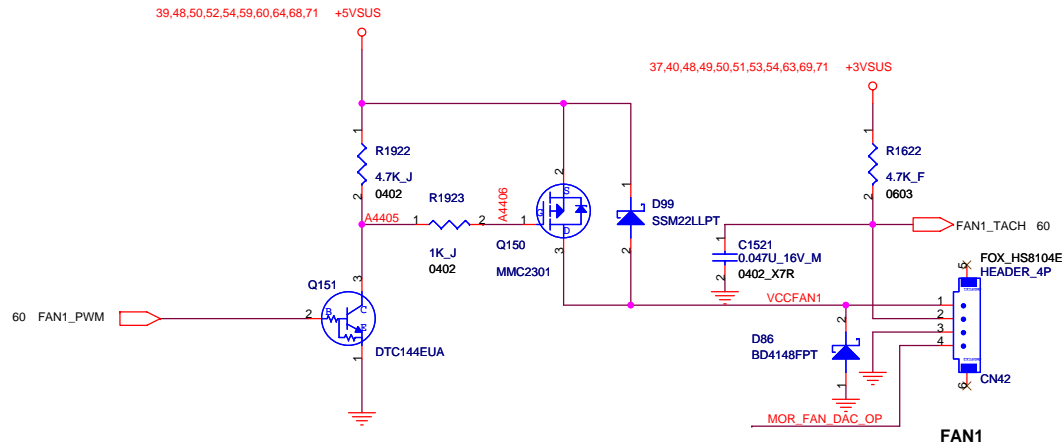
JIG-120



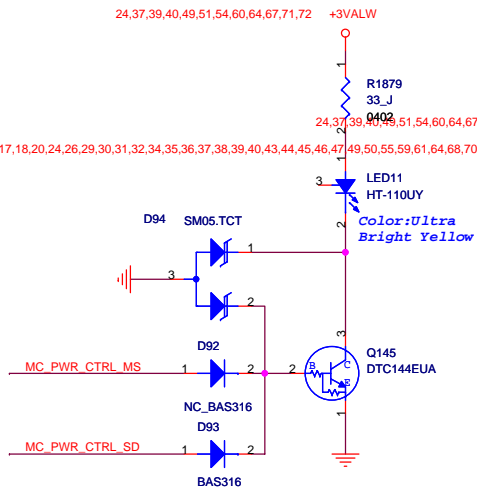
X-BUS



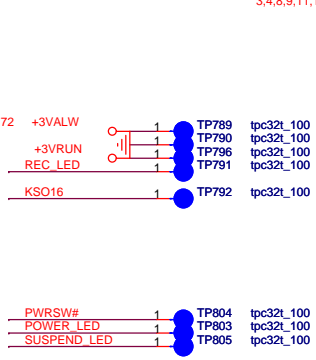
FAN(FAN1+MOR FAN)



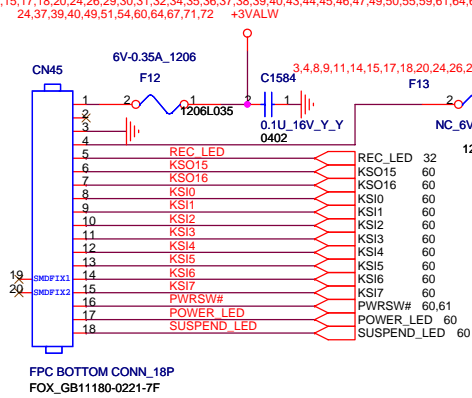
6/28 MOR fan circuit modify to backup
 (NC)U118
 (NC)R1893
 (NC)R1894
 (NC)R1895
 (NC)R1624
 (NC)C1473



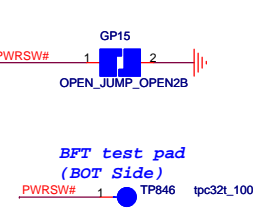
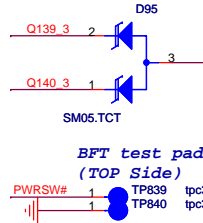
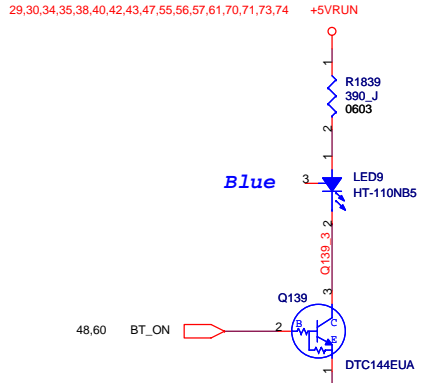
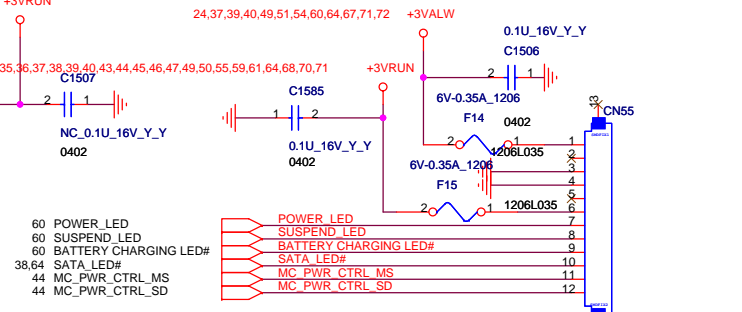
**SD LED
BLUETOOTH LED**



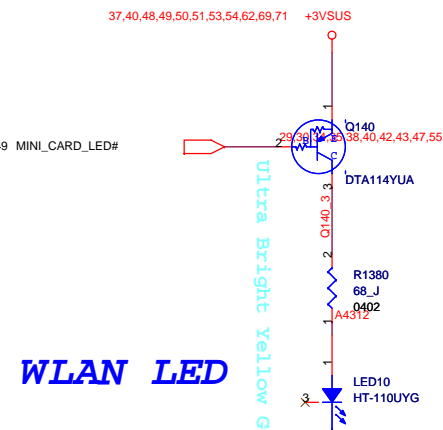
To Power Button Board Connector



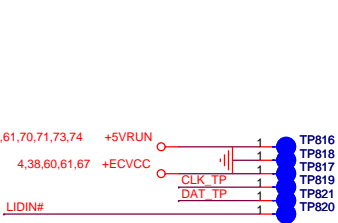
To LED Board Connector



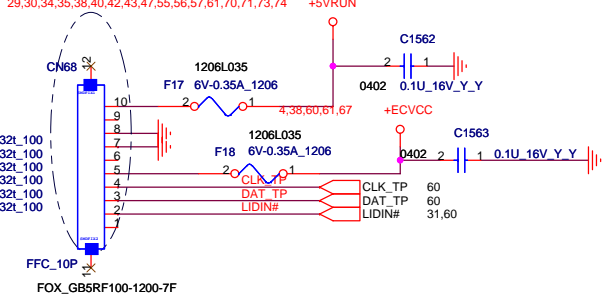
CN68 Change from MOLEX to FOXCONN By kain 0517



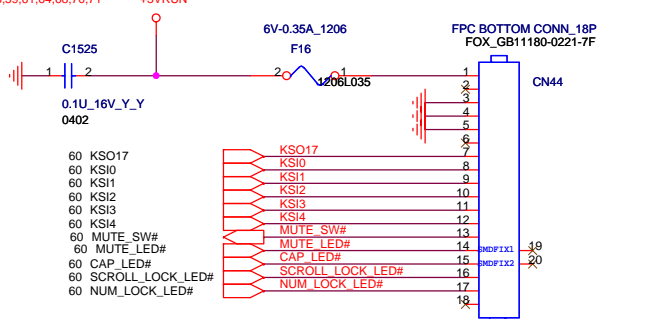
LED IF SPEC:
20mA(TYP), 30mA(MAX)



To Touch Pad Board Connector



062606: Move Logo Led Circuit module to page 74.



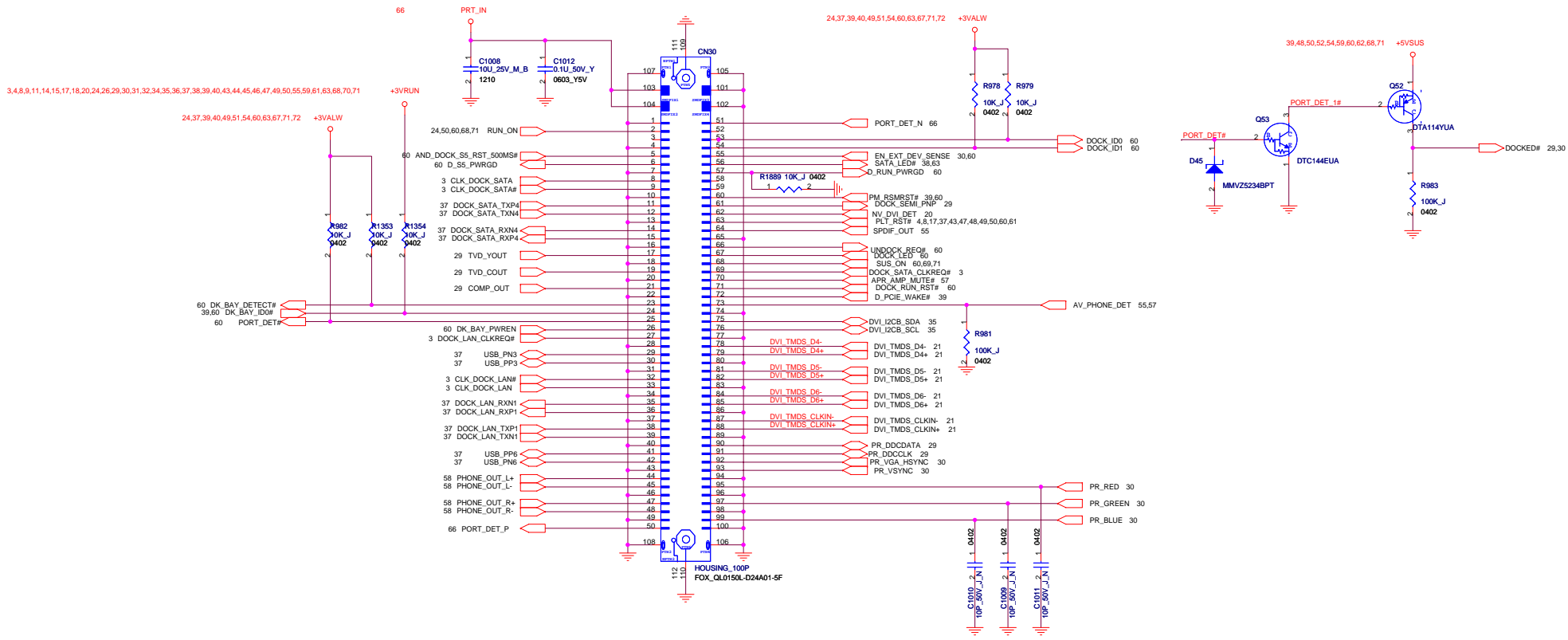
To AV Function Board Connector

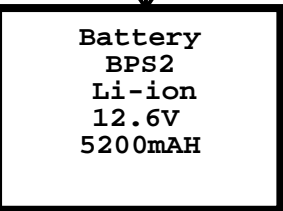
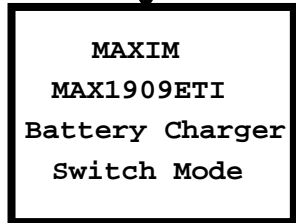
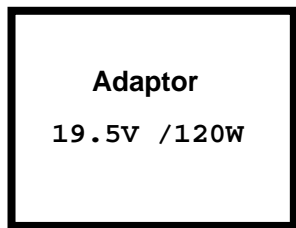
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **POWER BD + HOT KEY BD + T/P&LED BD + LOGO LED**

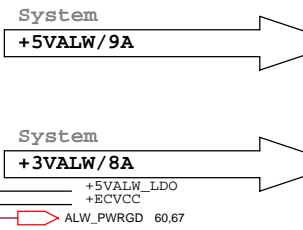
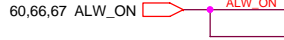
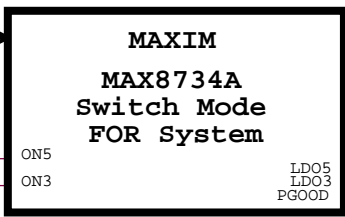
Size: Document Number
43 (MS21-1-01) MainBoard (MBX-164) TYPE 2

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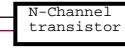




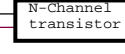
DCBATOUT



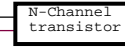
60,64,69,71 SUS_ON



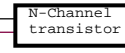
+5VSUS/3.1A



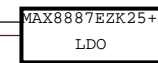
+5VRUN/4.5A



+3VSUS/1.5A

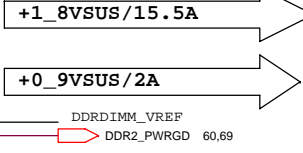
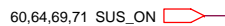
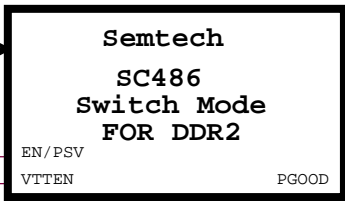


+3VRUN/7A

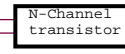


+2_5VRUN/300mA

DCBATOUT

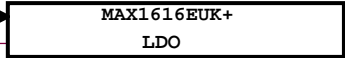
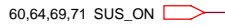
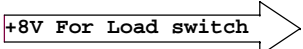
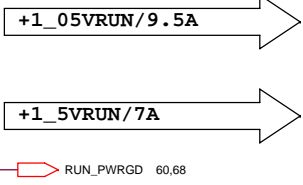
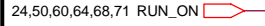
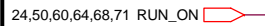
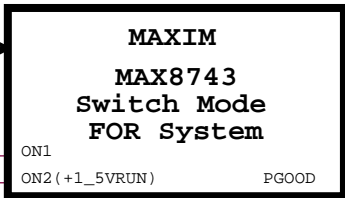


60,71 RUN_ON2

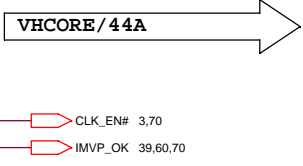
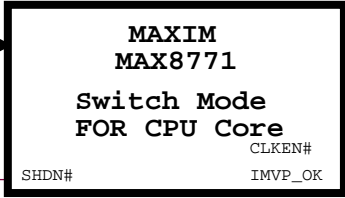


+1_8VRUN/6A

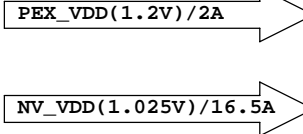
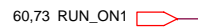
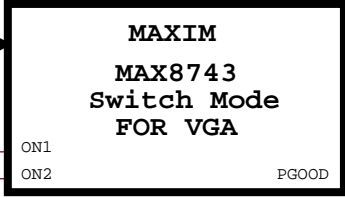
DCBATOUT

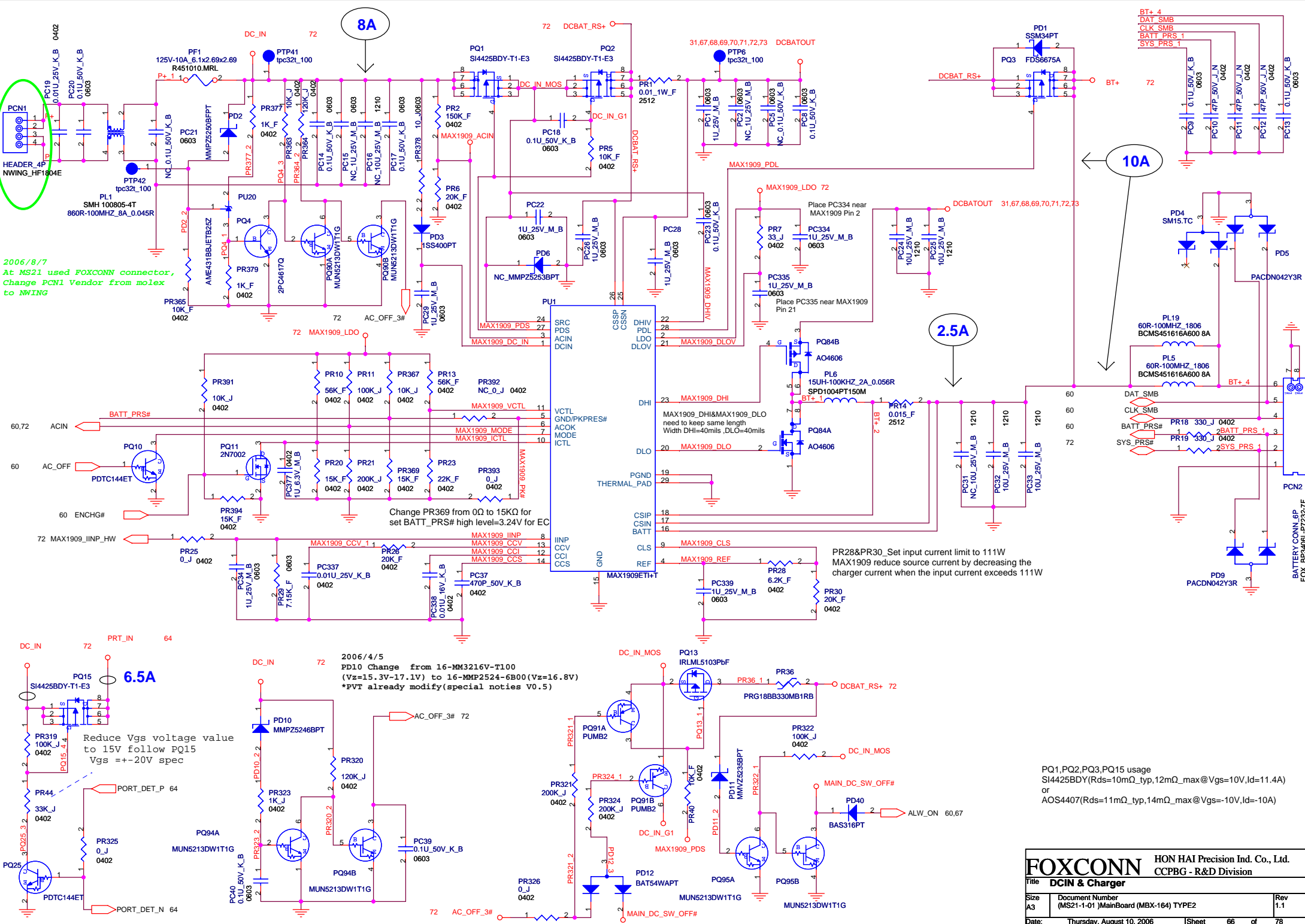


DCBATOUT



DCBATOUT





2006/8/7
 At MS21 used FOXCONN connector,
 Change PCN1 Vendor from molex
 to Nwing

2006/4/5
 PD10 Change from 16-MM3216V-T100
 (Vz=15.3V-17.1V) to 16-MMP2524-6B00 (Vz=16.8V)
 *PVT already modify (special notices V0.5)

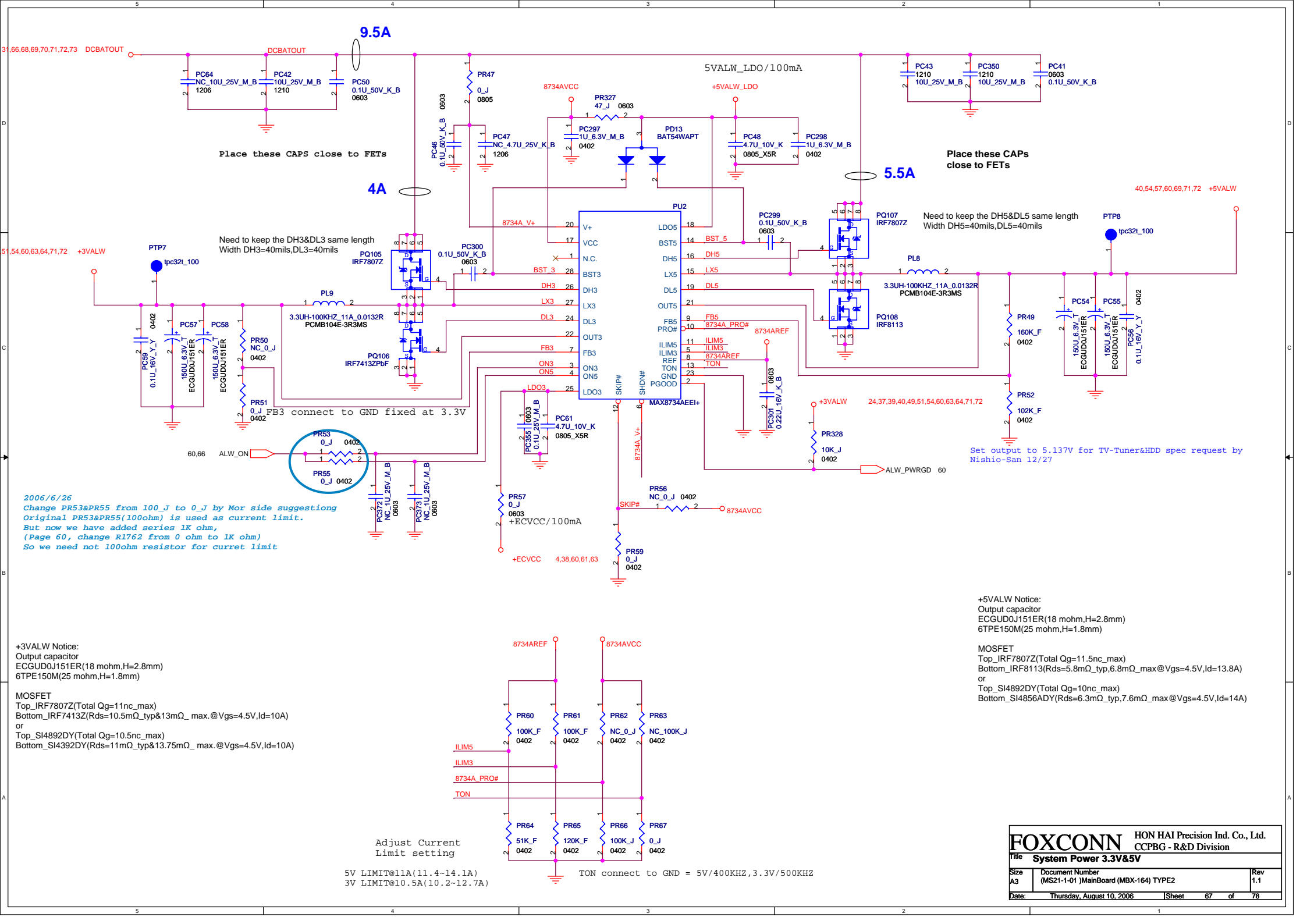
Reduce Vgs voltage value
 to 15V follow PQ15
 Vgs = +-20V spec

PR28&PR30, Set input current limit to 111W
 MAX1909 reduce source current by decreasing the
 charger current when the input current exceeds 111W

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 CCPBG - R&D Division

Title: **DCIN & Charger**

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2006/6/26
 Change PR53&PR55 from 100_J to 0_J by Mor side suggesting
 Original PR53&PR55(100ohm) is used as current limit.
 But now we have added series 1K ohm,
 (Page 60, change R1762 from 0 ohm to 1K ohm)
 So we need not 100ohm resistor for curret limit

+3VALW Notice:
 Output capacitor
 ECGUD0J151ER(18 mohm,H=2.8mm)
 6TPE150M(25 mohm,H=1.8mm)

MOSFET
 Top_IRF7807Z(Total Qg=11nc_max)
 Bottom_IRF7413Z(Rds=10.5mΩ_typ&13mΩ_max.@Vgs=4.5V,Id=10A)
 or
 Top_SI4892DY(Total Qg=10.5nc_max)
 Bottom_SI4392DY(Rds=11mΩ_typ&13.75mΩ_max.@Vgs=4.5V,Id=10A)

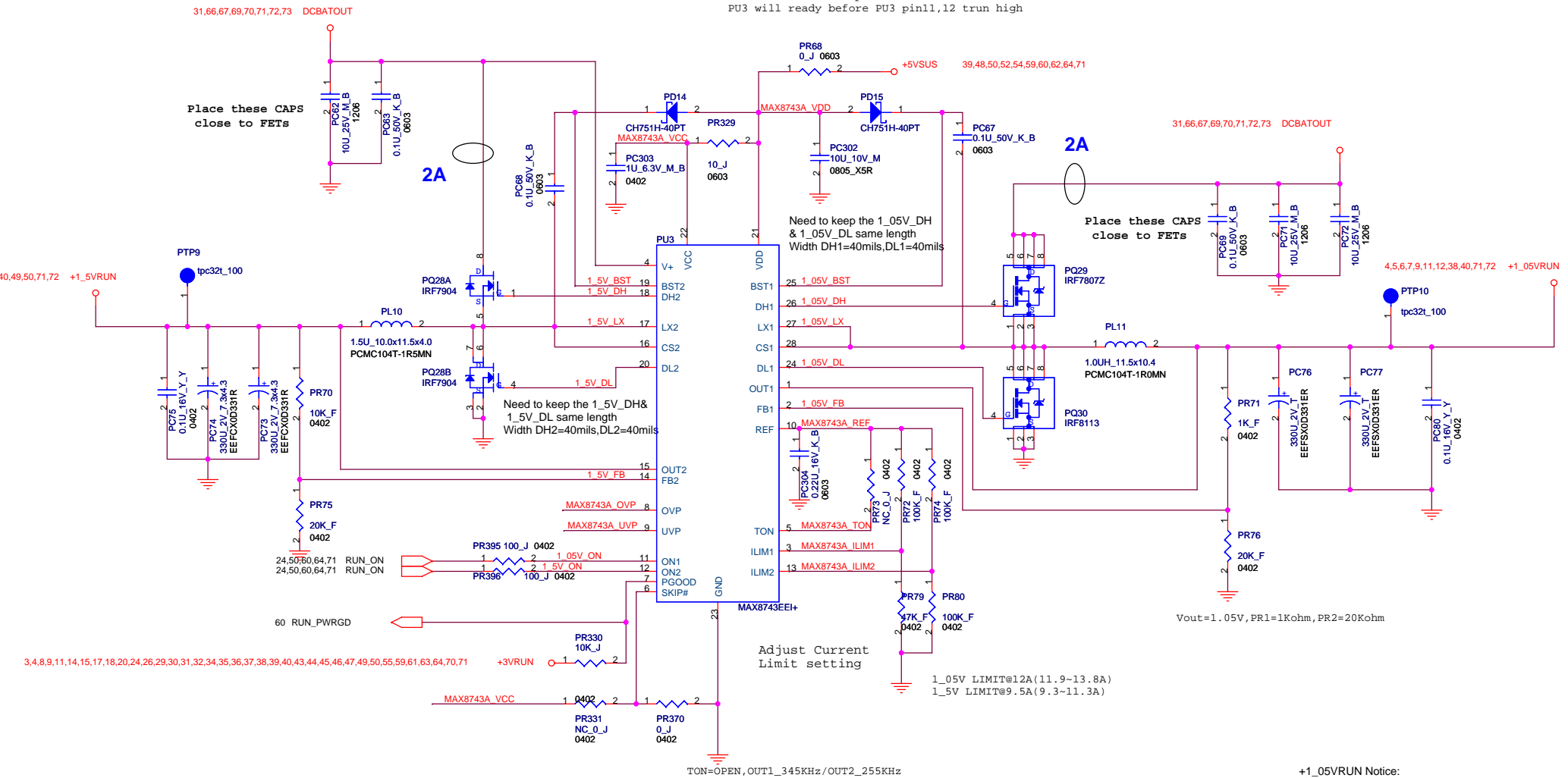
Adjust Current
 Limit setting
 5V LIMIT@11A(11.4~14.1A)
 3V LIMIT@10.5A(10.2~12.7A)

+5VALW Notice:
 Output capacitor
 ECGUD0J151ER(18 mohm,H=2.8mm)
 6TPE150M(25 mohm,H=1.8mm)

MOSFET
 Top_IRF7807Z(Total Qg=11.5nc_max)
 Bottom_IRF8113(Rds=5.8mΩ_typ,6.8mΩ_max@Vgs=4.5V,Id=13.8A)
 or
 Top_SI4892DY(Total Qg=10nc_max)
 Bottom_SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title System Power 3.3V&5V			
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1	
Date: Thursday, August 10, 2006	Sheet 67	of 78	

Use +5VSUS for PU3 pin21 to ensure
PU3 will ready before PU3 pin11,12 trun high

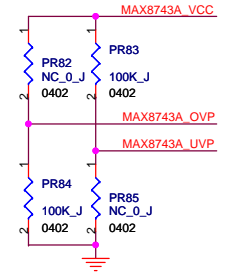


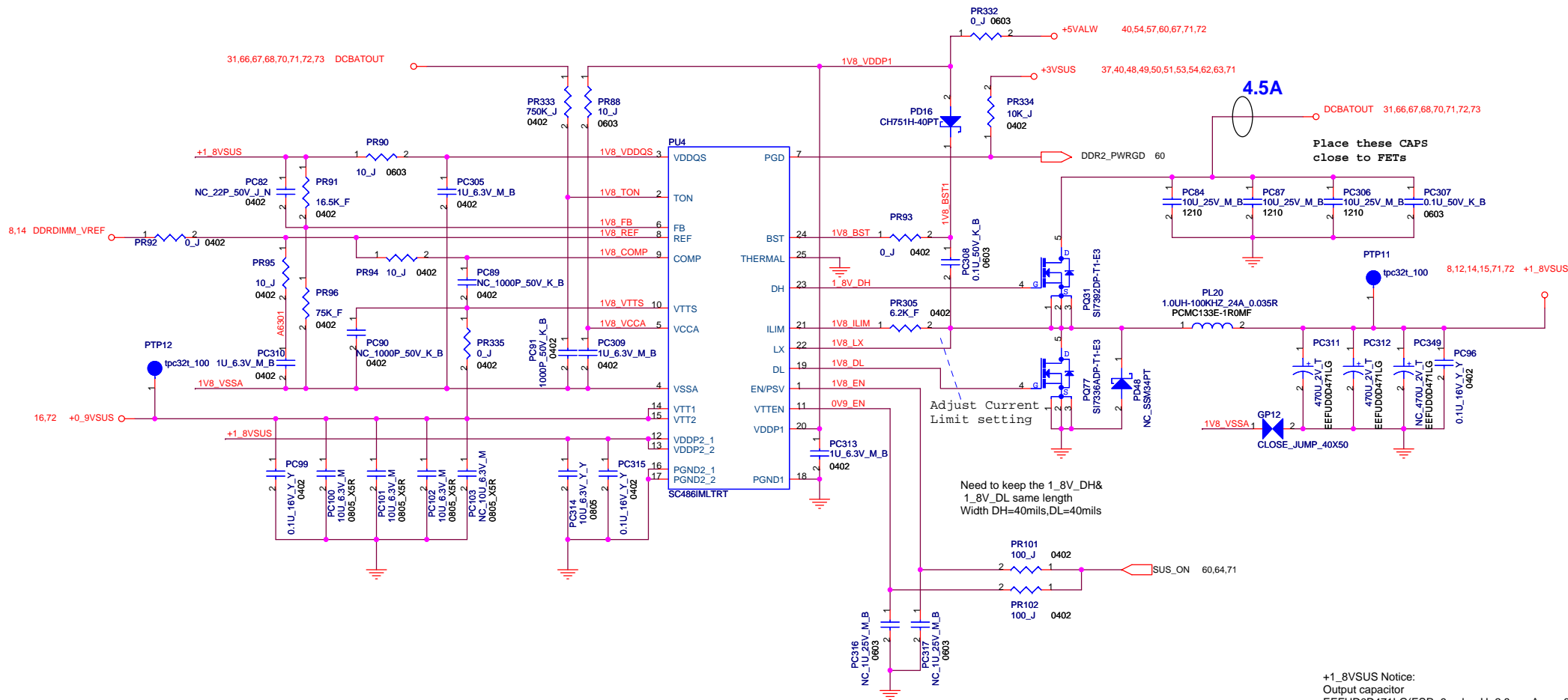
+1_5VRUN Notice:
Output capacitor
EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1A)

MOSFET(Top+Bottom)
IRF7904(Low side Rds=10.5mΩ_typ,13mΩ_max@Vgs=4.5V,Id=8.9A)

+1_05VRUN Notice:
Output capacitor usage
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_IRF7807Z(Total Qg=11.5nc_max)
Bottom_IRF8113(Rds=5.8mΩ_typ,6.8mΩ_max@Vgs=4.5V,Id=13.8A)
or
Top_SI4892DY(Total Qg=10nc_max)
Bottom_SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)





Place these CAPS close to FETs

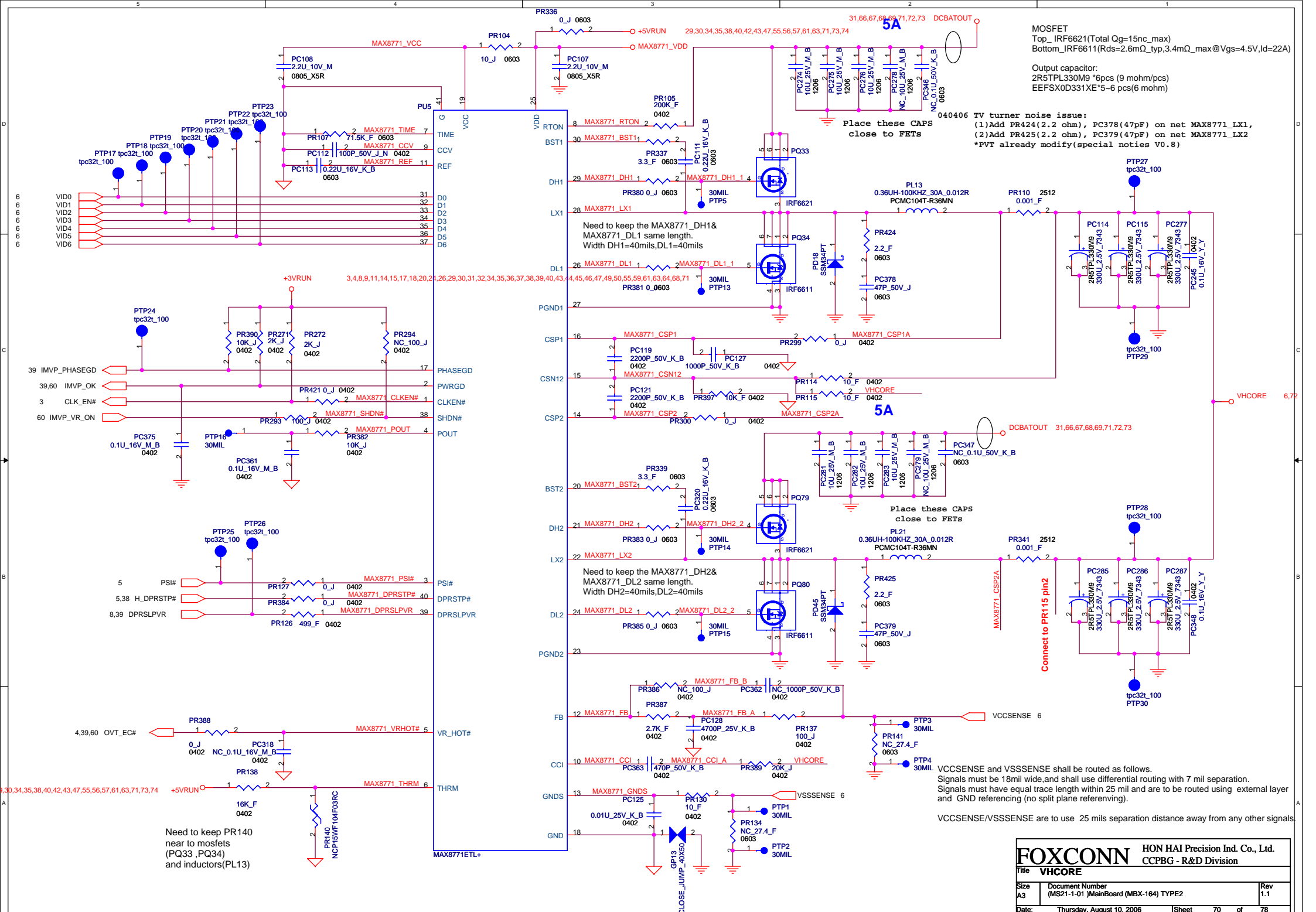
Adjust Current Limit setting

Need to keep the 1.8V_DH & 1.8V_DL same length
Width DH=40mils, DL=40mils

+1.8VSUS Notice:
Output capacitor
EEFUD0D471LG(ESR=9mohm,H=2.8mm,Arms=3.4A)
2R5TPE470M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_Si7392DP(Total Qg=15nc_max)
Bottom_Si7336ADP(Rds=3.1mΩ_typ,4.0mΩ_max@19A)
or
Top_NTMFS4707N(Total Qg=15nc_max)
Bottom_NTMFS4119N(Rds=3.1mΩ_typ,4.8mΩ_max@25A)

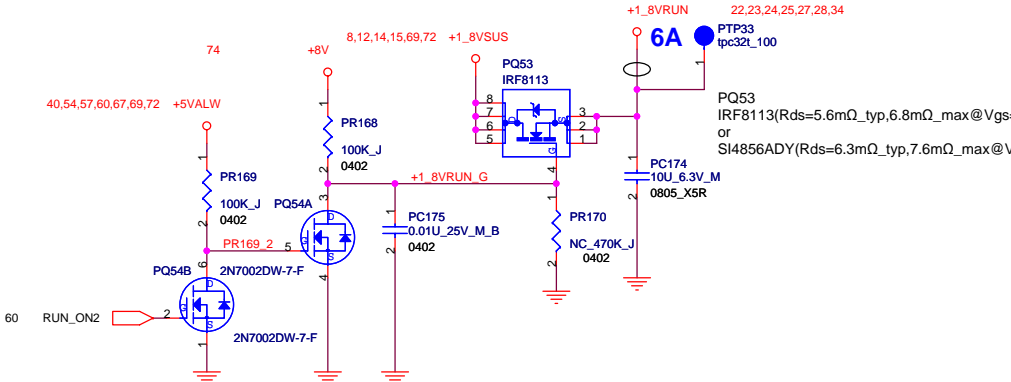
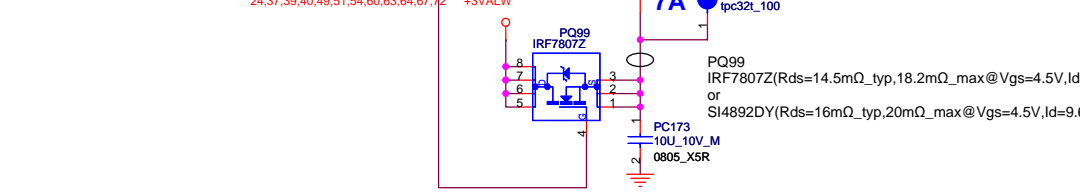
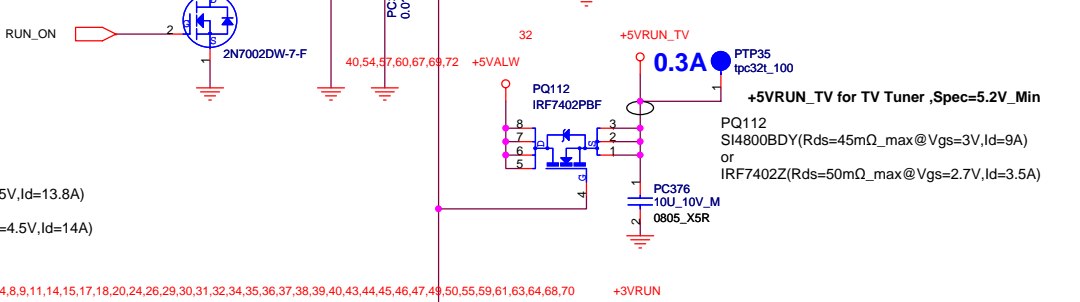
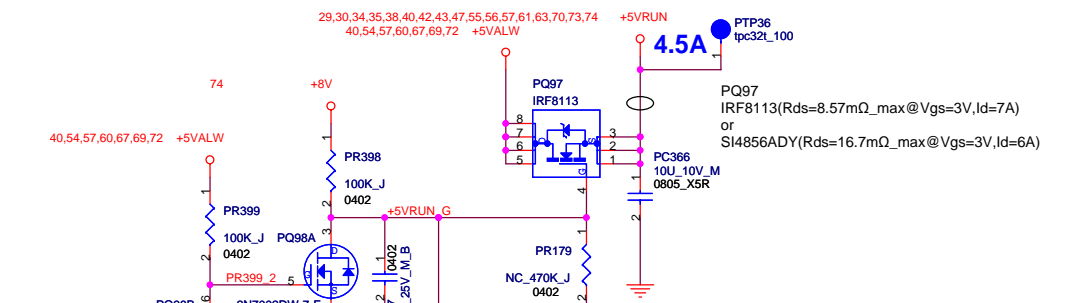
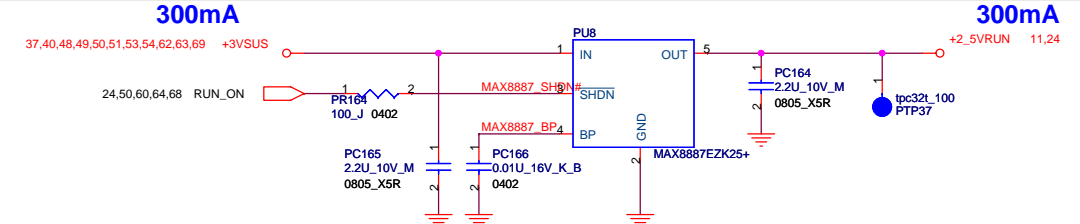
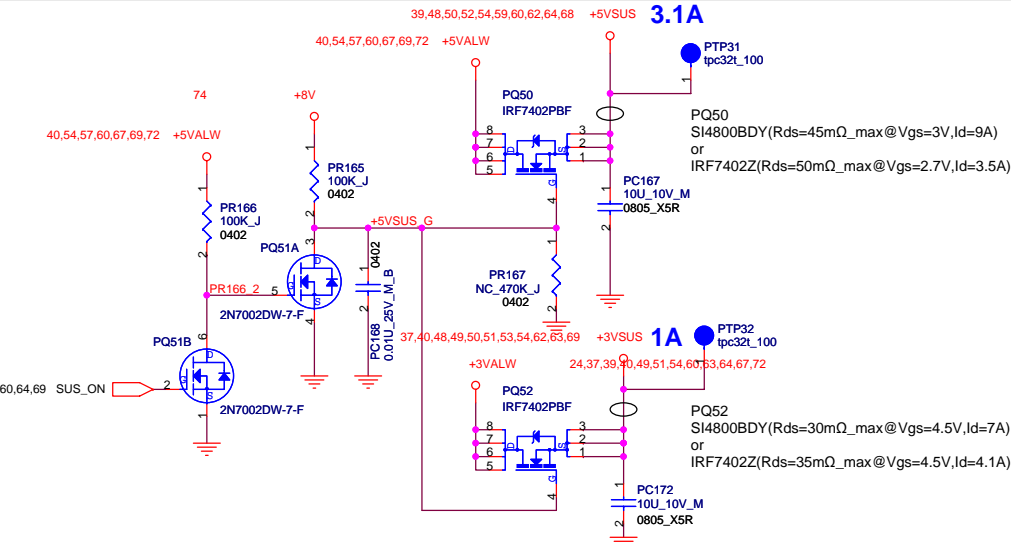
1.8V LIMIT@20A(19.2-24A)



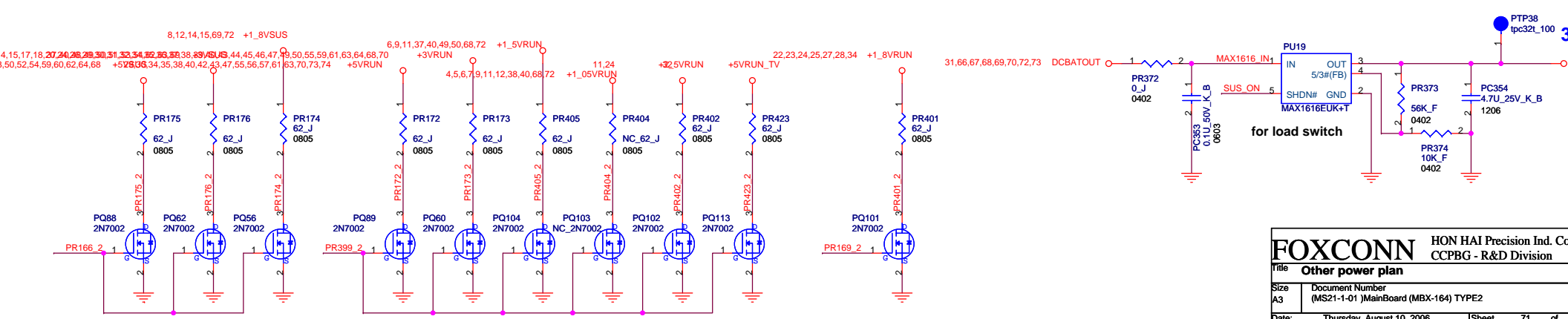
MOSFET
 Top_ IRF6621 (Total Qg=15nc_max)
 Bottom_ IRF6611 (Rds=2.6mΩ typ, 3.4mΩ_max @ Vgs=4.5V, Id=22A)

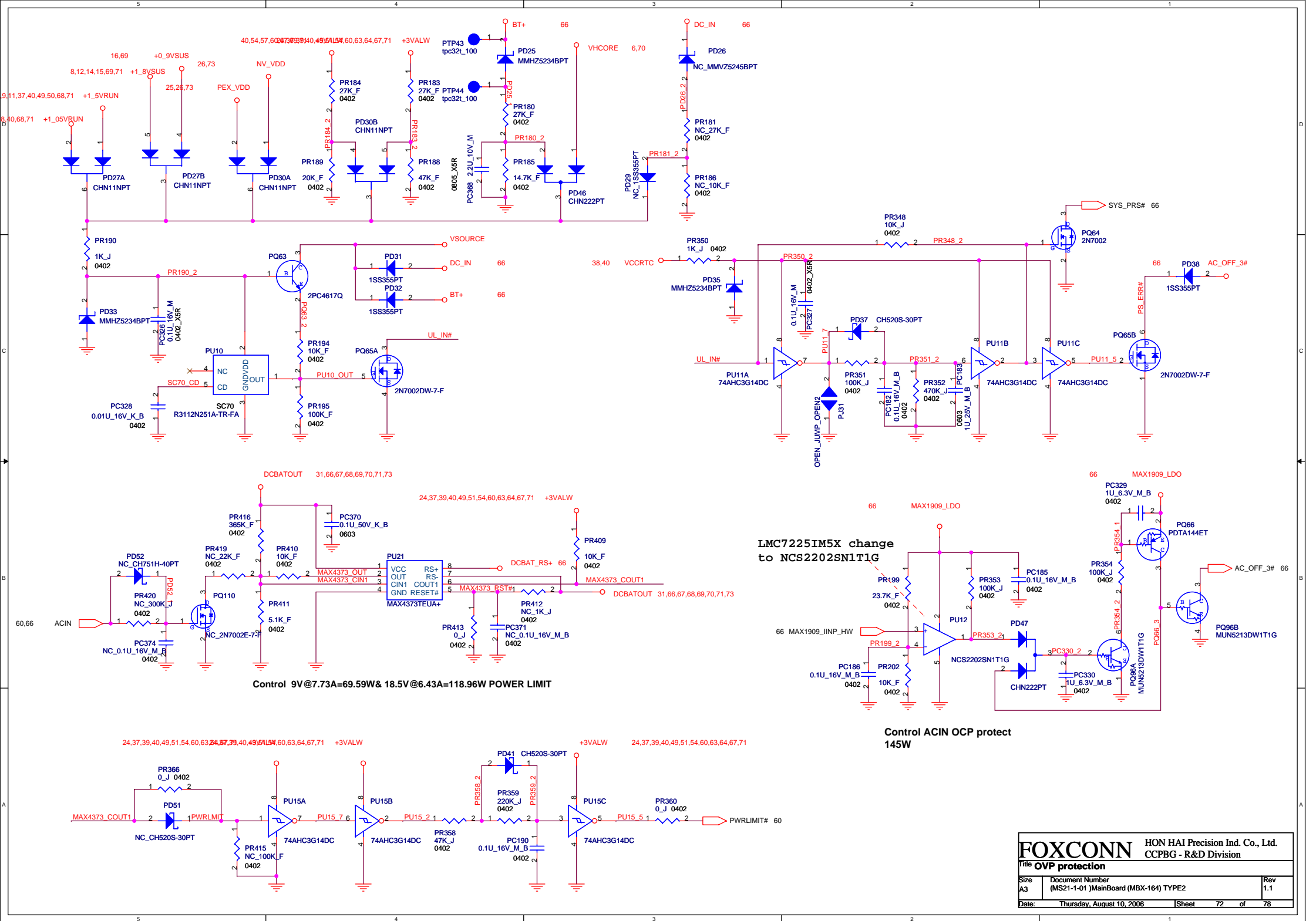
Output capacitor:
 2R5TPL330M9 *6pcs (9 mohm/pcs)
 EEFSX0D331XE*5-6pcs (6 mohm)

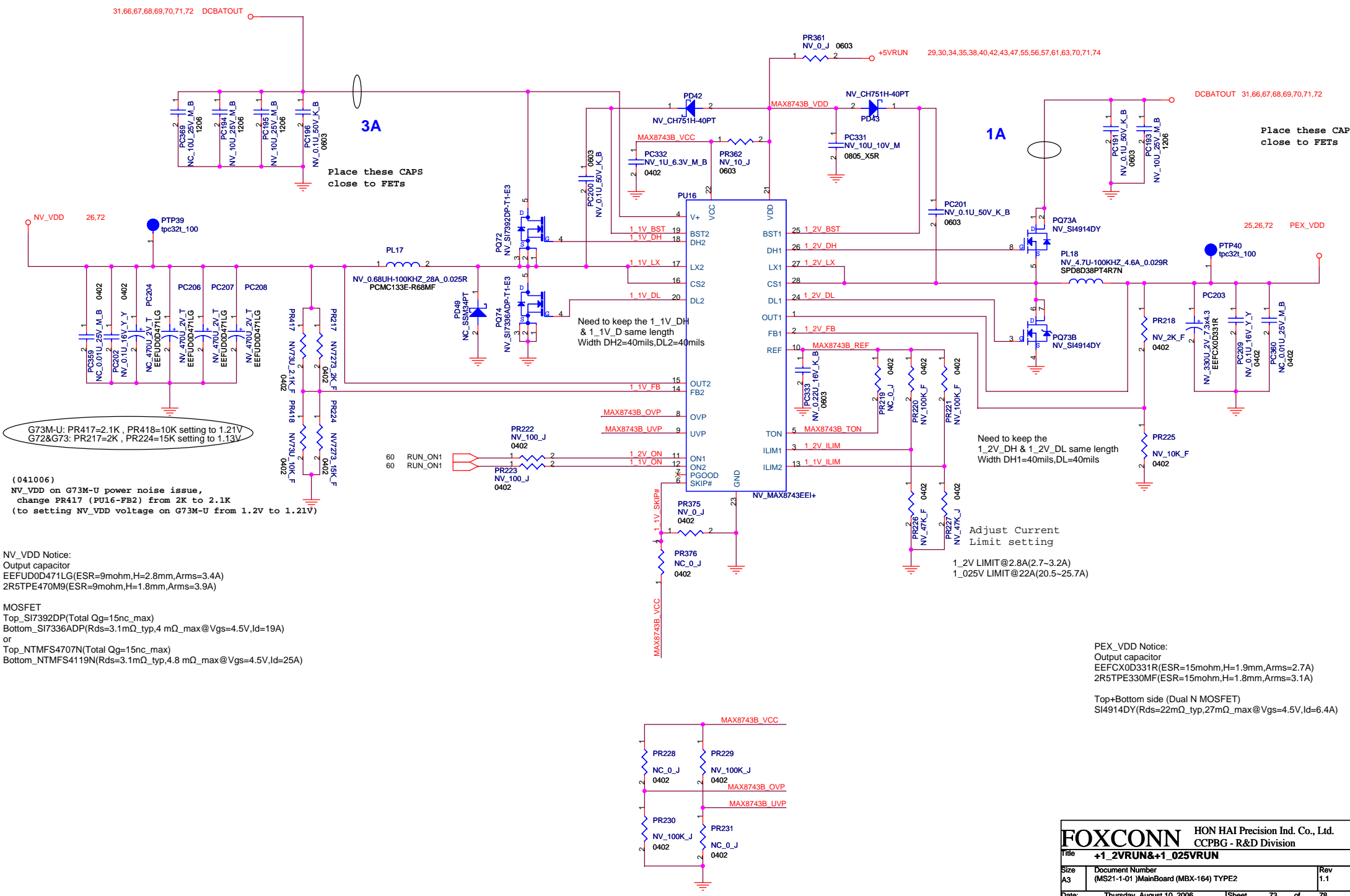
TV turner noise issue:
 (1) Add PR424 (2.2 ohm), PC378 (47pF) on net MAX8771_LX1,
 (2) Add PR425 (2.2 ohm), PC379 (47pF) on net MAX8771_LX2
 *PVT already modify (special notes V0.8)



Discharge circuit for power-off







G73M-U: PR417=2.1K , PR418=10K setting to 1.21V
 G72&G73: PR217=2K , PR224=15K setting to 1.13V

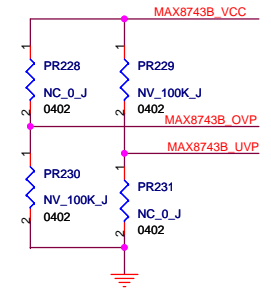
(041006)
 NV_VDD on G73M-U power noise issue,
 change PR417 (PU16-FB2) from 2K to 2.1K
 (to setting NV_VDD voltage on G73M-U from 1.2V to 1.21V)

NV_VDD Notice:
 Output capacitor
 EEFUD0D471LG (ESR=9mohm,H=2.8mm,Arms=3.4A)
 2R5TPE470M9 (ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
 Top_S17392DP (Total Qg=15nc_max)
 Bottom_S17336ADP (Rds=3.1mΩ_typ,4 mΩ_max@Vgs=4.5V,Id=19A)
 or
 Top_NTMFS4707N (Total Qg=15nc_max)
 Bottom_NTMFS4119N (Rds=3.1mΩ_typ,4.8 mΩ_max@Vgs=4.5V,Id=25A)

PEX_VDD Notice:
 Output capacitor
 EEFCX0D331R (ESR=15mohm,H=1.9mm,Arms=2.7A)
 2R5TPE330MF (ESR=15mohm,H=1.8mm,Arms=3.1A)

Top+Bottom side (Dual N MOSFET)
 S14914DY (Rds=22mΩ_typ,27mΩ_max@Vgs=4.5V,Id=6.4A)



FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
File	+1_2VRUN&+1_025VRUN	
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Modify Constant-Current SONY LOGO LED circuit

for U138 cost issue

- 1.Back up:U138(MAX1916EZT),R1936 (91K ohm,0402),R1982(OR,NC),R1983(OR,NC)
- 2.Remove back up solution U139(GMT,G5920TB1UE),C1660(0.1u)
- 3.Add new Constant-Current circuit (OP + MOS)
 - 51K ohm: R1972 ,
 - 1.2K ohm: R1973 ,
 - 1k ohm:R1974 ,
 - 10 ohm: R1975
 - (NC)0 ohm: R1976(for back up U138 MAX1916)
 - 0.1uF,16V: C1679
 - (NC)22uF,6.3V: C1680
 - OP LM358 ADR : U139
 - N-MOS 2N7002: Q158
 - N-MOS DTA114YUA:Q159
 - P-MOS DTC144EUA:Q160

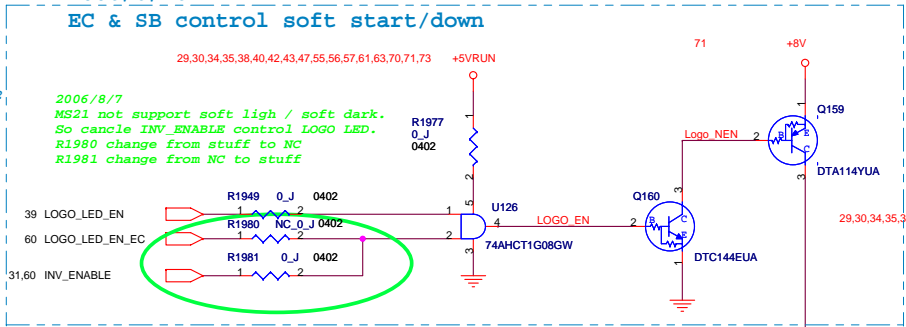
Constant-Current SONY LOGO LED

for EC control soft start/down (function up)issue

- 1.Del R1948(back up LOGO_LED_EN_EC to U126 pin1)
- 2.Serial (Back up) R1981 between INV_ENABLE to U126 pin2
- 3.Move net LOGO_LED_EN_EC from R1948 pin1 to R1980 pin1
- 4.Add R1977 between +5VRUN to U126 pin5(VCC)
- 5.Add R1980 between Logo_led_en_ec to U126 pin2

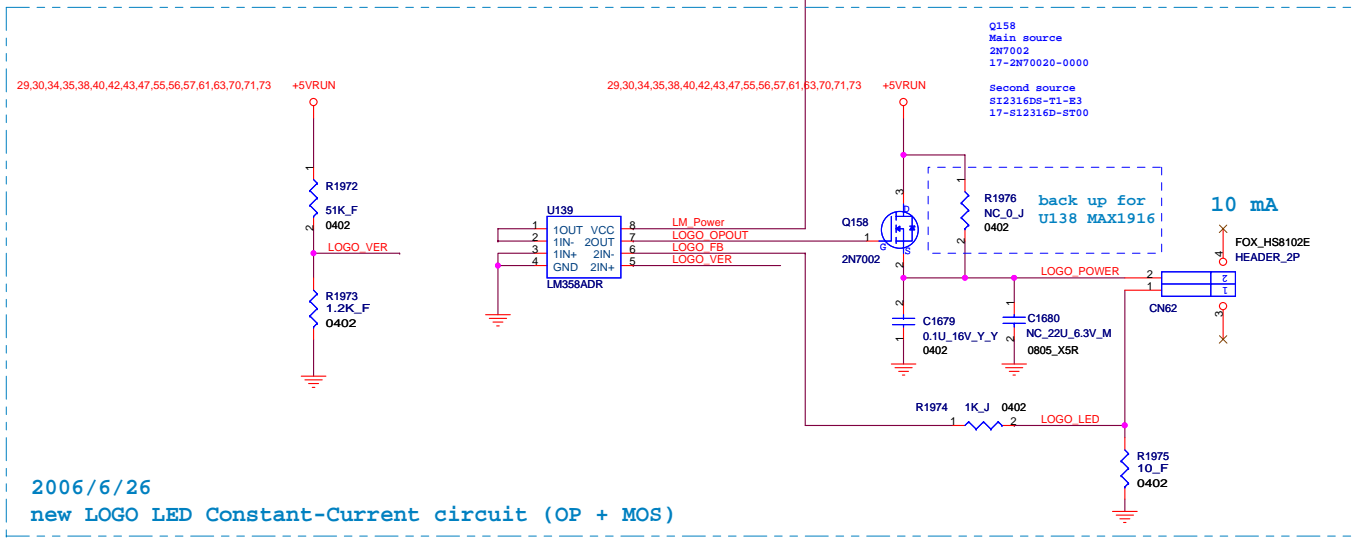
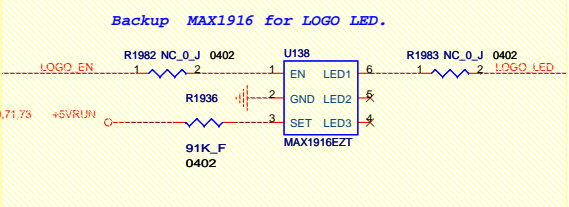
2006/6/26

EC & SB control soft start/down



2006/8/7

MS21 not support soft light / soft dark.
So cancel INV_ENABLE control LOGO LED.
R1980 change from stuff to NC
R1981 change from NC to stuff



2006/6/26

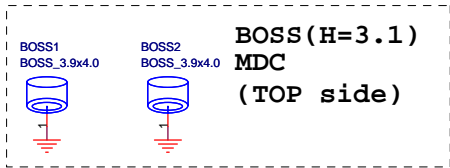
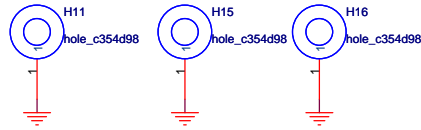
new LOGO LED Constant-Current circuit (OP + MOS)

2006/6/26
(1)remove TP835(GND Test Pad)
(2)add TP857(LOGO_POWER)

2006/6/26
(Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP)
Detail location
10U_25V_M*9pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390) ,
0.01U_25V_K*1pcs(PC387) ,1U_25V_M*1pcs(PC388) ,0.22U_16V_M*1pcs(PC391) ,
220P_50V_K*1pcs(PC392) ,SKS30-04AT-G*1pcs(PD53) ,8UH-100KHZ_2.5A_0.07R*1pcs(PL22) ,
2N7002*2pcs(PQ9114,PQ116) ,FDS6680A*1pcs(PQ117) ,120K_F*1pcs(PR432) ,
0.03_F*1pcs(PR434)95.3K_F*1pcs(PR435) ,10K_F*1pcs(PR436) ,MAX668EUB+T*1pcs(PU22) ,

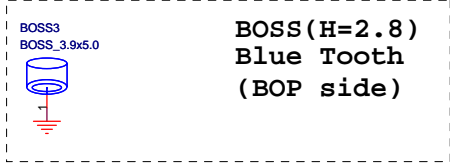
HOLE

Type 1



Type 2

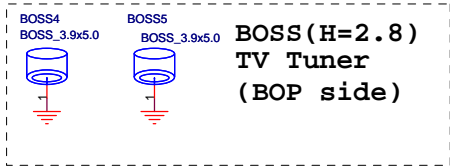
2005/10/24
Remove Screw Hole H2 P/N 1X-HOLE000-0108
because the Hole overlay with CN32 and layout will
modify component screw shipe



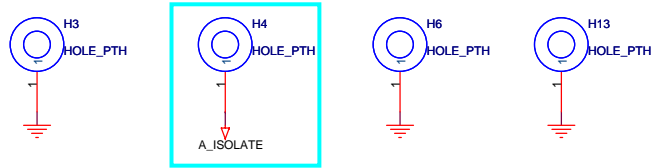
Type 3

2005/10/24
Remove Screw Hole H1 P/N 1X-HOLE000-0110
because the Hole overlay with CN32 and layout will
modify component screw shipe

2006/5/6
Separat analog ground for digital Noise issue:
Isolate screw hole H4 Change H4 net name from
A_GND to A_ISOLATE

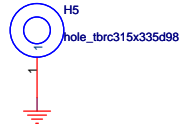


Type 4

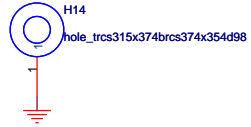


Type NPTH Guide (spherical)HOLD

Type 5

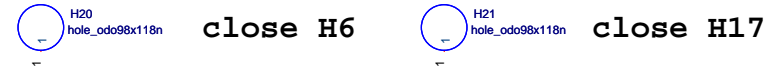


Type 6

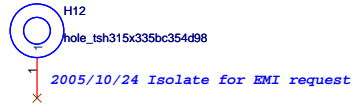


Type NPTH Guide (oval-shaped)HOLD

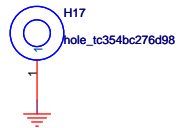
Type 7



Type 8



Type 9



Type CPU



FOXCONN		HON HAI Precision Ind. Co., Ltd.
Title HOLE & BOSS		CCPBG - R&D Division
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MS20 MP to MS21 DVT Change History

(2006/5/23)

- (川) 01.(Page08) Remove R110 for PM_EXTTSH1 back up pull up res.ICH7 (DPRSLPVR)already have internal pull up
- (川) 02.(Page14) Remove backup DIMM thermal sensor Change R168 from stuff to NC(basis on MS20 MP ECR)
- (川) 03.(Page15) Remove backup DIMM thermal sensor Change R1627 from stuff to NC(basis on MS20 MP ECR)
- (蘭) 04.(Page34) US Silicon Image ATC test HDMI DDC capacitance fail(>50pF)change U128 no stuff Basis on MS20 MP ECR add back up res.(R1962)no stuff for U128 VCC
- (才) 05.(Page39) Delete U30,R1183,R649 (backup circuit)
- (業) 06.(Page42) For power droop cause 0.16V voltage loss Issue(1)F7,F8,F19,F20 no stuff(2)Co-layout GP17-GP20 with fuse
- (業) 07.(Page55) Separate analog ground for digital Noise issue
(1)Add bead (L152)before LDO chipand
(2)Change C873 from GND to A_GND
(3)Add C1675 on +5VRUN before L152
- (業) 08.(Page56) Shoei CAP will EOL. CAP24,CAP25(SF CAP) change to Stuff: CAP22,CAP23(Shoei CAP) change to No Stuff
- (業) 09.(Page56) PBSS2515F.115 will EOL ,Q77,Q78,Q143,Q144 change to PBSS2515E.115
- (業) 10.(Page56) Improve the voice of speaker up to 0.94W
(1)Add damping Resistors R1953 on SRIN,R1954 on AMP_SLIN then speaker amp output won't be distorted.
(2)Change R1932 from 6.8K to 5.6K, then amp gain change from 8dB to 10dB.
- (業) 11.(Page57) PBSS2515F.115 will EOL Q89,Q90,Q91,Q92 change to PBSS2515E.115
- (業) 12.(Page59) Improve SMR issue,Add 1uF capacitors close CN64 :C1671,C1672 on USB_VCC2,C1669 on +3VRUN_AUDIO_BD, and C1670 on VDDA .
- (業) 13.(Page59) Separate analog ground for digital Noise issue:
(1)Remove GP3 (Close Jumper)not bridge between GND and A_GND
(2)Backup two jumper resistors for bridge between GND and A_GND
(C1388,C1966 on Screw hole H3,C1957,C1959 on screw hole H5)
(3)Isolate screw hole H4,add 100pF capacitors C1673,C1674 for EMF,Zener diode D100 for ESD
(4)Add jumper resistor for Return patch R1955 close L70(+5VAMP), & R1960 close codec
- (才) 14.(Page39) Remove back up circuit LVDS GPIO on U29 pinU2(1)Add Test Pad TP890 on GPIO34(2)Del Q126
- (業) 15.(Page54) Remove back up F6 power source from +3VALW (Del)R1944,R1946
- (業) 16.(Page67) Reserve PC64(10U_25V_M_B 1206) for 1210 size shortage. Change PR57 from 0805 size to 0603 size for 0603 size rated current is also enough.
- (業) 17.(Page70) Add PC375 (0.1uF) to avoid IMVP_OK signal 700mV pulse when power on. Change PC107/PC108 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- (業) 18.(Page71) Change PC164/PC165 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage.
- (業) 19.(Page71) Change PC368 from 2.2U_16V_M to 2.2U_10V_M for 2.2U_16V_M shortage. Change PU12 from LMC7225IM5X to NCS2202SN1T1G for LMC7225IM5X shortage.
- (才) 20.(Page60) Modify system ID setting. R725 from stuff change to NC,R726 from NC change to stuff
- (蘭) 21.(Page32) CN66,CN67 Change from MOLEX(IN-0010000-MWGO) to FOXCONN(IN-0010000-F0T0)
- (業) 22.(Page63) CN68 Change from MOLEX(IN-0010000-MWGO) to FOXCONN(IN-0010000-F0T0)
- (業) 23.(Page57) Add C1676 (4.7 uF/bypass cap) close A_U99 pin8
- (業) 24.(Page58) Add C1677,C1678 (4.7 uF/bypass cap) close A_U101,U102 pin8
- (業) 25.(Page74) Add Inverter Boost Circuit

(2006/5/24)

- (業) 1.(Page55) According to MOR suggest Change Int MIC topology from single end to differential
(1) C1251 change from 33pF 0402 to 1uF 0603
(2) C1252 change from 12pF 0402 to 1uF 0603
(3) C1270 change from 0.1F 0402 to 1uF 0603
(4) Add R1967, R1968 100 ohm 0402
- 2.(Page57) According to MOR suggest Change Int MIC topology from single end to differential
(1) C1231 change from 4.7uF 0805 to 220pF 0402
(2) C1232 change from 1uF 0805 to 4.7uF 0805
(3) C1233 change from 4.7uF 0805 to NC_33pF 0402
(4) C1234 change from 100pF 0402 to NC_33pF 0402
(5) C1237 change from 100pF 0402 to 33pF 0402
(6) R1318 change from 10Kohm 0402 to 5.1Kohm 0402
(7) R1319 change from 1Kohm 0402 to 4.7Kohm 0402
(8) R1320 change from 33ohm 0402 to 100ohm 0402
(9) R1321 change from NC_0ohm 0402 to 4.7Kohm 0402
(10) R1325 change from 47Kohm 0402 to 4.7Kohm 0402
(11) R1326 change from 7.5Kohm 0402 to 2.2Kohm 0402
(12) R1327 change from 100ohm 0402 to 1Kohm 0402
(13) Add R1970, R1971 100 ohm 0402
(14) Add R1969 4.7 Kohm 0402
(15) R1236 change from 4.7u to 1u

(2006/5/26)

- (業) (1) C1230 change from 2200pF to 4700 pF by MOR request

MS21 DVT to MS21 PVT Change History

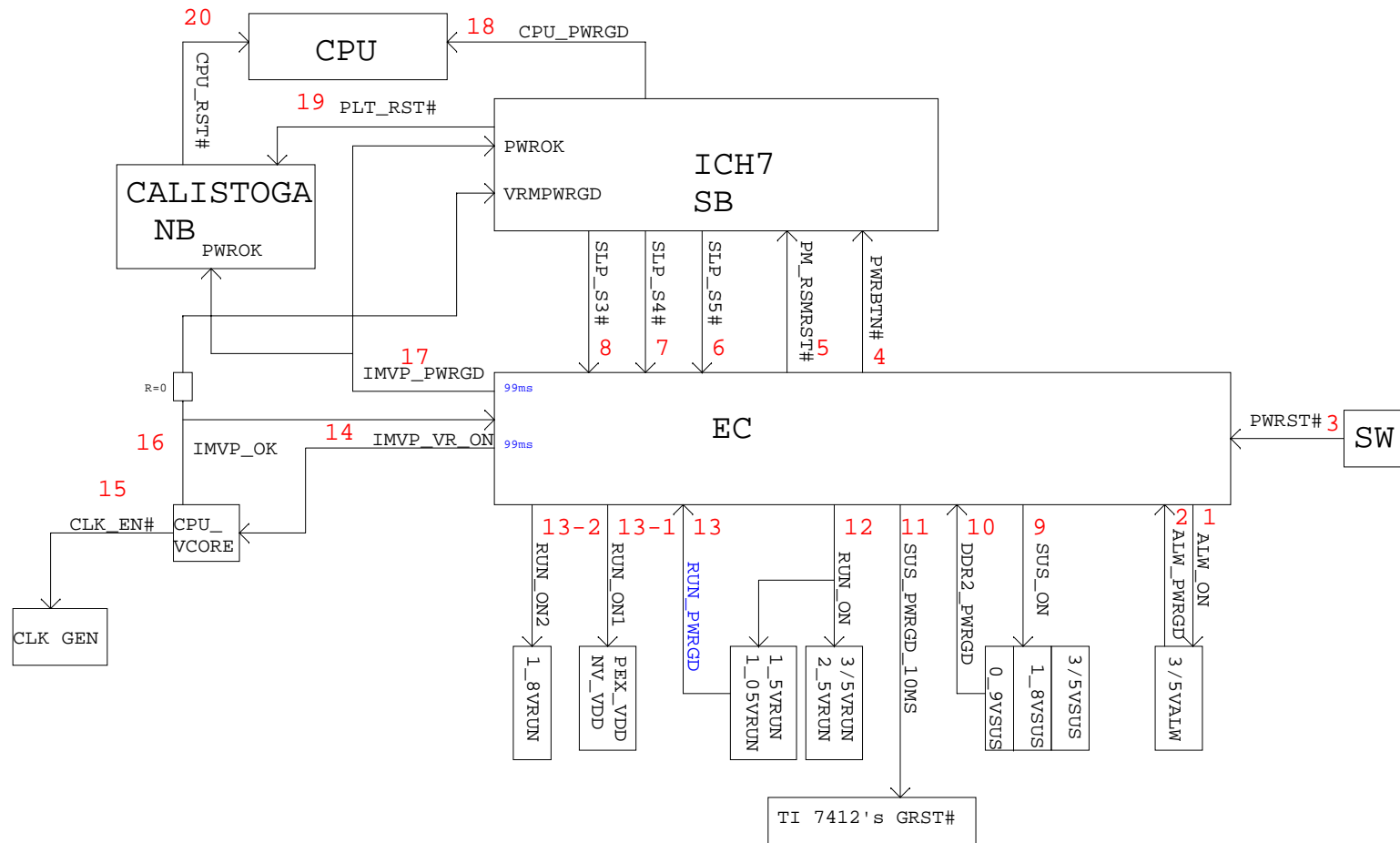
(2006/6/26)

- (才) 01.(Page60) Solve Doi san concern EC's GPIO23 is CMOS out and if BTR drive it to GND it may damage the EC.
(1)Change R1762 from 0 to 1K ohm,
(2)Change net name R1762-2 from N18386242 to EC_GPIO23
(3)Change net name R690-1 from ALW_ON to EC_GPIO23
- (蘭) 02.(Page31) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP
(1)Delete PR426&PR427
(2)change C604-1,C1557-1,C1558-1,CN49 pin1,pin2 net name INVERTER_VCC to net DCBATOUT.
- (業) 03.(Page74) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP
Delete 10U_25V_M*9pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390),
0.01U_25V_K*1pcs(PC387),1U_25V_M*1pcs(PC388),0.22U_16V_M*1pcs(PC391),
220P_50V_K*1pcs(PC392),SKS30-04AT-G*1pcs(PD53),8UH-100KHZ_2.5A_0.07R*1pcs(PL22),
2N7002*2pcs(PQ114,PQ116),FDS86680A*1pcs(PQ117),120K_F*1pcs(FR432),
0.03_F*1pcs(FR434)95.3K_F*1pcs(FR435),10K_F*1pcs(FR436),MAX668EUB+T*1pcs(PU22),
100K_u*1pcs (FR428) 100K_u*1pcs (FR429)
- (業) 04.(Page67)Change PR53&PR55 from 100_J to 0_J by Mor side suggestions
Original PR53&PR55(100ohm) is used as current limit.But now we have added series 1K ohm,
(Page 60, change R1762 from 0 ohm to 1K ohm) So we need not 100ohm resistor for curret limit
- (業) 05.(Page56) Modify internal speaker AMP gain setting,change R1953/R1954 from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98W) to fit in speaker (1.0W)spec.
- (業) 06.(Page57) Modify internal MIC AMP gain setting,change R1318 from 5.1K to 5.9K ohm, To lead TYPE2 board gain (differential type MIC)the same with TYPE1 board single end MIC) (Gain=9.2)
- (才) 07.(Page60) Modify Constant-Current SONY LOGO LED circuit for EC control soft start/down (function up)issue
(1).Del back up Test Pad TP864
(2).Add R1978 (0 ohm) link EC pin176 and INV_ENABLE
- (業) 08.(Page74) Modify Constant-Current SONY LOGO LED circuit
A. for U138 cost issue
1.Back up:U138(MAX1916E2T),R1936 (91K ohm,0402),R1982(0R,NC),R1983(0R,NC)
2.Remove back up solution U139(GMT,G5920TB1UF),C1660(0.1u)
3.Add new Constant-Current circuit (OP + MOS)
51K ohm: R1972 ,
1.2K ohm: R1973 ,
1k ohm:R1974
10 ohm: R1975
(NC)0 ohm: R1976(for back up U138 MAX1916)
0.1uF,16V: C1679
(NC)22uF,6.3V: C1680
OP LM558 AMP : U139
N-MOS 2N7002: Q158
N-MOS DTA114YUA:Q159
P-MOS DTCL44EUA:Q160
B. for EC control soft start/down (function up)issue
1.Del R1948(back up LOGO_LED_EN_EC to U126 pin1)
2.Serial (Back up) R1981 between INV_ENABLE to U126 pin2
3.Move net LOGO_LED_EN_EC from R1948 pin1 to R1980 pin1
4.Add R1977 between +5VRUN to U126 pin5(VCC)
5.Add R1980 between Logo_led_en_ec to U126 pin2
- (業) 09.(Page 42) Delete SATA HDD Fuse backup circuit
(1)Remove F7,F8,F19,F20 Pad
(2)Remove GP17-GP18 open gap
- (才) 10. (Page 62) MOR fan circuit modify to backup
(NC)U118 (NC)R1893
(NC)R1624 (NC)C1473
(NC)R1894 (NC)R1895

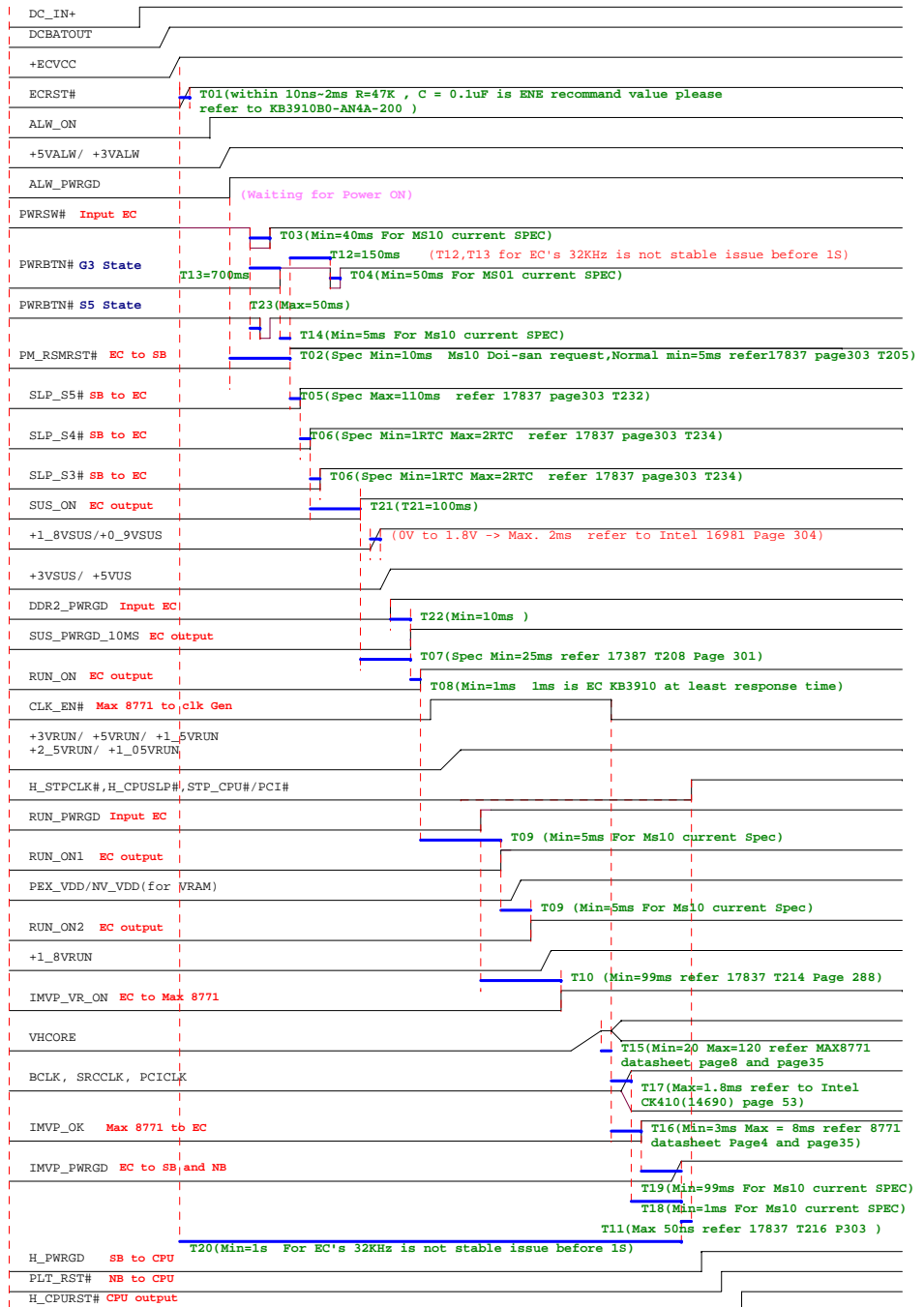
MS21 PVT to MS21 MP Change History

- (業) 01.(Page74) MS21 not support soft light / soft dark. So cancle INV_ENABLE control LOGO LED.
R1980 change from stuff to NC
R1981 change from NC to stuff
- (才) 02.(Page60) MS21 not support soft light / soft dark. So cancle INV_ENABLE control LOGO LED.
R1978 Change from stuff to NC
- (業) 03.(Page57) Change C1676 from stuff to NC for MOR suggestion Cost down request.
- (業) 04.(Page66) At MS21 PCN1 used FOXCONN connector, Change PCN1 Vendor from molex to NWING
- (業) 05.(Page29) Change D60,D61,D81 Value from NV to Normal
- (業) 06.(Page20) Change Y2 Value from Normal to NV

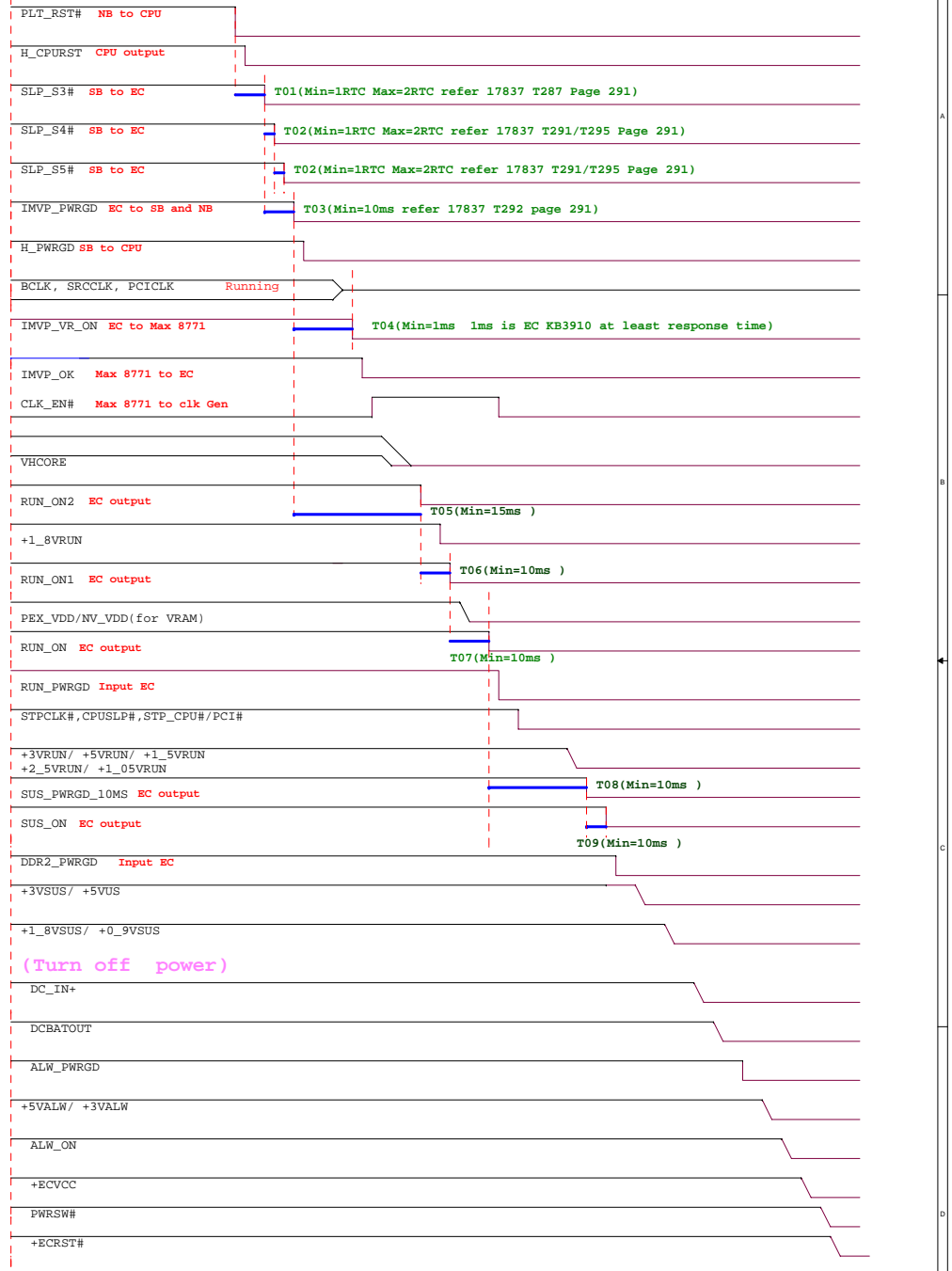
MS21 Power On Sequence Block Diagram



Power On/Off Sequerce Specification



T01	T02	T03	T04	T05	T06	T07	T08	T09	T10	T11	
within 10ns-2ms	Min. 10ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCCLK	Min. 25ms	Min. 1ms	Min. 10ms	Min. 99ms	Max. 50ms	
T12	T13	T14	T15	T16	T17	T18	T19	T20	T21	T22	T23
Min. 150ms	Min 700ms	Min 5ms	Min : 20us Max : 120us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min. 99ms	Min. 1s	100ms	Min. 10ms	Max 50ms



T01	T02	T03	T04	T05	T06	T07	T08	T09
1 - 2 RTCCCLK	1 RTCCLK	Min. 10ms	Min. 1ms	Min. 15ms	Min. 10ms	Min. 10ms	Min. 10ms	Min. 10ms

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

File: MS21 Power On Sequence Timing specification

Doc Number: MS21-1-01 MainBoard (MBX-164) TYPE2

Date: Thursday, August 10, 2006

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