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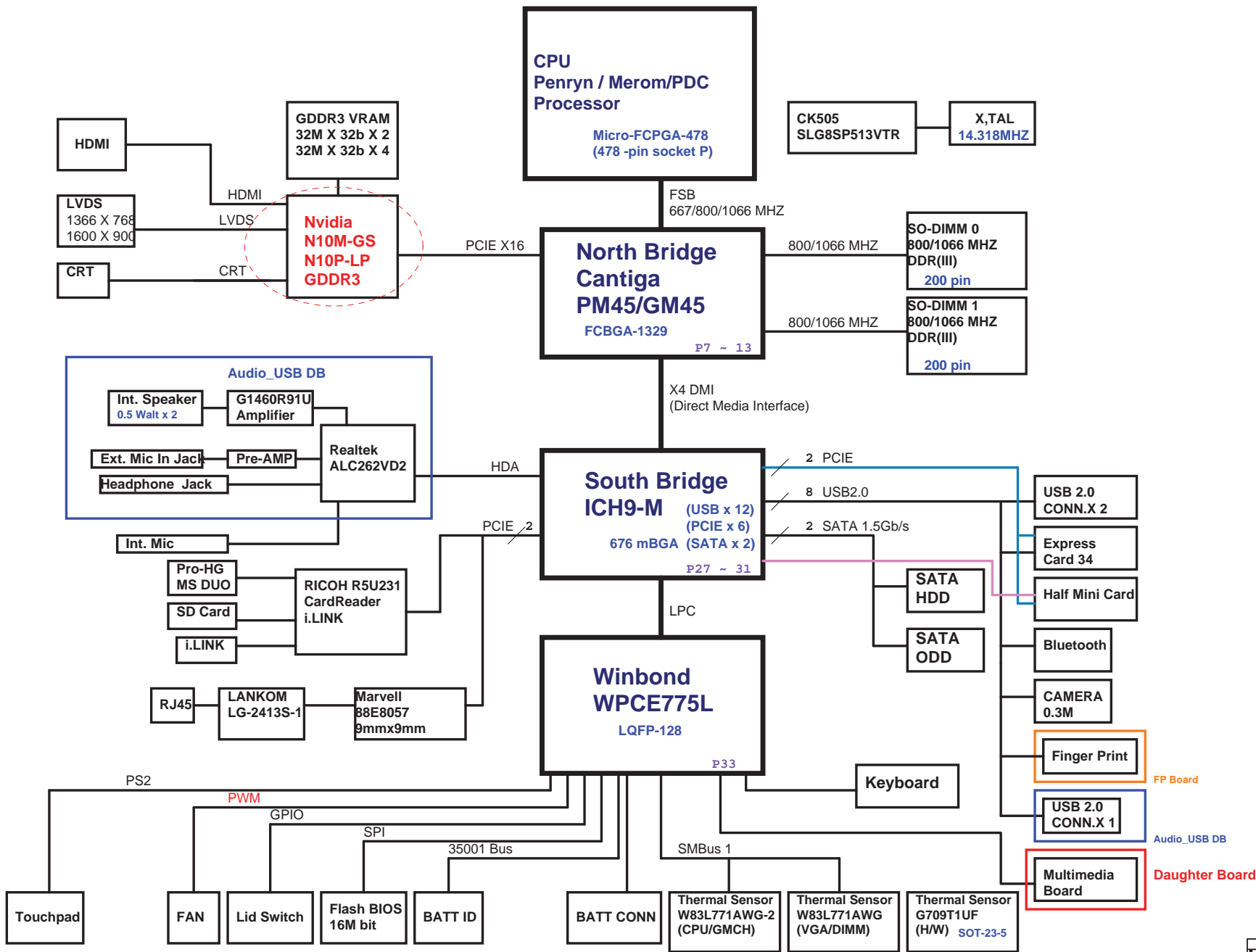
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19	VGA(GDDR)# 4/9	1.0	09'07'27	56	SYS Power(+1_5V/+1_05V)	1.0	09'07'27
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21	VGA (LVDS/TMDS) 6/9	1.0	09'07'27	58	CPU_Vcore---ISL6266A	1.0	09'07'27
22	VGA (XTAL/GPIO) 7/9	1.0	09'07'27	59	Others power plane	1.0	09'07'27
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37	EC+KBC (WPCE775L)	1.0	09'07'27	74	History (4)	1.0	09'07'27

Project Code & Schematics Subject: M870 Main Board_8L

PCB P/N:	(IRIS) :1P-0097J00-8010 (HANNSTAR) :1P-0097500-8010
A/B P/N:	(IRIS) :1P-1097J02-8010 (HANNSTAR) :1P-1097500-8010
FU/B P/N:	(IRIS) :1P-1097J00-8010 (HANNSTAR) :1P-1097503-8010
Ch/B P/N:	(IRIS) :1P-1097J01-8010 (HANNSTAR) :1P-1097501-8010
FP/B P/N:	(IRIS) :1P-1097J03-8010 (HANNSTAR) :1P-1097502-8010

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M870(Montevina + N10M/N10P-LP)



TI CHARGER	
BQ24753 P.54	
OUTPUTS	
DC_IN	BT+
	DCBATOUT
SYSTEM DC/DC	
MAX17020ETJ+ P.55	
INPUTS	OUTPUTS
DCBATOUT	+5VALW
	+5VALW_LDO
	+3VALW
	+ECVCC
	+12V
SYSTEM DC/DC	
SC412 P.56	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN
	+1_05VRUN
SYSTEM DC/DC	
SC412+G2998 P.57	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS
+1_8VSUS	+0_9VRUN
CPU DC/DC	
ISL6266A P.58	
INPUTS	OUTPUTS
DCBATOUT	VHORE
SYSTEM DC/DC	
SC411+APL5913 P.61	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD
+1_5VRUN	PEX_VDD

7 H_A# [3..35]

7 H_ADSTB#0
7 H_REQ# [4..0]

7 H_ADSTB#1

33 H_A20M#

33 H_FERR#

33 H_IGNNE#

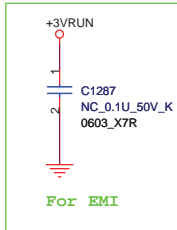
33 H_STPCLK#

33 H_INTR#

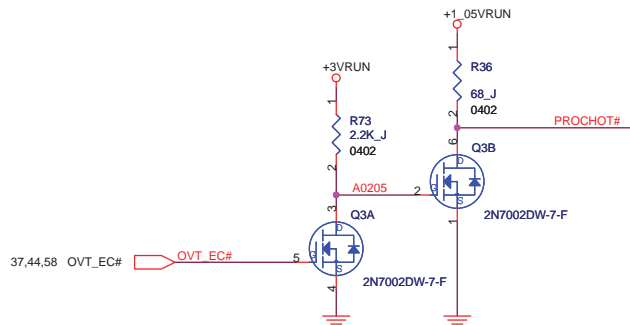
33 H_NMI#

33 H_SMI#

- TP15 20MIL 1 TP CPU RSVD01 M4
- TP18 20MIL 1 TP CPU RSVD02 N5
- TP7 20MIL 1 TP CPU RSVD03 T2
- TP11 20MIL 1 TP CPU RSVD04 V3
- TP5 20MIL 1 TP CPU RSVD05 B2
- TP14 20MIL 1 CPU TEST7 C3
- TP6 20MIL 1 TP CPU RSVD07 D2
- TP25 20MIL 1 TP CPU RSVD08 D22
- TP10 20MIL 1 TP CPU RSVD09 D3
- TP19 20MIL 1 TP CPU RSVD10 F6



CPU SOCKET_478P
FOX_P24782A-274M-01



U26A

ADDR GROUP 0

ADDR GROUP 1

XDP/TIP SIGNALS

THERMAL

H CLK

RESERVED

CONTROL

H ADSTB

H A20M#

H FERR#

H IGNNE#

H STPCLK#

H INTR#

H NMI#

H SMI#

RSVD

PROCHOT#

THERMDA

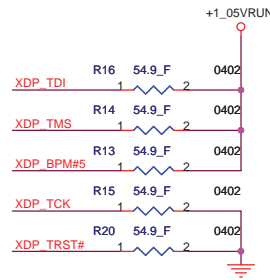
THERMDC

THERMTRIP#

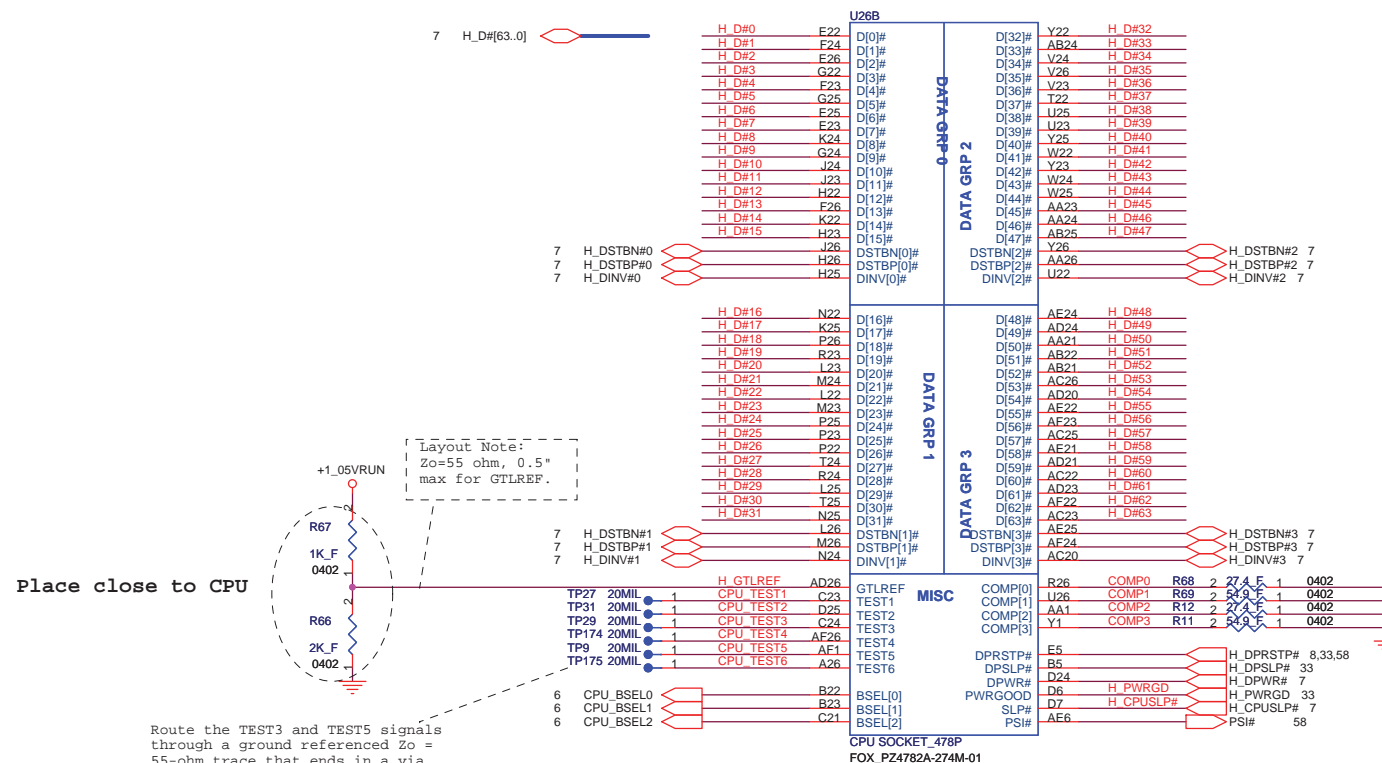
CLK_CPU_BCLK

CLK_CPU_BCLK#

H_CPURST# 1 20MIL TP2



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7 H_D#[63..0]

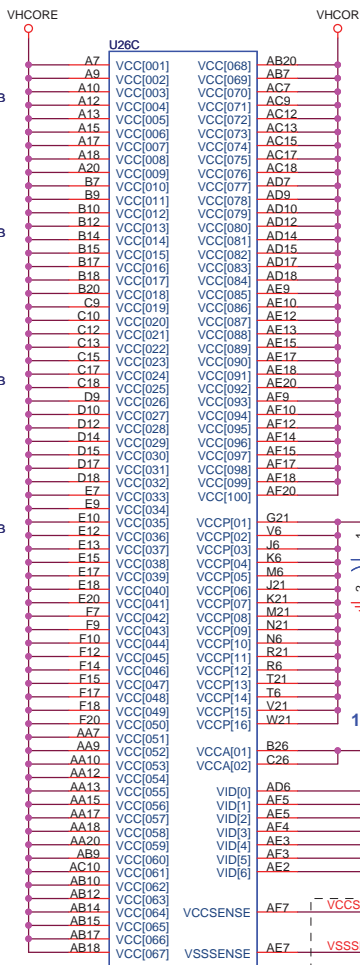
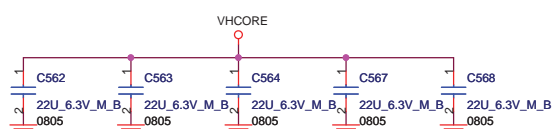
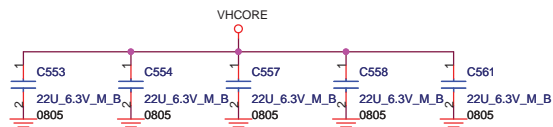
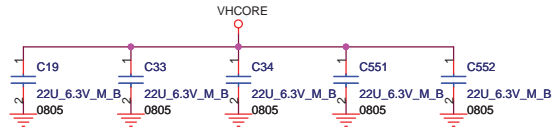
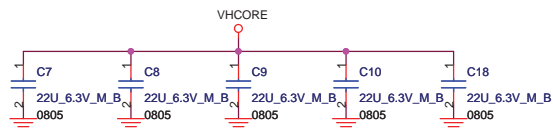
Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

Place close to CPU

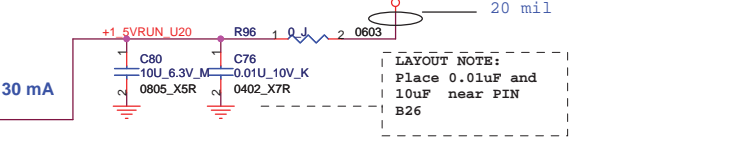
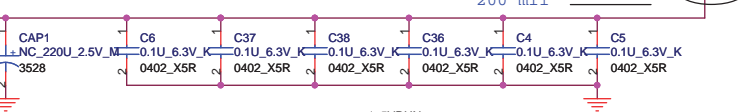
Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=18mil(MS)
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)

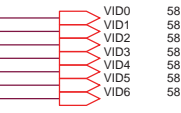
H_PWRGD 1 20MIL TP135
H_CPUSLP# 1 20MIL TP20



CPU_VCCA---->0.13A
 CPU_VCCP---->4.5A
 CPU_VCC---->50A

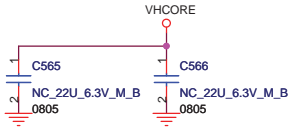
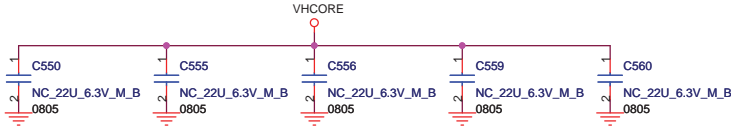
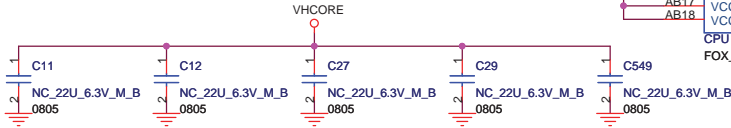
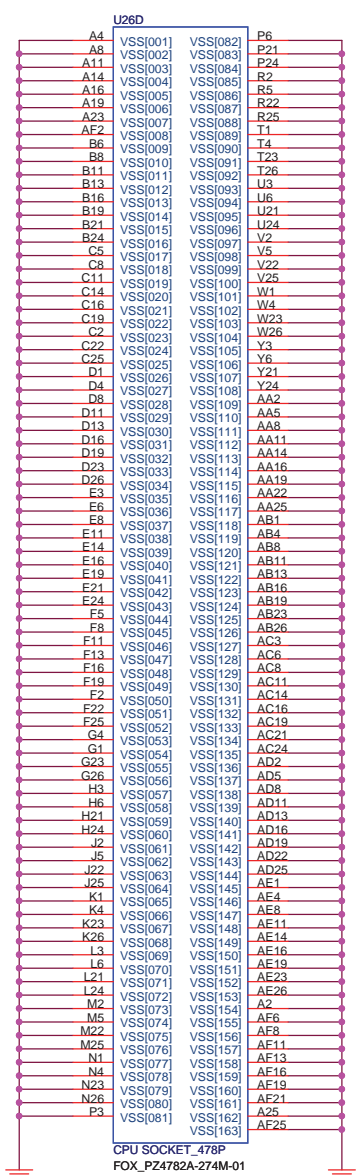


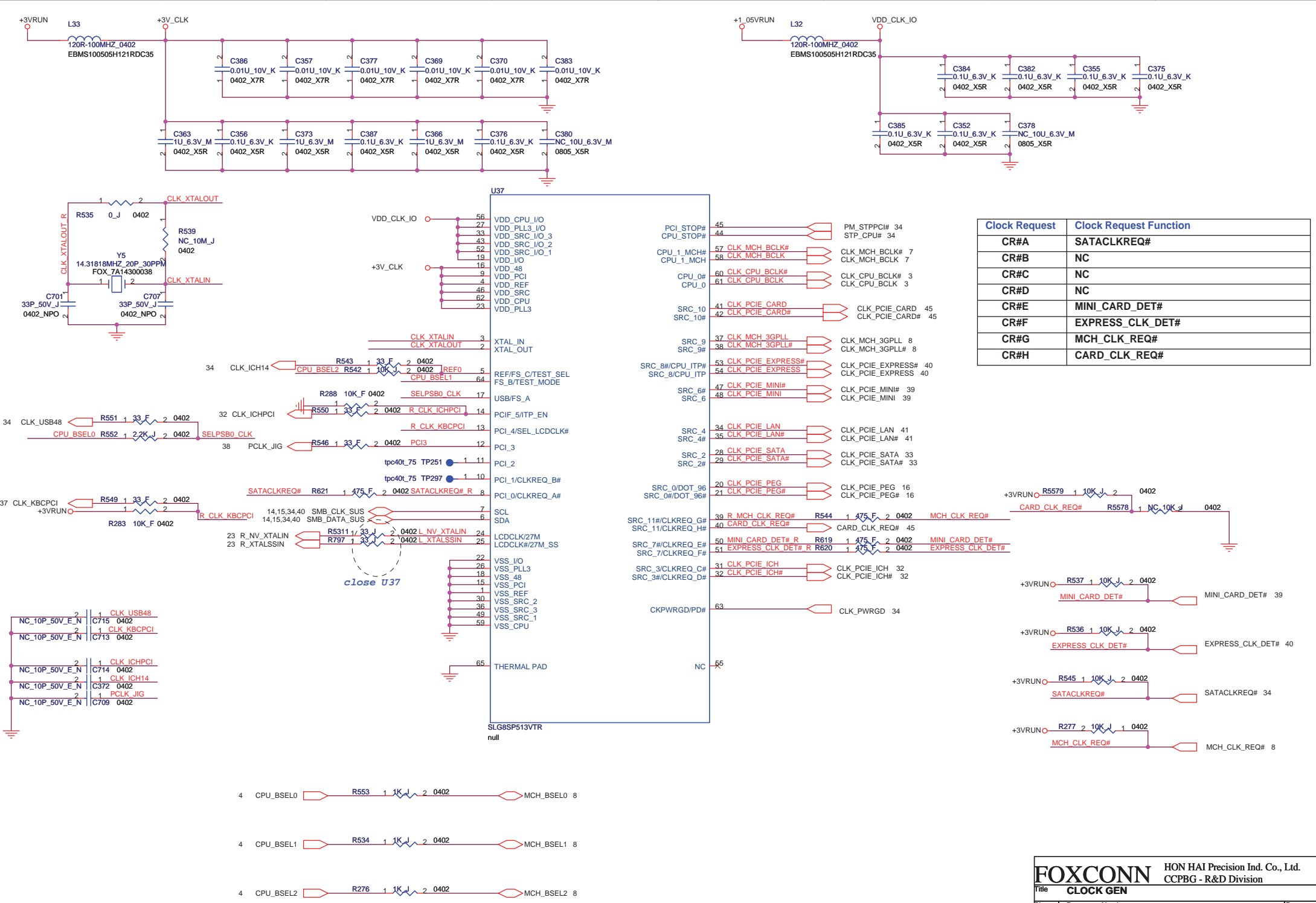
LAYOUT NOTE:
 Place 0.01uF and 10uF near PIN B26



Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 1 inch of CPU.

Outer width=18 mil spacing=7 mil
 Inner width=14 mil spacing=7 mil
 Length match < 25 mil





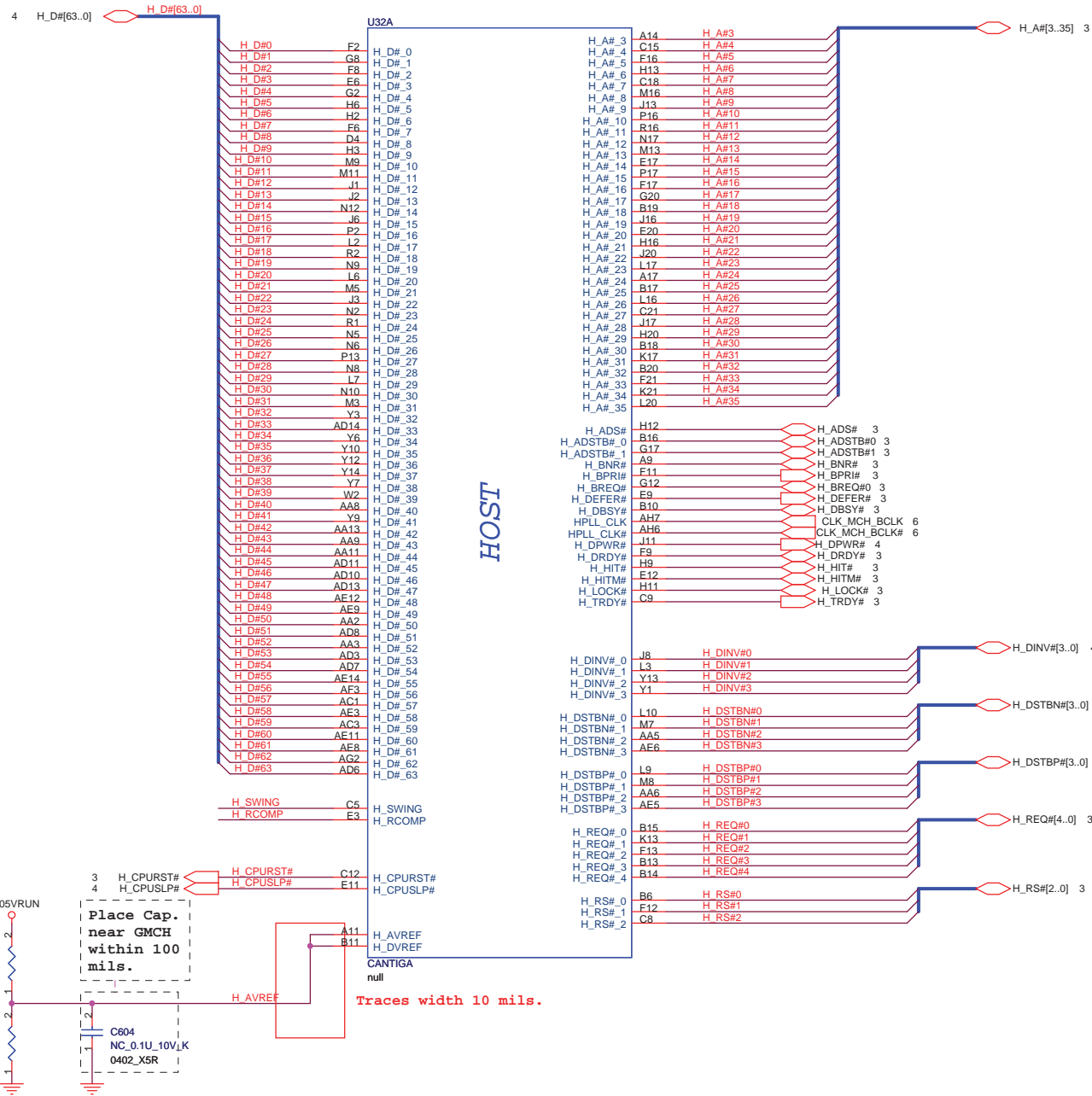
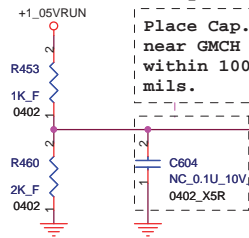
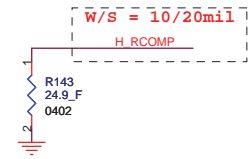
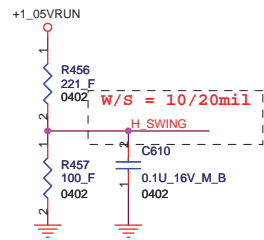
Clock Request	Clock Request Function
CR#A	SATACLKREQ#
CR#B	NC
CR#C	NC
CR#D	NC
CR#E	MINI_CARD_DET#
CR#F	EXPRESS_CLK_DET#
CR#G	MCH_CLK_REQ#
CR#H	CARD_CLK_REQ#

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Title: **CLOCK GEN**

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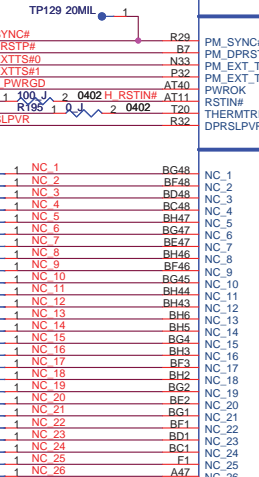
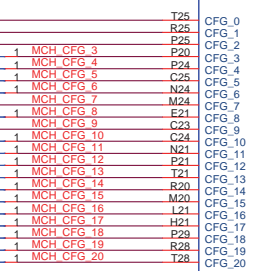
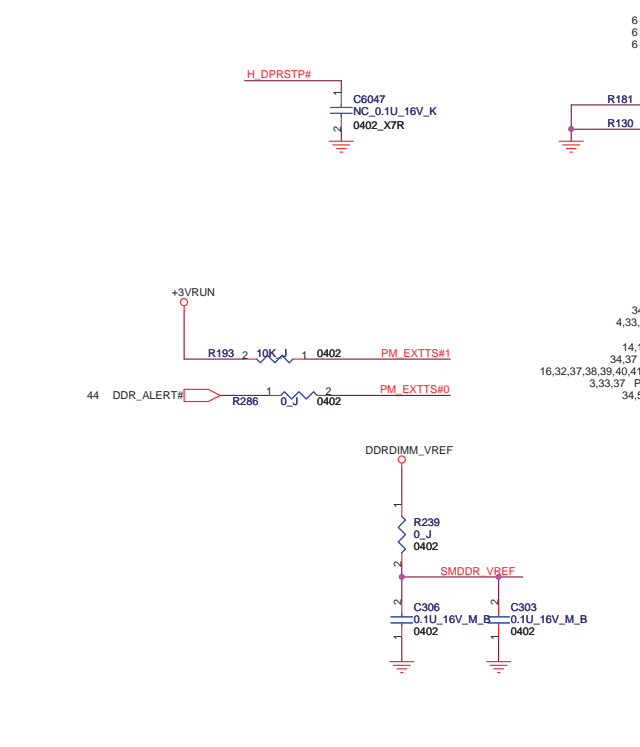
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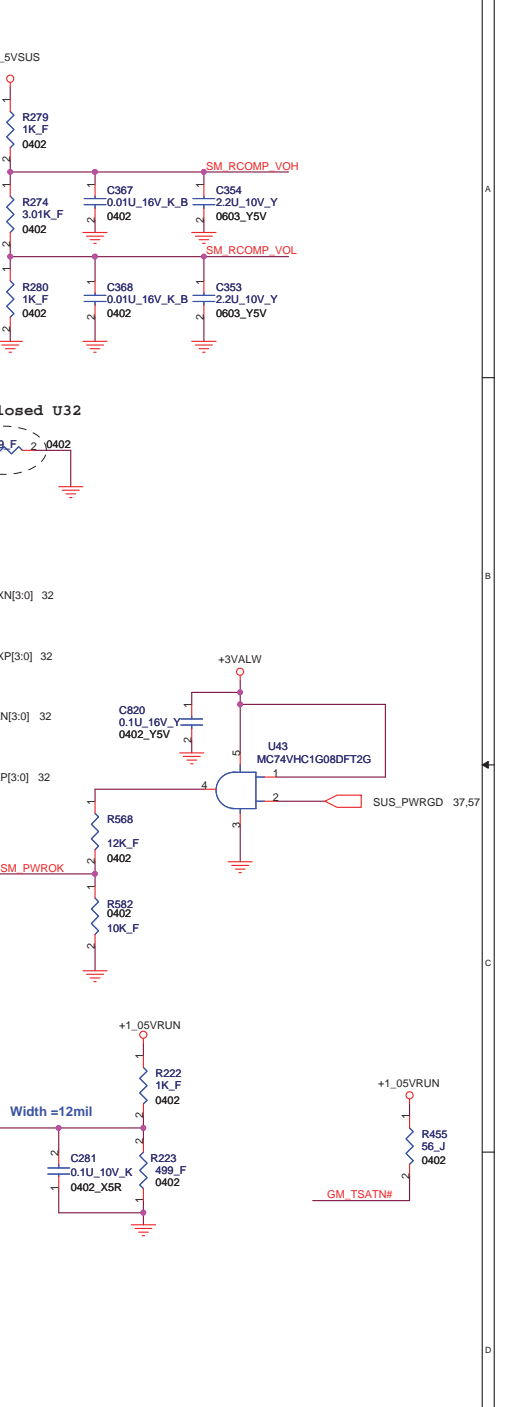
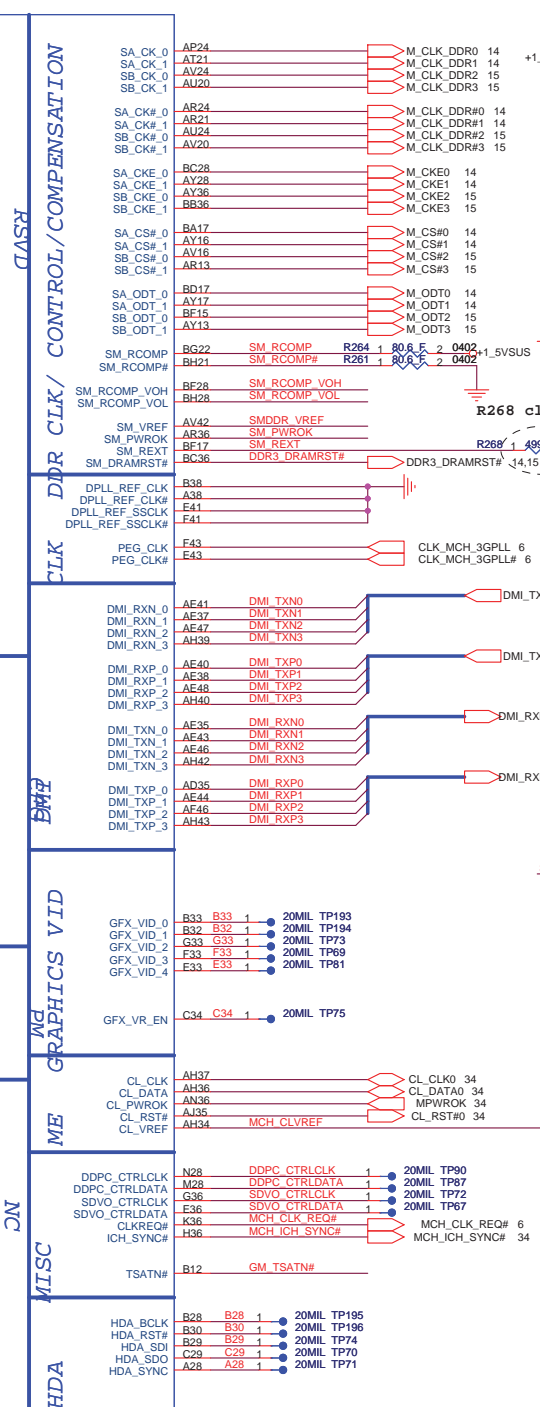
MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

- U32B**
- TP112 20MIL 1 M36 M36 RSV01
 - TP132 20MIL 1 N36 N36 RSV02
 - TP148 20MIL 1 R33 R33 RSV03
 - TP133 20MIL 1 T33 T33 RSV04
 - TP157 20MIL 1 AH9 AH9 RSV05
 - TP156 20MIL 1 AH10 AH10 RSV06
 - TP77 20MIL 1 AH12 AH12 RSV07
 - TP173 20MIL 1 AH13 AH13 RSV08
 - TP181 20MIL 1 K12 K12 RSV09
 - TP182 20MIL 1 AL34 AL34 RSV10
 - TP183 20MIL 1 AK34 AK34 RSV11
 - TP184 20MIL 1 AN35 AN35 RSV12
 - TP185 20MIL 1 AM35 AM35 RSV13
 - TP188 20MIL 1 T24 T24 RSV14
 - TP187 20MIL 1 B31 B31 RSV15
 - TP80 20MIL 1 B2 B2 RSV16
 - TP192 20MIL 1 M1 M1 RSV17
 - TP186 20MIL 1 AY21 AY21 RSV20
 - TP78 20MIL 1 BG23 BG23 RSV22
 - TP189 20MIL 1 BF23 BF23 RSV23
 - TP190 20MIL 1 BH18 BH18 RSV24
 - TP191 20MIL 1 BF18 BF18 RSV25

- CFG**
- CFG_0
 - CFG_1
 - CFG_2
 - CFG_3
 - CFG_4
 - CFG_5
 - CFG_6
 - CFG_7
 - CFG_8
 - CFG_9
 - CFG_10
 - CFG_11
 - CFG_12
 - CFG_13
 - CFG_14
 - CFG_15
 - CFG_16
 - CFG_17
 - CFG_18
 - CFG_19
 - CFG_20



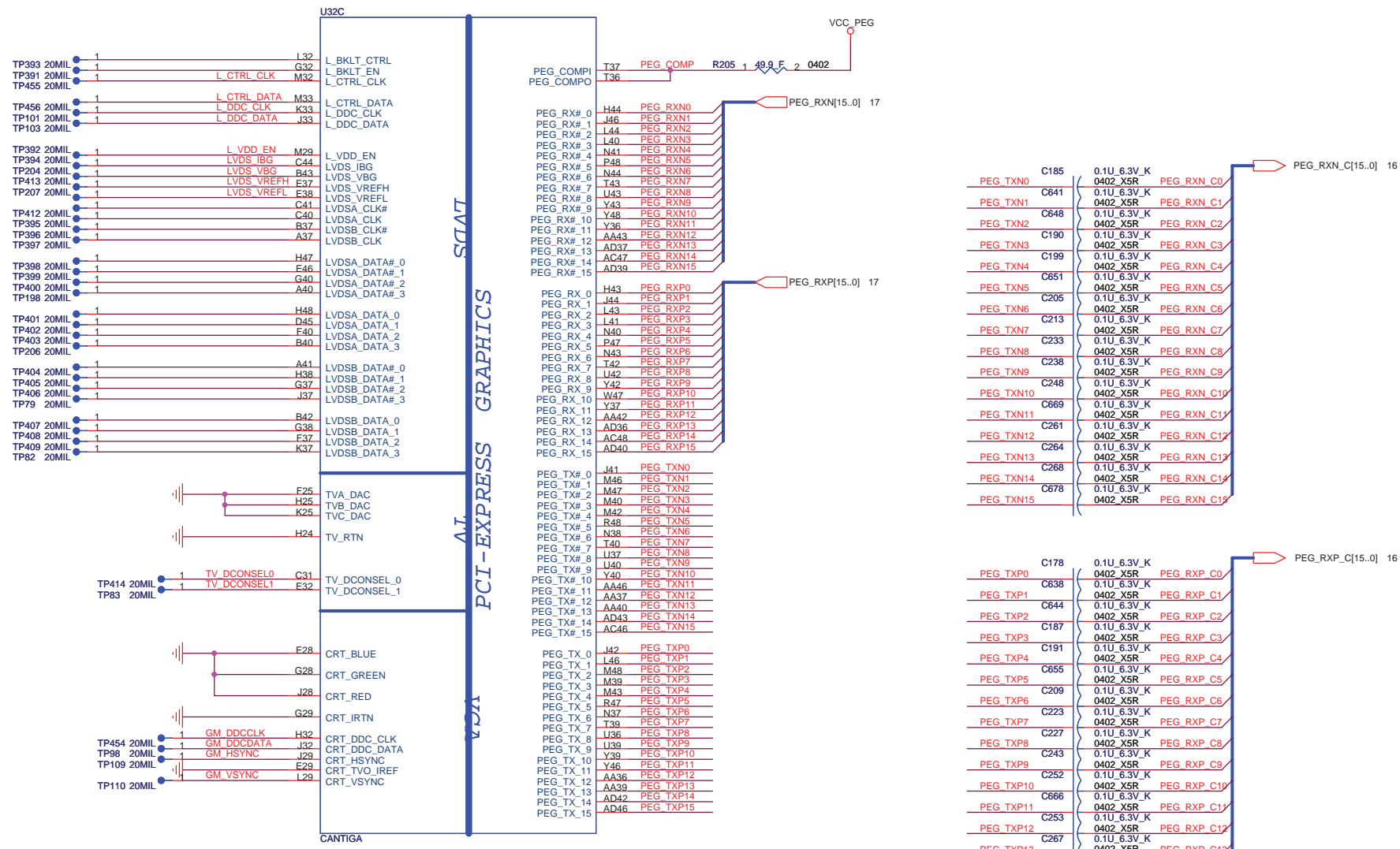
- NC**
- TP231 20MIL 1 NC 1 BG48 NC 1
 - TP229 20MIL 1 NC 2 BF48 NC 2
 - TP223 20MIL 1 NC 3 BD48 NC 3
 - TP222 20MIL 1 NC 4 BC48 NC 4
 - TP234 20MIL 1 NC 5 BH47 NC 5
 - TP230 20MIL 1 NC 6 BG47 NC 6
 - TP224 20MIL 1 NC 7 BE47 NC 7
 - TP240 20MIL 1 NC 8 BH46 NC 8
 - TP232 20MIL 1 NC 9 BF46 NC 9
 - TP238 20MIL 1 NC 10 BG45 NC 10
 - TP237 20MIL 1 NC 11 BH44 NC 11
 - TP223 20MIL 1 NC 12 BH43 NC 12
 - TP239 20MIL 1 NC 13 BH46 NC 13
 - TP236 20MIL 1 NC 14 BH5 NC 14
 - TP241 20MIL 1 NC 15 BG4 NC 15
 - TP242 20MIL 1 NC 16 BH4 NC 16
 - TP228 20MIL 1 NC 17 BF3 NC 17
 - TP235 20MIL 1 NC 18 BH2 NC 18
 - TP226 20MIL 1 NC 19 BG2 NC 19
 - TP220 20MIL 1 NC 20 BE2 NC 20
 - TP227 20MIL 1 NC 21 BG1 NC 21
 - TP225 20MIL 1 NC 22 BF1 NC 22
 - TP221 20MIL 1 NC 23 BD1 NC 23
 - TP219 20MIL 1 NC 24 BC1 NC 24
 - TP213 20MIL 1 NC 25 F1 NC 25
 - TP205 20MIL 1 NC 26 A47 NC 26



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Cantiga (DMI) 2/7

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14 M_A_DQ[63..0]

M_A DQ0	AJ38	SA_DQ_0
M_A DQ1	AJ41	SA_DQ_1
M_A DQ2	AN38	SA_DQ_2
M_A DQ3	AM38	SA_DQ_3
M_A DQ4	AJ36	SA_DQ_4
M_A DQ5	AJ40	SA_DQ_5
M_A DQ6	AM44	SA_DQ_6
M_A DQ7	AM42	SA_DQ_7
M_A DQ8	AN43	SA_DQ_8
M_A DQ9	AN44	SA_DQ_9
M_A DQ10	AJ40	SA_DQ_10
M_A DQ11	AT38	SA_DQ_11
M_A DQ12	AN41	SA_DQ_12
M_A DQ13	AN39	SA_DQ_13
M_A DQ14	AJ44	SA_DQ_14
M_A DQ15	AJ42	SA_DQ_15
M_A DQ16	AV39	SA_DQ_16
M_A DQ17	AY44	SA_DQ_17
M_A DQ18	BA40	SA_DQ_18
M_A DQ19	BD43	SA_DQ_19
M_A DQ20	AV41	SA_DQ_20
M_A DQ21	AY43	SA_DQ_21
M_A DQ22	BB41	SA_DQ_22
M_A DQ23	BC40	SA_DQ_23
M_A DQ24	AY37	SA_DQ_24
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M_A DQ26	AV37	SA_DQ_26
M_A DQ27	AT36	SA_DQ_27
M_A DQ28	AY38	SA_DQ_28
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M_A DQ39	BC12	SA_DQ_39
M_A DQ40	BB9	SA_DQ_40
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M_A DQ42	AU10	SA_DQ_42
M_A DQ43	AV9	SA_DQ_43
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M_A DQ48	AV7	SA_DQ_48
M_A DQ49	AT9	SA_DQ_49
M_A DQ50	AN8	SA_DQ_50
M_A DQ51	AU5	SA_DQ_51
M_A DQ52	AU6	SA_DQ_52
M_A DQ53	AT5	SA_DQ_53
M_A DQ54	AN10	SA_DQ_54
M_A DQ55	AM11	SA_DQ_55
M_A DQ56	AM5	SA_DQ_56
M_A DQ57	AM5	SA_DQ_57
M_A DQ58	AJ9	SA_DQ_58
M_A DQ59	AJ8	SA_DQ_59
M_A DQ60	AN12	SA_DQ_60
M_A DQ61	AM13	SA_DQ_61
M_A DQ62	AJ11	SA_DQ_62
M_A DQ63	AJ12	SA_DQ_63

CANTIGA

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21 M_A_BS0 14
BG18 M_A_BS1 14
AT25 M_A_BS2 14
BB20 M_A_RAS# 14
BD20 M_A_CAS# 14
AY20 M_A_WE# 14

AM37 M_A_DM0 M_A_DM[7..0] 14
AT41 M_A_DM1
AY41 M_A_DM2
AU39 M_A_DM3
BB12 M_A_DM4
AY6 M_A_DM5
AT7 M_A_DM6
AJ5 M_A_DM7

AJ44 M_A_DQS0 M_A_DQS[7..0] 14
AT44 M_A_DQS1
BA43 M_A_DQS2
BC37 M_A_DQS3
AW12 M_A_DQS4
BC8 M_A_DQS5
AU8 M_A_DQS6
AM7 M_A_DQS7
AJ43 M_A_DQS#0 M_A_DQS#[7..0] 14
AT43 M_A_DQS#1
BA44 M_A_DQS#2
BD37 M_A_DQS#3
AY12 M_A_DQS#4
BD8 M_A_DQS#5
AU9 M_A_DQS#6
AM8 M_A_DQS#7

BA21 M_A_A0 M_A_A[0..14] 14
BC24 M_A_A1
BG24 M_A_A2
BH24 M_A_A3
BG25 M_A_A4
BA24 M_A_A5
BD24 M_A_A6
BG27 M_A_A7
BF25 M_A_A8
AW24 M_A_A9
BC21 M_A_A10
BG26 M_A_A11
BH26 M_A_A12
BH17 M_A_A13
AY25 M_A_A14

15 M_B_DQ[63..0]

M_B DQ0	AK47	SB_DQ_0
M_B DQ1	AH46	SB_DQ_1
M_B DQ2	AP47	SB_DQ_2
M_B DQ3	AP46	SB_DQ_3
M_B DQ4	AJ46	SB_DQ_4
M_B DQ5	AJ48	SB_DQ_5
M_B DQ6	AM48	SB_DQ_6
M_B DQ7	AP48	SB_DQ_7
M_B DQ8	AU47	SB_DQ_8
M_B DQ9	AJ46	SB_DQ_9
M_B DQ10	BA48	SB_DQ_10
M_B DQ11	AY48	SB_DQ_11
M_B DQ12	AT47	SB_DQ_12
M_B DQ13	AR47	SB_DQ_13
M_B DQ14	BA47	SB_DQ_14
M_B DQ15	BC47	SB_DQ_15
M_B DQ16	BC46	SB_DQ_16
M_B DQ17	BC44	SB_DQ_17
M_B DQ18	BG43	SB_DQ_18
M_B DQ19	BF43	SB_DQ_19
M_B DQ20	BE43	SB_DQ_20
M_B DQ21	BC41	SB_DQ_21
M_B DQ22	BE40	SB_DQ_22
M_B DQ23	BF41	SB_DQ_23
M_B DQ24	BG38	SB_DQ_24
M_B DQ25	BF38	SB_DQ_25
M_B DQ26	BH35	SB_DQ_26
M_B DQ27	BG35	SB_DQ_27
M_B DQ28	BH39	SB_DQ_28
M_B DQ29	BG39	SB_DQ_29
M_B DQ30	BG34	SB_DQ_30
M_B DQ31	BH34	SB_DQ_31
M_B DQ32	BH14	SB_DQ_32
M_B DQ33	BG12	SB_DQ_33
M_B DQ34	BH11	SB_DQ_34
M_B DQ35	BG8	SB_DQ_35
M_B DQ36	BH12	SB_DQ_36
M_B DQ37	BF11	SB_DQ_37
M_B DQ38	BF8	SB_DQ_38
M_B DQ39	BG7	SB_DQ_39
M_B DQ40	BC8	SB_DQ_40
M_B DQ41	AY3	SB_DQ_41
M_B DQ42	AY1	SB_DQ_42
M_B DQ43	BF6	SB_DQ_43
M_B DQ44	BF5	SB_DQ_44
M_B DQ45	BA1	SB_DQ_45
M_B DQ46	BD3	SB_DQ_46
M_B DQ47	AV2	SB_DQ_47
M_B DQ48	AU3	SB_DQ_48
M_B DQ49	AR3	SB_DQ_49
M_B DQ50	AN2	SB_DQ_50
M_B DQ51	AY2	SB_DQ_51
M_B DQ52	AP3	SB_DQ_52
M_B DQ53	AR1	SB_DQ_53
M_B DQ54	AL1	SB_DQ_54
M_B DQ55	AL2	SB_DQ_55
M_B DQ56	AJ1	SB_DQ_56
M_B DQ57	AH1	SB_DQ_57
M_B DQ58	AM2	SB_DQ_58
M_B DQ59	AM3	SB_DQ_59
M_B DQ60	AH3	SB_DQ_60
M_B DQ61	AH3	SB_DQ_61
M_B DQ62	AJ3	SB_DQ_62
M_B DQ63	AJ3	SB_DQ_63

CANTIGA

DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2
SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BC16 M_B_BS0 15
BB17 M_B_BS1 15
BB33 M_B_BS2 15
AU17 M_B_RAS# 15
BG16 M_B_CAS# 15
BF14 M_B_WE# 15

AM47 M_B_DM0 M_B_DM[7..0] 15
AY47 M_B_DM1
BD40 M_B_DM2
BF35 M_B_DM3
BG11 M_B_DM4
BA3 M_B_DM5
AP1 M_B_DM6
AK2 M_B_DM7

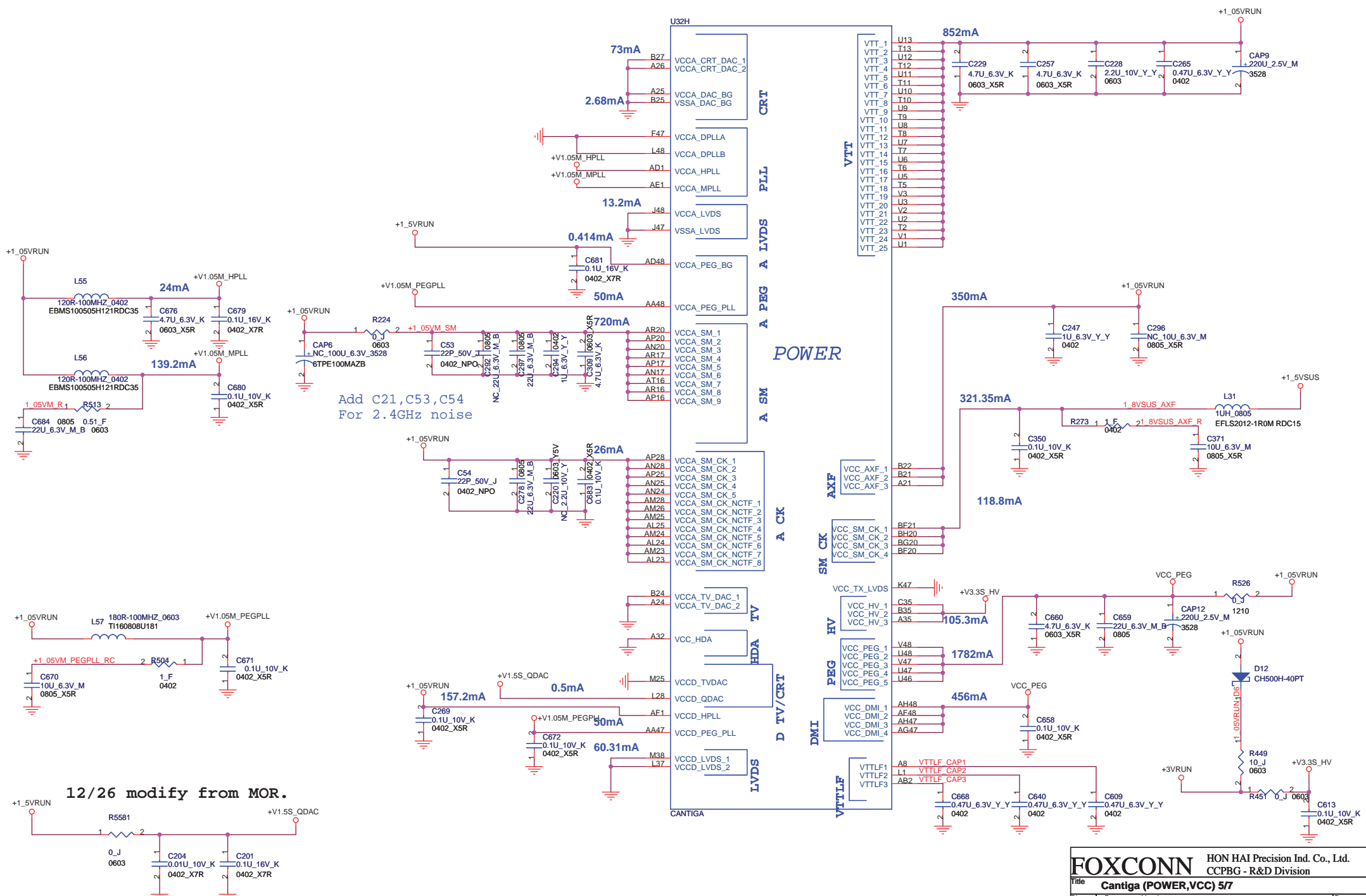
AL47 M_B_DQS0 M_B_DQS[7..0] 15
AV48 M_B_DQS1
BG41 M_B_DQS2
BG37 M_B_DQS3
BH9 M_B_DQS4
BB2 M_B_DQS5
AU1 M_B_DQS6
AN6 M_B_DQS7
AL46 M_B_DQS#0 M_B_DQS#[7..0] 15
AV47 M_B_DQS#1
BH41 M_B_DQS#2
BH37 M_B_DQS#3
BG9 M_B_DQS#4
BC2 M_B_DQS#5
AT2 M_B_DQS#6
AN5 M_B_DQS#7

AV17 M_B_A0 M_B_A[0..14] 15
BA25 M_B_A1
BC25 M_B_A2
AU25 M_B_A3
AW25 M_B_A4
BB28 M_B_A5
AU28 M_B_A6
AW28 M_B_A7
AT33 M_B_A8
BD33 M_B_A9
BB16 M_B_A10
AW33 M_B_A11
AY33 M_B_A12
BH15 M_B_A13
AU33 M_B_A14

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Title: **Cantiga (DDRIII) 4/7**

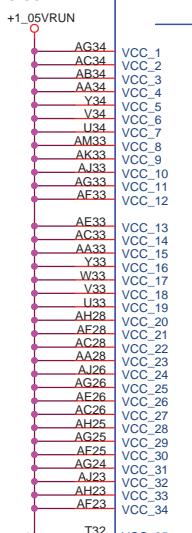
Size A3	Document Number M870-1-01	Rev 1.0
Date: Monday, July 27, 2009	Sheet 10 of 75	



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Cantiga (POWER, VCC) 5/7			
Title	Cantiga (POWER, VCC) 5/7		
Size	Document Number	Rev	
A3	M870-1-01	1.0	
Date:	Monday, July 27, 2009	Sheet	11 of 75

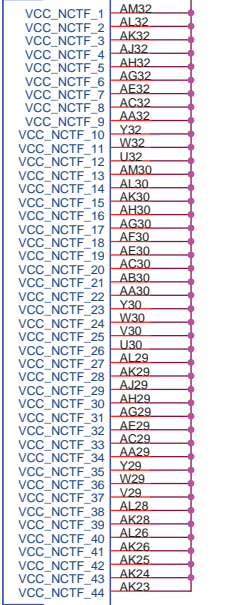
3.06A



VCC CORE

POWER

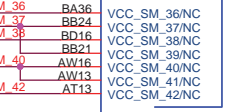
VCC NCTF



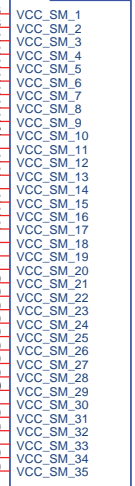
+1_05VRUN



3A +1_5VSUS



U32G

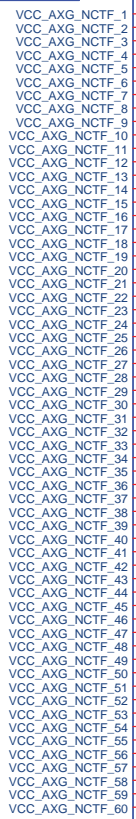


POWER

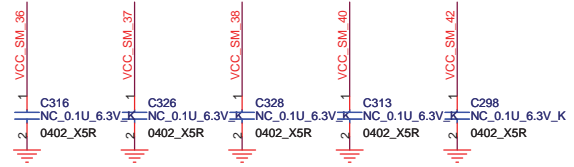
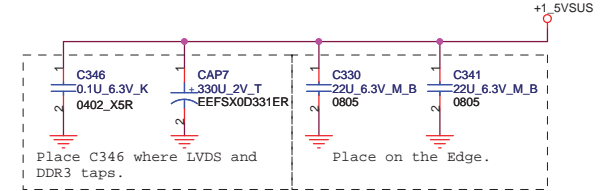
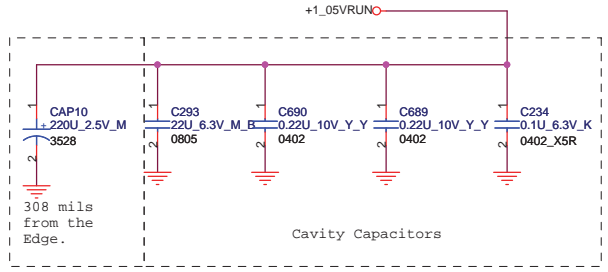
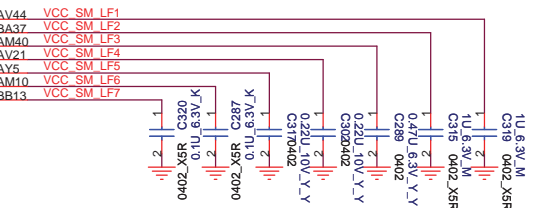
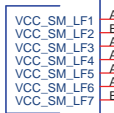
VCC SM

VCC GFX NCTF

VCC GFX



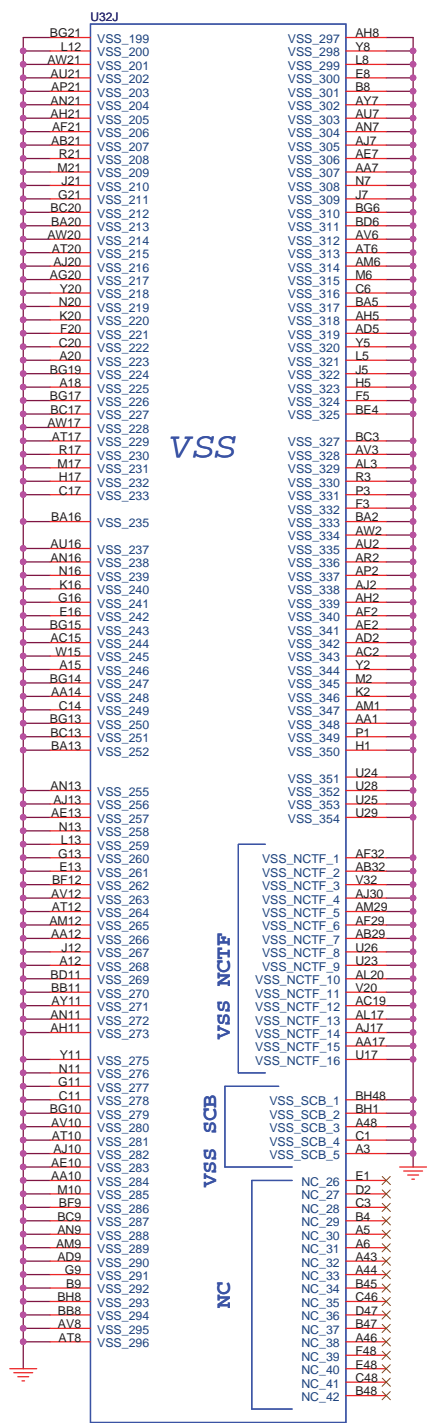
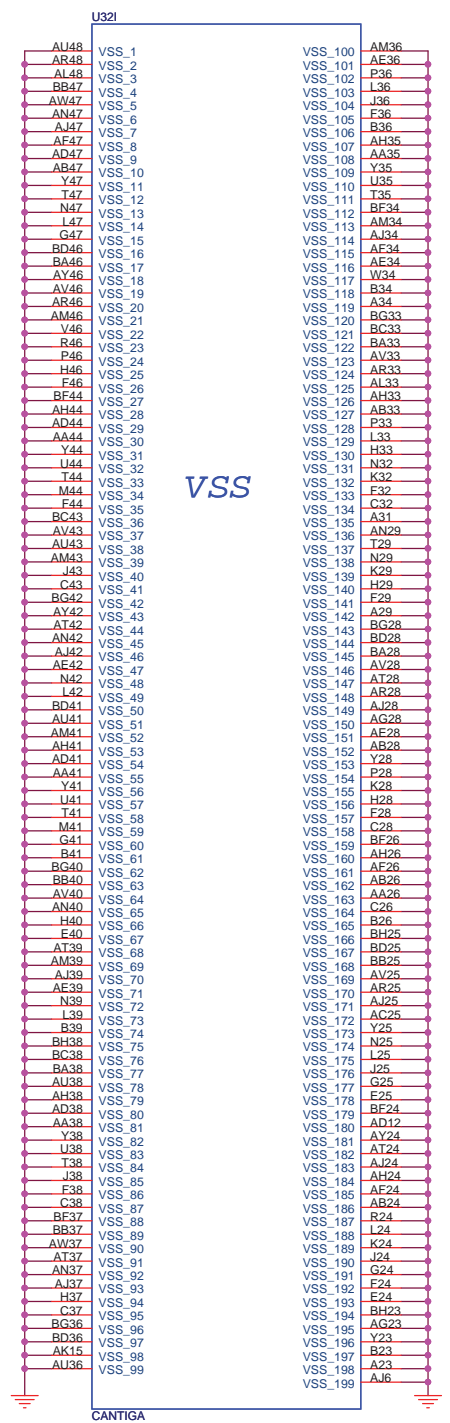
VCC SM I/F



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Title: **Cantiga (VCC CORE) 6/7**

Size A3	Document Number M870-1-01	Rev 1.0
Date: Monday, July 27, 2009	Sheet 12	of 75



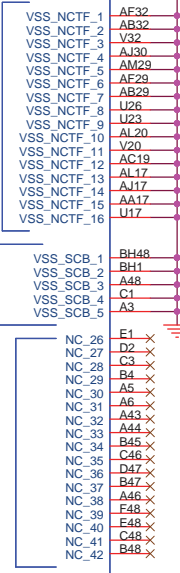
VSS

VSS

VSS NCTF

VSS SCB

NC

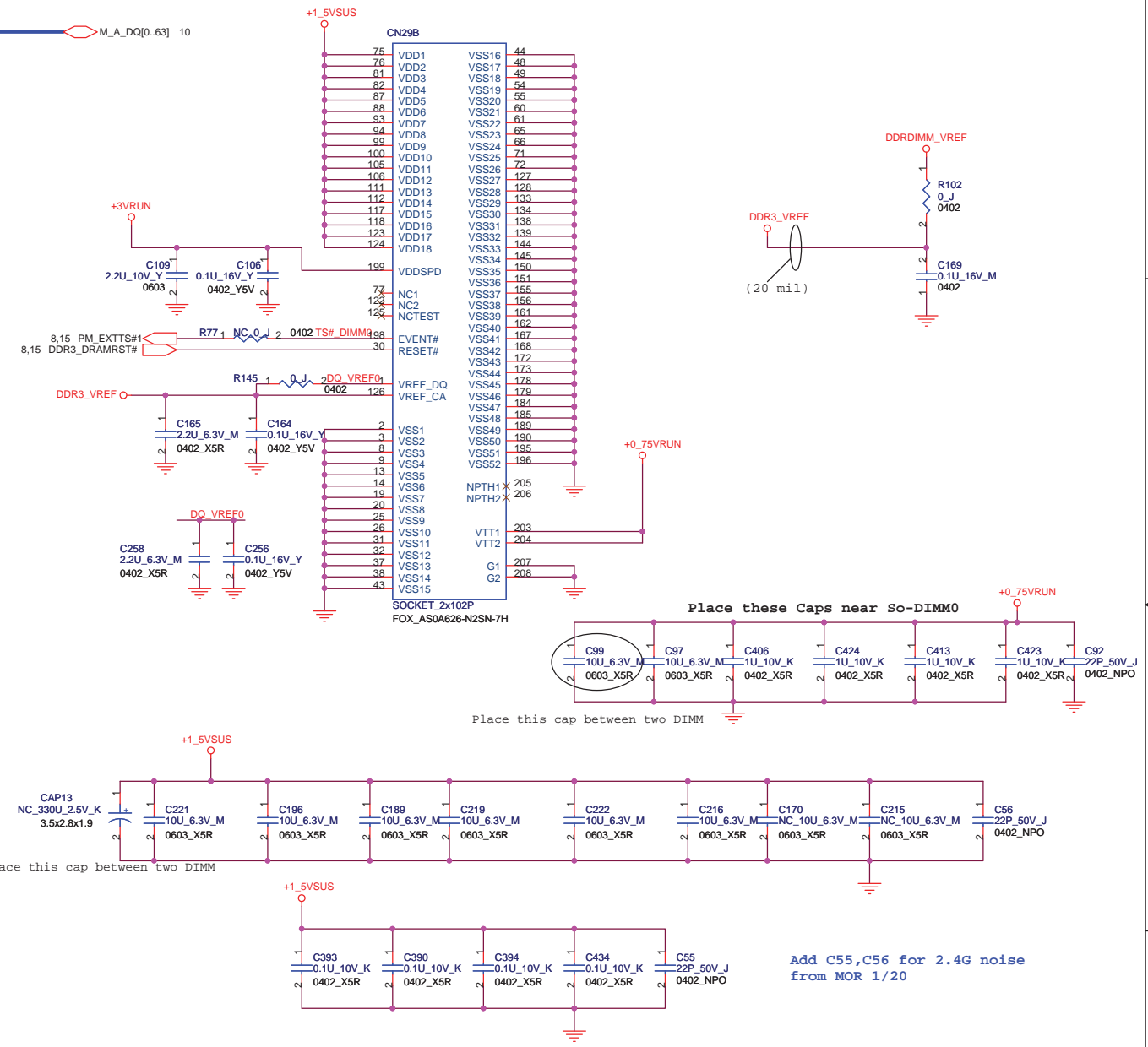
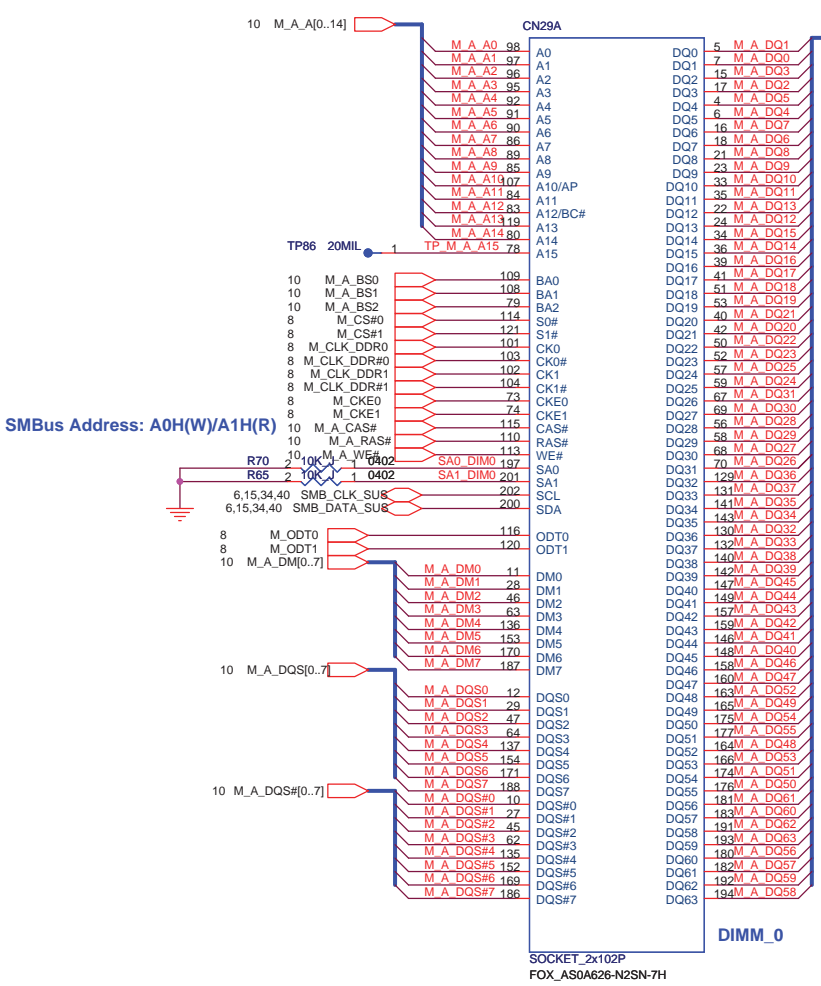


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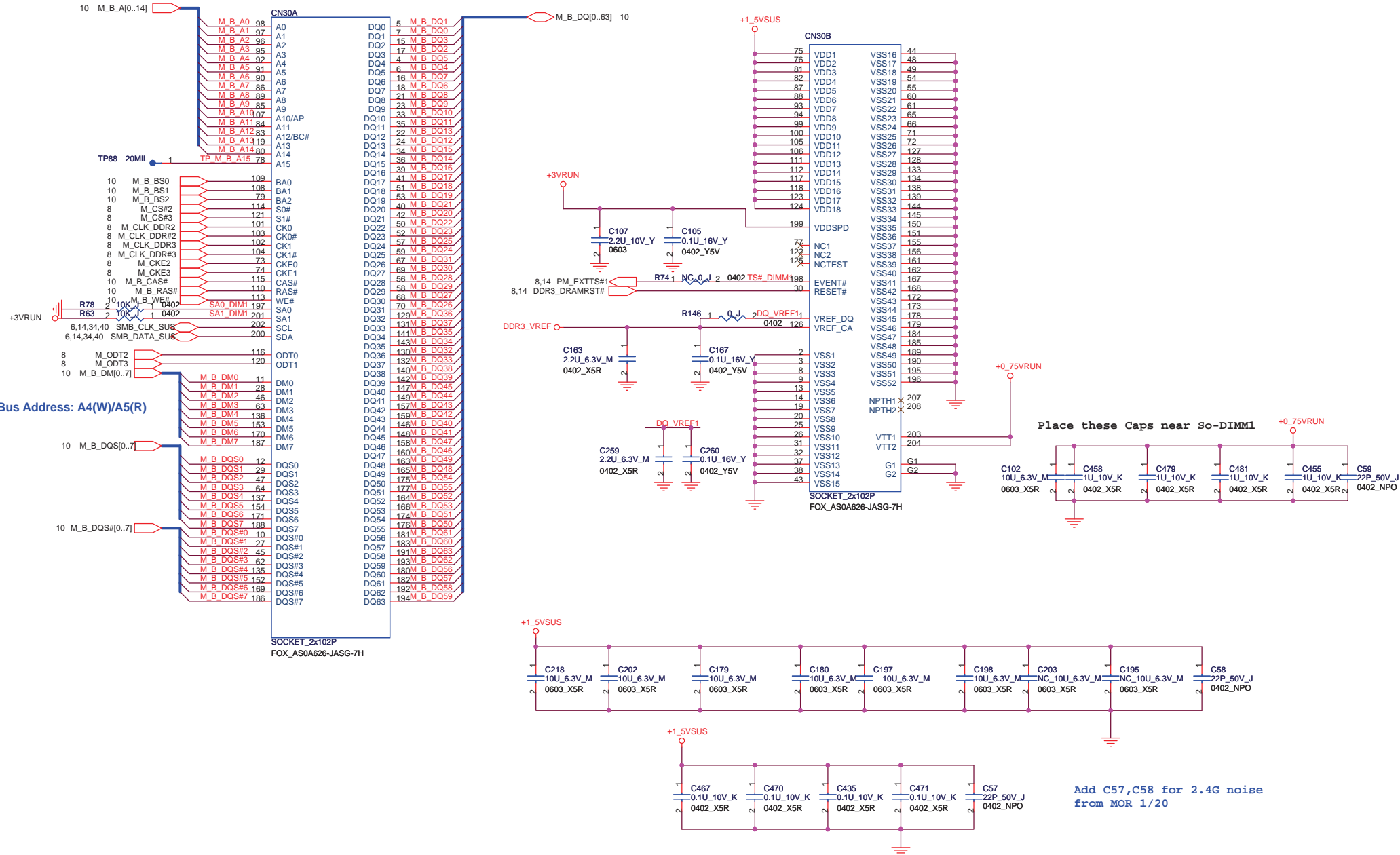
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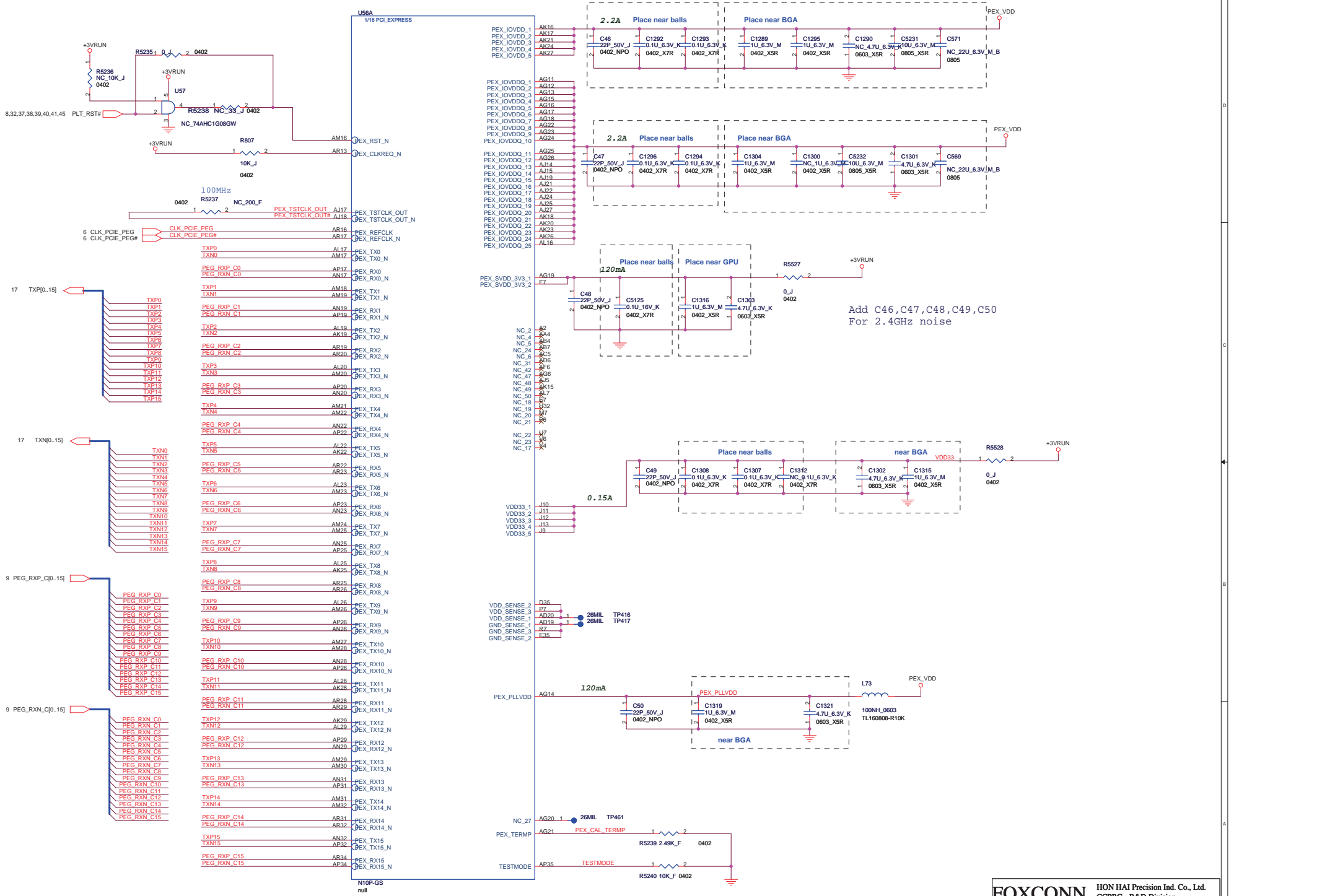
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Date: Monday, July 27, 2009	Sheet: 13	of: 75

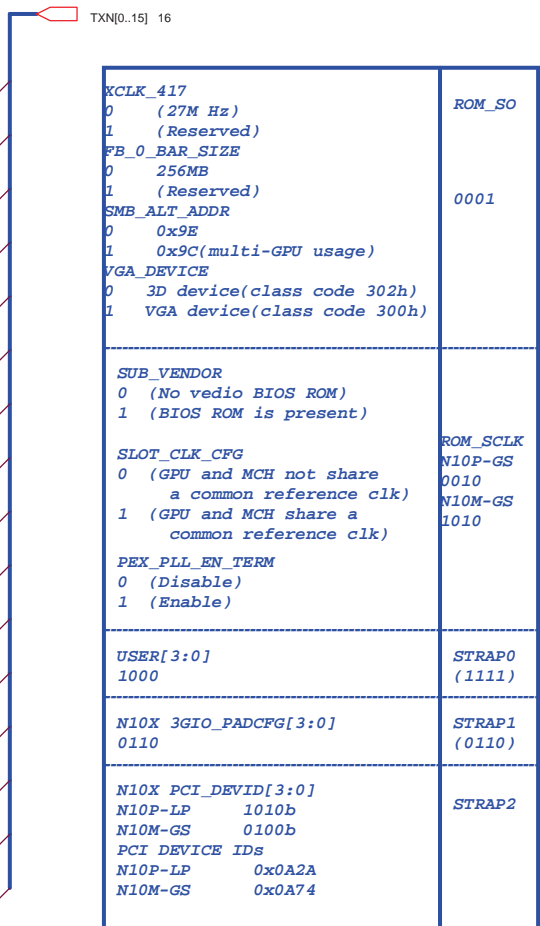
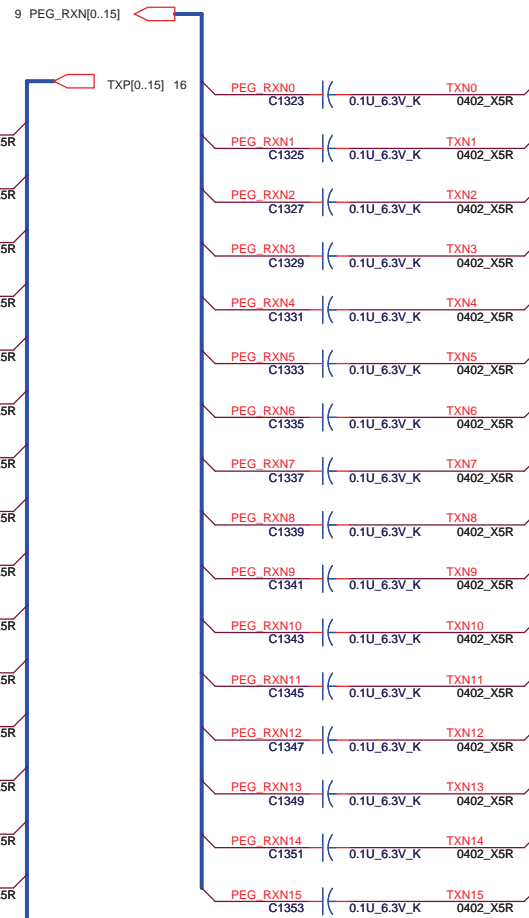
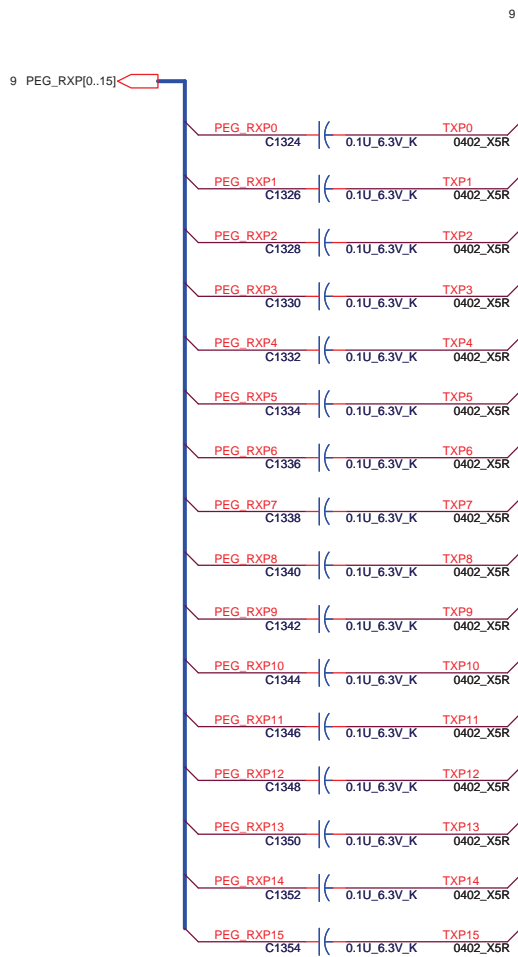
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<http://laptop-motherboard-schematic.blogspot.com/>







```

XCLK_417
0 (27M Hz)
1 (Reserved)
FB_0_BAR_SIZE
0 256MB
1 (Reserved)
SMB_ALT_ADDR
0 0x9E
1 0x9C(multi-GPU usage)
VGA_DEVICE
0 3D device(class code 302h)
1 VGA device(class code 300h)

SUB_VENDOR
0 (No video BIOS ROM)
1 (BIOS ROM is present)

SLOT_CLK_CFG
0 (GPU and MCH not share a common reference clk)
1 (GPU and MCH share a common reference clk)

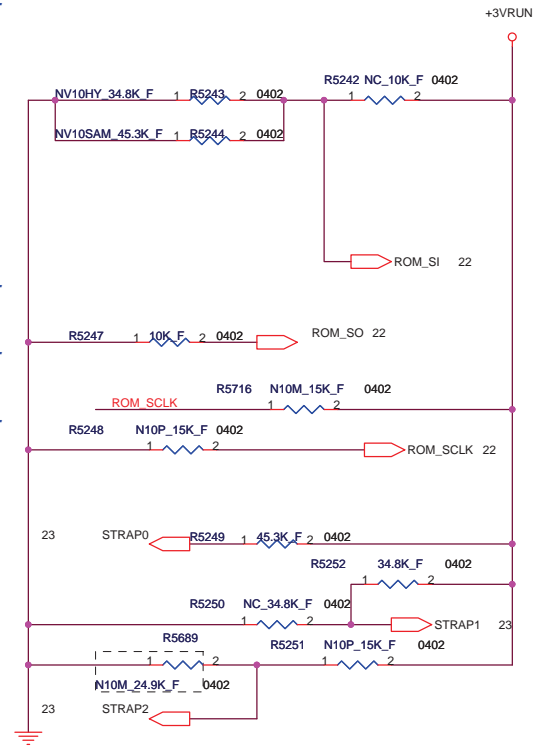
PEX_PLL_EN_TERM
0 (Disable)
1 (Enable)

USER[3:0]
1000 STRAP0 (1111)

N10X_3GIO_PADCFG[3:0]
0110 STRAP1 (0110)

N10X_PCI_DEVID[3:0]
N10P-LP 1010b
N10M-GS 0100b
PCI_DEVICE_IDS
N10P-LP 0x0A2A
N10M-GS 0x0A74
  
```

0000 64-bit Reserved
 0010 32Mx32 GDDR3 - 136 ball 64-bit Hynix - 35K pul Low.
 0011 32Mx32 GDDR3 - 136 ball 64-bit Samsung- 45K pull Low



Logical Strap bit Mapping

Resistor values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_Si	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-01176-001 v01 secured>

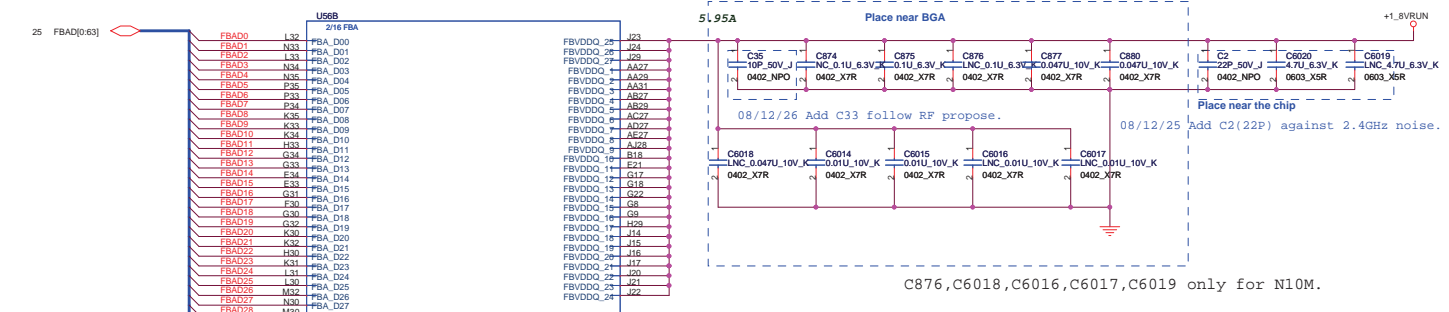
<http://laptop-motherboard-schematic.blogspot.com/>

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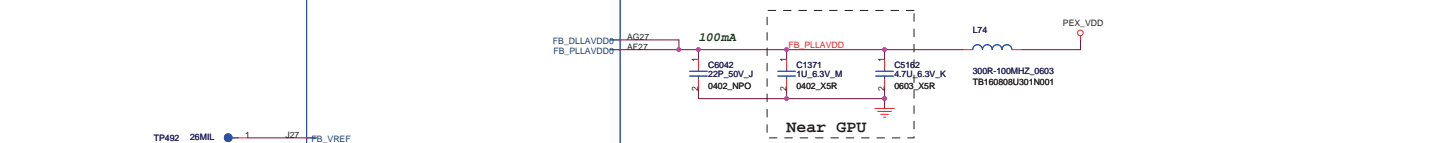
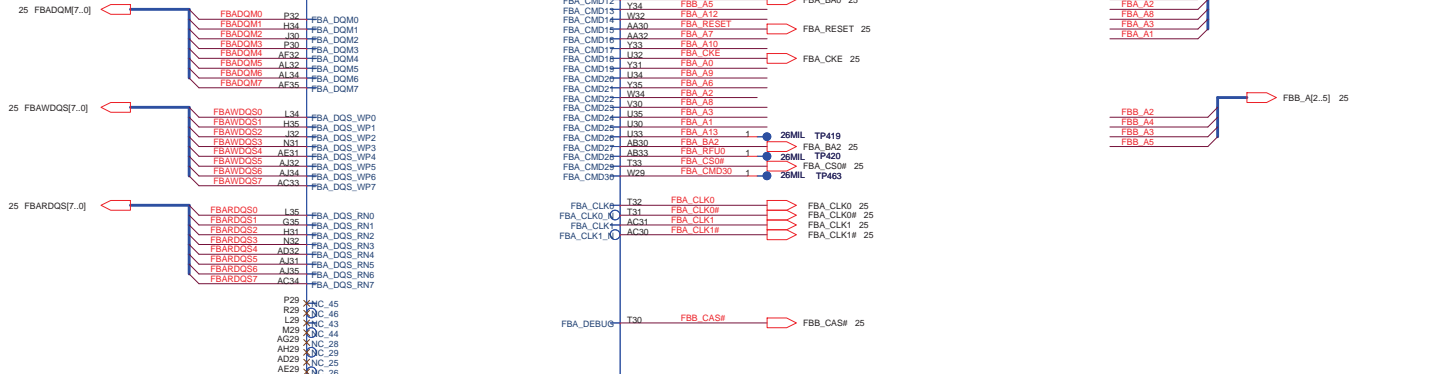
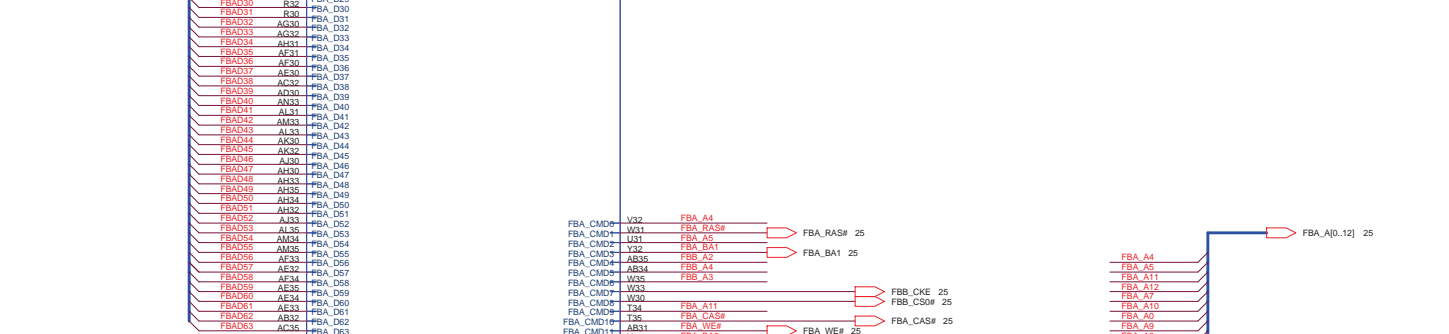
Title: **VGA (PCI-EXPRESS/STRAP) 2 OF 9**

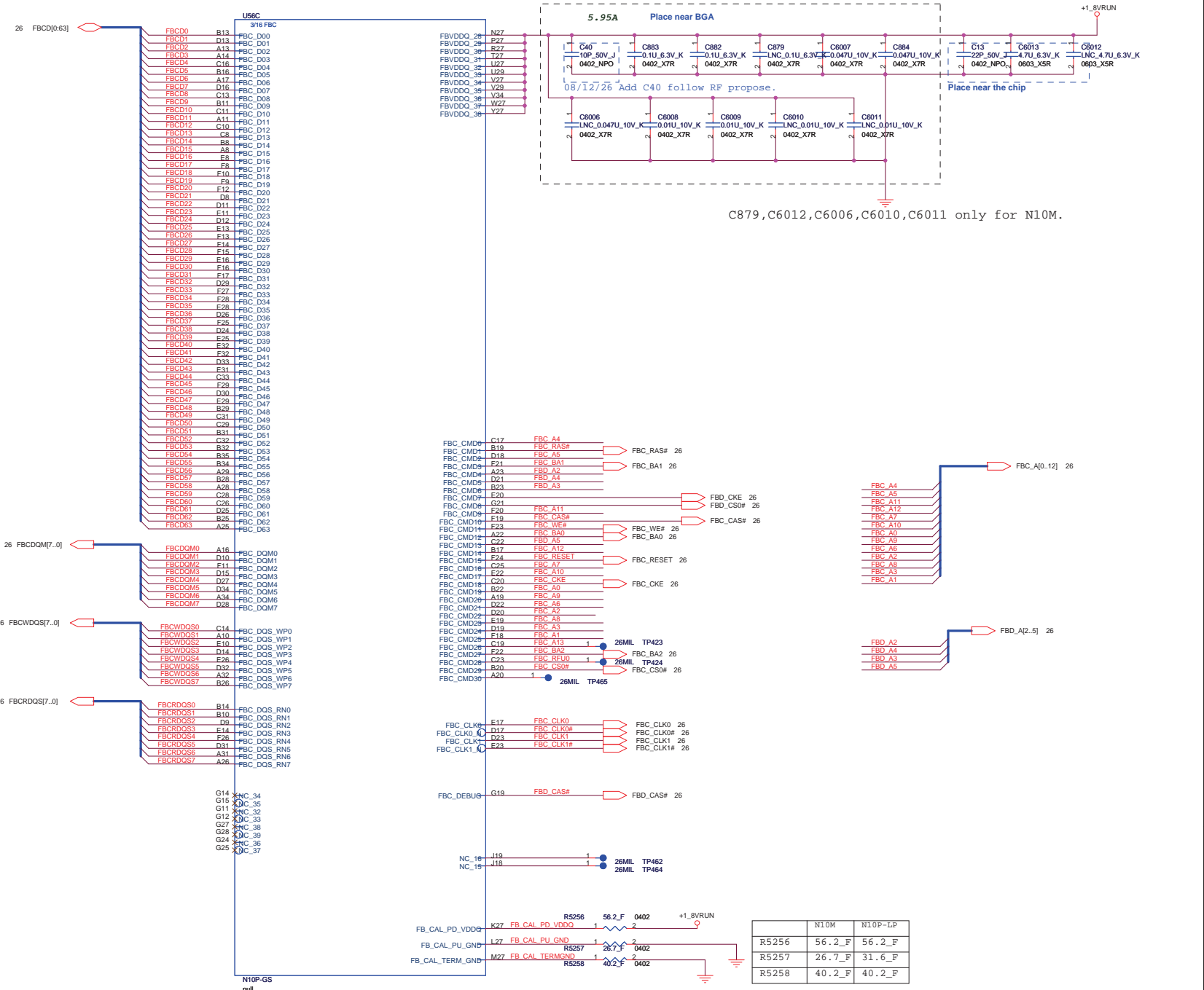
Size: Document Number
 A3: **M870-1-01** Rev: **1.0**

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C876,C6018,C6016,C6017,C6019 only for N10M.





C879,C6012,C6006,C6010,C6011 only for N10M.

R5256	N10M	N10P-LP
R5256	56.2_F	56.2_F
R5257	26.7_F	31.6_F
R5258	40.2_F	40.2_F

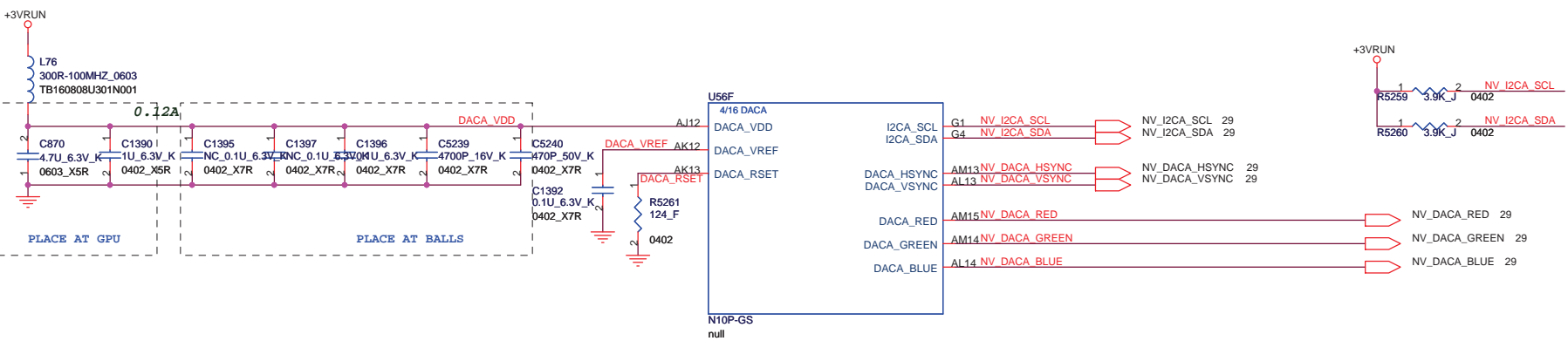
Place components close to the GPU

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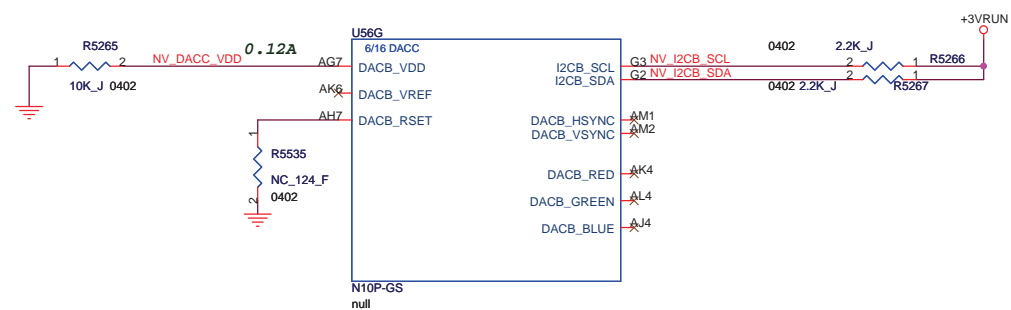
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Size: **M87** Document Number: **11** Rev: **1.0**

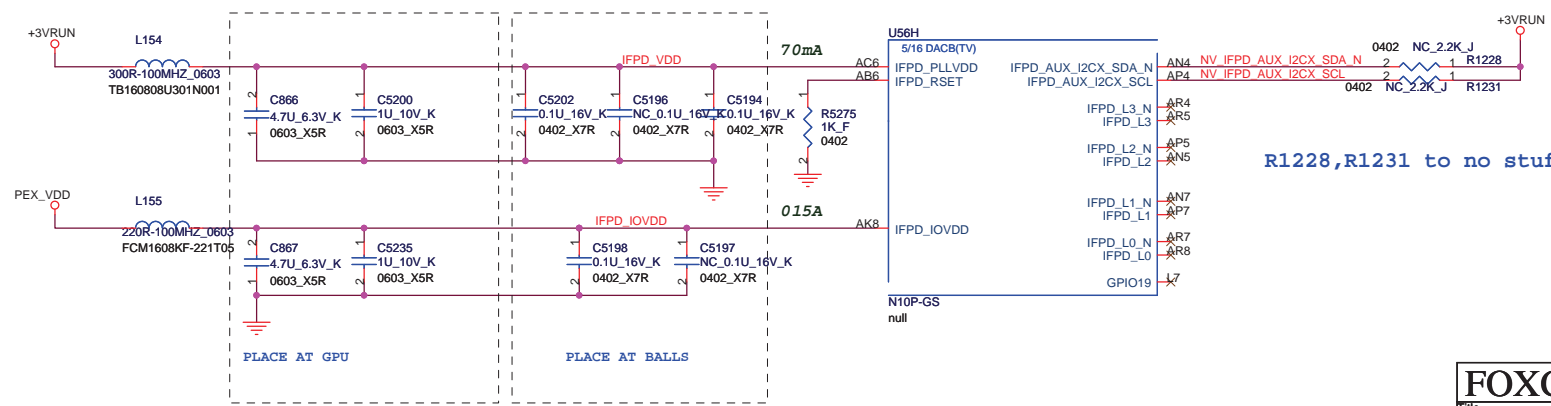
Rev: **1.0** Date: **2012.07.20** Sheet: **10** of **16**



R5262, R5263 and R5264 remove ---MOR 2/27



DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCLK	SCL
	VGA-DDCATA	SDA



R1228, R1231 to no stuff ---MOR 5/25

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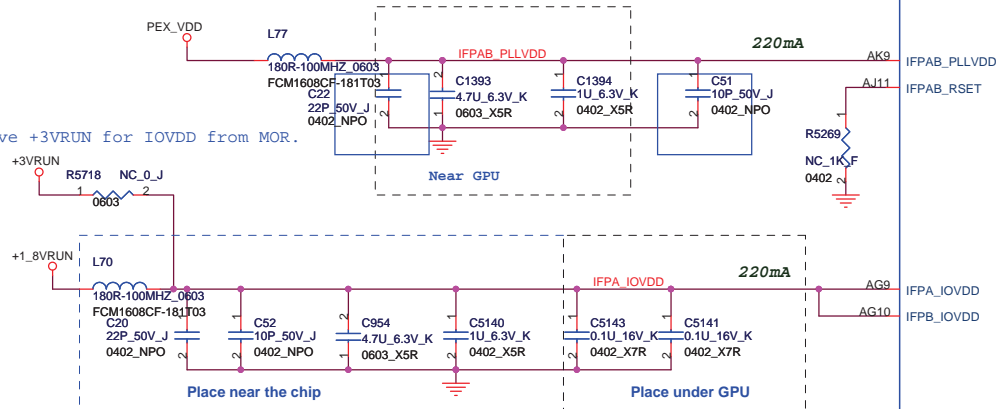
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Size: Document Number **M870-1-01** Rev **1.0**

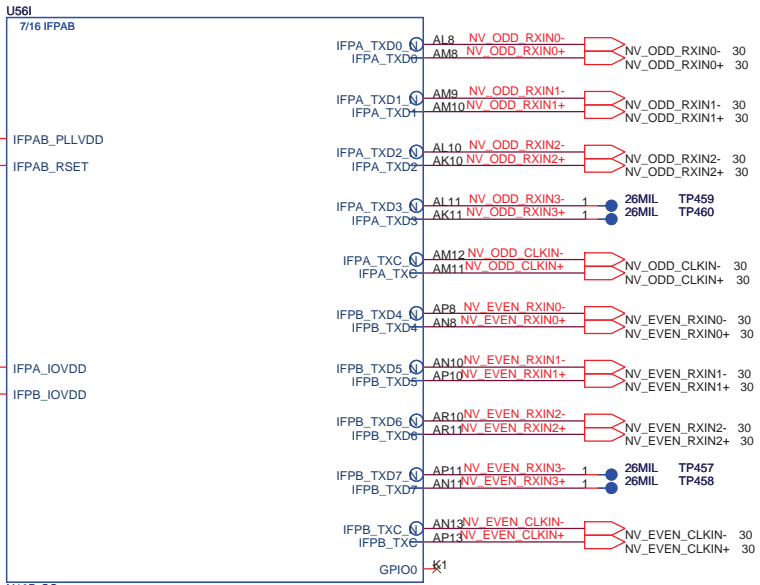
Date: Monday, July 27, 2009 Sheet 20 of 75

08/12/26 Add C51,C52 10p follow RF propose.

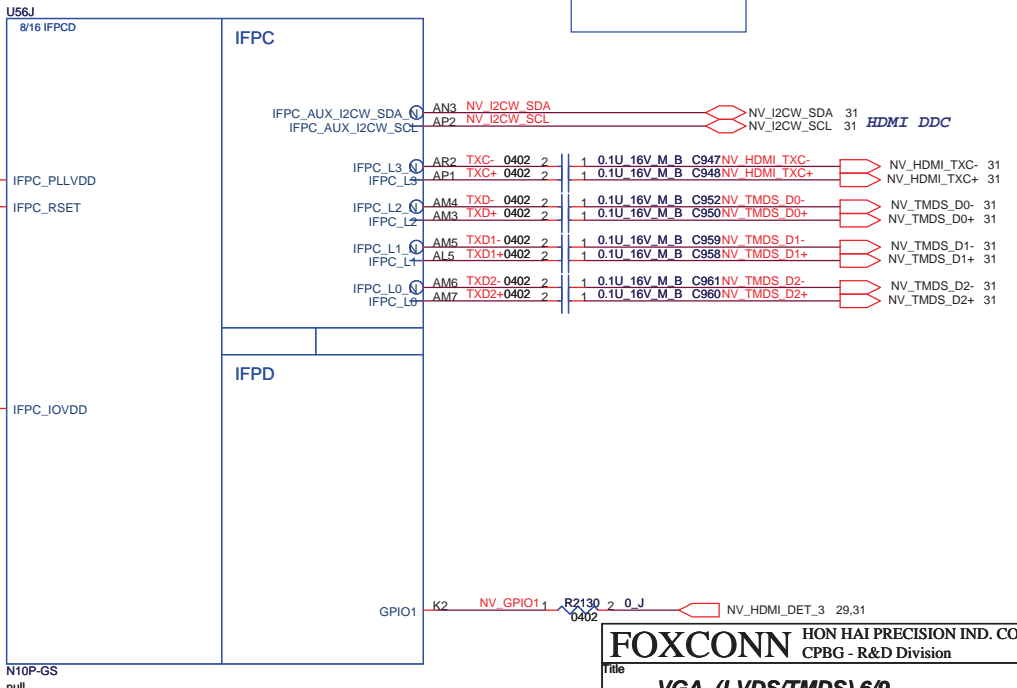
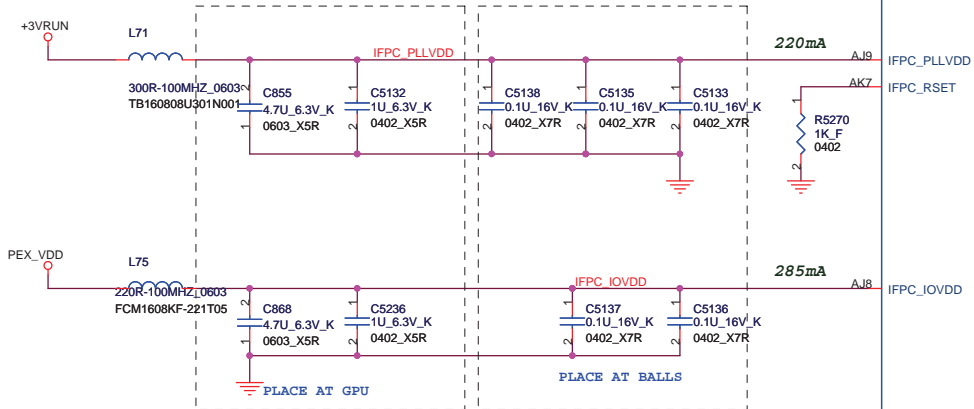
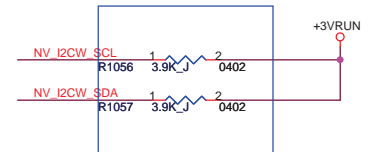
09/02/05 Reserve +3VRUN for IOVDD from MOR.

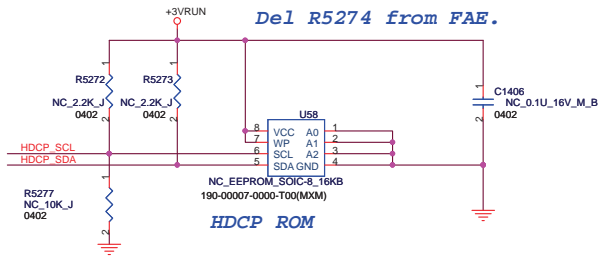


08/12/25 Add C20,C22 against 2.4GHz noise.

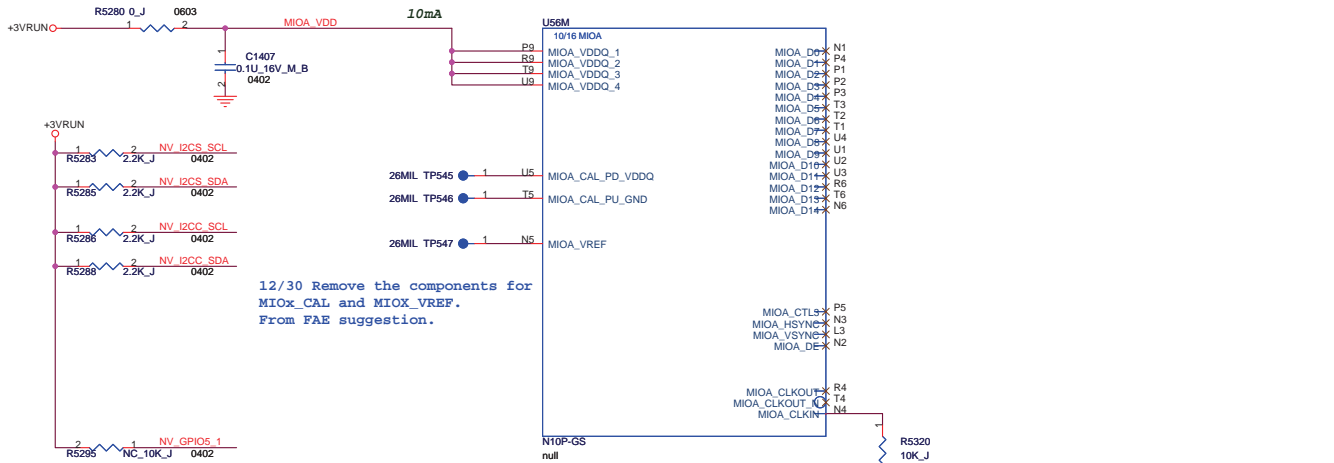
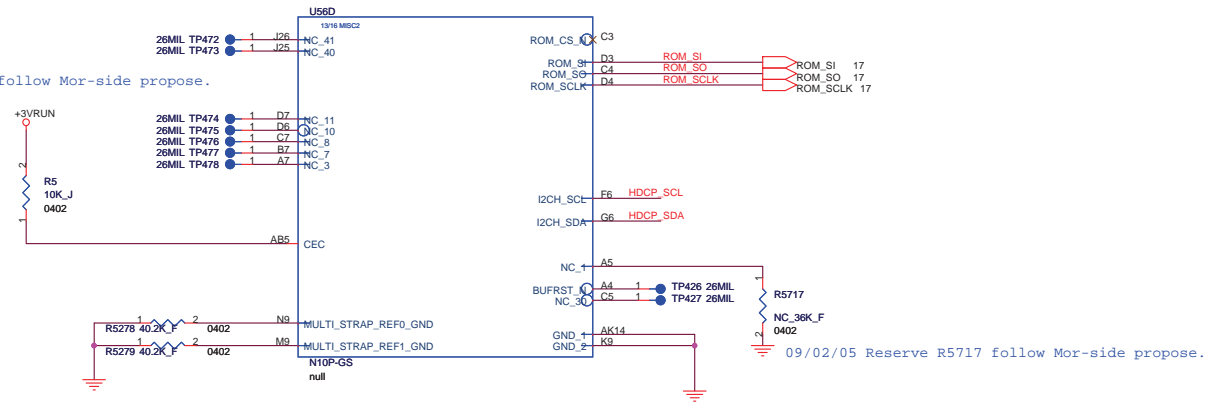


08/12/22 Change R1056,R1057 from 2.2K to 3.9K follow Mor-side propose.



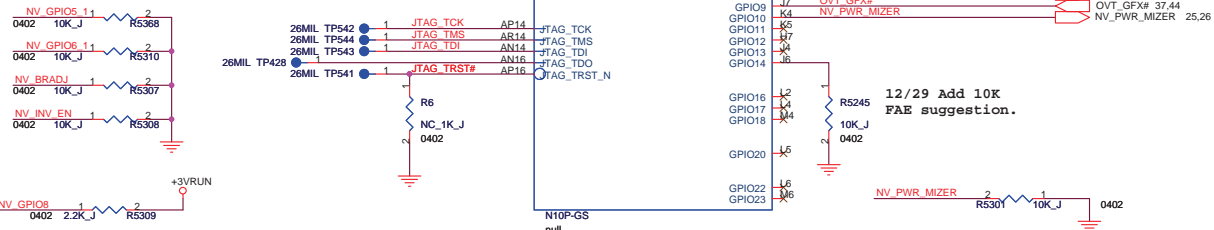


08/12/26 Add R5 follow Mor-side propose.



GPIO	I/O	Internal pull low	GPIO TABLE
GPIO0	I	Yes	
GPIO1	I	Yes	HDMI Hot Plug Detect 0 (HPD0) Active High
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM) Active High
GPIO3	O	No	Panel Power(LCD0_VDD) Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN) Active High
GPIO5	O	Yes	FOR Power Control NVDD 0.95V/1.05V Active High
GPIO6	O	No	reserve for NVDD adjust.
GPIO8	O	No	reserve for reset EC
GPIO9	I	No	System Power Limit Alert Input Active Low

12/29 Add R5310 10K FAE suggestion.



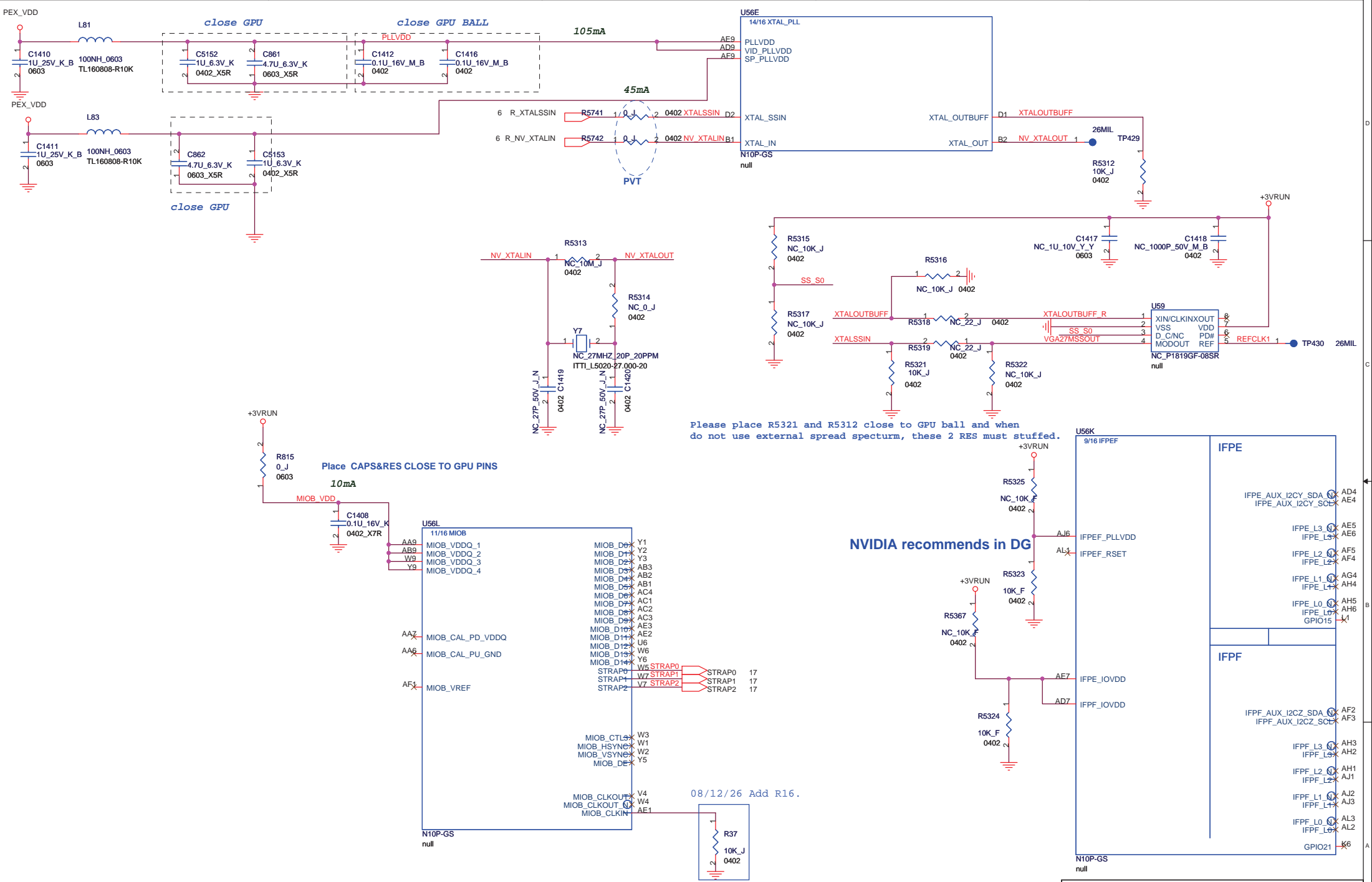
SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL I2CS_SDA	I/O	For VGA thermal I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor

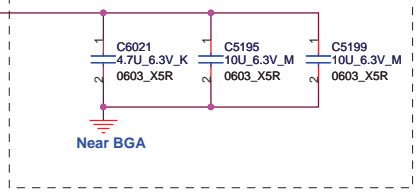
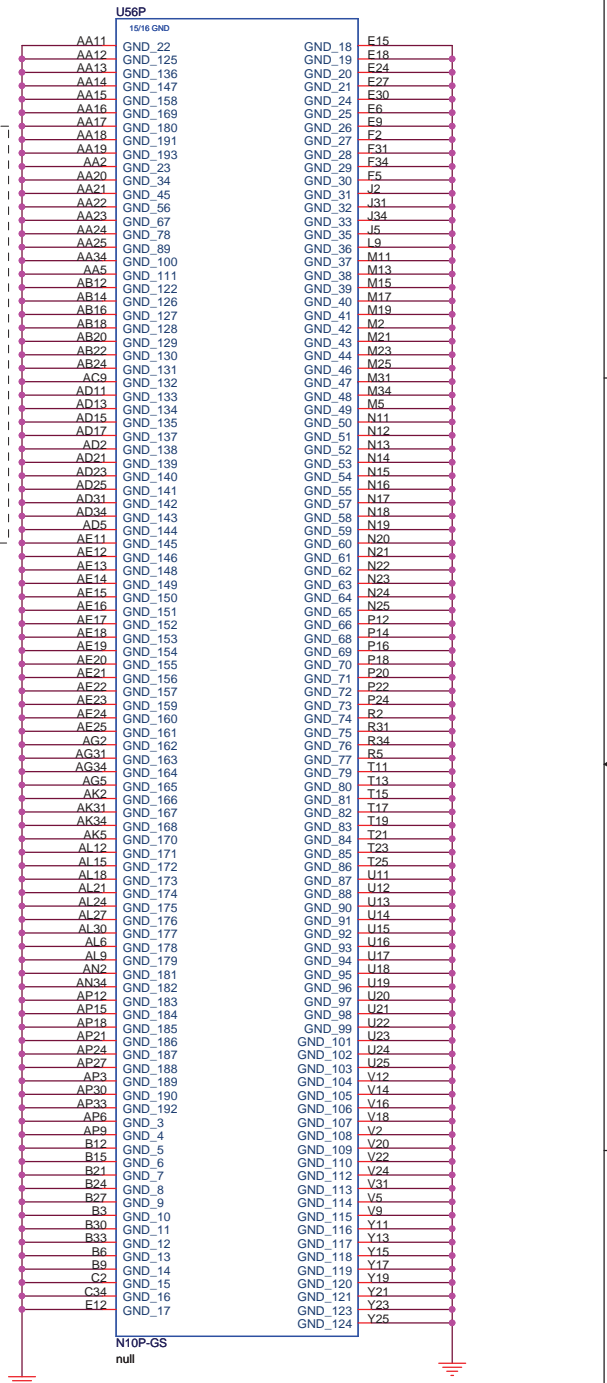
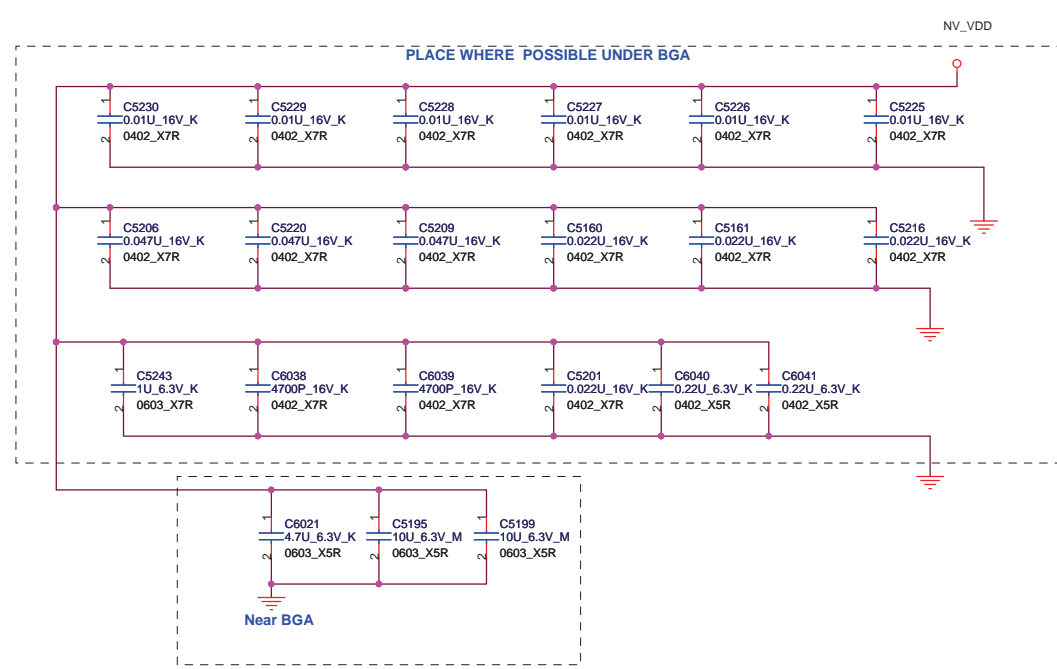
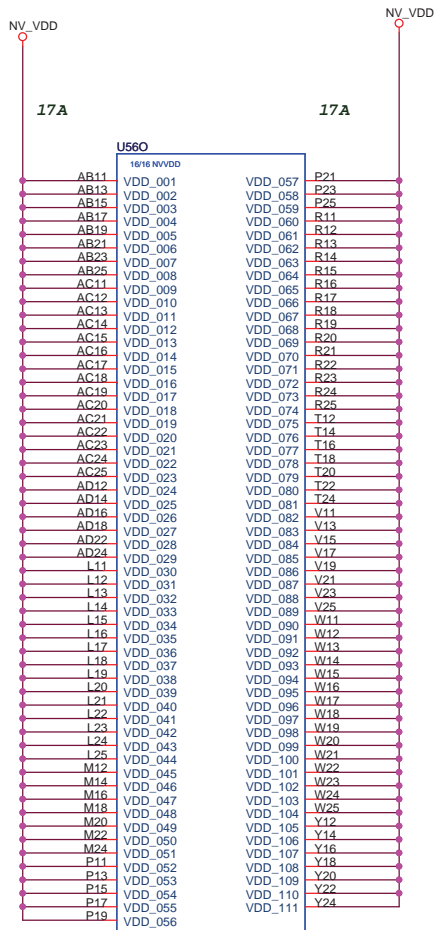
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **VGA (XTAL/GPIO) 7/9**

Size: Custom Document Number: **M870-1-01** Rev: **1.0**

Date: Monday, July 27, 2009 Sheet: 22 of 75



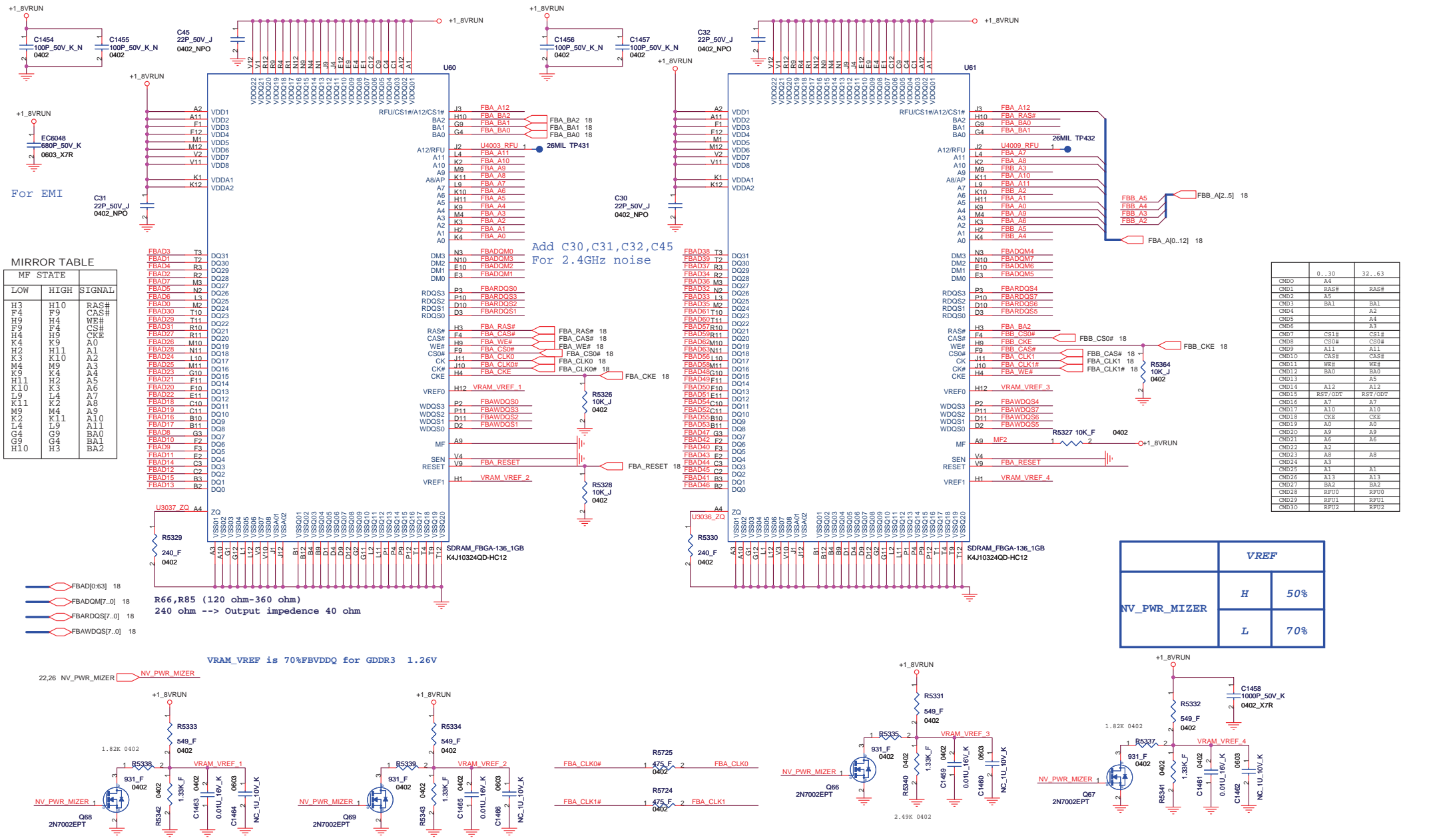


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Title: **VGA(POWER/GROUND) 9/9**

Size: Document Number
A3: **M870-1-01** Rev: **1.0**

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MIRROR TABLE

LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
H9	H4	BA1
H10	H3	BA2

	0..30	32..63
CM00	A4	
CM01	RAS#	RAS#
CM02	A5	BA1
CM03	BA1	BA1
CM04	A2	A2
CM05	A4	A4
CM06	A3	A3
CM07	CS1#	CS1#
CM08	CS0#	CS0#
CM09	A11	A11
CM10	CAS#	CAS#
CM11	WE#	WE#
CM12	BA0	BA0
CM13	A5	A5
CM14	A12	A12
CM15	RST7/ODT	RST7/ODT
CM16	A7	A7
CM17	A10	A10
CM18	CKE	CKE
CM19	A0	A0
CM20	A9	A9
CM21	A6	A6
CM22	A2	A2
CM23	A8	A8
CM24	A3	A3
CM25	A1	A1
CM26	A13	A13
CM27	B02	B02
CM28	RFU0	RFU0
CM29	RFU1	RFU1
CM30	RFU2	RFU2

VREF	
H	50%
L	70%

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

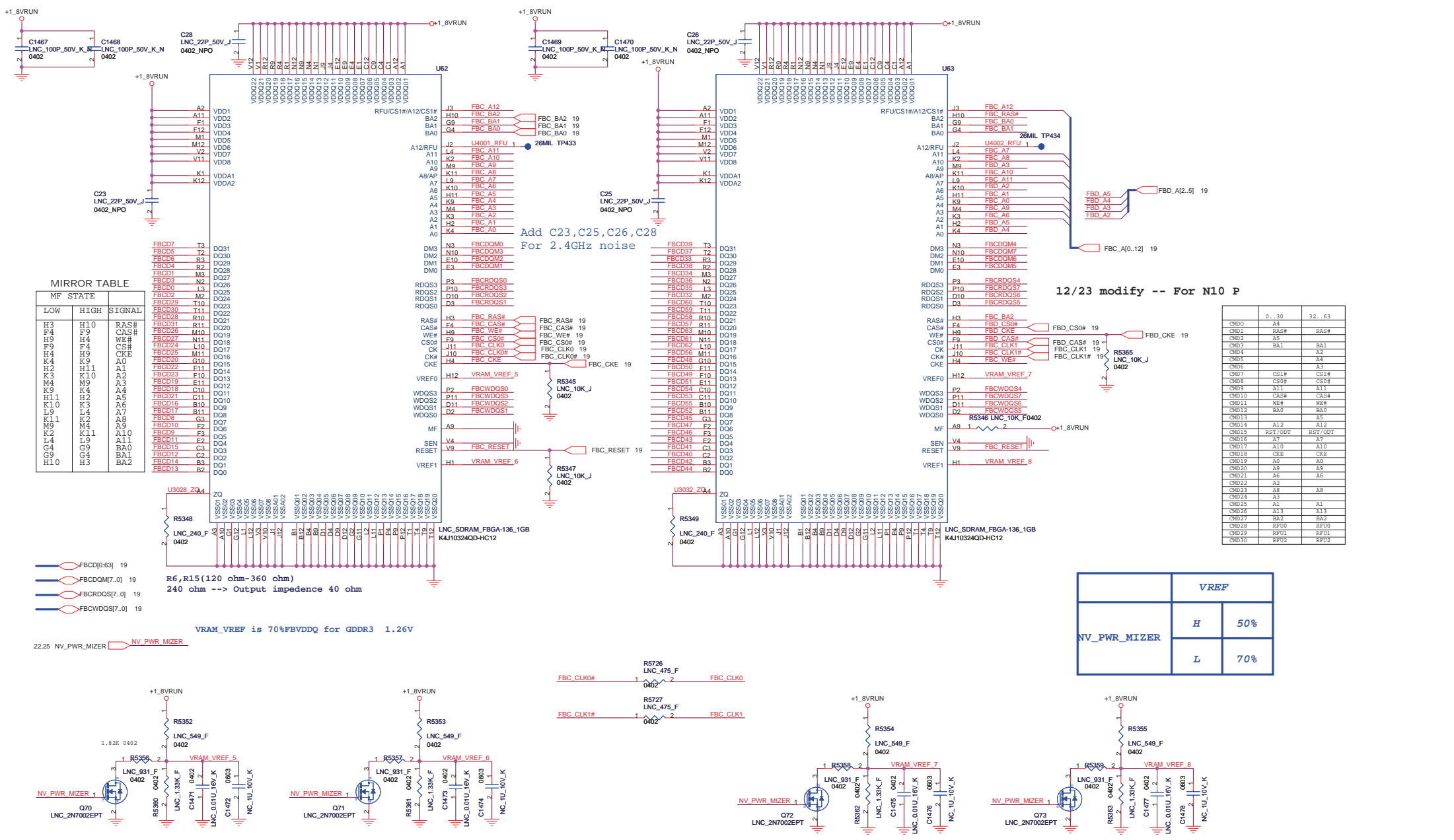
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **VRAM(GDDR)# 1/2**

Size: Document Number
Custom: **M870-1-01**

Date: Monday, July 27, 2009 Sheet 25 of 75

Rev: **1.0**



MIRROR TABLE

MF STATE	LOW	HIGH	SIGNAL
H3	H10	RAS#	CAS#
F4	F9	CAS#	WE#
H9	H4	WE#	C#
F9	F4	C#	CKE
H4	H9	CKE	FBD A5
K4	K9	A0	FBD A4
H2	H11	A1	FBD A3
K3	K10	A2	FBD A2
M4	M9	A3	FBD A1
K9	K4	A4	FBD A0
H11	H2	A5	FBD A0..12
K10	K3	A6	FBD A0..12
L9	L4	A7	FBD A0..12
K11	K2	A8	FBD A0..12
M9	M4	A9	FBD A0..12
K2	K11	A10	FBD A0..12
L4	L9	A11	FBD A0..12
G4	G9	BA0	FBD A0..12
G9	G4	BA1	FBD A0..12
H10	H3	BA2	FBD A0..12

- FBCD7 T3
- FBCD6 R3
- FBCD5 R2
- FBCD4 R2
- FBCD3 M3
- FBCD2 M2
- FBCD1 M2
- FBCD0 L3
- FBCD29 T10
- FBCD28 T10
- FBCD27 R10
- FBCD26 M10
- FBCD25 N11
- FBCD24 L10
- FBCD23 G10
- FBCD22 F11
- FBCD21 C11
- FBCD20 B10
- FBCD19 B11
- FBCD18 G3
- FBCD17 E2
- FBCD16 G3
- FBCD15 F3
- FBCD14 E2
- FBCD13 B2
- FBCD12 C2
- FBCD11 B2
- FBCD10 D2
- FBCD9 F2
- FBCD8 E2
- FBCD7 C3
- FBCD6 B3
- FBCD5 A3
- FBCD4 B3
- FBCD3 A3
- FBCD2 C2
- FBCD1 B2
- FBCD0 D2

R6, R15 (120 ohm-360 ohm)
240 ohm --> Output impedance 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

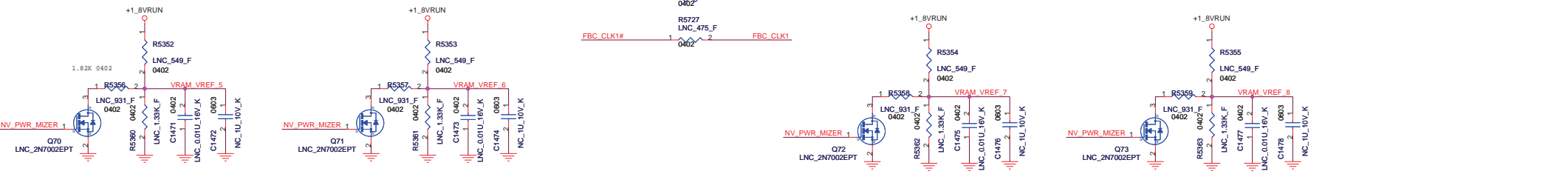
22.25 NV_PWR_MIZER NV_PWR_MIZER

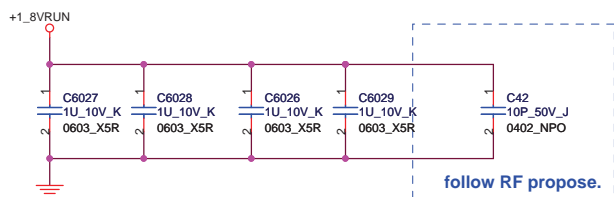
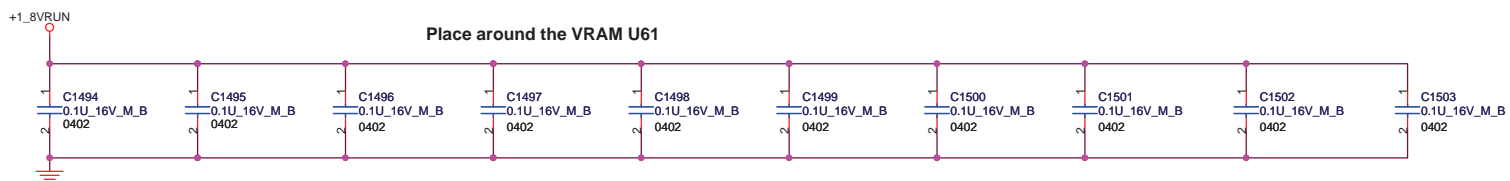
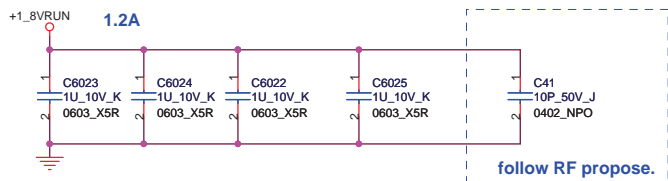
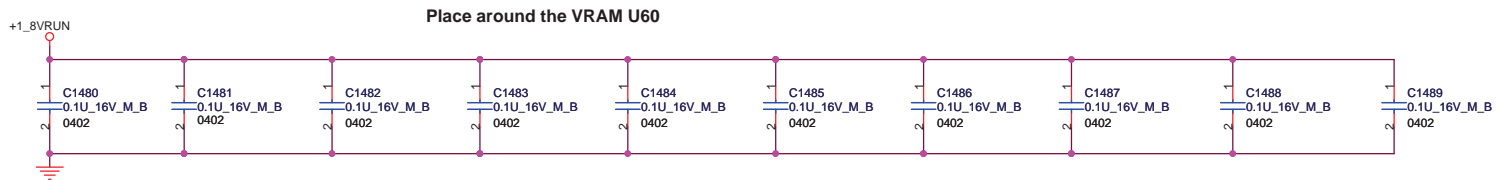
Add C23, C25, C26, C28
For 2.4GHz noise

12/23 modify -- For N10 P

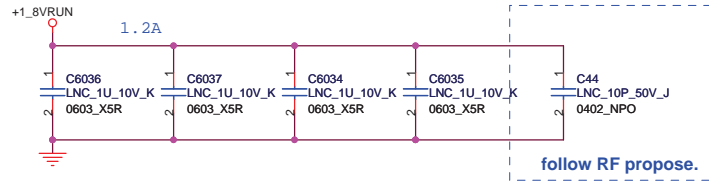
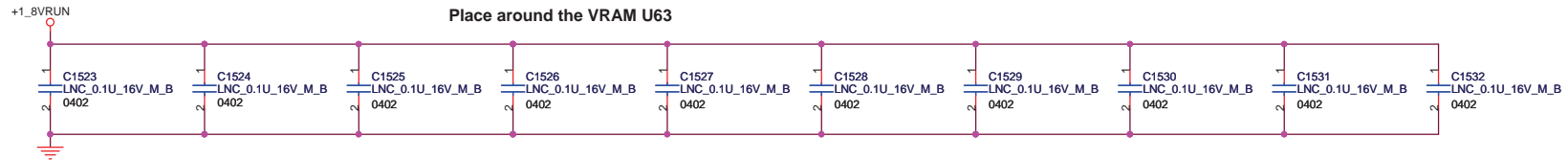
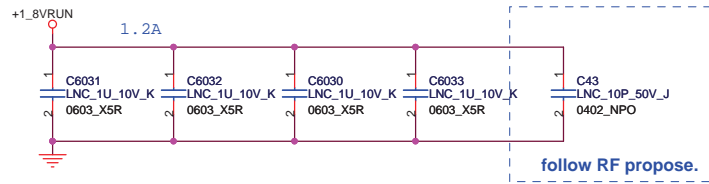
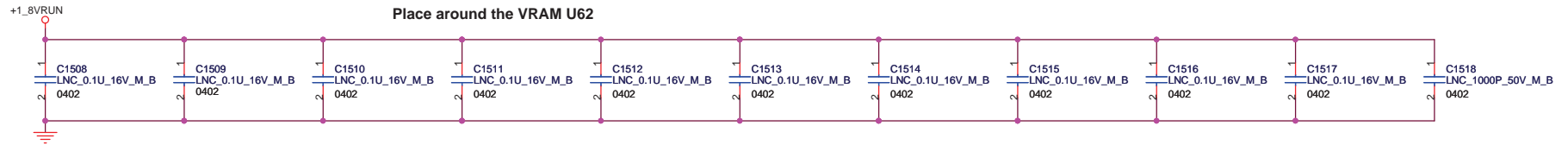
	0..30	32..63
CMD0	A4	RAS#
CMD1	RAS#	RAS#
CMD2	A5	RAS#
CMD3	BA1	BA1
CMD4	A2	A2
CMD5	A4	A4
CMD6	A3	A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	A5
CMD14	A12	A12
CMD15	RST/OUT	RST/OUT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A9	A9
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	AB	AB
CMD24	A3	A3
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

		VREF	
NV_PWR_MIZER	H	50%	
	L	70%	

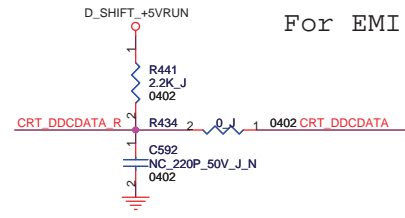
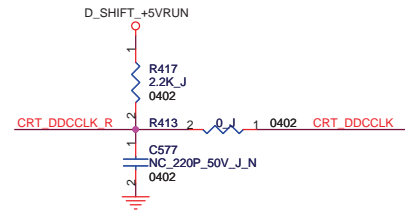




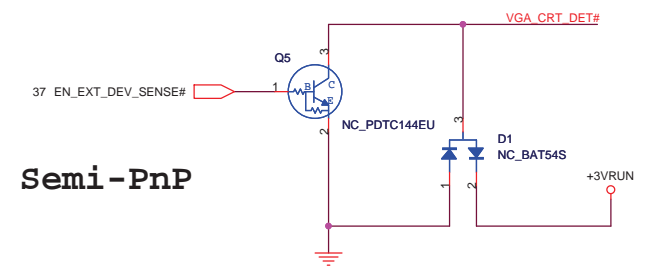
FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title VRAM (POWERBYPASS) 1 OF 2		
Size A3	Document Number M870-1-01	Rev 1.0
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FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
VRAM (POWERBYPASS) 2 OF 2			
Size	Document Number	Rev	
A3	M870-1-01	1.0	
Date:	Monday, July 27, 2009	Sheet	28 of 75

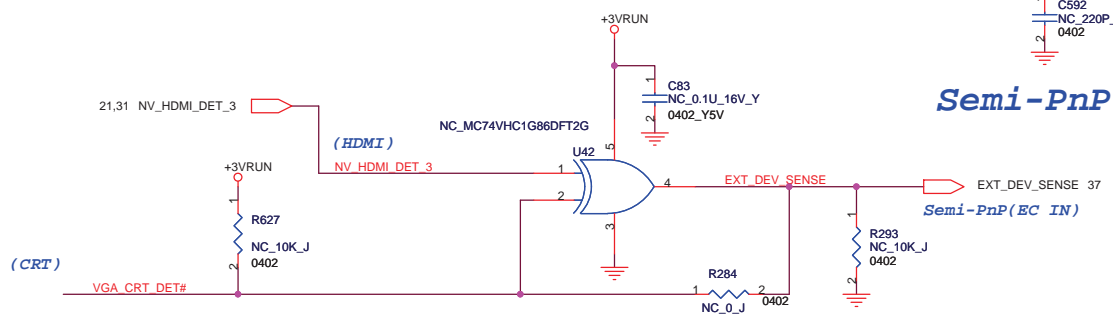


Semi-PnP

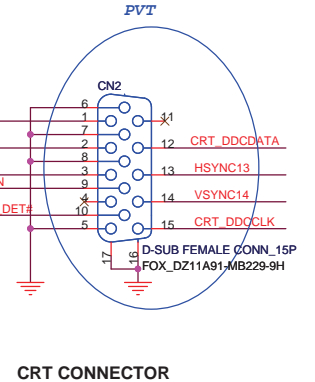
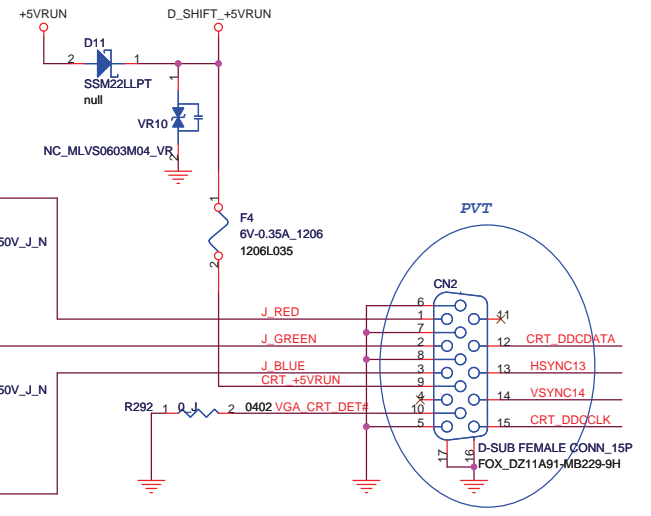
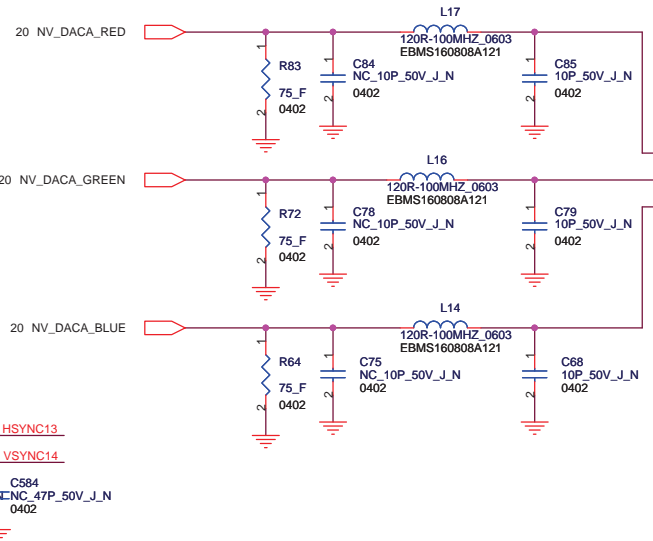


For EMI

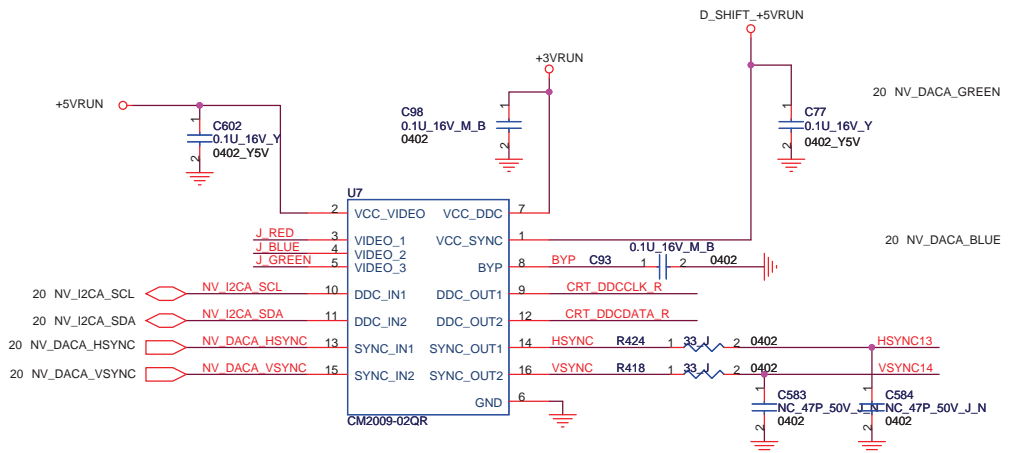
Semi-PnP Circuit



Change R83,R72,R64 to 75ohm --MOR 2/27



CRT CONNECTOR

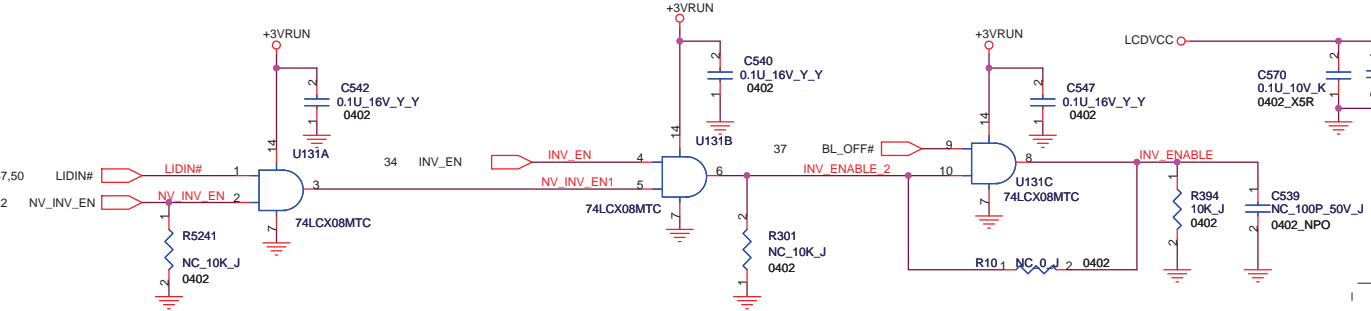
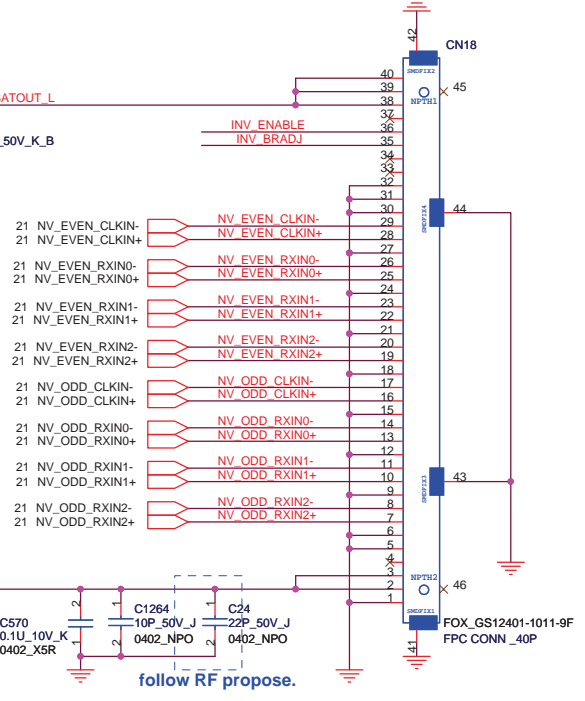
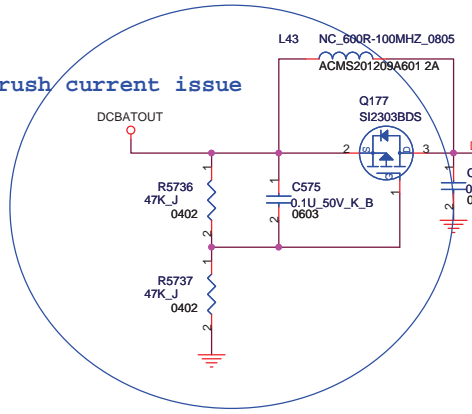
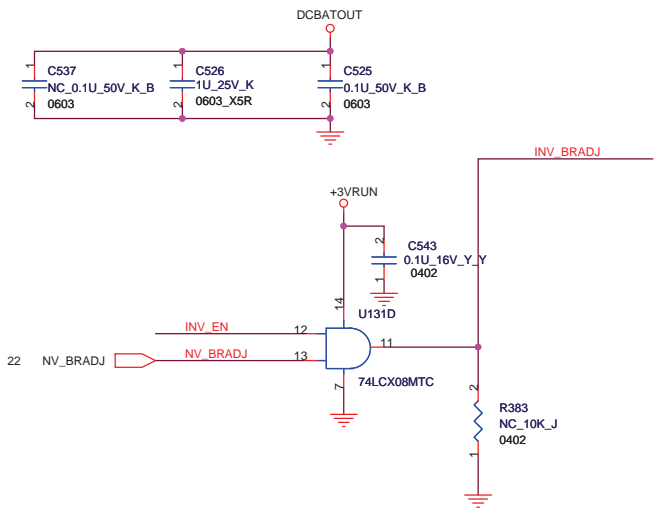


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title CRT		CCPBG - R&D Division	
Size A3	Document Number M870-1-01	Rev 1.0	
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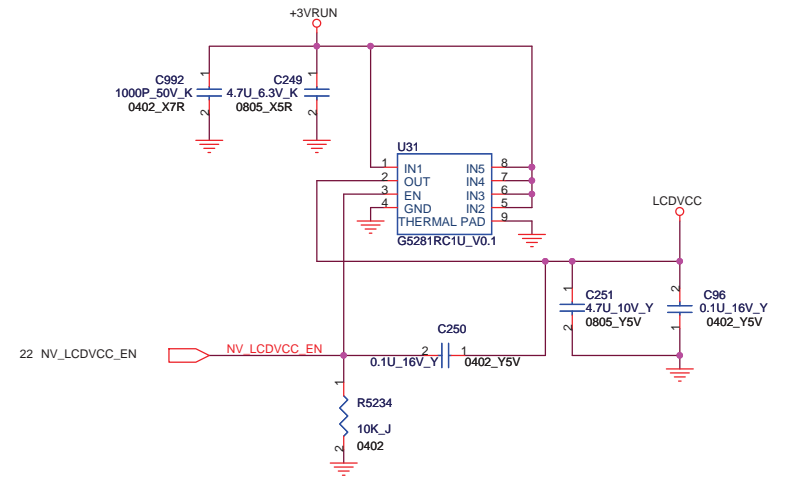
<http://laptop-motherboard-schematic.blogspot.com/>

LVDS CONNECTOR

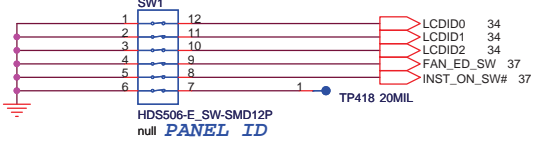
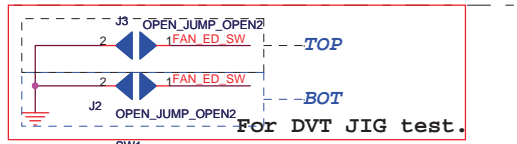
PVT
For rush current issue



Current limit is from 1.1A to 2.1A.



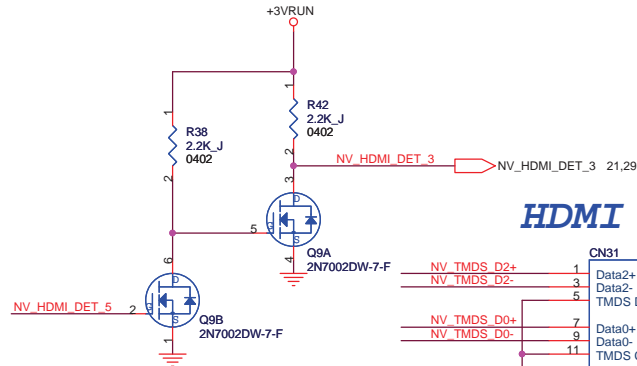
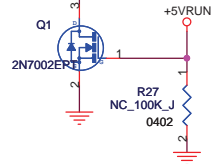
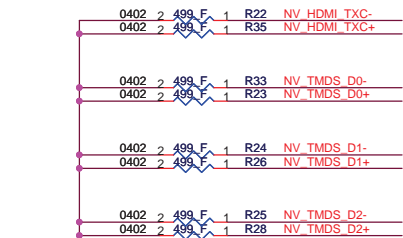
12/29 change to 10K
FAE suggestion.



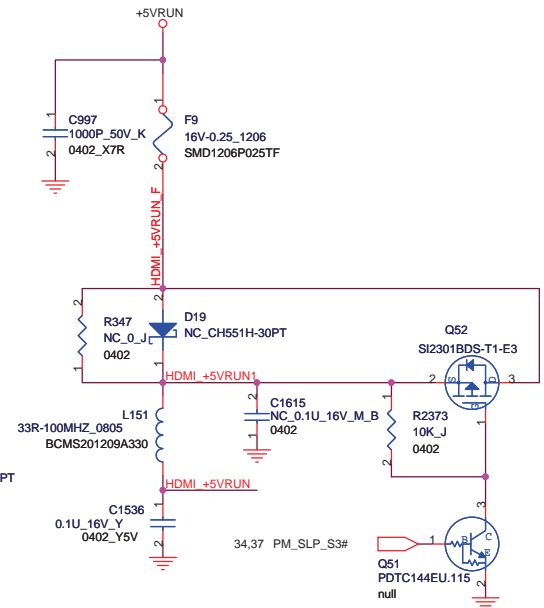
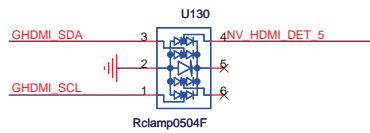
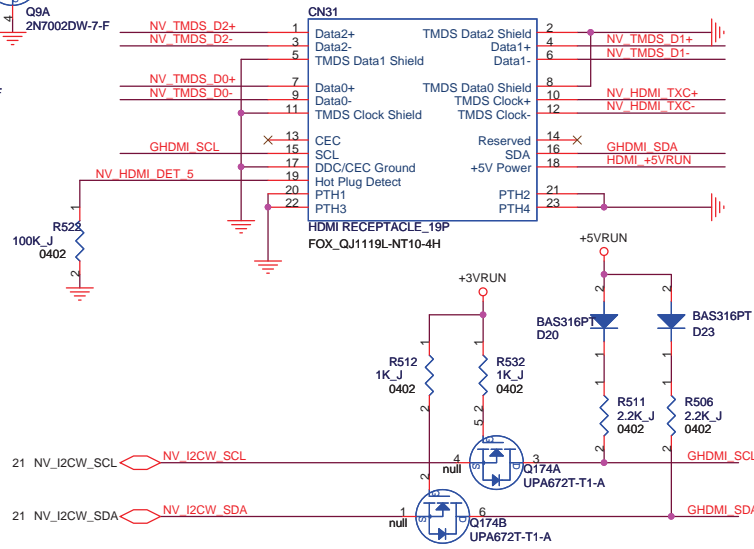
	DIS_FAN_MON#	LCDID2	LCDID1	LCDID0
AUD_E140XW02	0	0	0	0
LCD_E140WH2	0	0	0	1
SAMSUNG_LFN140A08	0	0	1	1
DISABLE FAN LOCK FUNCTION	0	X	X	X

ON:0, OFF:1

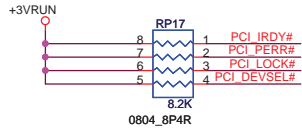
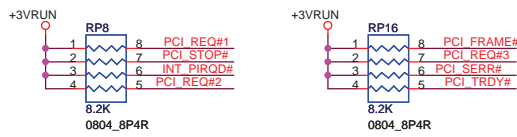
- 21 NV_HDMI_TXC-
- 21 NV_HDMI_TXC+
- 21 NV_TMDS_D0-
- 21 NV_TMDS_D0+
- 21 NV_TMDS_D1-
- 21 NV_TMDS_D1+
- 21 NV_TMDS_D2-
- 21 NV_TMDS_D2+



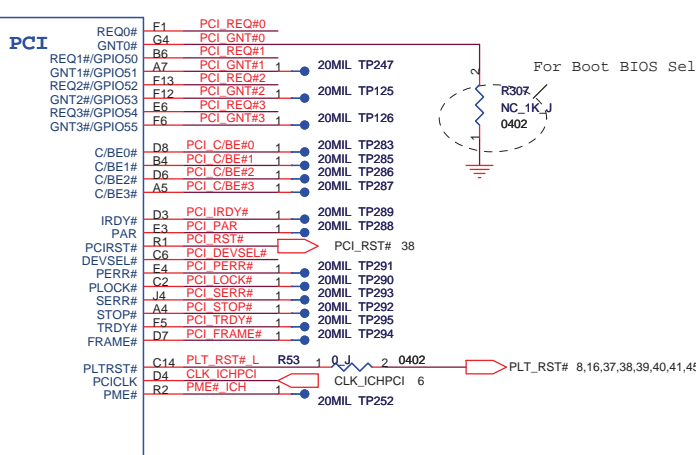
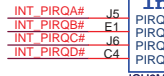
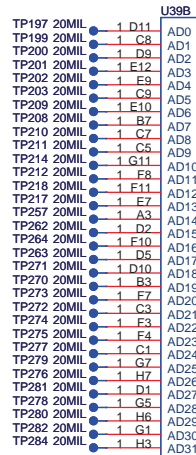
HDMI CONNECTOR



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	HDMI	
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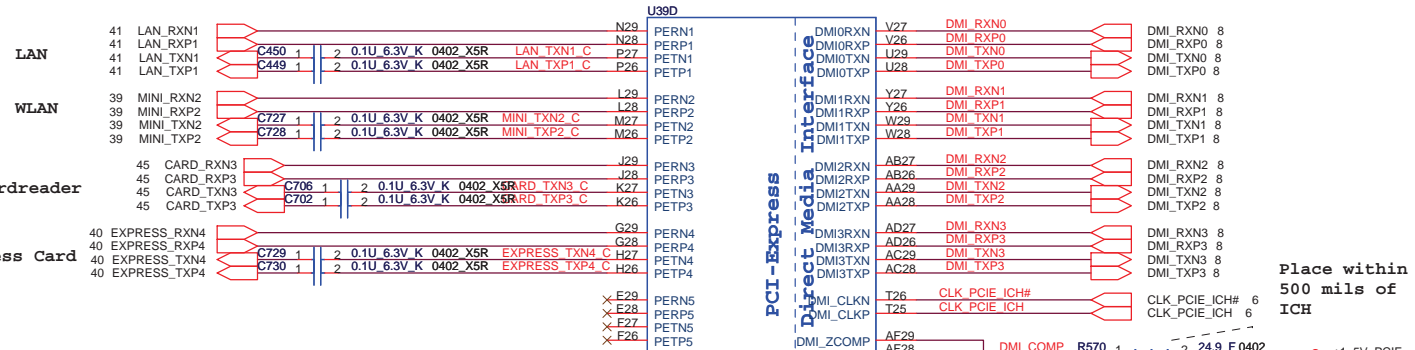
PCI Pullups



For Boot BIOS Selection.

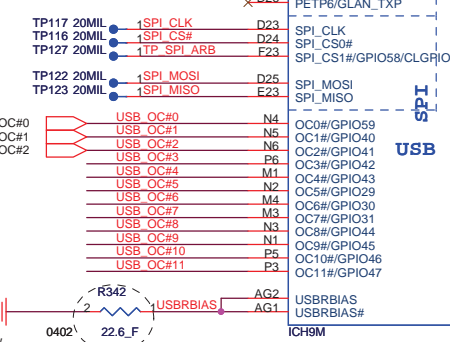
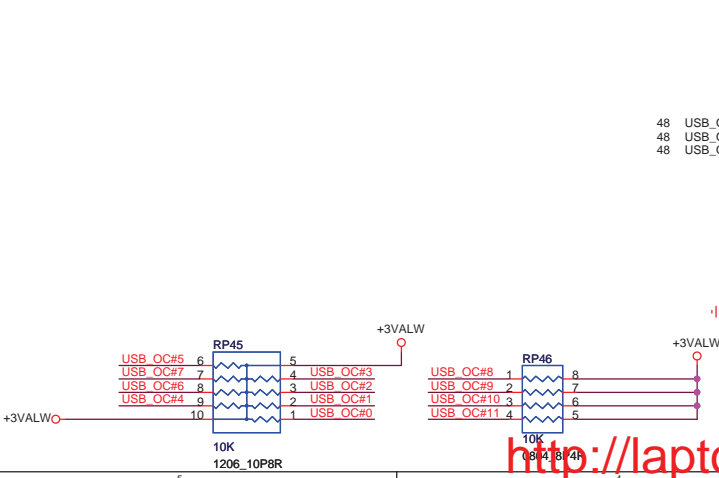
Strap for Boot-BIOS

	GNT0#	SPI_CS1#
LPC(Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI



USB PORT	Function
PORT-0	Ext. Port
PORT-1	Ext. Port
PORT-2	Ext. Port
PORT-3	
PORT-4	Bluetooth
PORT-5	EXPRESS CARD
PORT-6	Fingerprint
PORT-7	Camera
PORT-8	
PORT-9	
PORT-10	Wi-MAX
PORT-11	

Place within 500 mils of ICH

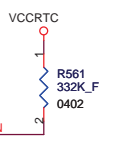


Place within 500 mils of ICH and don't routing next to high speed signals

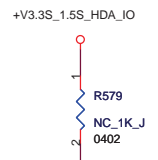
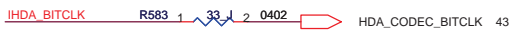
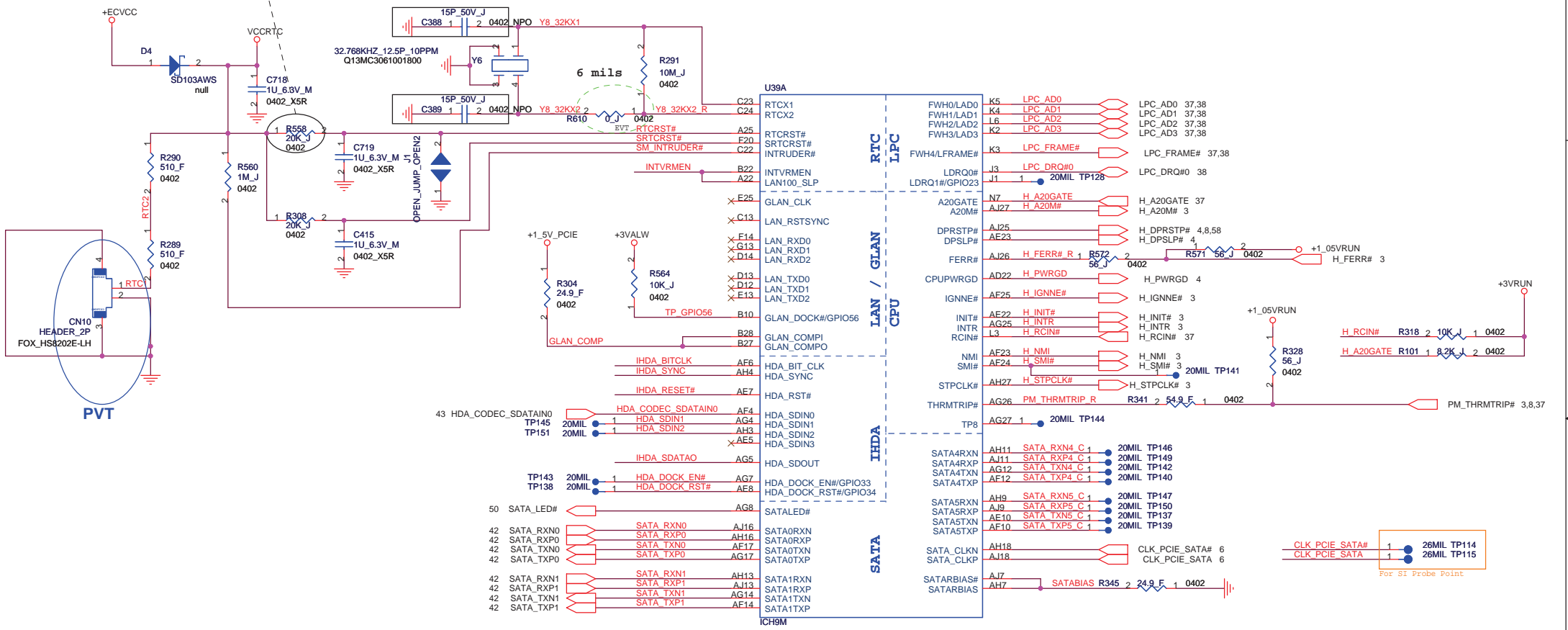
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division
 Title: **ICH9-M(PCI/DMI/USB/PCIE) 1/5**
 Size: Document Number M870-1-01 Rev 1.0
 A3: Monday, July 27, 2009 Sheet 32 of 75



Internal VRM enabled for VccSus1_05, VccSus1_5, VccC1_5, VccLAN1_05 and VccC1_05	
INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)



The traces inside this block should be wider.

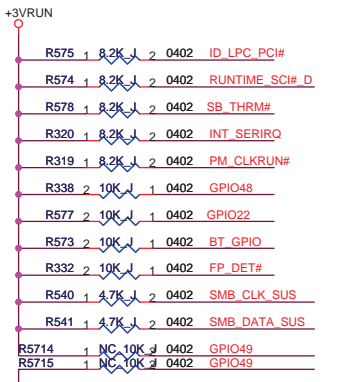
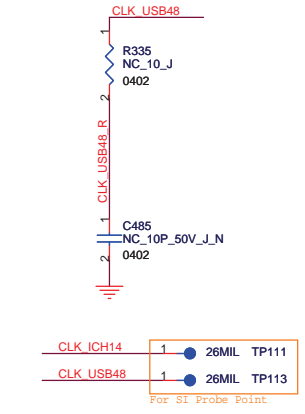
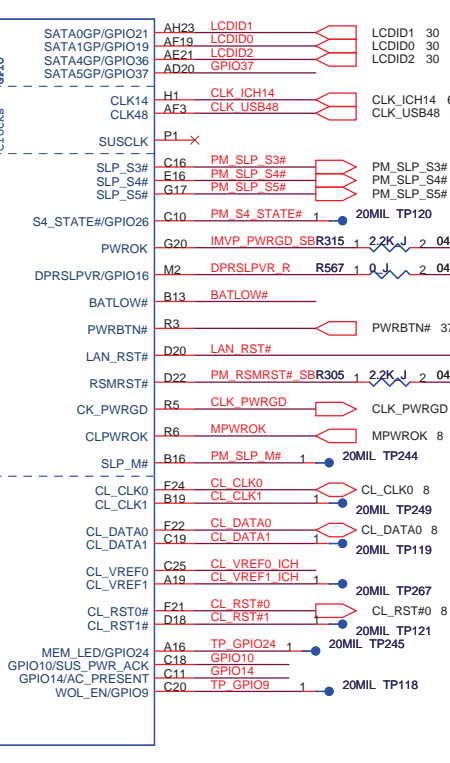
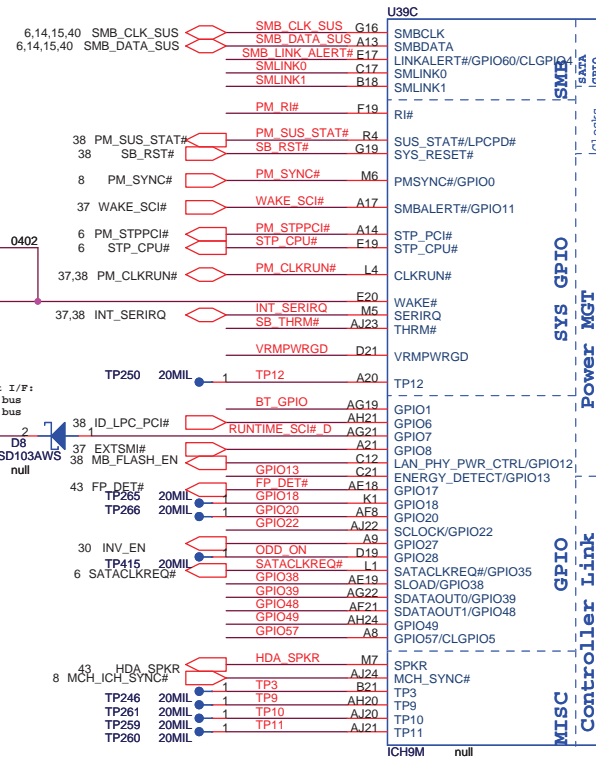
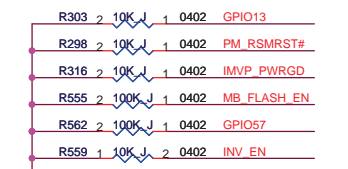
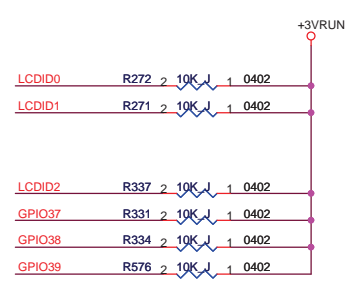
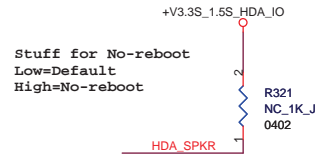
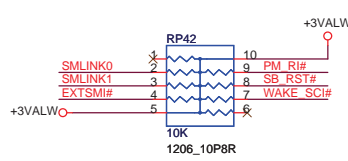


<http://laptop-motherboard-schematic.blogspot.com/>

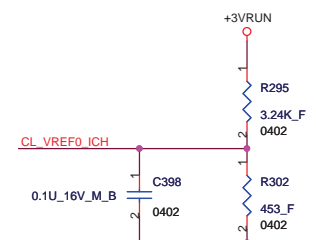
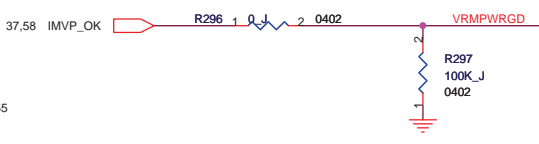
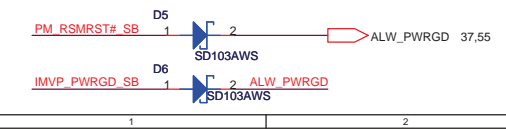
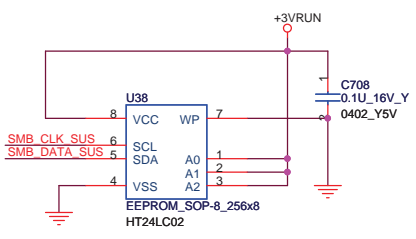
FOXCONN HON HAI Precision Ind. Co., Ltd.
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Title: **ICH9-M (LPC,IDE,SATA) 2/5**

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Pull-High GPU--ES
Pull-Low GPU--QS

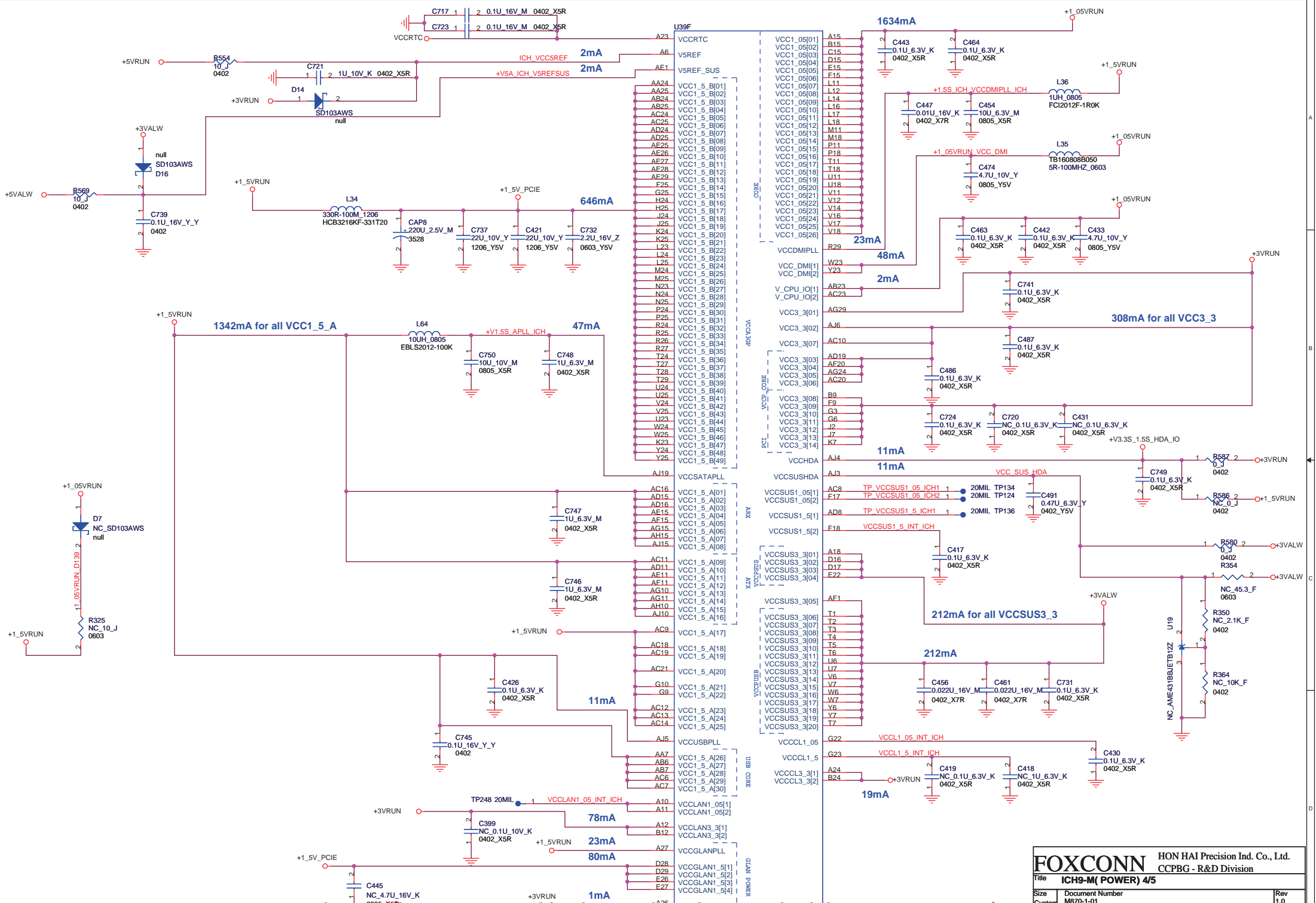


FOXCONN HON HAI Precision Ind. Co., Ltd.
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Title: **ICH9-M (GPIO) 3/5**

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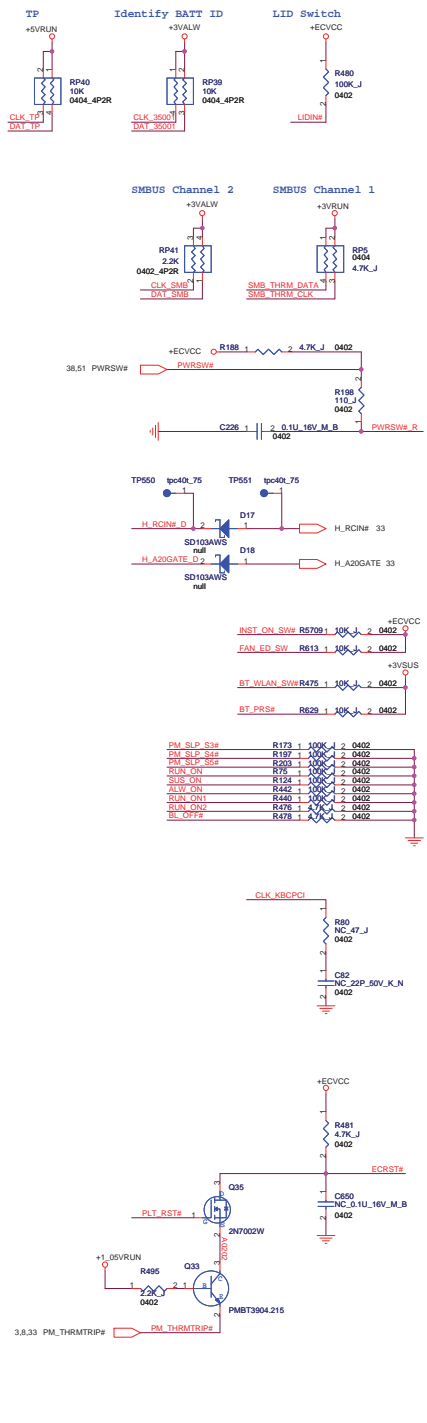
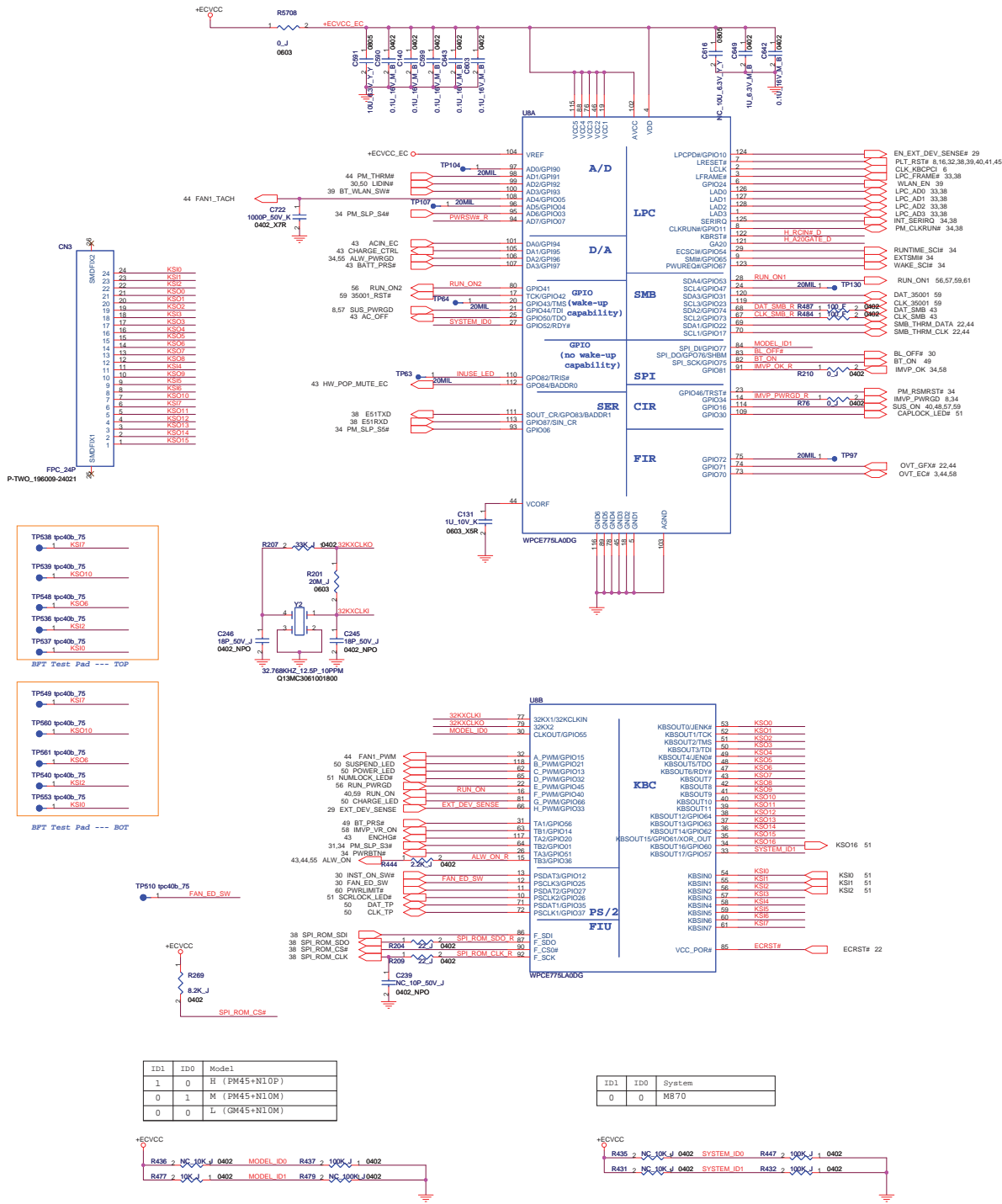


U39E		H5	
AA26	VSS[001]	VSS[107]	J23
AA27	VSS[002]	VSS[108]	J26
AA3	VSS[003]	VSS[109]	J27
AA6	VSS[004]	VSS[110]	AC22
AB1	VSS[005]	VSS[111]	K28
AA23	VSS[006]	VSS[112]	K29
AB28	VSS[007]	VSS[113]	L13
AB29	VSS[008]	VSS[114]	L15
AB4	VSS[009]	VSS[115]	L2
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L5
AC27	VSS[013]	VSS[119]	L7
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD18	VSS[021]	VSS[127]	M28
AD21	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	N11
AD29	VSS[024]	VSS[130]	N12
AD4	VSS[025]	VSS[131]	N13
AD5	VSS[026]	VSS[132]	N14
AD6	VSS[027]	VSS[133]	N15
AD7	VSS[028]	VSS[134]	N16
AD9	VSS[029]	VSS[135]	N17
AE12	VSS[030]	VSS[136]	N18
AE13	VSS[031]	VSS[137]	N26
AE14	VSS[032]	VSS[138]	N27
AE16	VSS[033]	VSS[139]	P12
AE17	VSS[034]	VSS[140]	P13
AE2	VSS[035]	VSS[141]	P14
AE20	VSS[036]	VSS[142]	P15
AE24	VSS[037]	VSS[143]	P16
AE3	VSS[038]	VSS[144]	P17
AE4	VSS[039]	VSS[145]	P2
AE6	VSS[040]	VSS[146]	P23
AE9	VSS[041]	VSS[147]	P28
AF13	VSS[042]	VSS[148]	P29
AF16	VSS[043]	VSS[149]	P4
AF18	VSS[044]	VSS[150]	P7
AF22	VSS[045]	VSS[151]	R11
AH26	VSS[046]	VSS[152]	R12
AF26	VSS[047]	VSS[153]	R13
AF5	VSS[048]	VSS[154]	R14
AF7	VSS[049]	VSS[155]	R15
AF9	VSS[050]	VSS[156]	R16
AG13	VSS[051]	VSS[157]	R17
AG16	VSS[052]	VSS[158]	R18
AG18	VSS[053]	VSS[159]	R28
AG20	VSS[054]	VSS[160]	T12
AG23	VSS[055]	VSS[161]	T13
AG3	VSS[056]	VSS[162]	T14
AG6	VSS[057]	VSS[163]	T15
AG9	VSS[058]	VSS[164]	T16
AH12	VSS[059]	VSS[165]	T17
AH14	VSS[060]	VSS[166]	T23
AH17	VSS[061]	VSS[167]	B26
AH19	VSS[062]	VSS[168]	U12
AH2	VSS[063]	VSS[169]	U13
AH22	VSS[064]	VSS[170]	U14
AH25	VSS[065]	VSS[171]	U15
AH28	VSS[066]	VSS[172]	U16
AH5	VSS[067]	VSS[173]	U17
AH8	VSS[068]	VSS[174]	AD23
AH8	VSS[069]	VSS[175]	U26
AJ12	VSS[070]	VSS[176]	U27
AJ14	VSS[071]	VSS[177]	U3
AJ17	VSS[072]	VSS[178]	V1
AJ8	VSS[073]	VSS[179]	V13
B11	VSS[074]	VSS[180]	V15
B14	VSS[075]	VSS[181]	V23
B17	VSS[076]	VSS[182]	V28
B2	VSS[077]	VSS[183]	V29
B20	VSS[078]	VSS[184]	V4
B23	VSS[079]	VSS[185]	V5
B5	VSS[080]	VSS[186]	W26
B8	VSS[081]	VSS[187]	W27
C26	VSS[082]	VSS[188]	W3
C27	VSS[083]	VSS[189]	Y1
E11	VSS[084]	VSS[190]	Y28
E14	VSS[085]	VSS[191]	Y29
E18	VSS[086]	VSS[192]	Y4
E2	VSS[087]	VSS[193]	Y5
E21	VSS[088]	VSS[194]	AG28
E24	VSS[089]	VSS[195]	AH6
E5	VSS[090]	VSS[196]	AF2
E8	VSS[091]	VSS[197]	B25
F16	VSS[092]	VSS[198]	
F28	VSS[093]		
F29	VSS[094]	VSS_NCTF[01]	A1
G12	VSS[095]	VSS_NCTF[02]	A2
G14	VSS[096]	VSS_NCTF[03]	A28
G18	VSS[097]	VSS_NCTF[04]	A29
G21	VSS[098]	VSS_NCTF[05]	AH1
G24	VSS[099]	VSS_NCTF[06]	AH29
G26	VSS[100]	VSS_NCTF[07]	AJ1
G27	VSS[101]	VSS_NCTF[08]	AJ2
G8	VSS[102]	VSS_NCTF[09]	AJ28
H2	VSS[103]	VSS_NCTF[10]	AJ29
H23	VSS[104]	VSS_NCTF[11]	B1
H28	VSS[105]	VSS_NCTF[12]	B29
H29	VSS[106]		

ICH9M

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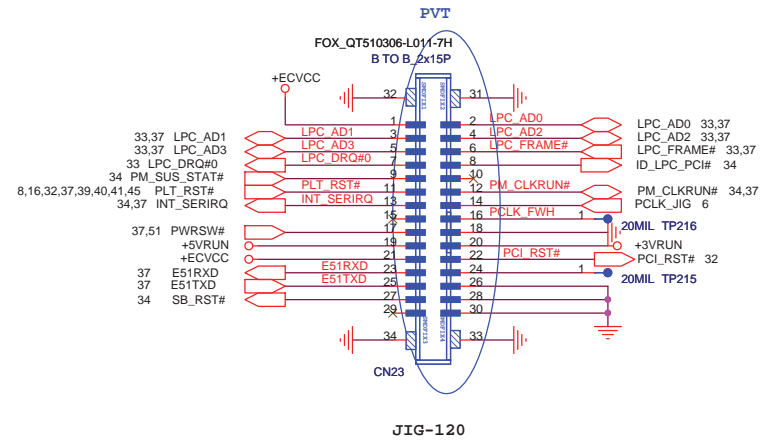
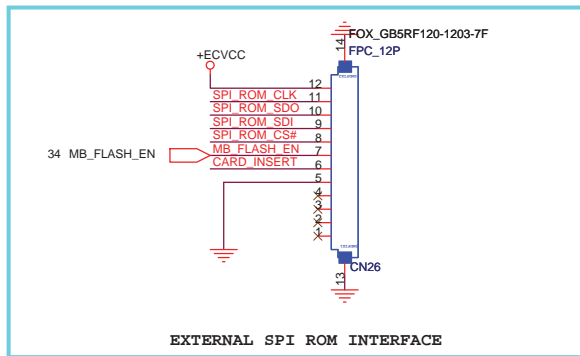
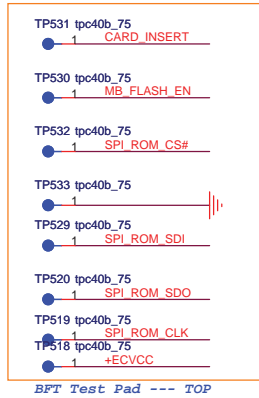
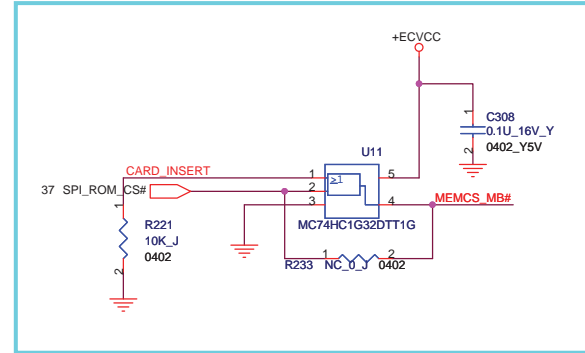
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		CCPBG - R&D Division	
Title	ICH9-M(GND) 5/5		
Size	Document Number	Rev	
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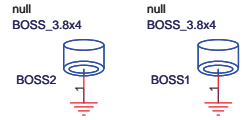
ID1	ID0	Model
1	0	H (PM45+N1OP)
0	1	M (PM45+N1OM)
0	0	L (GM45+N1OM)

ID1	ID0	System
0	0	MB70

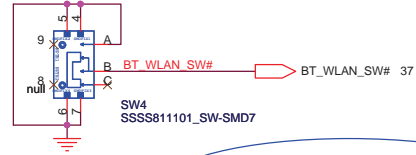
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division



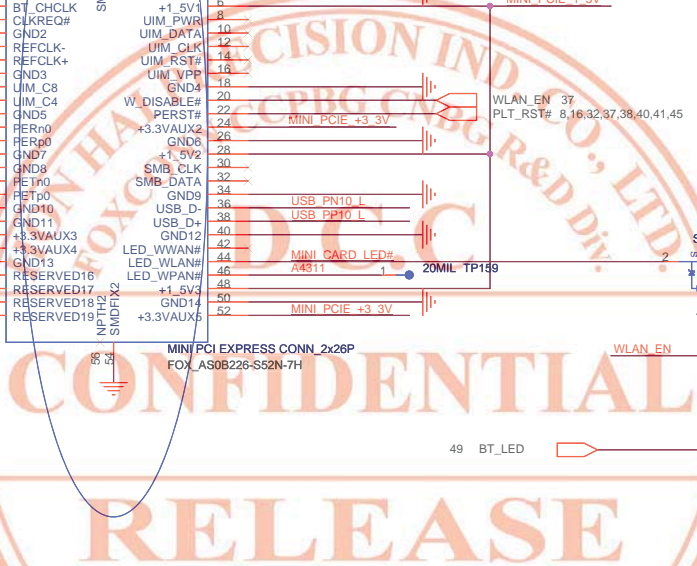
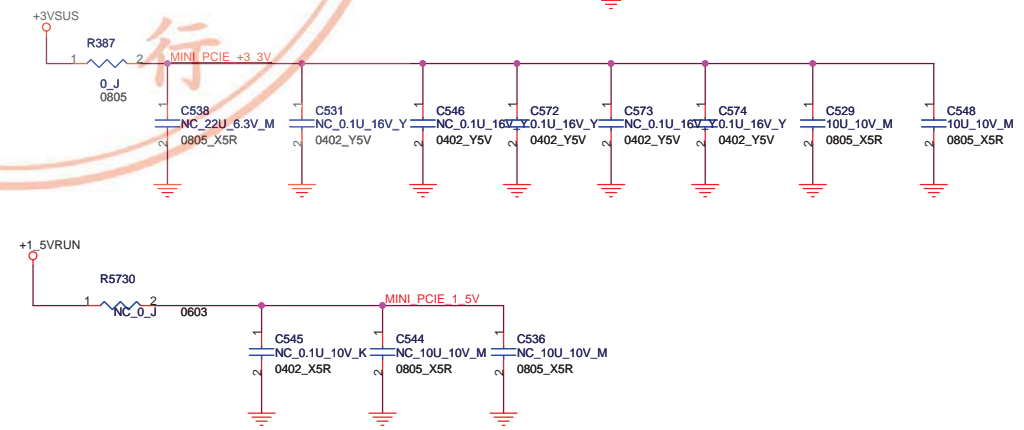
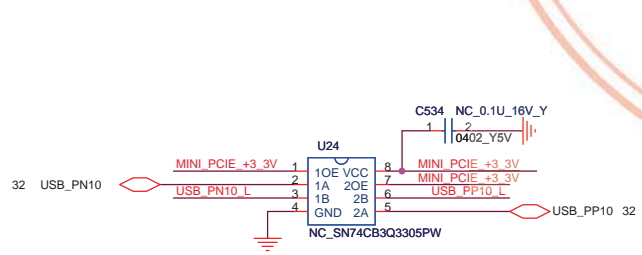
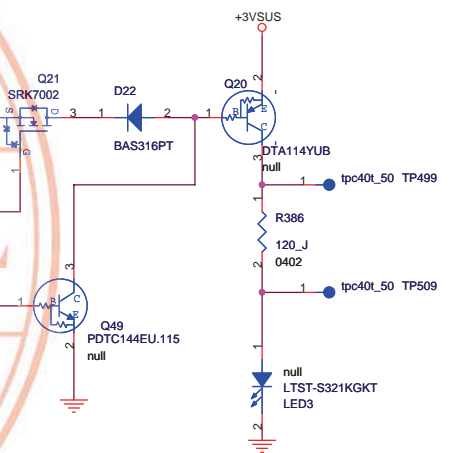
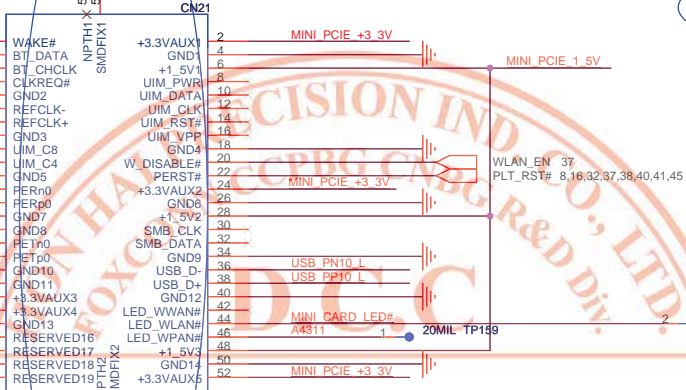
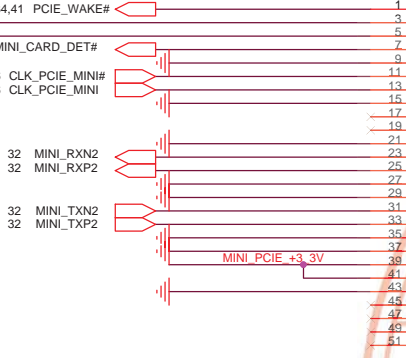
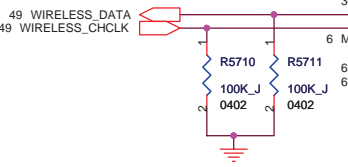
SW4.C pin delete and SW4.A connect to GND.



PVT



PVT

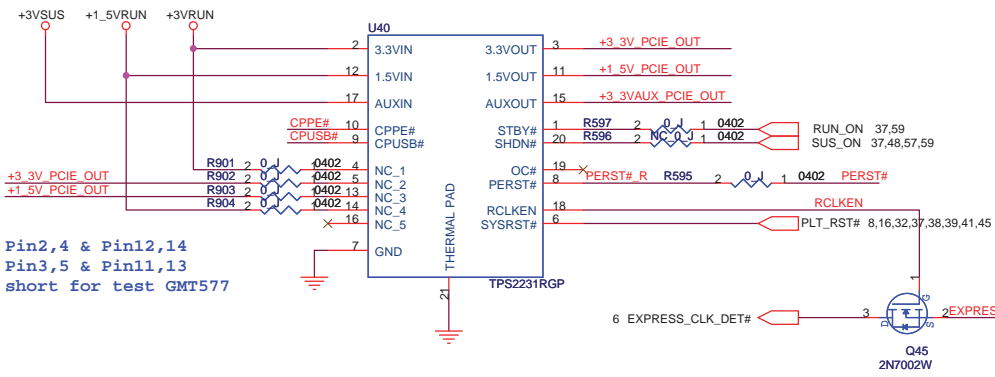


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		Half Mini Card	
Size	Document Number	Rev	
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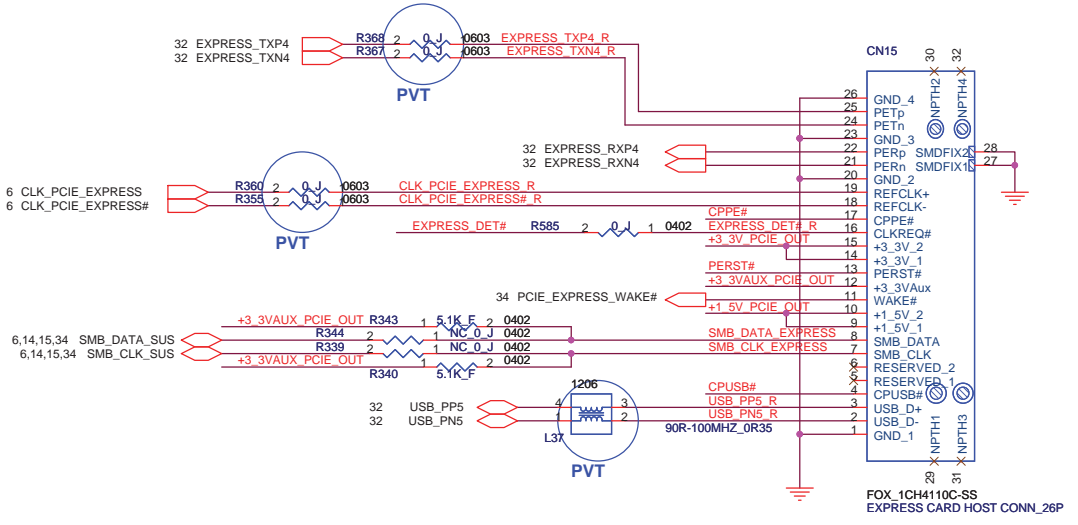
<http://laptop-motherboard-schematic.blogspot.com/>

+1_5V=>1.3A
 +3_3VAux=>0.6A
 +3_3V=>2.5A

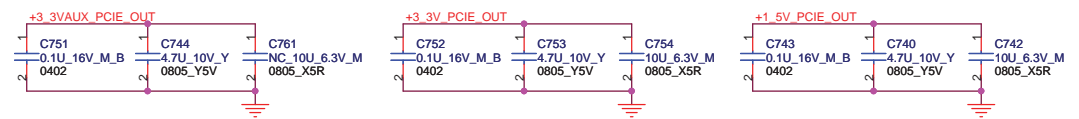
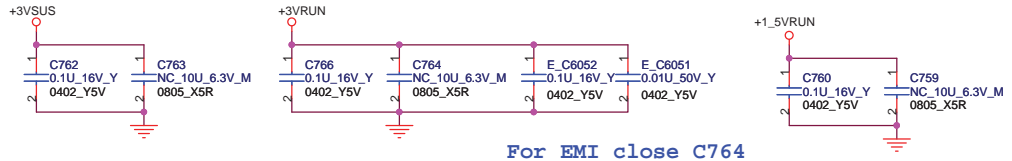
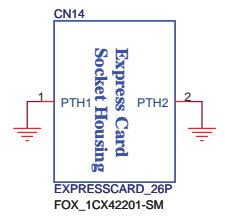
Express Card Power Switch



Pin2,4 & Pin12,14
 Pin3,5 & Pin11,13
 short for test GMT577

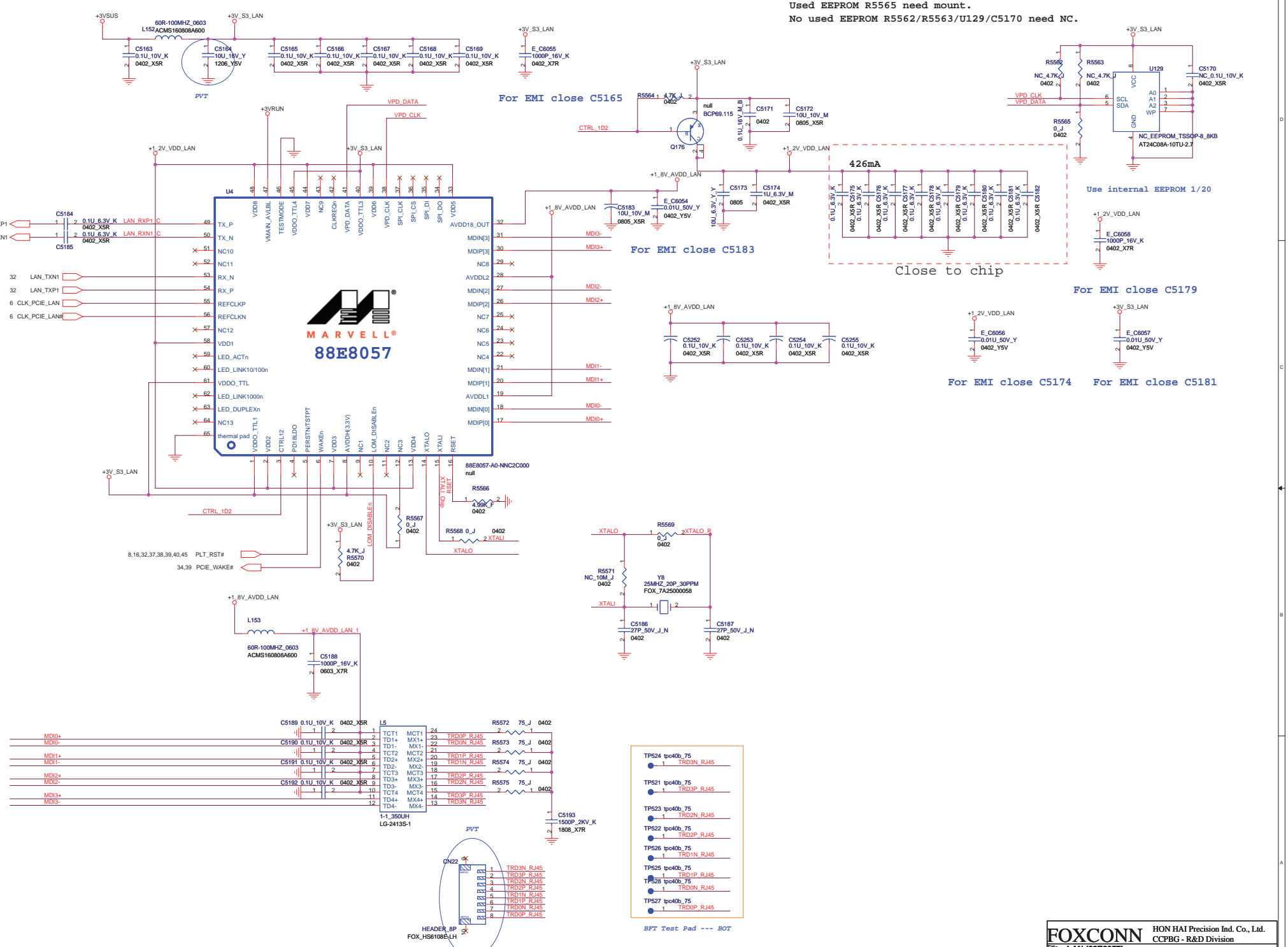


Express Card Slot.



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title EXPRESS CARD		CCPBG - R&D Division	
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Used EEPROM R5565 need mount.
 No used EEPROM R5562/R5563/U129/C5170 need NC.



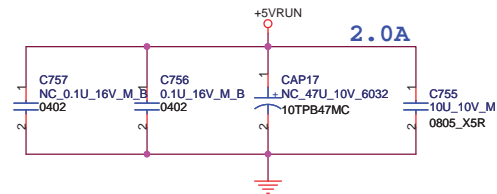
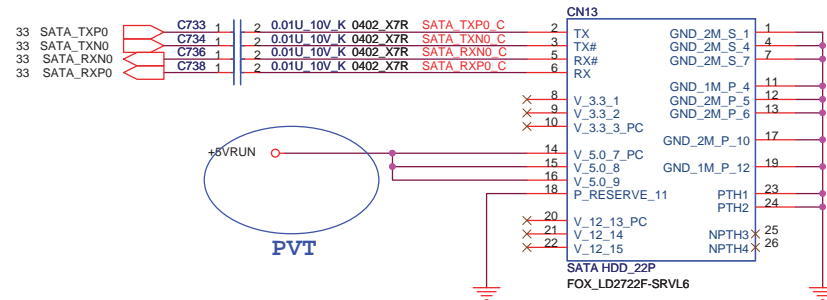
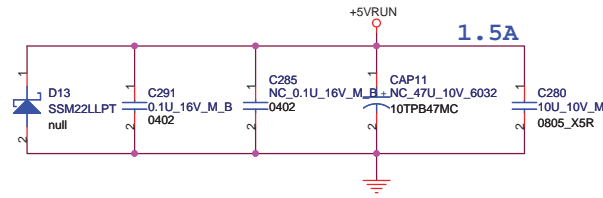
<http://laptop-motherboard-schematic.blogspot.com/>

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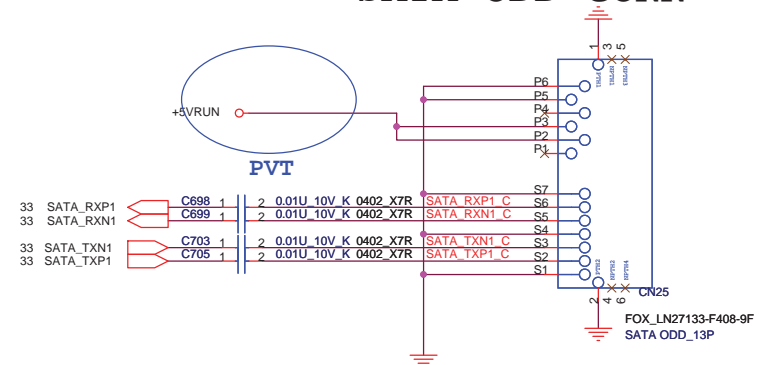
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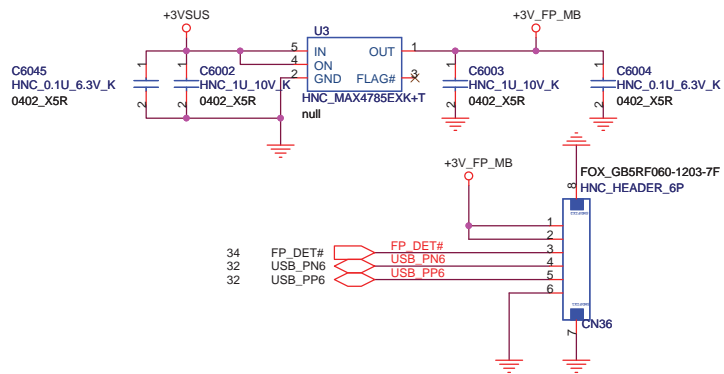
Size	Document Number	Rev
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SATA HDD CONN

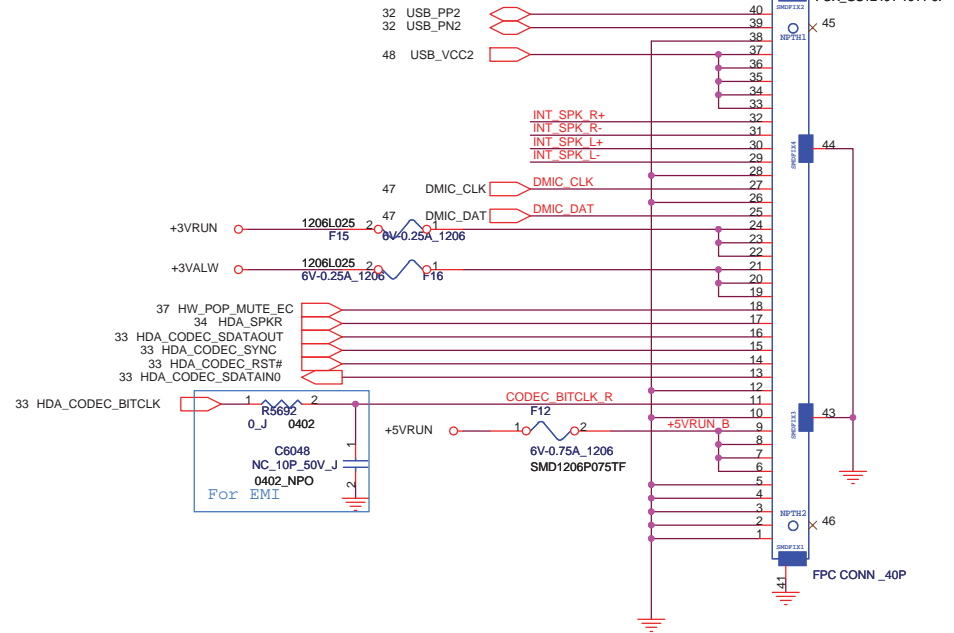


SATA ODD CONN

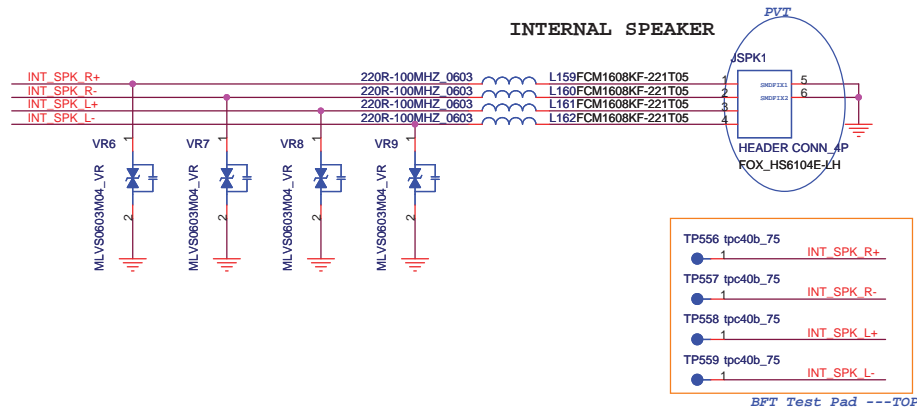




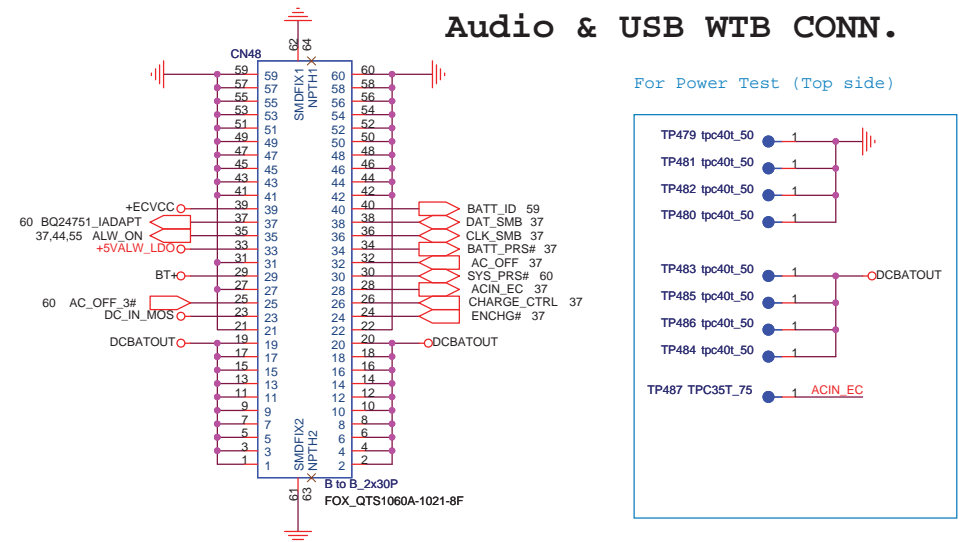
FingerPrint FTB CONN.



Audio & USB WTB CONN.

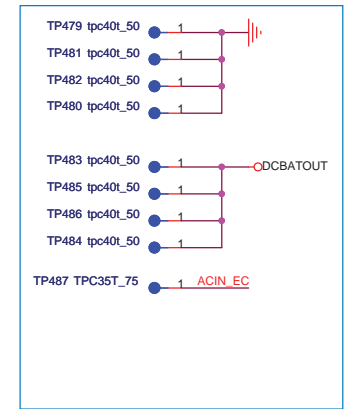


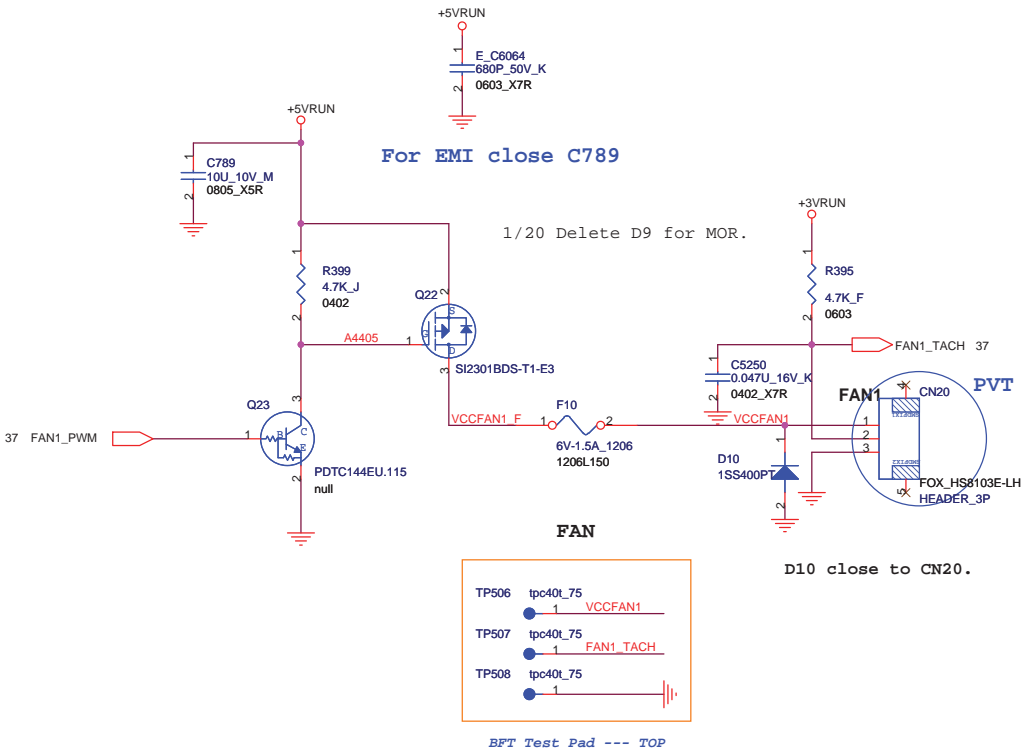
- TP556 tpc40b_75 INT_SPK R+
 - TP557 tpc40b_75 INT_SPK R-
 - TP558 tpc40b_75 INT_SPK L+
 - TP559 tpc40b_75 INT_SPK L-
- BFT Test Pad ---TOP



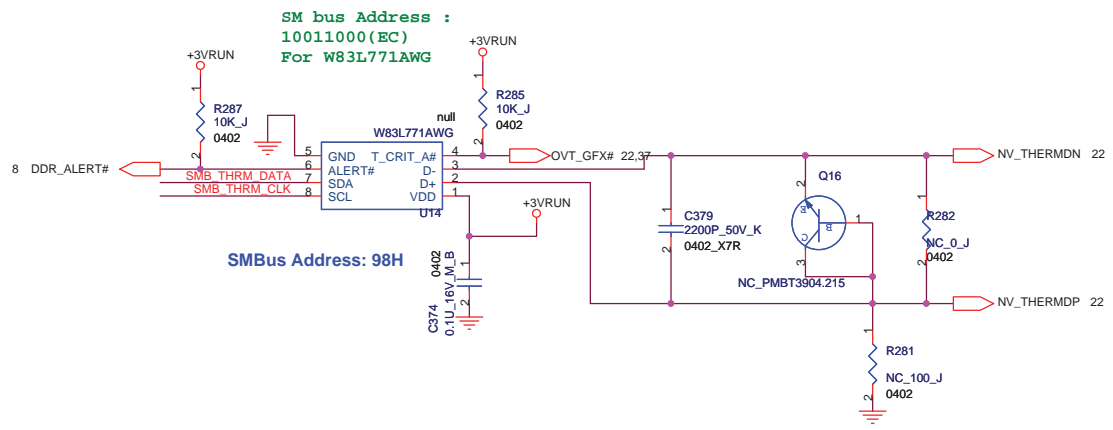
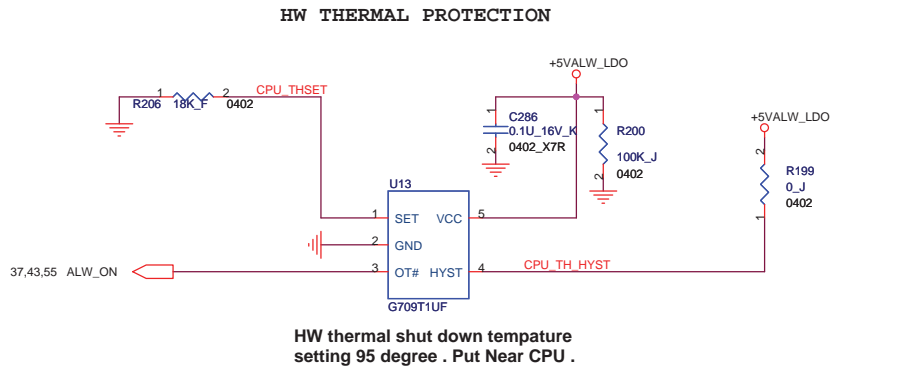
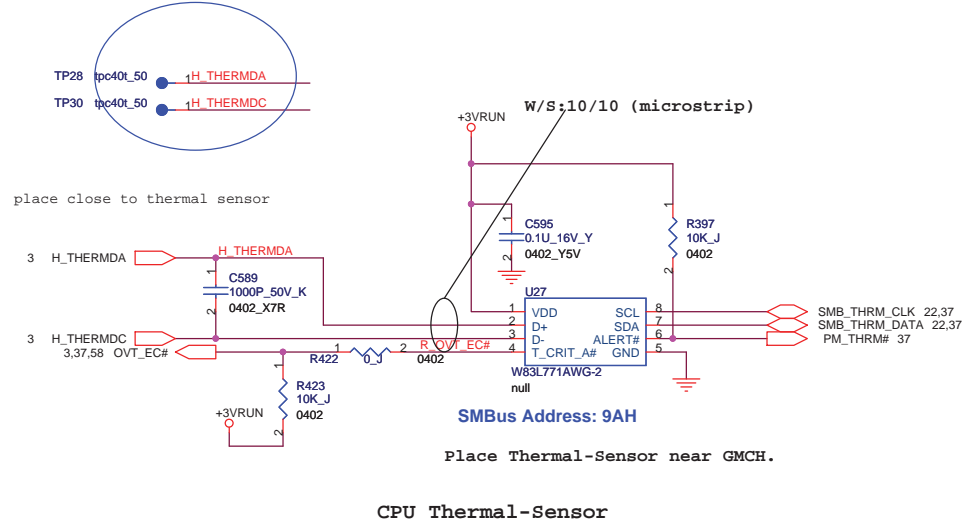
Charger Board CONN.

For Power Test (Top side)

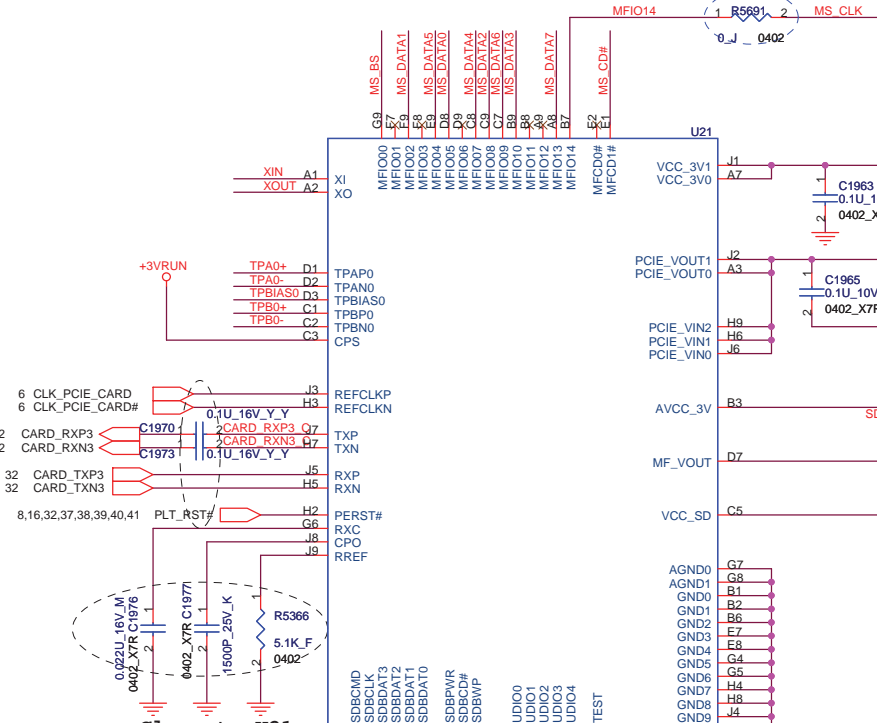
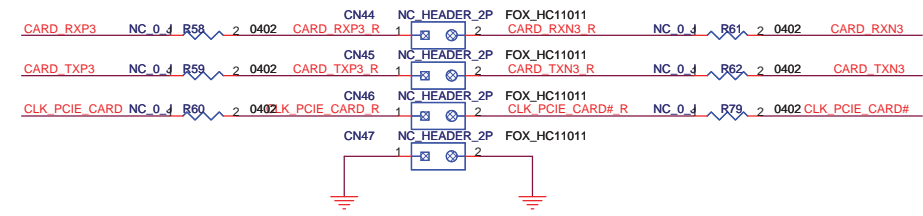
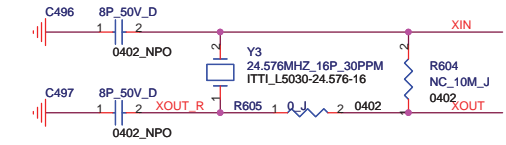




將這2個點位置拉大至少100mil，DVT時距離太進影響測

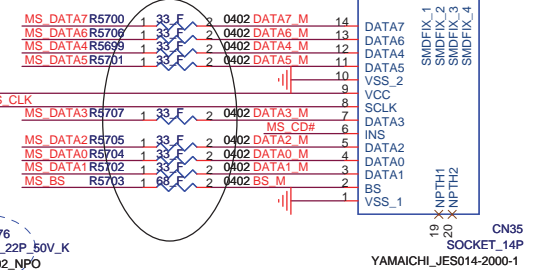


01/20 Add pin headers and resistors for PCIe protocol measurement for R5U231.

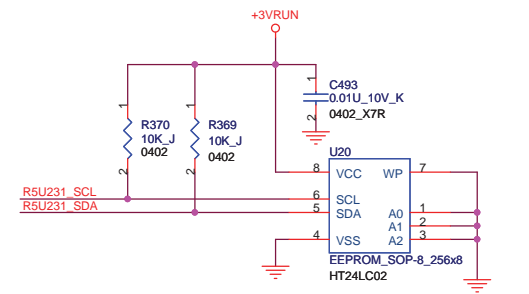
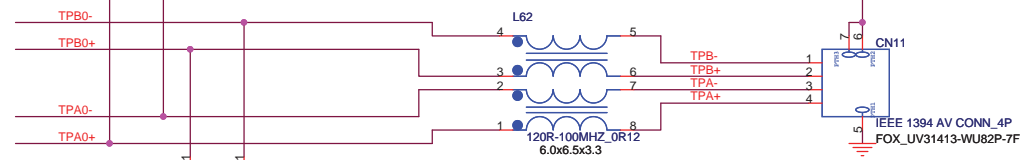
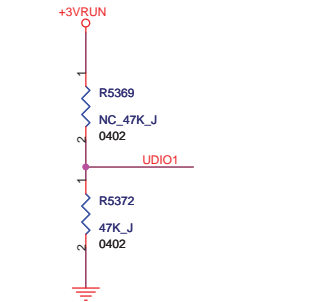
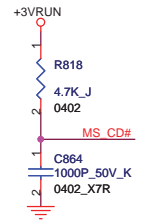
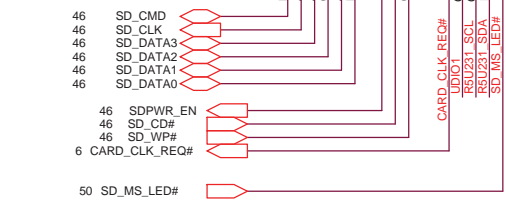


Change CN35 From ME request.

Close to U21



Close to U21



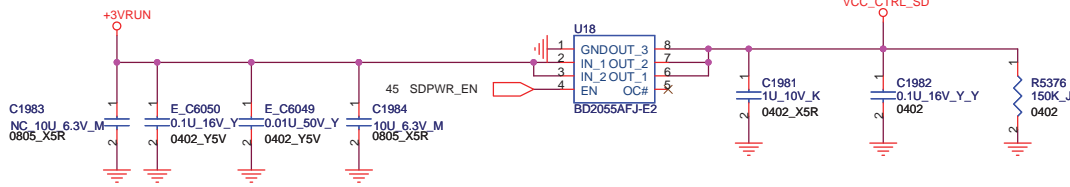
SROM: UDIO1
Pull-Hi: Disable
Pull-Lo: Enable (Default)

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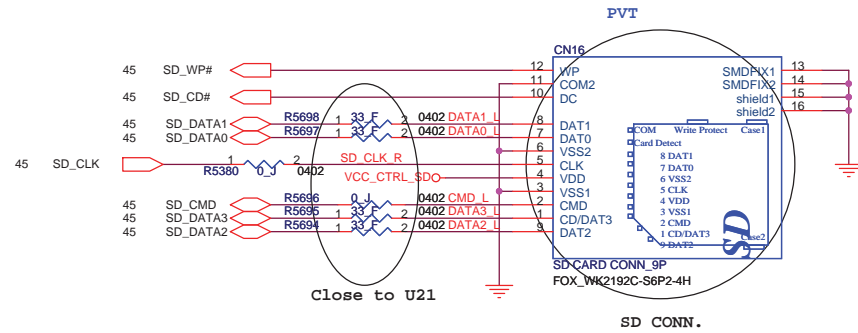
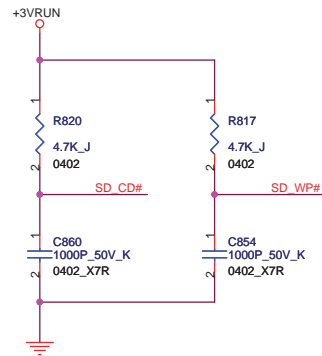
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SD POWER

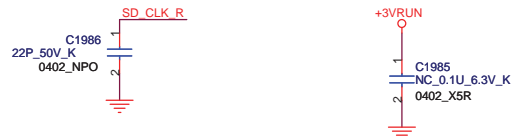
For EMI close C1983

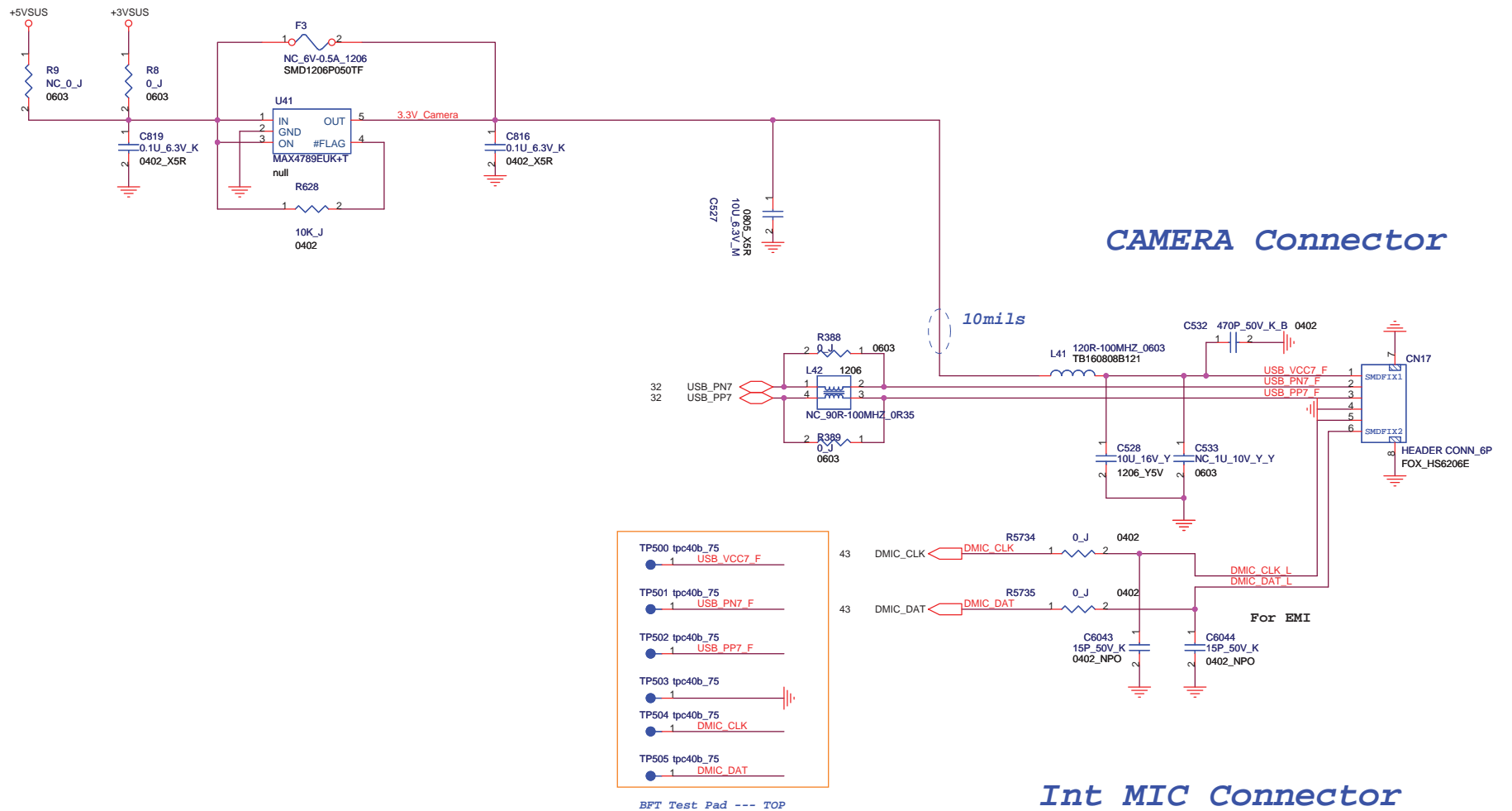


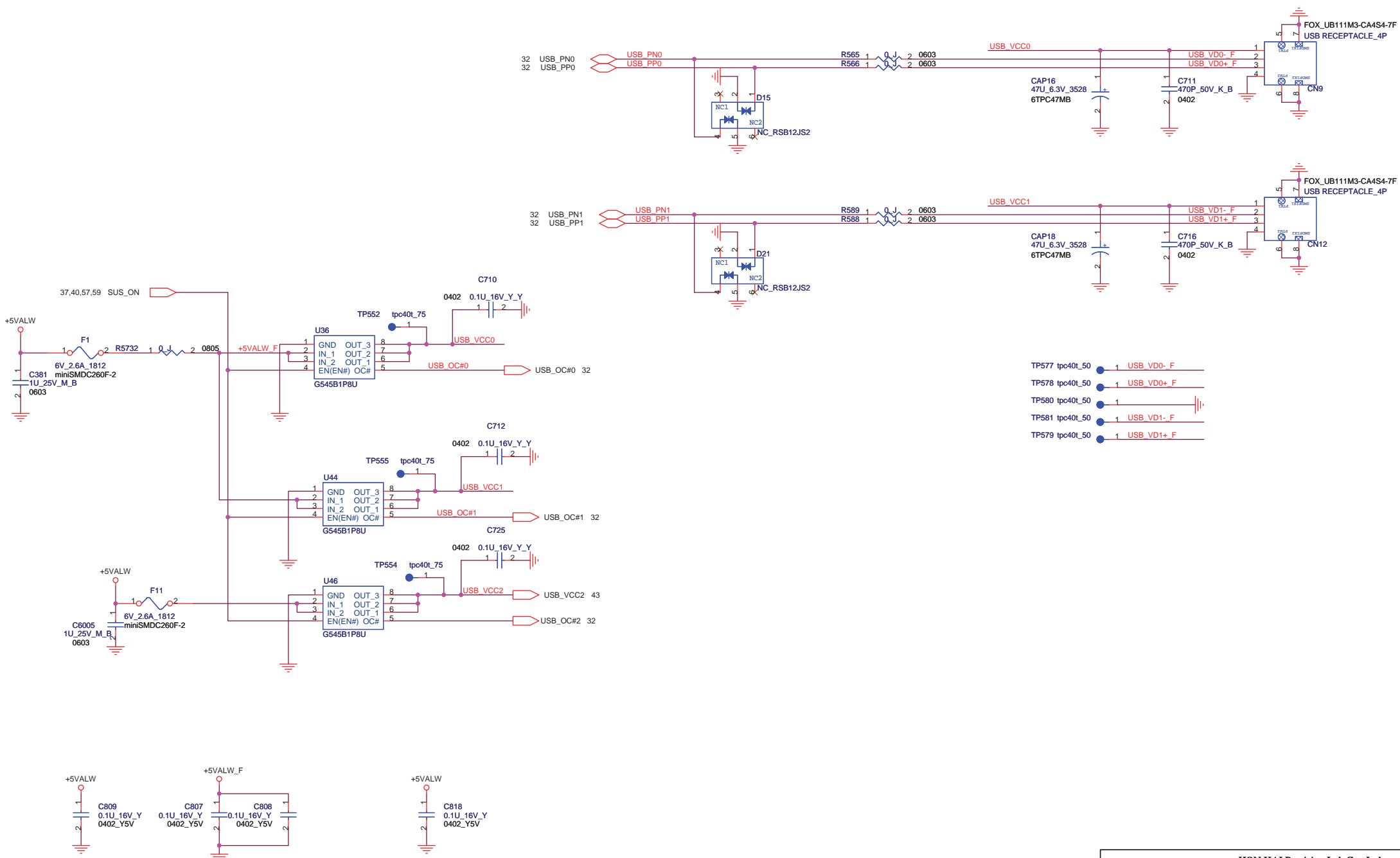
Close to U21

SD CONN.

For EMI







- TP577 tpc40t_50 1 USB_VD0- F
- TP578 tpc40t_50 1 USB_VD0+ F
- TP580 tpc40t_50 1
- TP581 tpc40t_50 1 USB_VD1- F
- TP579 tpc40t_50 1 USB_VD1+ F

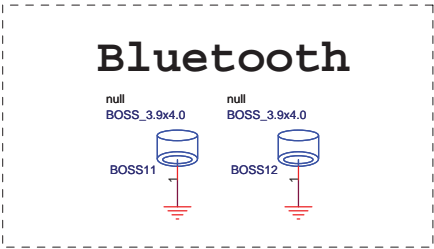
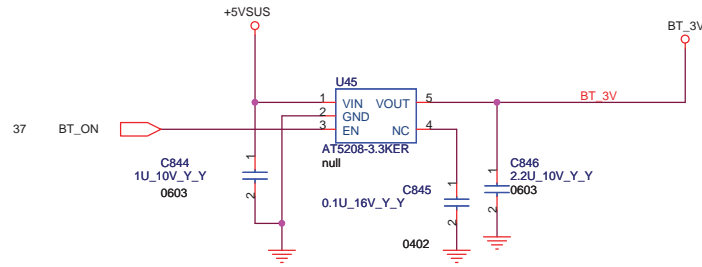
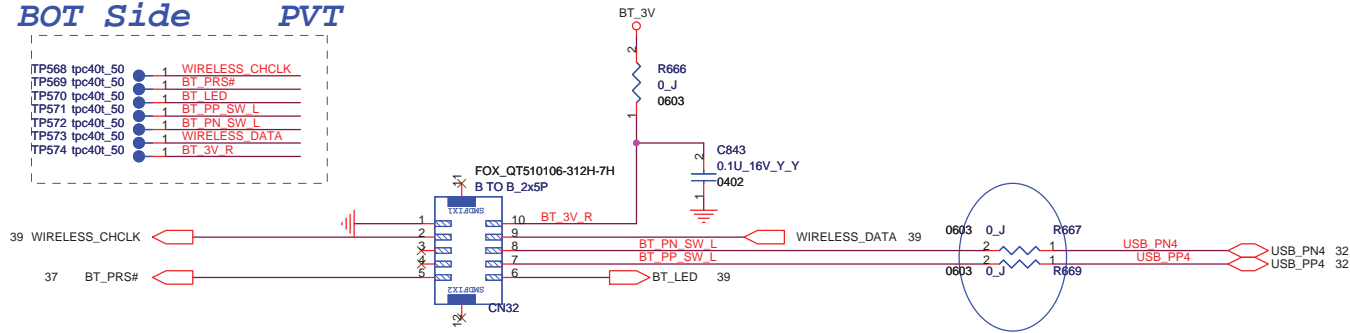
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Title USB2.0		CCPBG - R&D Division	
Size A3	Document Number M870-1-01	Rev 1.0	
Date: Monday, July 27, 2009	Sheet 48	of 75	

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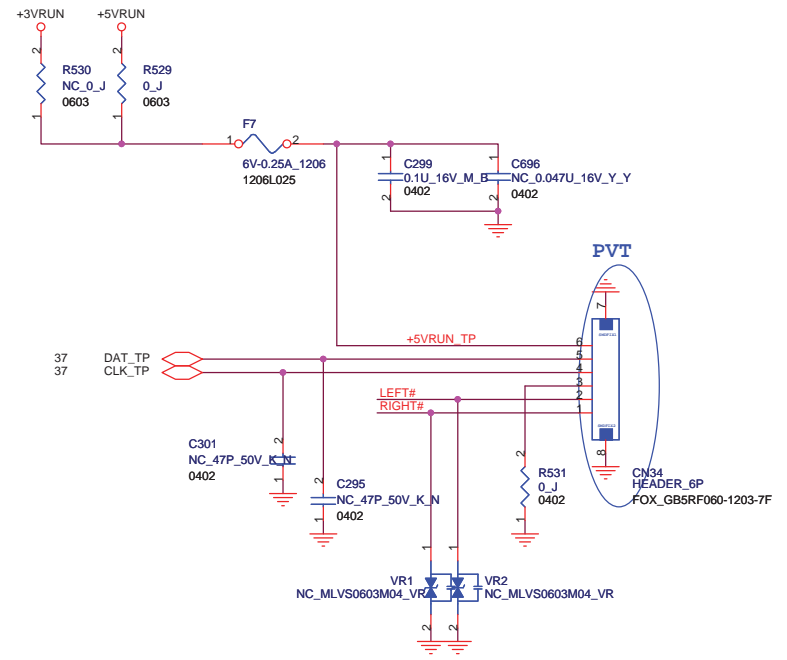
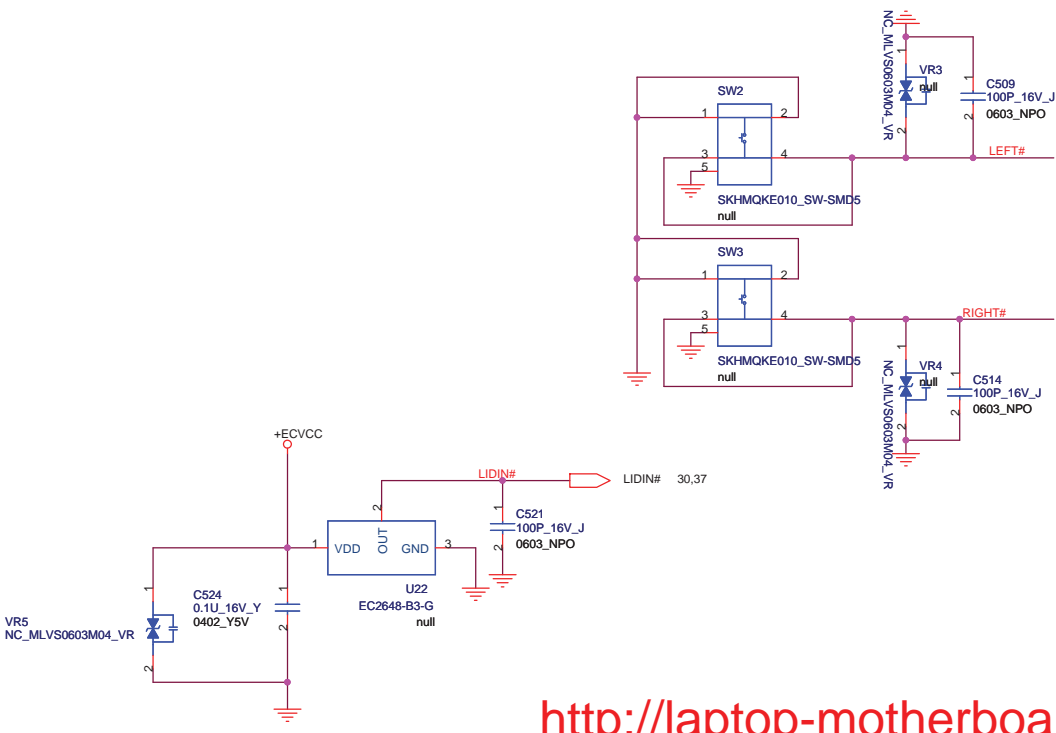
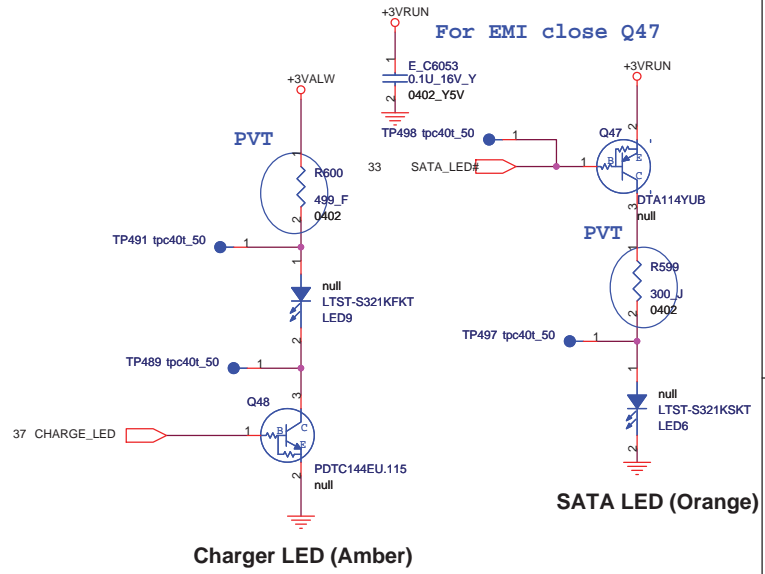
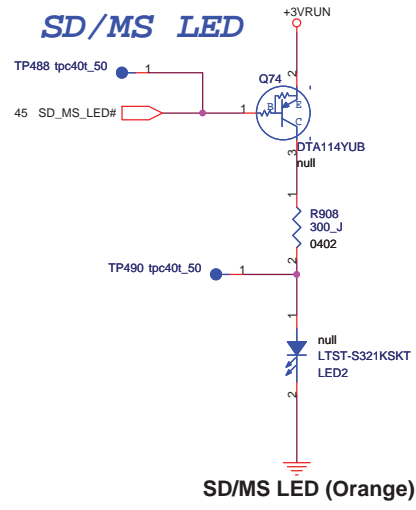
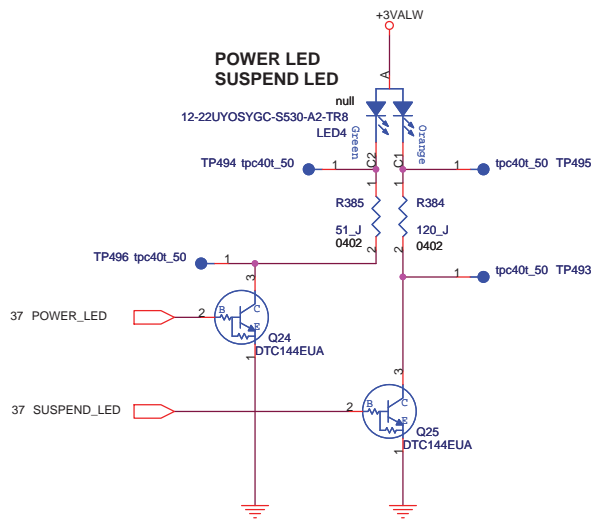
Bluetooth connector

BOT Side PVT

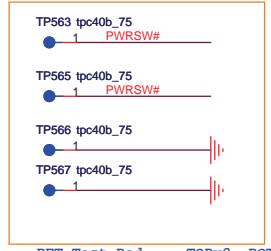
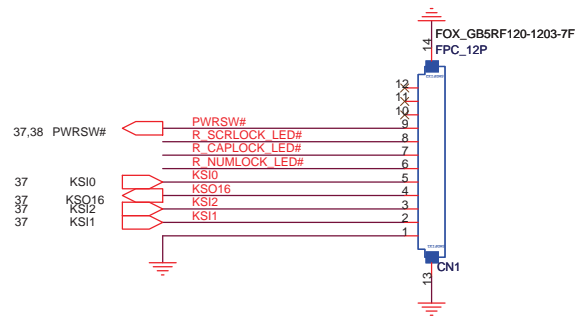
- TP568 tpc40t_50 1 WIRELESS_CHCLK
- TP569 tpc40t_50 1 BT_PR#
- TP570 tpc40t_50 1 BT_LED
- TP571 tpc40t_50 1 BT_PP_SW_L
- TP572 tpc40t_50 1 BT_PN_SW_L
- TP573 tpc40t_50 1 WIRELESS_DATA
- TP574 tpc40t_50 1 BT_3V_R



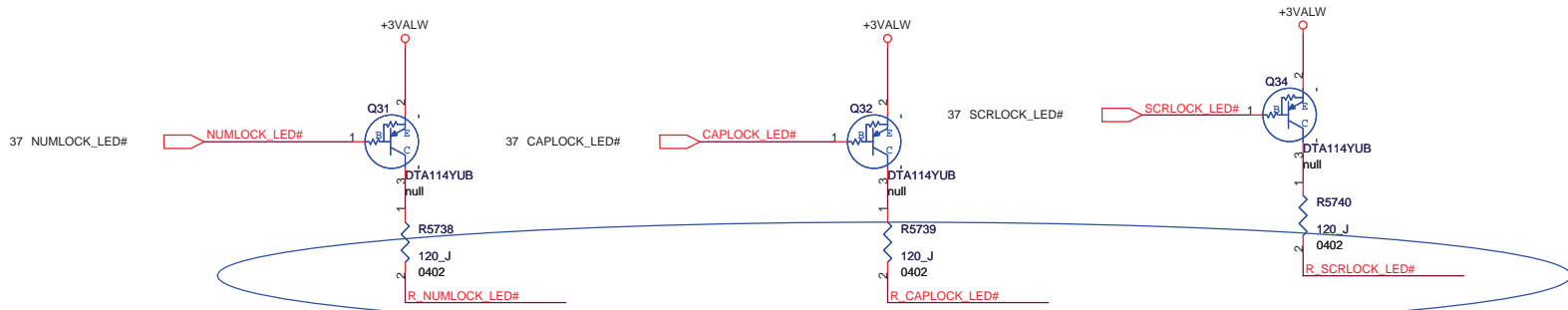
FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title Bluetooth	
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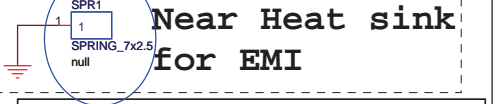
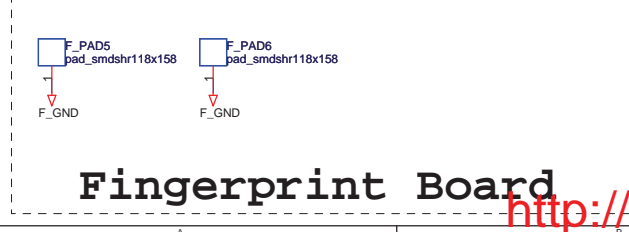
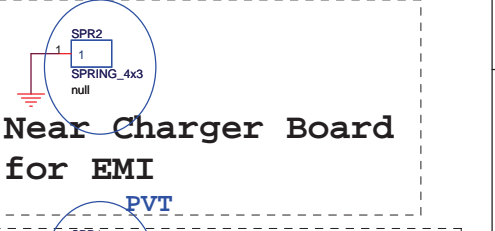
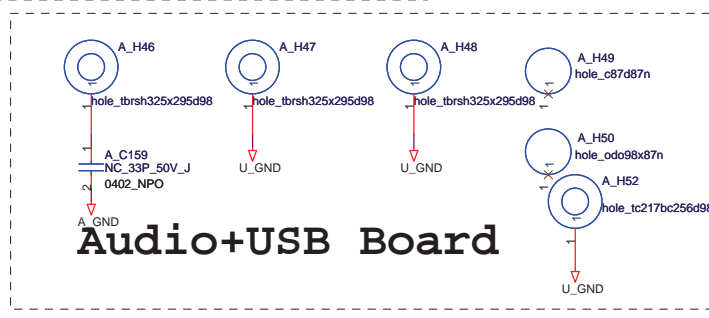
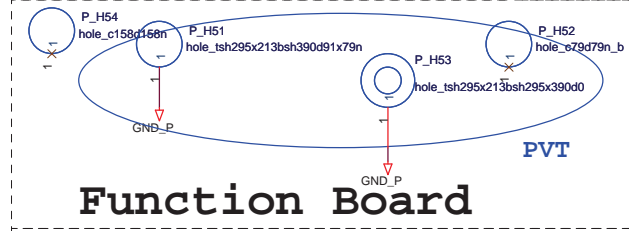
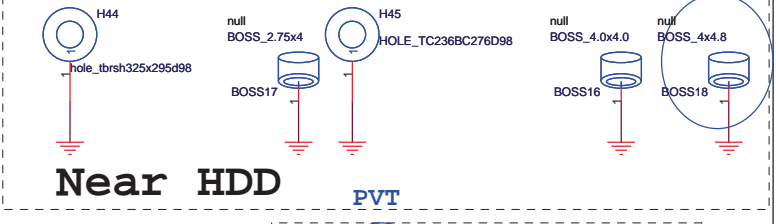
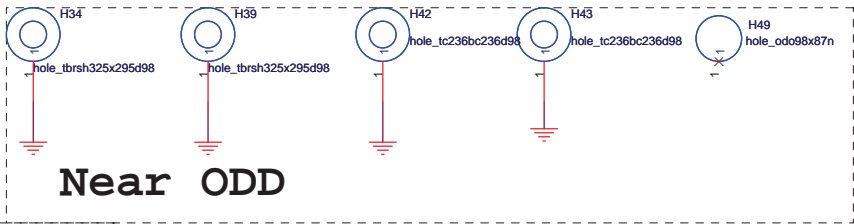
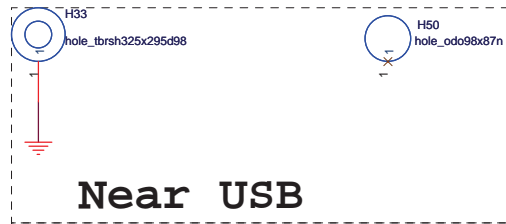
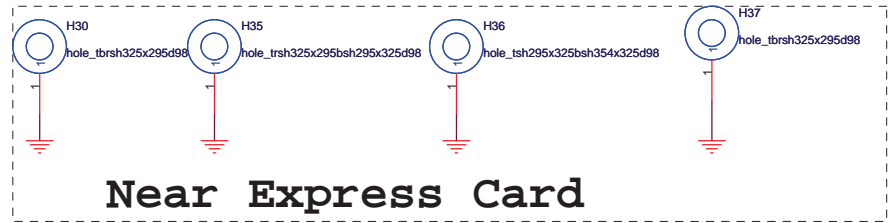
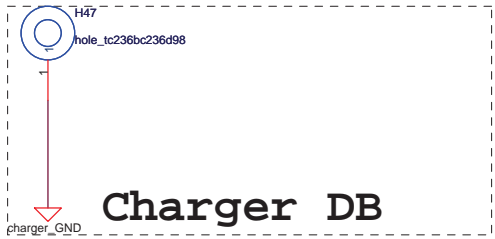
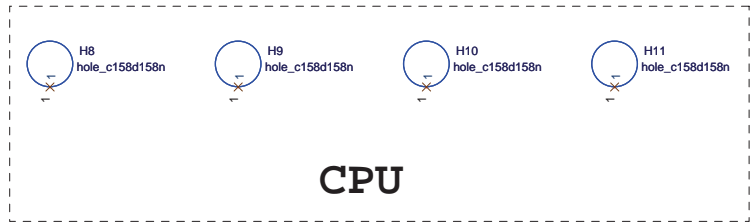
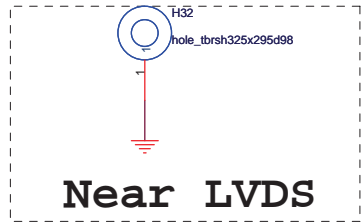
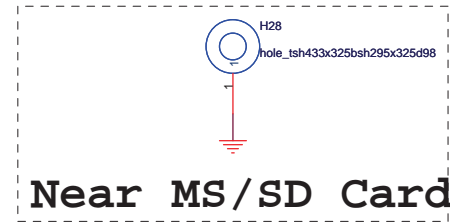
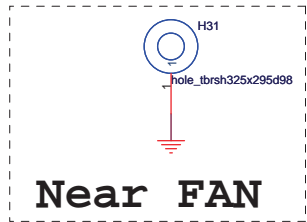
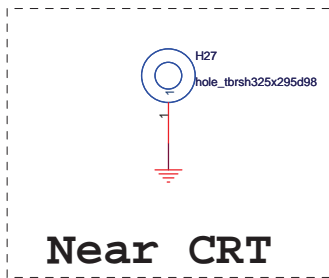
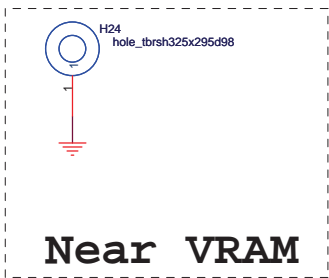
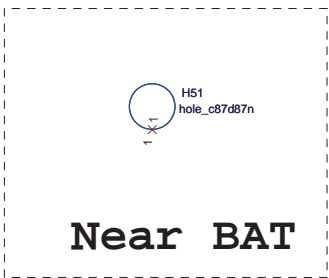
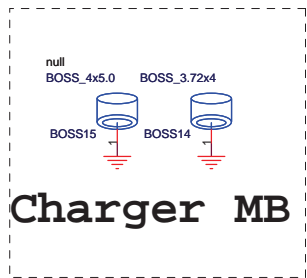
BFT Test Pad --- TOPx2, BOTx2



PVT

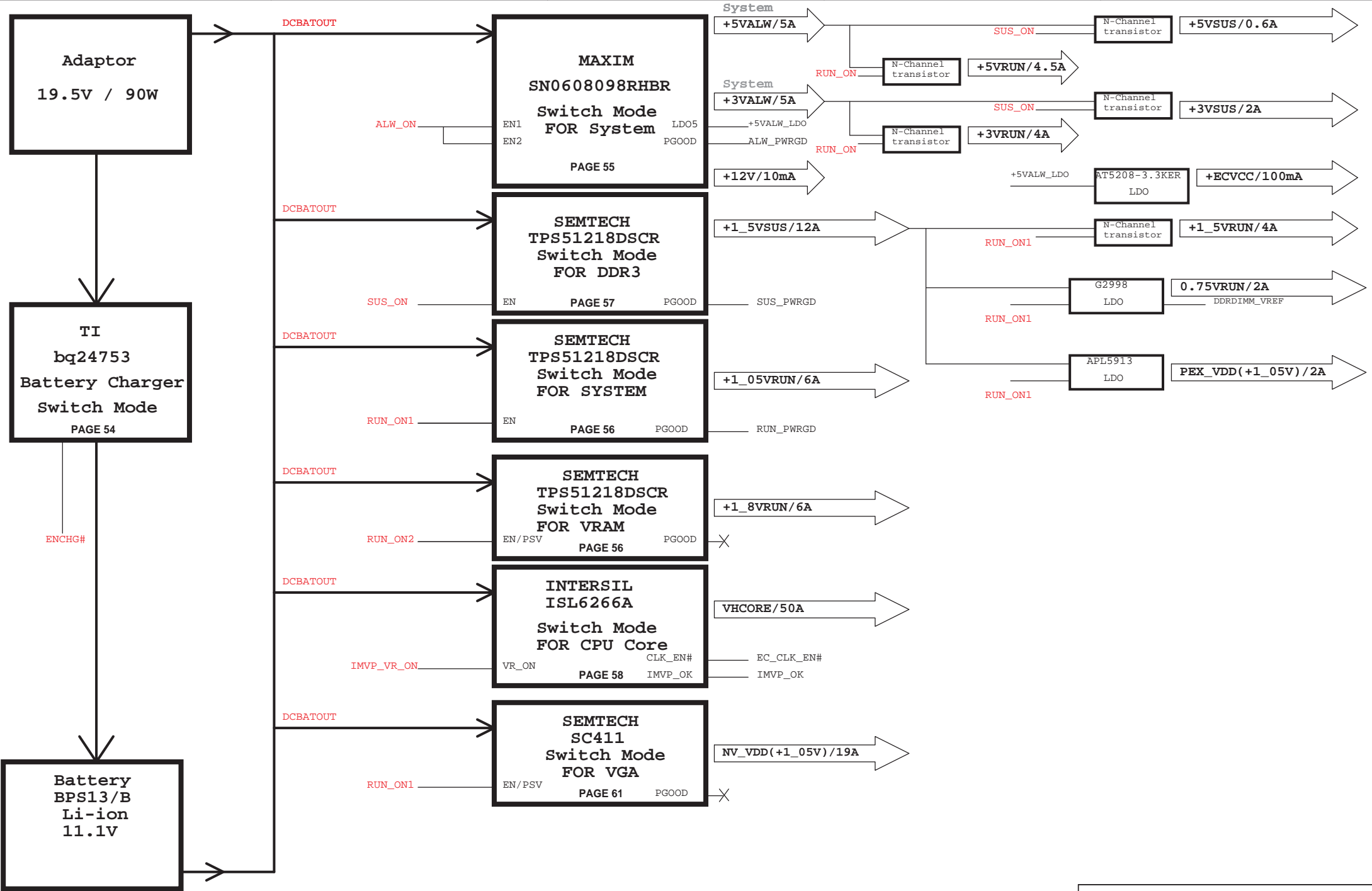
<http://laptop-motherboard-schematic.blogspot.com/>

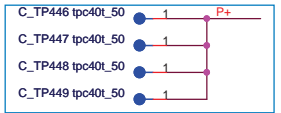
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Power Board MB CONN		
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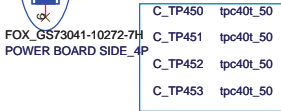
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FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	HOLE	
Size A3	Document Number M870-1-01	Rev 1.0
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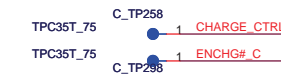




For BFT Test (2 Top, 2 Bottom)

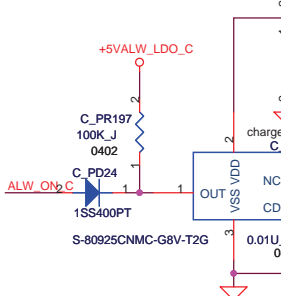


For BFT Test (2 Top, 2 Bottom)



For BFT Test (2 Top, 2 Bottom)

Battery UVP protect



charge current set table:

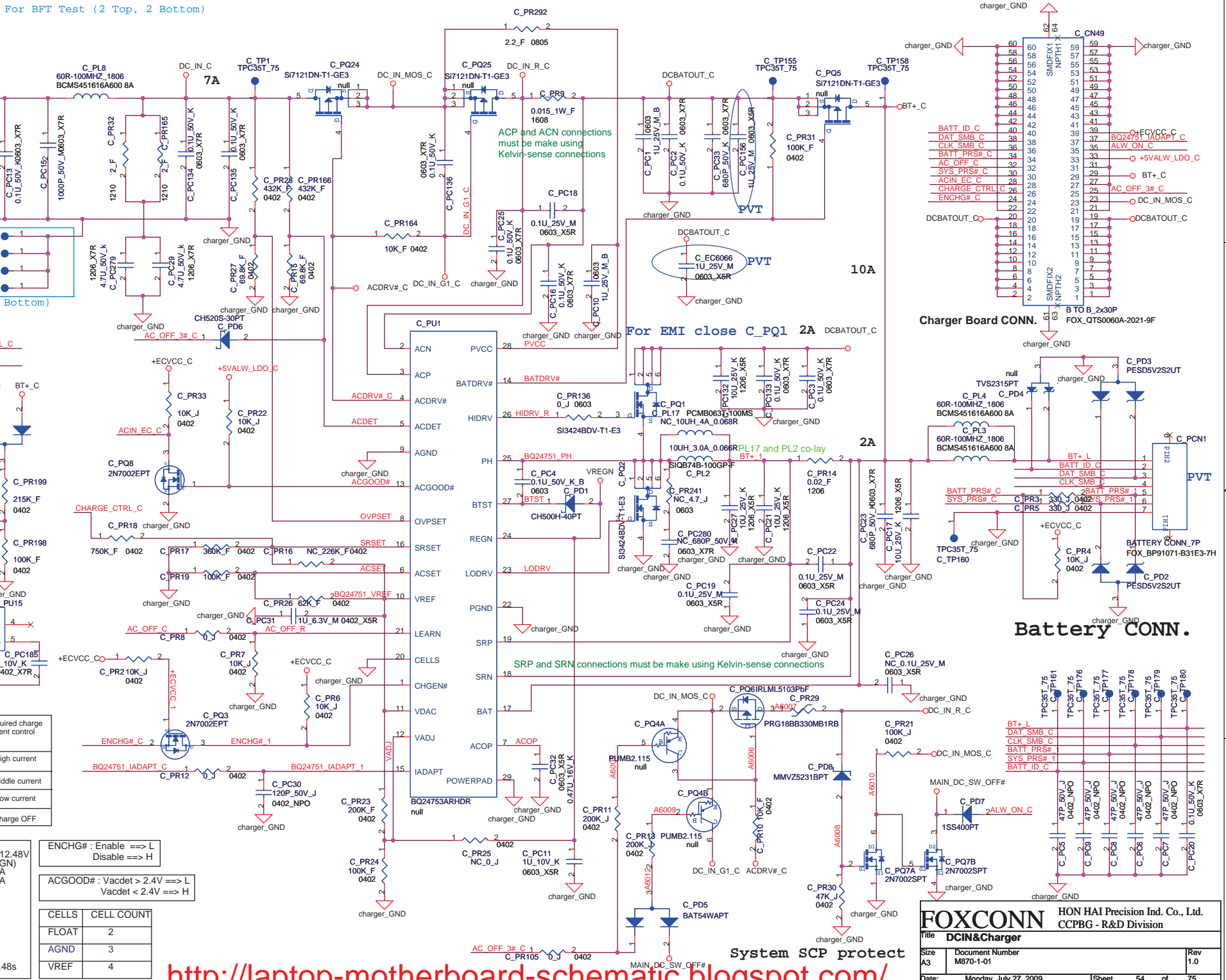
charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREG=3.3V --> Vdac
 $V_{bat} = cell\ count * [4V + 0.5 * (V_{adj} / V_{vdc})] = 12.48V$
 (Vbat=4.2V when Vadj connected to REGN)
 $I_{charge} = (V_{srset} / V_{dac}) * (0.1 / PR14) = 1.5A$
 $I_{adapts} = (V_{acset} / V_{dac}) * (0.1 / PR9) = 4.1A$
 $I_{ADAPT} = (V_{acp} - V_{vacn}) * 20$
 Input OVP : 2.2 - 2V
 Input UVP : 17V
 Battery OCP : Icharge*145%
 Battery OVP : Vbat*104%
 Pre-charge : <2.9V/cell ==> Icharge/8
 Battery OTP : Tshut=155 degree
 Fsw : 300KHz
 Time that input current limit :
 $t = (C_{acop} * 2) / (18uA * V * (PVCC - AC)) = 0.48s$

ENCHG# : Enable ==> L
 Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L
 Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

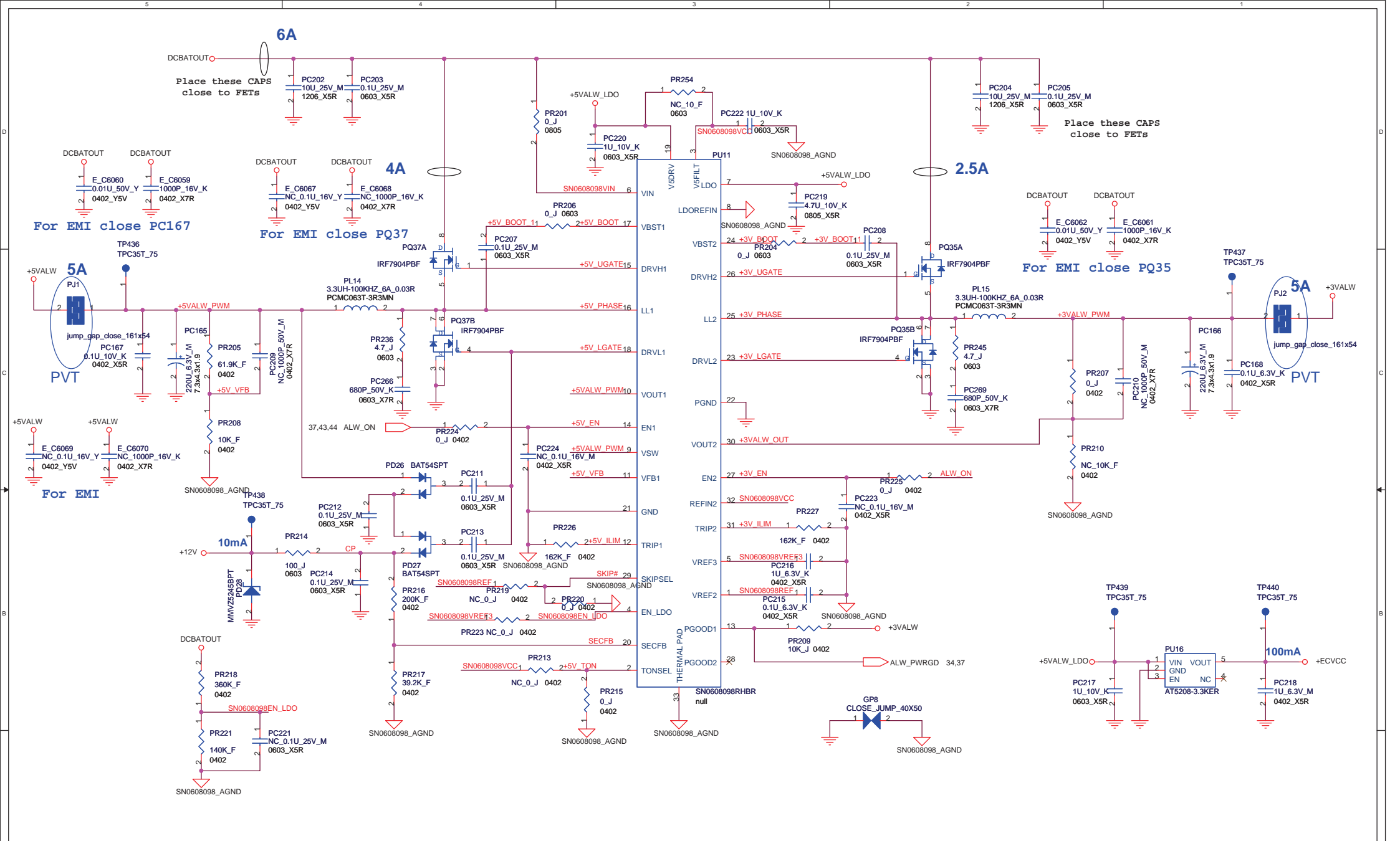


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Title: **DCIN&Charger**

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TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = VOUT(VIN - VOUT) / (VIN * f * LIR * ILOAD(MAX))$$

$$Rocp = (Iocp - Iripple/2) * (10 * Rds(ON)) / 5u$$

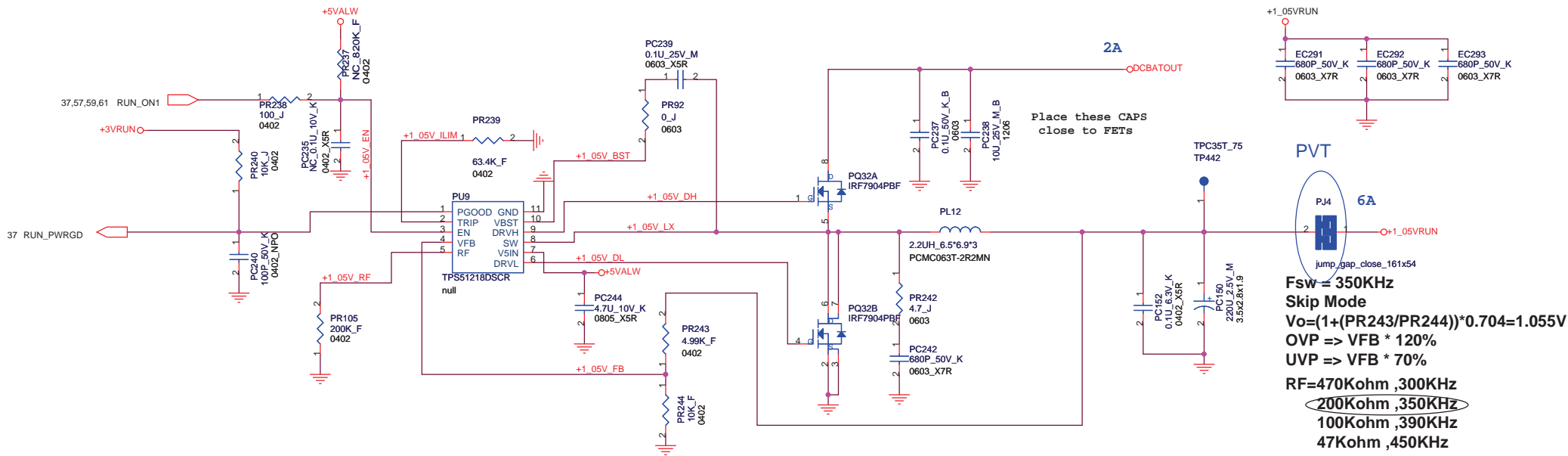
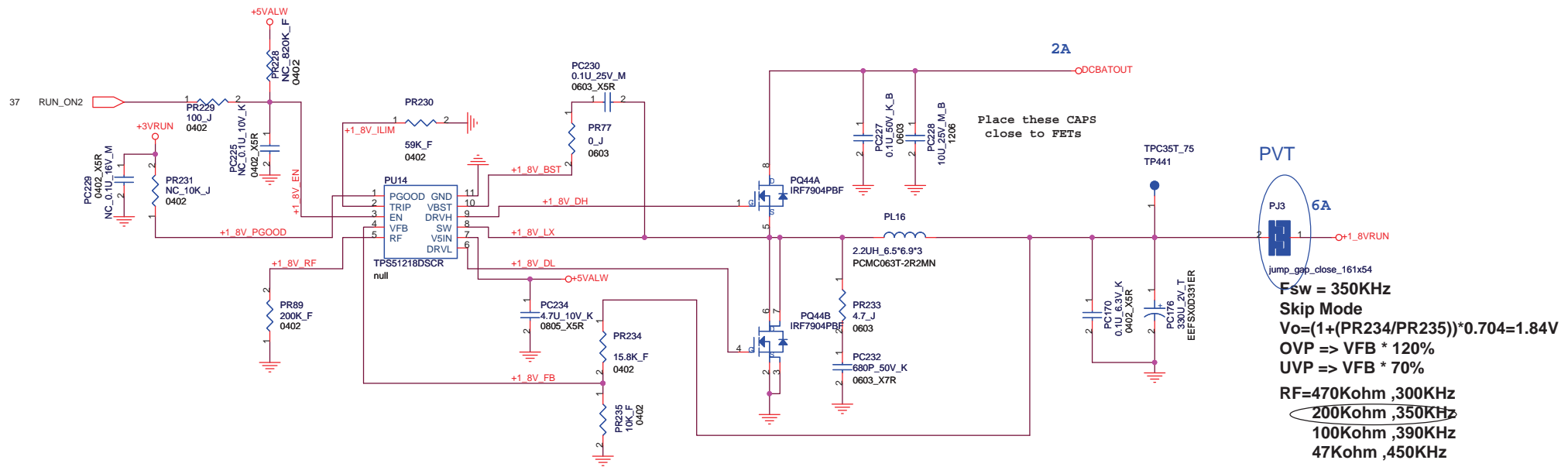
$$+5VALW = ((PR205 / PR208) + 1) * VFB1$$

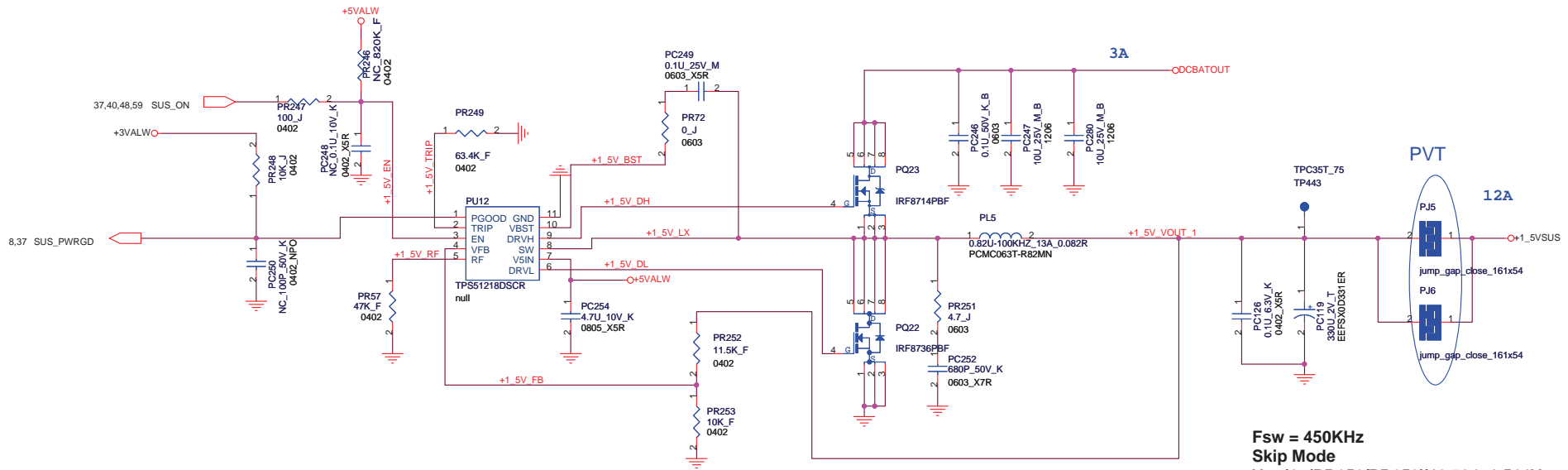
<http://laptop-motherboard-schematic.blogspot.com/>

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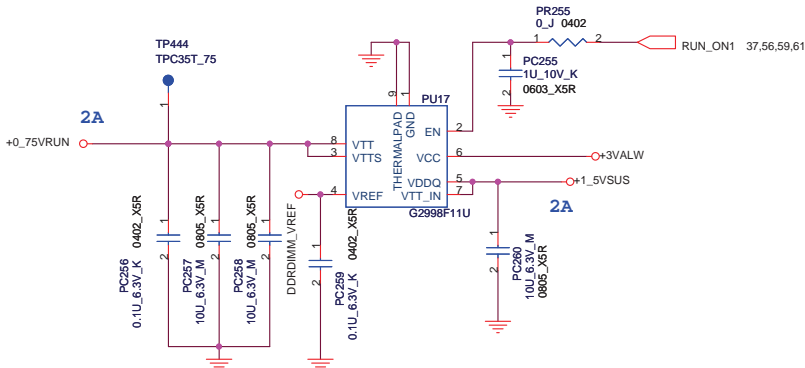
Title: **SYS Power (+3.3V/+5V)**

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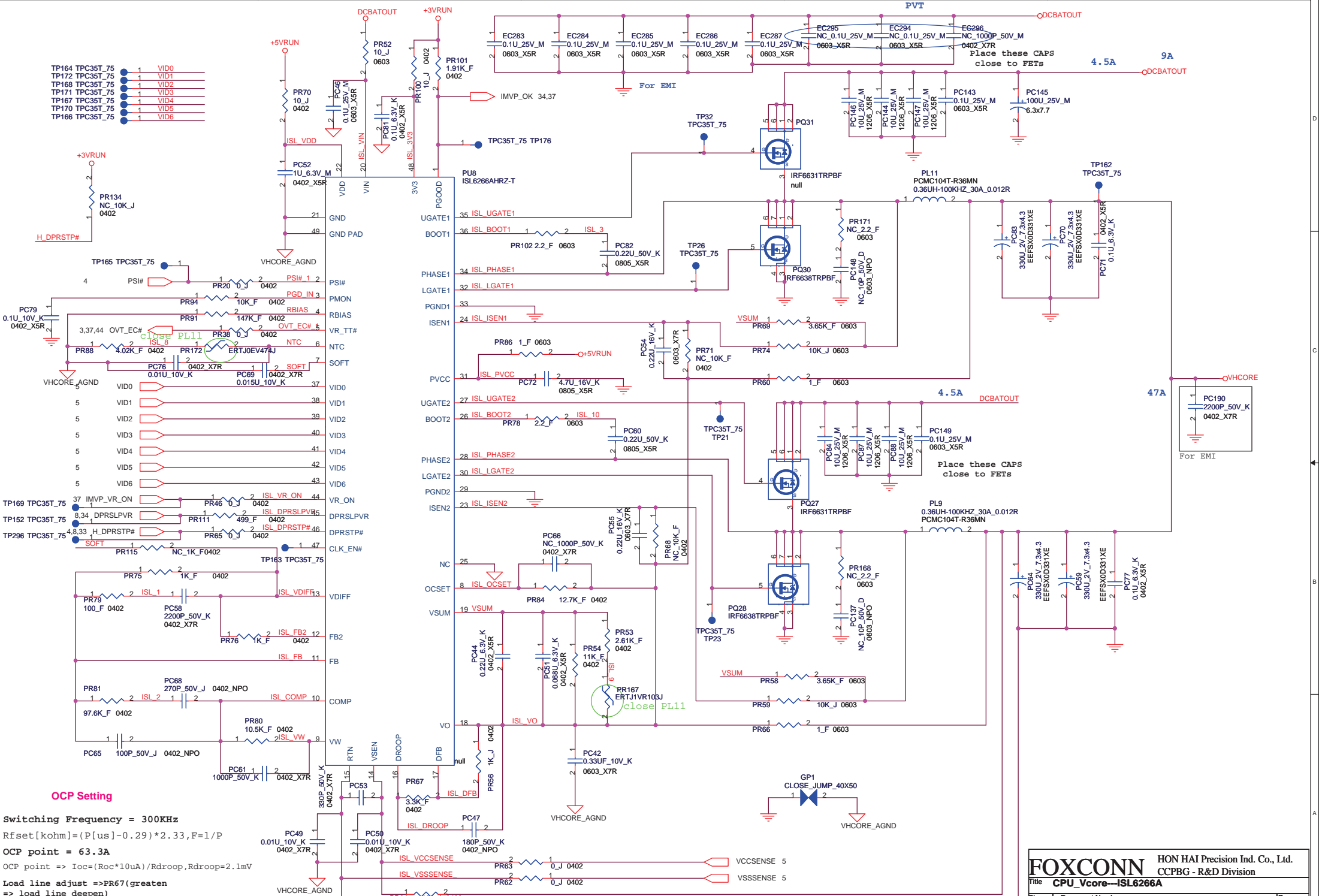


Fsw = 450KHz
Skip Mode
 $V_o = (1 + (PR252/PR253)) * 0.704 = 1.514V$
OVP => VFB * 120%
UVP => VFB * 70%
RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title DDR3 Power(+1.5V/+0.75V)		CCPBG - R&D Division	
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Date:	Monday, July 27, 2009	Sheet	57 of 75

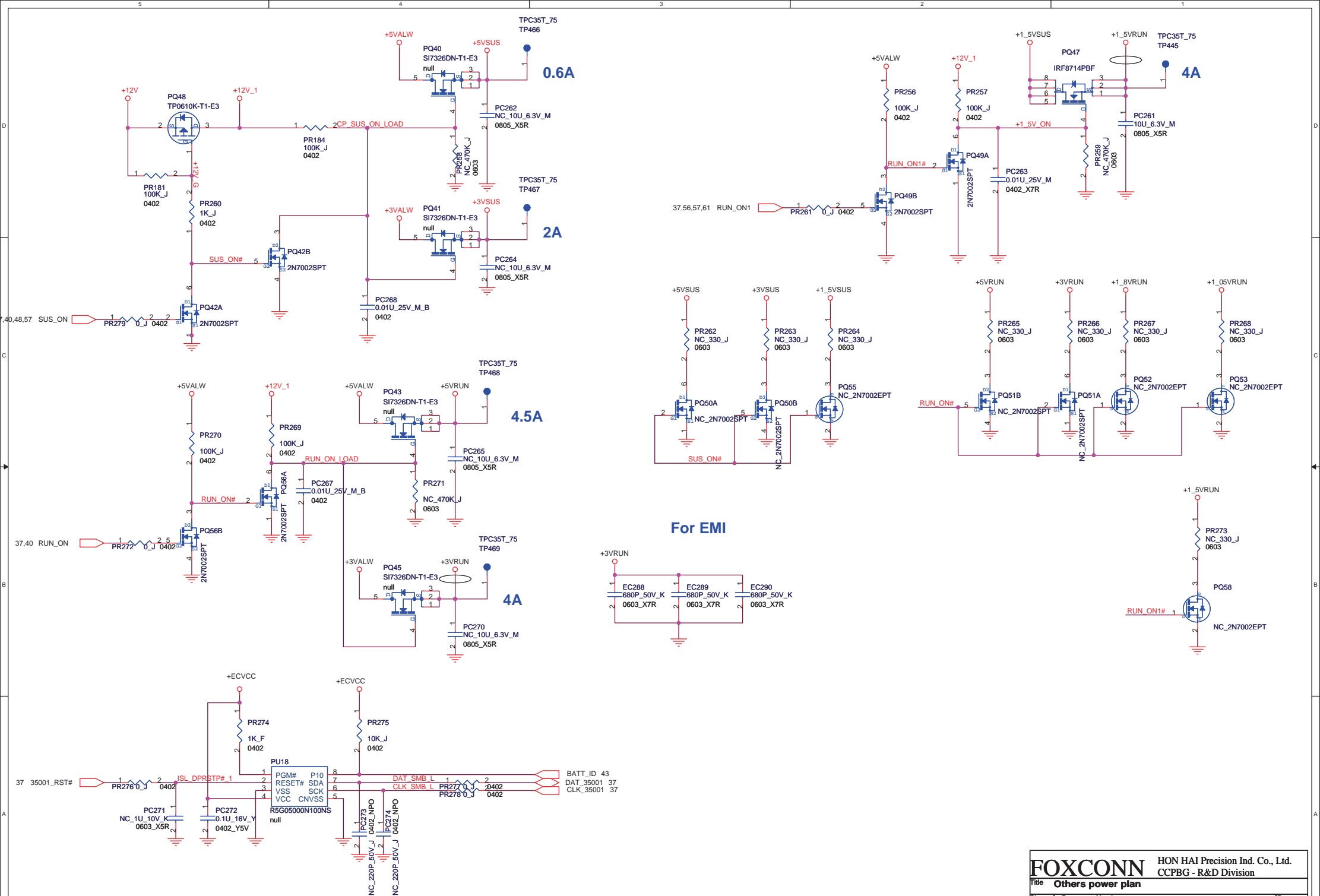
- TP164 TPC35T_75 1 VID0
- TP172 TPC35T_75 1 VID1
- TP168 TPC35T_75 1 VID2
- TP171 TPC35T_75 1 VID3
- TP167 TPC35T_75 1 VID4
- TP170 TPC35T_75 1 VID5
- TP166 TPC35T_75 1 VID6



OCP Setting

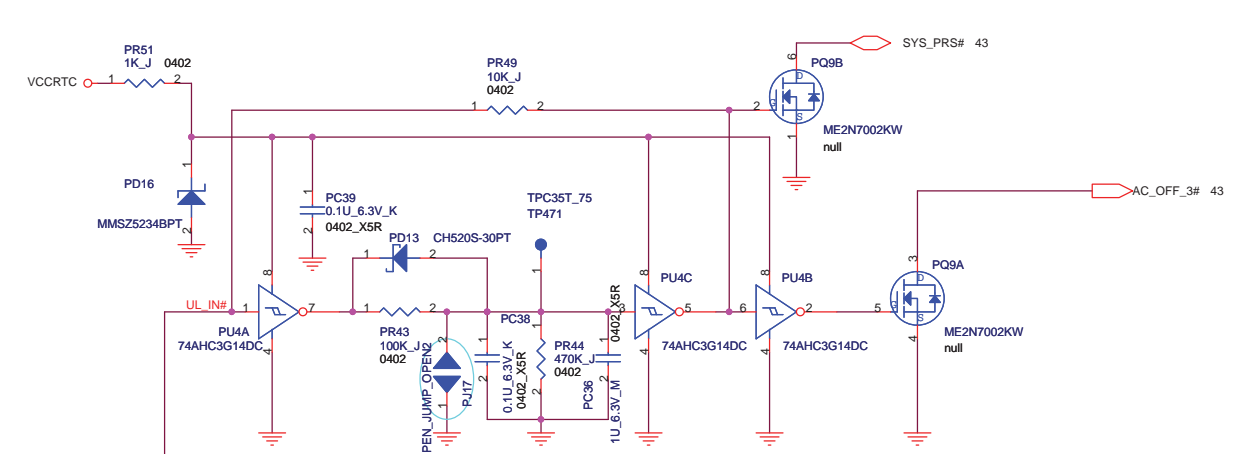
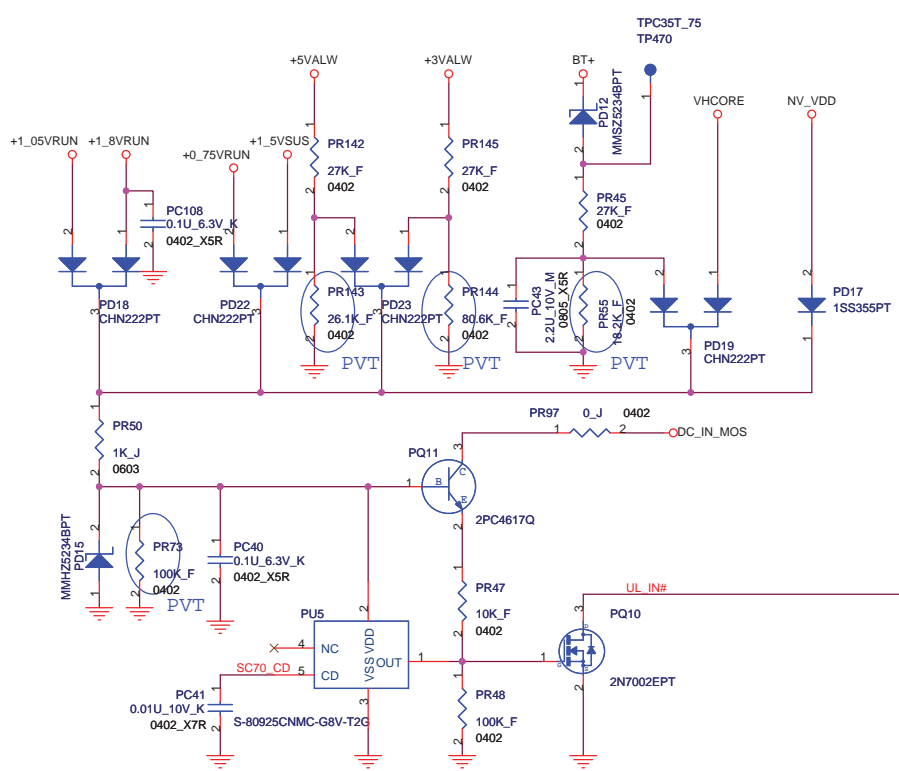
Switching Frequency = 300KHz
 $R_{fset} [k\Omega] = (P_{us} - 0.29) * 2.33, F=1/P$
 OCP point = 63.3A
 OCP point => $I_{oc} = (R_{oc} * 10\mu A) / R_{droop}, R_{droop} = 2.1mV$
 Load line adjust => PR67 (greater => load line deepen)

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Title	CPU_Vcore-ISL6266A	
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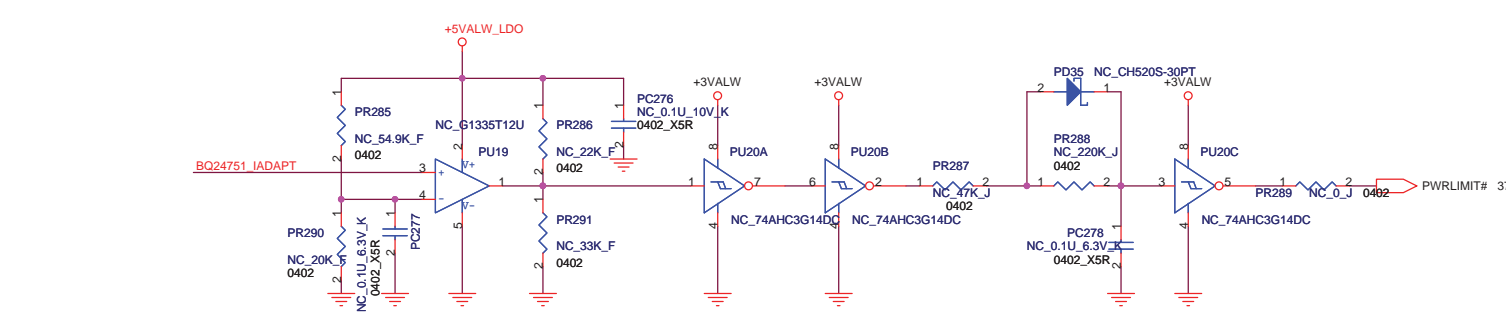
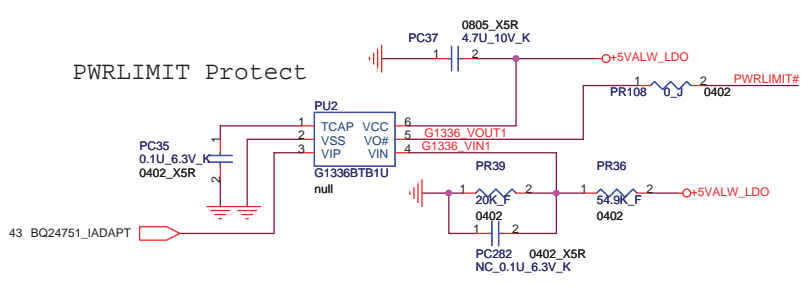


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Title Others power plan		CCPBG - R&D Division	
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PJ17 Near the DDR socket door



VIINP	90W adaptor
PWRLIMIT	1.3V/85W

adaptor max load : 5.7A/3000ms
adaptor OCP : 7.5Amax

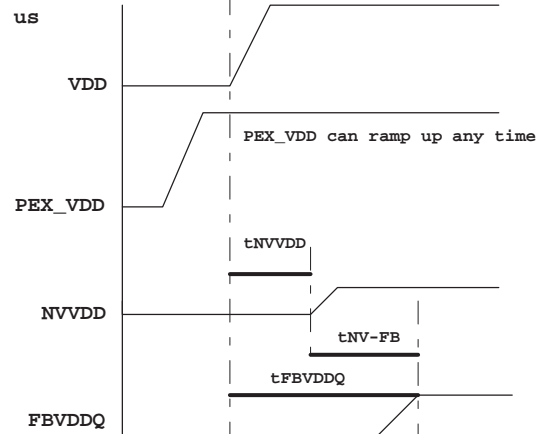
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title **OVP protection**

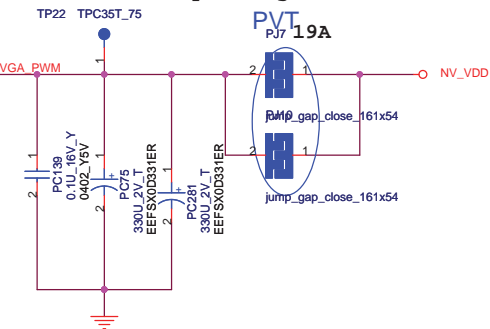
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The ramp time for any rail must be more than 40 us
 $NVVDQ \leq VDD (3.3V + 0.5V)$
 $FBVDDQ \leq VDD (3.3V + 0.5V)$



Recommended Power sequencing order



$V_o = (1 + (PR181/PR184)) * 0.5$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR180) / R_{dson}$
 Operating Frequency : 300KHz
 OVP $\Rightarrow V_{FB} * 116\%$
 UVP $\Rightarrow V_{FB} * 70\%$

N10P-LP	I/O	Inter pull low	GPIO TABLE
PWRCNTL_0	O	Yes	GPU Voltage fix 0.85V

N10M-GS	I/O	Inter pull low	GPIO TABLE
PWRCNTL_0	O	Yes	GPU Voltage H:=1.00V GPU Voltage L:=0.85V

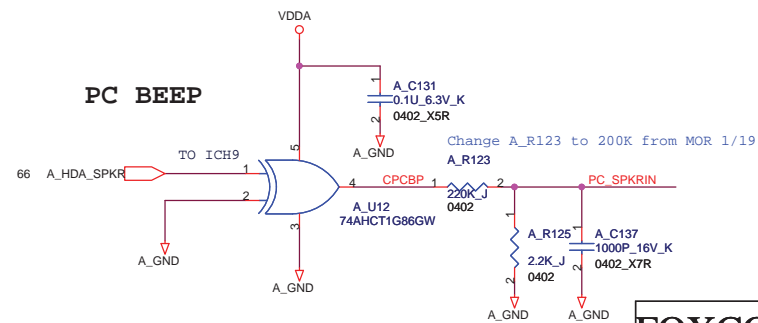
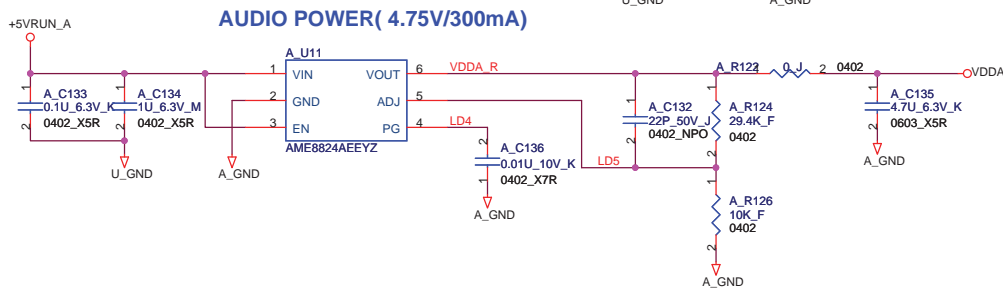
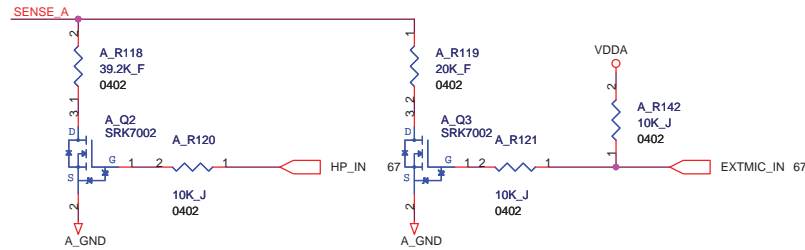
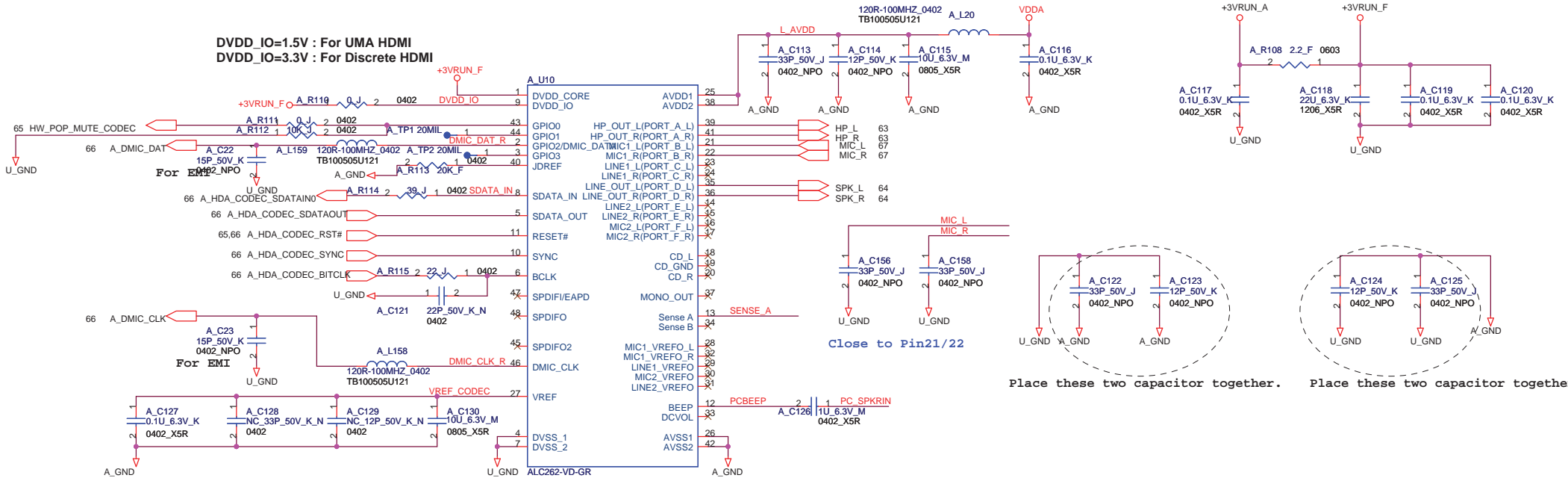
FOXCONN HON HAI Precision Ind. Co., Ltd.
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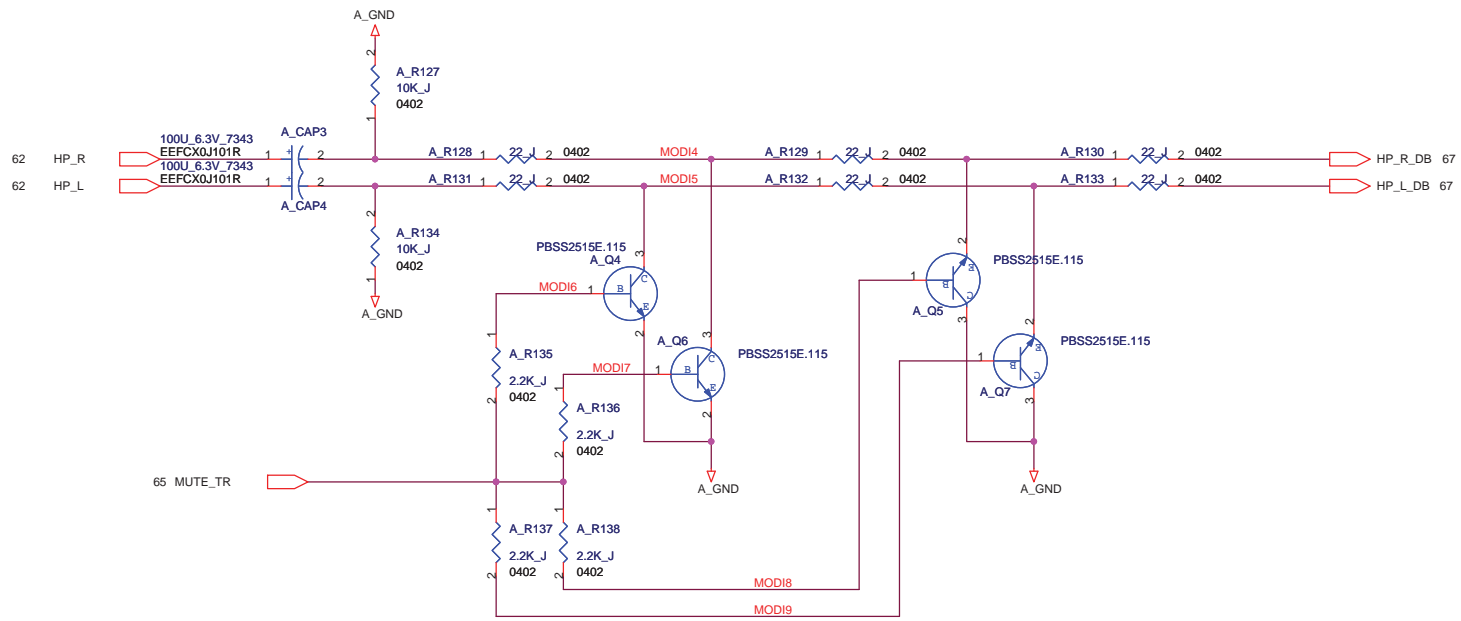
Title: **VGA Power(Fix +1.1V)**

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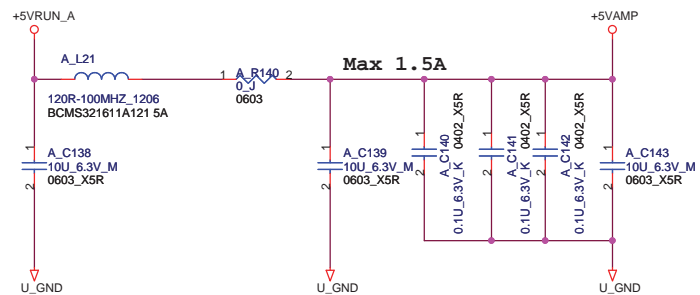
DVDD_IO=1.5V : For UMA HDMI
 DVDD_IO=3.3V : For Discrete HDMI



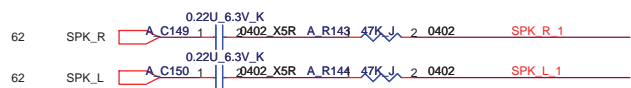
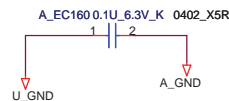


<http://laptop-motherboard-schematic.blogspot.com/>

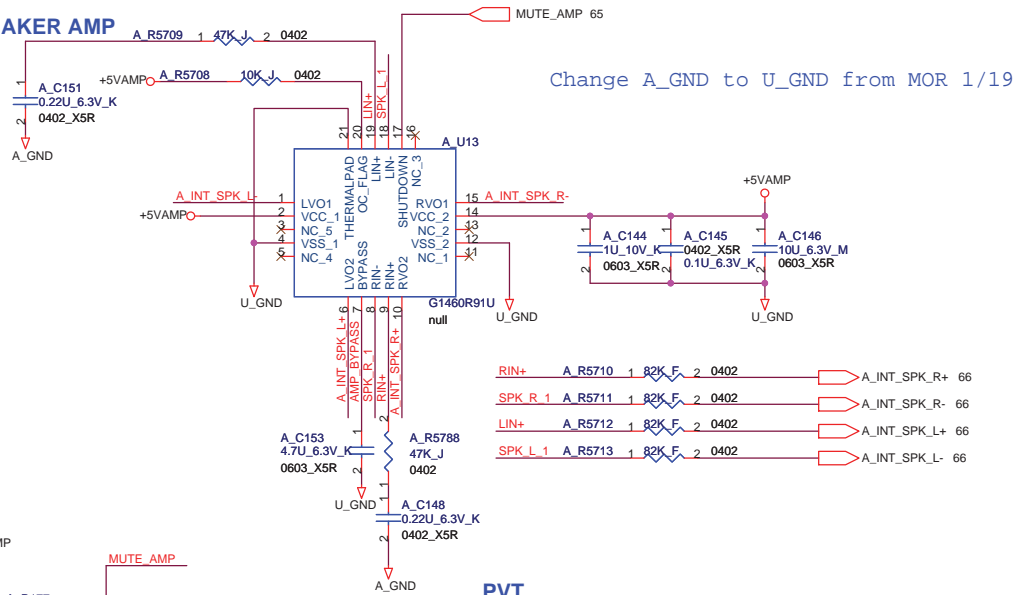
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title Audio (HP)		CCPBG - R&D Division	
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For EMI



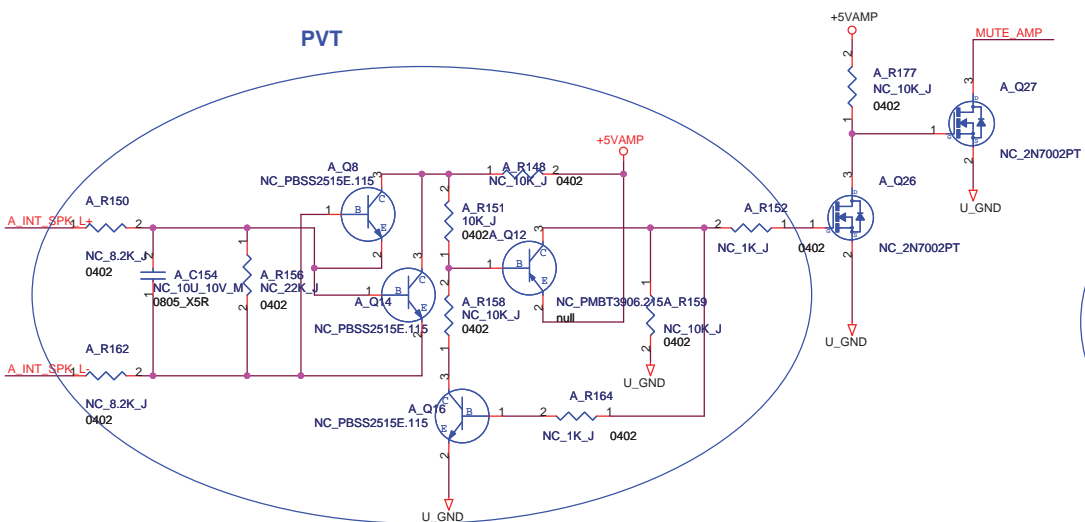
SPEAKER AMP



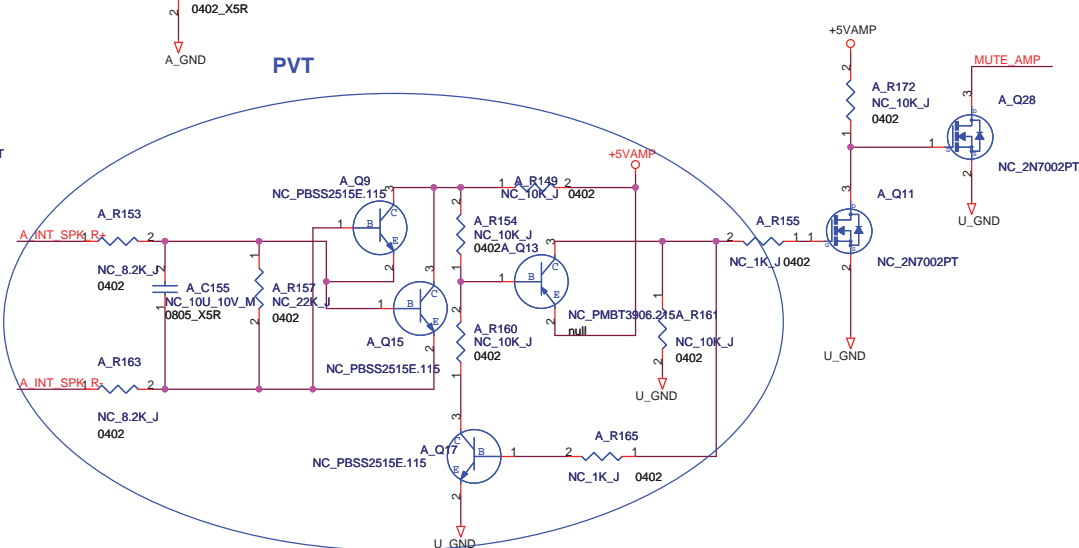
Change A_GND to U_GND from MOR 1/19

- RIN+ A_R5710 1 82K_F 2 0402 → A_INT_SPK_R+ 66
- SPK R 1 A_R5711 1 82K_F 2 0402 → A_INT_SPK_R- 66
- LIN+ A_R5712 1 82K_F 2 0402 → A_INT_SPK_L+ 66
- SPK L 1 A_R5713 1 82K_F 2 0402 → A_INT_SPK_L- 66

PVT



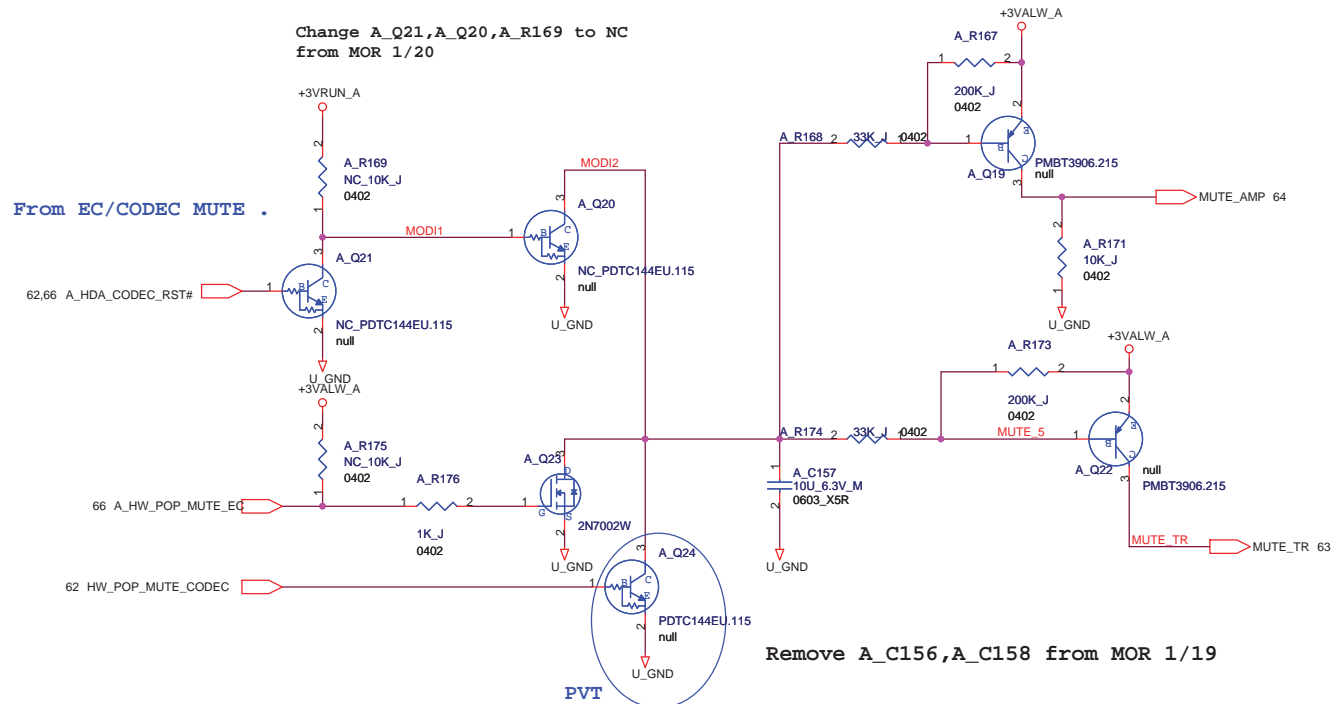
PVT

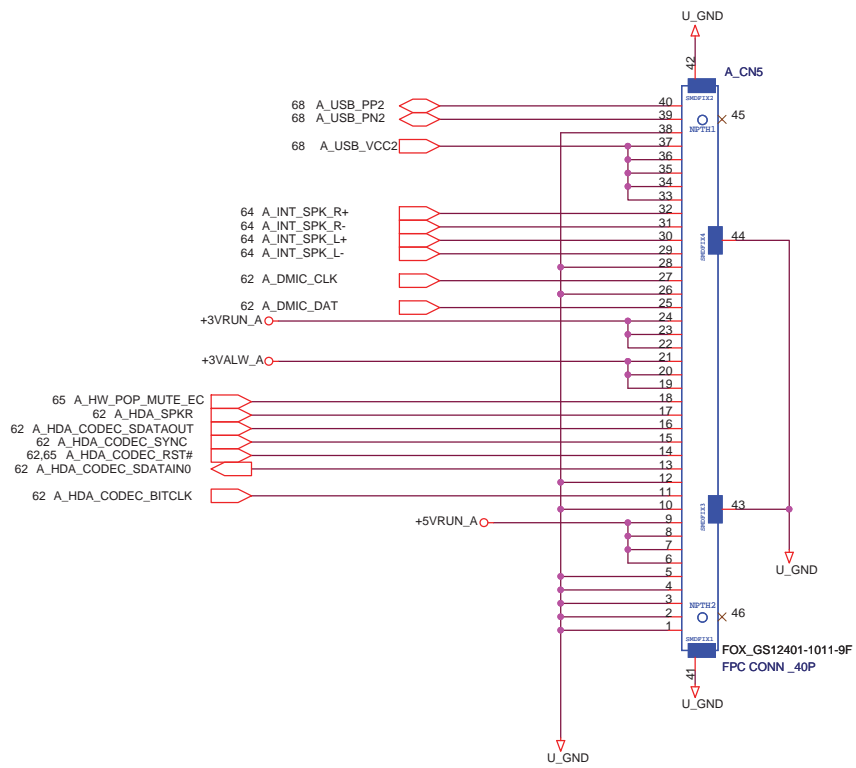


For Mor request, add the speaker cable short protection circuit

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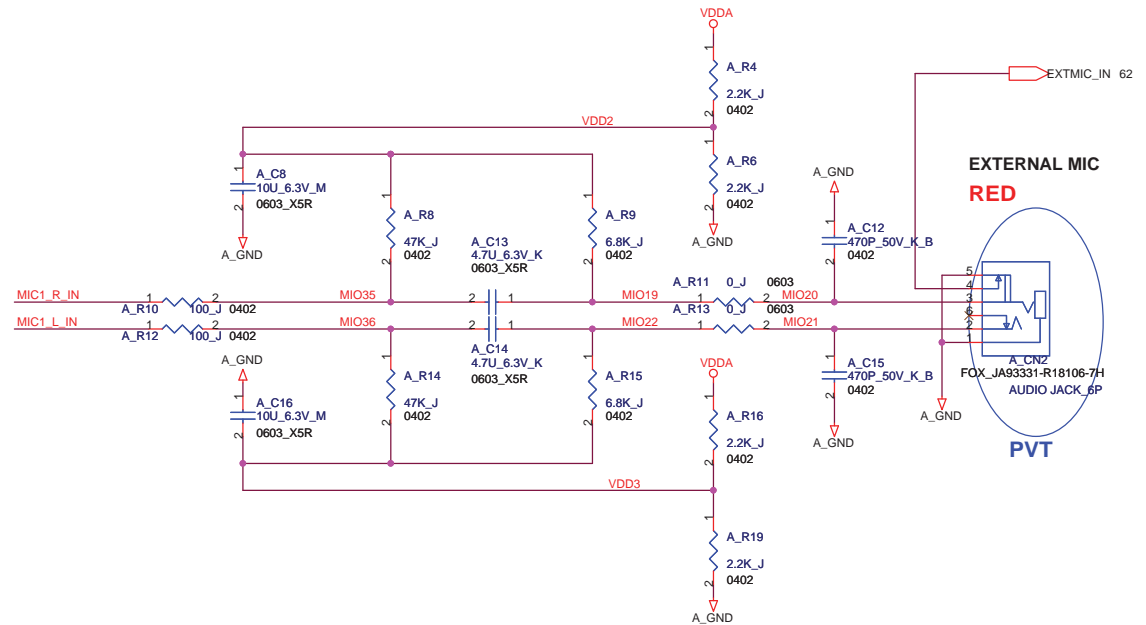
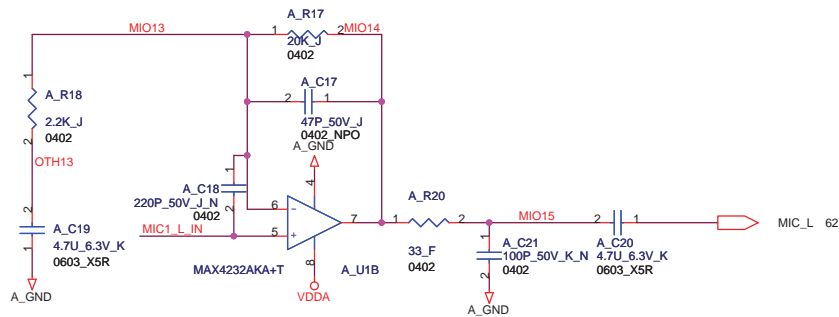
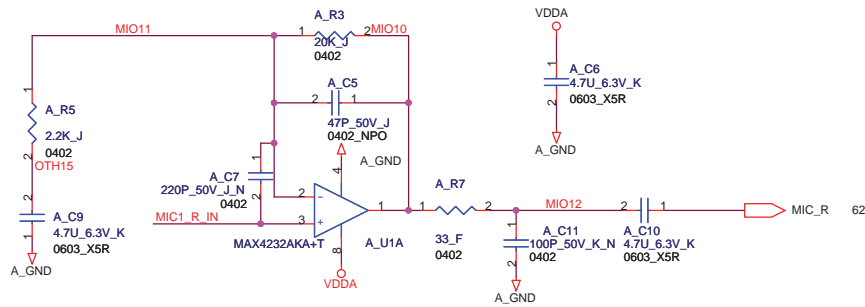
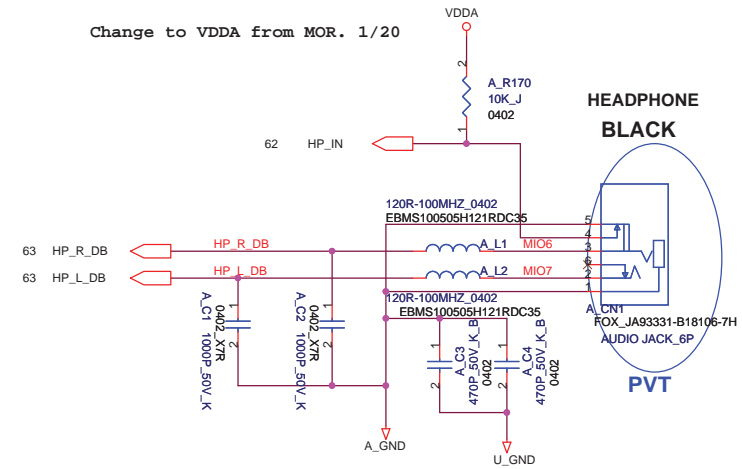
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title Audio (SPKR)		CCPBG - R&D Division	
Size A3	Document Number M870-1-01	Rev 1.0	
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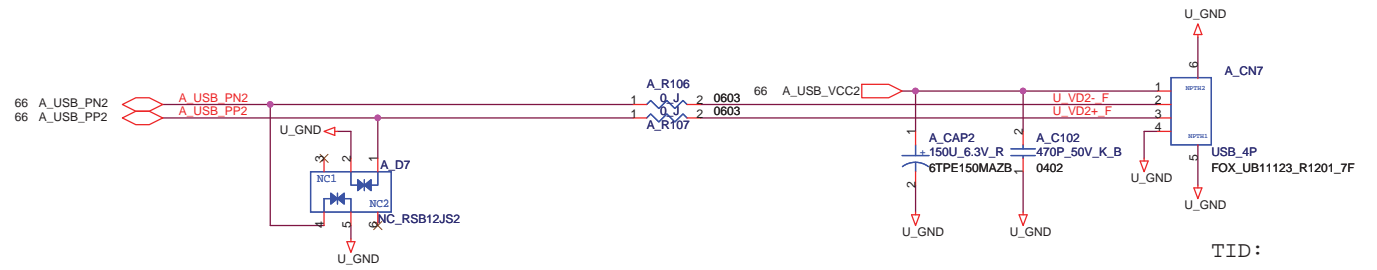




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Title Audio+USB DB CONN		
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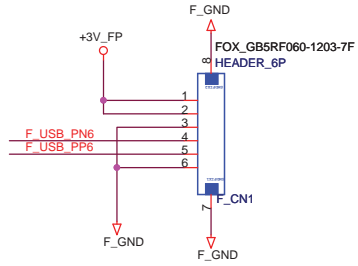
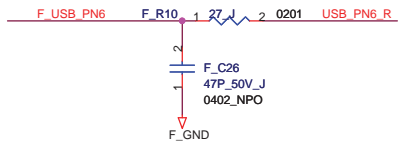
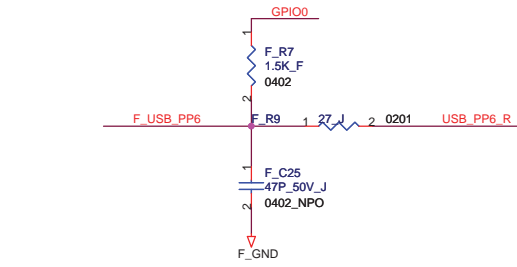
Change to VDDA from MOR. 1/20



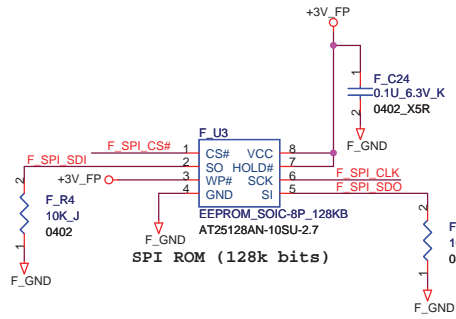
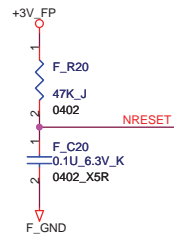
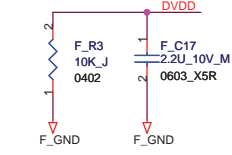
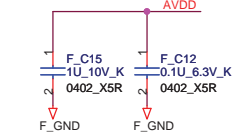
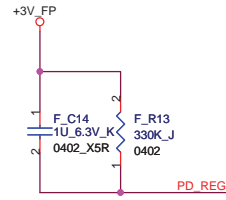


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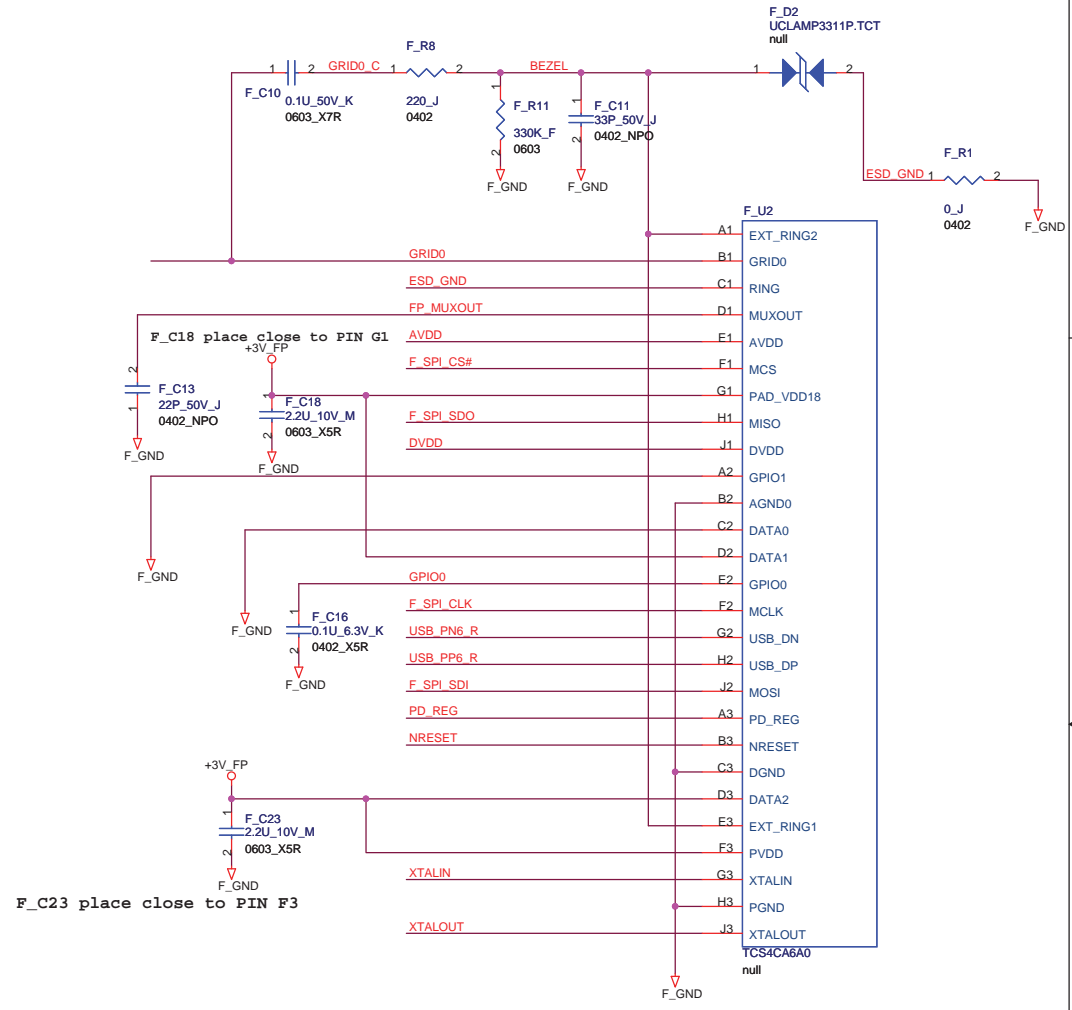
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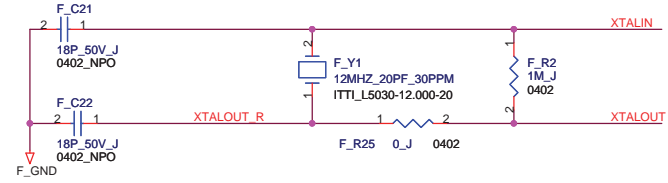
Fingerprint FTB CONN.



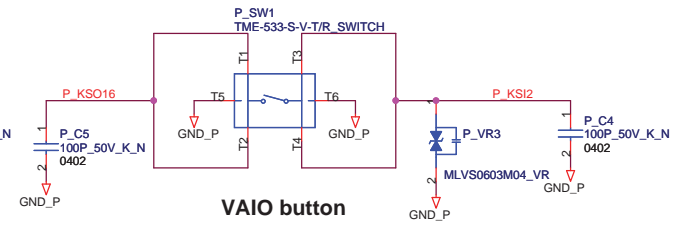
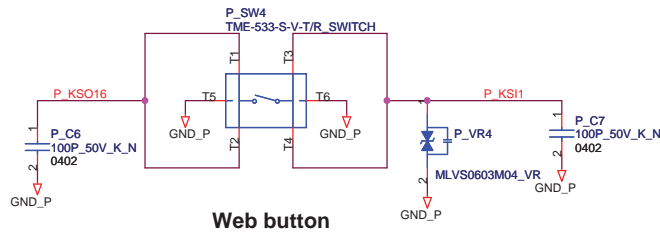
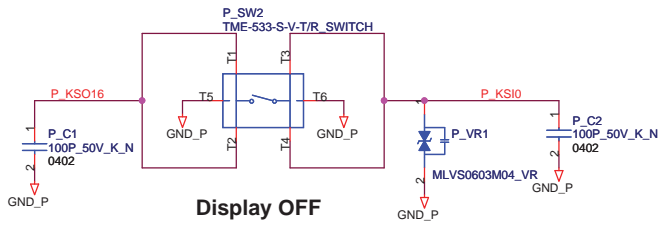
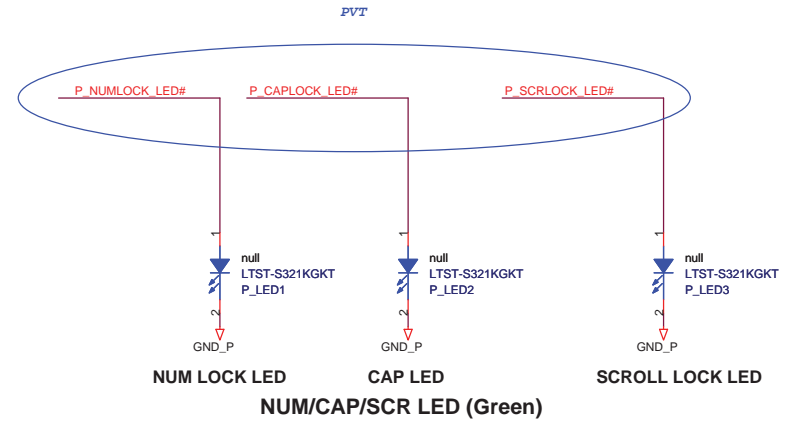
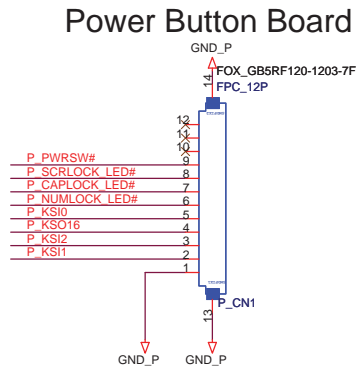
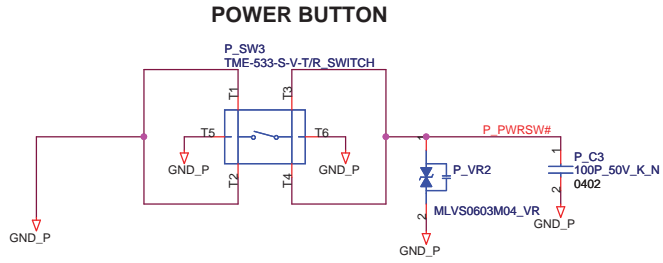
- F_TP5 1 26MIL F_SPI_CS#
- F_TP6 1 26MIL F_SPI_SDI
- F_TP7 1 26MIL F_SPI_CLK
- F_TP8 1 26MIL F_SPI_SDO



F_C23 place close to PIN F3



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(2009/01/08)

- P.37 RP41 pin swap for layout request.
- P.31 RP1-RP4 pin swap for layout request.
- P.30 Reserve R5693 for SW test od del SW1.
- P.41 Change C5183 4.7u to 10u for FAE suggestion.
- P.33 Change D4 footprint for SMT request.
- P.34 Change D5,D6,D8 footprint for SMT request.
- P.35 Change D7,D14,D16 footprint for SMT request.
- P.37 Change D17,D18 footprint for SMT request.

(2009/01/09)

- P.44 Change R200 from 150 ohm to 100K.C286 change to 0402.
- P.50 Modify MS/SD LED circuit of active low schematic.
- P.06 Del R547,R556 for FAE suggestion.
- P.09,17 Change PCIE cap to 0402 size.
- P.46 Add 0 ohm resistor for SD Data.
- P.45 Add 0 ohm resistor for MS Data.
- P.64 Change SPK AMP circuit.
- P.41 Add C5252,C5253,C5254,C5255 for FAE suggestion.

(2009/01/10)

- P.03 Add Test point for CPU side (TP34,TP38)
- P.69 Change F_U3 to AT25128AN-10SU-2.7.

(2009/01/12)

- P.37,43 Add LED control signal for MOR request.
- P.64 Add A_R5708,A_R5709,A_R5710,A_R5711,A_R5712,A_R5713 for FAE request.

(2009/01/13)

- P.18 Add C878 change L74 for demo circuit.
- P.23 Remove R4813,R4802,R4803,R4804,C5127 from FAE.
- P.20 Change C1390 to 1u.
- P.16 Remove C1322
- P.20 Change R5265 to 10K ohm from Design guide.
- P.58 Add PC145 for power suggestion.
- P.41 Change C5184,C5185 cap size to 0402.
- P.69 Change F_C12,F_C16,F_C20,F_C24 size to 0402.
- P.46 Change C1985 size to 0402.
- P.70 Change P_LED1,P_LED2,P_LED3 to HT-170UYG for PE suggestion.
- P.50 Change LED9 to HT-170UD,LED2,LED8,LED6 to HT-170UY for PE suggestion.
- P.32 Change PCIE port, port3 for cardreader,port4 for Express from MOR suggestion.
- P.50 Add Q59,Q60 for power and suspend LED control.
- P.24 Add C5195,C5199 for DG.
- P.15 RP36,RP34,RP33,RP38 pin3,4 swap for layout.
- P.20 Change C5240 for PUR request.
- P.24 Change C5243,C5246 for PUR suggestion.
- P.30 Change C1264 for PUR suggestion.
- P.69 Change F_C10 for PUR suggestion.
- P.69 Change F_C28 size to 0402.

(2009/01/14)

- P.37 Add R5708 for power request.
- P.62 Add A_R117 and reserve A_C22,A_C23,A_CN3,change A_R116 for EMI suggestion.
- P.50 Modify power and suspend LED schematic.
- P.42 Change CN13 to LD2722F-S08L6 for ME request.
- P.54 Change PCN1 to BP91071-B71E3-7F for ME request.

(2009/01/15)

- P.62 Delete A_C112,A_R109.
- P.43,66 Modify DB conector pin define.
- P.21 Change R5269 value to stuff from MOR suggestion.

(2009/01/15)

- P.31 {HDMI}Delete R515,R538 because double pull-high.
- P.18/19 {VGA}Remove R5576,R5579,R5577,R5580
- P.62 {Audio}Change A_R112 to 10K and add A_R142 from MOR request.
- P.64 {Audio}Remove A_R150,A_R162,A_R153,A_R163.
- P.65 {Audio}Remove A_R172 because have double resistor.
- P.16 {VGA}Remove C5124.Add C1303 for DG.
- P.22 {VGA}Remove R5300 from FAE suggestion.
- P.17 {VGA}Add R5251 for N10P-Lp deivce ID 0x0A2A.
- P.43 {LED}Move LED circuit to MB.

(2009/01/19)

- P.55 {3V/5V}Add PR236,PR245,PC266,PC269 for EMI request.
- P.62 {Audio}A_CN3 For EMI Request.
- P.12 {Cantiga}Remove R211 from MOR request
- P.30 {LVDS} Change L43 to 600R-100MHZ_0805 from MOR request.
- P.37 {EC} Add 10K pull-high resistor for INST_ON_SW.
- P.30 Change SW1 to HDS406-021E_SW-SMD12 for INST_ON_SW function.
- P.45 {Cardreader} Add R818,C864 MOR request (For noise reduction).
- P.45 {Cardreader} Change C489 to 1u MOR request.
- P.46 {Cardreader} Change C1981 to X5R MOR request.
- P.46 {Cardreader} Remove R5377 for MOR request.
- P.65 {Audio}Remove A_C156,A_C158 from MOR request.
- P.62 {Audio} Change A_R123 to 200K from MOR request.
- P.64 {Audio} Change A_5709,A_5788 to 47K,A_C148,A_C151 to 1U from MOR request.

- P.26 {VRAM} Add C23,C25,C26,C28 For 2.4GHz noise.
- P.25 {VRAM} Add C30,C31,C32,C45 For 2.4GHz noise.
- P.16 {VGA} Add C46,C47,C48,C49,C50 For 2.4GHz noise.
- P.11 {Cantiga} Add C21,C53,C54 For 2.4GHz noise.
- P.14/15 {DDR3} Modify to DDR3 circuit from MOR request.

(2009/01/20)

- P.60 {OVP} Remove PD10 from MOR request.
- P.08 {Cantiga} Add U43, C820, R568,R582 to solve SUS_PWRGD level drop issue.
- P.37 {EC} EXT_DEV_SENSE change to GPIO33 from EC request.

(2009/01/23)

- P.45,46 {Cardreader} Change CN35,CN16 connector from ME request.
- P.34 {ICH9} Add R5714 for GPU ES sample.
- P.17 {VGA} Change R5251 to 15K,Add R5716 15K for FAE request.
- P.38 {EC} Add 1K pull-high from Vendor suggestion.
- P.43 {LED} Change LED power plan from 3V to 5V from MOR suggestion.
- P.17 {VGA} Change R5249 to 45.3K.

(2009/02/05)

- P.38 {SPI} Change U12 to MX25L1605DM2I-12G.
- P.21 {VGA} R5269 to no stuff from MOR request.
- P.22 {VGA} Reserve R5717 from MOR request.
- P.30 {LVDS} Change U29.1 to INV_EN from MOR request.(LCD timing)
- P.21 {VGA} Reserve R5718(+3VRUN) for IOVDD backup from MOR.

(2009/02/16)

- P.42 {SATA} Change CN13 HDD CONN from ME request.
- P.21 {VGA} Add C5138 for design guide v03.
- P.31 {HDMI} Delete LEVEL SHIFTER circuit from MOR.
- P.56 {+1_8V/+1_05V} Change PL12 to PCMB053T-1R5MS for Power request.
- P.45 {Cardreader} Change PCIE Head connector.
- P.43,69 {Fingerprint} Change Fingerprint CONN to 6pin for layout sapce.

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(2009/02/19)

- P.24 {VGA Power} Delete C5246,C5207,C5210
Add C6038,C6039,C5201,C6040,C6041 from DG v04.
- P.25 {VRAM} Delete R5336,R5720,R5344,R5721 Add R5724,R5725
from DG v04.
- P.26 {VRAM} Delete R5350,R5723,R5351,R5722 Add R5726,R5727
from DG v04.
- P.18 {VGA} Delete C876,C6018,C6016,C6017,C6019 for M and L board.
for N10M.
- P.18 {VGA} Delete C879,C6012,C6006,C6010,C6011 for M and L board.
for N10M.
- P.21 {VGA} Change L70,L77 to 180R from DG v04.
- P.21 {VGA} Change L75 to 220R from DG v04.
- P.21 {VGA} Change C5132 to 1U from DG v04.
- P.20 {VGA} Change C5200 to 1U and add C5202 from DG v04.
- P.20 {VGA} Change L155 to 220R from DG v04.
- P.20 {VGA} Add C1395,C1397,C1396 from DG v04.
- P.14 {DDR} Change CAP13,C222,C219,C196,C221 to stuff.
- P.15 {DDR} Change C202,C179,C197 to stuff.
- P.54 {Charger} Reserve PQ14,PD9 and PR34.
- P.41 {LAN} Change L5 to LFE9249-R for PUR request.
- P.70 {Power Board} Change P_SW1~P_SW4 to TME-533-S-V-T/R_SWITCH
from PUR request.
- P.38 {SPI} Change R269 to 8.2K from FAE.

(2009/02/23)

- P.50 {LED} Change LED2,LED6,LED9 for ME request.
- P.49 {BT} Change BOSS11,BOSS12 to A40M20-31BS for ME request.
- P.52 {HOLE} Change BOSS14 to A40M20-40BS for ME request.
- P.39 {WLAN} Change BOSS1,BOSS2 to A40M20-30BS for ME request.
- P.39 {WLAN} Change SW4 to 1BS007-12120-002-7F fro ME request.
- P.39 {WLAN} Change CN21 to AS0B226-S52N-7F fro ME request.
- P.68 {USB/DB} Change A_CN7 to UB11123_R1201_7F for ME request.
- P.16 {VGA} Change L73 to 100NH from DG v04.
- P.18 {VGA} Change L74 to 300R from DG v04.
- P.50 {TP} Change F7 to 6V-0.25A_1206 from MOR request.
- P.21 {VGA} Change L71 to 300R from DG v04.
- P.20 {VGA} Change L76 to 300R from DG v04.
- P.20 {VGA} Change L81,L83 to 100NH from DG v04.
- P.42 {HDD} Change CN13 to LD2522H-S02 from ME request.
- P.42 {ODD} Change CN25 to LN27133-F408-9F from ME request.

(2009/02/24)

- P.69 Change F_D2 to UCLAMP3311P.TCT.
- P.22 {VGA} Delete R5297,R5296.
- P.47 {CAM} Change U41 to MAX4789EUK+T.
- P.31 {HDMI} Delete RP1,RP2,RP3,RP4 from FAE suggestion.
- P.24 {VGA} Change C6040,C6041 to 0.22U_6.3V_K from PUR suggestion.

(2009/02/25)

- P.18 {VGA} Remove U56.J27 reserve circuit from FAE suggestion.
- P.30 {LVDS} Change CN18 to GS12401-1011-9F from ME request.
- P.54 {Charger} Change PF1 to 24V-7A_1206 from power request.
- P.52 {HOLE} Delete BOSS3,BOSS13, add BOSS15 from ME request.
- P.69 {FP} Delete F_BOSS1 from ME request.
- P.64 {Audio} Change A_R5710,A_R5711,A_R5712,A_R5713 to 105K
from FAE suggestion.
- P.22 {VGA} Add R5728,R5729 from FAE sguusetion.
Because use external thermal sensor.

(2009/02/26)

- P.45 {Cardreader} Change CN11 to UV31413-RU82P-7H from ME request.
- P.49 {BT} Change CN32 to QT510106-312H-7H from ME request.
- P.29 {CRT} Change CN2 to DZ11A91-MB229-9F from ME request.
- P.48 {USB} Change CN9,CN12 to UB111M3-CAGS4-7H from ME request.
- P.42 {HDD} Change CN13 to LD2722F-SRYL6 from ME request.
- P.41 {LAN} Chnage L5 to LG-2413S-1 from PUR suggestion.
- P.47 {CAM} Change CN17 to HS6204E. Because move MIC to Audio board from MI request.
- P.62 {Audio} Change A_CN3 to HS6202E from ME request.
- P.47 {CAM} Delete L65,L63,C779,C780 from EMI request.
- P.62 {Audio} Add A_L27,A_L28,A_C159,A_C160 from EMI request.
- P.17 {VGA} Change R5251 to 15K from FAE request.

(2009/02/27)

- P.20 {VGA} Change L154 to 33ohm from DG v04.
- P.47 (CAM) Remove R7,R4. Add R8 from MOR suggestion.
- P.11 {Cantiga} Change C21 value to NC from MOR request.
- P.15 (DDR3) Add C59 from MOR request.
- P.16,23 {VGA} Change L73,L81,L83 to TL160808-R10K.
- P.18 {VGA} Add C6042 from MOR request.
- P.27 {VRAM} Remove C14,C15 from MOR request.
- P.28 {VRAM} Remove C16,C17 from MOR request.
- P.39 {WLAN} Reserve R5370 from MOR request.
- P.29 {CRT} Change R83,R72,R64 to 75ohm from MOR suggestion.
- P.20 {VGA} Remove R5262,R5263,R5264 from MOR suggestion.

(2009/03/02)

- P.39 {WLAN} Change BOSS1,BOSS2 footpint.
- P.14 {DDR} Change C92 to 22P for RE suggestion.
- P.14,15 {DDR} Remove C214,C200, because had same solution.
- P.52 {HOLE} Modify F_PAD5,F_PAD6 PAD size from EMI request.
- P.42 {HDD} Remove R5712, add open jump.
- P.42 {ODD} Remove R5713, add open jump.
- P.54 {Charger} Change PCN2 to GS73041-10272-7F from ME request.
- P.21 {VGA} Change C5132,C5236 size to 0402 from DG v04.
- P.54 {Charger} Change PCN1 to BP91071-B71E3-7H from ME request.

(2009/03/03)

- P.62 {Audio} Change A_CN3 to HS8202E from ME request.
- P.52 {HOLE} Add P_R4,P_C8(reserve) for EMI request.
- P.50 {LED} Change LED2,6 to L-C170KRCT-FX for SPEC.
- P.50 {LED} Change LED9 to HT-191UD for SPEC.
- P.70 {Function} Change P_LED1,P_LED2,P_LED3,P_LED11 to L-C170KGCT-FX for SPEC.
- P.39 {WLAN} Change LED3 to L-C170KGCT-FX for SPEC.
- P.50 {TP} Chnage CN34 to GB5RF060-1203-7F for ME request.
- P.39 {WLAN} Change SW4 to SSSS811101_SW-SMD7 from ME request.

(2009/03/04)

- P.50 {TP} Add R5733~R5740 for co-lay 2 TP vendor.
- P.14 {DDR} Change CN29 to AS0A626-U2SN-7F from ME request.
- P.48 {USB} Add L156 for EMI suggestion.
- P.61 {VGA} Change PR87 to 7.15K for power request.
- P.52 {HOLE} Add BOSS16 for ME request.

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(2009/03/09)

P.48,43 {USB} Change F1,F11,F12 to 6V_2.6A_1812.
 P.62 {Audio} Change A_R118,A_R119,A_R120,A_R121,A_C116,A_C117,A_C119,A_C120,A_C127,A_C133,A_C131,A_C136 to 0402 size.
 P.62,67 {Audio} Change A_C137,A_R119,A_R125,A_R5,A_R18 to 0402 size.
 P.63 {HP} Change A_R127,A_R134,A_R128,A_R129,A_R130,A_R131,A_R132,A_R133,A_R135,A_R136,A_R137,A_R138 to 0402 size.
 P.37 {EC} Change R476,R487,R484,R76,R210,R437,R479,R447,R432,R173,R197,R203,R124,R75,R442,R440,R477,R436,R431,R435,R613,R475,R629,R444 to 0402 size.
 P.34 {ICH9} Change R302,R295,R563,R575,R574,R578,R320,R319,R271,R272,R337,R331,R334,R576,R309,R294,R300,R306,R298,R303,R316,R338,R577,R573,R332,R555,R562,R297,R322,R296,R567,R54,R540,R541,R299,R321,R305,R315 to 0402 size.
 P.06 {CLK} Change R288,R283,R542,R537,R536,R545,R277,R553,R534,R276,R552,C357,C377,C369,C370,C383,C386 to 0402 size.
 P.64 {SPK} Change A_C145,A_C140,A_C141,A_C142 to 0402 size.
 P.54 {Charger} SWAP PD2 Pin1.2 for layout.
 P.12 {Cantiga} Change R208,C234,C346,C320,C287,C316,C326,C328,C313,C298 to 0402 size.
 P.06 {CLK} Change R544,R619,R620,R621,R543,R550,R546,R551,R549,C384,C382,C355,C375,C385,C352,C376,C387,C356 to 0402 size.
 P.32 {ICH9} Change R53,R307,C449,C450,C727,C728,C706,C702,C729,C730 to 0402 size.
 P.69 {FP} Change F_R9,F_R10,F_R20,F_R1,F_R25,F_R3,F_R26,F_R4,F_C12,F_C20,F_C24,F_C16 to 0402 size.
 P.65 {Audio} Change A_R166,A_R171,A_R169,A_R175,A_R176 to 0402 size.
 P.67 {HP} Change A_R7,A_R20,A_R170 to 0402 size.
 P.08 {Cantiga} Change R268,R195,R286,R181,R130,R193 to 0402 size.
 P.33 {ICH9} Change R101,R610,R318,R564 to 0402 size.
 P.67 {MIC} Change A_R17,A_R3 to 0402 size.
 P.65 {MUTE} Change A_R174,A_R168,A_R167,A_R173 to 0402 size.
 P.38 {FLASH} Change R233 to 0402 size.

(2009/03/10)

P.55 {3V/5V} Change PU11 to SN0608098RHBR for power request.
 P.55 {3V/5V} Change PC216 to 1U for power request.
 P.54 {Charger} Add 2 test point for BFT.
 P.43 {Audio} Move D-MIC and SPK circuit to MB for ME request.
 P.43,66 {Audio} Change CN37 to 40 pin for ME request.
 P.49 {BT} Delete R909 from MOR suggestion.Because Vespa is used only UGPZ9.

(2009/03/11)

P.46 {SD} Change U18 to BD2055AFJ-E2 for VEDS spec.
 P.50 {TP} Change R529 value to stuff.
 P.43,66 {Audio} Modify Audio connector pin define for layout.

(2009/03/12)

P.52 {HOLE} Add A_C159 for EMI request.
 P.31 {HDMI} Delete U128, add U130 for low cost solution.

(2009/03/13)

P.29 {CRT} Change Q5,D1,R627,R284 value to no stuff from MOR request.
 P.29 {CRT} Add R292 from MOR request.
 P.37 {EC} Change C616 value to no stuff from power request.

(2009/03/16)

P.43,66 {Audio} Change Audio BTB connector pin define for EMI suggestion.
 P.52 {HOLE} Change H45 for ME request.
 P.42 {HDD} Change CN13 to LD2722F-SRVL6 from ME request.

(2009/03/17)

P.64 {SPK} Change cable short circuit from A_GND to U_GND.
 P.50 {TP} Delete R5733-R5740 for remove co-lay 2 TP vendor.
 P.64 {SPK} Change A_R5710,A_R5711,A_R5712,A_R5713 to 75K from FAE suggestion.

(2009/03/18)

P.50,70 {LED} Move Power & suspend LED to MB for ID modify.
 P.54 {Charger} Change PCN1 to BP91071-B31E3-7H from ME request.
 P.52 {HOLE} Add A_H49,A_H50 for ME request.
 P.70 {LED} Change P_LED1,P_LED2,P_LED3 to L-S110KGCT-FX from ME request.
 P.50 {TP} Change SW2,SW3 SKHMQKE010_SW-SMD5 from ME suggestion.
 P.52 {HOLE} Delete P_PAD1,P_PAD2,P_PAD3,P_PAD4 for EMI request.

(2009/03/19)

P.52 {HOLE} Change BOSS14,BOSS15 from ME request.
 P.49 {BT} Change U45 to AT5208-3.3KER.
 P.50 {TP} Change R530 to stuff,R529 to no stuff from MOR request.
 P.64 {SPK} Change A_Q10,A_Q11 to 2N7002PT and add A_Q27,A_Q28,A_R172,A_R177.
 P.65 {MUTE} Delete A_Q18,A_R166 for MUTE_AMP high active of AMP.

(2009/03/20)

P.52 {HOLE} Delete A_C159 from EMI suggestion.
 P.52 {HOLE} Change BOSS15 to BOSS_3.72x4 from ME request.
 P.31 {HDMI} Change CN31 to QJ1119L-NT10-4H from ME request.
 P.04 {CPU} Reserve C6047 for H_DPRSTP#.

(2009/03/23)

P.22 {VGA} Delete R5728,R5729 because double pull-high.
 P.38 {EC} Move R269 to SPI_ROM_CS# signal of EC side.
 P.16 {VGA} Change C571,C569 value to no stuff. because control IC have 22uF.
 P.14 {DDR3} Change CAP13 to no stuff.
 P.54 {Charger} SWAP PD2 pin1,2 for layout request.
 P.30 {LVDS} Add CN18.32 to GND.
 P.17 {GPU} Change R5689 to 24.9K from DG v04.
 P.52 {HOLE} Reserve A_C159 to A_GND from EMI suggestion.
 P.69 {FP} Change F_R9,F_R10 to 0201 size for layout space issue.

(2009/03/24)

P.52 {HOLE} Delete SPR1 for EMI request.

(2009/03/25)

P.19 {VGA} Change R5256,R5257 to 56.2 and 27 ohm from N10M PUN modify.

(2009/03/27)

P.50 {TP} Change R529 to stuff,R530 to no stuff for new TP power.
 P.08 {Cantiga} Change C820 to Y5V.
 P.57 {1.5V_0.75V} Change PC250 to no stuff.
 P.59 {Others} Change PC262,PC264,PC265,PC270,PR262,PR263,PR264,PQ50,PQ55,PR265,PR266,PQ51 to no stuff.
 P.29 {CRT} C577,C592,C583,C584 to no stuff.
 P.30 {LVDS} Delete L43,Add R5731 and change R394 to no stuff.
 P.41 {LAN} Delete L152,Add R5733.C5164 change to 10U.
 P.42 {SATA} Change C285,C757 to no stuff.
 P.48 {USB} Delete L156, Add R5372, Change CAP16,CAP18 to 47UF.
 P.50 {LED} Change C6045,C6046,C295,C301 value to no stuff.

(2009/04/03)

P.34 {ICH9} Change R5714 value to no stuff.
 P.17 {VGA} Change R5250 to 34.8K from PUN update.
 P.39 {WLAN} Change C531,C546,C573 value to no stuff.
 P.16 {VGA} Change C1290,C1300,C1312 to no stuff.
 P.18 {VGA} Change C874 value to no stuff.
 P.20 {VGA} Change C1395,C1397,C5196,C5197 value to no stuff.
 P.11 {Canita} Change CAP6 to NC.

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DVT**(2009/04/10)**

- P.21 {VGA} HDMI I2C data and CLK signal swap.
- P.19 {VGA} Change R5256 to 56.2_F,R5257 to 40.2_F for PUN V07.
- P.37 {EC} Add R478 pull-down resistor for BL_OFF#.
- P.50 {TP} Modify SW2,SW3 pin define.

(2009/04/18)

- P.39 {WLAN} SW4.C pin delete and SW4.A connect to GND for ME ID design.
- P.61 {VGA POWER} Change PR99 to 13.7K, PR110 to 33K,PC85 value to stuff for N10M GPU power.
- P.61 {VGA POWER} Change PR99 to 13.7K, Change PR110 to NC_* for N10P GPU power.
- P.44 {Thermal} Delete R426,R430 for vendor suggestion.
- P.30 {LVDS} Delete U25,U29,U2,U23 and Add U131 (4 channel) for can reducing parts.

(2009/04/21)

- P.58 {CPU_CODE} Change PR67 to 3.3K from Power request.

(2009/04/22)

- P.43,54 {Charger} Modify charger board BTB connector from ME request.
- P.55 {3V/5V} Change PC216 to 1U_6.3V from power request.

(2009/04/28)

- P.50 {LED} Change LED2,LED6 to HT-110UY for ME request.
- P.50 {LED} Change LED9 to HT-110UD for ME request.
- P.43 {SPK} Change JSPK1 to HS6104E for ME request.
- P.47 {CAM} Change CN17 to HS6106E for ME request.
- P.52 {HOLE} Add BOSS17 for ME request.

(2009/04/30)

- P.54 {Charger} Change charger board location to C_*.
- P.29 {CRT} Change D11 to SSM22LLPT for leakage issue.
- P.30 {LVDS} Change R5241 to no stuff, because had double PL.

(2009/05/04)

- P.43 {Audio} Change F12 from 2.6A to 0.75A, because +5VRUN power budget only 0.55A.
- P.50 {LED} Change power/suspend LED circuit, same M850.
- P.37 {KB} Add 10 test point for BFT.

(2009/05/05)

- P.39 {WLAN} Chnage LED3 to HT-110UYG for ME request.
- P.70 {Function} Change P_LED1~PLED3 to HT-110UYG for ME request.
- P.30 {LVDS} Add J3 for BFT test.

(2009/05/07)

- P.39 {WLAN} Add TP499,TP509 for Power test.
- P.50 {LED} Add TP494,TP496,TP495,TP493,TP488,TP490,TP491,TP489,TP498,TP497 for power test.
- P.57 {DDR Power} Change PU17 pin6 change from +3VSUS to +3VALW for Power request.
- P.58 {CPU Power} Add TP176 for Power test.
- P.54 {Charger} C_PUI change to BQ24753ARHDR and schematic_part select bq24753ARHDR_T821_PWR for power request.
- P.60 {OVP} PU2 change to G1336BTB1U for power request.
- P.60 {OVP} Del PR40,PR41 and pin6 link to +5VALW_LDO directly.
- P.30,43,66 {LVDS,BTB,Audio} Change CN18,CN37,A_CN5 to GS12407-11151-9F from ME request.

(2009/05/11)

- P.58 {CPU} Add 0.lux5pcs (EC283~EC287) and PC143,PC149 stuff for EMI suggestion.
- P.25 {VRAM} Add EC6048 for EMI suggestion.
- P.59 {Others} Add EC288,EC289,EC290 for EMI suggestion.
- P.64 {Audio} Delete A_R141, Add A_EC160 for EMI suggestion.
- P.14 {DDR} Change CN29 to AS0A626-N2SN-7H from ME request.
- P.15 {DDR} Change CN30 to AS0A626-JASG-7H from ME request.
- P.40 {Express} Delete R330,R333, Add L37 for express card SI test fail issue.

(2009/05/13)

- P.46 {SD} Change R5694,R5695,R5697,R5698 to 33ohm for SI test solution.
- P.45 {MS} Change R5704,R5705,R5707,R5701 to 33ohm R5703 to 68ohm for SI test solution.
- P.43 {Audio} Chnage A_C110 to C6048 for layout suggestion.
- P.43 {Audio} Chnage A_F16,A_F17 to F15,F16 for layout suggestion.
- P.33 {ICH9} Change CN10 to HS8102E from ME request.
- P.45 {MS} Change CN35 to JES014-2000-1 from ME request.
- P.30,43,66 {LVDS,BTB,Audio} Change CN18,CN37,A_CN5 to GS12401_1011 for ME request.
- P.52 {HOLE} Change function board and Audio board serew.
- P.69 {FP} Change F_CN1 pin define from ME request.
- P.70 {Function} Change P_CN1 pin define from ME request.

(2009/05/18)

- P.56 {+1.05V} Add 3pcs 680p CAP of EMI suggestion.
- P.54 {Charger} Add C_PR136 of EMI request.
- P.47 {DMI} Delete L157,L158, add R5734,R5735 for EMI request.
- P.43,54 {Charger} Modify charger board CONN pin define for EMI suggestion.

(2009/05/19)

- P.62 {Audio} Change A_C23,A_C22 to 15p, And delete A_R117,A_R116 Add A_L158,A_159 for EMI request.

(2009/05/20)

- P.56 {1.8/1.05V} Change power solution to TPS51218DSCR for power request.
- P.57 {1.05/0.75V} Change power solution to TPS51218DSCR for power request.

(2009/05/21)

- P.41 {LAN} Change R5733 to Bead (L152),Add E_C6054,E_C6055,E_C6056 for EMI request.
- P.46 {SD} Add E_C6049,E_C6050 for EMI request.
- P.40 {Express} Add E_C6051,E_C6052 for EMI request.
- P.50 {LED} Add E_C6053 for EMI request.

(2009/05/22)

- P.56 {1.8V_1.05V} Change PR235 to 9.76K, PC176 to 330U for power request.
- P.52 {HOLE} Add SPR1,SPR2 for EMI request.
- P.41 {LAN} Add E_C6054~E_C6057 for EMI request.
- P.70 {Function LED} Change P_LED1,P_LED2,P_LED3 for factory request.
- P.39 {WLAN LED} Change LED3 for factory request.
- P.50 {LED} Change LED2,LED6 for factory request.

(2009/05/23)

- P.55 {SYSPPOWER} Add E_C6059,E_C6060,E_C6061,E_C6062 for EMI request.
- P.41 {LAN} Add E_C6058 for EMI request.
- P.44 {LAN} Add E_C6064 for EMI request.
- P.61 {VGA Power} Add E_C6063,E_C6065 for EMI request.
- P.54 {Charger} Reserve E_C6066 for EMI request.
- P.55 {SYSPPOWER} Reserve E_C6067,E_C6068,E_C6069,E_C6070 for EMI request.

(2009/05/25)

- P.11 {Cantiga} Delete C21 from MOR request.
- P.45 {MS} Change R376,R373,R5373,R5374 to 54.9 ohm for i.LINK test issue.
- P.20 {VGA} Change R1228,R1231 to NC_* from MOR suggestion.
- P.47 {CAM} Change CN17 to HS6206E for ME request.
- P.64 {SPK} Delete A_C147,A_C152,Change A_C149,A_C148,A_C150,A_C151 to 0.22u for POP noise issue.
- P.64 {SPK} Change A_R5710~A_R5713 resistor to 82K for SPK low voice issue.
- P.43 {FP} Change U3 to Max4785 for FP current limit issue.
- P.46 {SD} Change CN16 to WK21923-S6P1-7F from ME request.
- P.30 {LVDS} Add Swith circuit

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(2009/06/03)

P.30 {LVDS} Change SW1 to DHNF-06F-T-V-T-R_SW-SMD12 because original part well EOL.
P.17 {VGA} Add R5252 for nVIDIA suggestion.

PVT

(2009/07/01)

P.30 {LVDS} Modify rush current circuit.
P.29 {CRT} Change CN2 to DZ11A91-MB229-9H for ME request.
P.44 {FAN} Change CN20 to HS8103E-LH for ME request.
P.37 {EC} Change CN3 to 196009-24021-3 for ME request.
P.41 {LAN} Change CN22 to HS6108E-LH fot ME request.
P.50/43/69 {TP} Change CN34/CN36/F_CN1 to GB5RF060-1203-7H for ME request.
P.39 {WLAN} Change CN21 to AS0B226-S52N-7H for ME request.
P.43 {BTB} Change JSPK1 to HS6104E-LH for ME request.
P.67 {HP} Change A_CN1 to JA93331-B18106-7H for ME request.
P.52 {HOLE} Change BOSS16 and Add BOSS18 for ME request.
P.45 {Cardreader} Change CN11 to UV31413-WU82P-7H for ME request.
P.38 {Flash} Change CN23 to QT510306-L011-7H for ME request.

(2009/07/03)

P.65 {MUTE} Change A_Q24 to stuff from MOR request.
P.42 {HDD/ODD} Remove PJ12,PJ13,F13,F14 for PVT not need.
P.64 {AMP} Modify cable circuit to no stuff.

(2009/07/06)

P.49 {BT} Add TP568~TP574 test point of BT.
P.49 {BT} Remove L72. DVT no mount becasue have 2 0ohm res.
P.40 {Express} Delete R333,R330,L38,L40. becasue have colay parts.
P.48 {USB} Delete L66,L61 becasue have colay res.

(2009/07/07)

P.67 {Audio} Change A_CN2 to JA93331-R18106-7H from ME request.
P.33 {ICH9} Change CN10 to HS8202E-LH from ME request.
P.70 {Function} Move P_R1,P_R2,P_R3 TO PAGE. 50 from MOR side suggestion.
P.55,56,57,61 {Power JP} Modify power Jump for power request.
P.30 {LVDS} L43 no stuff and Q177,C575,R5736,R5737 stuff for LVDS dcbatout inruch current issue.

(2009/07/10)

P.57 {DDR3} Add PJ6 for Power request.
P.45 {MS} Change R5700,R5706,R5699,R5702 to 33ohm for overshoot issue.
P.68 {USB} Change A_CN7 to UB11123-R1201-7H for ME request.
P.39 {WLAN} Add TP575 for WLAN test point.

(2009/07/15)

P.05 {CPU VID} Delete R29,R30,R31,R32,R39,R40,R41 for power suggestion.
P.54 {Charger} Change C_EC6066,C_PC156 to 1u for EMI request.
P.48 {USB} Add USB test point of BFT.
P.58 {CPU} Reserve EC294,EC295,EC296 on DCBATOUT for EMI request.

(2009/07/16)

P.52 {HOLE} Change SPR1,SPR2 for EMI request.
P.46 {SD} Change CN16 to WK2192C-S6P2-4H for ME request.
P.54 {Charger} Change C_PC1 to BP91071-B31E3-7H for ME request.
P.46 {SD} Change CN16 to WK2192C-S6P2-4H from ME request.

(2009/07/17)

P.23 {VGA} Add R5741,R5742 0 ohm for MOR suggestion.
P.52 {HOLE} Change P_H51,P_H53 for ME request.

(2009/07/18)

P.52 {HOLE} Add function board hole for ME request.
P.50 {LED} Change R599,R600 to 499,300 ohm for brightness issue.

(2009/07/24)

P.60 {OVP} Change PR55 to 18.2K,PR143 to 26.1K,PR144 to 80.6K and mount PR73 from MOR request.

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