

Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Index page	1.0	07'10/19	36	Flash ROM/XBUS	1.0	07'10/19
02	Block Diagram	1.0	07'10/19	37	Mini-PCIE Card	1.0	07'10/19
03	Merom(HOST BUS) 1/3	1.0	07'10/19	38	FeliCa/MDC	1.0	07'10/19
04	Merom(HOST BUS) 2/3	1.0	07'10/19	39	EXPRESS	1.0	07'10/19
05	Merom(Power/Gnd) 3/3	1.0	07'10/19	40	AUDIO(CODEC/POWER) 1/4	1.0	07'10/19
06	CLOCK GEN	1.0	07'10/19	41	AUDIO(AMP/HP/SPK) 2/4	1.0	07'10/19
07	Crestline (HOST) 1/7	1.0	07'10/19	42	AUDIO(EXTMIC) 3/4	1.0	07'10/19
08	Crestline (DMI) 2/7	1.0	07'10/19	43	AUDIO(MUTE) 4/4	1.0	07'10/19
09	Crestline (GRAPHIC) 3/7	1.0	07'10/19	44	FAN/Thermal-Sensor	1.0	07'10/19
10	Crestline (DDRII) 4/7	1.0	07'10/19	45	PCI (PCI BUS) 1/3	1.0	07'10/19
11	Crestline (POWER,VCC) 5/7	1.0	07'10/19	46	PCI (i.LINK) 2/3	1.0	07'10/19
12	Crestline (VCC CORE) 6/7	1.0	07'10/19	47	PCI (SD/MS-DUO) 3/3	1.0	07'10/19
13	Crestline (VSS) 7/7	1.0	07'10/19	48	USB2.0	1.0	07'10/19
14	DDRII(SO-DIMM_0) 1/3	1.0	07'10/19	49	LAN (88E8039)	1.0	07'10/19
15	DDRII(SO-DIMM_1) 2/3	1.0	07'10/19	50	LAN Transformer	1.0	07'10/19
16	DDRII(Termination) 3/3	1.0	07'10/19	51	Touch/Lid/LED	1.0	07'10/19
17	VGA(PCI-E)	1.0	07'10/19	52	Power Bottom & USB Board	1.0	07'10/19
18	VGA(STRAP)	1.0	07'10/19	53	Power Design Diagram	1.0	07'10/19
19	VGA(GDDR)	1.0	07'10/19	54	DCIN&Charger	1.0	07'10/19
20	VGA(MULTIUSE)	1.0	07'10/19	55	SYS Power (+3_3V/+5V)	1.0	07'10/19
21	VGA(LVDS/VDAC)	1.0	07'10/19	56	SYS Power(+1_5V/+1_05V)	1.0	07'10/19
22	VRAM(GDDR)	1.0	07'10/19	57	DDR2 Power(+1_8V/+0_9V)	1.0	07'10/19
23	VGA(POWER) 1/3	1.0	07'10/19	58	CPU Power_VHCORE	1.0	07'10/19
24	VGA(POWER) 2/3	1.0	07'10/19	59	VGA Power(+1_2V/+1_2V)	1.0	07'10/19
25	VGA(POWER) 3/3	1.0	07'10/19	60	Others power plane	1.0	07'10/19
26	VRAM(BYPASS)	1.0	07'10/19	61	OVP protection	1.0	07'10/19
27	CRT	1.0	07'10/19	62	HOLE	1.0	07'10/19
28	LVDS	1.0	07'10/19	63	History (1)	1.0	07'10/19
29	ICH8-M(PCI/USB) 1/5	1.0	07'10/19	64	History (2)	1.0	07'10/19
30	ICH8-M(LPC, IDE, SATA) 2/5	1.0	07'10/19	65	History (3)	1.0	07'10/19
31	ICH8-M(GPIO) 3/5	1.0	07'10/19	66	History (4)	1.0	07'10/19
32	ICH8-M(POWER) 4/5	1.0	07'10/19	67	History (5)	1.0	07'10/19
33	ICH8-M(GND) 5/5	1.0	07'10/19	68			
34	SATA HDD/CD-ROM	1.0	07'10/19	69			
35	EC+KBC(3910)	1.0	07'10/19	70			

M730 Main Board

M/B P/N: 1P-0079100-8010 (FUBAI)
 1P-0079500-8010 (HANSTAR)
 1P-0079G00-8010 (TRIPOD)

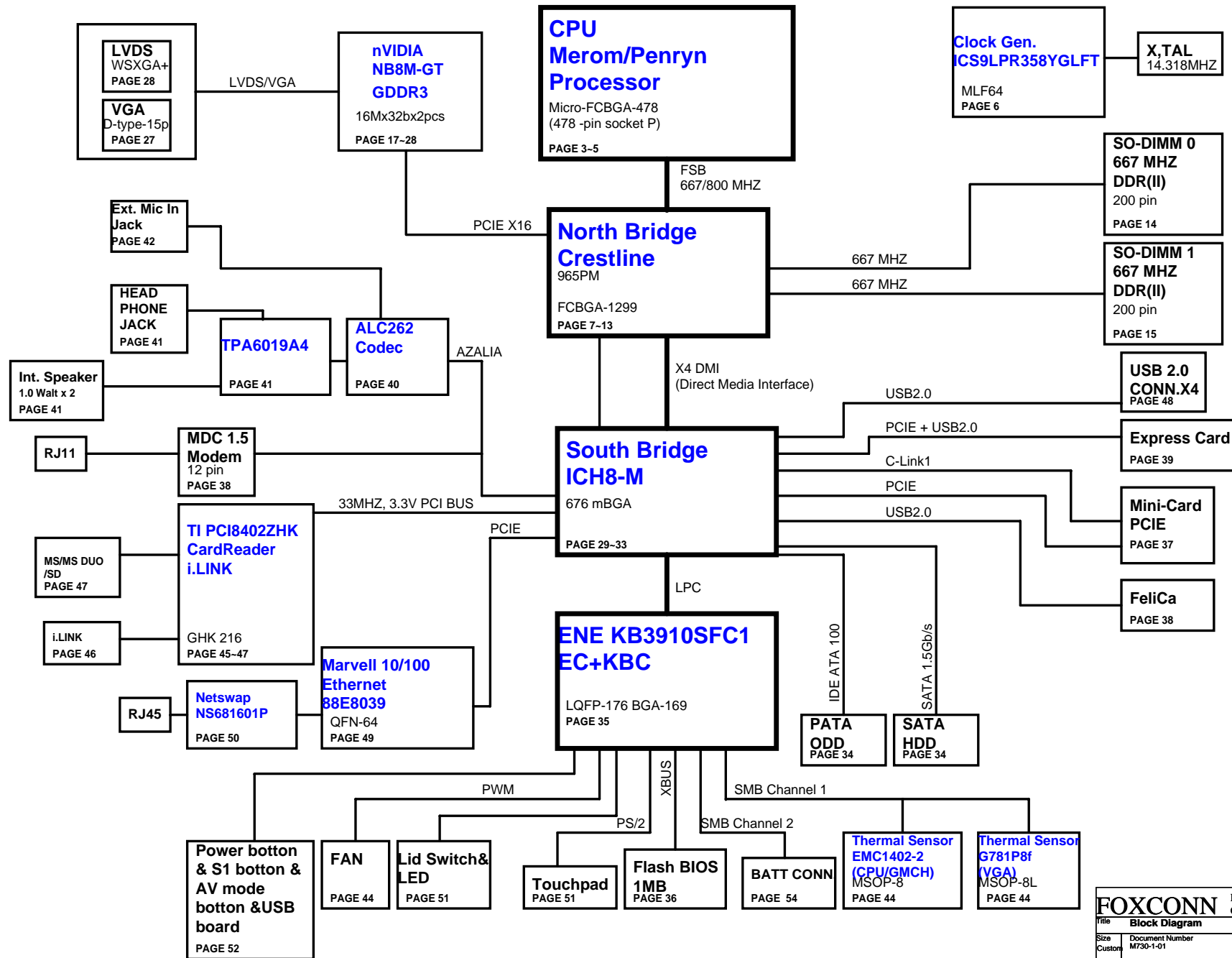
P/B P/N: 1P-1079100-8010 (FUBAI)
 1P-1079500-8010 (HANSTAR)
 1P-1079G00-8010 (TRIPOD)

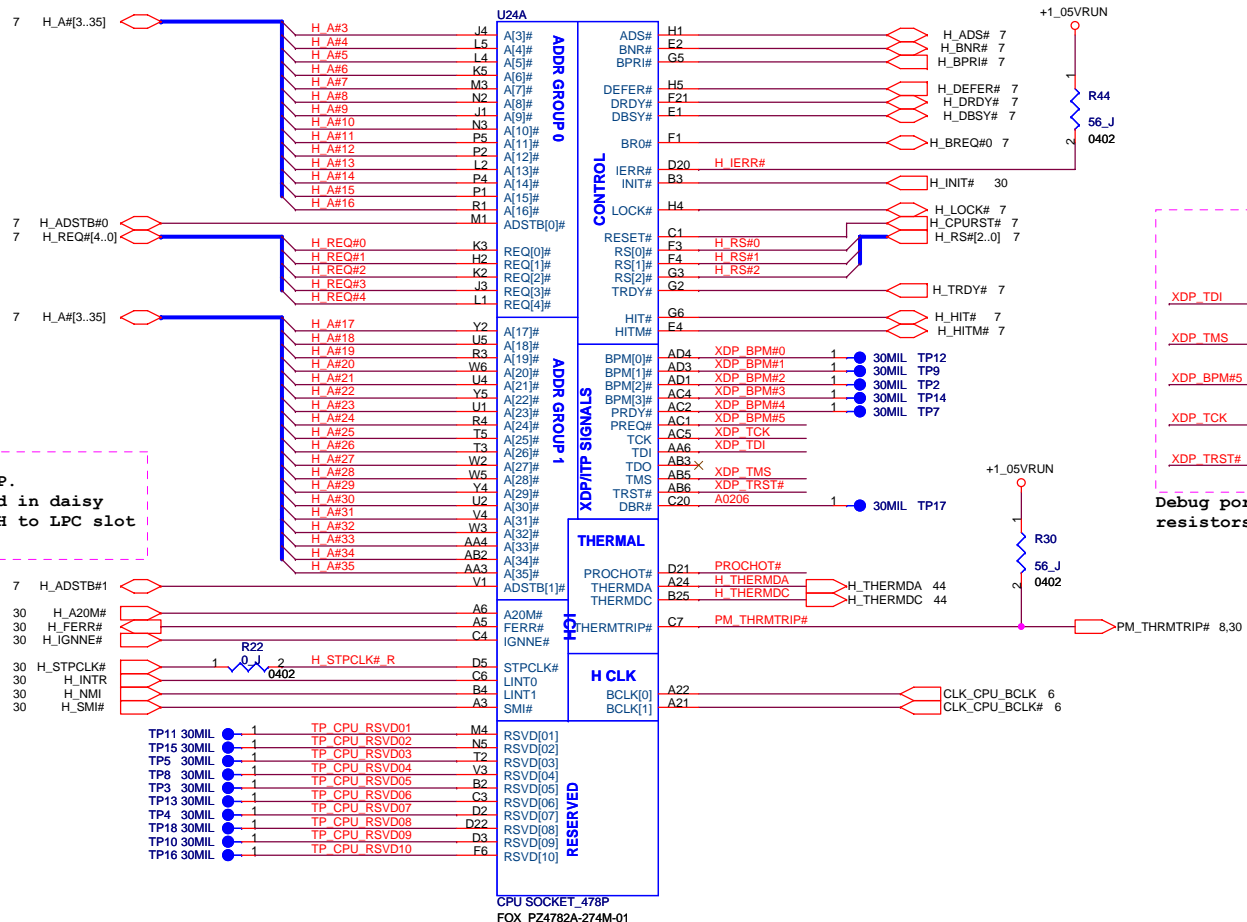
U/B P/N: 1P-1079101-8010 (FUBAI)
 1P-1079501-8010 (HANSTAR)
 1P-1079G01-8010 (TRIPOD)

P. Leader	Check by	Design by

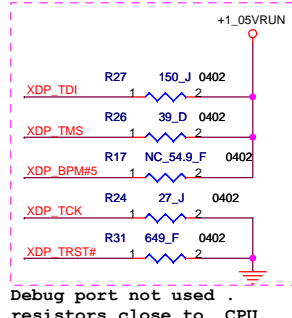
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Index Page		
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 1	of 67

M730 (Crestline PM+Gfx Block Diagram)





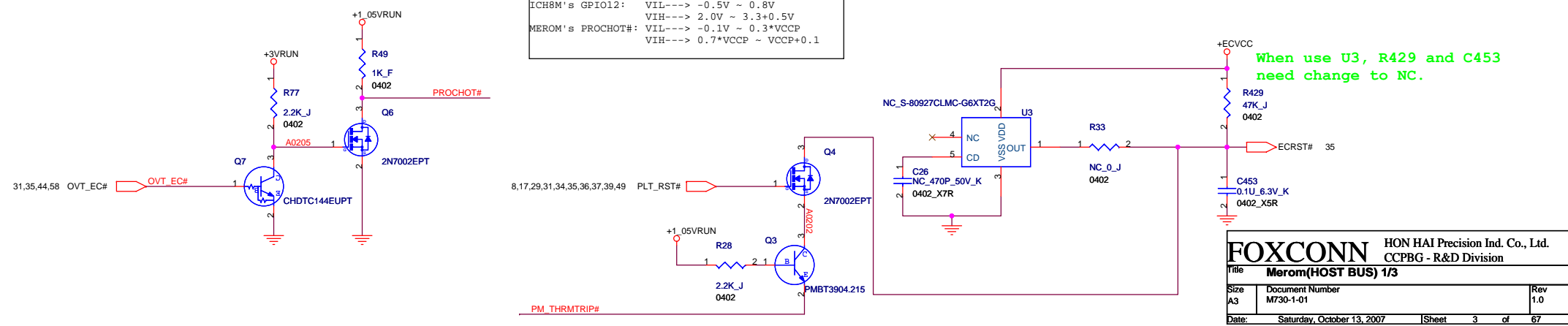
Layout note:
no stub on H_STPCLK TP.
H_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.



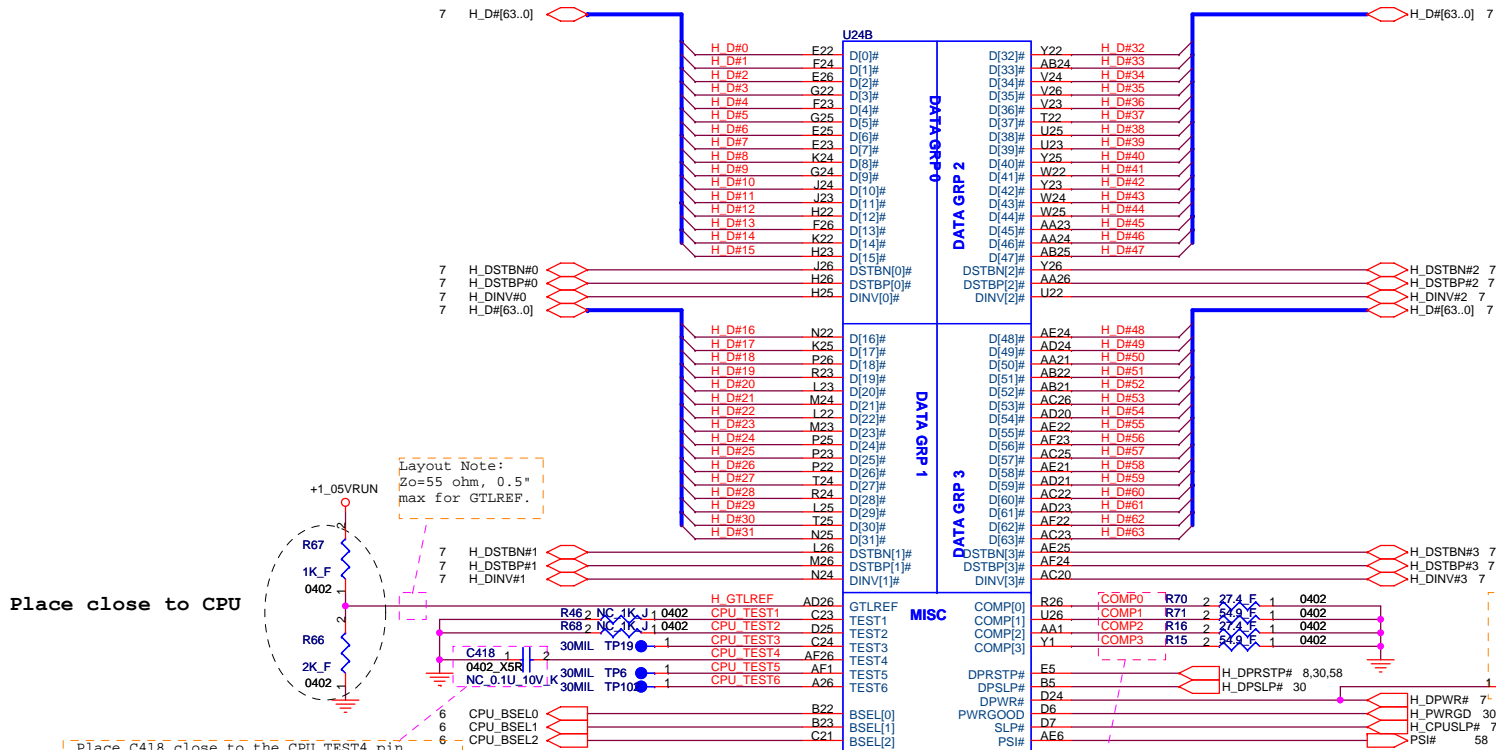
Debug port not used. resistors close to CPU.

PM_THRMTRIP# should connect to ICH8-M and GMCH without T-ing (No stub)

ICH8M's GPIO12: VIL---> -0.5V ~ 0.8V
VIH---> 2.0V ~ 3.3+0.5V
MEROM's PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
VIH---> 0.7*VCCP ~ VCCP+0.1



When use U3, R429 and C453 need change to NC.



Layout Note:
 $Z_0=55$ ohm, 0.5"
 max for GTLREF.

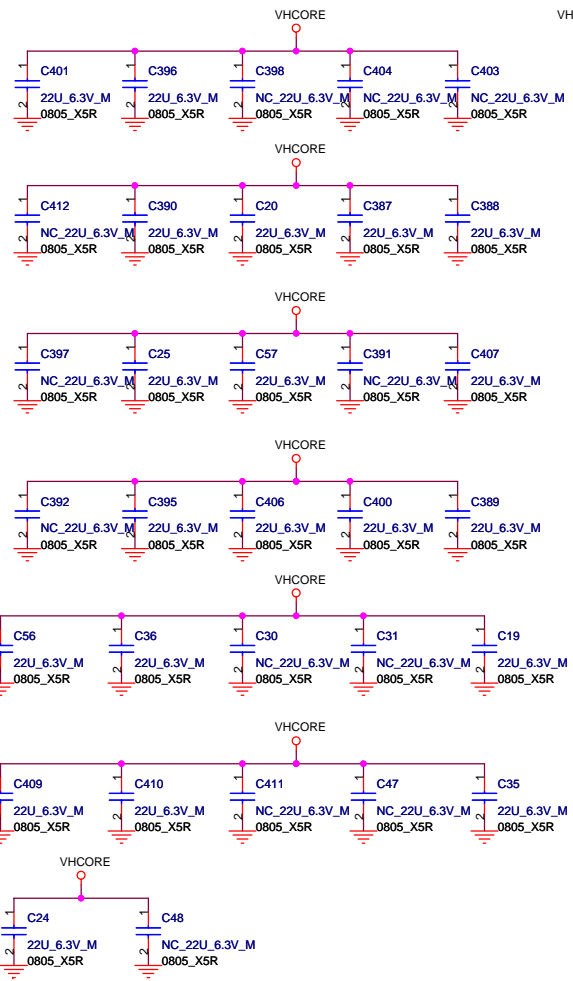
Place close to CPU

Place C418 close to the CPU_TEST4 pin.
 Make sure CPU_TEST4 routing is reference
 to GND and away from other noisy signals.

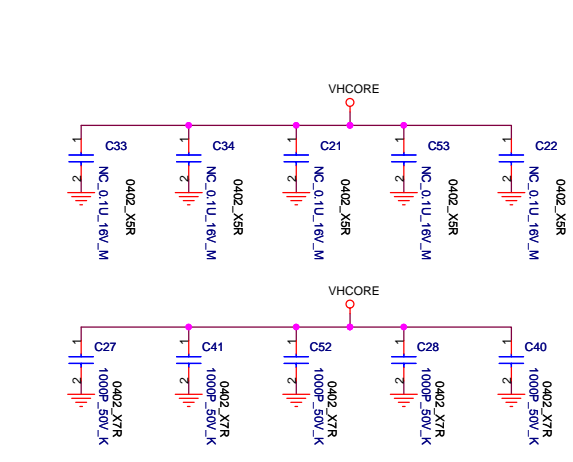
Layout:
 Connect test
 point with no
 stub

Layout Note:
 Comp0,2 connect with $Z_0=27.4$ ohm, make
 trace length shorter then 0.5".
 Comp1,3 connect with $Z_0=55$ ohm, make
 trace length shorter then 0.5".

IMVP6 (ISL6262ACRZ-T)
 cpu PSI# <-> ISL6262ACRZ-T PSI#
 ISL6262ACRZ-T: VIHmin=0.315V
 VILmax=0.735V
 (ref. IMVP-6 NO:18904)

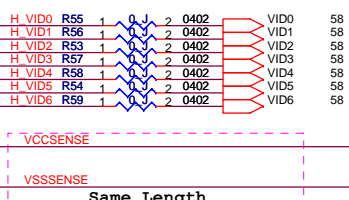
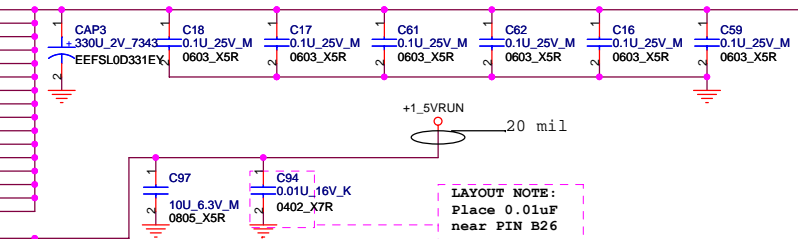


CPU_VCCA----->120mA
 CPU_VCCP----->2.5A
 CPU_VCC----->36A



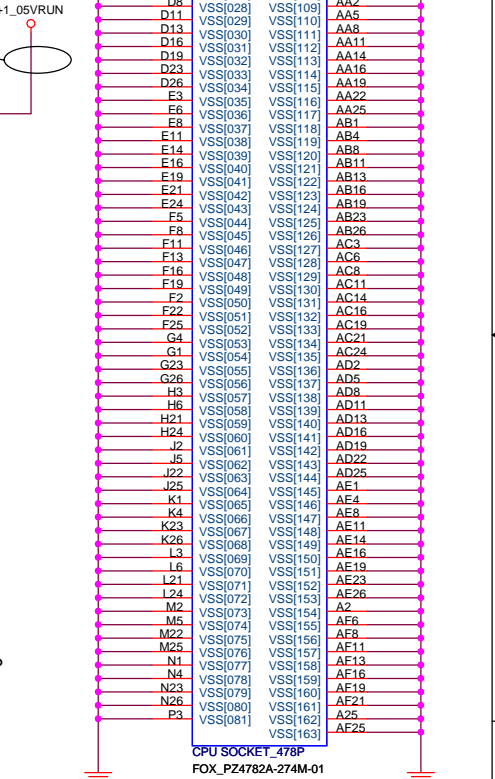
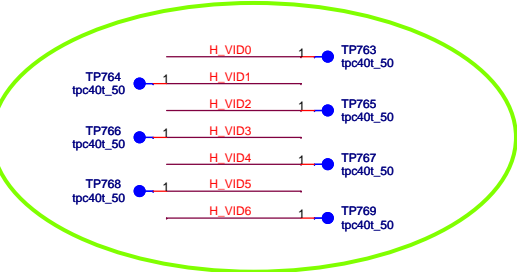
A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD10
B10	VCC[012]	VCC[079]	AD12
B12	VCC[013]	VCC[080]	AD14
B14	VCC[014]	VCC[081]	AD15
B15	VCC[015]	VCC[082]	AD17
B17	VCC[016]	VCC[083]	AD18
B18	VCC[017]	VCC[084]	AE9
B20	VCC[018]	VCC[085]	AE10
C9	VCC[019]	VCC[086]	AE12
C10	VCC[020]	VCC[087]	AE13
C12	VCC[021]	VCC[088]	AE15
C13	VCC[022]	VCC[089]	AE17
C15	VCC[023]	VCC[090]	AE18
C17	VCC[024]	VCC[091]	AE20
C18	VCC[025]	VCC[092]	AE9
D9	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	G21
E12	VCC[036]	VCCP[02]	J6
E13	VCC[037]	VCCP[03]	K6
E15	VCC[038]	VCCP[04]	IM6
E17	VCC[039]	VCCP[05]	J21
E18	VCC[040]	VCCP[06]	K21
E20	VCC[041]	VCCP[07]	M21
F7	VCC[042]	VCCP[08]	N21
F9	VCC[043]	VCCP[09]	R21
F10	VCC[044]	VCCP[10]	R6
F12	VCC[045]	VCCP[11]	T21
F14	VCC[046]	VCCP[12]	T6
F15	VCC[047]	VCCP[13]	VZ1
F17	VCC[048]	VCCP[14]	WZ1
F18	VCC[049]	VCCP[15]	
F20	VCC[050]	VCCP[16]	
AA7	VCC[051]	VCCA[01]	B26
AA9	VCC[052]	VCCA[02]	C26
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]		
AA15	VCC[056]		
AA17	VCC[057]		
AA18	VCC[058]		
AA20	VCC[059]		
AB9	VCC[060]		
AC10	VCC[061]		
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]		
AB17	VCC[066]		
AB18	VCC[067]		

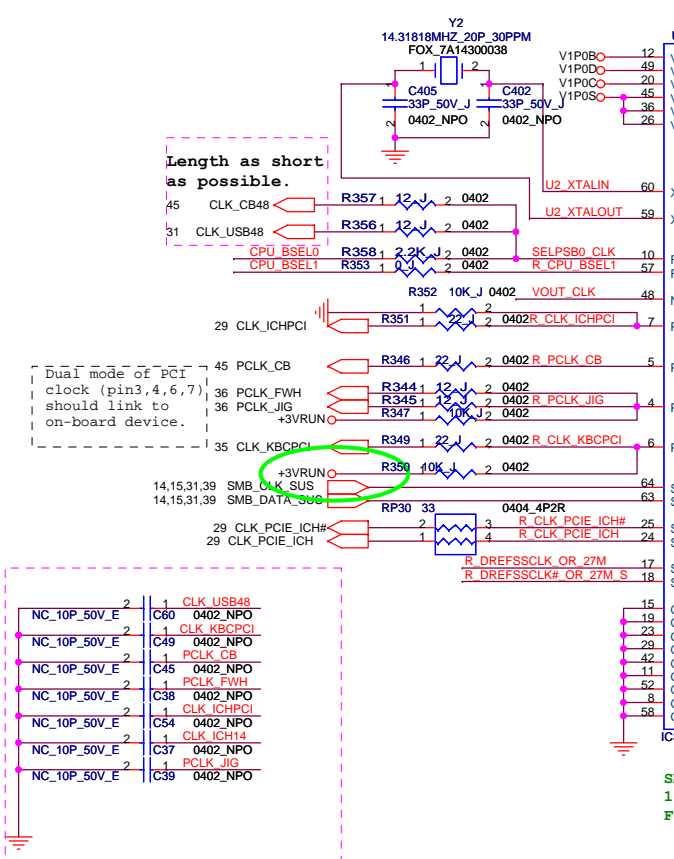
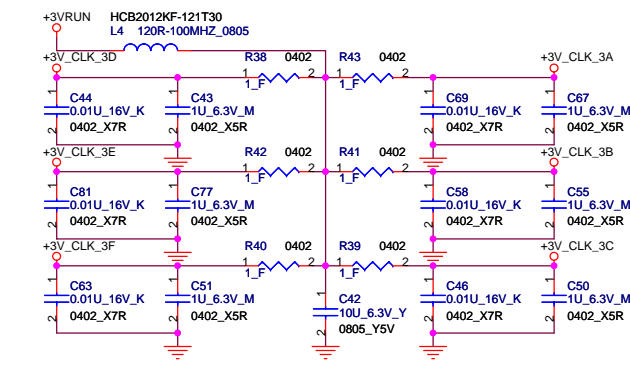
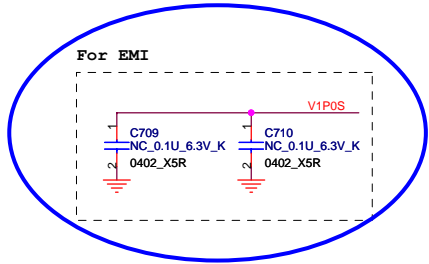
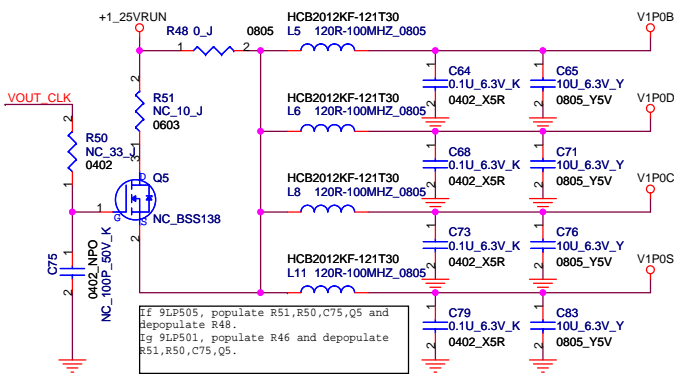
CPU SOCKET_478P
 FOX_P24782A-274M-01



Same Length

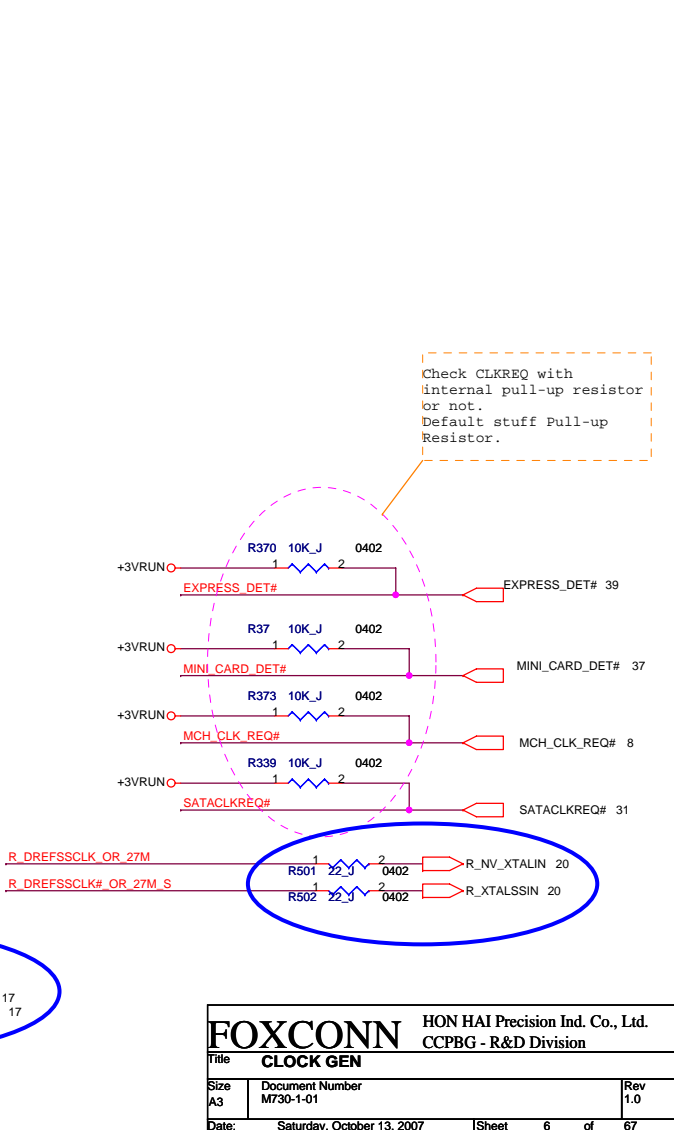
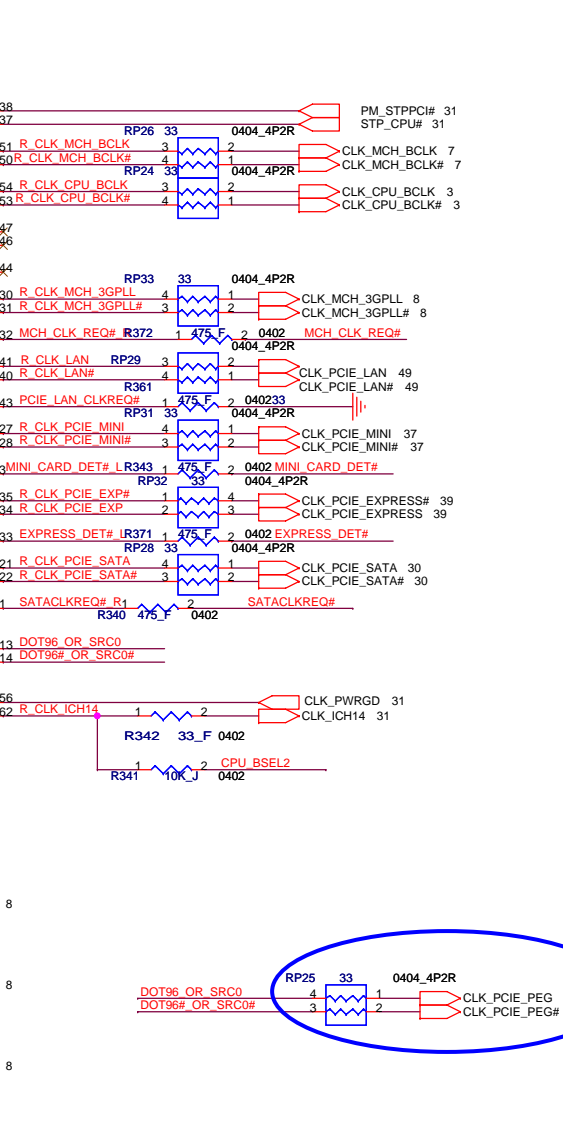
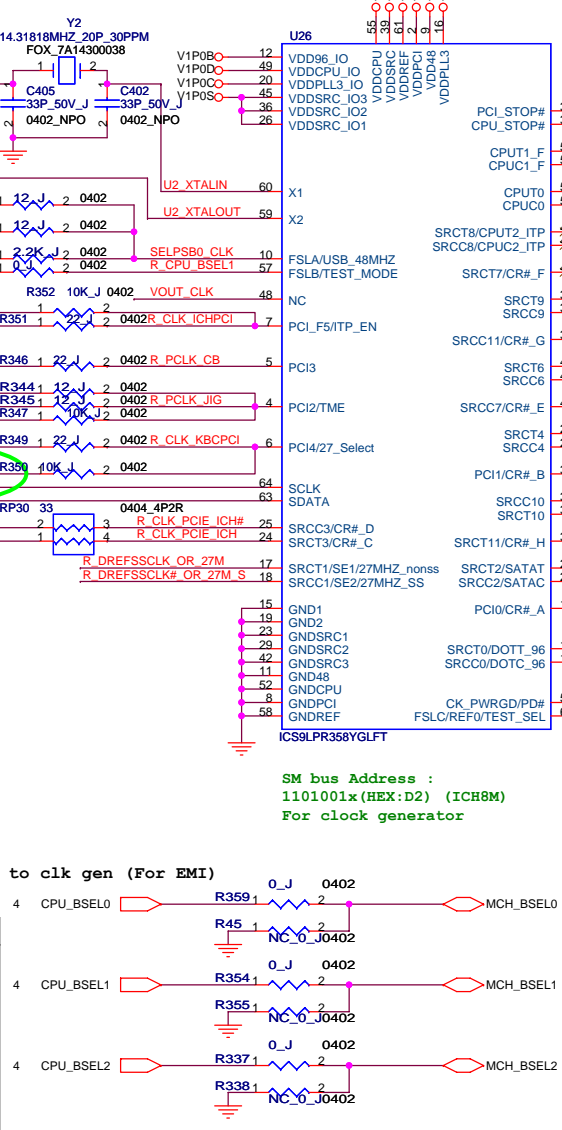
Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of CPU.
 width=18 mil
 spacing=7 mil





FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33



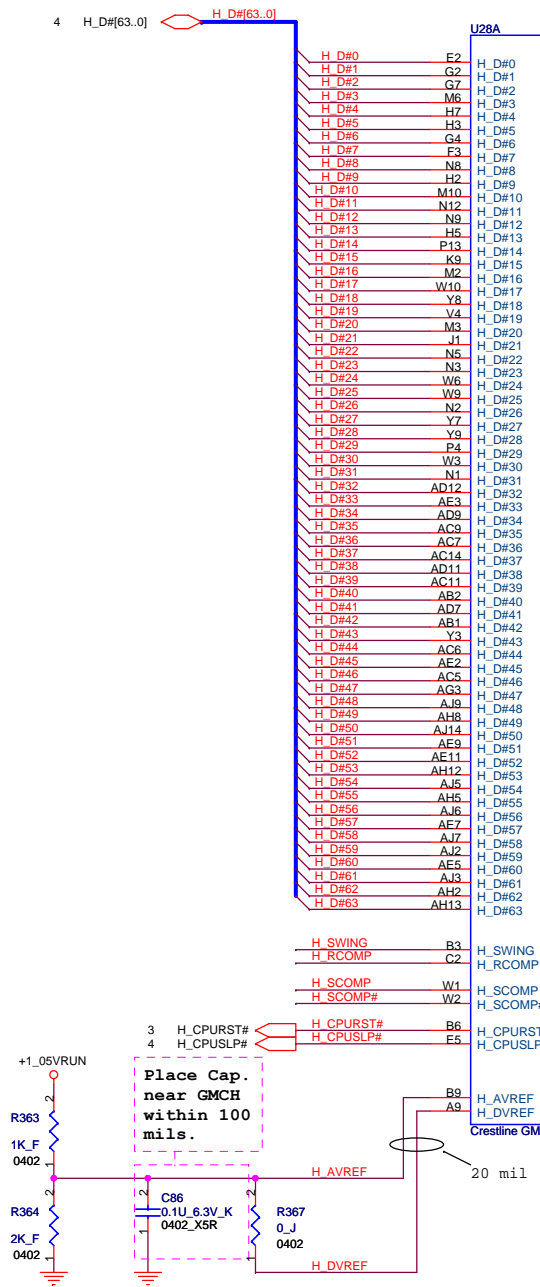
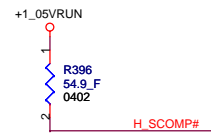
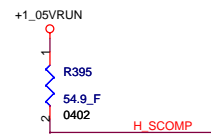
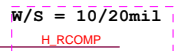
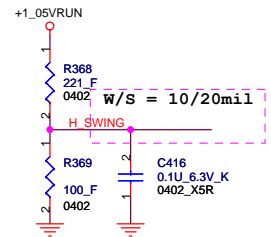
Check CLKREQ# with internal pull-up resistor or not. Default stuff Pull-up Resistor.

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 CCPBG - R&D Division

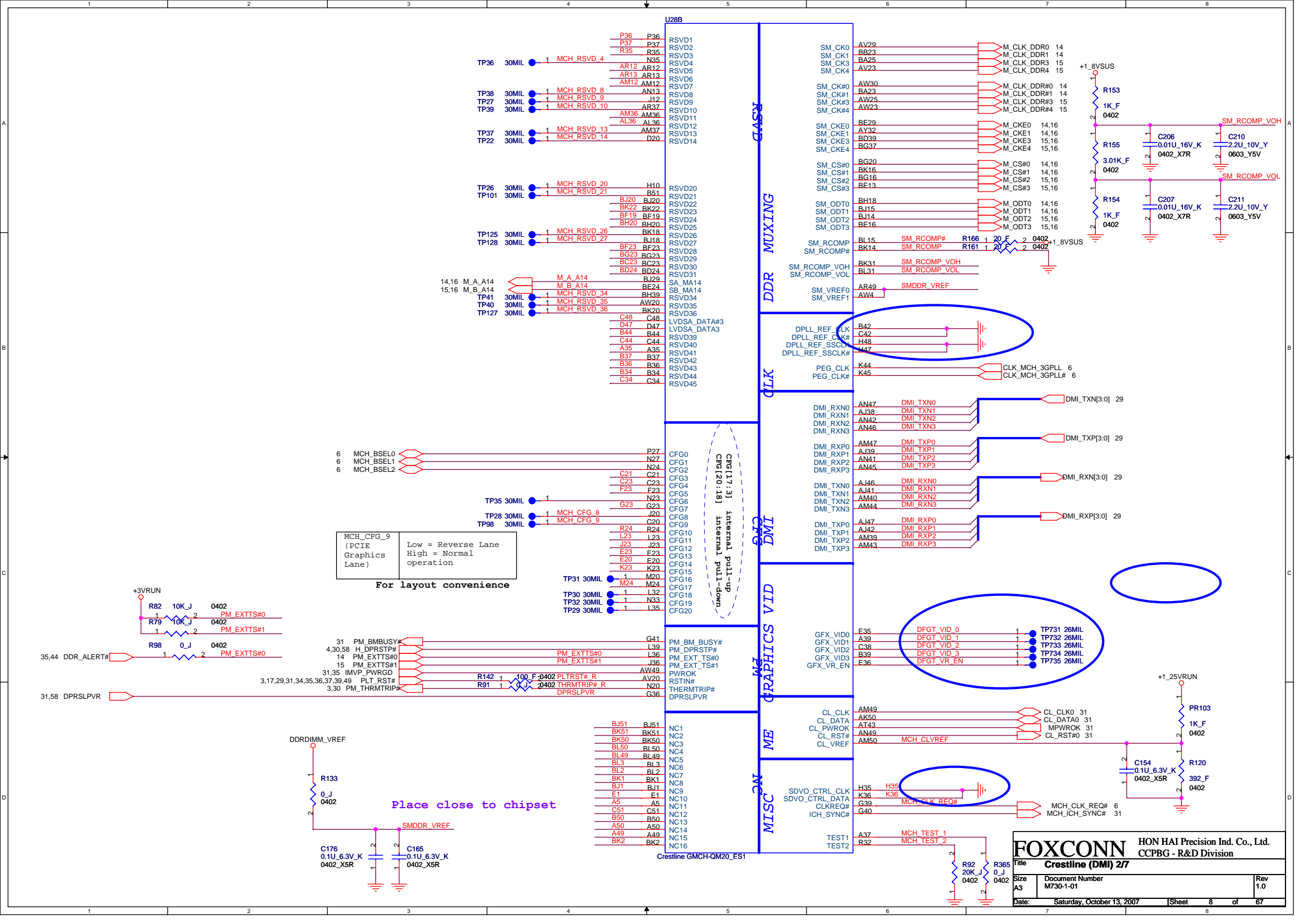
Title: **CLOCK GEN**

Size A3 Document Number M730-1-01 Rev 1.0

Date: Saturday, October 13, 2007 Sheet 6 of 67



HOST

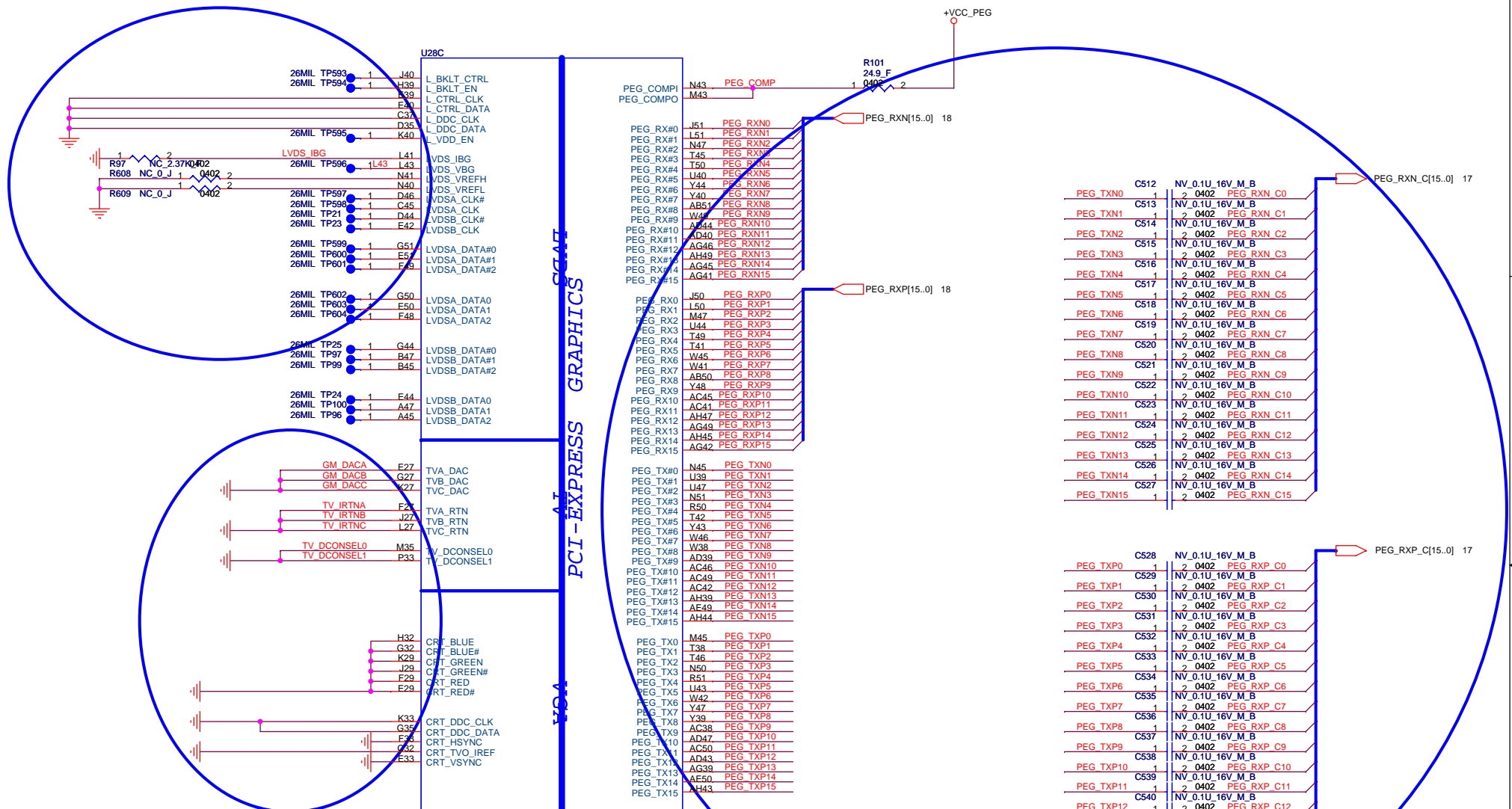


MCH_CFG_9
(PCIe Graphics Lane)
Low = Reverse Lane
High = Normal operation

For layout convenience

Place close to chipset

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Crestline (DMI) 2/7		CCPBG - R&D Division	
Title	Document Number	Rev 1.0	
Size A3	M730-1-01		
Date:	Saturday, October 13, 2007	Sheet	8 of 67



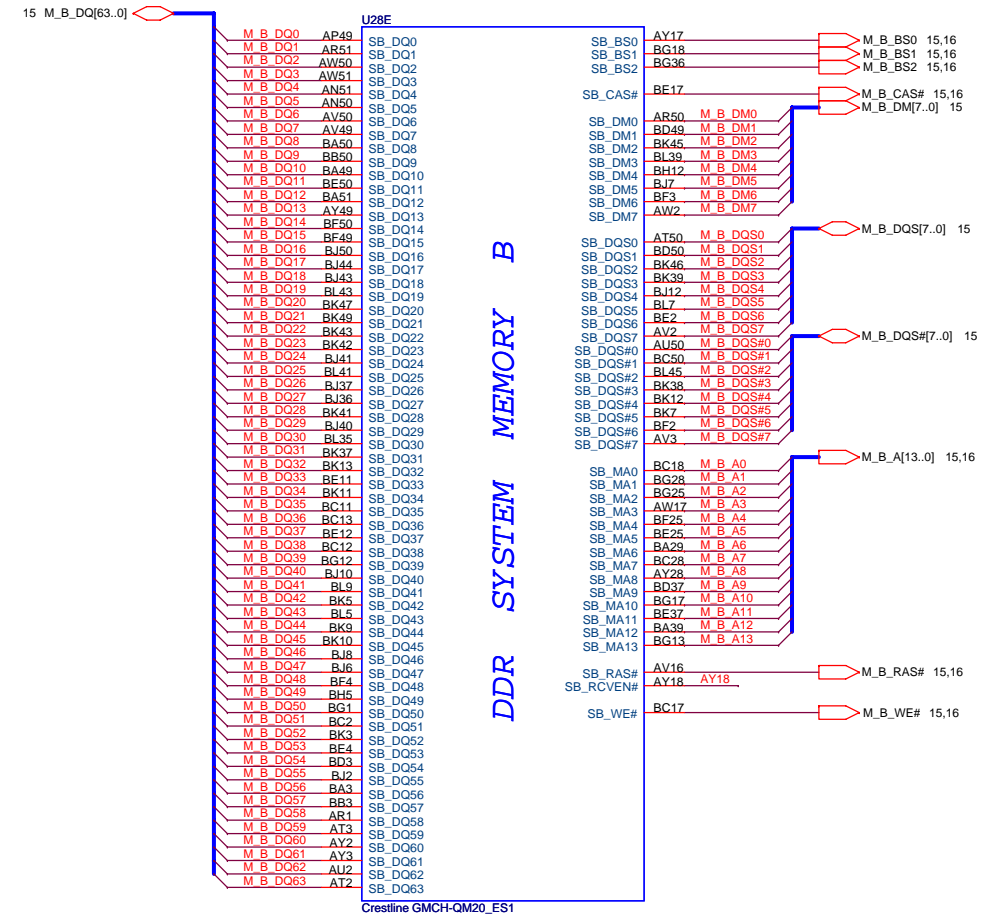
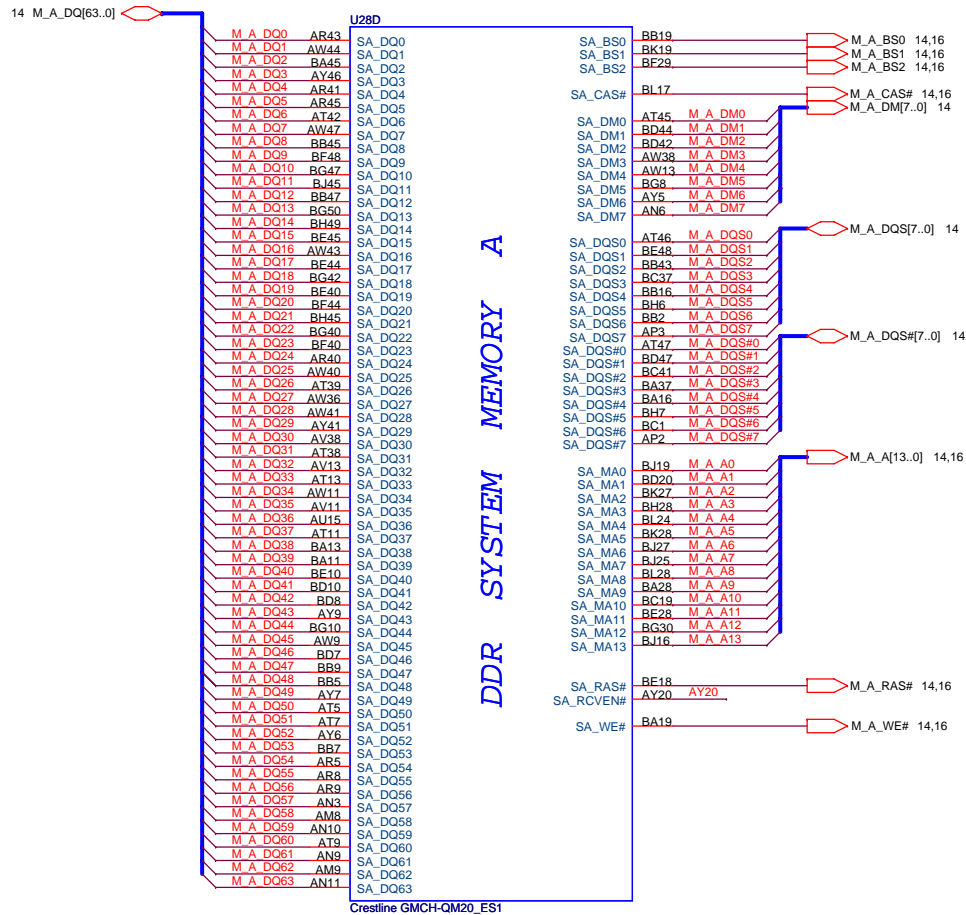
PCI-EXPRESS GRAPHICS

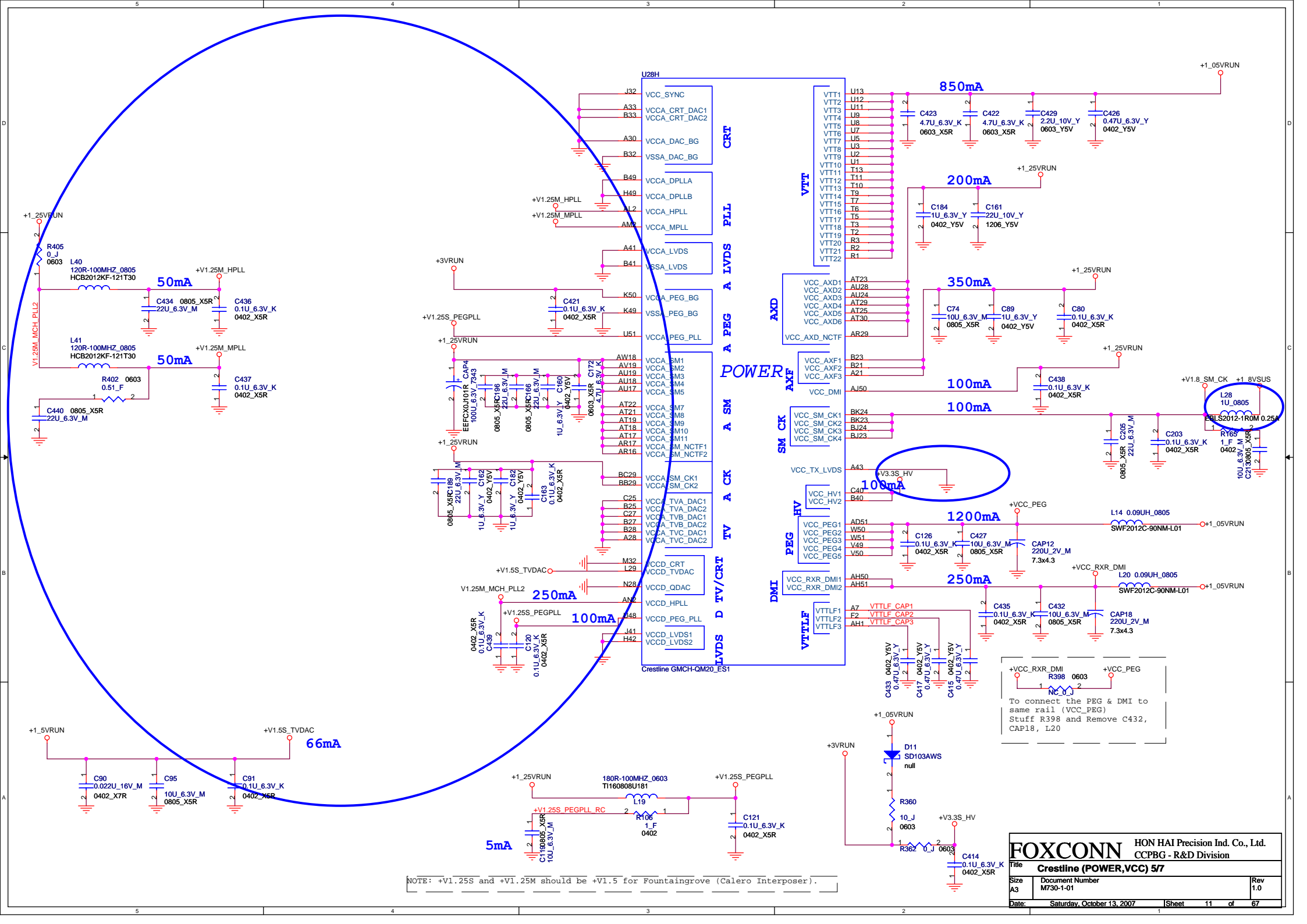
Pin	Signal	Component
L40	L_BKLT_CTRL	U28C
H39	L_BKLT_EN	U28C
E30	L_CTRL_CLK	U28C
C37	L_CTRL_DATA	U28C
D35	L_DDC_CLK	U28C
K40	L_DDC_DATA	U28C
L41	L_VDD_EN	U28C
L43	LVDS_IBG	U28C
N41	LVDS_VBG	U28C
N40	LVDS_VREFH	U28C
N42	LVDS_VREFL	U28C
D46	LVDS_CLK#	U28C
C45	LVDSA_CLK	U28C
D44	LVDSA_CLK#	U28C
E42	LVDSB_CLK	U28C
G51	LVDSA_DATA#0	U28C
E57	LVDSA_DATA#1	U28C
F49	LVDSA_DATA#2	U28C
G50	LVDSA_DATA0	U28C
E50	LVDSA_DATA1	U28C
F48	LVDSA_DATA2	U28C
G44	LVDSB_DATA#0	U28C
B47	LVDSB_DATA#1	U28C
B45	LVDSB_DATA#2	U28C
F44	LVDSB_DATA0	U28C
A47	LVDSB_DATA1	U28C
A45	LVDSB_DATA2	U28C
E27	TVA_DAC	U28C
G27	TVB_DAC	U28C
K27	TVC_DAC	U28C
F27	TVA_RTNA	U28C
J27	TVB_RTNA	U28C
L27	TVC_RTNA	U28C
M35	TV_DCONSEL0	U28C
P33	TV_DCONSEL1	U28C
H32	CRT_BLUE	U28C
G32	CRT_BLUE#	U28C
K29	CRT_GREEN	U28C
J29	CRT_GREEN#	U28C
F29	CRT_RED	U28C
E29	CRT_RED#	U28C
G33	CRT_DDC_CLK	U28C
G32	CRT_DDC_DATA	U28C
F32	CRT_HSYNC	U28C
E33	CRT_TVO_IREF	U28C
E33	CRT_VSYNC	U28C

N43	PEG_COMP	R101
M43	PEG_COMPO	R101
J51	PEG_RXN0	PEG_RXN[15..0]
L51	PEG_RXN1	PEG_RXN[15..0]
N47	PEG_RXN2	PEG_RXN[15..0]
T45	PEG_RXN3	PEG_RXN[15..0]
T50	PEG_RXN4	PEG_RXN[15..0]
U40	PEG_RXN5	PEG_RXN[15..0]
Y44	PEG_RXN6	PEG_RXN[15..0]
Y40	PEG_RXN7	PEG_RXN[15..0]
AB57	PEG_RXN8	PEG_RXN[15..0]
W45	PEG_RXN9	PEG_RXN[15..0]
AD44	PEG_RXN10	PEG_RXN[15..0]
D40	PEG_RXN11	PEG_RXN[15..0]
AG46	PEG_RXN12	PEG_RXN[15..0]
AH49	PEG_RXN13	PEG_RXN[15..0]
AG45	PEG_RXN14	PEG_RXN[15..0]
AG41	PEG_RXN15	PEG_RXN[15..0]
J50	PEG_RXP0	PEG_RXP[15..0]
L50	PEG_RXP1	PEG_RXP[15..0]
M47	PEG_RXP2	PEG_RXP[15..0]
U44	PEG_RXP3	PEG_RXP[15..0]
T49	PEG_RXP4	PEG_RXP[15..0]
T41	PEG_RXP5	PEG_RXP[15..0]
W45	PEG_RXP6	PEG_RXP[15..0]
W41	PEG_RXP7	PEG_RXP[15..0]
AB50	PEG_RXP8	PEG_RXP[15..0]
Y48	PEG_RXP9	PEG_RXP[15..0]
AC45	PEG_RXP10	PEG_RXP[15..0]
AC47	PEG_RXP11	PEG_RXP[15..0]
AH47	PEG_RXP12	PEG_RXP[15..0]
AG49	PEG_RXP13	PEG_RXP[15..0]
AH45	PEG_RXP14	PEG_RXP[15..0]
AG42	PEG_RXP15	PEG_RXP[15..0]
N45	PEG_TXN0	PEG_TXN[15..0]
U39	PEG_TXN1	PEG_TXN[15..0]
L47	PEG_TXN2	PEG_TXN[15..0]
N51	PEG_TXN3	PEG_TXN[15..0]
R50	PEG_TXN4	PEG_TXN[15..0]
T42	PEG_TXN5	PEG_TXN[15..0]
Y43	PEG_TXN6	PEG_TXN[15..0]
W46	PEG_TXN7	PEG_TXN[15..0]
W38	PEG_TXN8	PEG_TXN[15..0]
AD39	PEG_TXN9	PEG_TXN[15..0]
AC46	PEG_TXN10	PEG_TXN[15..0]
AC49	PEG_TXN11	PEG_TXN[15..0]
AC42	PEG_TXN12	PEG_TXN[15..0]
AH38	PEG_TXN13	PEG_TXN[15..0]
AE49	PEG_TXN14	PEG_TXN[15..0]
AH44	PEG_TXN15	PEG_TXN[15..0]
M45	PEG_TXP0	PEG_TXP[15..0]
T38	PEG_TXP1	PEG_TXP[15..0]
T46	PEG_TXP2	PEG_TXP[15..0]
N50	PEG_TXP3	PEG_TXP[15..0]
R51	PEG_TXP4	PEG_TXP[15..0]
U43	PEG_TXP5	PEG_TXP[15..0]
W42	PEG_TXP6	PEG_TXP[15..0]
Y47	PEG_TXP7	PEG_TXP[15..0]
Y39	PEG_TXP8	PEG_TXP[15..0]
AC38	PEG_TXP9	PEG_TXP[15..0]
AD47	PEG_TXP10	PEG_TXP[15..0]
AC50	PEG_TXP11	PEG_TXP[15..0]
AD43	PEG_TXP12	PEG_TXP[15..0]
AG39	PEG_TXP13	PEG_TXP[15..0]
AE50	PEG_TXP14	PEG_TXP[15..0]
AH43	PEG_TXP15	PEG_TXP[15..0]

C512	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C513	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C514	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C515	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C516	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C517	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C518	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C519	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C520	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C521	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C522	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C523	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C524	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C525	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C526	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C527	NV_0.1U_16V_M_B	PEG_RXN_C[15..0]
C528	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C529	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C530	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C531	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C532	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C533	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C534	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C535	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C536	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C537	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C538	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C539	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C540	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C541	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C542	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]
C543	NV_0.1U_16V_M_B	PEG_RXP_C[15..0]

Crestline GMCH-QM20_ES1



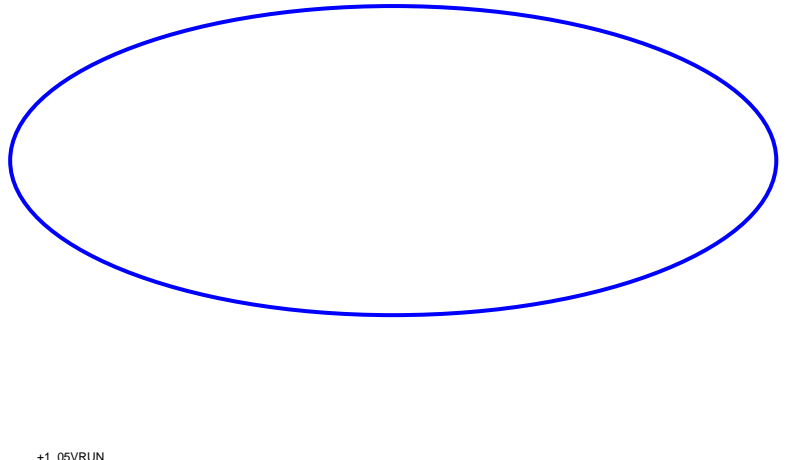
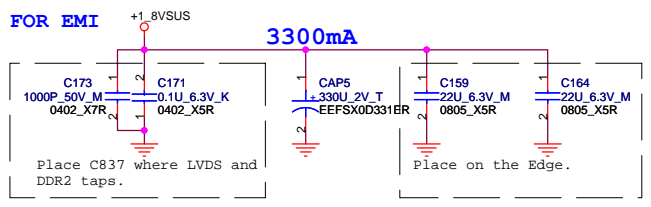
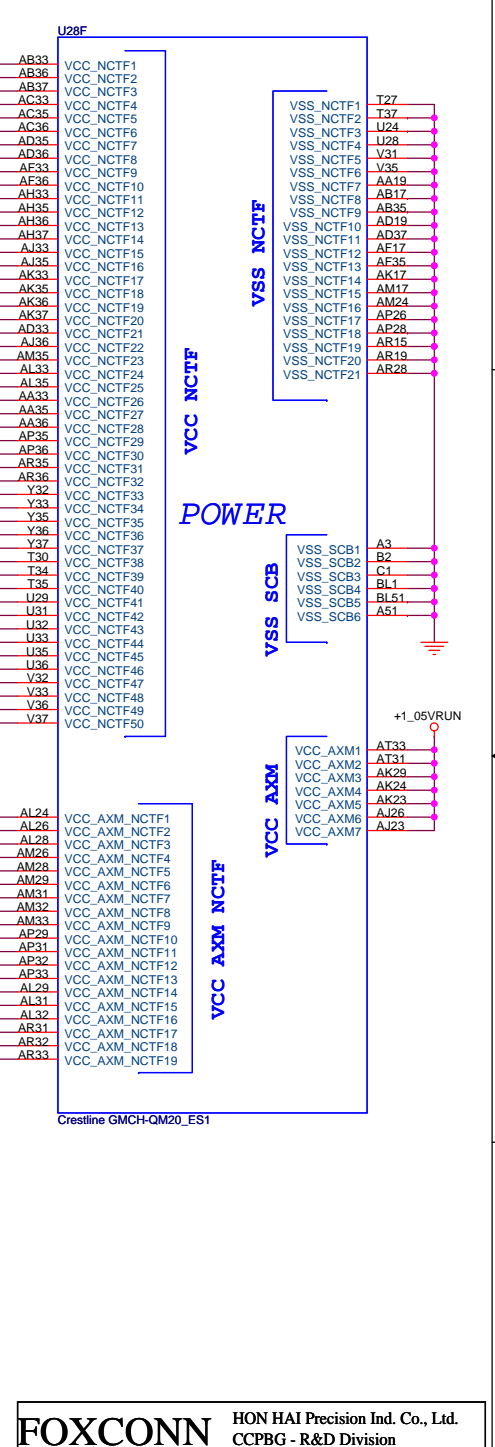
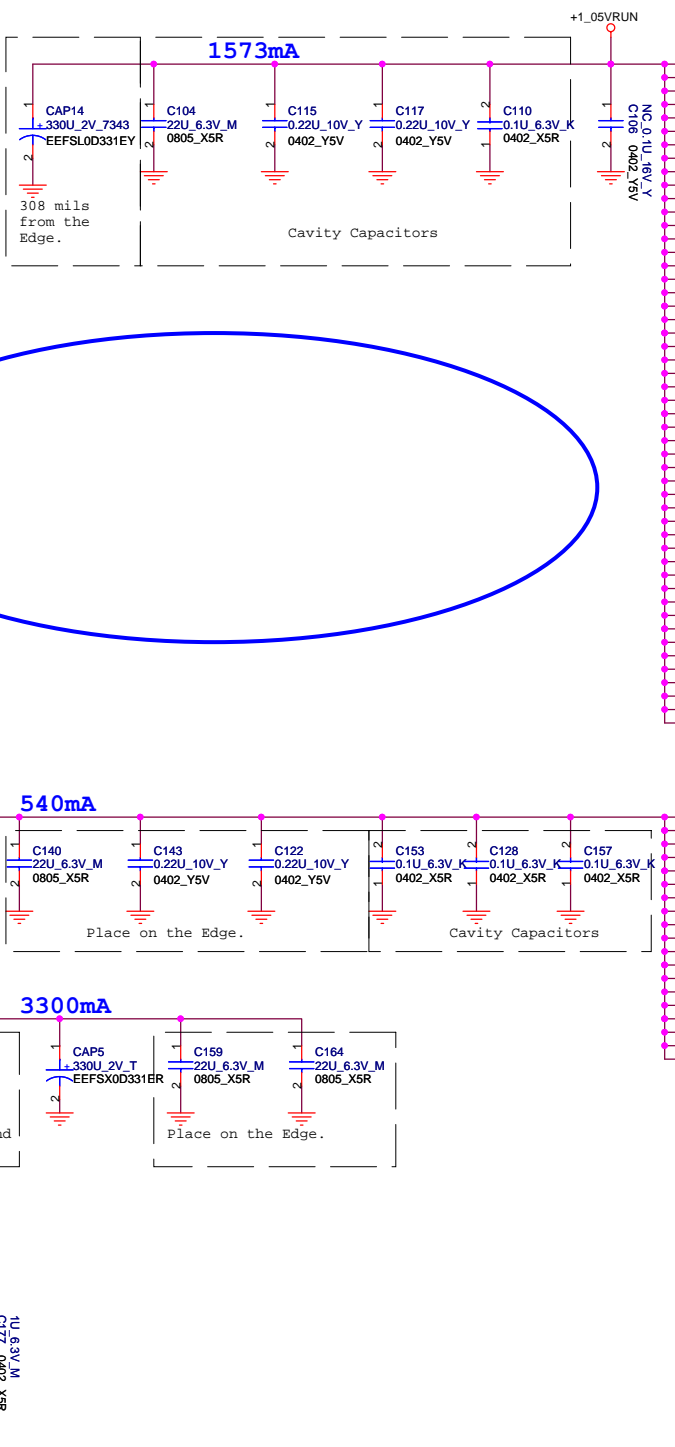
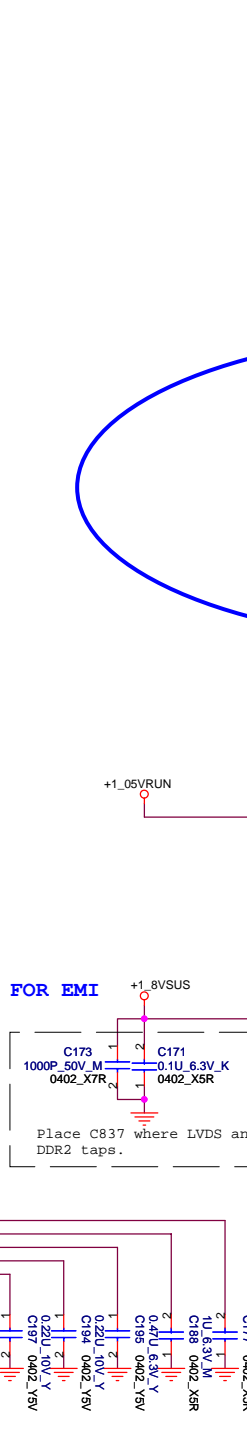
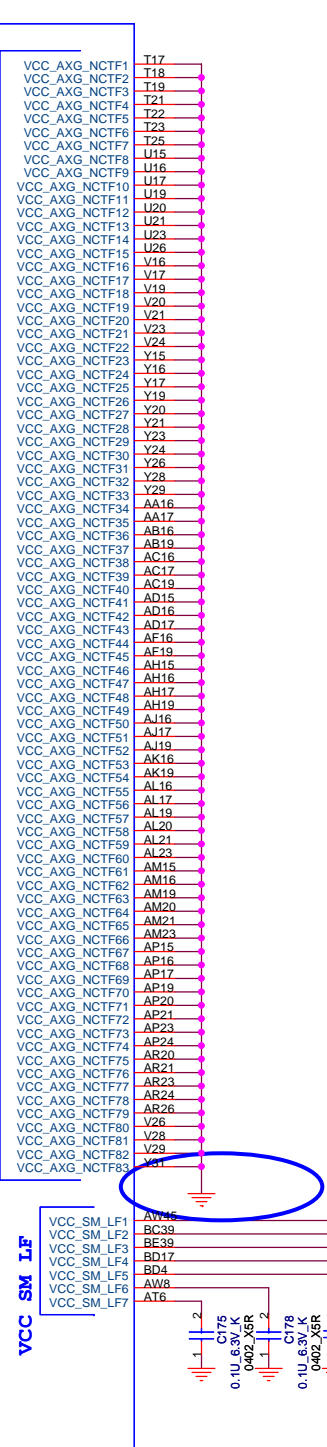
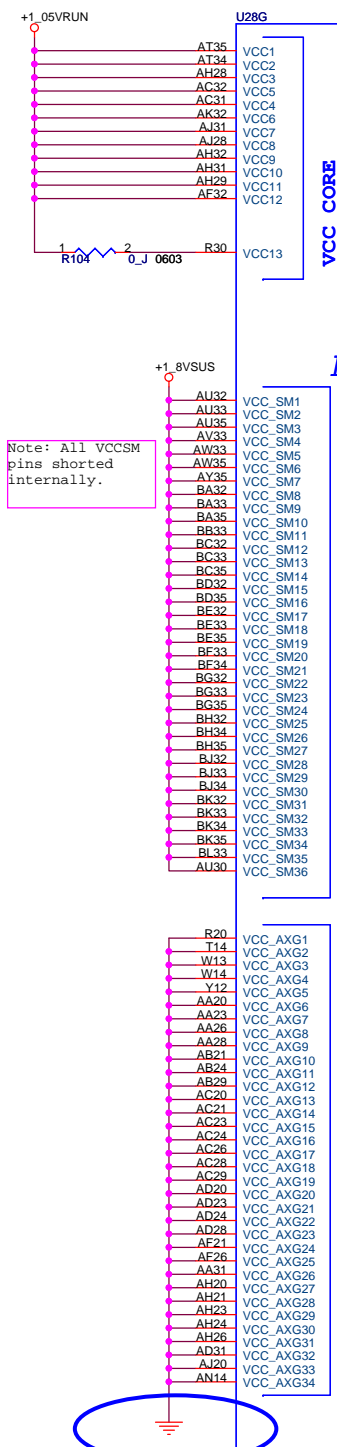


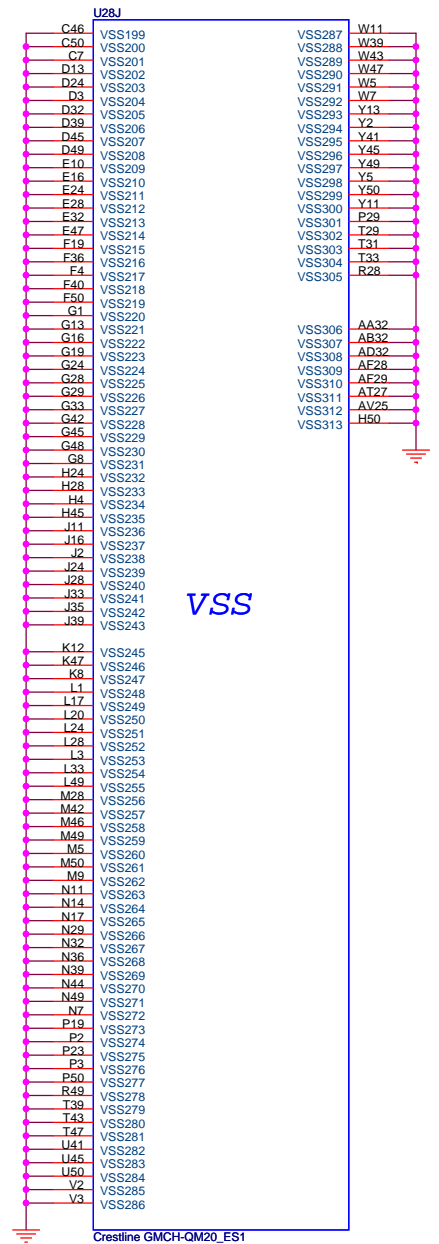
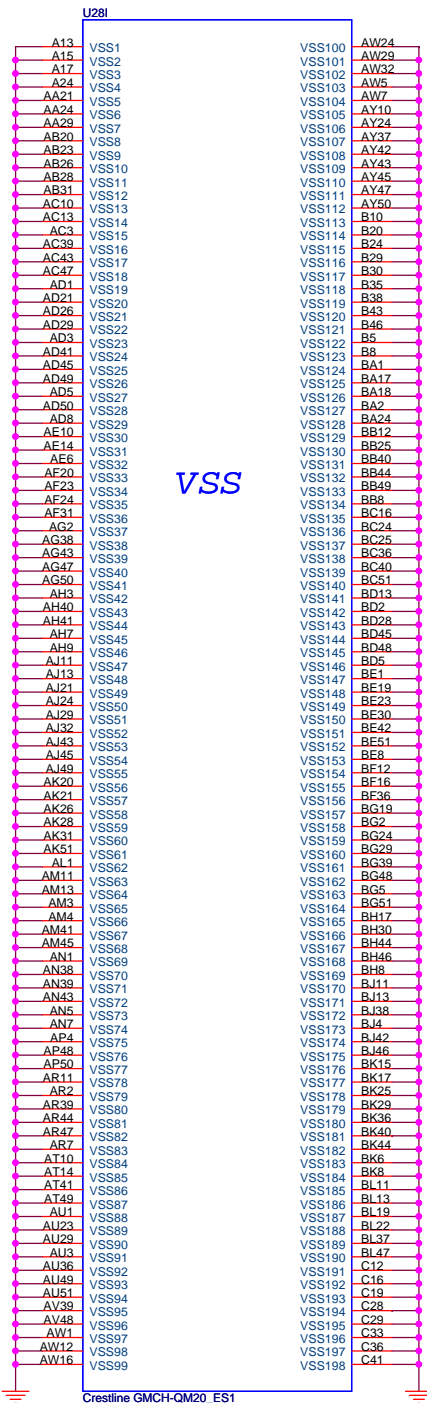
Crestline GMCH-QM20_ES1

NOTE: +V1.25S and +V1.25M should be +V1.5 for Fountaingrove (Calero Interposer).

To connect the PEG & DMI to same rail (VCC_PEG) Stuff R398 and Remove C432, CAP18, L20

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Crestline (POWER,VCC) 57			
Size A3	Document Number M730-1-01	Rev 1.0	
Date: Saturday, October 13, 2007	Sheet 11	of 67	



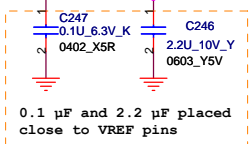


Crestline GMCH-QM20_ES1

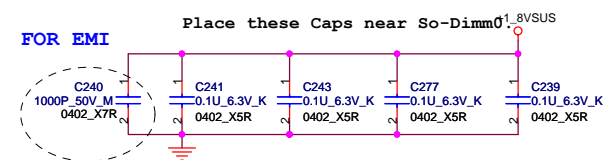
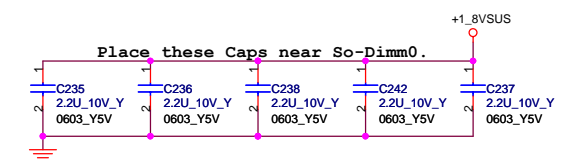
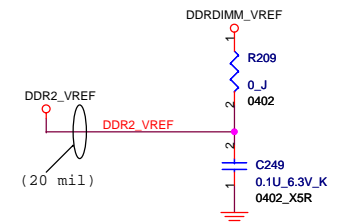
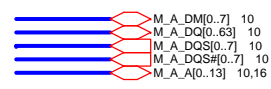
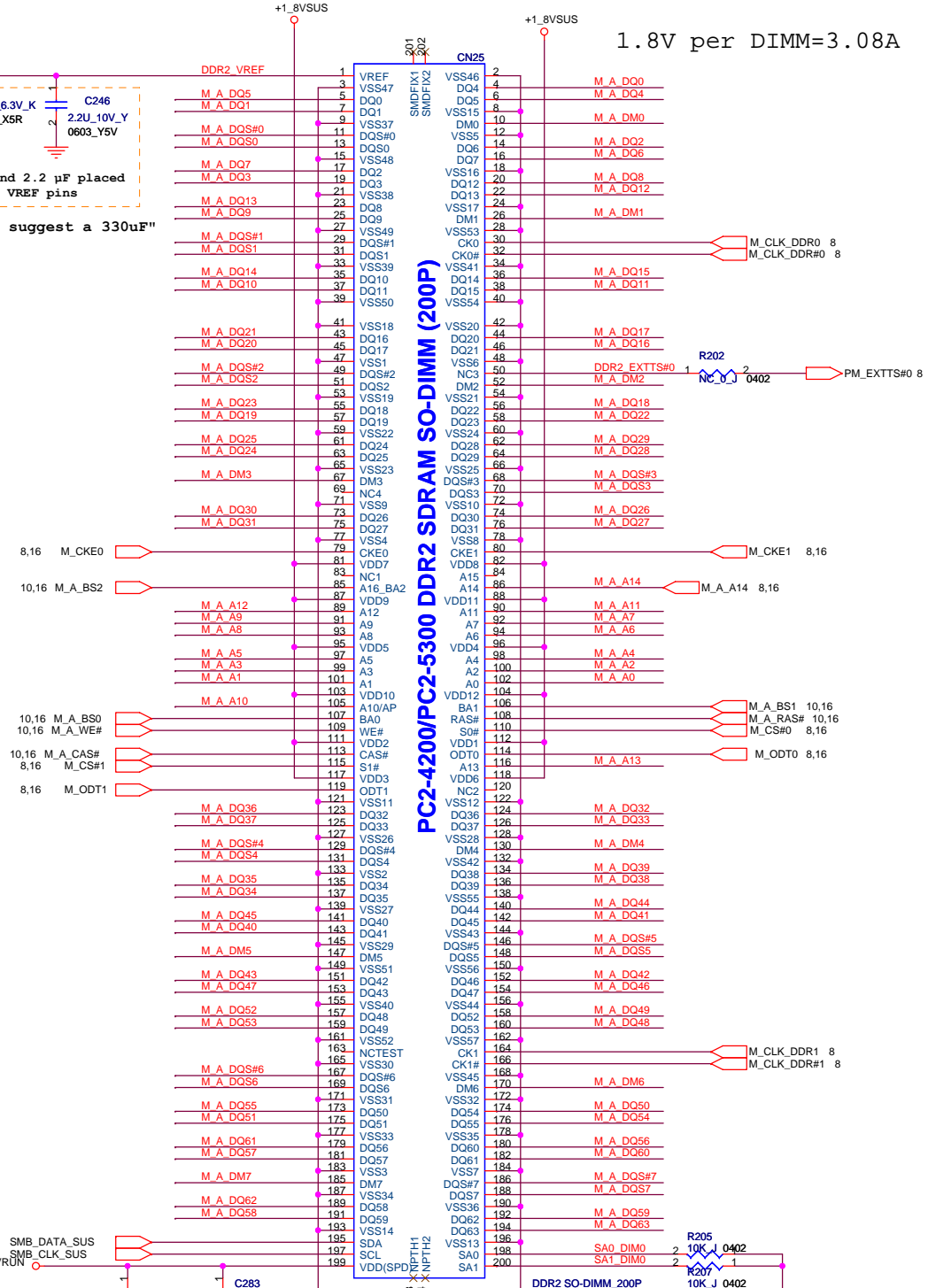
Crestline GMCH-QM20_ES1

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Crestline (VSS) 7/7		CCPBG - R&D Division	
Title	Document Number	Rev	
A3	M730-1-01	1.0	
Date:	Saturday, October 13, 2007	Sheet	13 of 67

1.8V per DIMM=3.08A



"Intel check list suggest a 330uF"

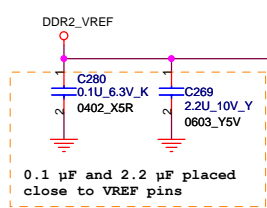


FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

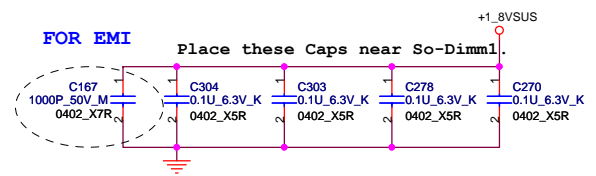
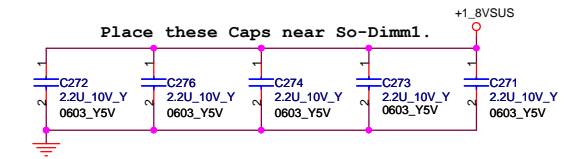
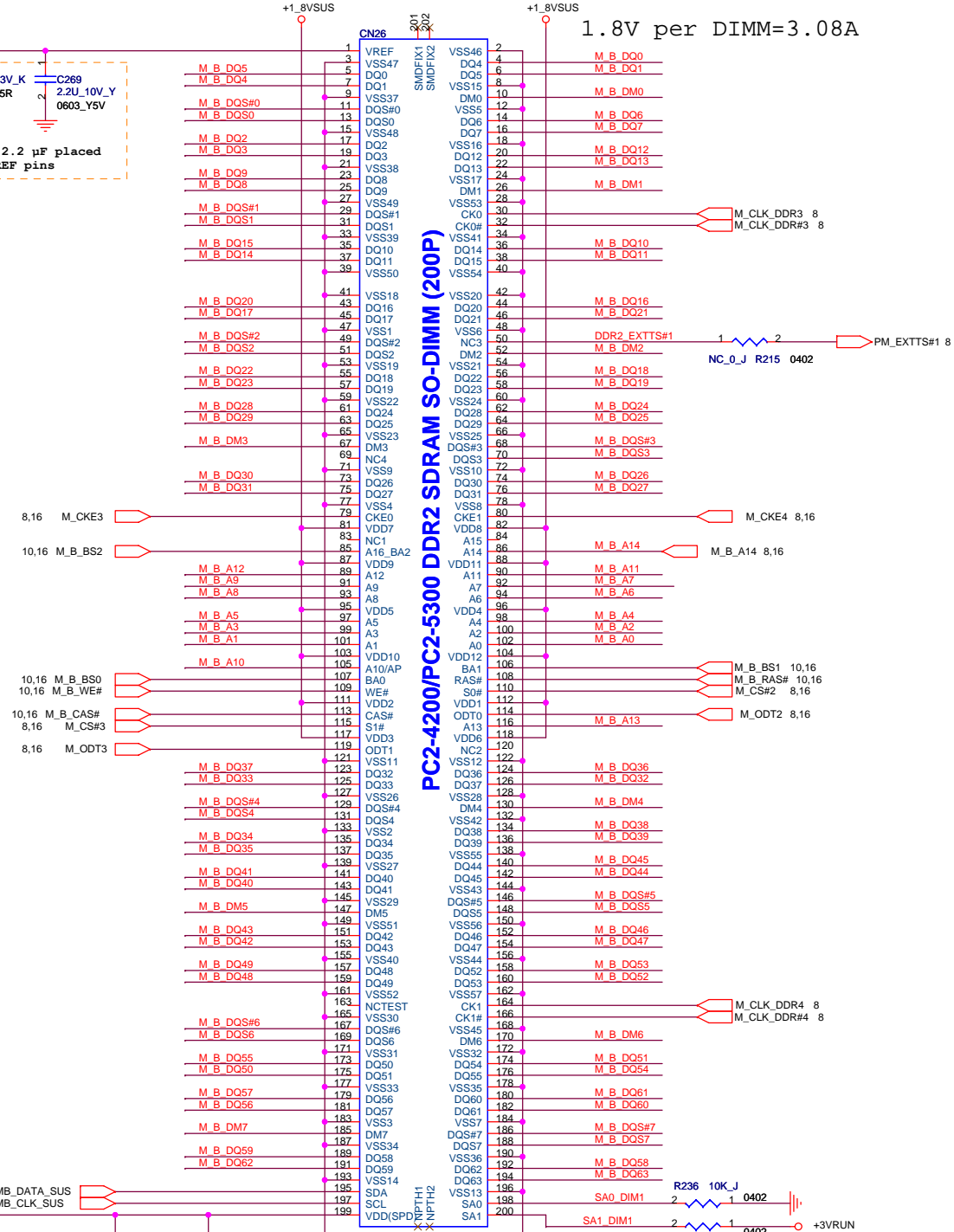
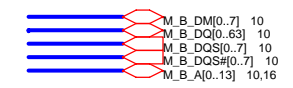
Title: **DDR(H)SO-DIMM_0**

Size A3	Document Number M730-1-01	Rev 1.0
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Date: Saturday, October 13, 2007 Sheet 14 of 67



1.8V per DIMM=3.08A

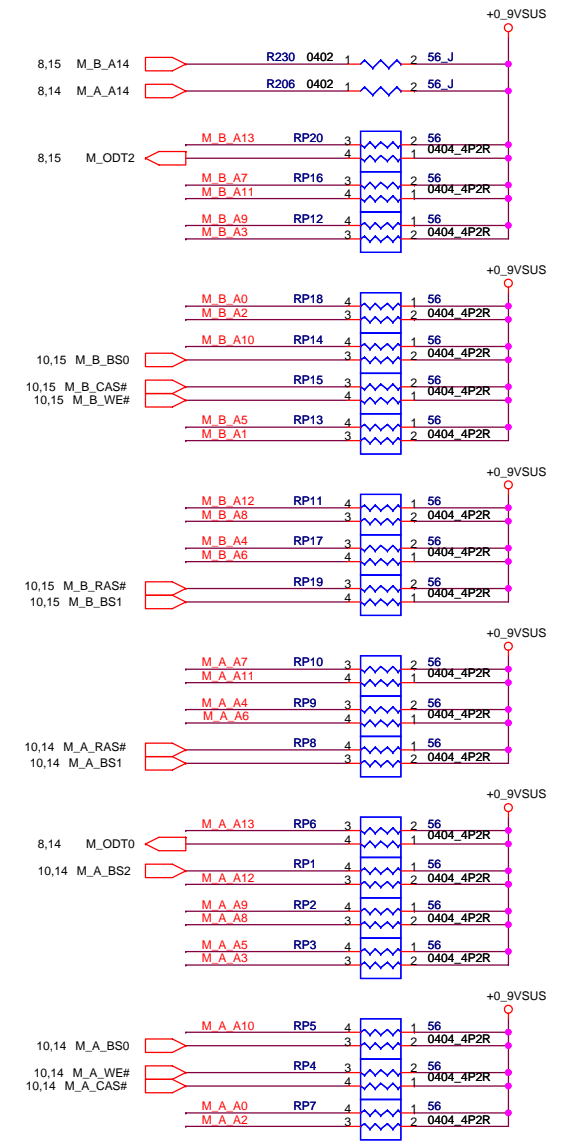
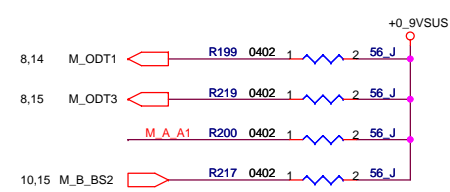
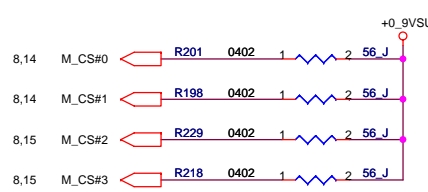
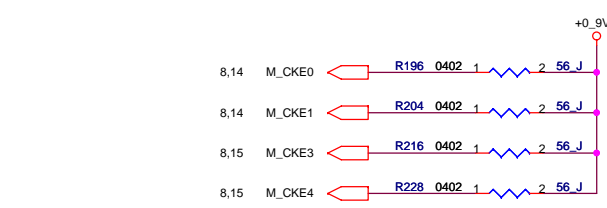
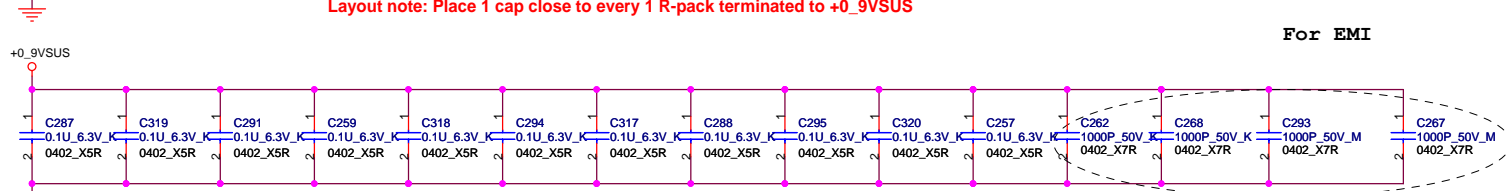
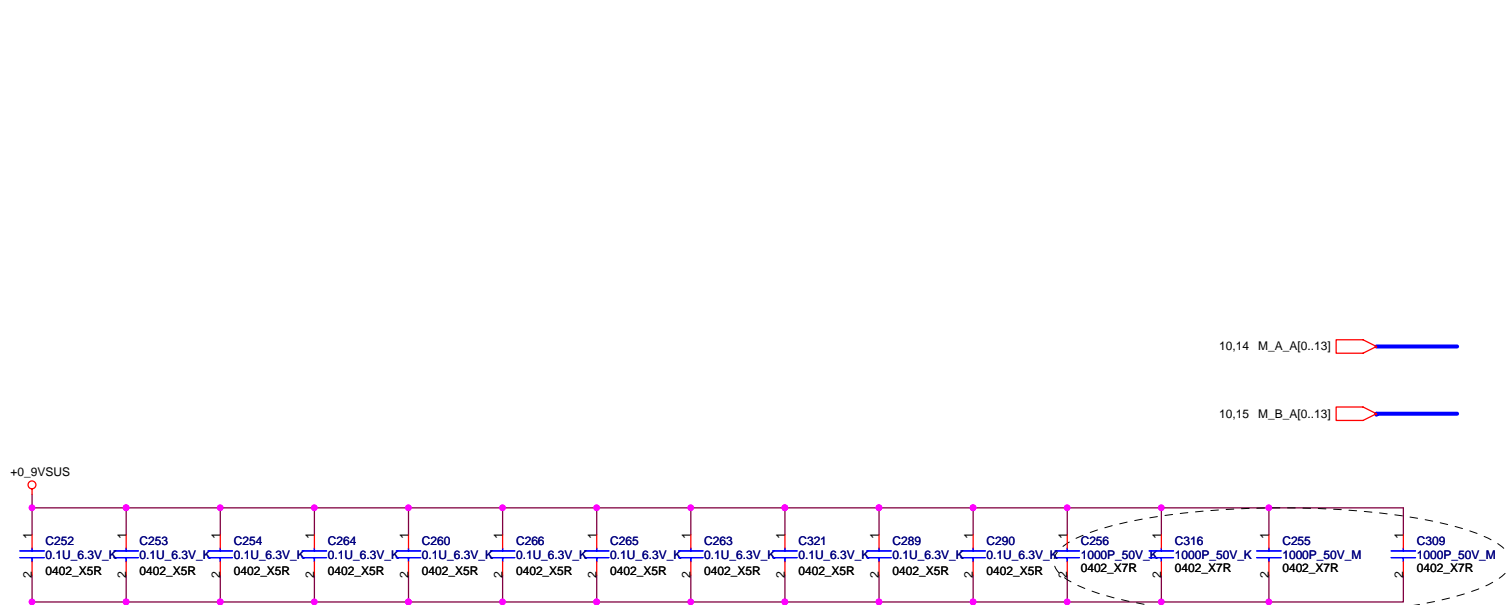


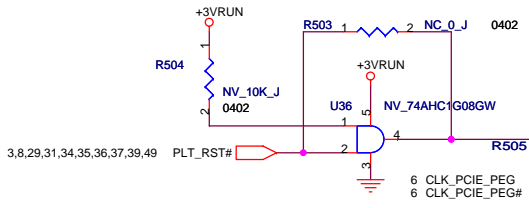
DIMM_1

SMBus Address: A4 (W) / A5 (R)

DIMM_1 is placed farther from the GMCH than DIMM_0

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DDR(I)SO-DIMM_1			
Size A3	Document Number M730-1-01	Rev 1.0	
Date:	Saturday, October 13, 2007	Sheet	15 of 67





- TXP0 AH15 PEX_TX0
- TXP1 AH16 PEX_TX1#
- TXN1 AG16 PEX_TX1#
- TXP2 AG17 PEX_TX2
- TXN2 AH17 PEX_TX2#
- TXP3 AG18 PEX_TX3
- TXN3 AH18 PEX_TX3#
- TXP4 AK18 PEX_TX4
- TXN4 AJ18 PEX_TX4#
- TXP5 AJ19 PEX_TX5
- TXN5 AH19 PEX_TX5#
- TXP6 AG20 PEX_TX6
- TXN6 AH20 PEX_TX6#
- TXP7 AG21 PEX_TX6#
- TXN7 AH21 PEX_TX7
- TXP8 AK21 PEX_TX8
- TXN8 AJ21 PEX_TX8#
- TXP9 AJ22 PEX_TX9
- TXN9 AH22 PEX_TX9#
- TXP10 AG23 PEX_TX9#
- TXN10 AH23 PEX_TX10
- TXP11 AK24 PEX_TX10#
- TXN11 AJ24 PEX_TX11
- TXP12 AJ25 PEX_TX12
- TXN12 AH25 PEX_TX12#
- TXP13 AH26 PEX_TX13#
- TXN13 AG26 PEX_TX13
- TXP14 AK27 PEX_TX14#
- TXN14 AJ27 PEX_TX14#
- TXP15 AJ28 PEX_TX15
- TXN15 AH27 PEX_TX15#

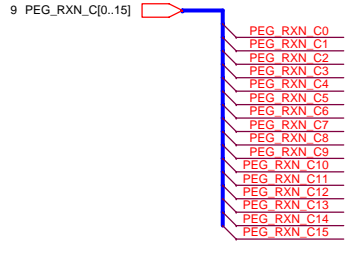
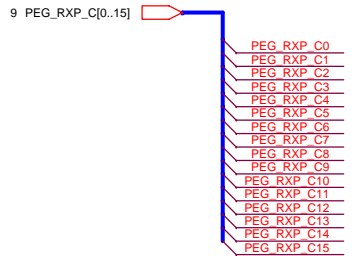
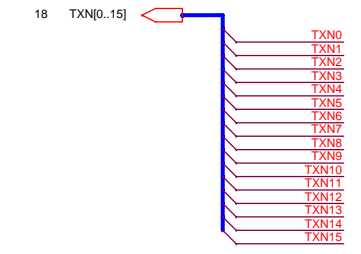
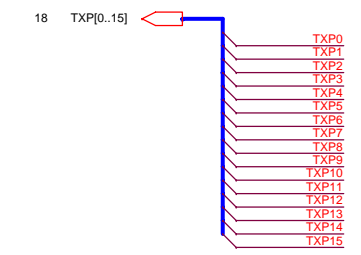
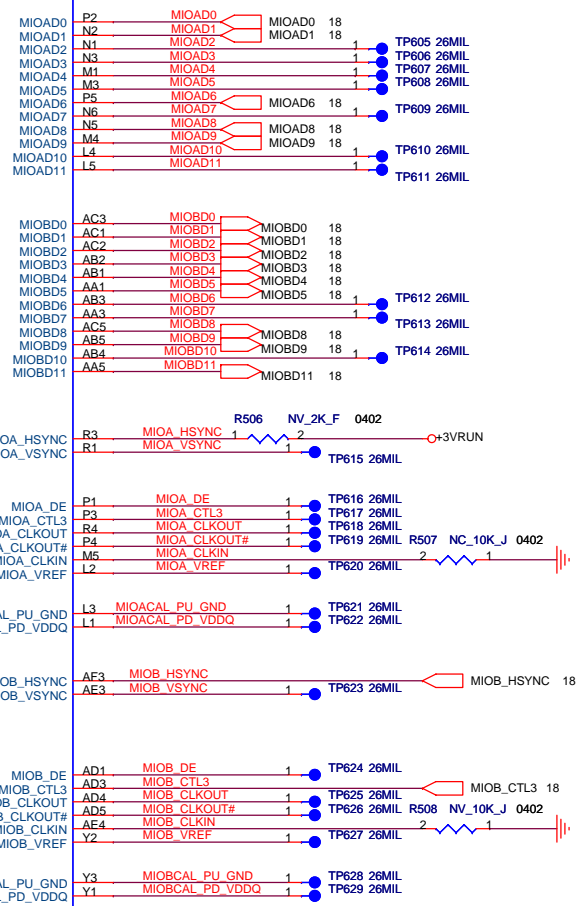
- PEG_RXP_C0 AK13 PEX_RX0
- PEG_RXN_C0 AK14 PEX_RX0#
- PEG_RXP_C1 AM14 PEX_RX1
- PEG_RXN_C1 AM15 PEX_RX1#
- PEG_RXP_C2 AL15 PEX_RX2
- PEG_RXN_C2 AL16 PEX_RX2#
- PEG_RXP_C3 AK16 PEX_RX3
- PEG_RXN_C3 AK17 PEX_RX3#
- PEG_RXP_C4 AL17 PEX_RX4
- PEG_RXN_C4 AL18 PEX_RX4#
- PEG_RXP_C5 AM18 PEX_RX5
- PEG_RXN_C5 AM19 PEX_RX5#
- PEG_RXP_C6 AK19 PEX_RX6
- PEG_RXN_C6 AK20 PEX_RX6#
- PEG_RXP_C7 AL20 PEX_RX7
- PEG_RXN_C7 AL21 PEX_RX7#
- PEG_RXP_C8 AM21 PEX_RX8
- PEG_RXN_C8 AM22 PEX_RX8#
- PEG_RXP_C9 AK22 PEX_RX9
- PEG_RXN_C9 AK23 PEX_RX9#
- PEG_RXP_C10 AL23 PEX_RX10
- PEG_RXN_C10 AL24 PEX_RX10#
- PEG_RXP_C11 AM24 PEX_RX11
- PEG_RXN_C11 AM25 PEX_RX11#
- PEG_RXP_C12 AK25 PEX_RX12
- PEG_RXN_C12 AK26 PEX_RX12#
- PEG_RXP_C13 AL26 PEX_RX13
- PEG_RXN_C13 AL27 PEX_RX13#
- PEG_RXP_C14 AM27 PEX_RX14
- PEG_RXN_C14 AM28 PEX_RX14#
- PEG_RXP_C15 AL28 PEX_RX15
- PEG_RXN_C15 AL29 PEX_RX15#

NV_NB8M-GT-B-A2(G86-750-A2)



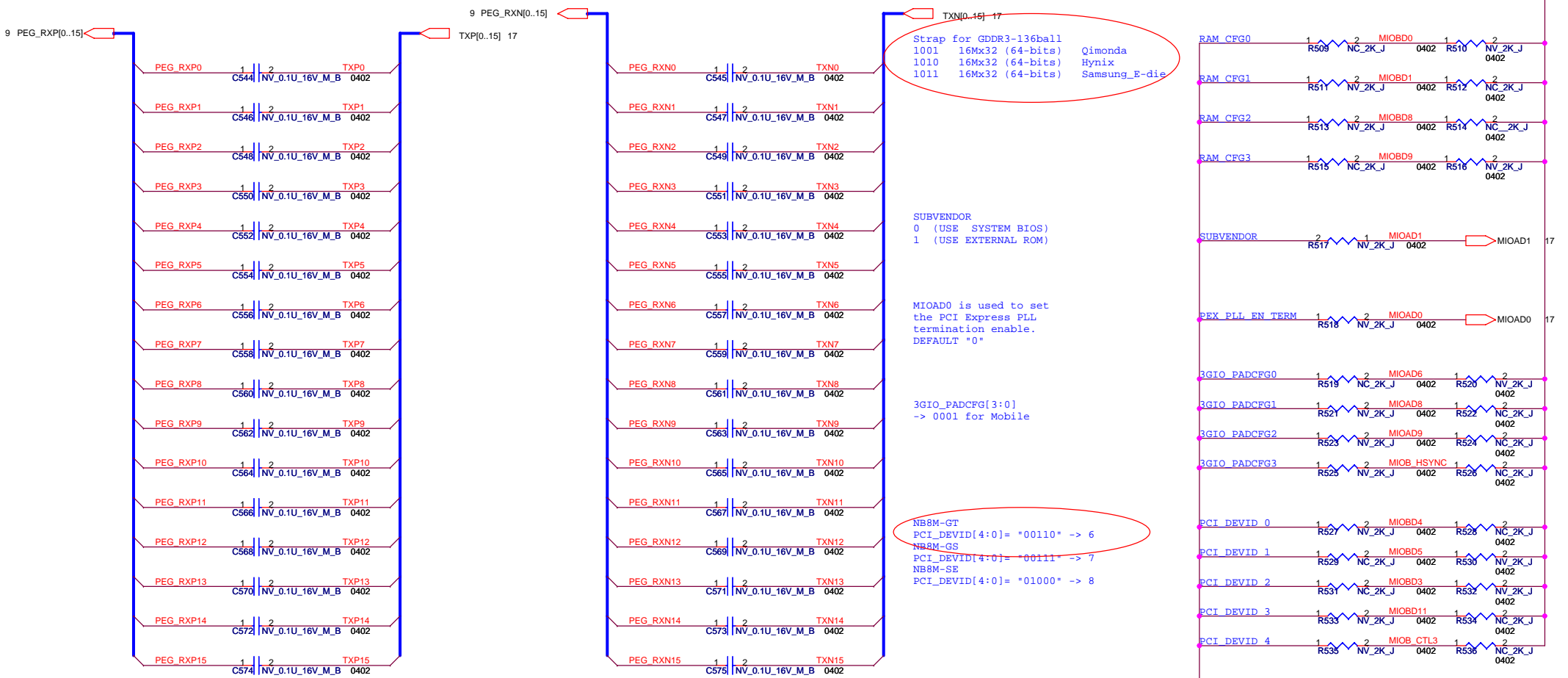
PCI EXPRESS

MULTI-USE I/O INTERFACE

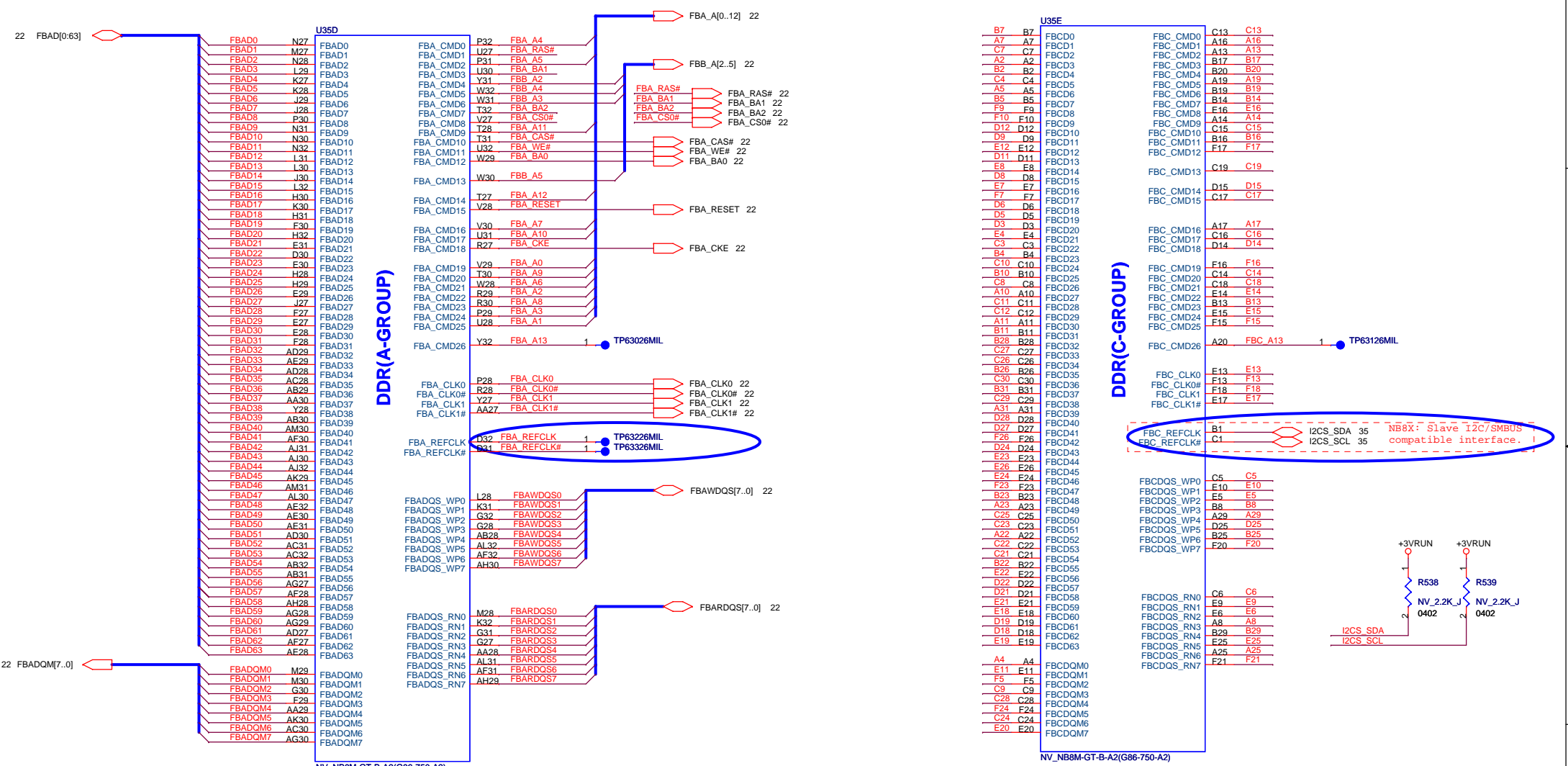


SKU			
Vendor	Qimonda (Infineon)	HYNIX	Samsung
Vendor PN	HYB18H512321BF-14	HY5RS123235BFP-14	K4J52324QE-BC14
H.H PN	13-HYB18H5-3003	13-HY5RS12-3001	13-K4J5232-3001
Configuration	NB8M-GT with 2pcs (16Mx32) GDDR3		
LOCATION	Stuff R511,R510	Stuff R512,R509	Stuff R512,R510
	No Stuff R512,R509	No Stuff R511,R510	No Stuff R511,R509

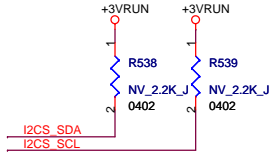
FAE: TV Mode Strap no use, remove.
(MIOAD7, MIOAD10, MIOBD6)

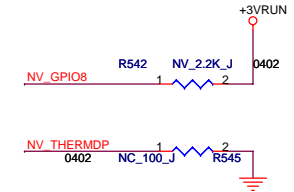
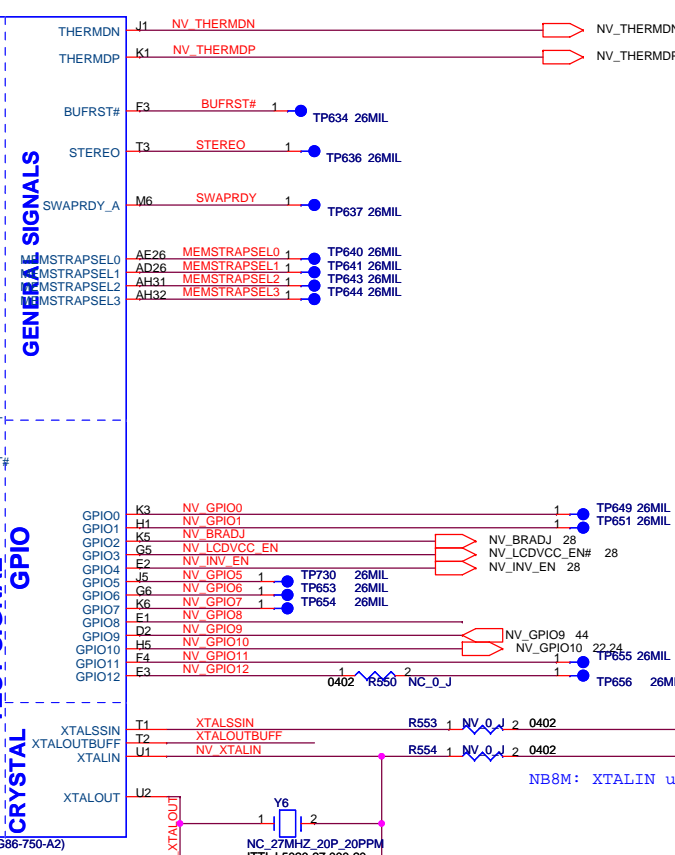
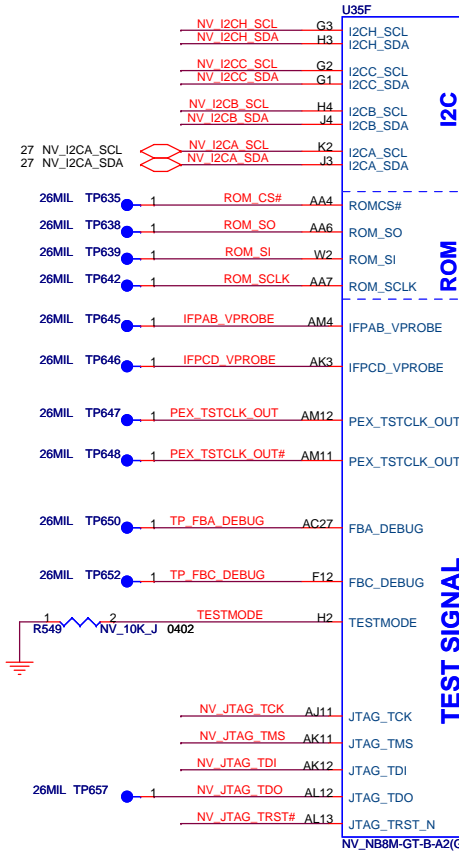
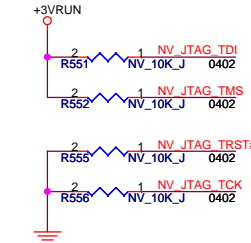
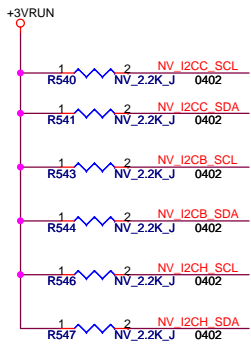


- MIOAD6 -> MIOAD6 17
- MIOAD8 -> MIOAD8 17
- MIOAD9 -> MIOAD9 17
- MIOBD0 -> MIOBD0 17
- MIOBD1 -> MIOBD1 17
- MIOBD3 -> MIOBD3 17
- MIOBD4 -> MIOBD4 17
- MIOBD5 -> MIOBD5 17
- MIOBD8 -> MIOBD8 17
- MIOBD9 -> MIOBD9 17
- MIOBD11 -> MIOBD11 17
- MIOB_CTL3 -> MIOB_CTL3 17
- MIOB_HSYNC -> MIOB_HSYNC 17

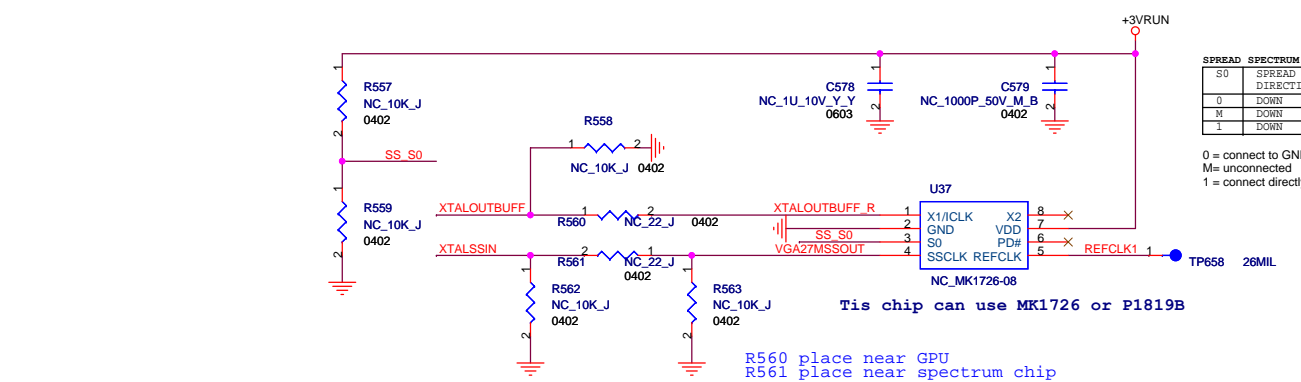
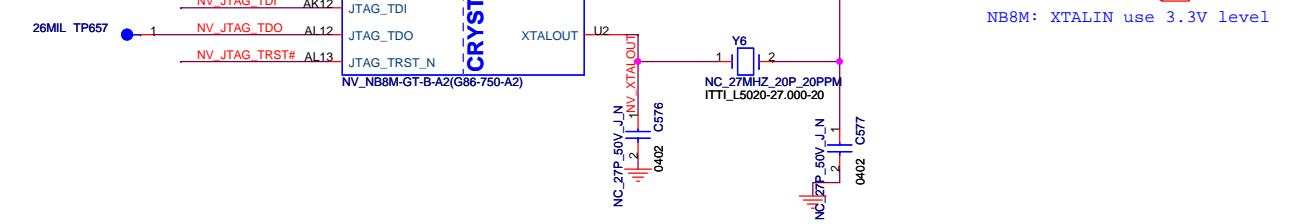


FBC_REFCLK# I2CS_SDA 35 NB8X Slave I2C/SMBUS compatible interface.
 FBC_REFCLK# I2CS_SCL 35





	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	Yes	TP	
GPIO1	I	Yes	TP	
GPIO2	O	Yes	Panel Brightness (PWM)	Active High
GPIO3	O	No	Panel Power Enable	Active Low
GPIO4	O	Yes	Panel Backlight On/Off	Active High
GPIO5	O	Yes	TP	
GPIO6	O	Yes	TP	
GPIO7	O	Yes	TP	
GPIO8	OD	No		
GPIO9	OD	No	THERM	Active Low
GPIO10	O	No	Memory Vref switch	
GPIO11	O	No	TP	
GPIO12	I	--	TP	



SPREAD SPECTRUM SETTING FOR MK			SPREAD SPECTRUM SETTING FOR P1819B		
S0	SPREAD DIRECTION	Spread Percentage(%)	SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8	0	DOWN	-1.25
M	DOWN	-0.6	1	DOWN	-1.75
1	DOWN	-2.5			

0 = connect to GND
M = unconnected
1 = connect directly to VDD

nVidia support Down -1.25%

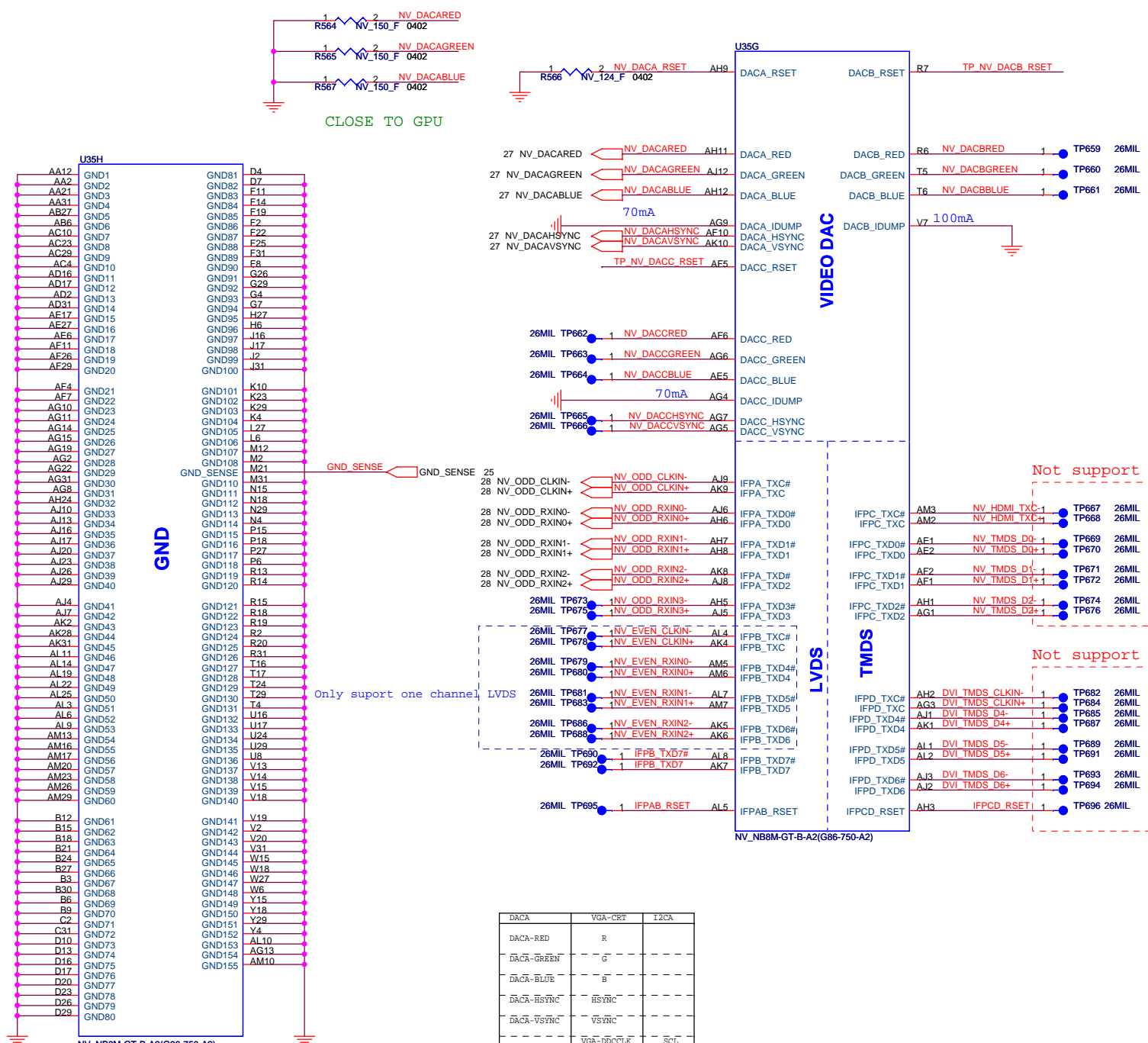
Tis chip can use MK1726 or P1819B

R560 place near GPU
R561 place near spectrum chip

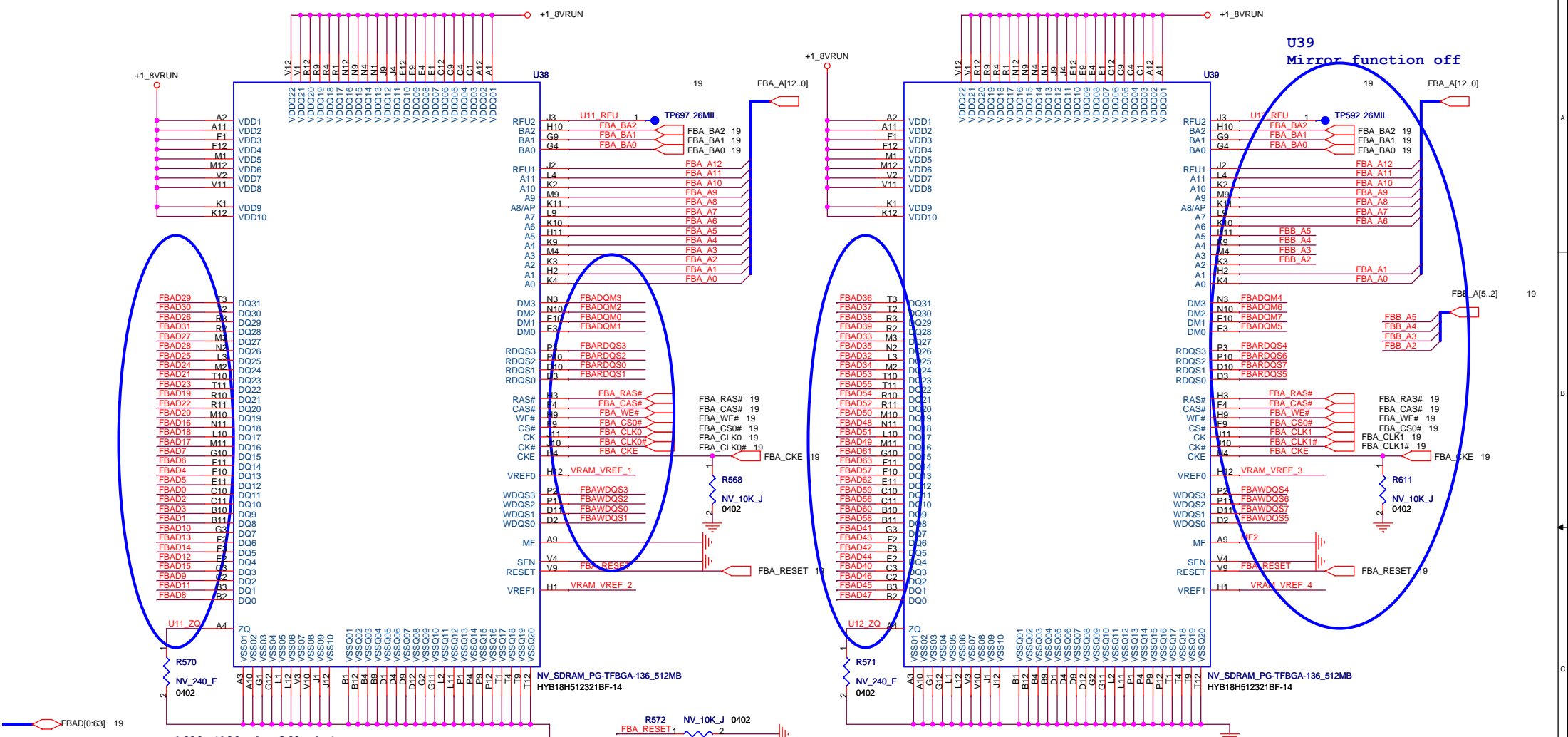
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **VGA(MULTIUSE)**

Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 20	of 67



DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SDA
	VGA-DDCDATA	SDA

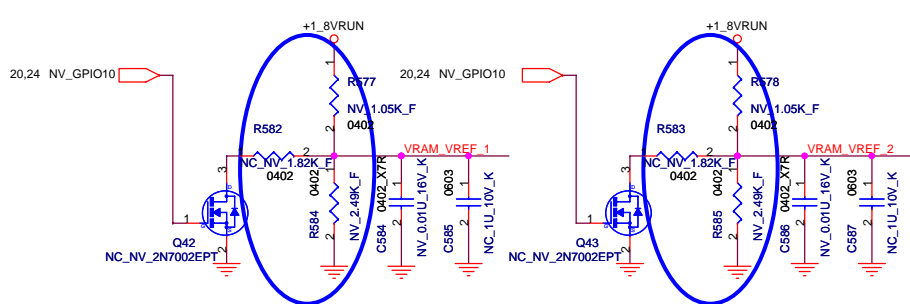


FBAD[0:63] 19
 FBADQM[7:0] 19
 FBARDQS[7:0] 19
 FBADWS[7:0] 19

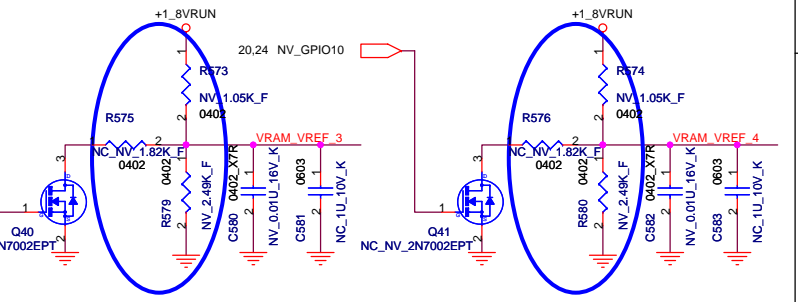
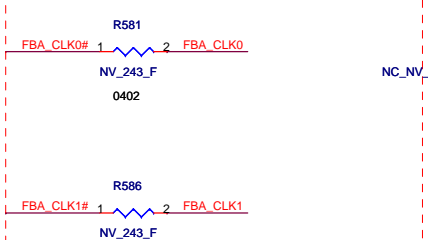
R1690 (120 ohm-360 ohm)
 240 ohm --> Output impedance 40 ohm

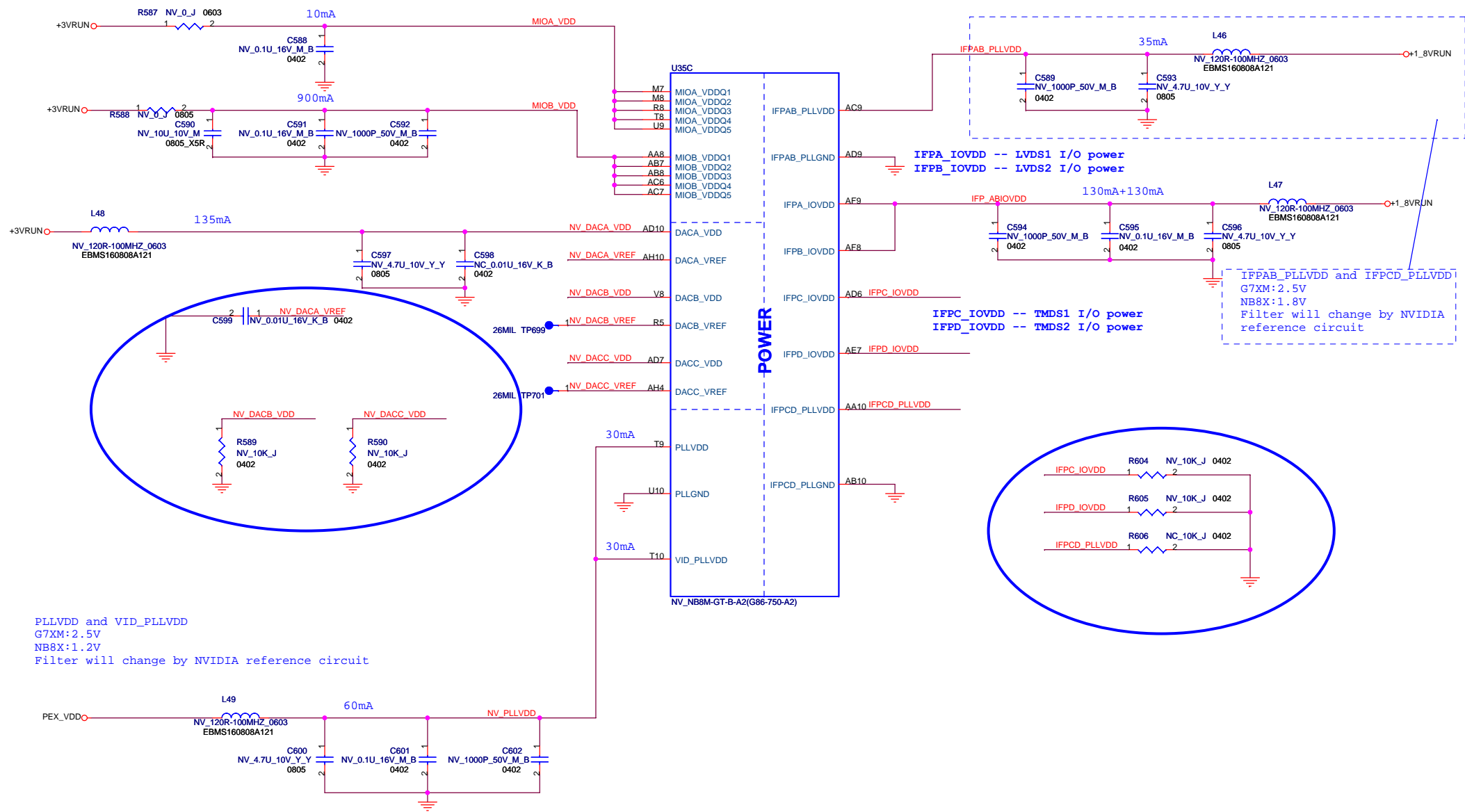
FBE: Remove termination resistor for A2,A3,A4,A5
Remove 16M/8M selection strap.

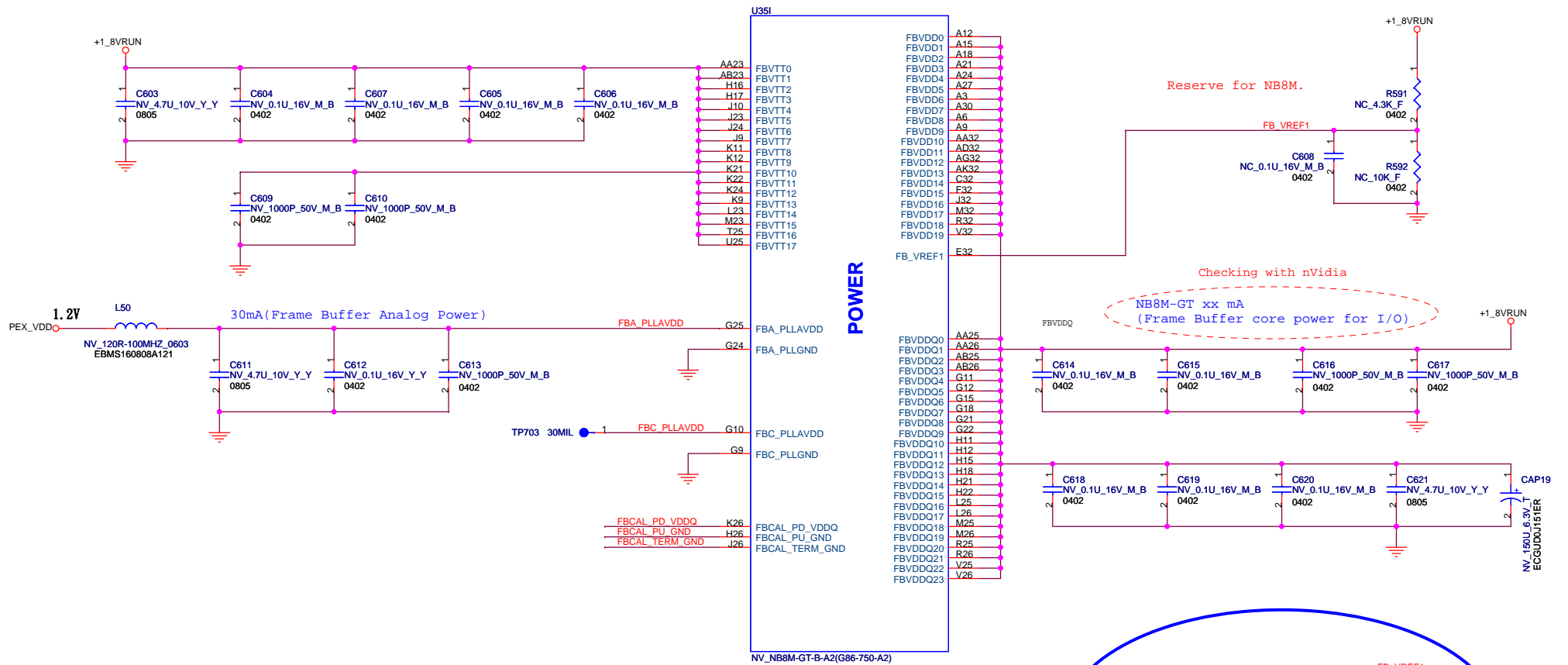
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V



7/19 FAE Suggest: Ball to termination resistor trace length < 75ps



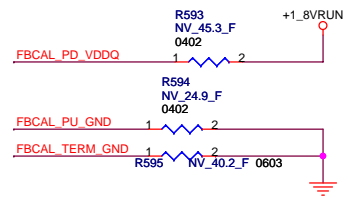




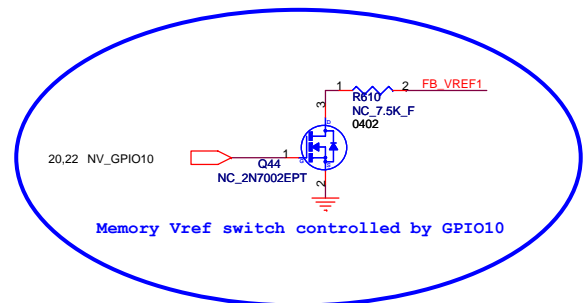
Reserve for NB8M.

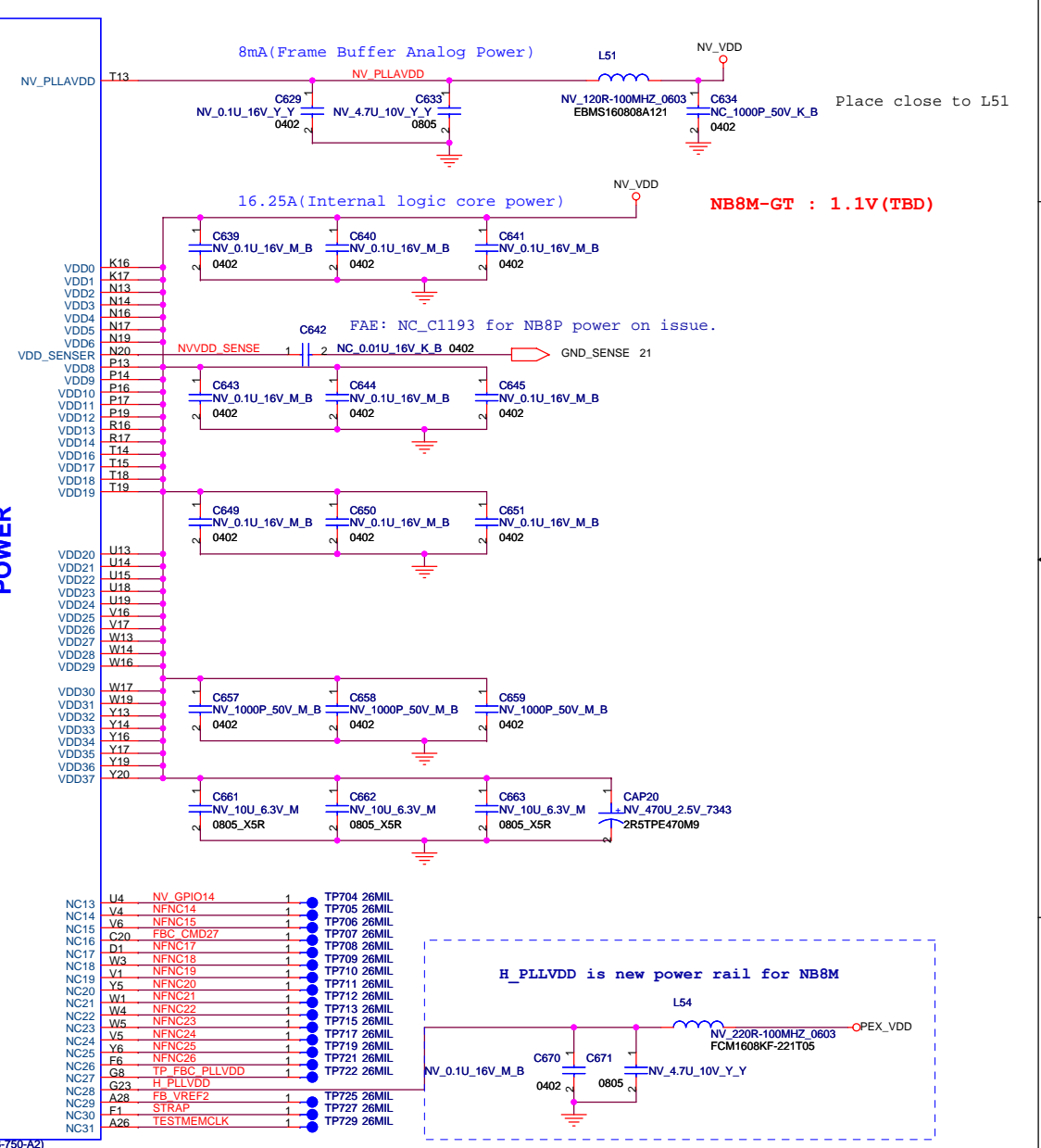
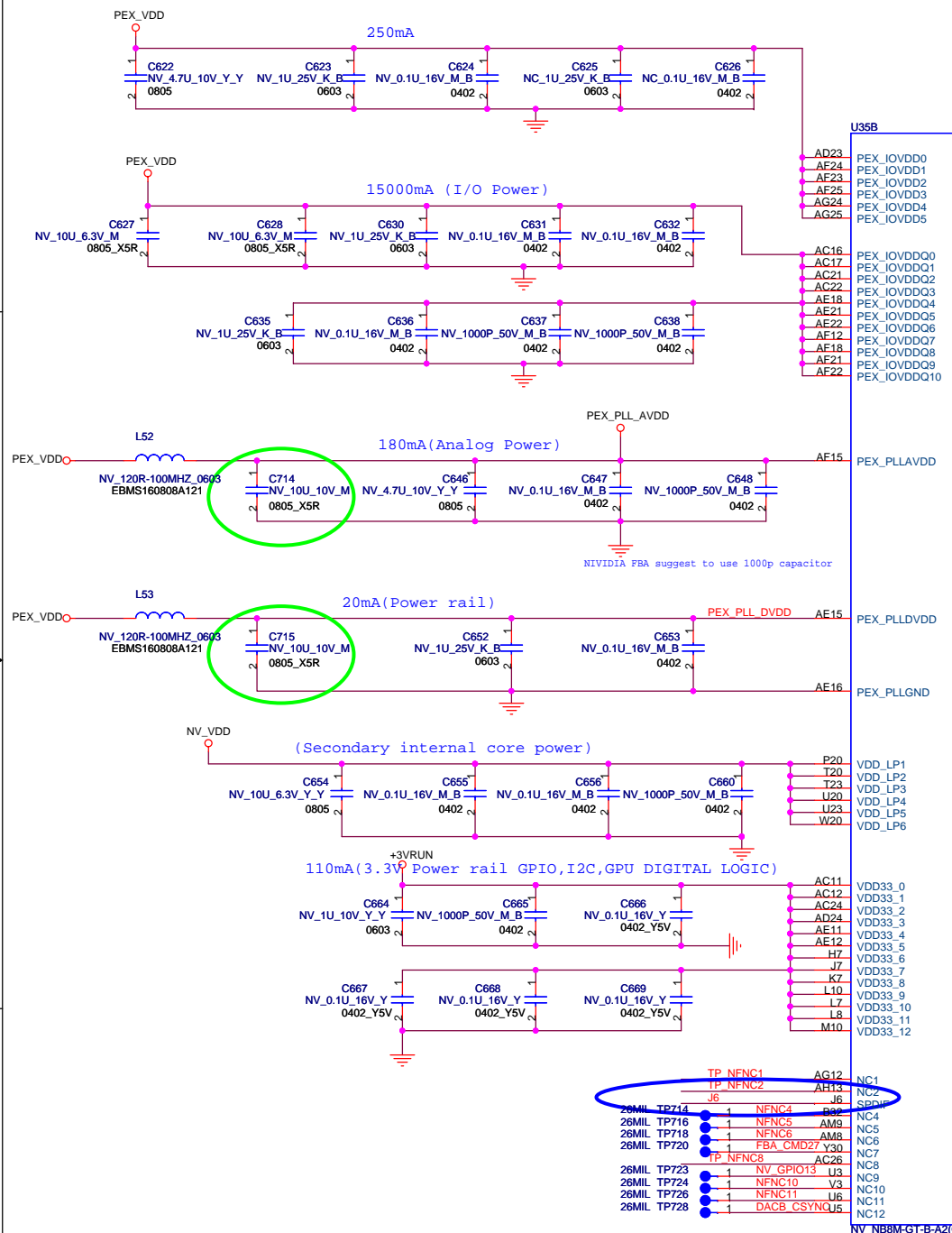
Checking with nVidia
 NB8M-GT xx mA
 (Frame Buffer core power for I/O)

FBCAL_PD_VDDQ K26
 FBCAL_PU_GND H26
 FBCAL_TERM_GND J26



	GDDR3/BGA136
FBCAL_PD_VDDQ	45.3 ohm
FBCAL_PU_GND	24.9 ohm
FBCAL_TERM_GND	40.2 ohm





U35B

AD23	PEX_IOVDD0
AF24	PEX_IOVDD1
AE23	PEX_IOVDD2
AE25	PEX_IOVDD3
AG24	PEX_IOVDD4
AG25	PEX_IOVDD5
AC16	PEX_IOVDDQ0
AC17	PEX_IOVDDQ1
AC21	PEX_IOVDDQ2
AC22	PEX_IOVDDQ3
AE18	PEX_IOVDDQ4
AE22	PEX_IOVDDQ5
AE12	PEX_IOVDDQ6
AE18	PEX_IOVDDQ7
AF21	PEX_IOVDDQ8
AF22	PEX_IOVDDQ9
	PEX_IOVDDQ10
AF15	PEX_PLLAVDD
AE15	PEX_PLLDVDD
AE16	PEX_PLLGND
P20	VDD_LP1
T20	VDD_LP2
T23	VDD_LP3
U20	VDD_LP4
U23	VDD_LP5
W20	VDD_LP6
VDD33_0	
VDD33_1	
VDD33_2	
VDD33_3	
VDD33_4	
VDD33_5	
VDD33_6	
VDD33_7	
VDD33_8	
VDD33_9	
VDD33_10	
VDD33_11	
VDD33_12	
NC1	
AH13	
NC2	
SPDIP	
J6	
NC4	
NC5	
NC6	
NC7	
NC8	
NC9	
NC10	
NC11	
NC12	

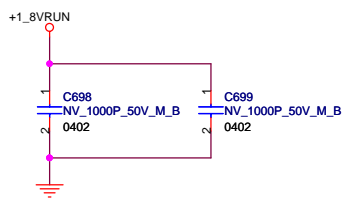
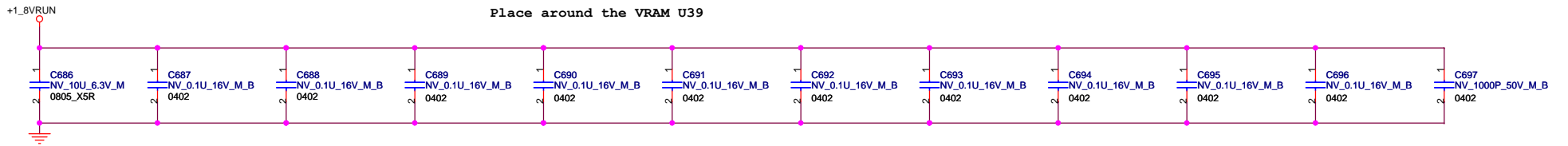
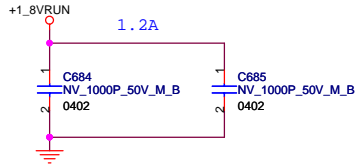
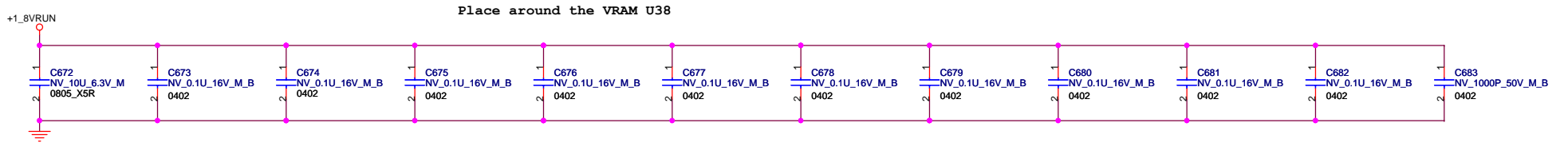
POWER

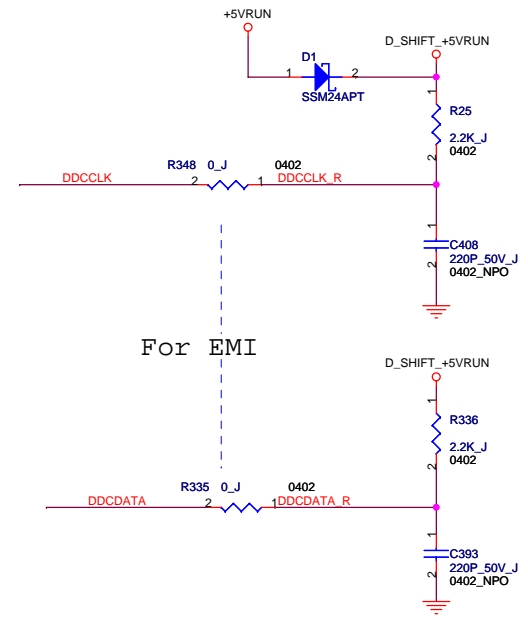
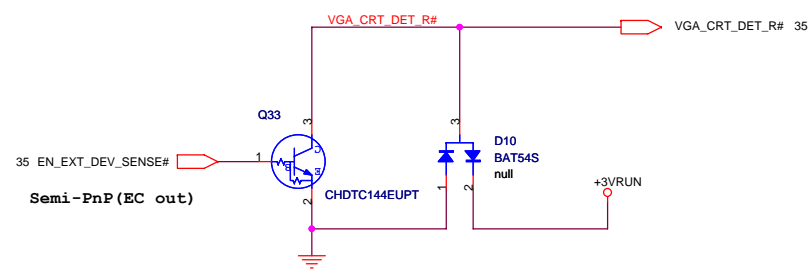
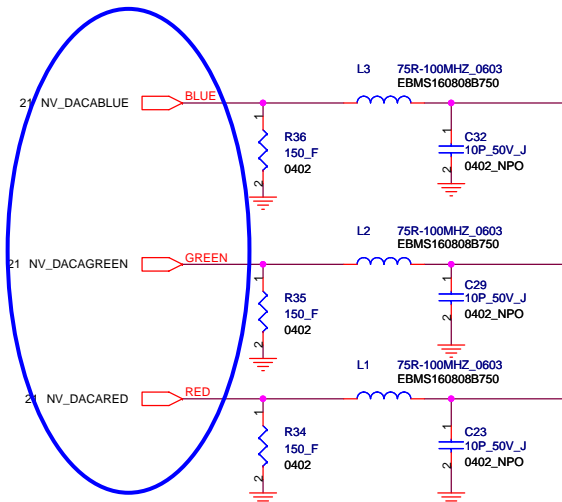
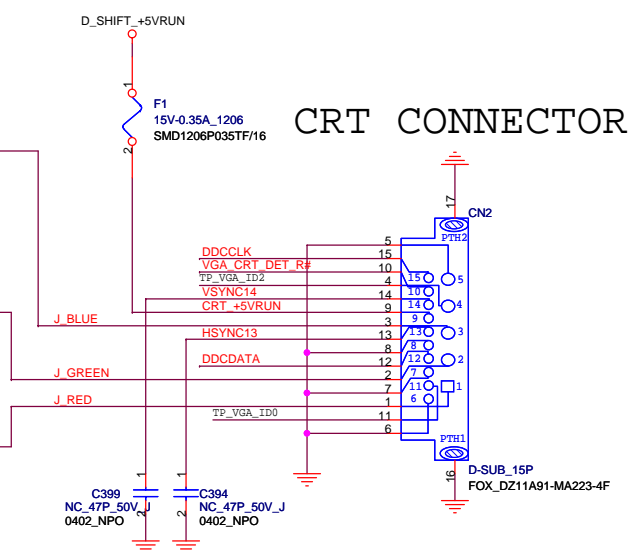
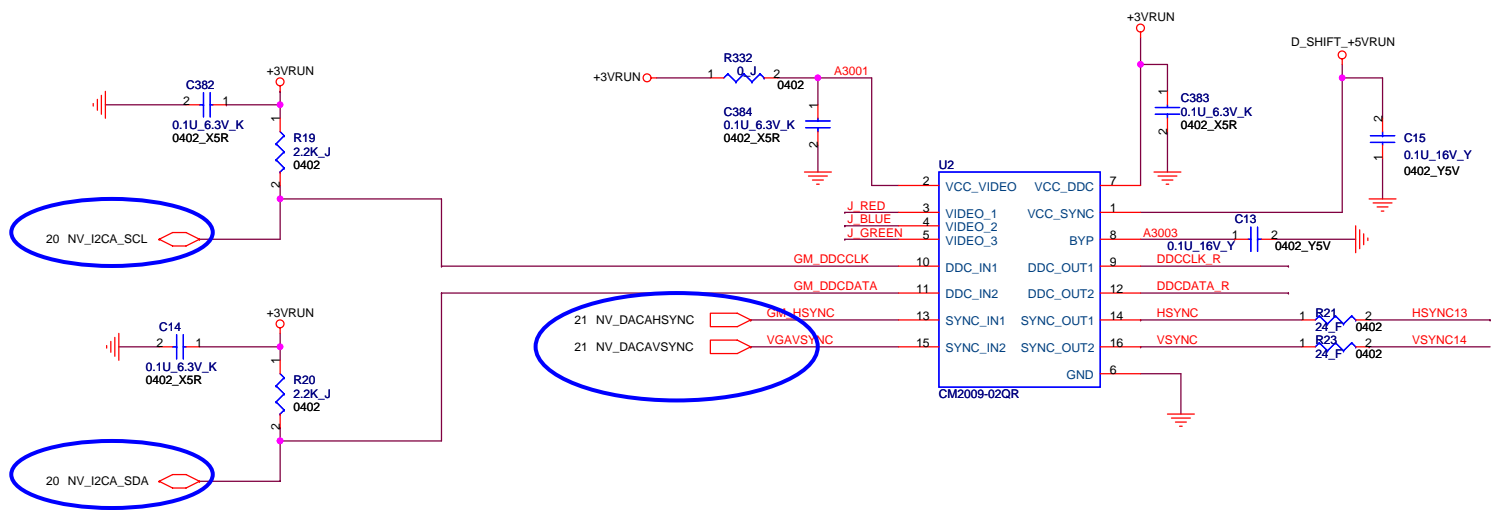
TP NFNC1

TP NFNC2	AG12	NC1
J6	AH13	NC2
26MIL TP714	NC4	TP704 26MIL
26MIL TP716	NC5	TP705 26MIL
26MIL TP718	NC6	TP706 26MIL
26MIL TP720	NC7	TP707 26MIL
26MIL TP723	NC8	TP708 26MIL
26MIL TP724	NC9	TP709 26MIL
26MIL TP726	NC10	TP710 26MIL
26MIL TP728	NC11	TP711 26MIL
	NC12	TP712 26MIL

NB8X update

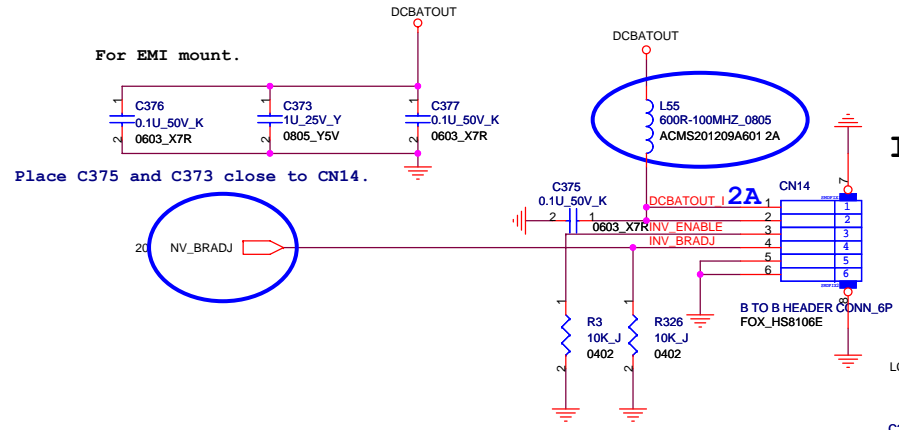
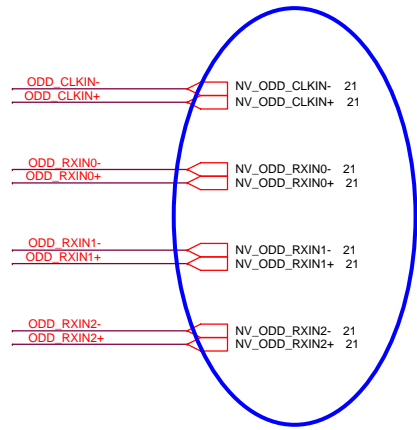
- FBA_CMD27/ FBC_CMD27: Additional memory address bit to support dual rank 8 bank memory configuration.
- DACB_CSYNQ: Composite sync for SCART support
- NV_GPIO14: Additional GPIO



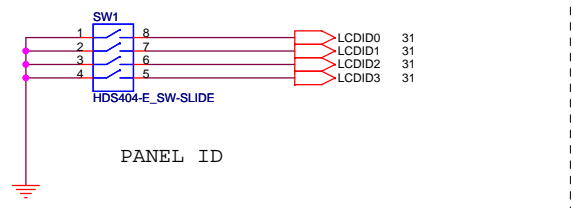
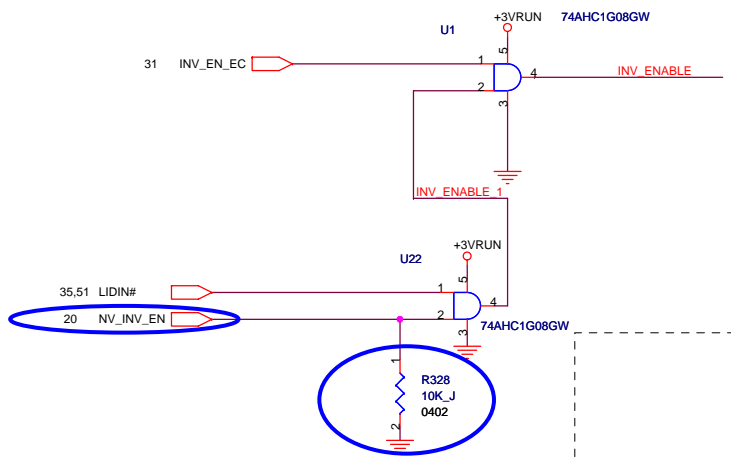
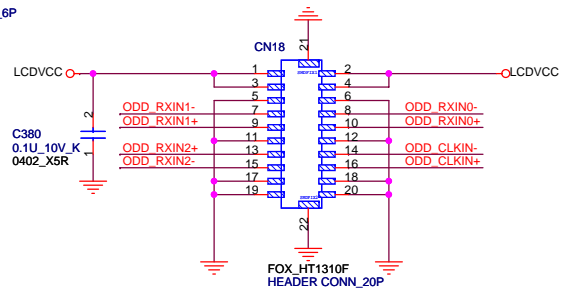


CRT CONNECTOR

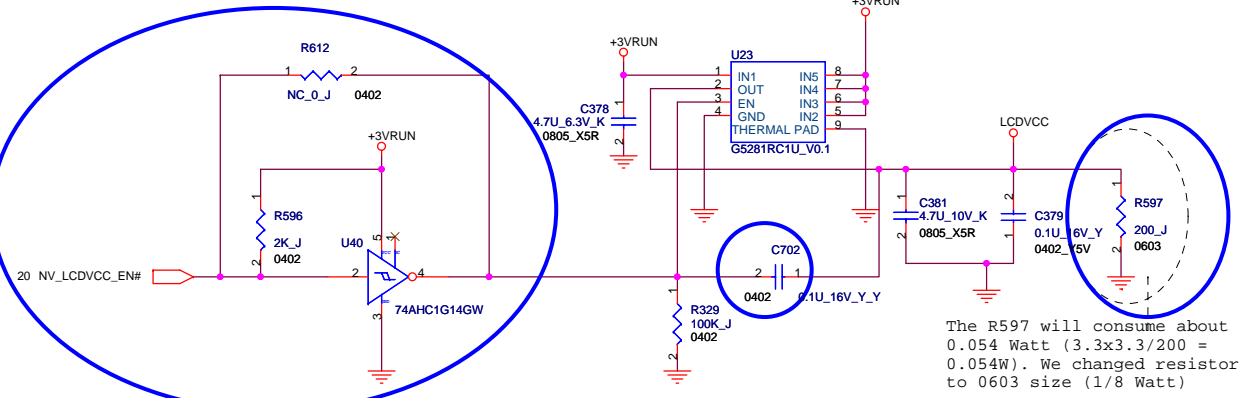
LVDS



INVERTER CONN.



Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vendor	AUO	CPT	LPL	AUO
Device Name	B154EW02V7	CLAA154WB05AN	LP154WX4-TLC5	QD15TL0703
Panel ID Check[3.0]	0001	0010	0011	0100



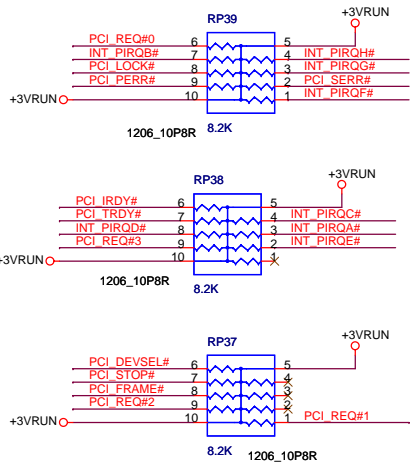
The R597 will consume about 0.054 Watt ($3.3 \times 3.3 / 200 = 0.054W$). We changed resistor to 0603 size (1/8 Watt)

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CCPBG - R&D Division

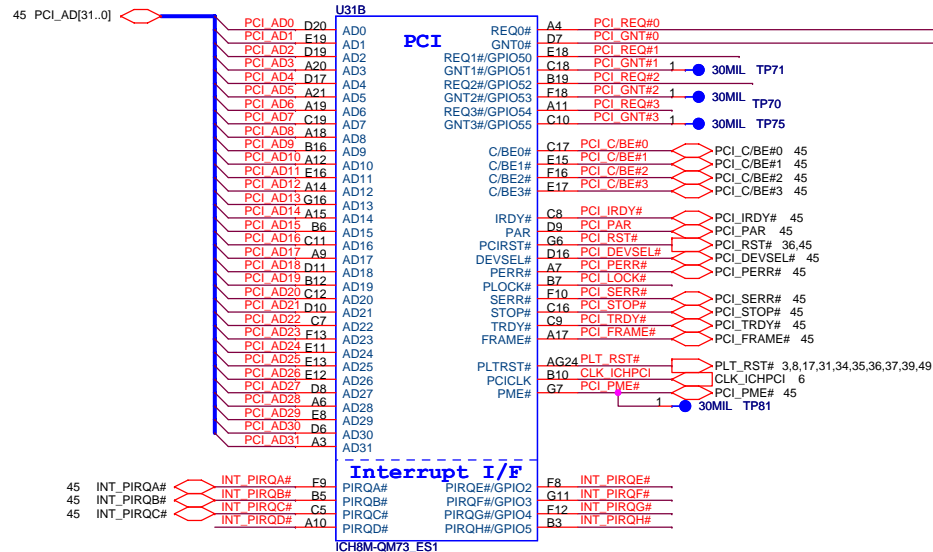
Title **LVDS**

Size A3	Document Number M730-1-01	Rev 1.0
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Date: Saturday, October 13, 2007 Sheet 28 of 67



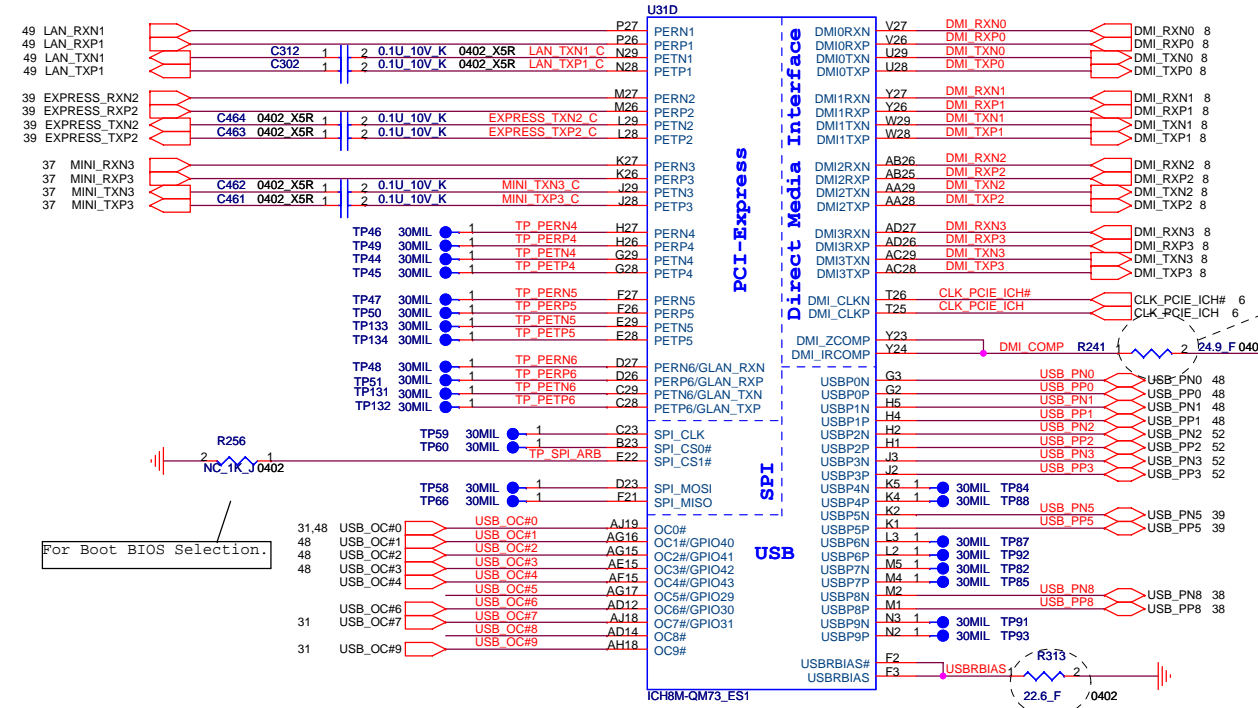
PCI Pullups



For Boot BIOS Selection.

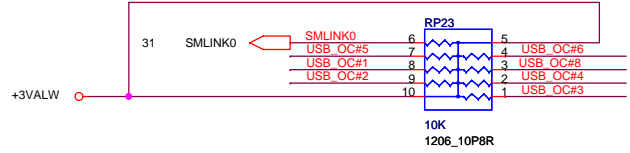
Strap for Boot-BIOS

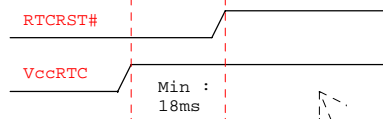
	GNT#	SPI_CS1#
LPC(Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI



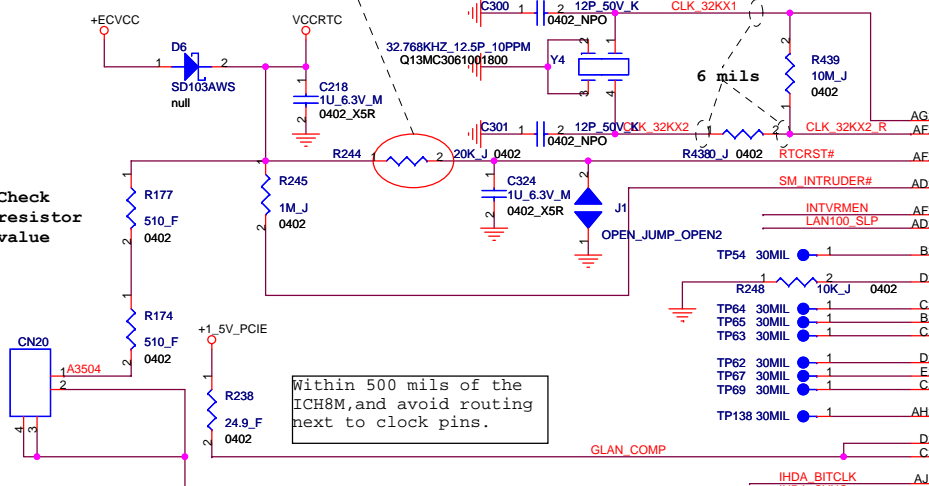
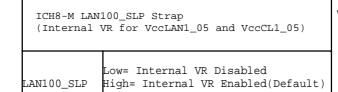
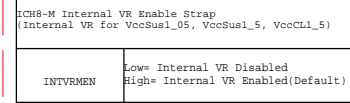
Place within 500 mils of ICH

Place within 500 mils of ICH and don't routing next to high speed signals





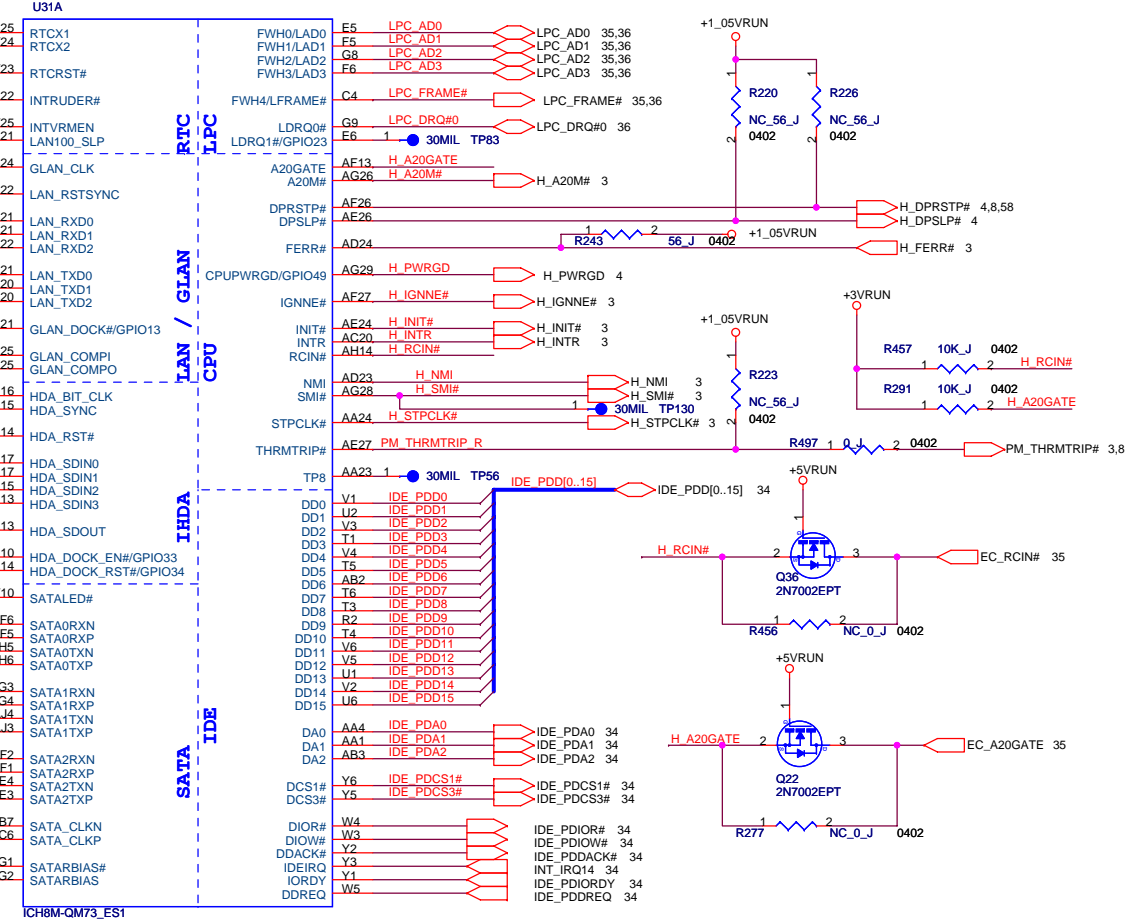
The traces inside this block should be wider. No digital signals routed under XTAL



Check resistor value

Within 500 mils of the ICH8M, and avoid routing next to clock pins.

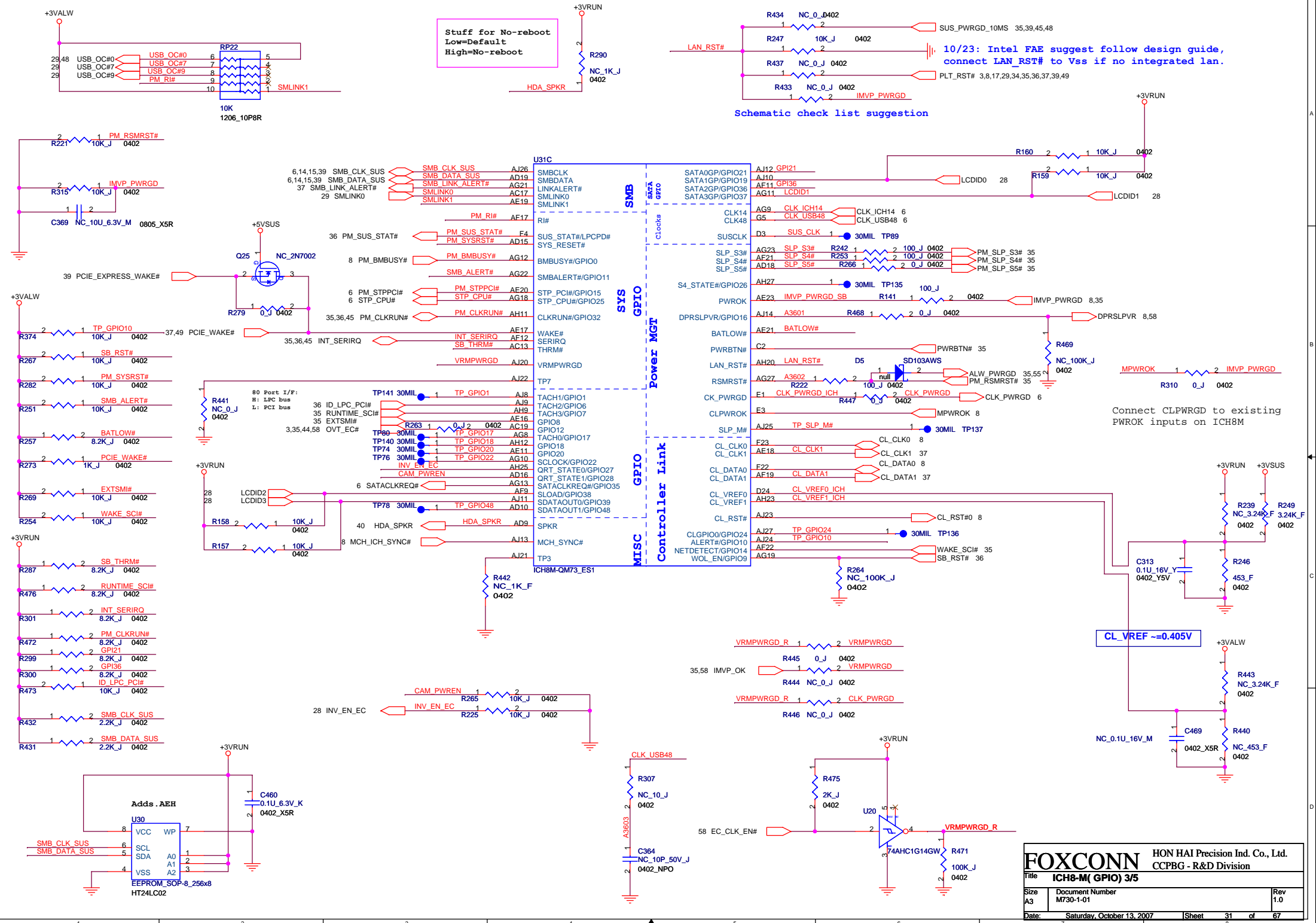
Within 500 mils of the ICH8M, and avoid routing next to clock pins.



Stuff for No-reboot
Low=Default
High=No-reboot

10/23: Intel FAE suggest follow design guide,
connect LAN_RST# to Vss if no integrated lan.

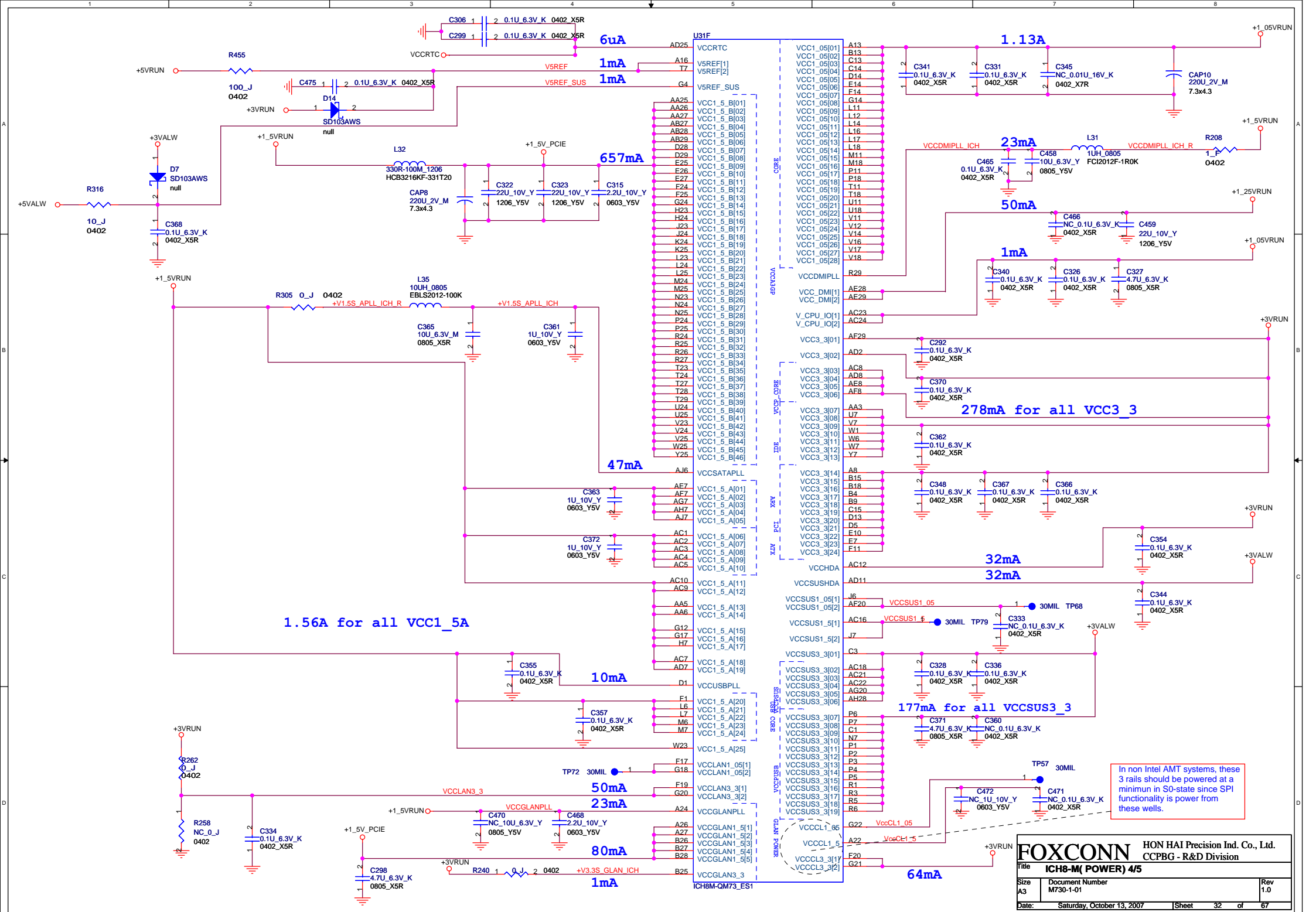
Schematic check list suggestion



Connect CLPWRGD to existing
PWROK inputs on ICH8M

CL_VREF ~0.405V

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title ICH8-M (GPIO) 3/5		
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 31	of 67



1.56A for all VCC1_5A

47mA

10mA

50mA

23mA

80mA

1mA

1.13A

23mA

50mA

1mA

278mA for all VCC3_3

32mA

32mA

177mA for all VCCSUS3_3

64mA

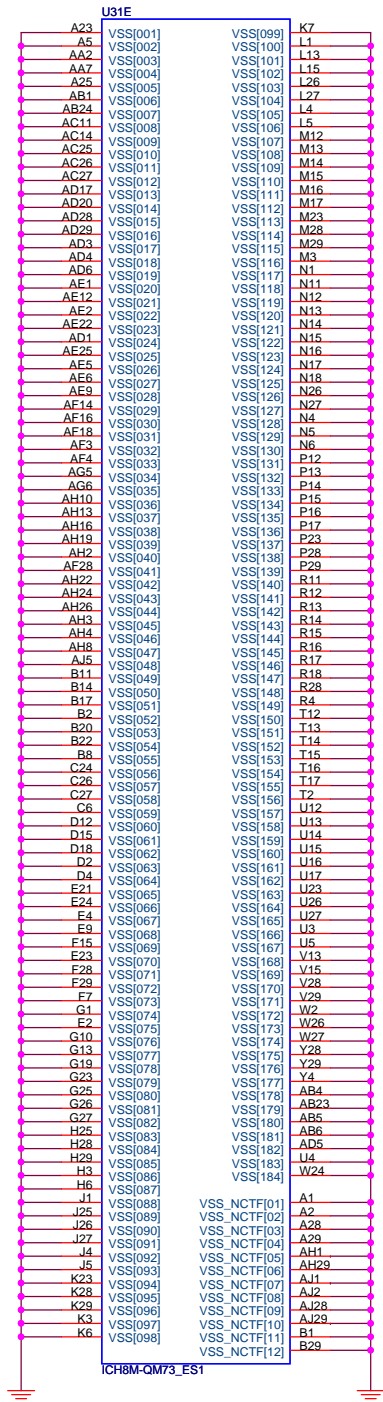
In non Intel AMT systems, these 3 rails should be powered at a minimum in S0-state since SPI functionality is power from these wells.

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

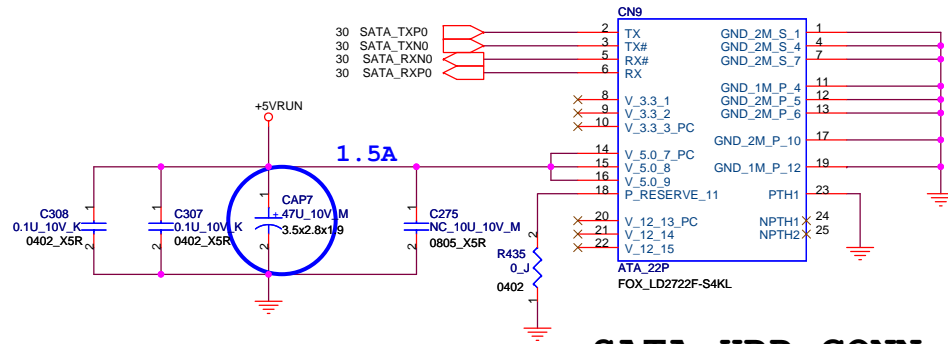
Title: **ICH8-M(POWER) 4/5**

Size A3	Document Number M730-1-01	Rev 1.0
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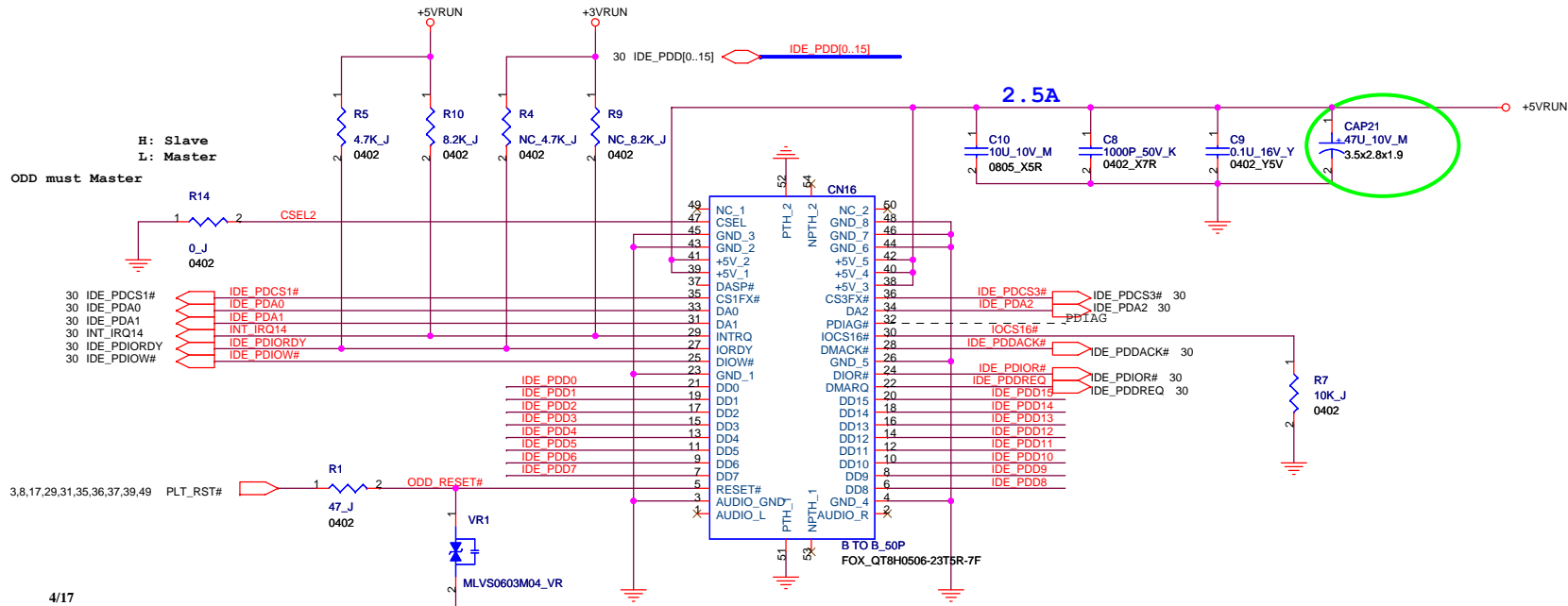
Date: Saturday, October 13, 2007 Sheet 32 of 67



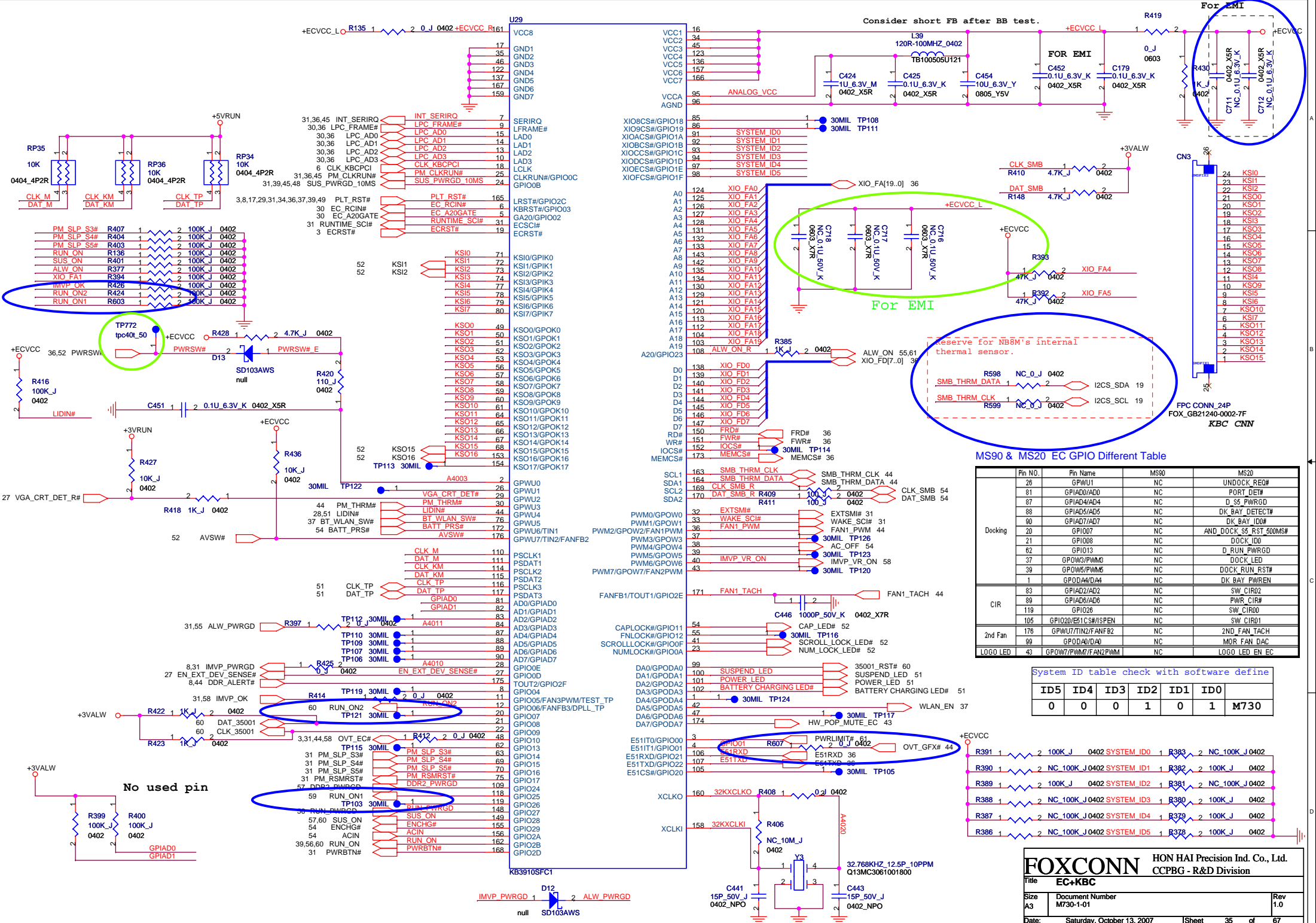
FOXCONN		HON HAI Precision Ind. Co., Ltd.
Title ICH8-M(GND) 5/5		CCPBG - R&D Division
Size A3	Document Number M730-1-01	Rev 1.0
Date: Saturday, October 13, 2007	Sheet 33	of 67



SATA HDD CONN



CD-ROM CONN



MS90 & MS20 EC GPIO Different Table

	Pin NO.	Pin Name	MS90	MS20
Docking	26	GPWU1	NC	UNDOCK_REQ#
	81	GP1AD0/AD0	NC	PORT_DET#
	87	GP1AD4/AD4	NC	D_35 PWRGD
	88	GP1AD5/AD5	NC	DK_BAY_DETECT#
	90	GP1AD7/AD7	NC	DK_BAY_ID#
	20	GPIO07	NC	AND_DOCK_S5_RST_600MS#
	21	GPIO08	NC	DOCK_ID0
	62	GPIO13	NC	D_RUN_PWRGD
	37	GP0W3/PW0M3	NC	DOCK_LED
	39	GP0W5/PW0M5	NC	DOCK_RUN_RST#
CIR	83	GP1AD2/AD2	NC	SW_CIR0
	89	GP1AD6/AD6	NC	PWR_CIR#
	119	GPIO26	NC	SW_CIR00
2nd Fan	105	GPIO20/EXTCS#/ISPEN	NC	SW_CIR01
	1	GP0D4/AD4	NC	DK_BAY_PWREN
LOGO LED	43	GP0W7/PW0M7/FAN2PWM	NC	LOGO_LED_EN_EC

System ID table check with software define

ID5	ID4	ID3	ID2	ID1	ID0	
0	0	0	1	0	1	M730

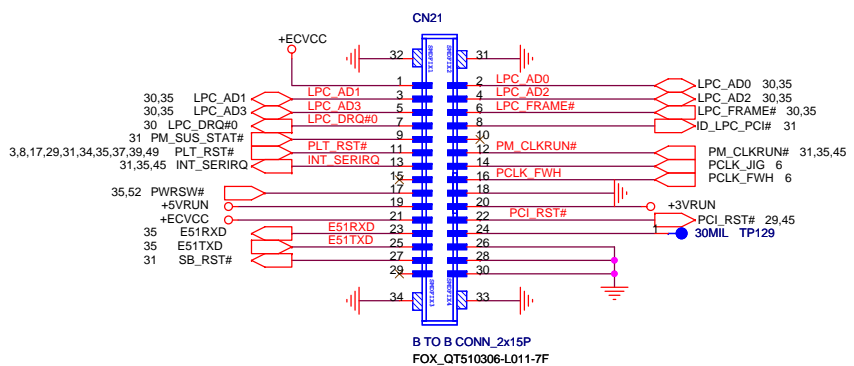
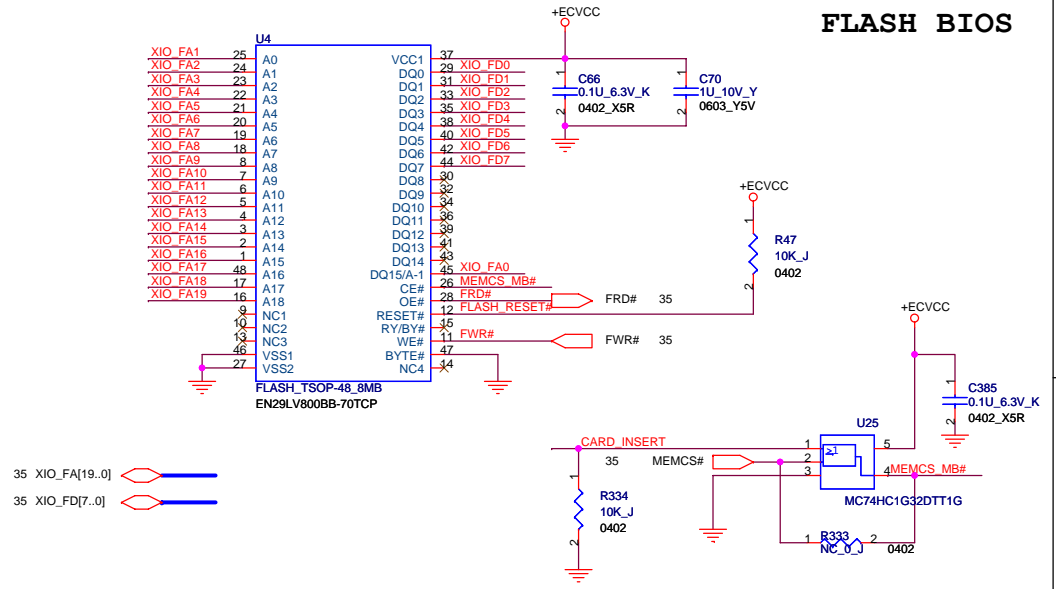
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **EC+KBC**

Size A3	Document Number M730-1-01	Rev 1.0
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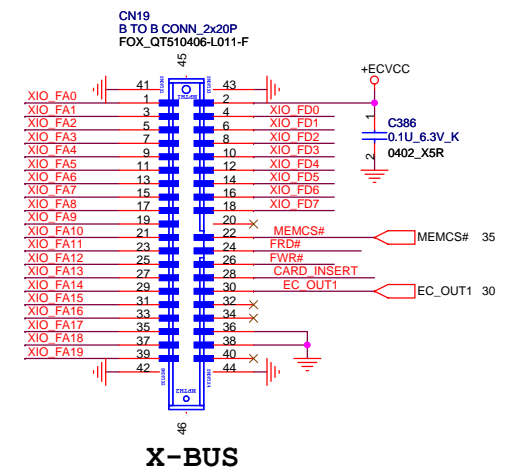
Date: Saturday, October 13, 2007 Sheet 35 of 67

FLASH BIOS

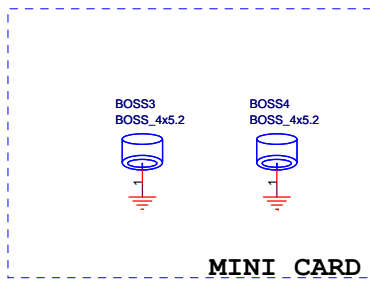


JIG-120

Pin 18 of JIG-120 is useless in debug board, so we let pin 18 NC.

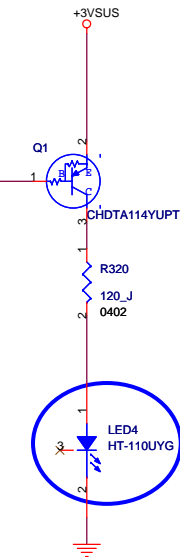
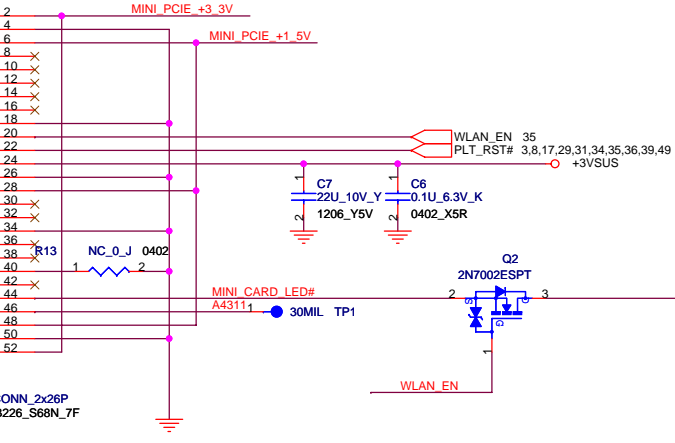
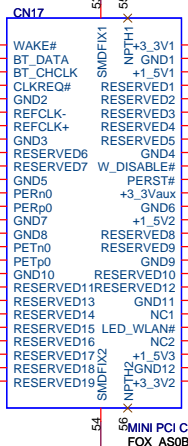
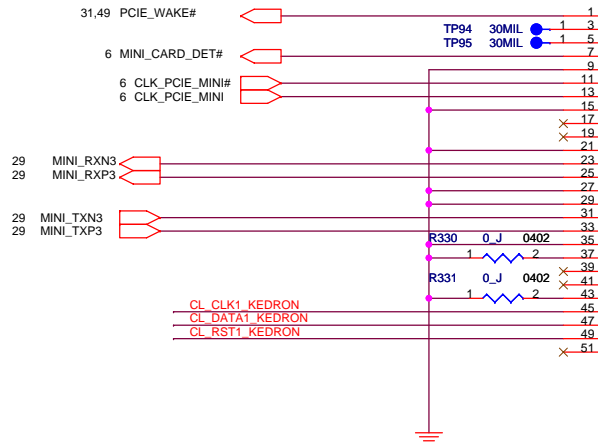
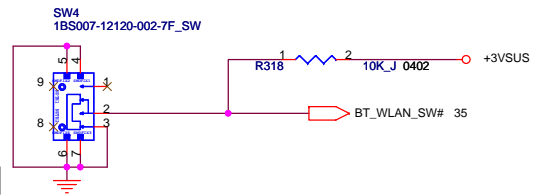


X-BUS



MINI CARD

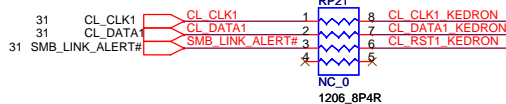
SW2 PIN8,9 : NPTH



LED IF SPEC:
20mA (TYP) , 30mA (MAX)

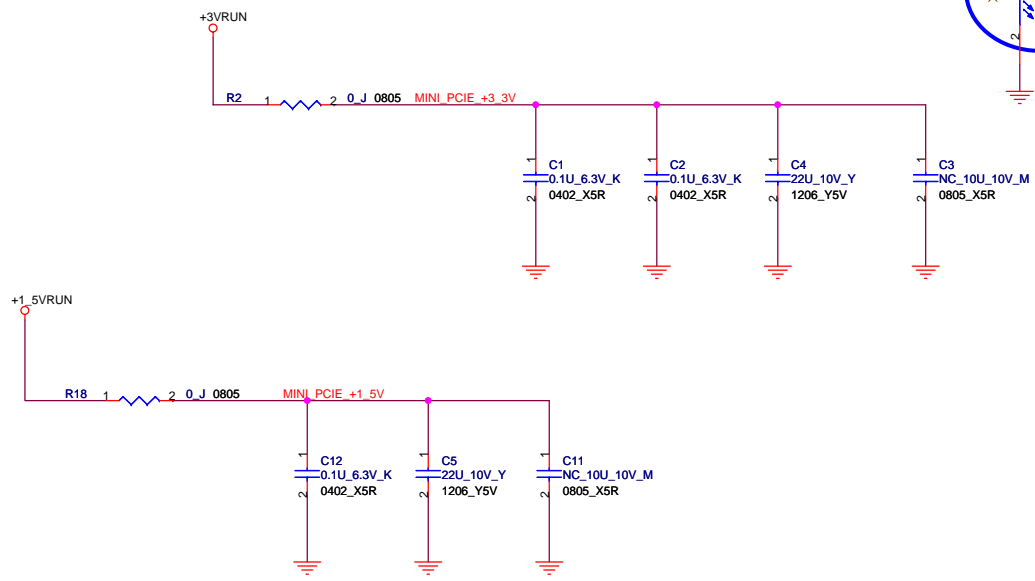
Green

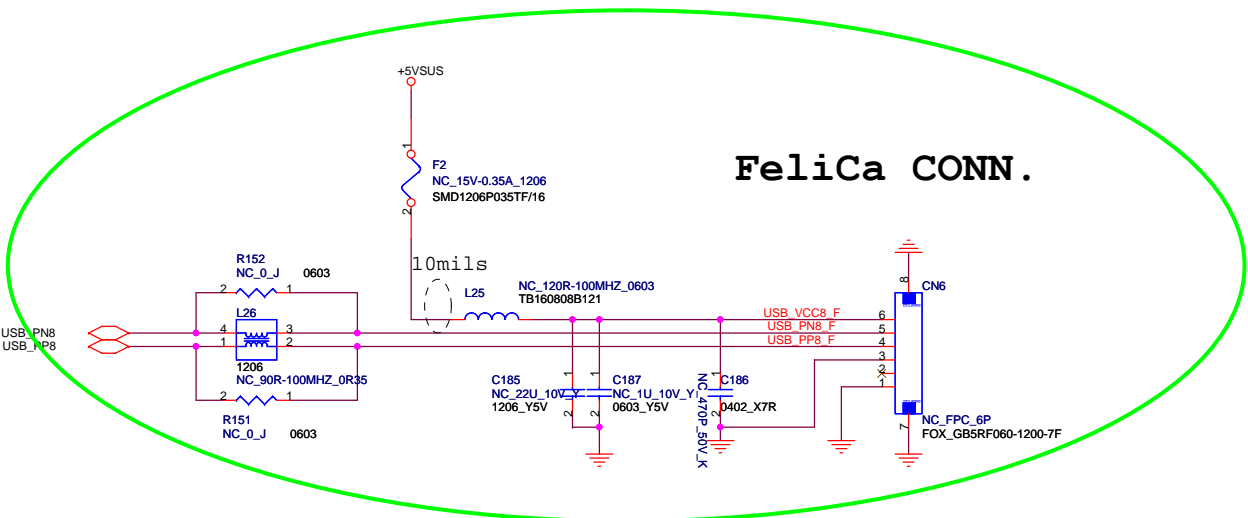
WLAN LED.



**Mini Card.
WLAN**

+1_5V=>0.5A
+3_3VAux=>0.33A
+3_3V=>1A

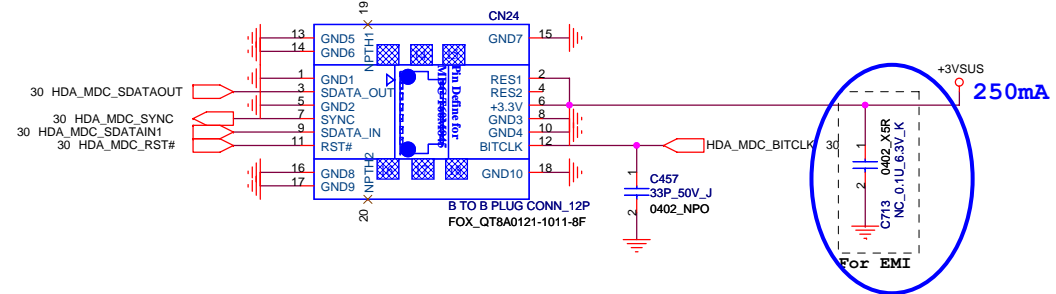


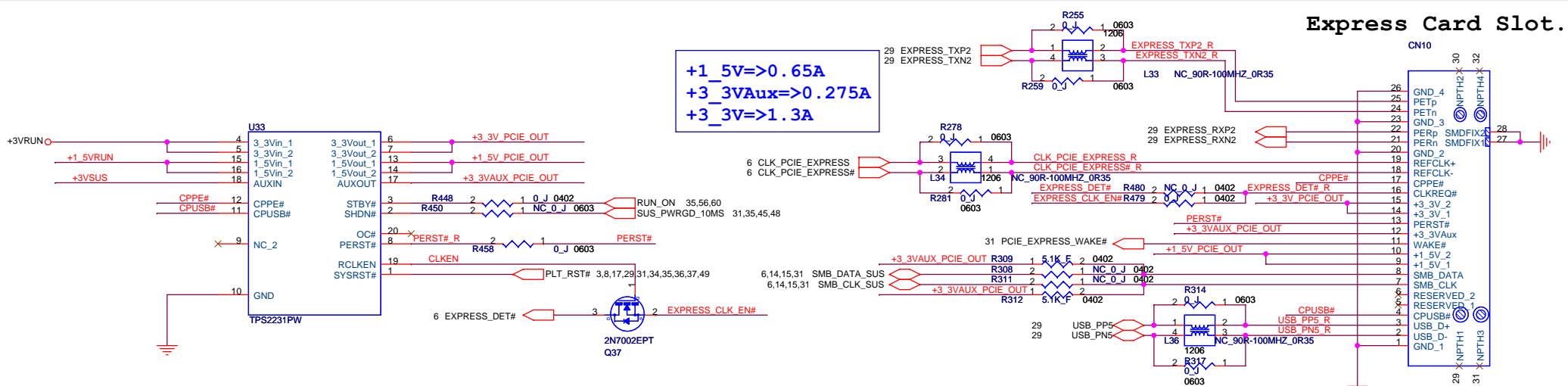


BOM Notice:

W/ FeliCa SKU	R151,R152,L25,C185,C186,F2,CN6	stuff
W/O FeliCa SKU	R151,R152,L25,C185,C186,F2,CN6	no stuff

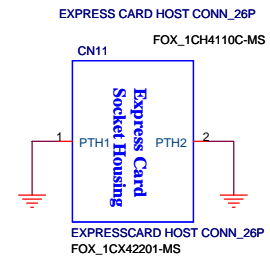
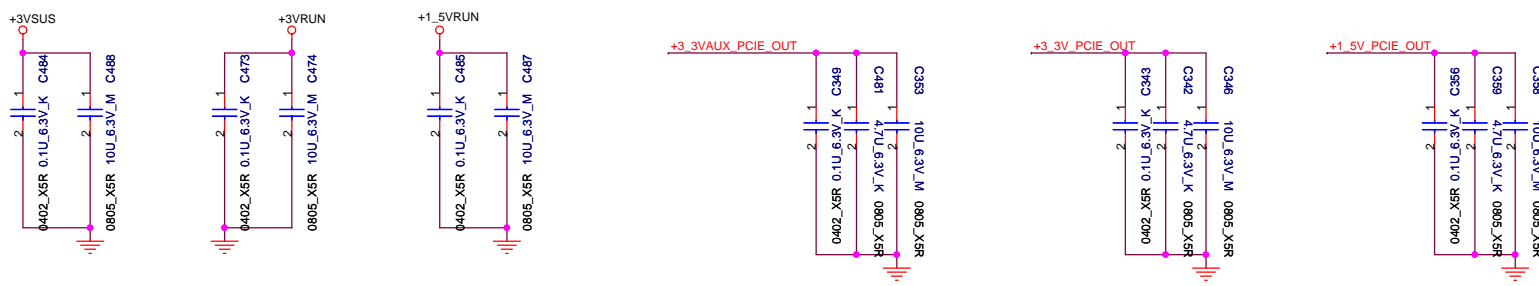
MDC CONN.



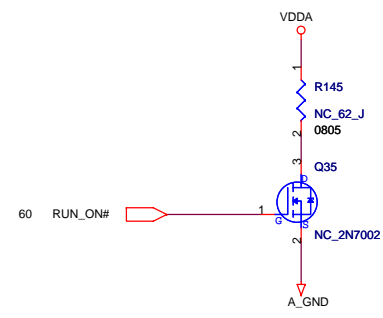
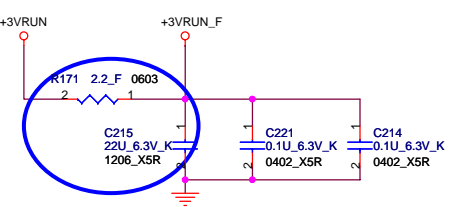
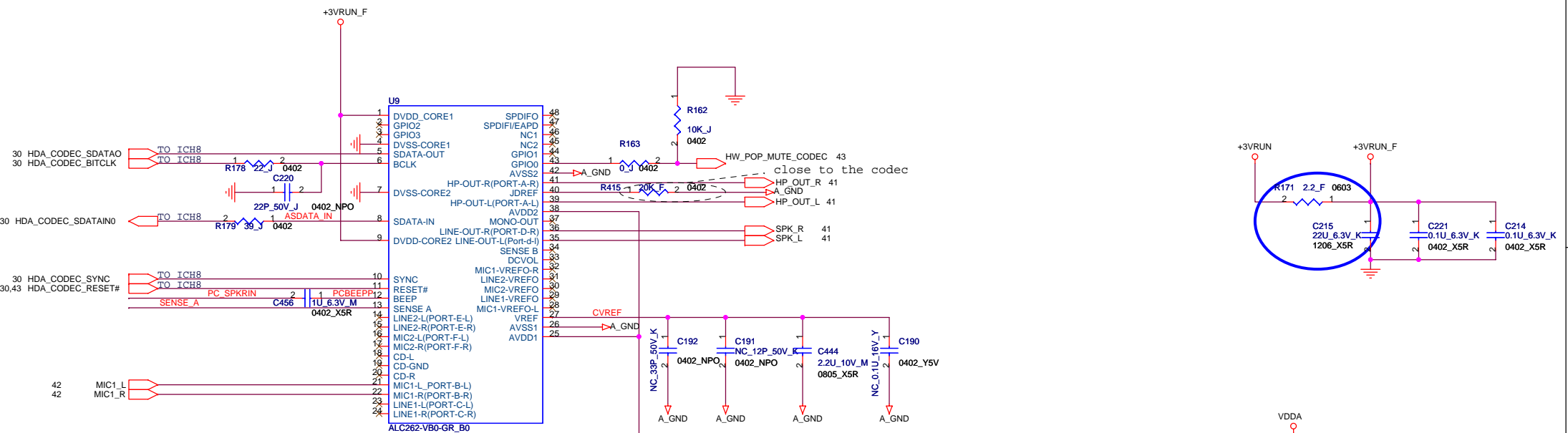


Express Card Slot.

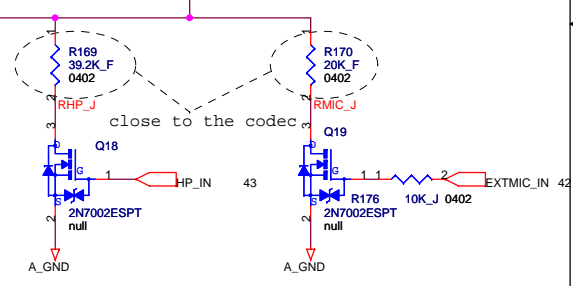
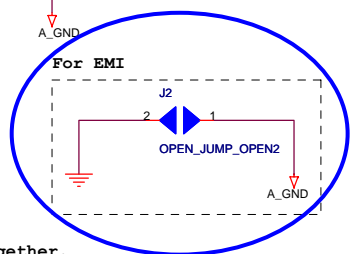
+1_5V=>0.65A
+3_3VAux=>0.275A
+3_3V=>1.3A



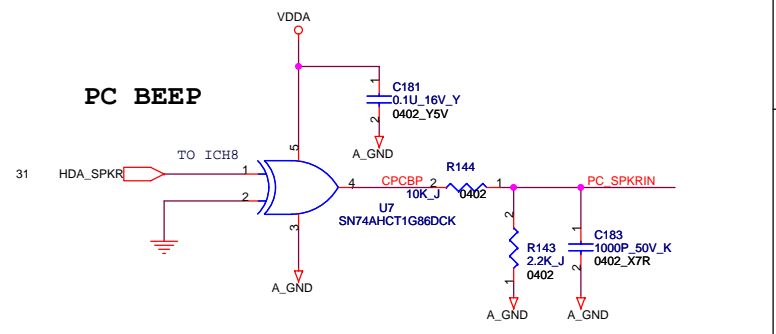
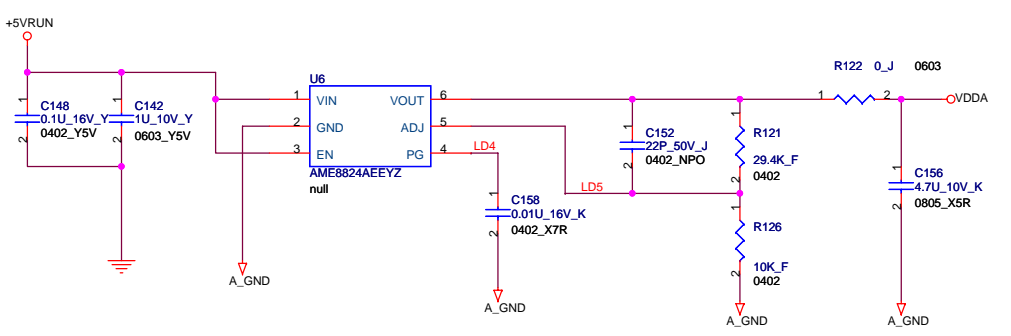
Express Card Housing.

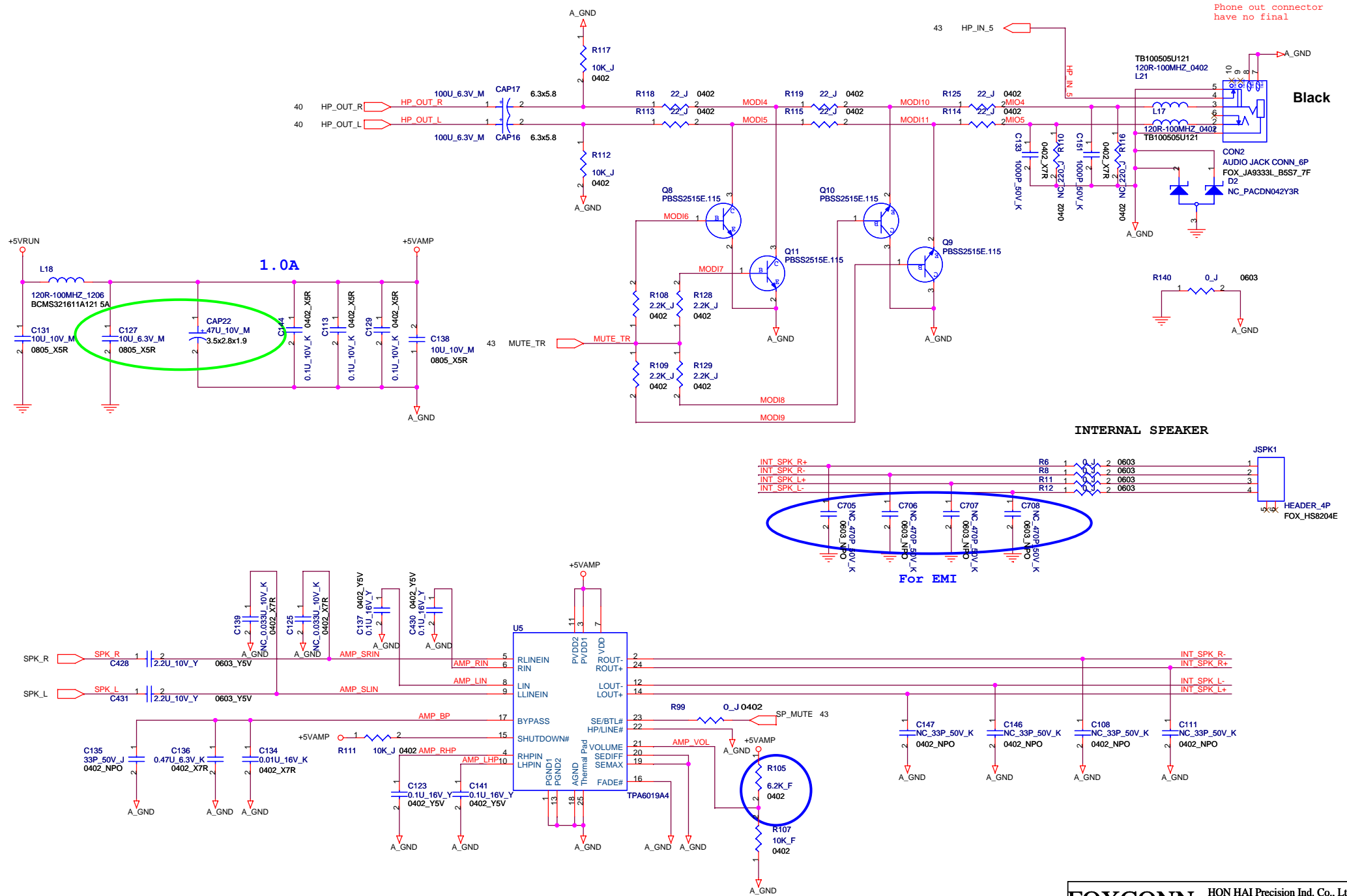


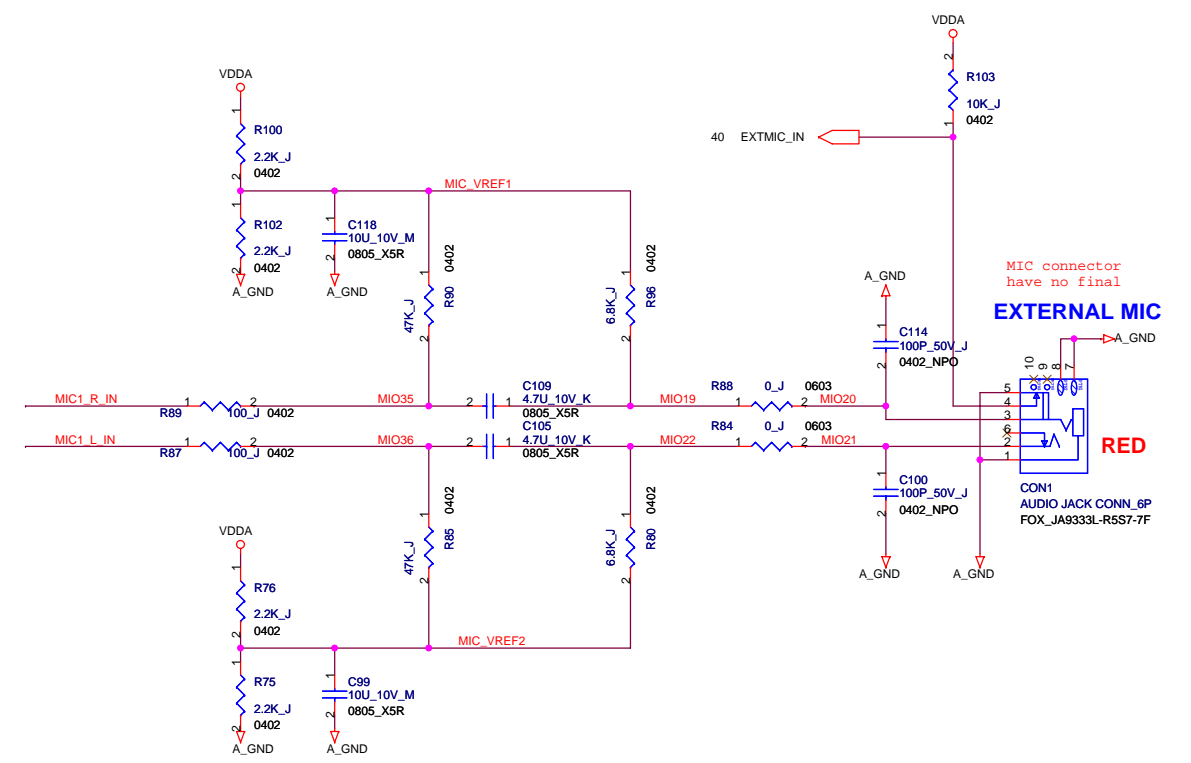
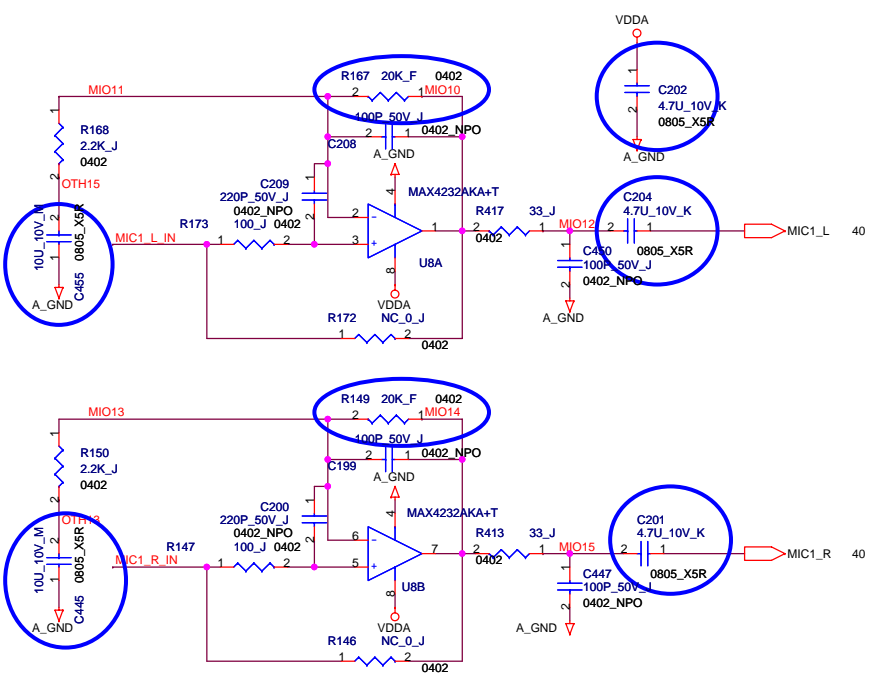
Place these two capacitor together. Place these two capacitor together.



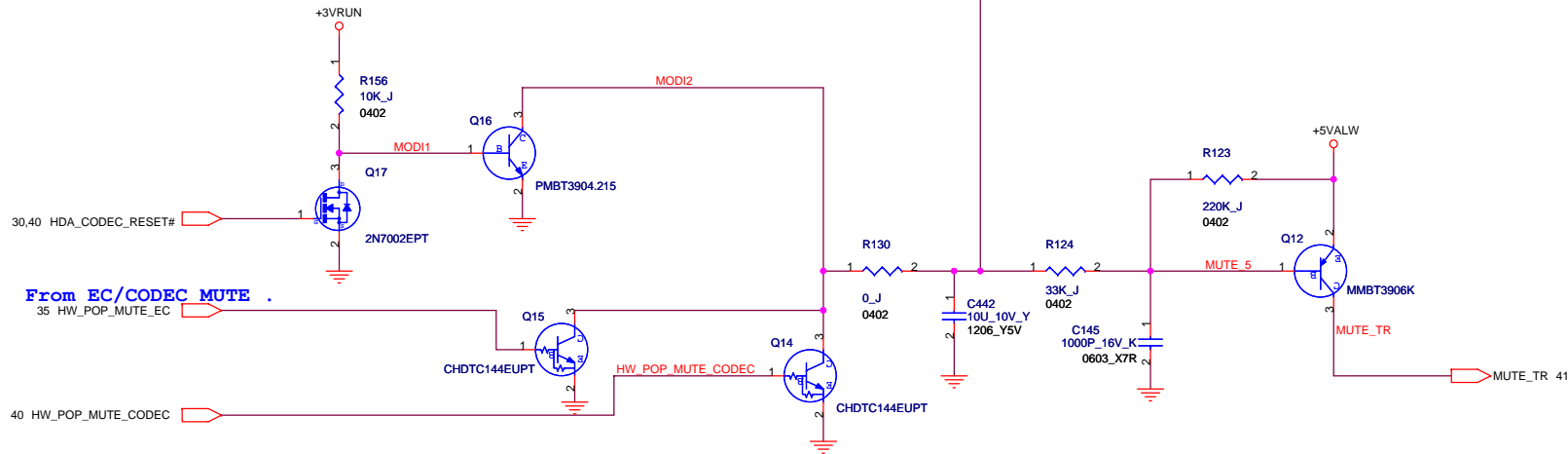
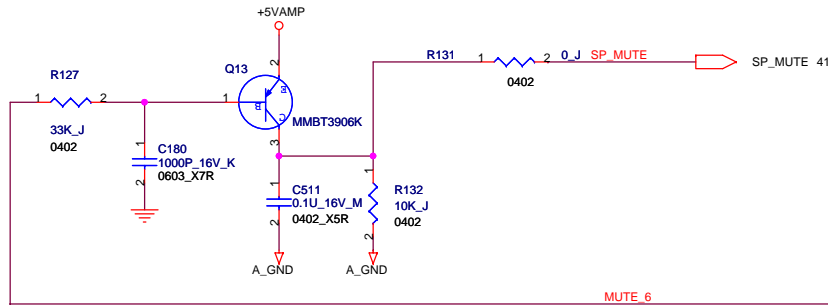
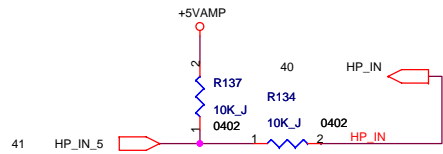
AUDIO POWER(Change to 4.75V/200mA)



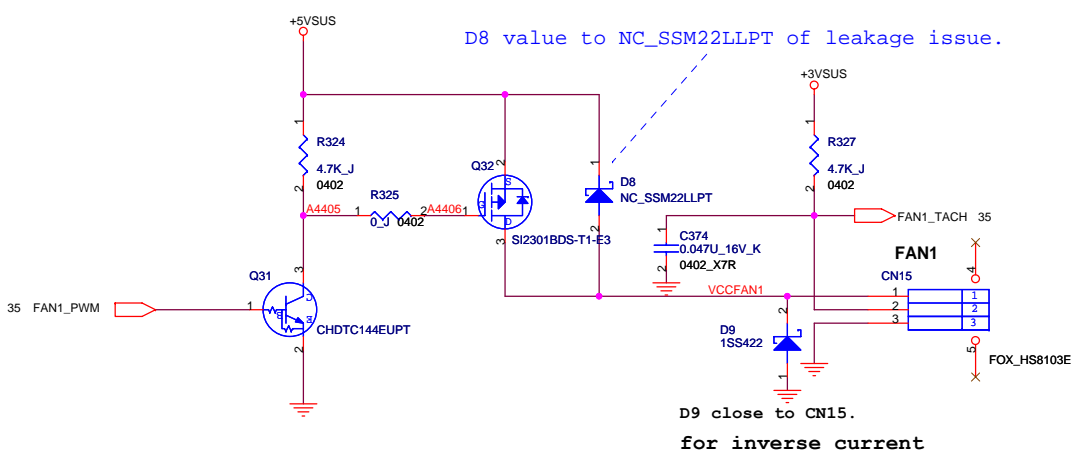




MIC connector
 have no final
EXTERNAL MIC
RED
 CON1
 AUDIO JACK CONN_6P
 FOX_JA9333L-R5S7-7F

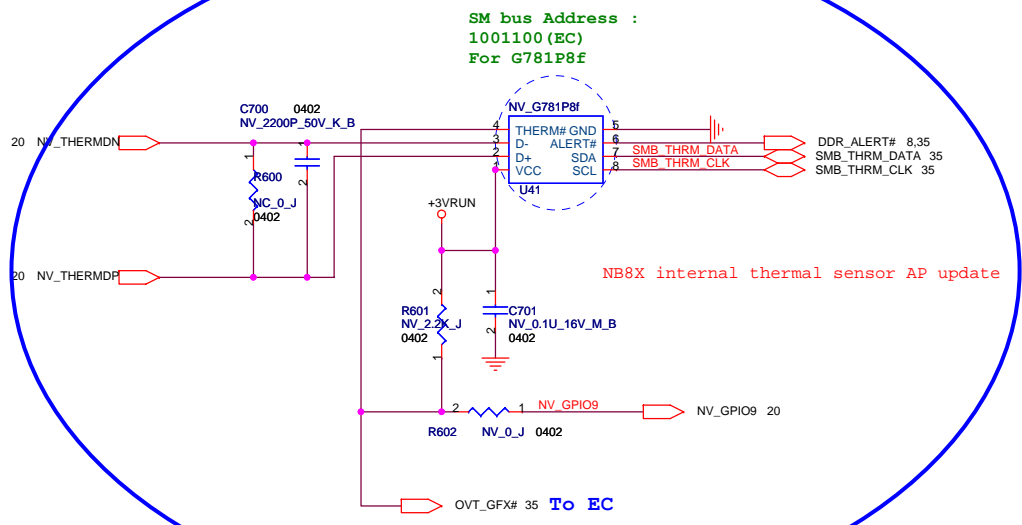


From EC/CODEC MUTE .



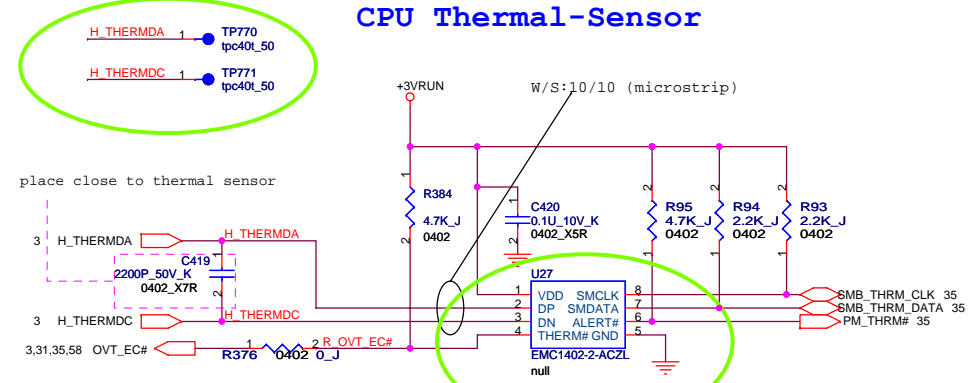
FAN

VGA Thermal-Sensor

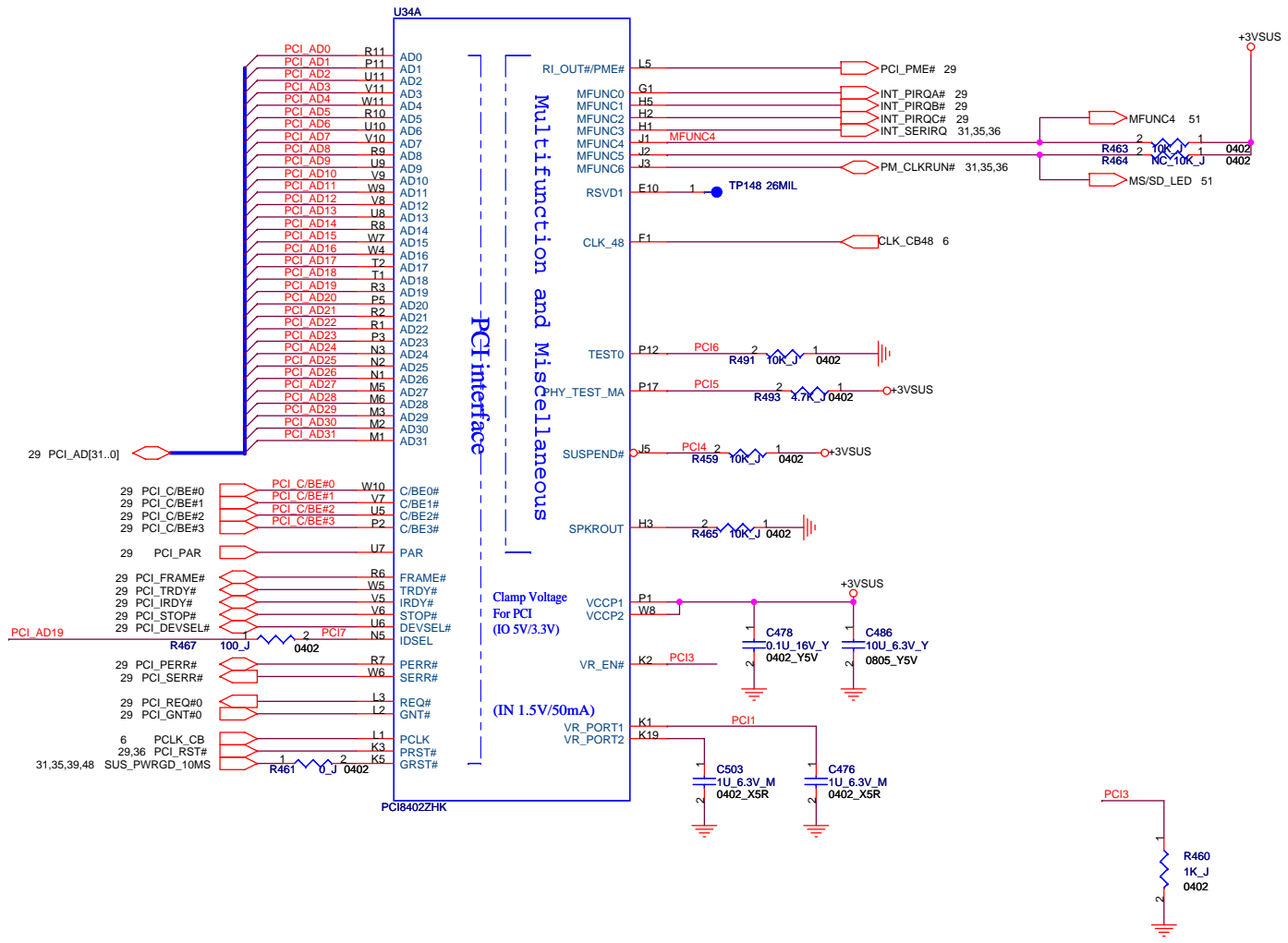


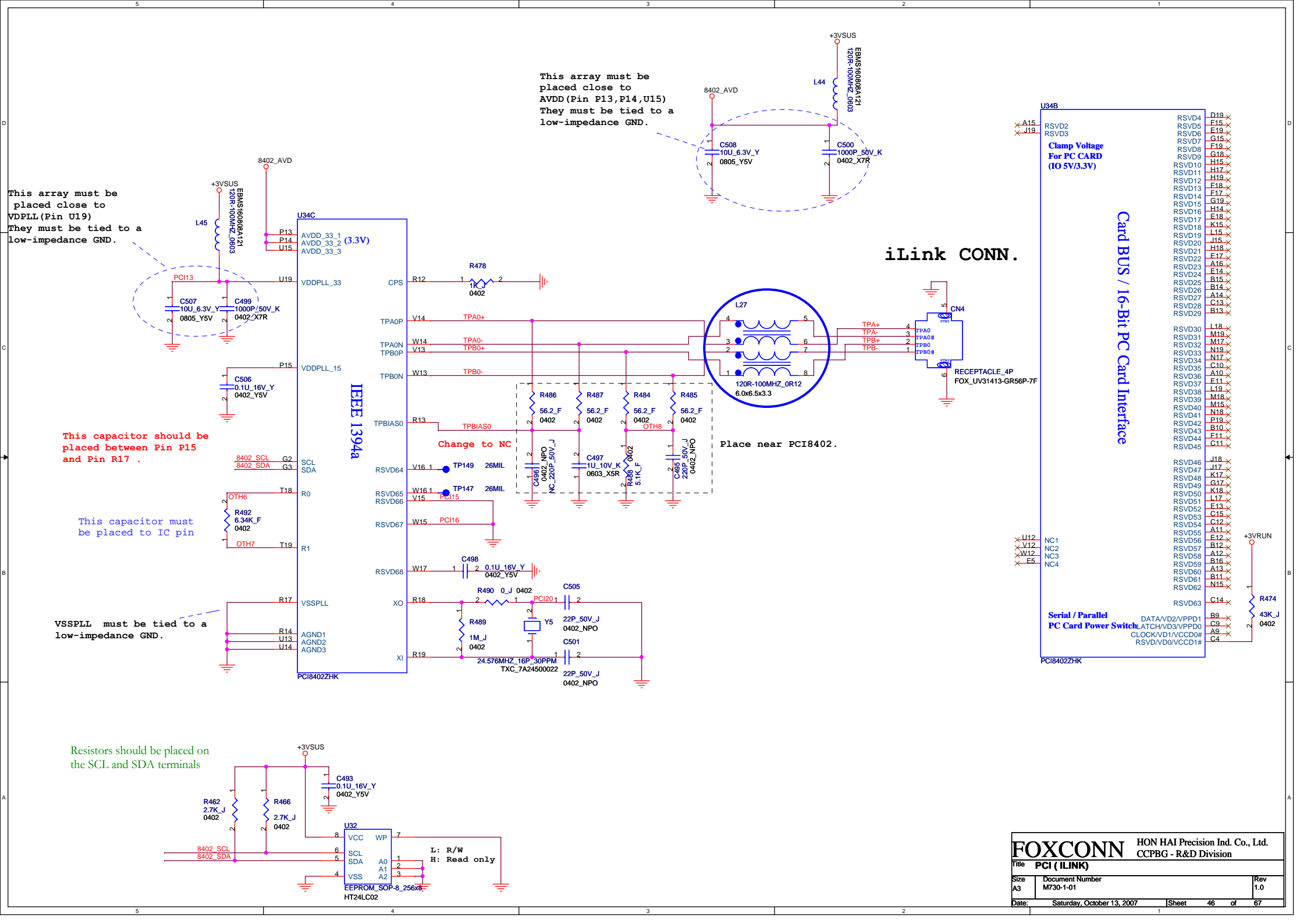
Close to CN25

CPU Thermal-Sensor

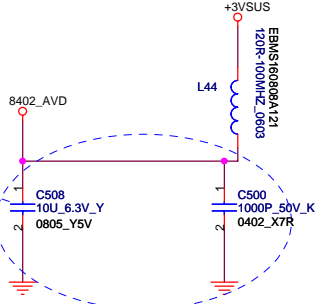


Close to U24

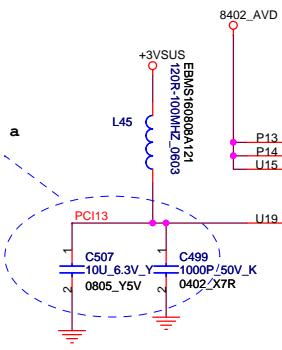




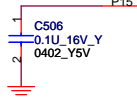
This array must be placed close to AVDD (Pin P13, P14, U15) They must be tied to a low-impedance GND.



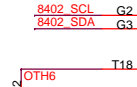
This array must be placed close to VDDPLL (Pin U19) They must be tied to a low-impedance GND.



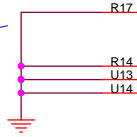
This capacitor should be placed between Pin P15 and Pin R17.



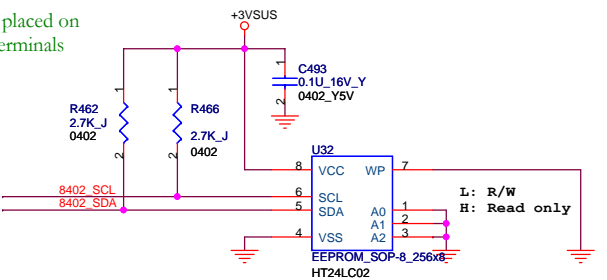
This capacitor must be placed to IC pin



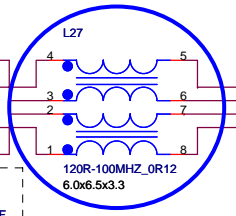
VSSPLL must be tied to a low-impedance GND.



Resistors should be placed on the SCL and SDA terminals

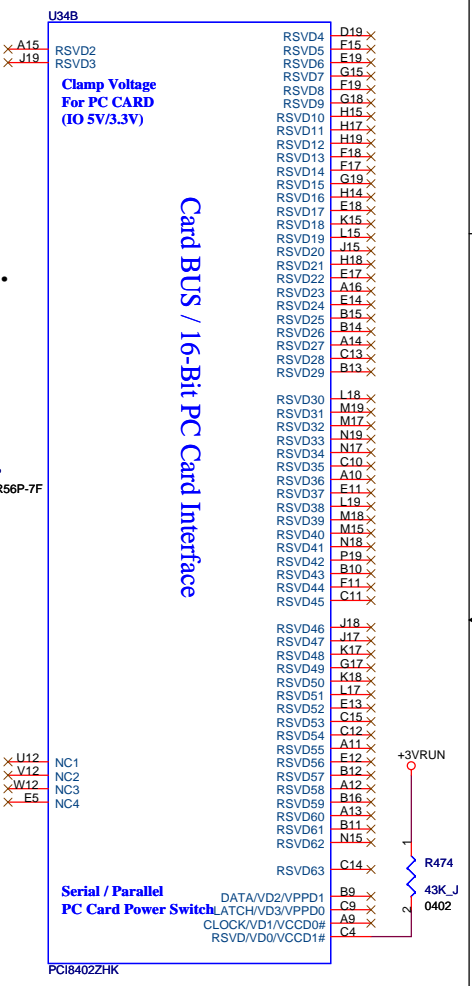


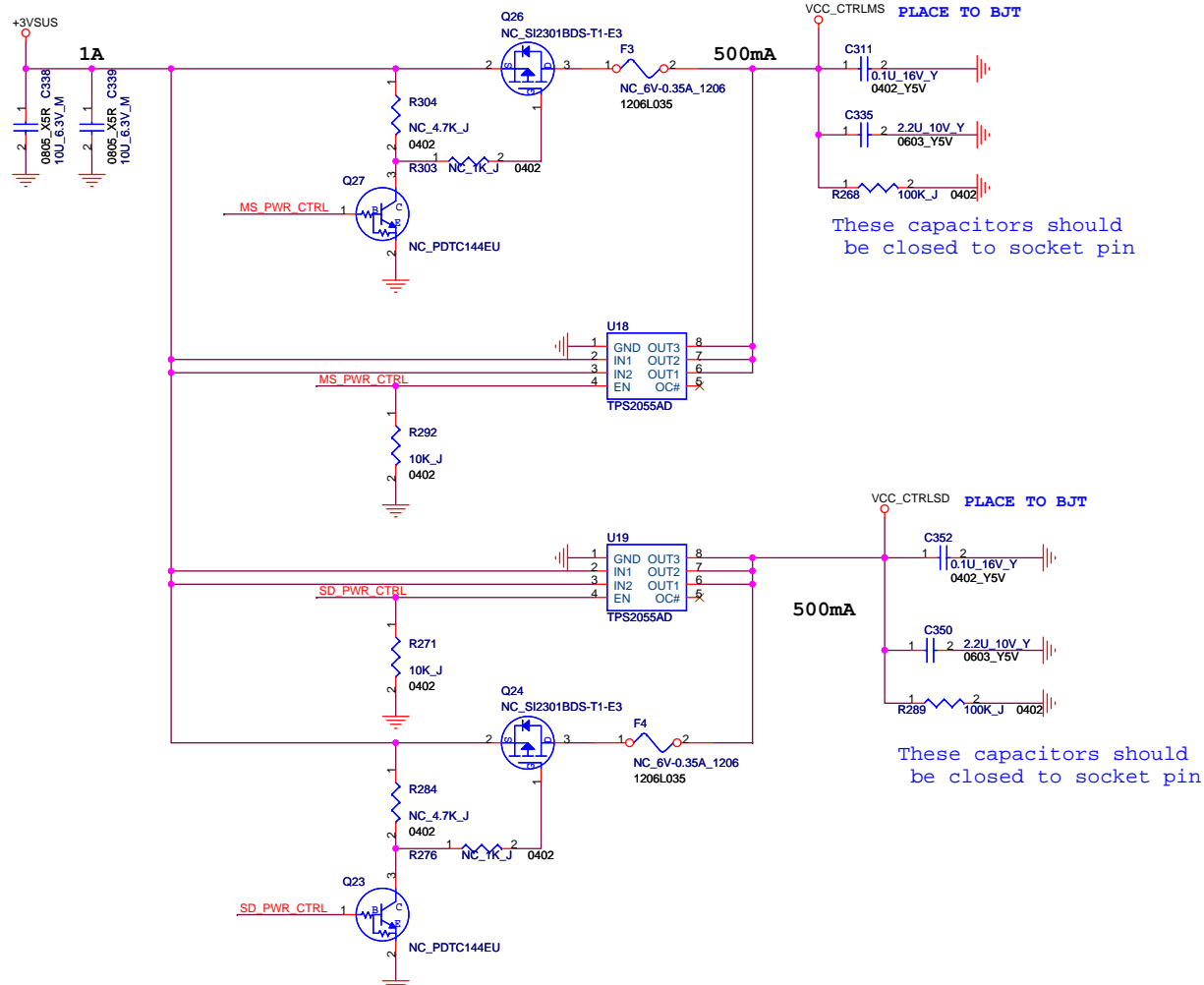
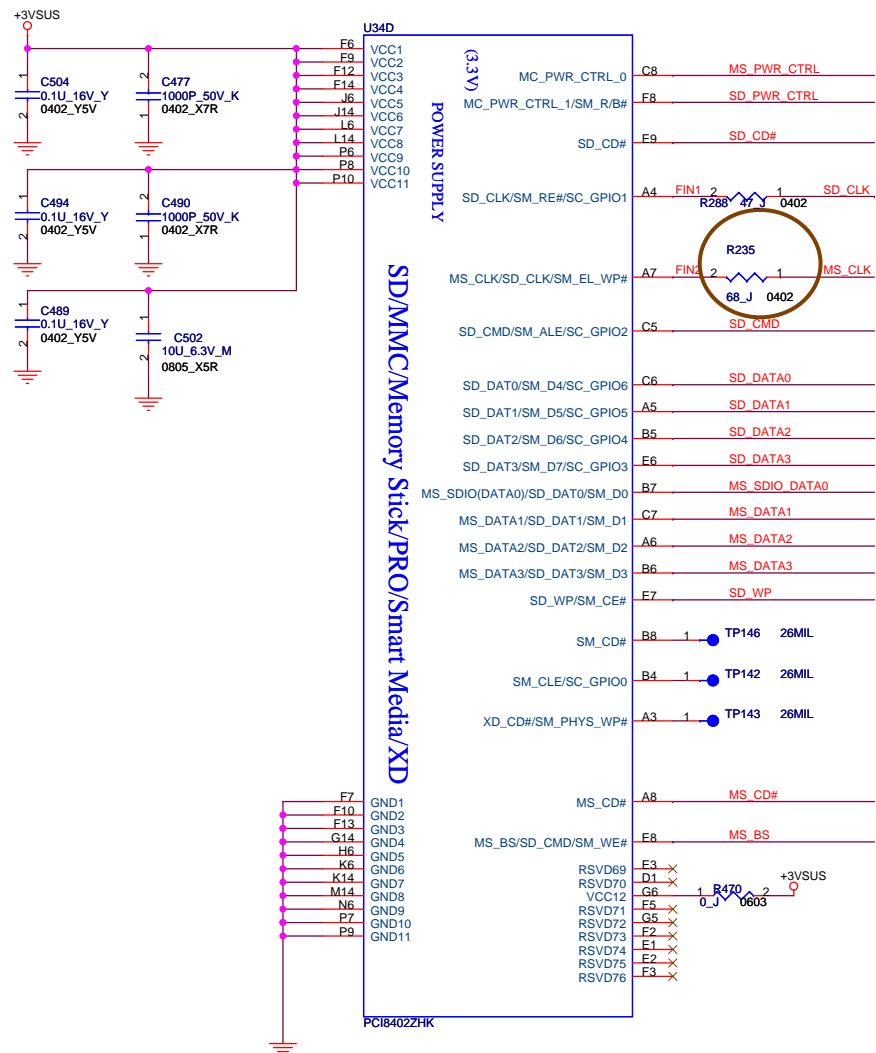
iLink CONN.



Place near PCI8402.

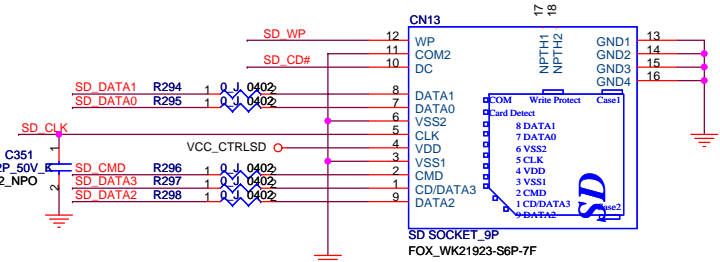
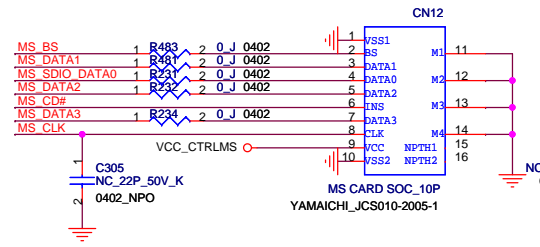
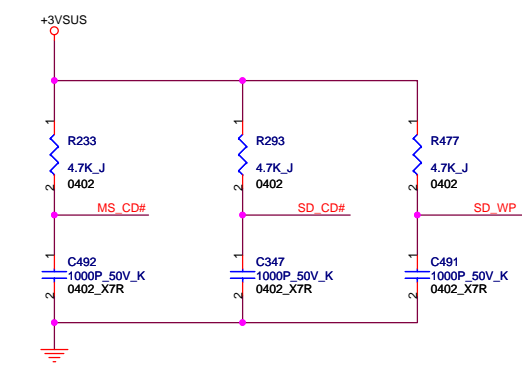
Card BUS / 16-Bit PC Card Interface



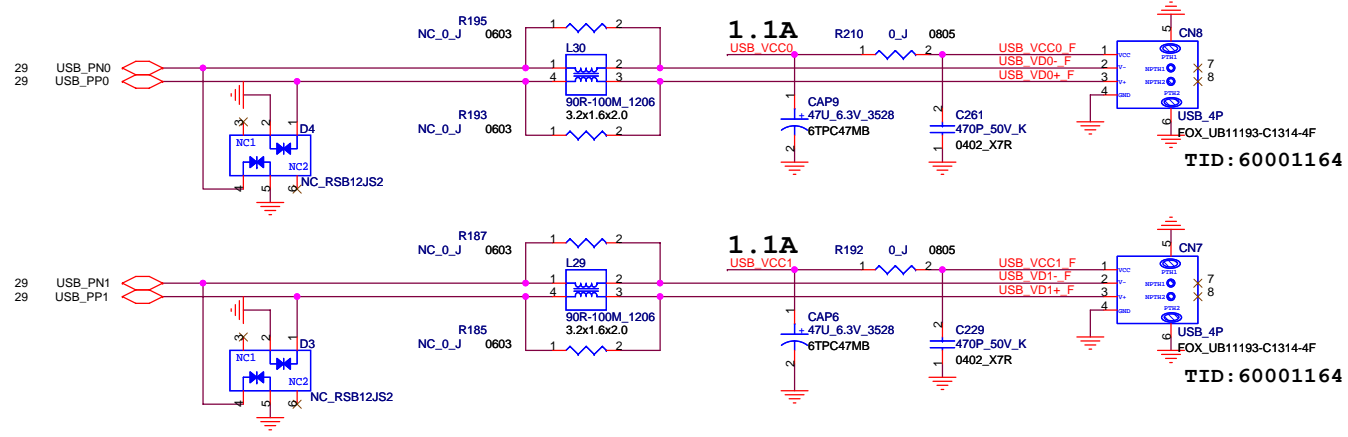
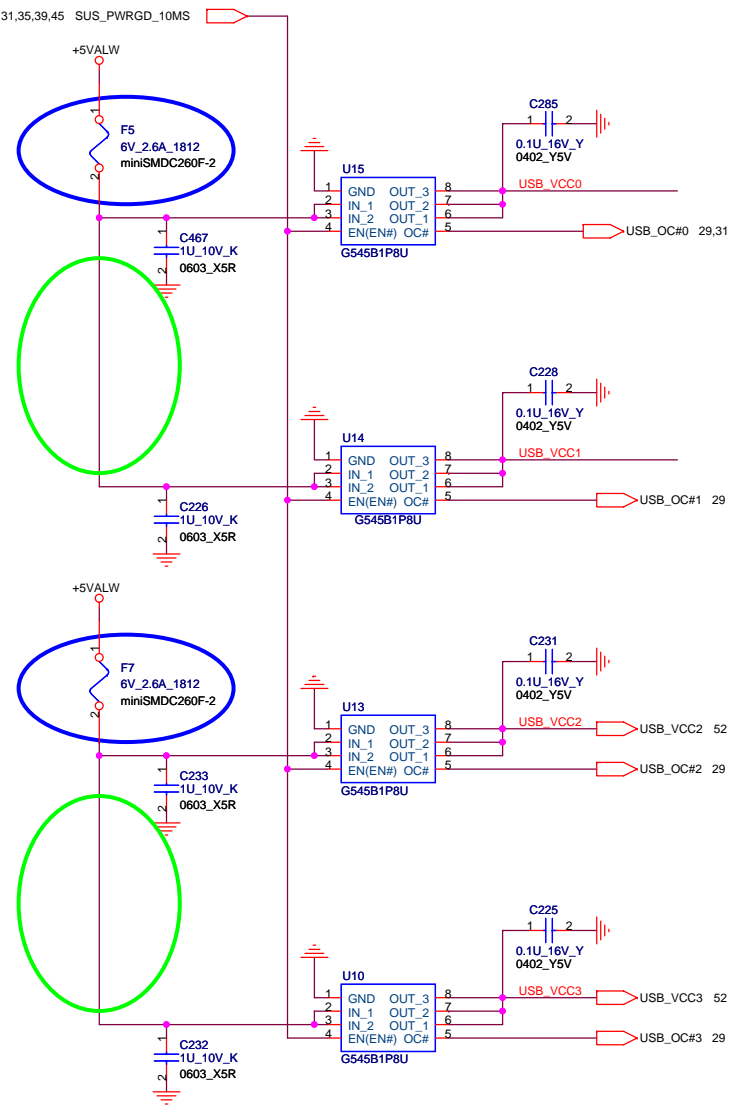


MS STD/DUO CONN.

SD CONN.

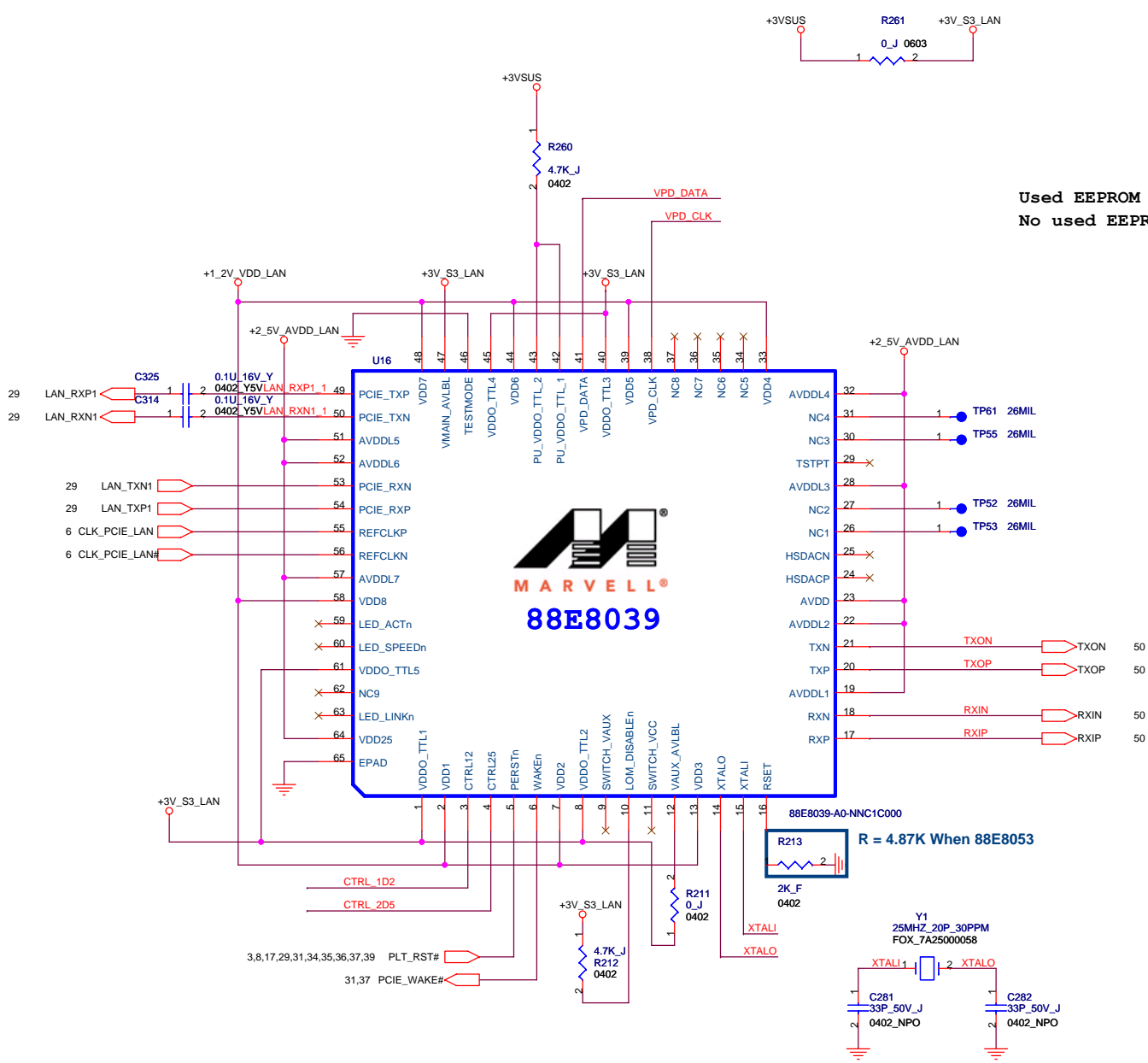


USB CONN.

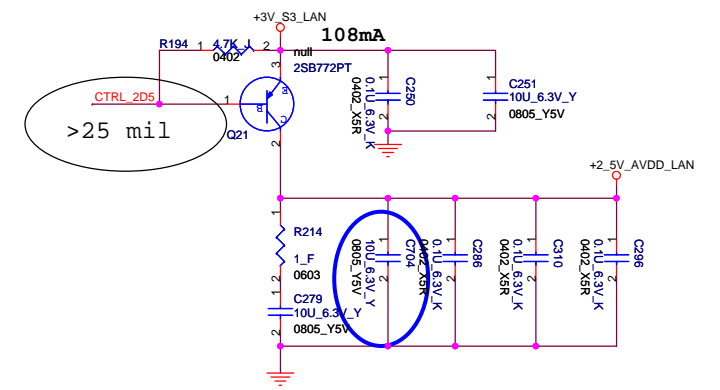
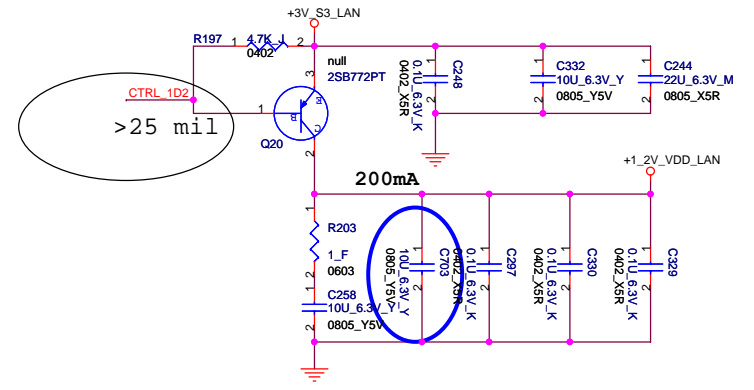
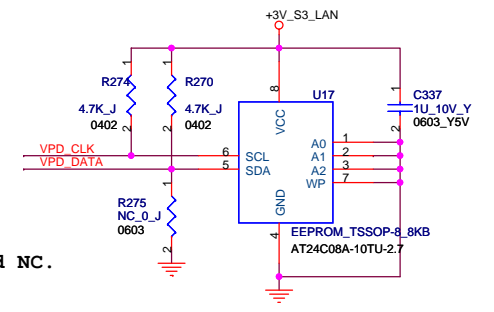


TID: 60001164

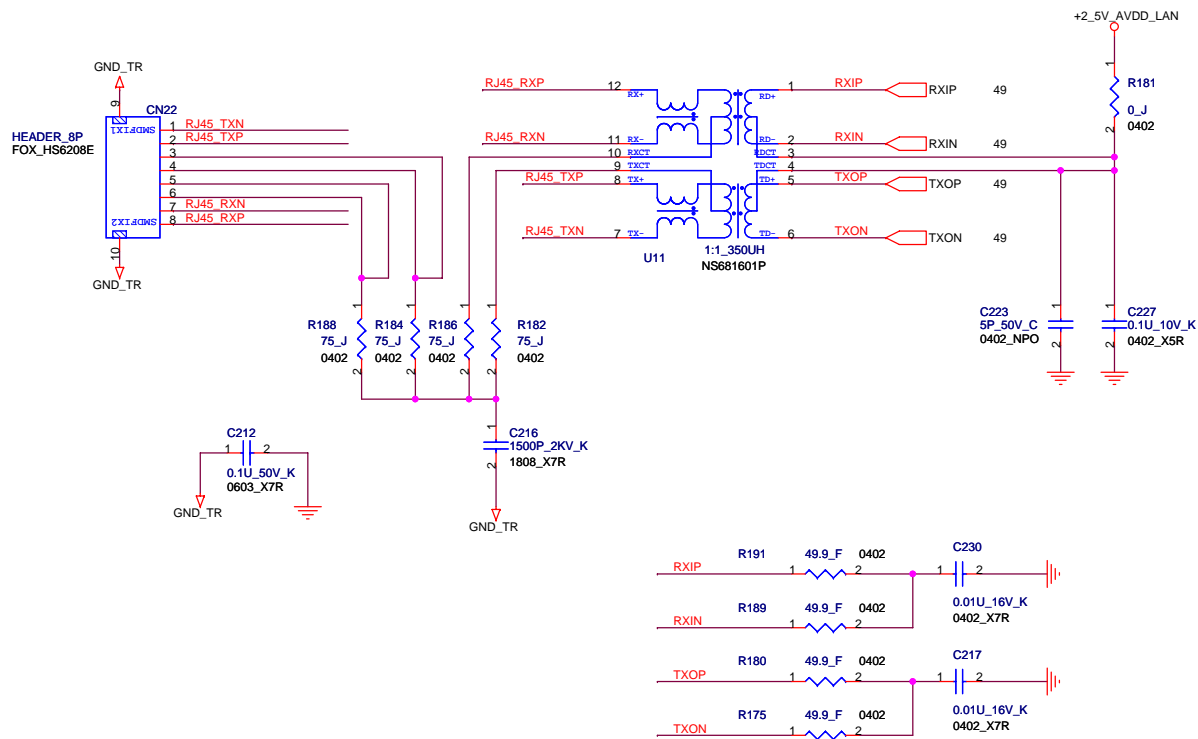
TID: 60001164



Used EEPROM R275 need NC.
No used EEPROM R270/U17/C337 need NC.

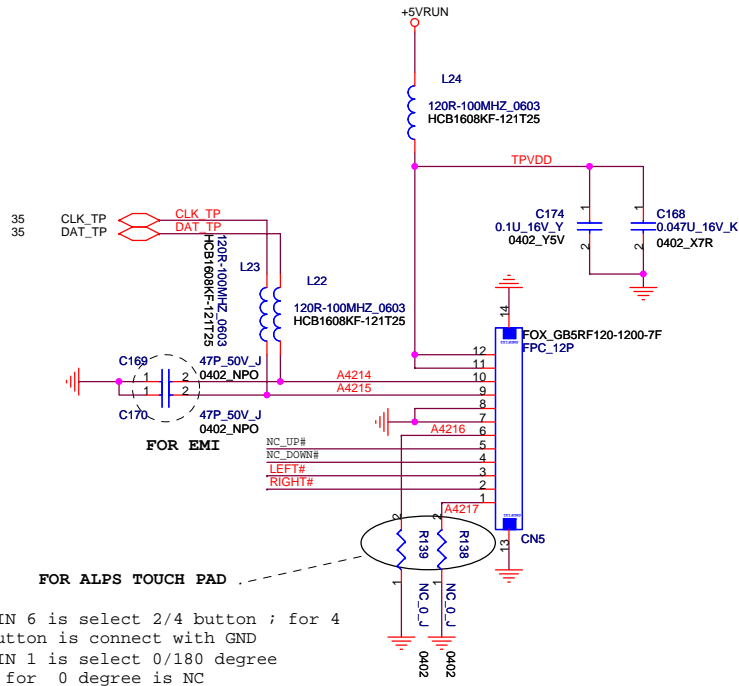


R = 4.87K When 88E8053

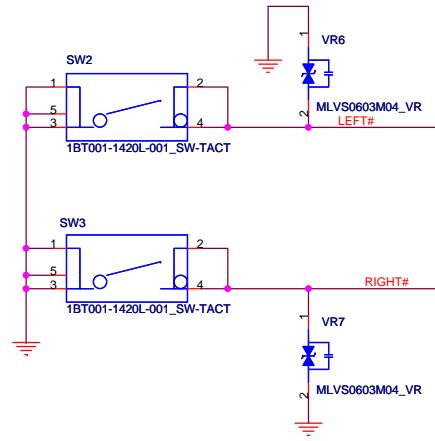


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		LAN Transformer	
Size	Document Number	Rev	
A3	M730-1-01	1.0	
Date:	Saturday, October 13, 2007	Sheet	50 of 67

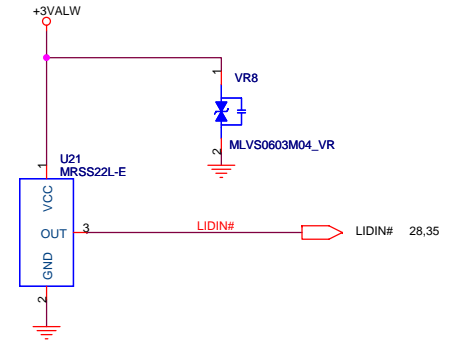
Touch Pad CONN.



TP_LEFT Button

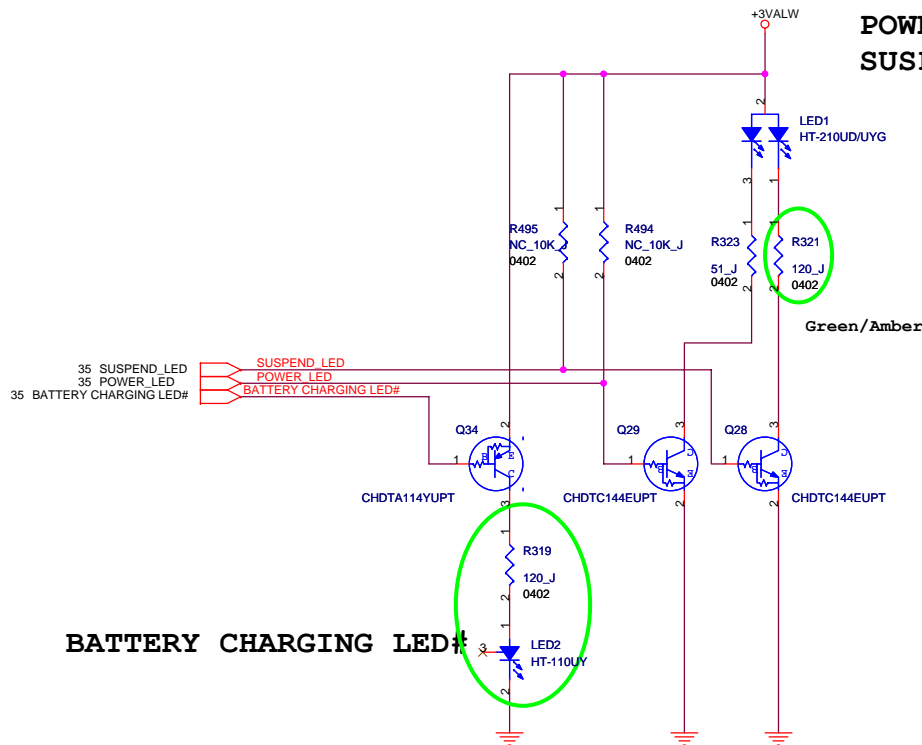


LID Switch

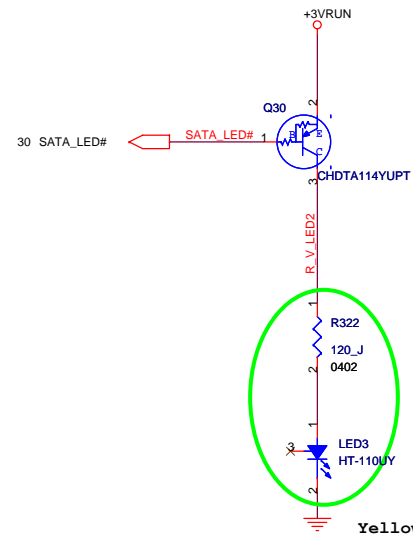


TP_Right Button

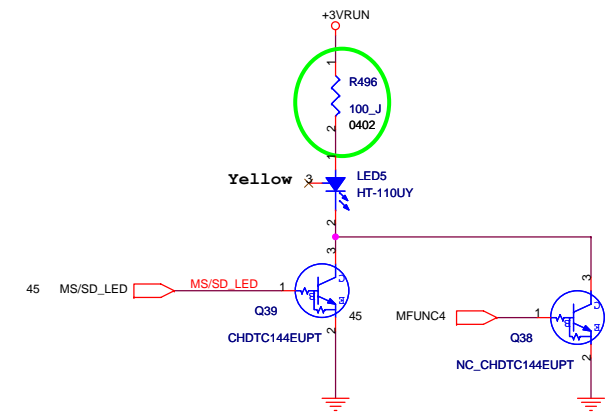
POWER_LED SUSPEND_LED



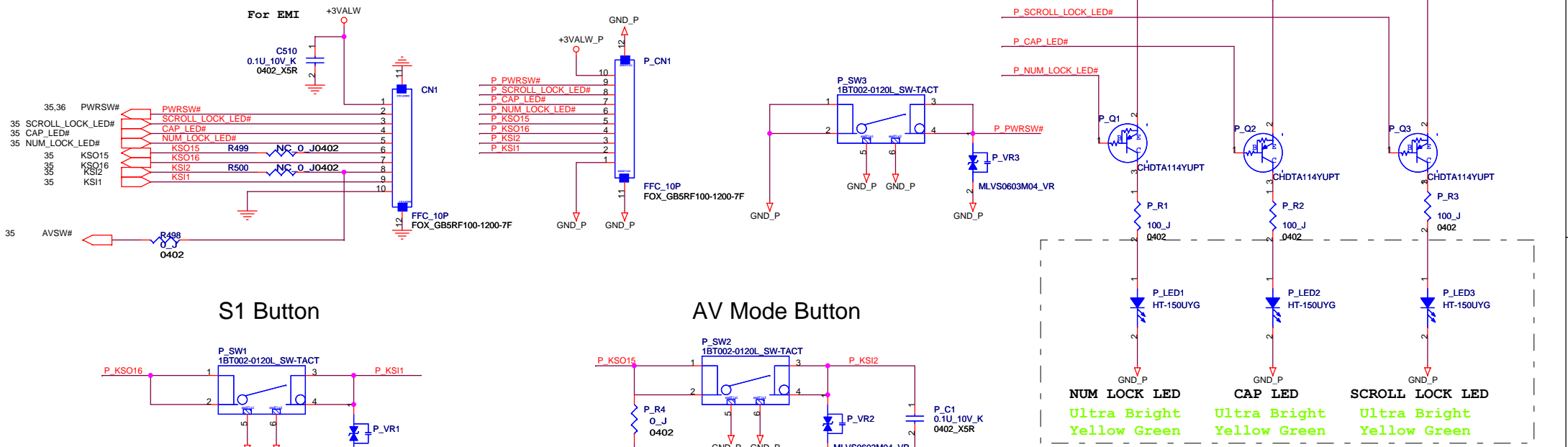
SATA_LED#



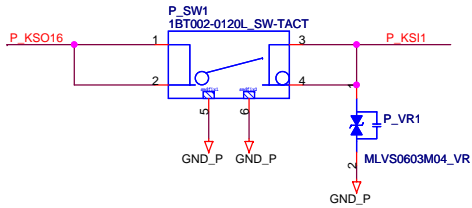
MS/SD LED



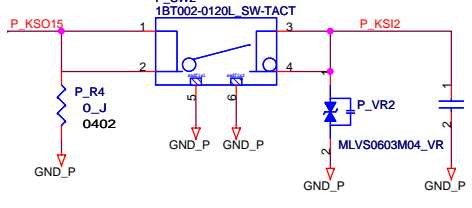
Power Button Board



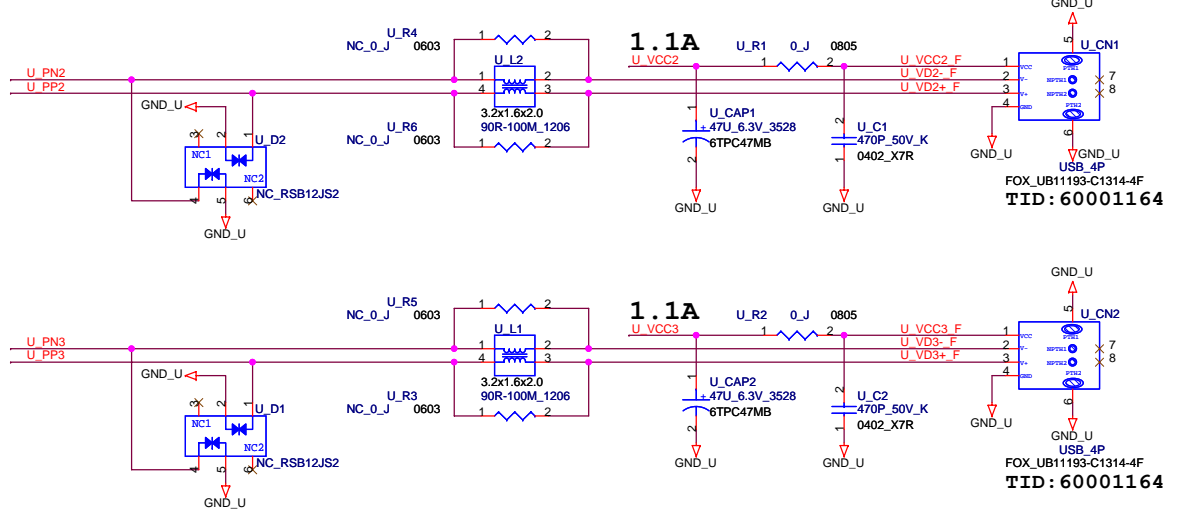
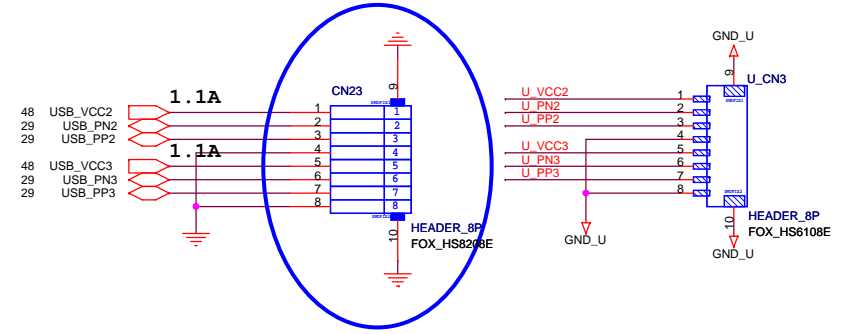
S1 Button

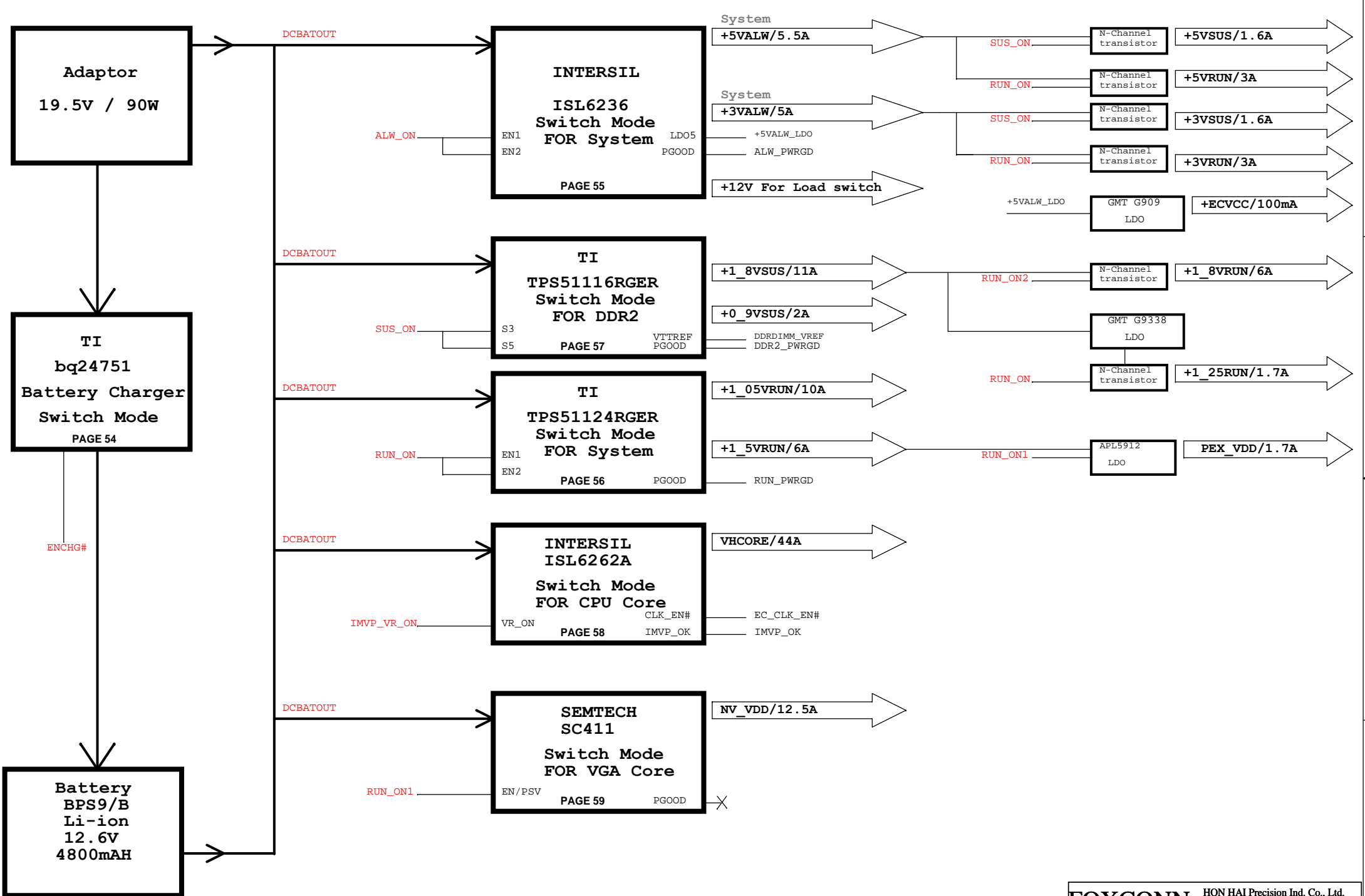


AV Mode Button

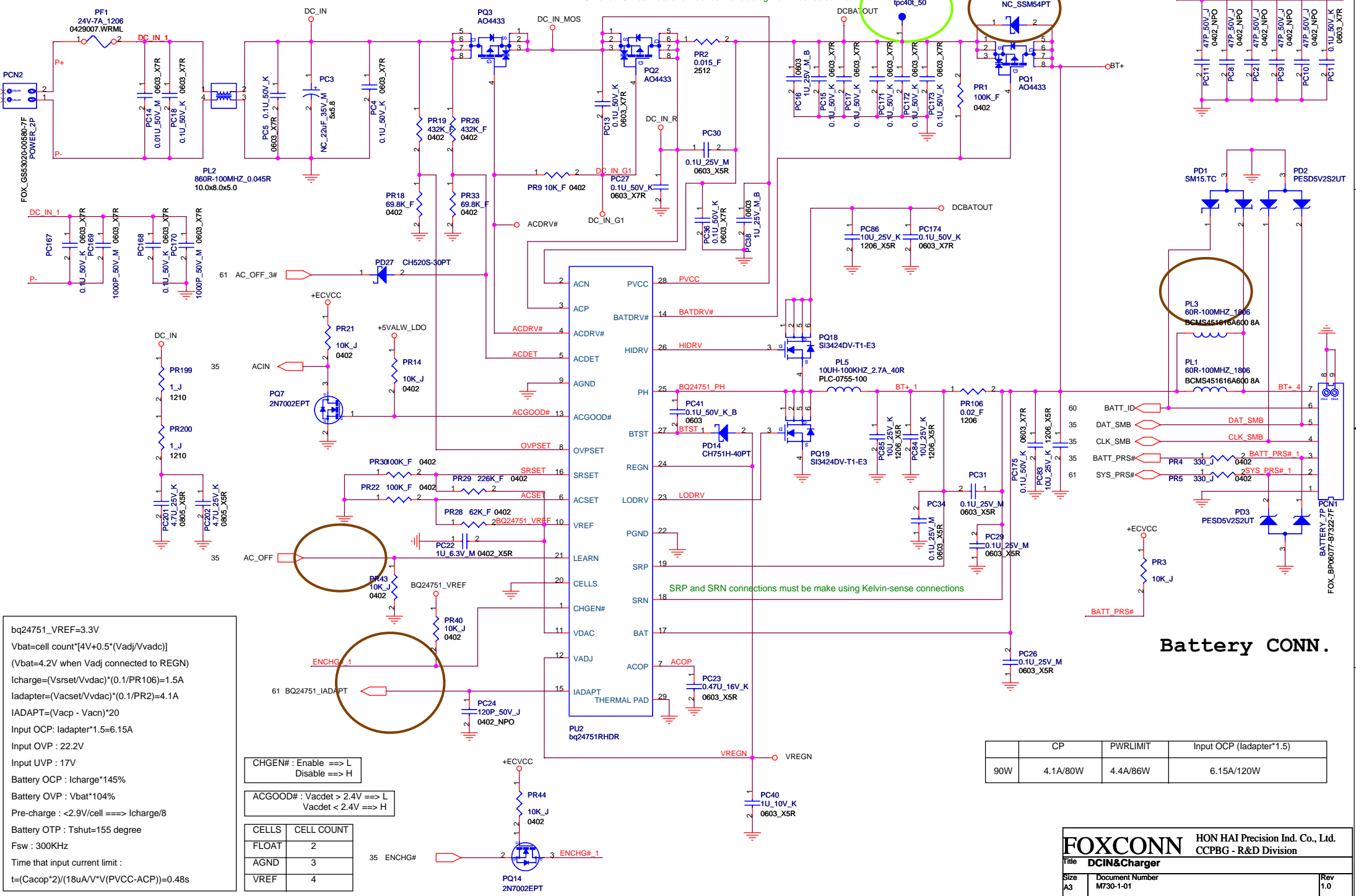
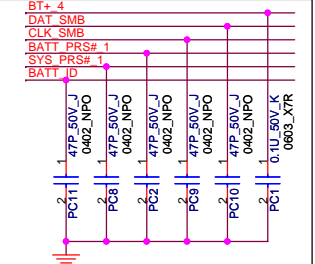
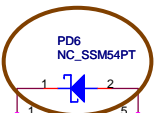
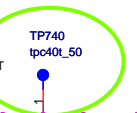


USB Board





ACP and ACN connections must be make using Kelvin-sense connections



bq24751_VREF=3.3V
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdc})]$
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to REGN})$
 $I_{charge} = (V_{srset} / V_{vdc}) * (0.1 / PR106) = 1.5A$
 $I_{adapter} = (V_{acset} / V_{vdc}) * (0.1 / PR2) = 4.1A$
 $IADAPT = (V_{acp} - V_{vacn}) * 20$
 Input OCP: $I_{adapter} * 1.5 = 6.15A$
 Input OVP: 22.2V
 Input UVP: 17V
 Battery OCP: $I_{charge} * 145\%$
 Battery OVP: $V_{bat} * 104\%$
 Pre-charge: $< 2.9V / \text{cell} ==> I_{charge} / 8$
 Battery OTP: $T_{shut} = 155 \text{ degree}$
 $F_{sw} = 300KHz$
 Time that input current limit:
 $t = (C_{acop} * 2) / (18uA / V * (V_{VCC} - ACP)) = 0.48s$

CHGEN# : Enable ==> L
 Disable ==> H

ACGOOD# : $V_{acdet} > 2.4V ==> L$
 $V_{acdet} < 2.4V ==> H$

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

Battery CONN.

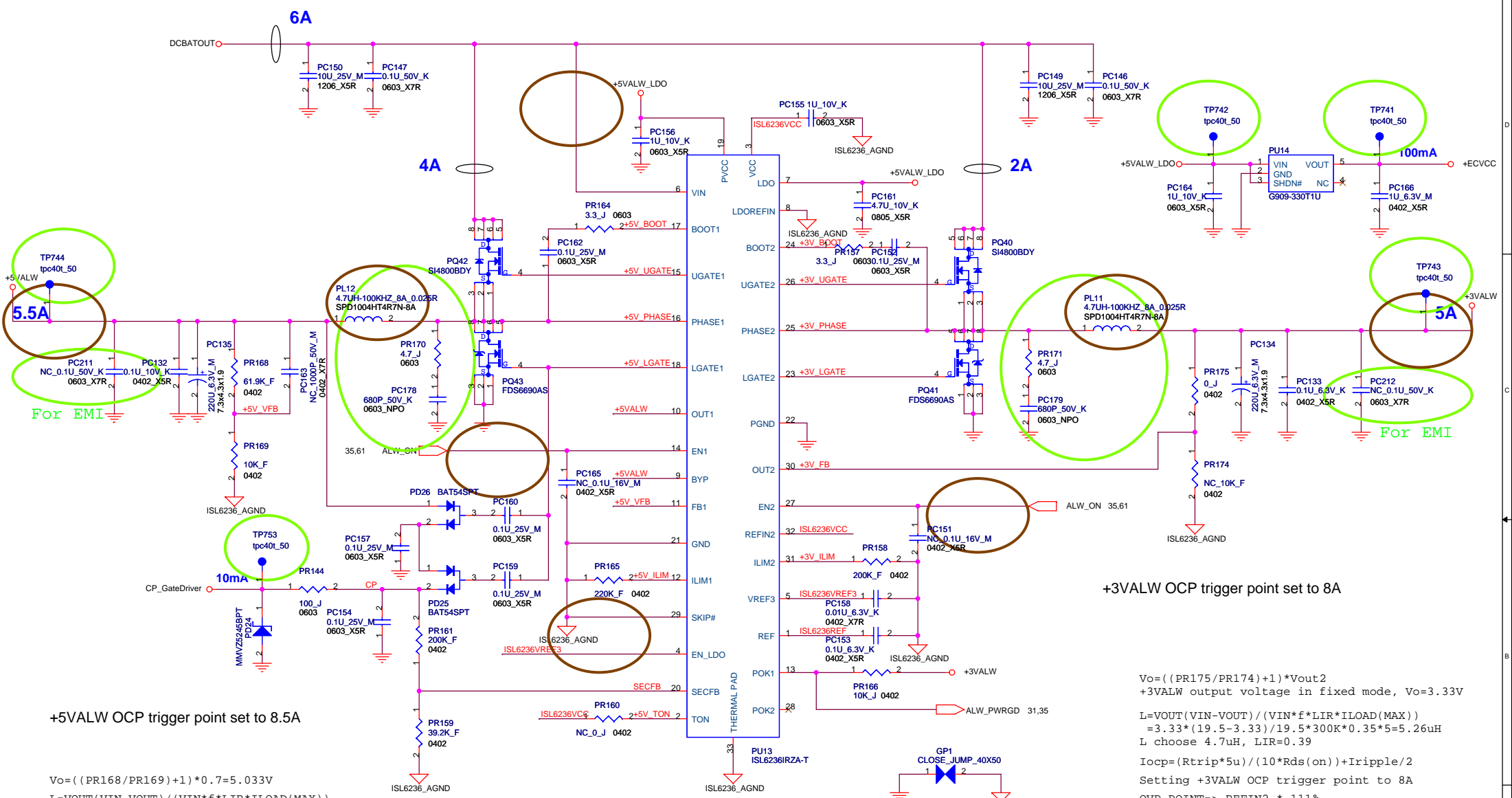
	CP	PWRLIMIT	Input OCP (Iadapter*1.5)
90W	4.1A/80W	4.4A/86W	6.15A/120W

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **DCIN&Charger**

Size A3	Document Number M730-1-01	Rev 1.0
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Date: Saturday, October 13, 2007 | Sheet 54 of 67



+5VALW OCP trigger point set to 8.5A

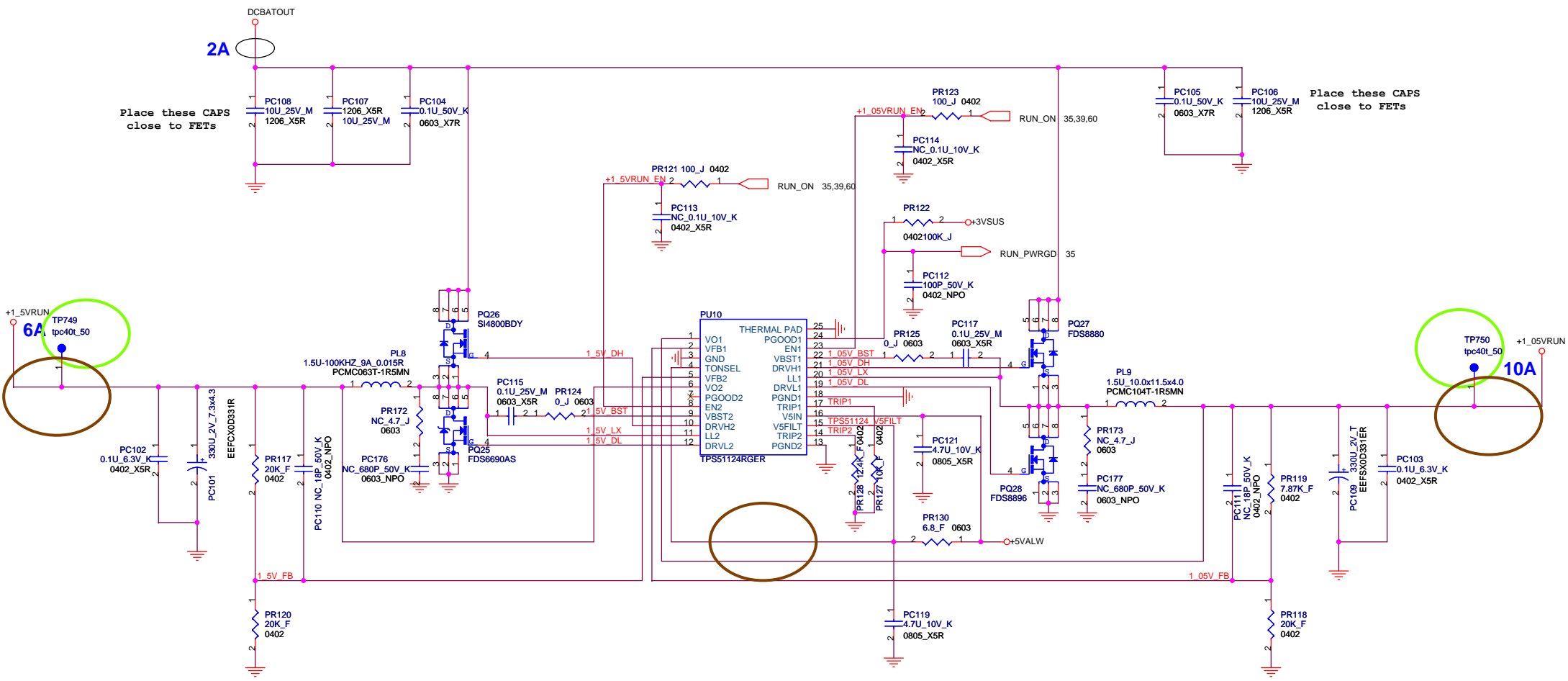
$V_o = ((PR168/PR169)+1) * 0.7 = 5.033V$
 $L = VOUT(VIN-VOUT) / (VIN * f * LIR * ILOAD(MAX))$
 $= 5 * (19.5-5) / 19.5 * 400K * 0.35 * 5 = 4.82uH$
 L choose 4.7uH, LIR=0.36
 $I_{ocp} = (R_{trip} * 5u) / (10 * R_{ds(on)}) + I_{ripple} / 2$
 Setting +5VALW OCP trigger point to 8.5A
 OVP POINT=> VFB * 111%
 UVP POINT=> VFB * 70%
 Switching Frequency = 400KHz

+3VALW OCP trigger point set to 8A

$V_o = ((PR175/PR174)+1) * V_{out2}$
 +3VALW output voltage in fixed mode, $V_o = 3.33V$
 $L = VOUT(VIN-VOUT) / (VIN * f * LIR * ILOAD(MAX))$
 $= 3.33 * (19.5-3.33) / 19.5 * 300K * 0.35 * 5 = 5.26uH$
 L choose 4.7uH, LIR=0.39
 $I_{ocp} = (R_{trip} * 5u) / (10 * R_{ds(on)}) + I_{ripple} / 2$
 Setting +3VALW OCP trigger point to 8A
 OVP POINT=> REFIN2 * 111%
 UVP POINT=> REFIN2 * 70%
 Switching Frequency = 300KHz

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM



Setting +1.5VRUN OCP trigger point to 10.6A

$$V_o = ((PR117/PR120)+1) * 0.758 = 1.516V$$

$$L = V_{OUT}(V_{IN} - V_{OUT}) / (V_{IN} * f * L_{IR} * I_{LOAD}(MAX))$$

$$= 1.5 * (19.5 - 1.5) / 19.5 * 420K * 0.35 * 6 = 1.57\mu H$$

L choose 1.5uH, LIR=0.366

$$I_{ocp} = (R_{trip} * 10u) / R_{ds(on)} + I_{ripple} / 2$$

Setting +1.5VRUN OCP trigger point to 10.6A

OVP POINT=> VFB * 115%

UVP POINT=> VFB * 70%

Switching Frequency = 420KHz

Setting +1.05VRUN OCP trigger point to 14.6A

$$V_o = ((PR119/PR118)+1) * 0.758 = 1.056V$$

$$L = V_{OUT}(V_{IN} - V_{OUT}) / (V_{IN} * f * L_{IR} * I_{LOAD}(MAX))$$

$$= 1.05 * (19.5 - 1.05) / 19.5 * 360K * 0.35 * 10 = 0.79\mu H$$

L choose 1.5uH, LIR=0.18

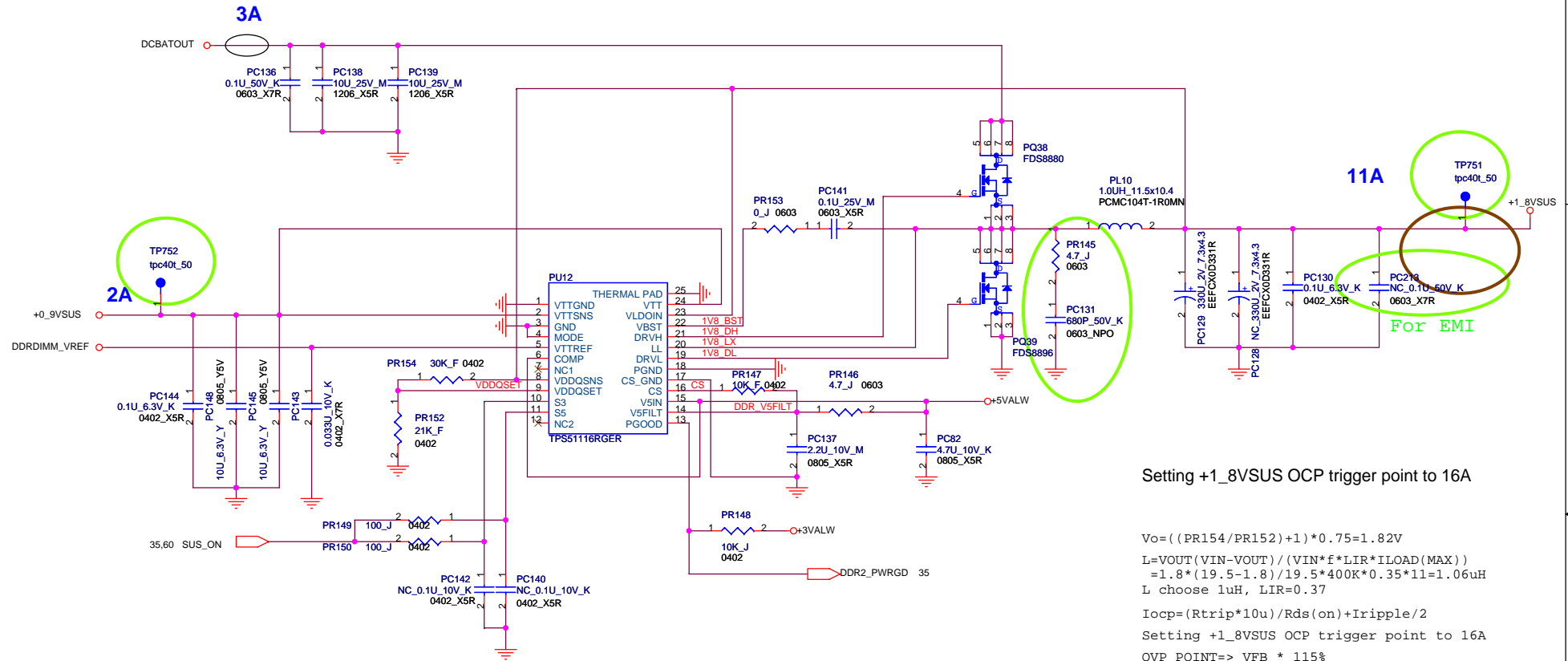
$$I_{ocp} = (R_{trip} * 10u) / R_{ds(on)} + I_{ripple} / 2$$

Setting +1.05VRUN OCP trigger point to 14.6A

OVP POINT=> VFB * 115%

UVP POINT=> VFB * 70%

Switching Frequency = 360KHz



Setting +1_8VSUS OCP trigger point to 16A

$$V_o = ((PR154/PR152)+1) * 0.75 = 1.82V$$

$$L = V_{OUT}(V_{IN}-V_{OUT}) / (V_{IN} * f * LIR * I_{LOAD}(MAX))$$

$$= 1.8 * (19.5 - 1.8) / (19.5 * 400K * 0.35 * 11) = 1.06 \mu H$$

L choose 1uH, LIR=0.37

$$I_{ocp} = (R_{trip} * 10u) / R_{ds(on)} + I_{ripple} / 2$$

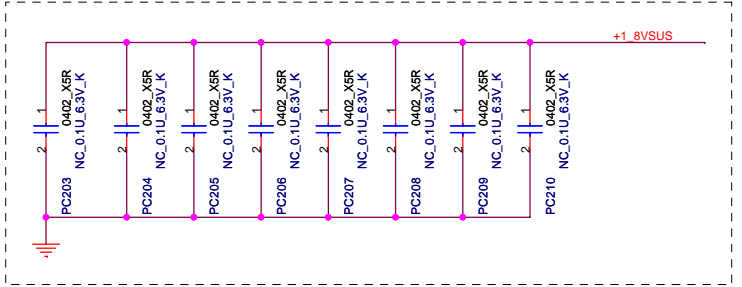
Setting +1_8VSUS OCP trigger point to 16A

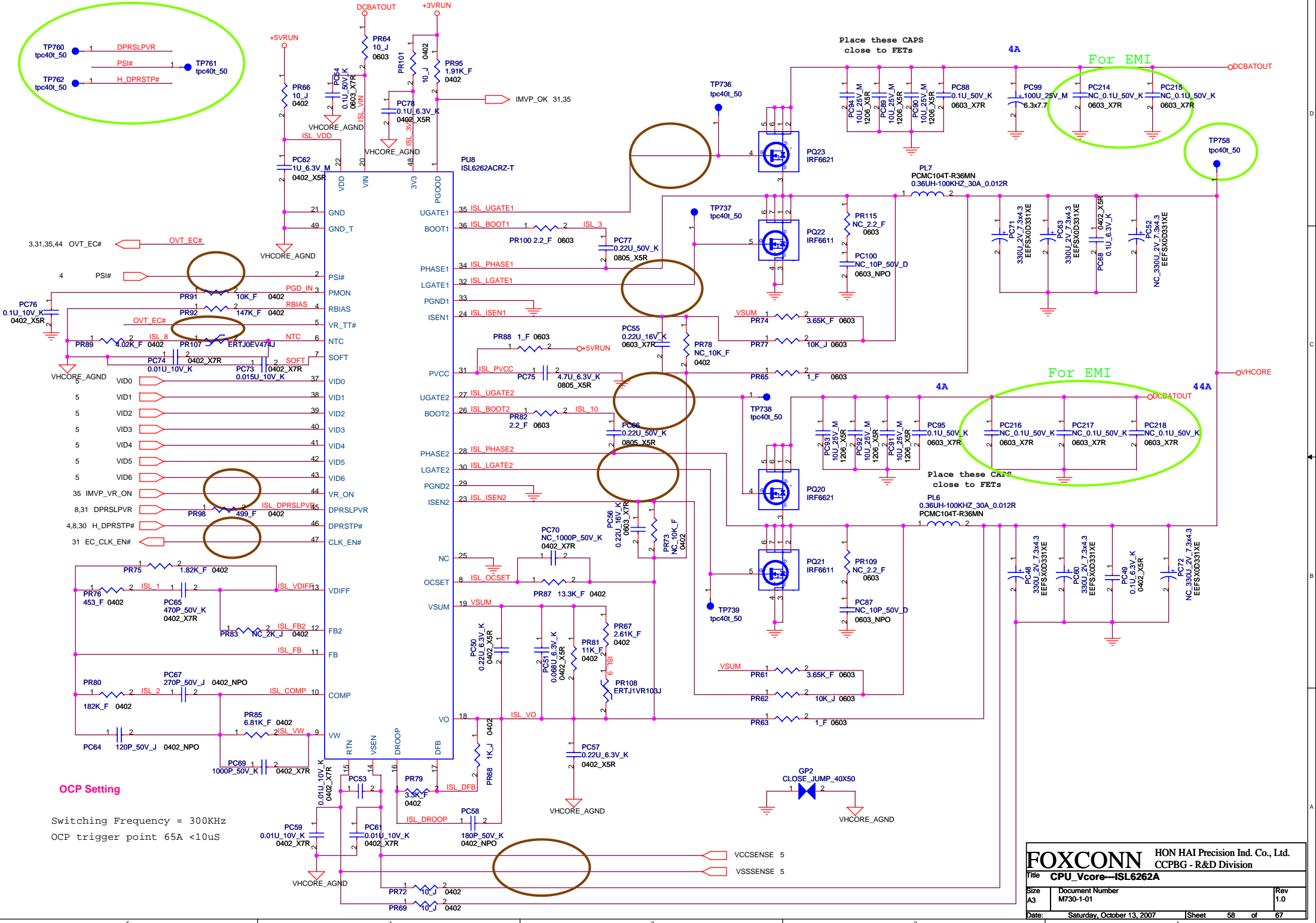
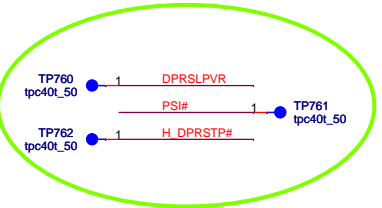
OVP POINT => VFB * 115%

UVP POINT => VFB * 70%

Switching Frequency = 400KHz

For EMI





Place these CAPS close to FETs

For EMI

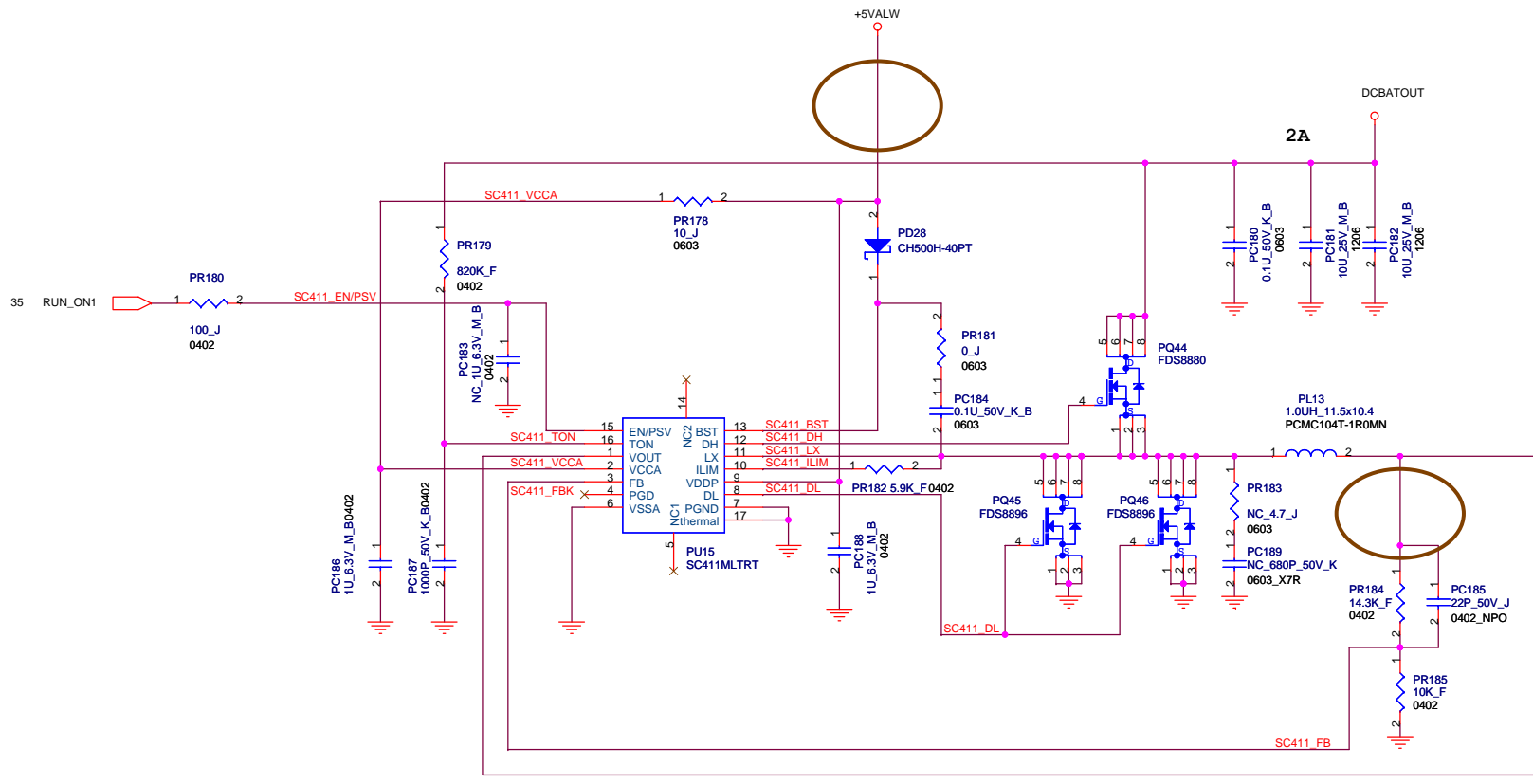
For EMI

Place these CAPS close to FETs

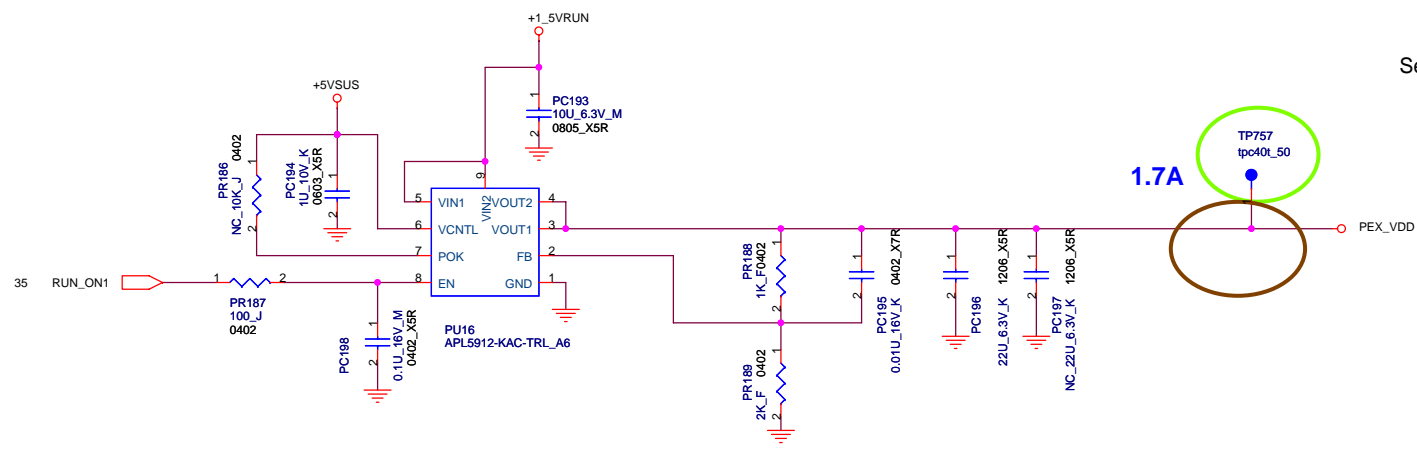
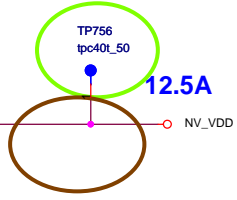
OCP Setting

Switching Frequency = 300KHz
 OCP trigger point 65A <10uS

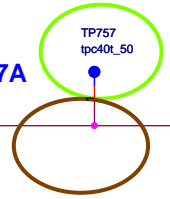
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title CPU_Vcore-ISL6262A			
Size A3	Document Number M730-1-01	Rev 1.0	
Date:	Saturday, October 13, 2007	Sheet 58	of 67



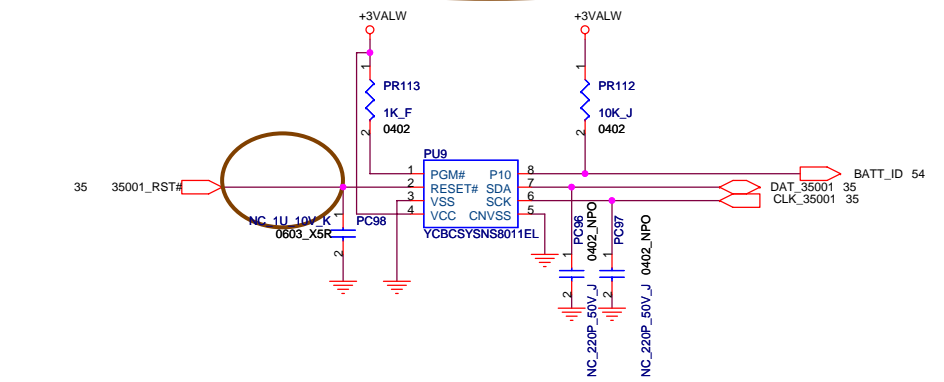
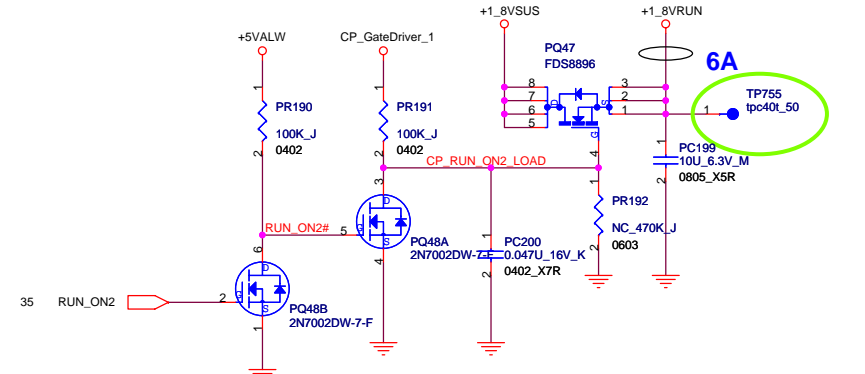
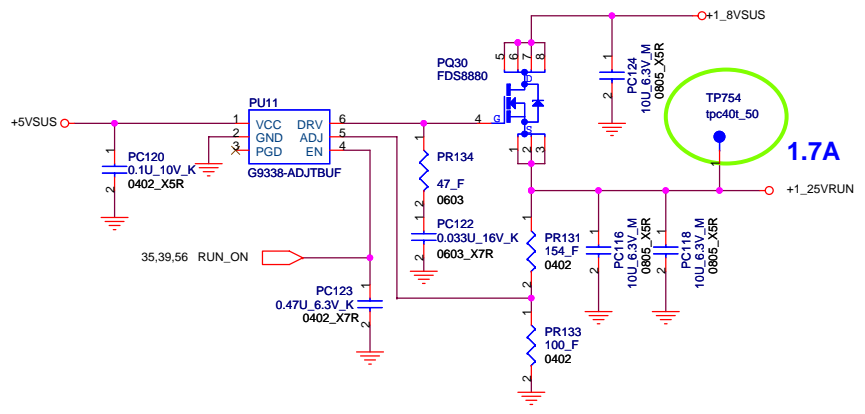
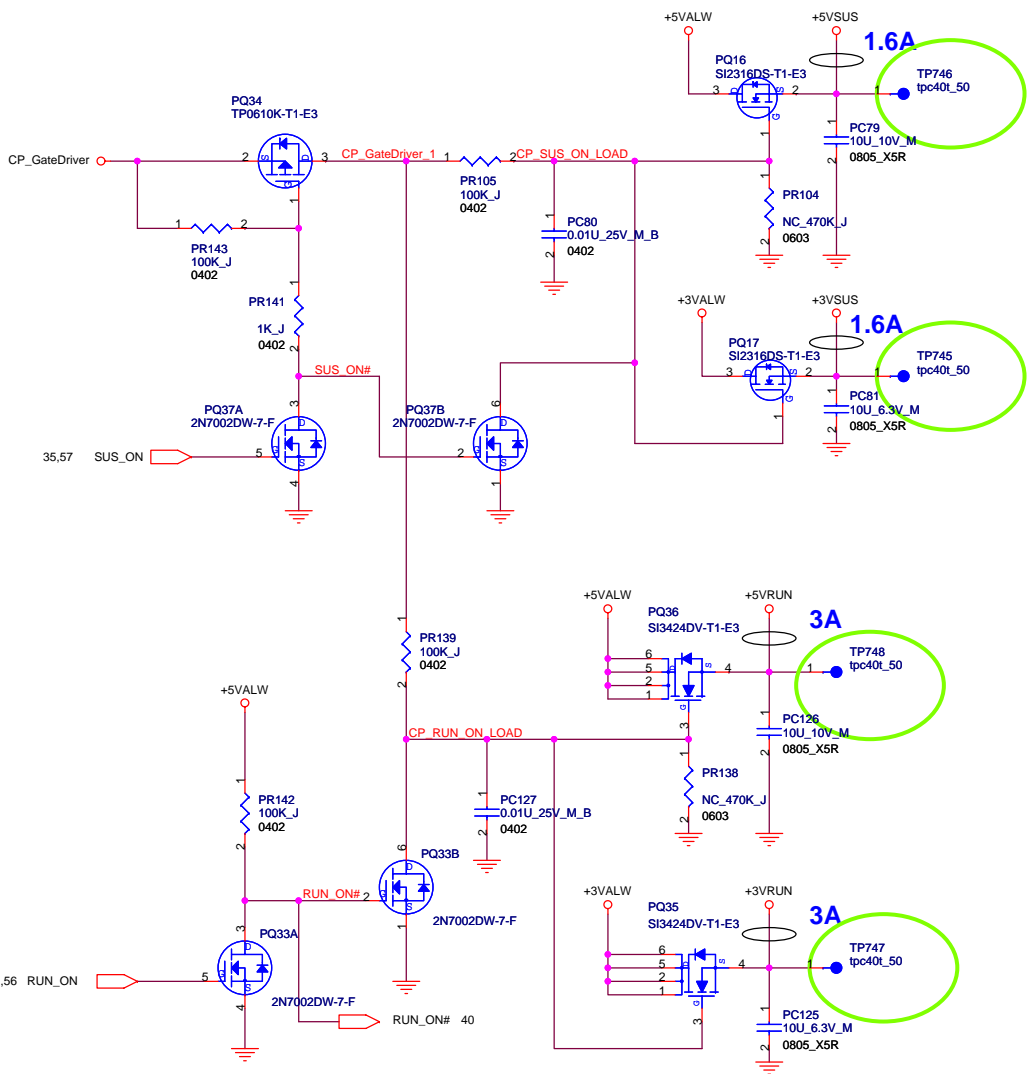
$V_o = ((PR184/PR185)+1) * 0.5 = 1.215V$
 $L = V_{OUT} (V_{IN} - V_{OUT}) / (V_{IN} * f * L_{IR} * I_{LOAD} (MAX))$
 $= 1.2 * (19.5 - 1.2) / (19.5 * 280K * 0.35 * 12.5) = 0.92uH$
 L choose 1uH, LIR=0.32
 $I_{ocp} = (R_{trip} * 10u) / R_{ds(on)} + I_{ripple} / 2$
 Setting +1_8VSUS OCP trigger point to 18A
 OVP POINT => VFB * 116%
 UVP POINT => VFB * 70%
 Switching Frequency = 280KHz



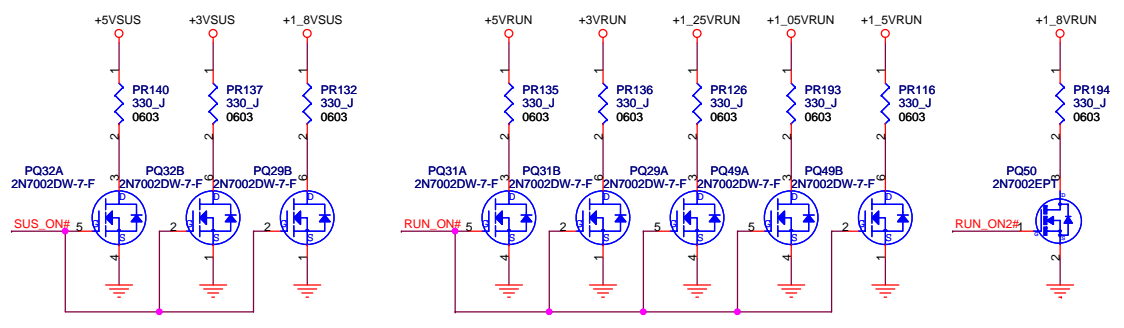
Setting +1_8VSUS OCP trigger point to 16A

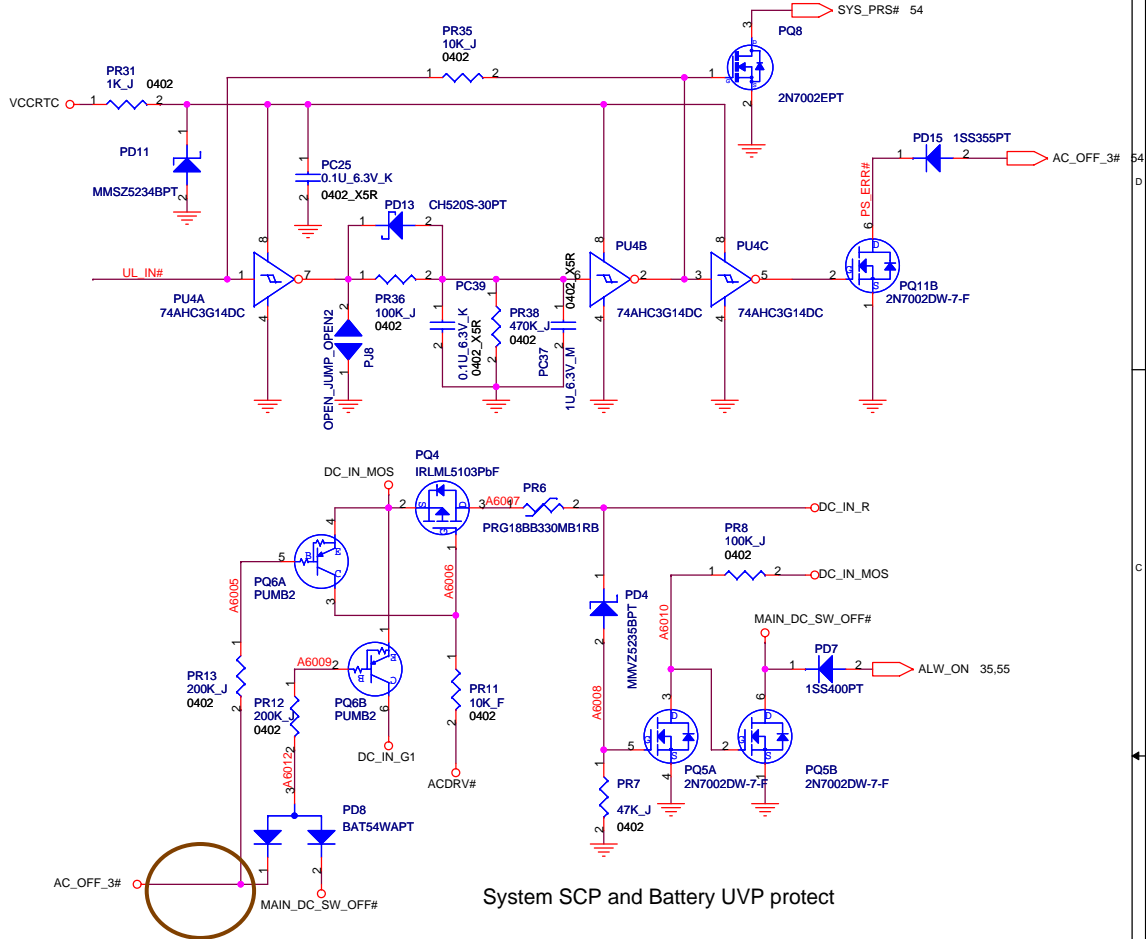
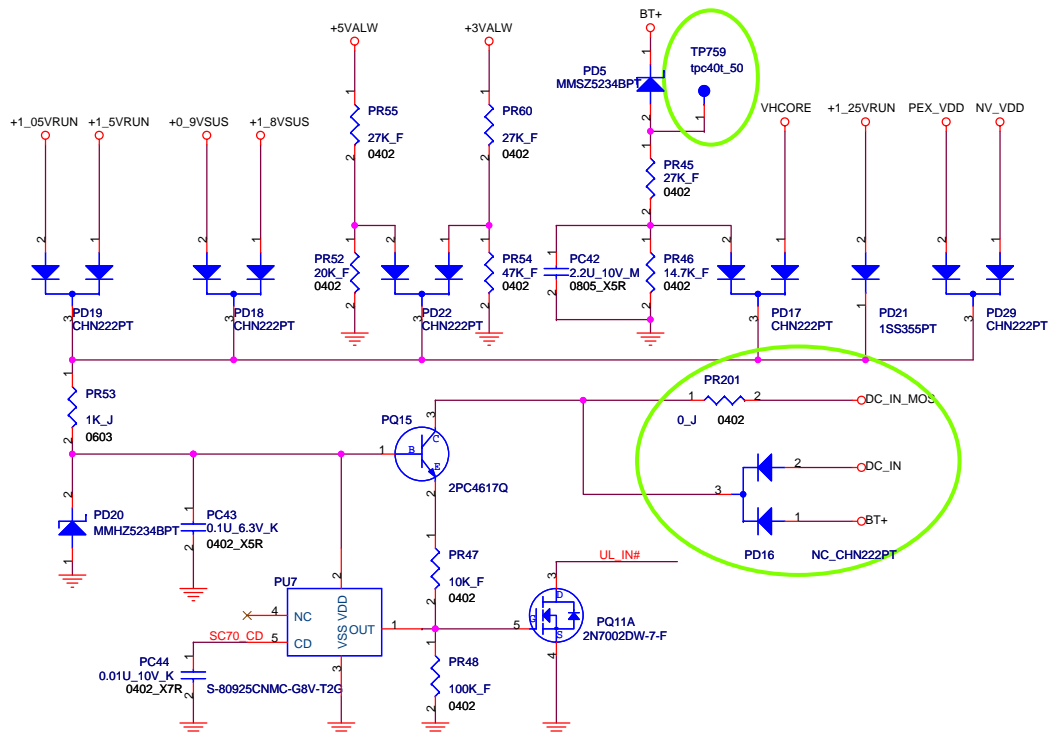


$V_o = ((PR188/PR189)+1) * 0.8 = 1.2V$

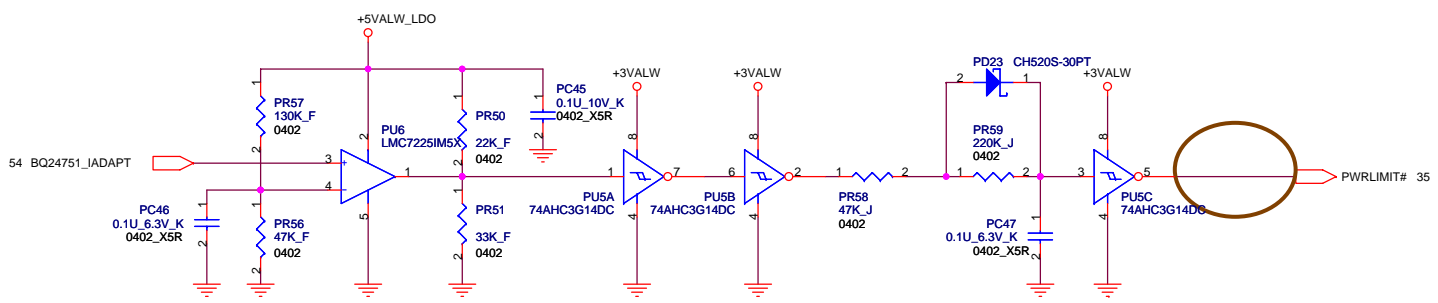


Discharge circuit for power-off

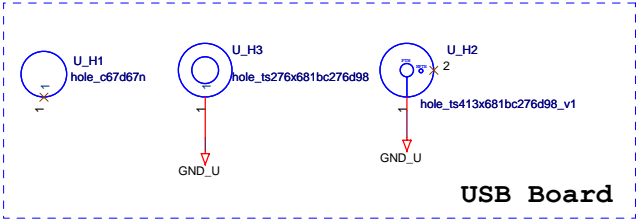
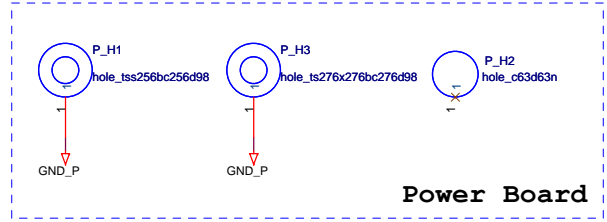
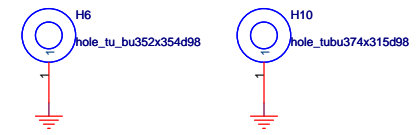
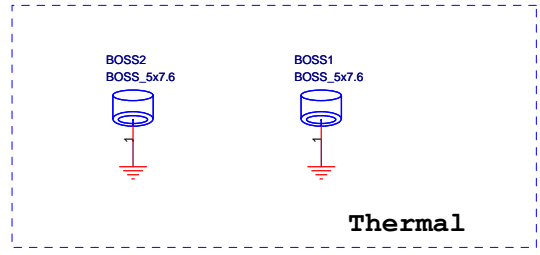
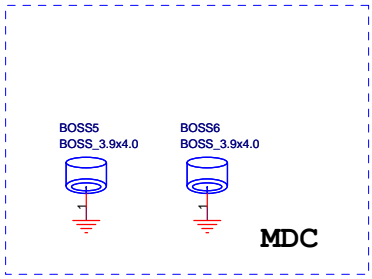
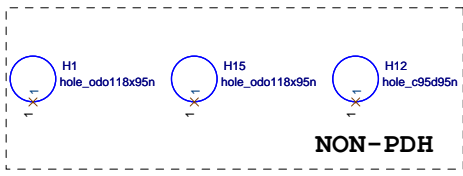
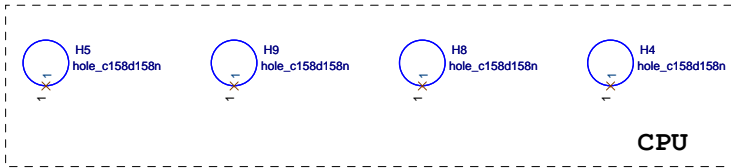




System SCP and Battery UVP protect



Setting PWRLIMIT# trigger point to 4.4A



M730 EVT

(2007/05/29)

Base on M720_SCHEMATIC_0528_1700.

(2007/05/30)

P.35 Add R607 for OVT_GFX#
P.23 Add R604,R605 and R606 for IFPC/D power

(2007/05/31)

P.40 Change R171 to 22ohm,C215 to 22uf.
P.42 Change C201,C202,C204 to X5R.
P.44 Delete U12,R183,R190 and C224 for remove memory thermal sensor solution.
P.9 Delete R366,R69,R74 and R81.
P.11 Delete Internal graphics power.
P.12 Delete Internal graphics power.
P.54 Change PR2 from 0.02_F 2512 to 0.015_F 2512 for 90W adapter application.
P.60 Change PQ47 from SI4800BDY to FDS8896
P.28 Add C702

(2007/06/04)

P.54 Change PR28 from 44.2K_F to 62K_F for setting constant power trigger point to 4.1A
P.57 Change PR147 from 6.8K_F to 10K_F for setting +1_8VSUS OCP trigger point to 16A
P.59 Change PR184 from 14K_F to 14.3K_F for setting NV_VDD to 1.215V
P.59 Change PR182 from 6.8K_F to 5.9K_F for setting NV_VDD OCP to 18A
P.59 Add PR197, PR198 0_J for NV_VDD feedback remote sense.
P.61 Change PR56 from 53.6K_F to 47K_F for setting PWRLIMIT trigger point to 4.4A.

(2007/06/05)

P.54 Change PQ18 and PQ19 from SI4800BDY to SI3424DV for layout space.
P.54 Change PC24 from 120pF 10% to 120pF 5% for purchase difficult.
P.60 Change PQ35 and PQ36 from SI4800BDY to SI3424DV for layout space.

(2007/06/08)

P.62 Add BOSS7 and BOSS8 for thermal request

(2007/06/14)

P.9 Change R97 to NC
P.9 Add R608/R609 and NC for LVDS_VREFH and LVDS_VREFL
P.8 Add TP731,TP732,TP733,TP734,TP735 for GFX_VID[3:0] and GFX_VR_EN

(2007/06/22)

P.19 Net I2CS_SDA & I2CS_SCL exchange with TP632 & TP633
P.22 Q40,Q41,Q42,Q43,R575,R576,R582 and R583 change from NC to mount for Nvidia save power function
P.24 Add and NC Q44,R610 for Nvidia save power function reserve
P.34 CAP7 change from 1C-41S0476-M000 to 1C-41R0476-M200 for layout convenient
P.62 Delete BOSS7,BOSS8 for ME request

(2007/06/23)

P.62 H14 change to 1X-HOLE000-0474 for ME request
P.62 H17 change to 1X-HOLE000-0473 for ME request

(2007/06/25)

P.62 Update H14 screw hole pad.
P.34 Change CAP7 to mount, and C275 to no mount for M720 HDD noise issue.
P.38 Update FeliCa pin define for M720 A'SSY issue.
P.49 Add C703,C704 for M720 LAN noise issue.

(2007/06/28)

P.57 Delete PR151 0ohm for application note.
P.58 Change PC67 from 270pF 10% to 270pF 5% for purchase difficult.
P.58 Add TP736, TP737, TP738 and TP739 test pin for application note.
P.56 PL8 change from 1L-DSPD100-4H02 to 1T-00001U5-0000 for layout convenient.

(2007/06/29)

P.22 Delete R569 and add R611 for mirror function off.
P.22 Modify address and command signals of U39 for mirror function off.

(2007/07/02)

P.22 R577,R578,R573,R574 change from 4.3k to 1.05k for nVidia's suggestion.
P.22 R582,R583,R575,R576 change from 4.02k to 1.82k for nVidia's suggestion.
P.22 R584,R585,R579,R580 change from 10k to 2.49k for nVidia's suggestion.
P.28 Add R612 and NC R596,U40 for GPIO3 of GPU is active high which is nVidia's suggestion.

(2007/07/03)

P.37 Change LED4 to HT-110YG for M720 LED issue.
P.51 Change R321,R323 to 51ohm,LED2,LED3 to HT-110Y for M720 LED issue.
P.48 Change F5~F8 to 2.6A poly-switch for M720 USB loading and noise issue.
P.52 Change CN23 to HS-8208E for M720 USB loading and noise issue.

(2007/07/05)

P.11 L28 change to 1uH/220mA for M720 component spec. issue.
P.08 Delete C509 for layout convenient.
P.46 Change L27 to SINKA OD6560T-E900T for purchase difficult.
P.28 NC R612 and mount R596,U40 for GPIO3 of GPU is set active low which is the same as MS90.
P.22 Swap data signals of VRAM for layout convenient.

(2007/07/06)

P.54 Change PC3 from mount to dummy for M720 application note.
P.54 Change PC38 from 4.7uF_25V 0805 to 1uF_25V 0603 for M720 application note.
P.54 Remove PR176 10_J for M720 application note.
P.54 Add PR199, PR200 1_J 1206 and PC201, PC202 4.7uF_25V 0805 for M720 DC_IN RC snubber circuit.
P.38 L25 change from BK1608LL121-T to TB160808B121 for purchase difficult.
P.54 PL1,PL3 change from BLM41PG600SN1L to BCMS451616A600-8A for purchase difficult.
P.05 CAP3 change from EEFSLOD331EY to 2R5TPE330M9 for purchase difficult.
P.12 CAP14 change from EEFSLOD331EY to 2R5TPE330M9 for purchase difficult.

(2007/07/09)

P.54 Change PR199, PR200 form 1206 to 1210 for M720 power rating safety.
P.05 CAP3 change back to EEFSLOD331EY for purchase difficult.
P.12 CAP14 change back to EEFSLOD331EY for purchase difficult.

(2007/07/10)

P.11 L28 change to EBL2012-1R0M 0.25A for M720 component spec. issue.

(2007/07/11)

P.28 Add L55 for M720 EMI issue.
P.41 Delete VR2~VR5 and add C705~C708(NC) for M720 EMI issue.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History (1)			
Size A3	Document Number M730-1-01	Rev 1.0	
Date:	Saturday, October 13, 2007	Sheet	63 of 67

(2007/07/12)

- P.54 Add PJ9 for application.
- P.55 PR170,PR171,PC178,PC179 change to NC for application.
- P.59 PR183,PC189 change to NC for application.
- P.22 Change Q40~Q43 and R575,R576,R582,R583 to NC for customer request.
- P.06 Add C709,C710 and reserve for EMI application.
- P.57 Add PC203~PC210 and reserve for EMI application.
- P.35 Add C711,C712 and reserve for EMI application.
- P.38 Add C713 and reserve for EMI application.

(2007/07/13)

- P.40 Add J2 for EMI application.

(2007/07/16)

- P.42 Change C455,C445 to 10uF,R167,R149 to 20 Kohm for M720 MIC. THD+N issue.
- P.35 Change R382 to mount and R390 to NC for system ID modification.
- P.54 PR199,PR200 change to 1/3 W for PUR issue.

(2007/07/17)

- P.37 Change LED4 to HT-110UYG for M720 MOR request.

(2007/07/20)

- P.41 Change R105 to 6.2Kohm for M720 audio issue.

M730 DVT

(2007/07/27)

- P.48 Delete F6,F8 for MOR's request.
- P.61 Change PD16 from mount to NC, add PR201 0ohm for application.
- P.06 Modify R350 pin1 connection from GND to +3VVRUN for GPU select 27MHz issue.

(2007/08/13)

- P.51 Change LED2,LED3 from HT-110Y to HT-110UY
- Change R319,R322 from 47ohm to 120ohm and R321 from 51ohm to 120ohm
- Change R496 from 47ohm to 100ohm for M720 LED brightness request from MOR

(2007/08/14)

- Add test pin TP740~TP772 for power test jig.

(2007/08/17)

- P.34 Add CAP21 for +5VVRUN noise issue of ODD
- P.41 Add CAP22 for +5VAMP noise issue of CODEC
- C127 change from no mount to mount for +5VAMP noise issue of CODEC
- P.25 Add C714/C715 for PEX_PLL_AVDD/PEX_PLL_DVDD noise issue

(2007/08/23)

- P.38 NC R152,R151,F2,L25,C185,C186,CN6 for no Felica SKU
- P.44 U27 change from GMT G781-1P8f to SMSC EMC1402-2-ACZL for Penryn CPU concern

(2007/08/25)

- P.62 H3 change to 1X-HOLE000-0519 for ME's request

(2007/08/28)

- P.55 PL11,PL12 change from SPD1004HT4R7N-8A to PCMC063T-4R7MN for ME interference issue.
- P.55 PR170,PR171,PC178,PC179 change from NC to mount for EMI issue.
- P.57 PR145 change from 3.3ohm to 4.7ohm and PC131 change from 1000P to 680P for EMI issue.

(2007/08/28)

- P.35 Add and reserve C716,C717,C718 0603 cap for EMI solution.
- P.55 Add and reserve PC211,PC212 0603 cap for EMI solution.
- P.57 Add and reserve PC213 0603 cap for EMI solution.
- P.58 Add and reserve PC214~PC218 0603 cap for EMI solution.

M730 PVT

(2007/09/27)

- P.54 Delete PJ9 for application.
- P.54 Change PD6 from mount to NC for UL_Lock issue.
- P.54 Delete PR25, PR41, PR42 for application.
- P.55 PL11,PL12 change from PCMC063T-4R7MN to SPD1004HT4R7N-8A for MOR request.
- P.55 Delete PJ4, PJ5 for application.
- P.55 Delete PR155, PR156, PR162, PR163, PR167 for application.
- P.56 Delete PJ1, PJ2 for application.
- P.56 Delete PR129 for application.
- P.57 Delete PJ3 for application.
- P.58 Delete PR70, PR71, PR84, PR86, PR90, PR93, PR94, PR96, PR97, PR99, PR102 for application.
- P.59 Delete PJ6, PJ7 for application.
- P.59 Delete PR177, PR197, PR198 for application.
- P.60 Delete PR110, PR111, PR114 for application.
- P.61 Delete PR20, PR49 for application.

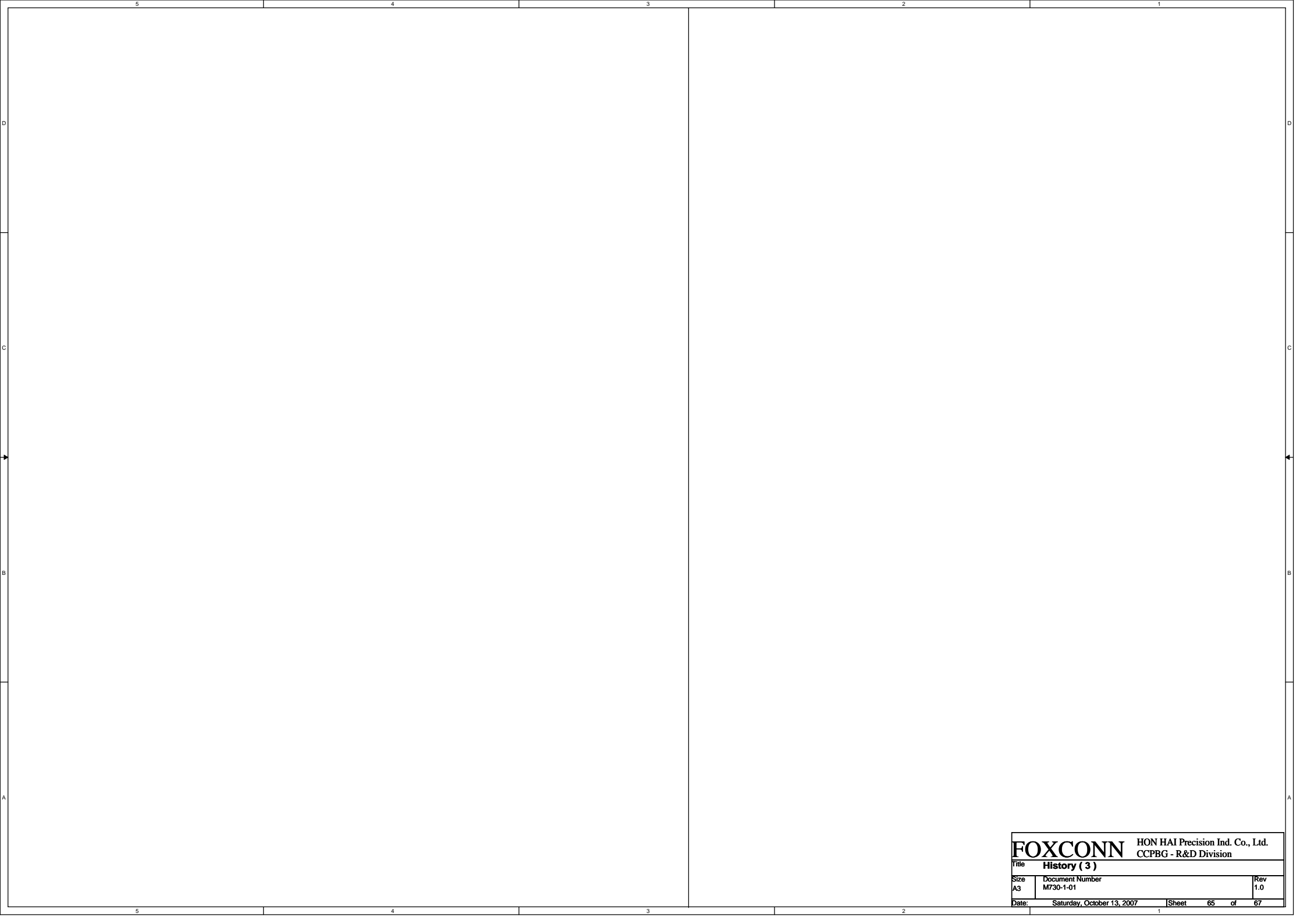
(2007/10/17)

- P.25 Add netname "J6" for U35 Pin J6 for application.

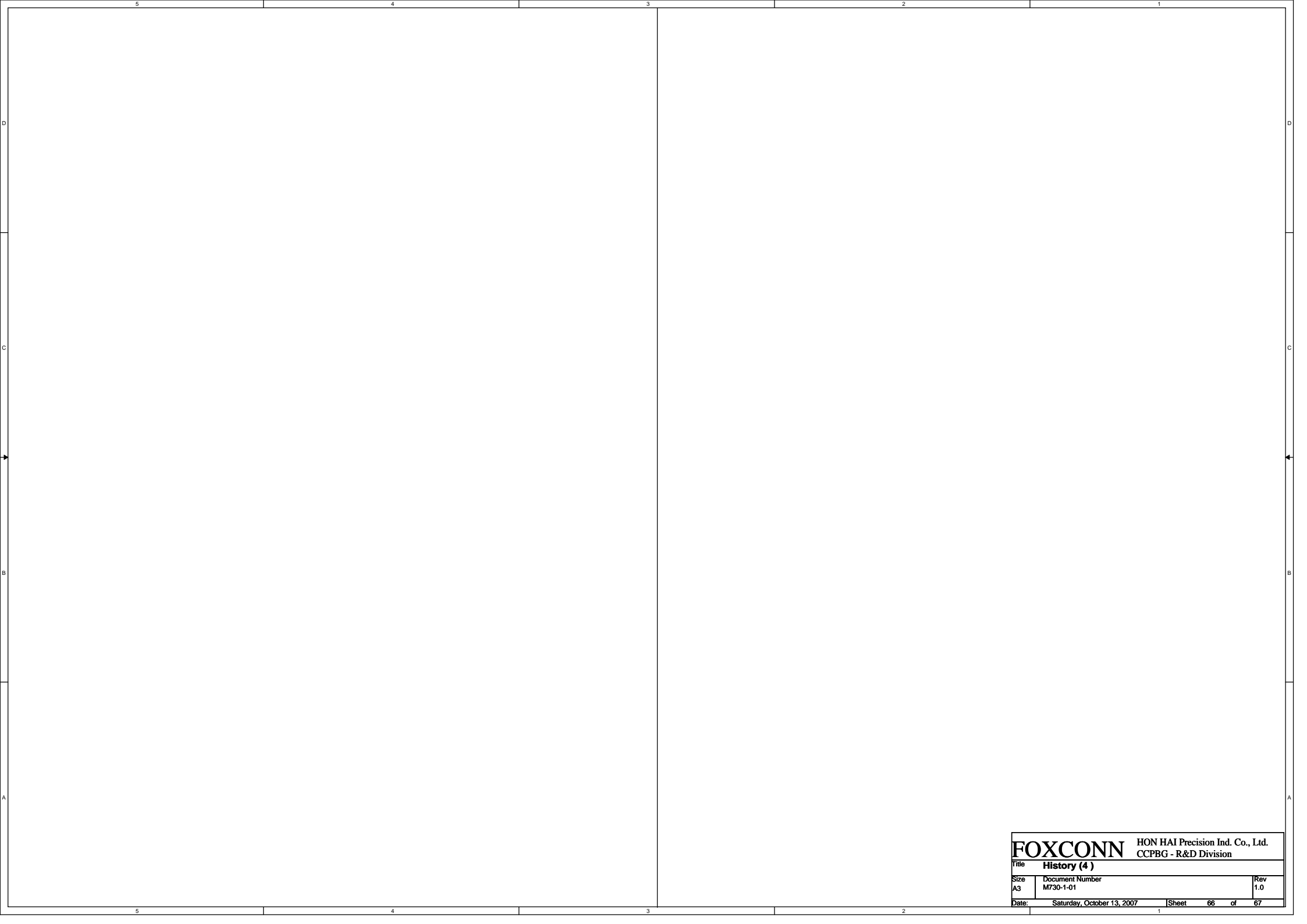
(2007/10/19)

- P.47 Change R235 from 47ohm to 68ohm for MS Card Media-C MS_CLK undershoot issue

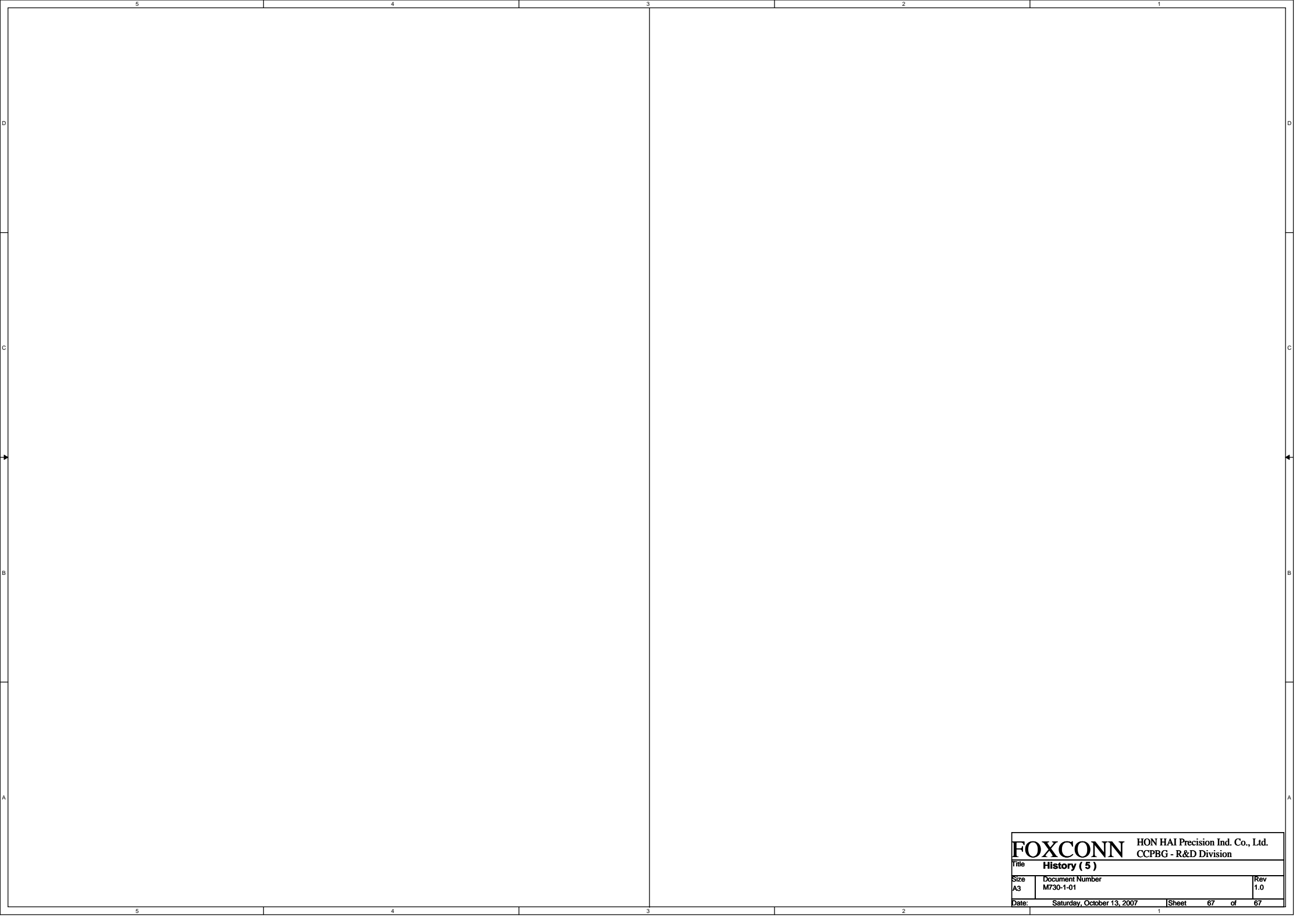
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
History (2)			
Title	M730-1-01		Rev 1.0
Size	A3		
Date:	Friday, October 19, 2007	Sheet	64 of 67



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	History (3)	
Size	Document Number	Rev
A3	M730-1-01	1.0
Date:	Saturday, October 13, 2007	Sheet 65 of 67



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	History (4)	
Size	Document Number	Rev
A3	M730-1-01	1.0
Date:	Saturday, October 13, 2007	Sheet 66 of 67



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	History (5)	
Size	Document Number	Rev
A3	M730-1-01	1.0
Date:	Saturday, October 13, 2007	Sheet 67 of 67