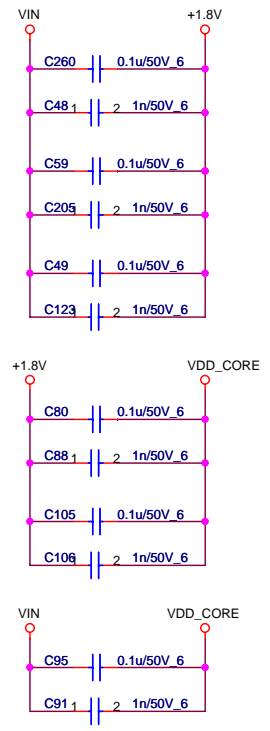
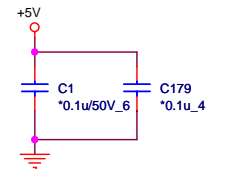


STITCH CAPACITORS

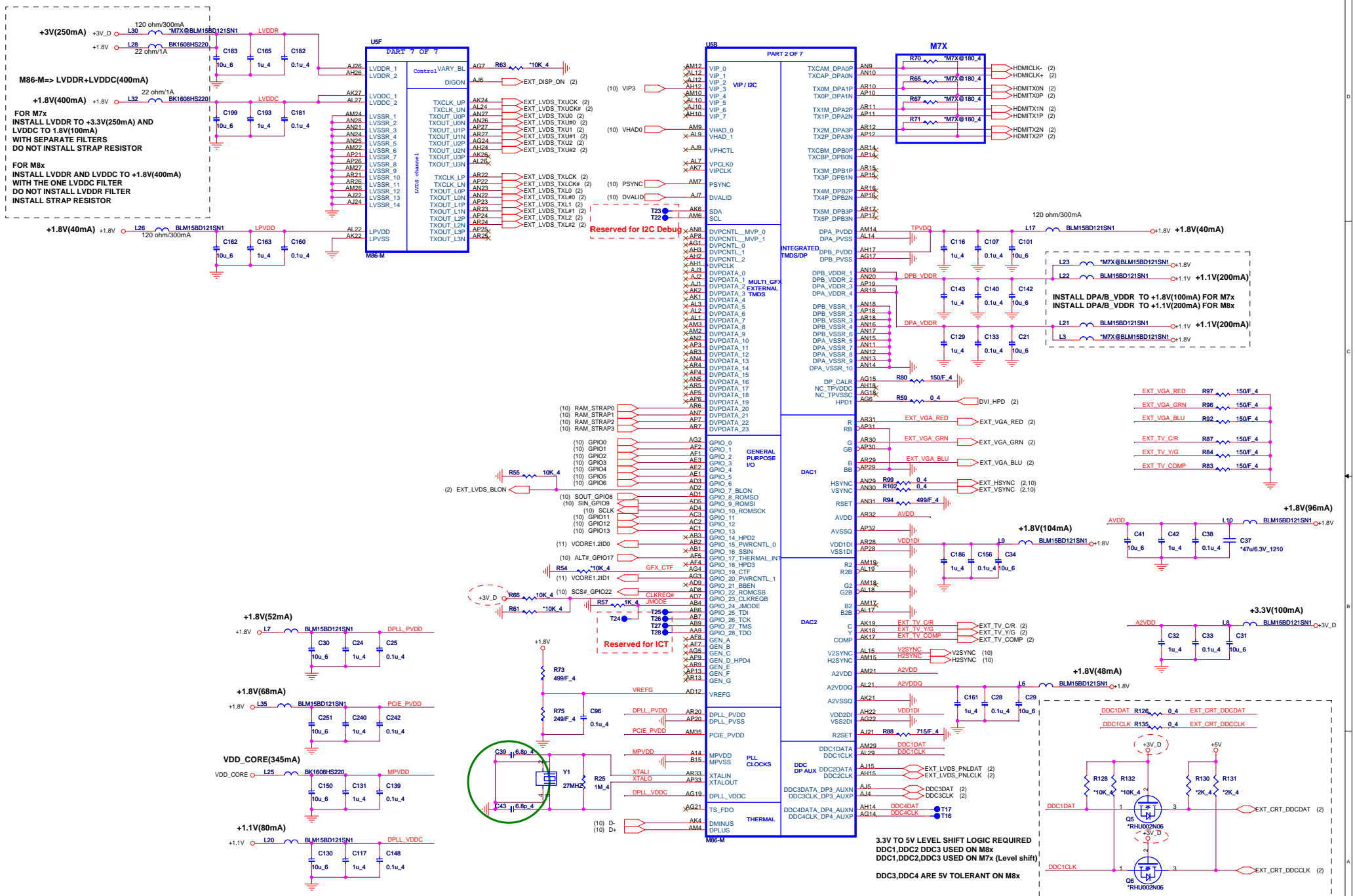


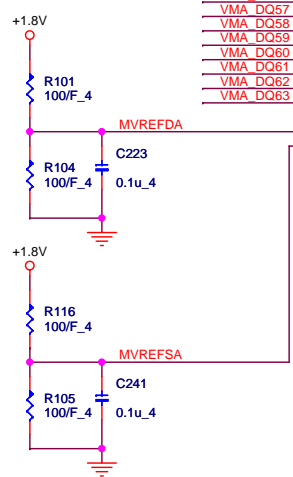
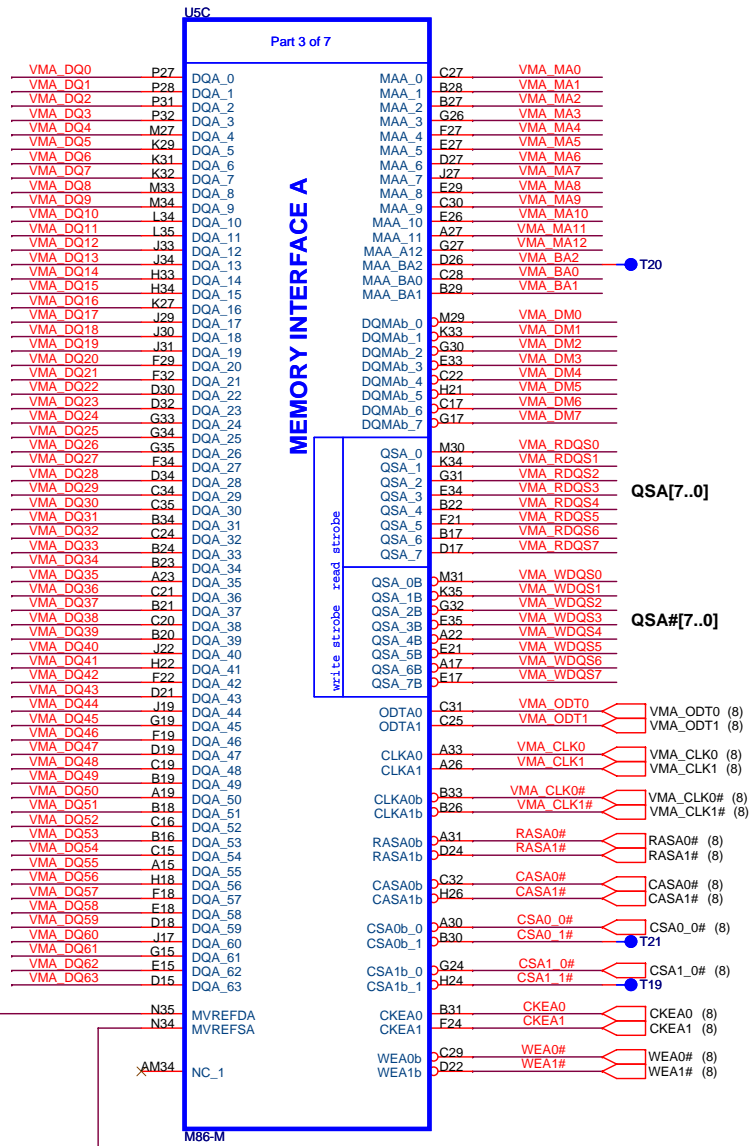
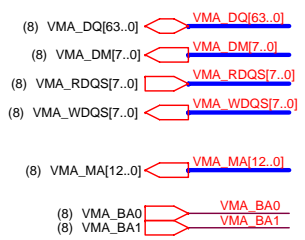
EMI CAP.



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Quanta Computer Inc.

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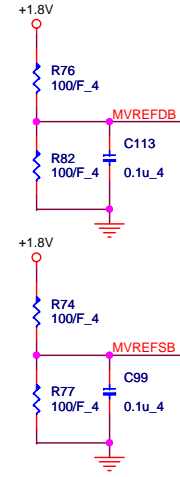
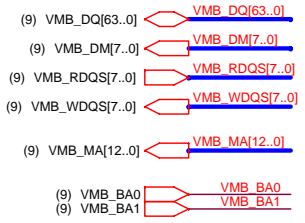


DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

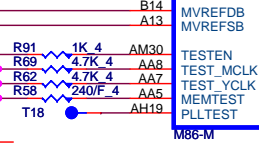
0.5*VDDQ 0.713*VDDQ

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Quanta Computer Inc.

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	GFX(MEM I/F 1/2)	1A
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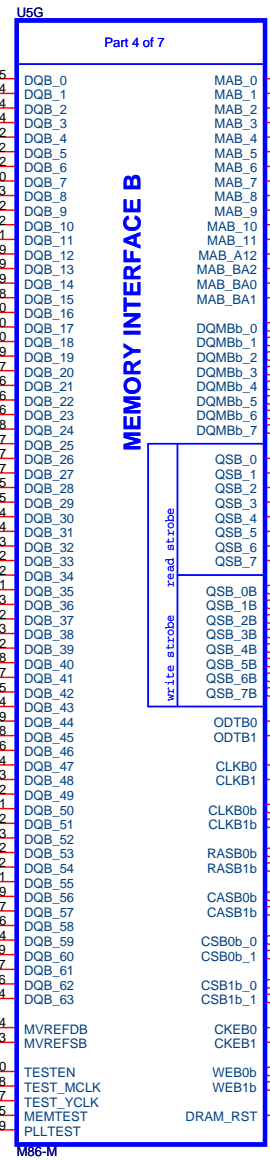


VMB DQ0	H15	DQB_0
VMB DQ1	G14	DQB_1
VMB DQ2	F14	DQB_2
VMB DQ3	D14	DQB_3
VMB DQ4	H12	DQB_4
VMB DQ5	G12	DQB_5
VMB DQ6	F12	DQB_6
VMB DQ7	D10	DQB_7
VMB DQ8	B13	DQB_8
VMB DQ9	C12	DQB_9
VMB DQ10	B12	DQB_10
VMB DQ11	B11	DQB_11
VMB DQ12	C8	DQB_12
VMB DQ13	B9	DQB_13
VMB DQ14	A9	DQB_14
VMB DQ15	B8	DQB_15
VMB DQ16	J10	DQB_16
VMB DQ17	H10	DQB_17
VMB DQ18	F10	DQB_18
VMB DQ19	D9	DQB_19
VMB DQ20	G7	DQB_20
VMB DQ21	G6	DQB_21
VMB DQ22	F6	DQB_22
VMB DQ23	D6	DQB_23
VMB DQ24	C5	DQB_24
VMB DQ25	C7	DQB_25
VMB DQ26	B7	DQB_26
VMB DQ27	A7	DQB_27
VMB DQ28	B5	DQB_28
VMB DQ29	A5	DQB_29
VMB DQ30	C4	DQB_30
VMB DQ31	B4	DQB_31
VMB DQ32	M3	DQB_32
VMB DQ33	M2	DQB_33
VMB DQ34	N2	DQB_34
VMB DQ35	N1	DQB_35
VMB DQ36	R3	DQB_36
VMB DQ37	R2	DQB_37
VMB DQ38	T3	DQB_38
VMB DQ39	T2	DQB_39
VMB DQ40	M8	DQB_40
VMB DQ41	M7	DQB_41
VMB DQ42	P5	DQB_42
VMB DQ43	P4	DQB_43
VMB DQ44	R9	DQB_44
VMB DQ45	R8	DQB_45
VMB DQ46	R6	DQB_46
VMB DQ47	U4	DQB_47
VMB DQ48	U3	DQB_48
VMB DQ49	U2	DQB_49
VMB DQ50	U1	DQB_50
VMB DQ51	Y2	DQB_51
VMB DQ52	Y3	DQB_52
VMB DQ53	Y2	DQB_53
VMB DQ54	AA2	DQB_54
VMB DQ55	AA1	DQB_55
VMB DQ56	U9	DQB_56
VMB DQ57	U7	DQB_57
VMB DQ58	U6	DQB_58
VMB DQ59	V4	DQB_59
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VMB DQ62	W6	DQB_62
VMB DQ63	W4	DQB_63

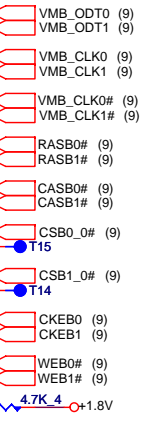
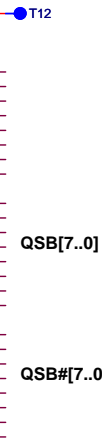


DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

0.5*VDDQ 0.713*VDDQ

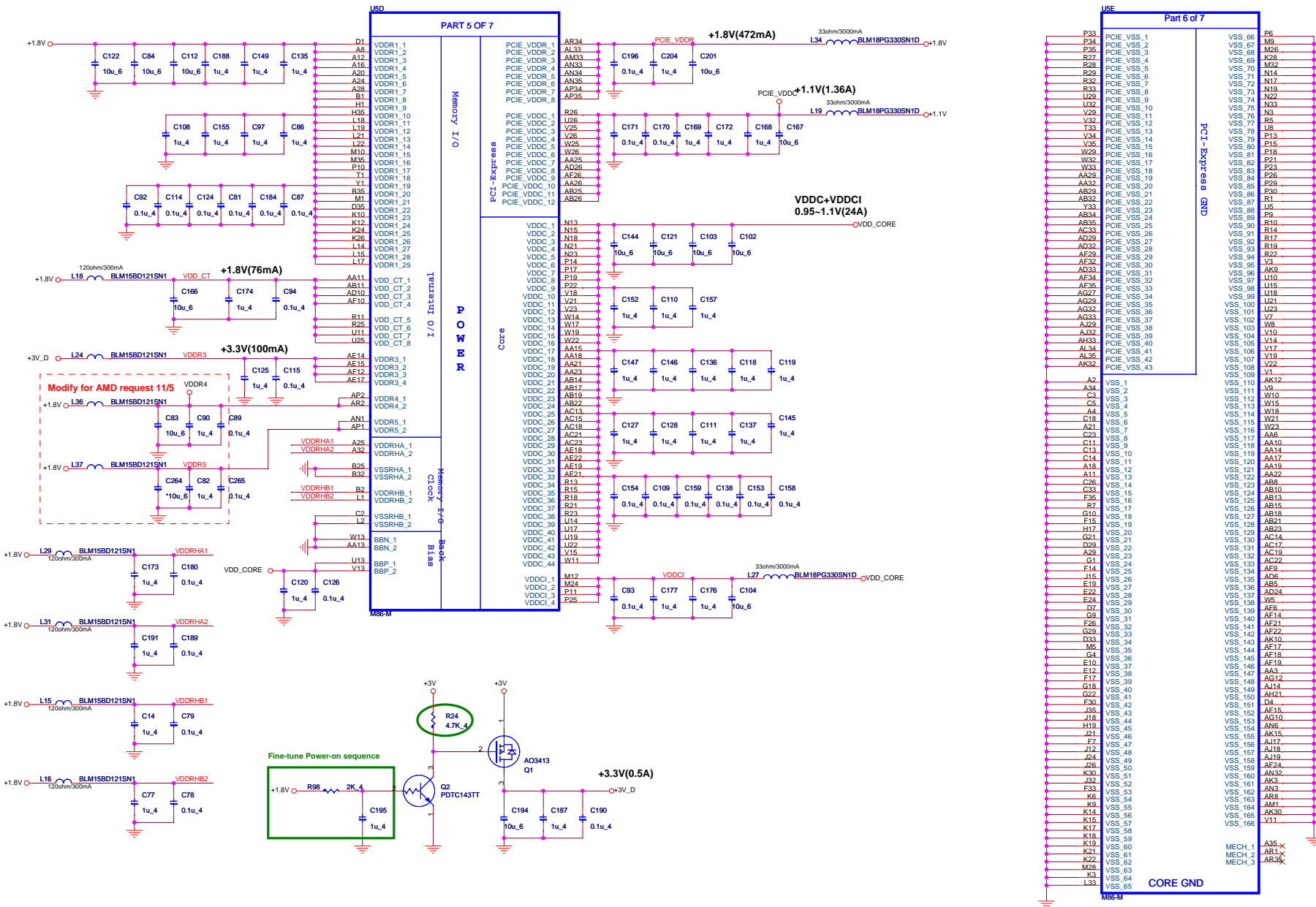


MAB_0	H2	VMB MA0
MAB_1	H3	VMB MA1
MAB_2	J3	VMB MA2
MAB_3	J5	VMB MA3
MAB_4	J4	VMB MA4
MAB_5	J6	VMB MA5
MAB_6	G5	VMB MA6
MAB_7	J9	VMB MA7
MAB_8	F3	VMB MA8
MAB_9	F4	VMB MA9
MAB_10	J1	VMB MA10
MAB_11	J2	VMB MA11
MAB_A12	J7	VMB MA12
MAB_BA2	F1	VMB BA2
MAB_BA0	G2	VMB BA0
MAB_BA1	G3	VMB BA1
DQMBb_0	D12	VMB DM0
DQMBb_1	C10	VMB DM1
DQMBb_2	E7	VMB DM2
DQMBb_3	C6	VMB DM3
DQMBb_4	P3	VMB DM4
DQMBb_5	R4	VMB DM5
DQMBb_6	W3	VMB DM6
DQMBb_7	V8	VMB DM7
QSB_0	J14	VMB RDQS0
QSB_1	B10	VMB RDQS1
QSB_2	F9	VMB RDQS2
QSB_3	B6	VMB RDQS3
QSB_4	P2	VMB RDQS4
QSB_5	P8	VMB RDQS5
QSB_6	W2	VMB RDQS6
QSB_7	V6	VMB RDQS7
QSB_0B	H14	VMB WDQS0
QSB_1B	A10	VMB WDQS1
QSB_2B	E9	VMB WDQS2
QSB_3B	A6	VMB WDQS3
QSB_4B	P1	VMB WDQS4
QSB_5B	P7	VMB WDQS5
QSB_6B	W1	VMB WDQS6
QSB_7B	V5	VMB WDQS7
ODTB0	D2	VMB ODT0
ODTB1	K5	VMB ODT1
CLKB0	A3	VMB CLK0
CLKB1	K1	VMB CLK1
CLKB0b	B3	VMB CLK0#
CLKB1b	K2	VMB CLK1#
RASB0b	D3	RASB0#
RASB1b	K7	RASB1#
CASB0b	C1	CASB0#
CASB1b	K4	CASB1#
CSB0b_0	E1	CSB0_0#
CSB0b_1	E2	CSB0_1#
CSB1b_0	L3	CSB1_0#
CSB1b_1	M4	CSB1_1#
CKEB0	E3	CKEB0
CKEB1	K8	CKEB1
WEB0b	F2	WEB0#
WEB1b	M6	WEB1#



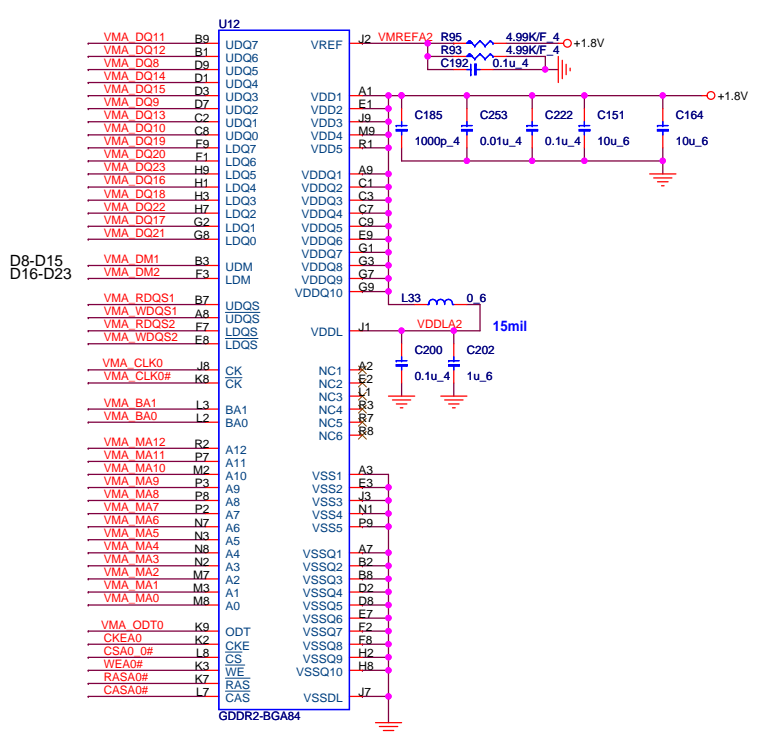
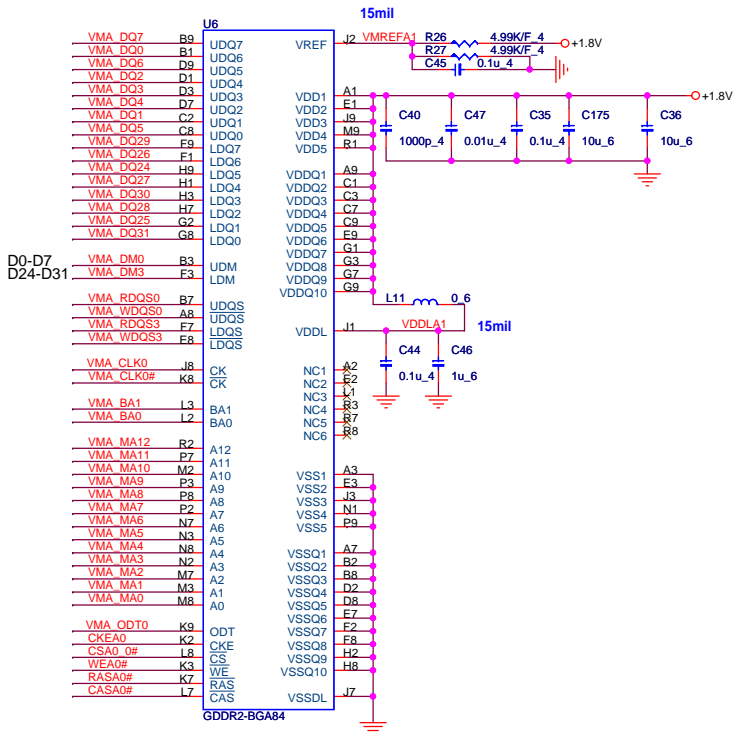
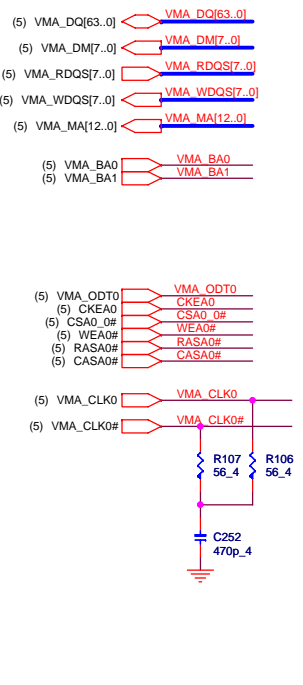
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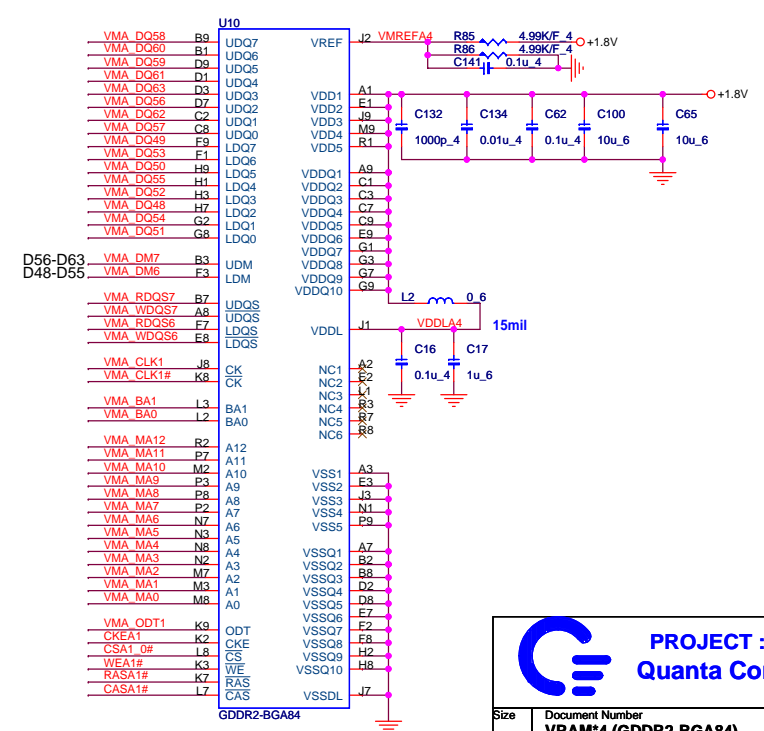
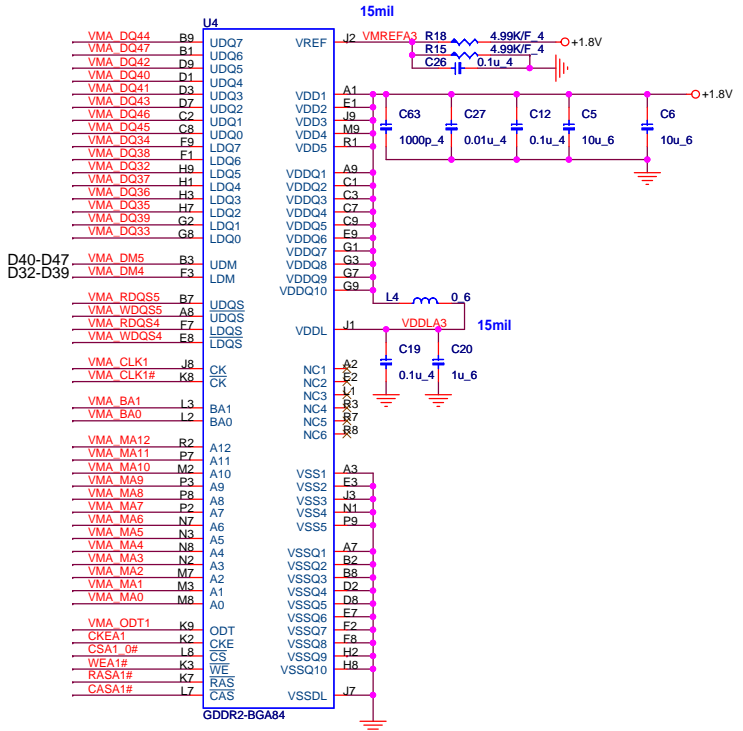
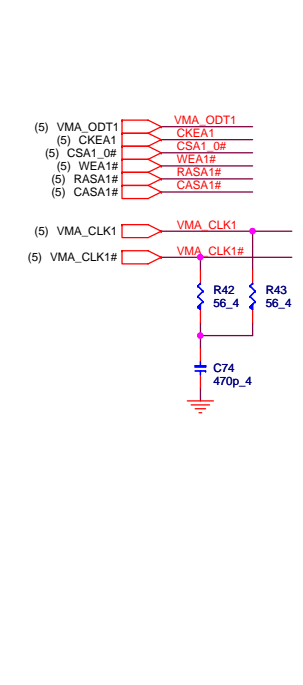


Part 6 of 7		
P33	PCIE_VSS_1	VSS_66
P34	PCIE_VSS_2	VSS_67
P35	PCIE_VSS_3	VSS_68
R27	PCIE_VSS_4	VSS_69
R28	PCIE_VSS_5	VSS_70
R29	PCIE_VSS_6	VSS_71
R32	PCIE_VSS_7	VSS_72
R33	PCIE_VSS_8	VSS_73
U29	PCIE_VSS_9	VSS_74
U32	PCIE_VSS_10	VSS_75
Y29	PCIE_VSS_11	VSS_76
Y32	PCIE_VSS_12	VSS_77
T33	PCIE_VSS_13	VSS_78
V34	PCIE_VSS_14	VSS_79
W32	PCIE_VSS_15	VSS_80
W29	PCIE_VSS_16	VSS_81
W32	PCIE_VSS_17	VSS_82
AA29	PCIE_VSS_18	VSS_83
AA32	PCIE_VSS_19	VSS_84
AB29	PCIE_VSS_20	VSS_85
AB32	PCIE_VSS_21	VSS_86
AB34	PCIE_VSS_22	VSS_87
AB33	PCIE_VSS_23	VSS_88
AB34	PCIE_VSS_24	VSS_89
AB35	PCIE_VSS_25	VSS_90
AC33	PCIE_VSS_26	VSS_91
AD29	PCIE_VSS_27	VSS_92
AD33	PCIE_VSS_28	VSS_93
AE29	PCIE_VSS_29	VSS_94
AE32	PCIE_VSS_30	VSS_95
AD33	PCIE_VSS_31	VSS_96
AE34	PCIE_VSS_32	VSS_97
AE35	PCIE_VSS_33	VSS_98
AG27	PCIE_VSS_34	VSS_99
AG29	PCIE_VSS_35	VSS_100
AG33	PCIE_VSS_36	VSS_101
AG33	PCIE_VSS_37	VSS_102
AJ29	PCIE_VSS_38	VSS_103
AJ32	PCIE_VSS_39	VSS_104
AH33	PCIE_VSS_40	VSS_105
AL34	PCIE_VSS_41	VSS_106
AL35	PCIE_VSS_42	VSS_107
AK32	PCIE_VSS_43	VSS_108
A2	VSS_1	VSS_109
A34	VSS_2	VSS_110
C3	VSS_3	VSS_111
C3	VSS_4	VSS_112
C3	VSS_5	VSS_113
A4	VSS_6	VSS_114
C18	VSS_7	VSS_115
A21	VSS_8	VSS_116
C23	VSS_9	VSS_117
C11	VSS_10	VSS_118
C14	VSS_11	VSS_119
A18	VSS_12	VSS_120
A11	VSS_13	VSS_121
C26	VSS_14	VSS_122
C33	VSS_15	VSS_123
F35	VSS_16	VSS_124
R7	VSS_17	VSS_125
G10	VSS_18	VSS_126
F15	VSS_19	VSS_127
H17	VSS_20	VSS_128
G21	VSS_21	VSS_129
D29	VSS_22	VSS_130
A29	VSS_23	VSS_131
G1	VSS_24	VSS_132
F14	VSS_25	VSS_133
H15	VSS_26	VSS_134
E19	VSS_27	VSS_135
E22	VSS_28	VSS_136
E22	VSS_29	VSS_137
E24	VSS_30	VSS_138
D7	VSS_31	VSS_139
G9	VSS_32	VSS_140
F26	VSS_33	VSS_141
G29	VSS_34	VSS_142
D33	VSS_35	VSS_143
M5	VSS_36	VSS_144
G4	VSS_37	VSS_145
E10	VSS_38	VSS_146
E12	VSS_39	VSS_147
F17	VSS_40	VSS_148
G18	VSS_41	VSS_149
G22	VSS_42	VSS_150
F30	VSS_43	VSS_151
J35	VSS_44	VSS_152
H18	VSS_45	VSS_153
H19	VSS_46	VSS_154
J21	VSS_47	VSS_155
F7	VSS_48	VSS_156
J22	VSS_49	VSS_157
J24	VSS_50	VSS_158
J32	VSS_51	VSS_159
K30	VSS_52	VSS_160
F33	VSS_53	VSS_161
K6	VSS_54	VSS_162
K9	VSS_55	VSS_163
K14	VSS_56	VSS_164
K15	VSS_57	VSS_165
K17	VSS_58	VSS_166
K18	VSS_59	
K19	VSS_60	
K21	VSS_61	
M28	VSS_62	
K3	VSS_63	
L33	VSS_64	
VSS_65		

Channel A-1

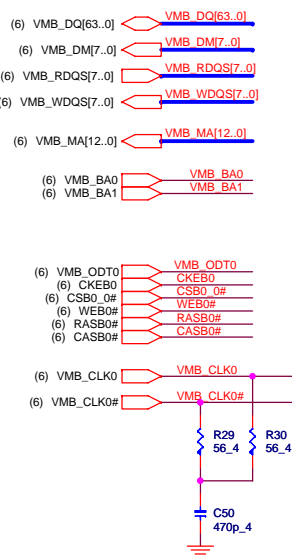


Channel A-1

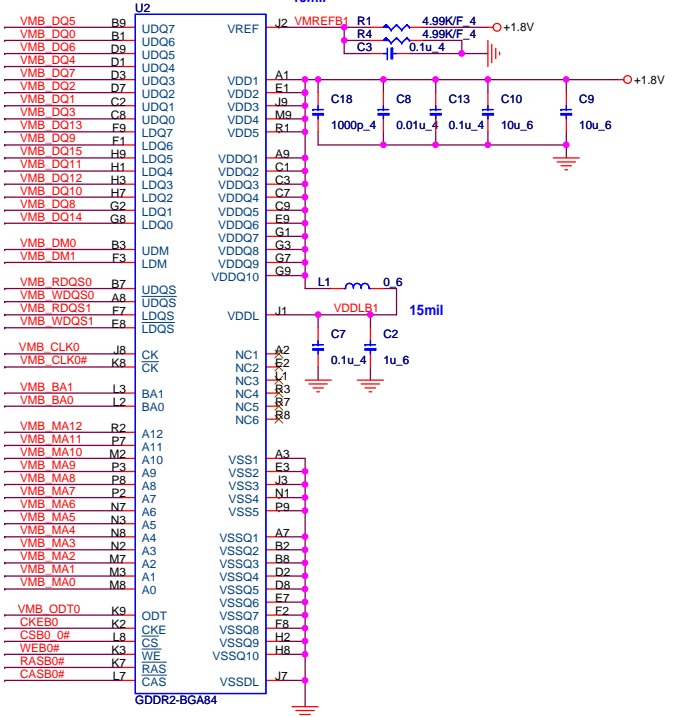


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VRAM*4 (GDDR2-BGA84)
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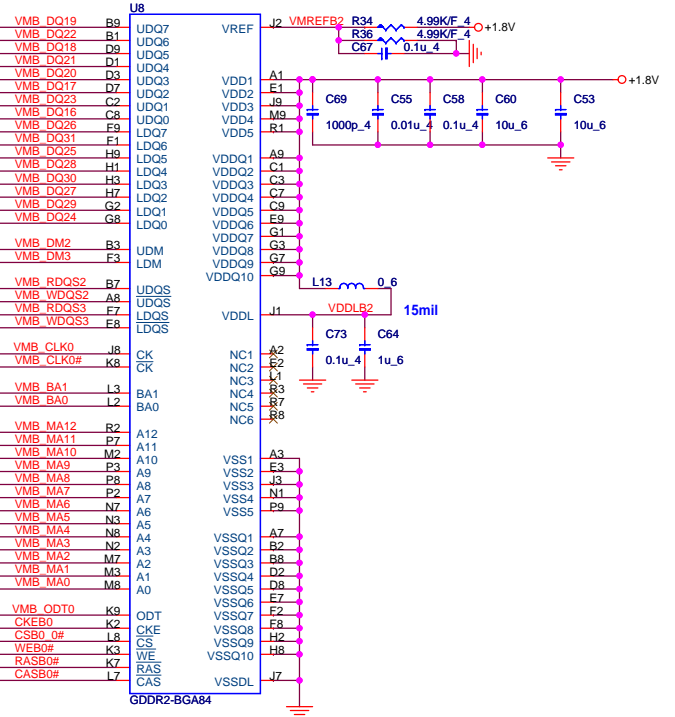
Channel B-1



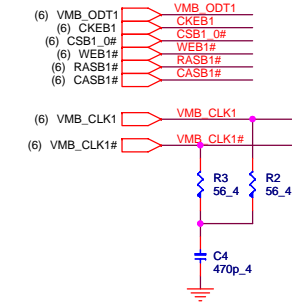
D0-D7
D8-D15



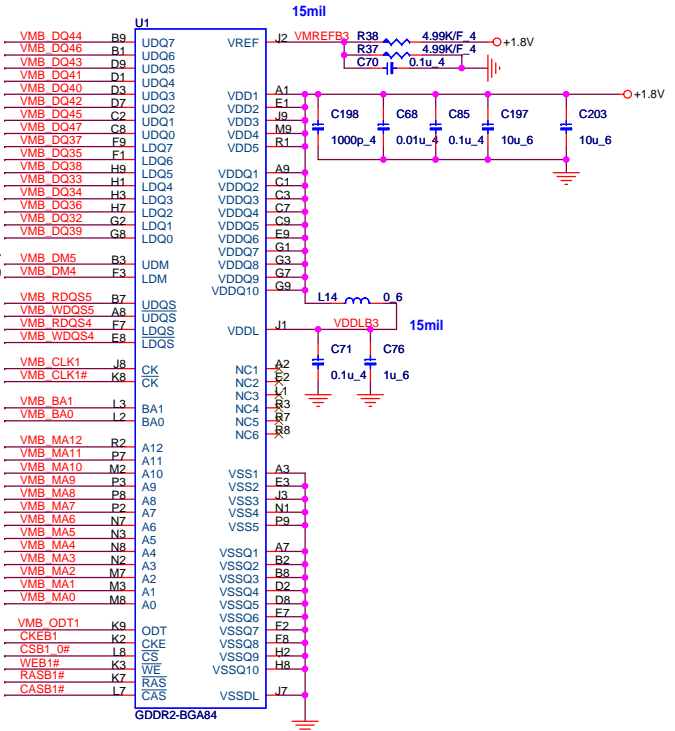
D16-D23
D24-D31



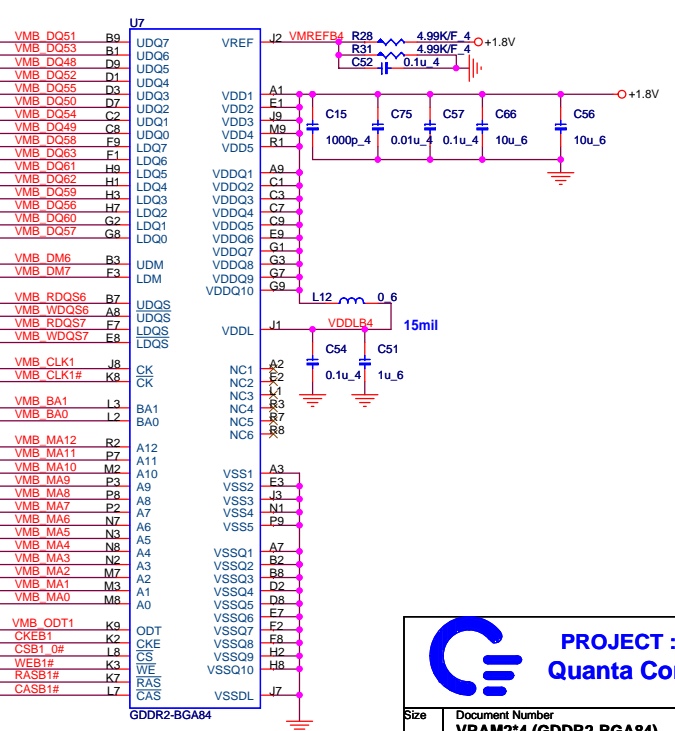
Channel B-2




D40-D47
D32-D39



D48-D55
D56-D63



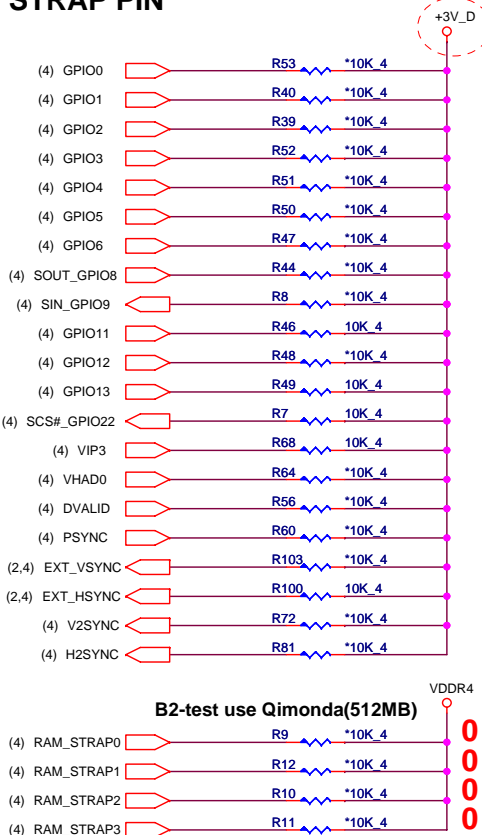


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hexaint@hotmail.com

STRAP PIN



CONFIGURATION STRAPS

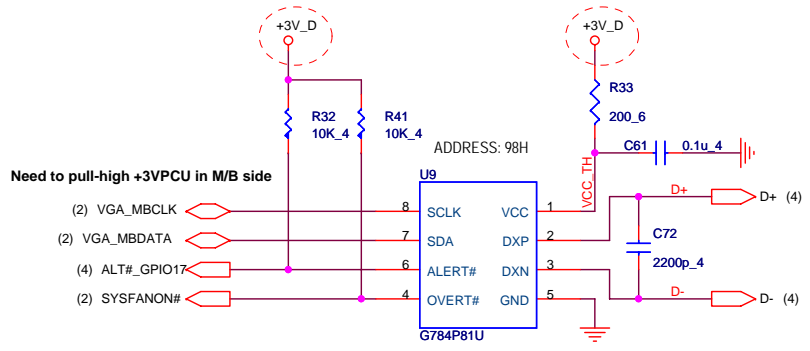
RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE
 RSVD = ATI RESERVED
 (DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7x/M8x-M)	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82-S)	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0	0
BIF_VGA_DIS	PSYNC	VGA ENABLED	0	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

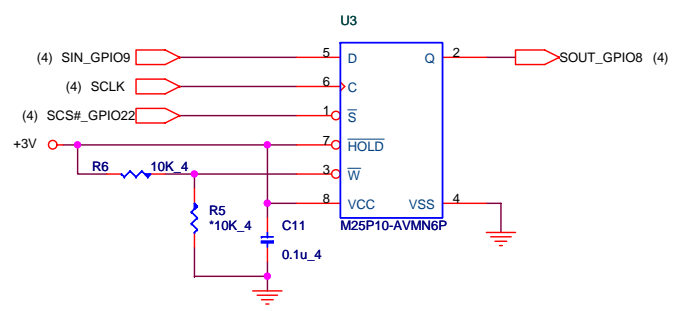
M86-DDR2 Memory Aperture size

Vendor	Size	RAM_STRAP3 DVPDATA_23	RAM_STRAP2 DVPDATA_22	RAM_STRAP1 DVPDATA_21	RAM_STRAP0 DVPDATA_20
Samsung	128M				
	256M				
	512M				
Hynix	128M	0	1	1	0
	256M	0	1	0	1
	512M	0	1	0	0
Qimonda (500MHz)	128M	0	0	1	0
	256M	0	0	0	1
	512M	0	0	0	0

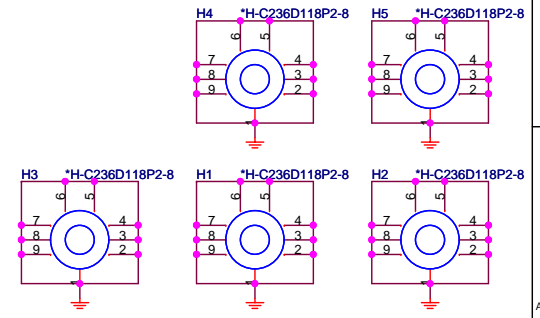
Thermal Sensor



Flash ROM



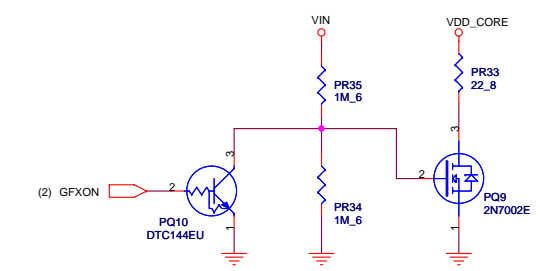
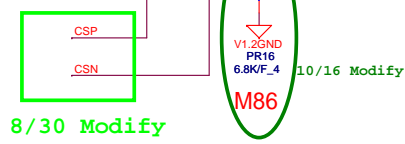
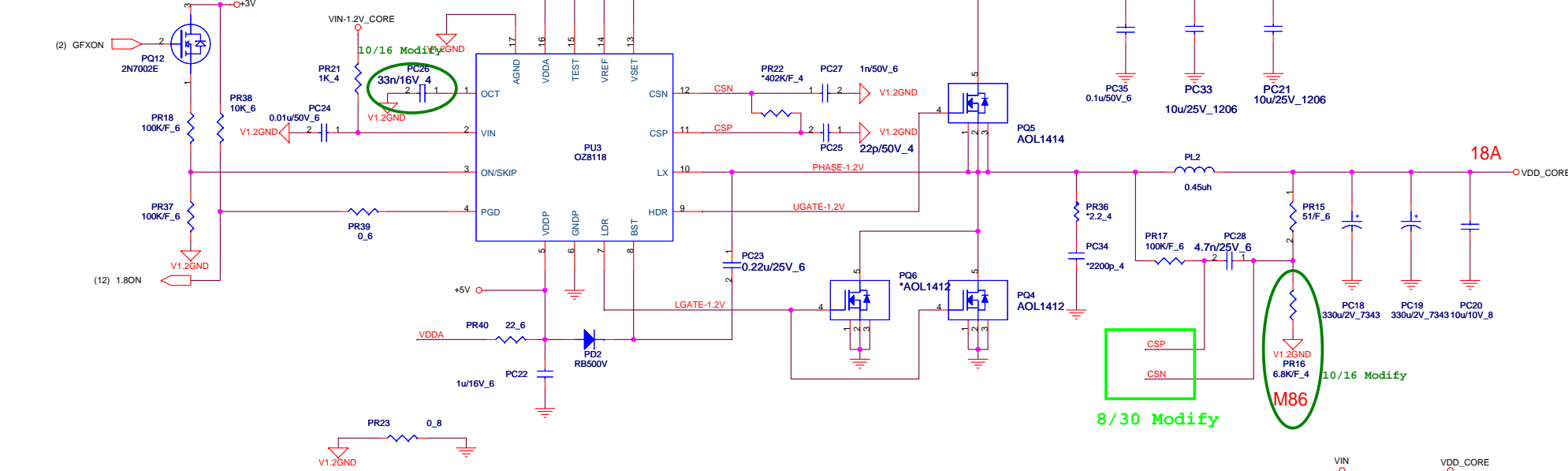
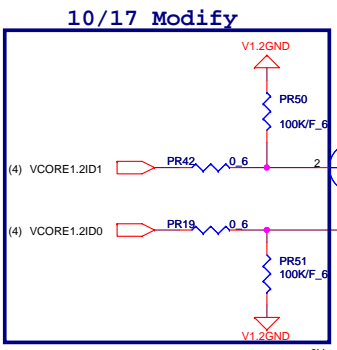
Hole



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VID[1:0]		VOUT1	INPUTS		OUTPUTS			VOUT1
VID1	VID0		G1	G0	OD1	OD2	OD3	
0	0	1.2V	0	0	$0.75 \times (1 + R1/R2 + R1/R3 + R1/R4)$			1.2V
0	1	1.1V	1	0	$0.75 \times (1 + R1/R2 + R1/R3)$			1.1V
1	0	1.0V	0	1	$0.75 \times (1 + R1/R2 + R1/R4)$			1.0V
1	1	0.9V	1	1	$0.75 \times (1 + R1/R2)$			0.9V

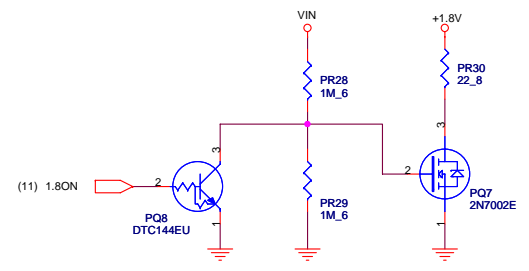
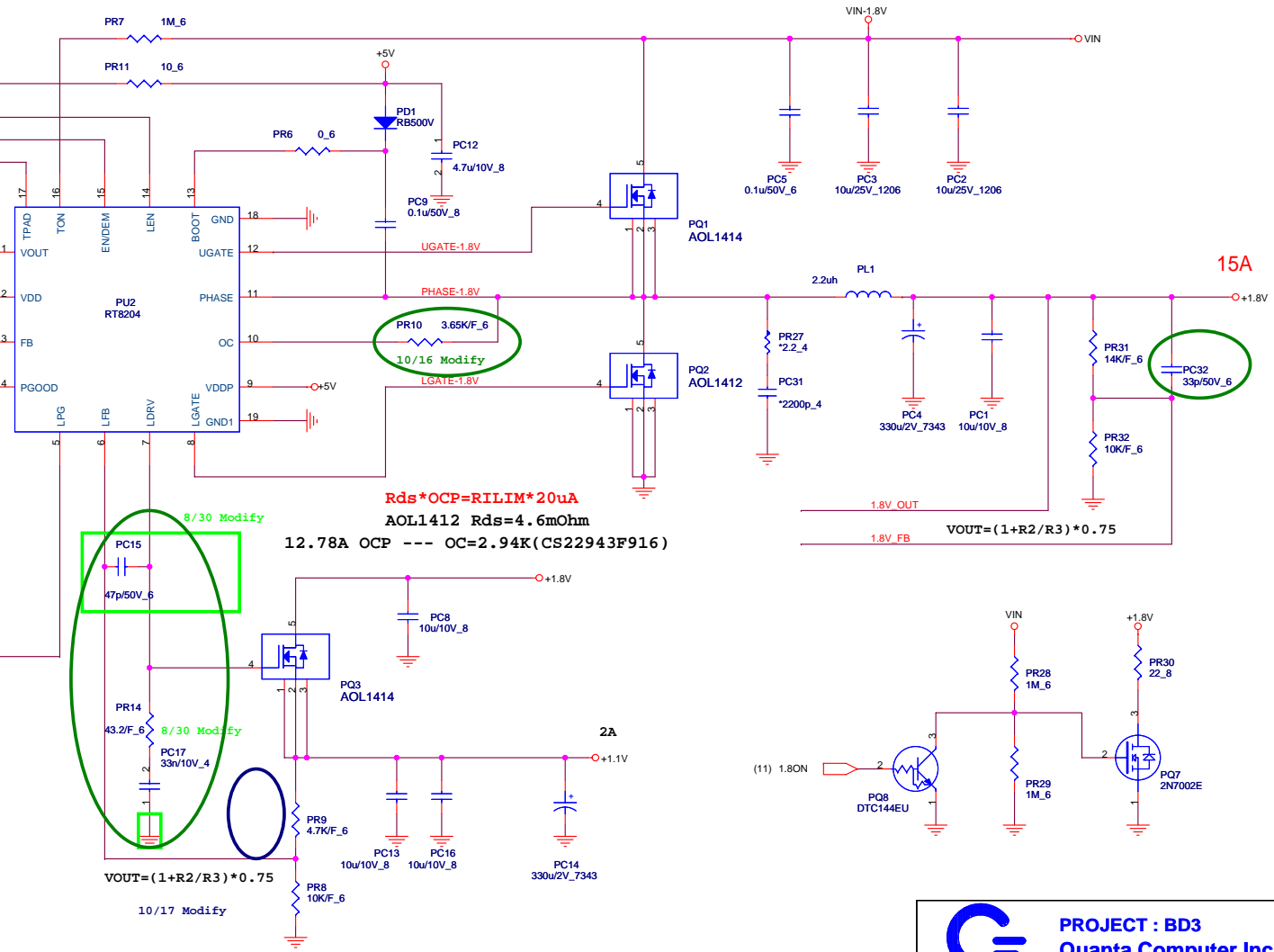
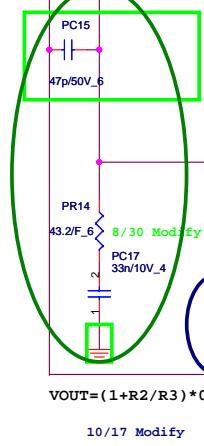
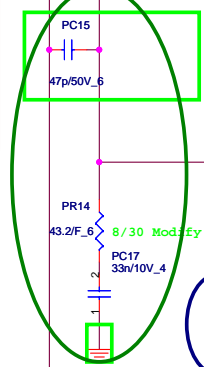
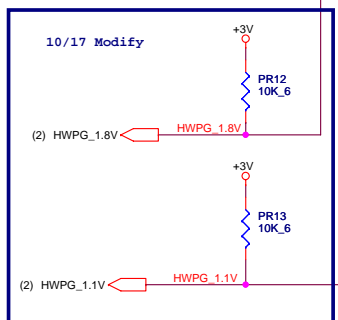
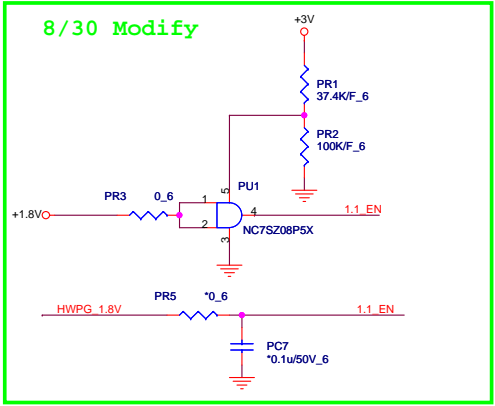
MCP67 TABLE

Set


PROJECT : BD3
Quanta Computer Inc.

Size: Document Number
1.2V_CORE (OZ8118)

Date: Monday, November 12, 2007 Sheet 11 of 12 Rev 1D



Model	REV	CHANGE LIST	MODEL	BD3 VGA/B	
				FROM	To
BD3 VGA/B	1A	FIRST RELEASED: E200710-1822 (PCB: DABD3UB18A0)		X	1A
	2A	2ND RELEASED: E200710-3032 (PCB: DABD3UB18B0) Page02 : Add AND gate circuit (U13/R136/R137/R138/C263) to fine-tune power-good signal Page04 : Because GPIO_19 (temp_fail) output high level, change pull-up to pull-down (reserve) ==>Don't highlight to customer Change C39/C43 from 15pf to 6.8pf (CH-686T0B07) for 27Mhz frequency correction Page07 : Change R98 (2Kohm)/C195(1uf) to fine-tune power-on sequence for +3V_D Power circuit (Pagell-12) 1. Change PC26 from original P/N: CH02206JB08 Value: 22p/25V_4 to final P/N: CH33303ZB30 Value: 33n/16V_4. 2. Change PC15 from original P/N: CH5103K9901 Value: 1u/16V_6 to final P/N: CH04706K909 Value: 47p/50V_6. 3. Change PR14 from original P/N: CS11003F953 Value: 100/F_6_4 to final P/N: CS04323F909 Value: 43.2/F_6. 4. Change PC17 from original P/N: CH23306JB16 Value: 3.3n/50V_4 to final P/N: CH33302KB12 Value: 33n/10V_4. 5. Remove PC11 original P/N: CH41006K911 Value: 0.1u/50V_6 6. Add PC14 original P/N: CH733RM8858 Value: 330u/2V_7343 7. Change PR16 from original P/N: CS21912FB13 Value: 1.91K/F_4 to final P/N: CS26802FB19 Value: 6.8K/F_4. 8. Change PR10 from original P/N: CS22943F916 Value: 2.94K/F_6 to final P/N: CS23653F912 Value: 3.65K/F_6. 9. Change PC26 from original P/N: CH3334K1B00 Value: 33n/25V_4 to final P/N: CH33303ZB30 Value: 33n/16V_4. 10.Add PC32 to final P/N: CH03306J905 Value: 33p/50V_6		X	1A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
		1A	2A		
		1A	2A		
		1A	2A		
		1A	2A		
2B	3RD RELEASED: E2007??-???? (PCB: DABD3UB18C0) Page02/04/10 : Change +3V to +3V_D (delayed 3.3V) power rail to avoid leakage during power-up for DDC/GPIO Page04 : Add test point (T22/T23) at SDA/SCL for I2C Debug access Add test point (T24/25/26/27/28) for GPU boundary scan test Page07 : Add bead(L36/L37) to separate VDDR4 and VDDR5 power for AMD request Page10 : Change DVPDATA[20..23] pull-up to VDDR4(+1.8V)		2A	2B	
			2A	2B	
			2A	2B	
			2A	2B	
			2A	2B	
3A					

 PROJECT : BD3
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Size Document Number Rev
Change list 2B
Date: Thursday, November 15, 2007 Sheet 13 of 13

DOC NO.	PROJECT MODEL :	BD3 VGA/B	APPROVED BY:		DATE:	2007/11/05
	PART NUMBER:		DRAWING BY:		REVISION:	2B