

PWWAA

LC Marseille

LA-6842P REV 0.2 Schematic

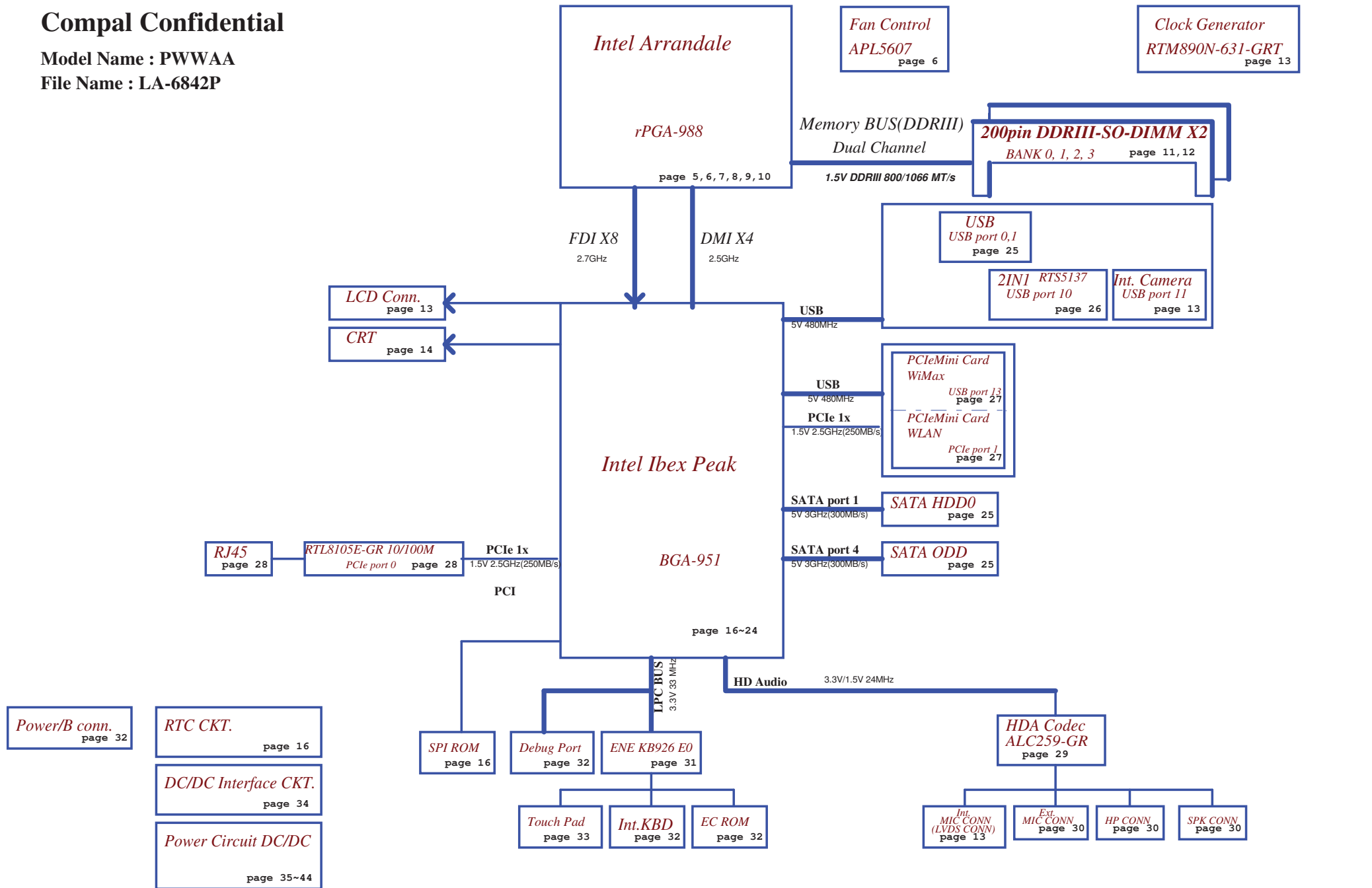
Intel Processor (ARD) /PCH (HM55)
2010-07-22 Rev 0.2

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Issued Date	2010/06/21	Deciphered Date	2011/06/21	Title	Cover Page	
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				Date: Wednesday, July 28, 2010	Sheet 1 of 45	

Compal Confidential

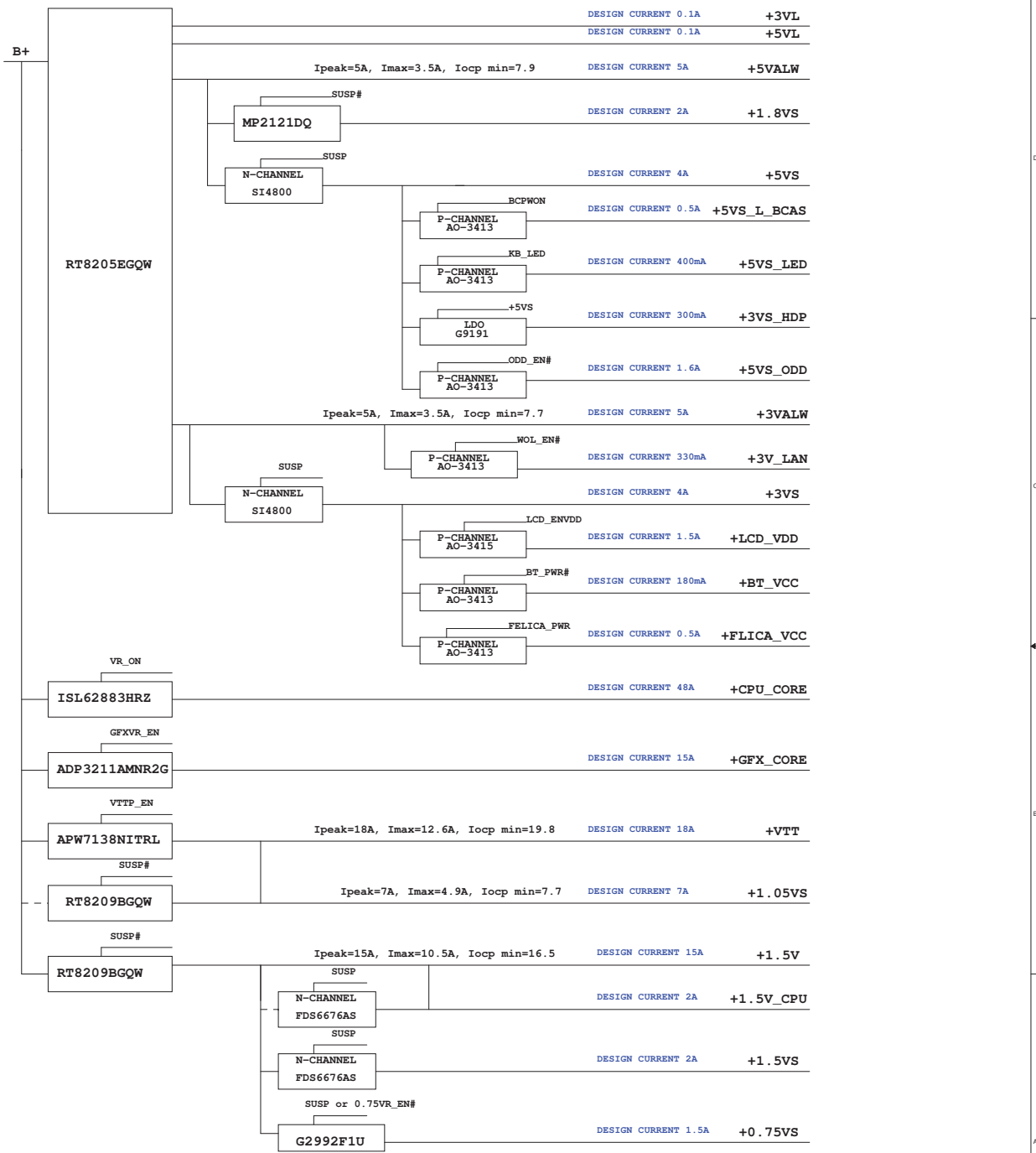
Model Name : PWVAA

File Name : LA-6842P



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Size	Document Number	PWVAA LA6842P M/B		Rev
				0.2
Date:	Wednesday, July 28, 2010	Sheet	2	of 45

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http://www.blogspot.com				Date: Wednesday, July 28, 2010 Sheet 3 of 45

Voltage Rails (O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	MINI PCI-E SLOT	LAN				
description		SLOT1	LAN			
explain		WLAN/BT	10/100M			
BTO						

Function		Camera & Mic			
description		Camera & Mic			
explain		Camera & Mic			
BTO		CAM@			

Function	S3 Power Saving	
description	S3 Power Saving	
explain	Power Saving	
BTO		

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address

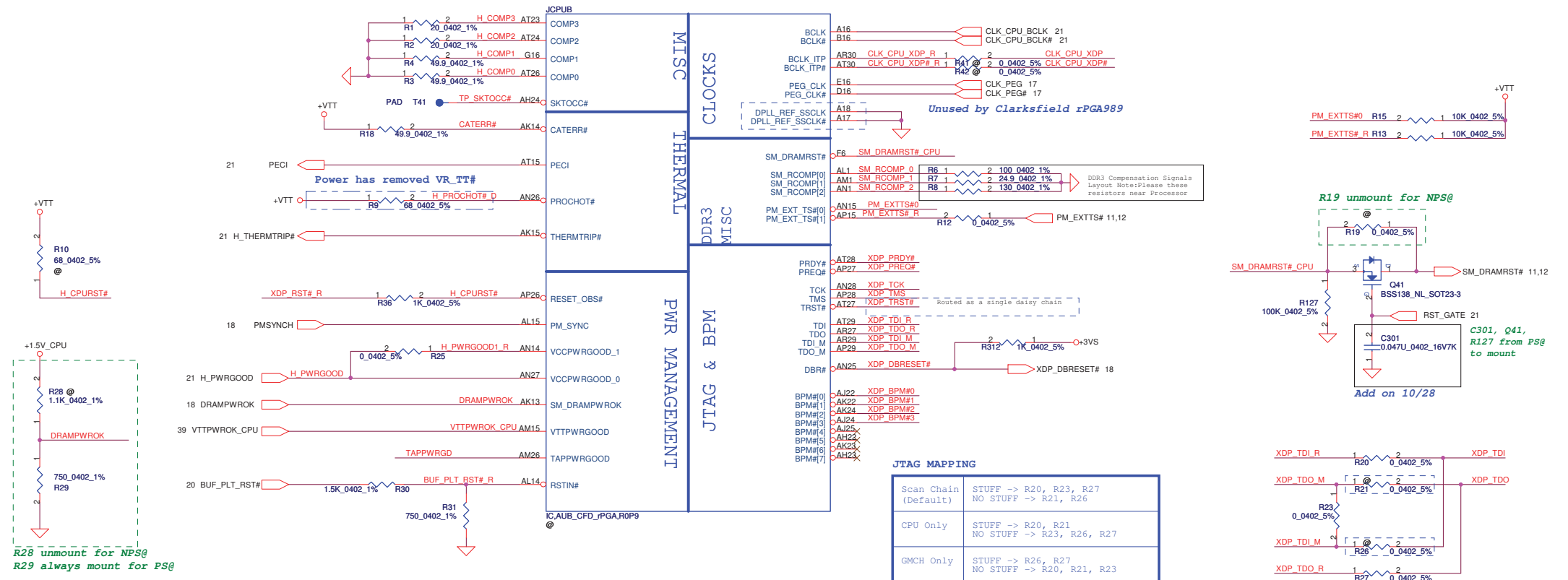
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

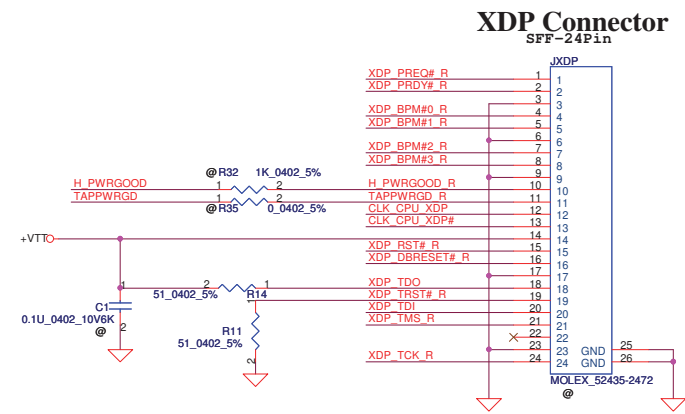
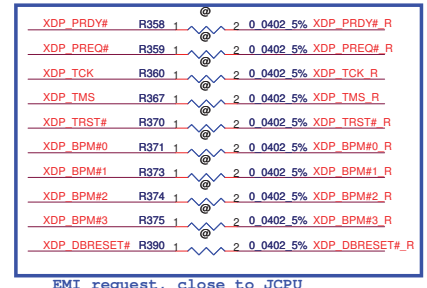
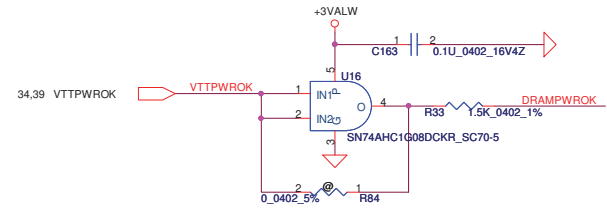
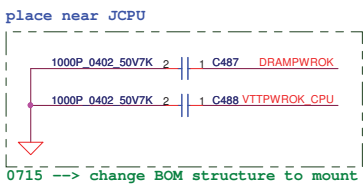
Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

Power	Device	HEX	Address

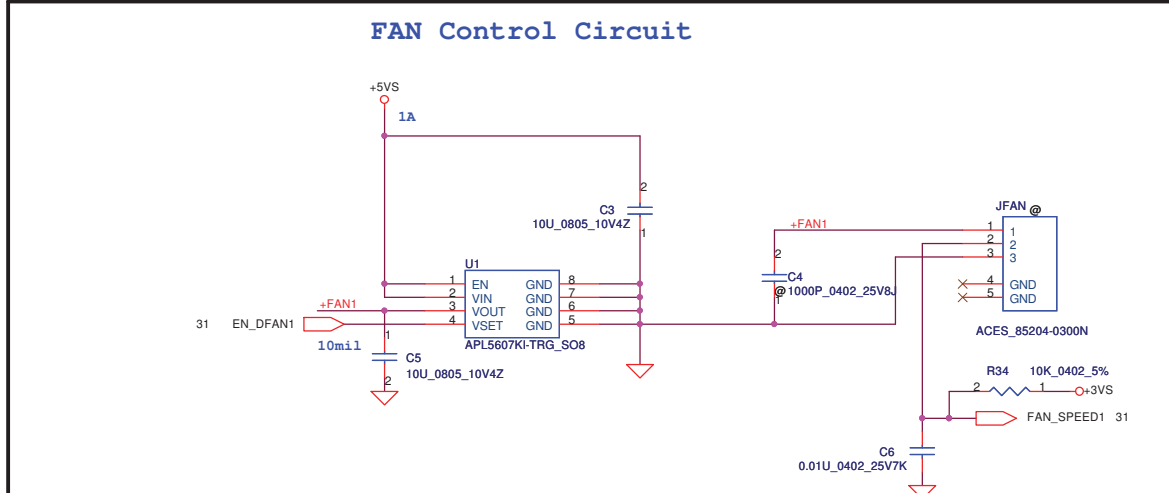
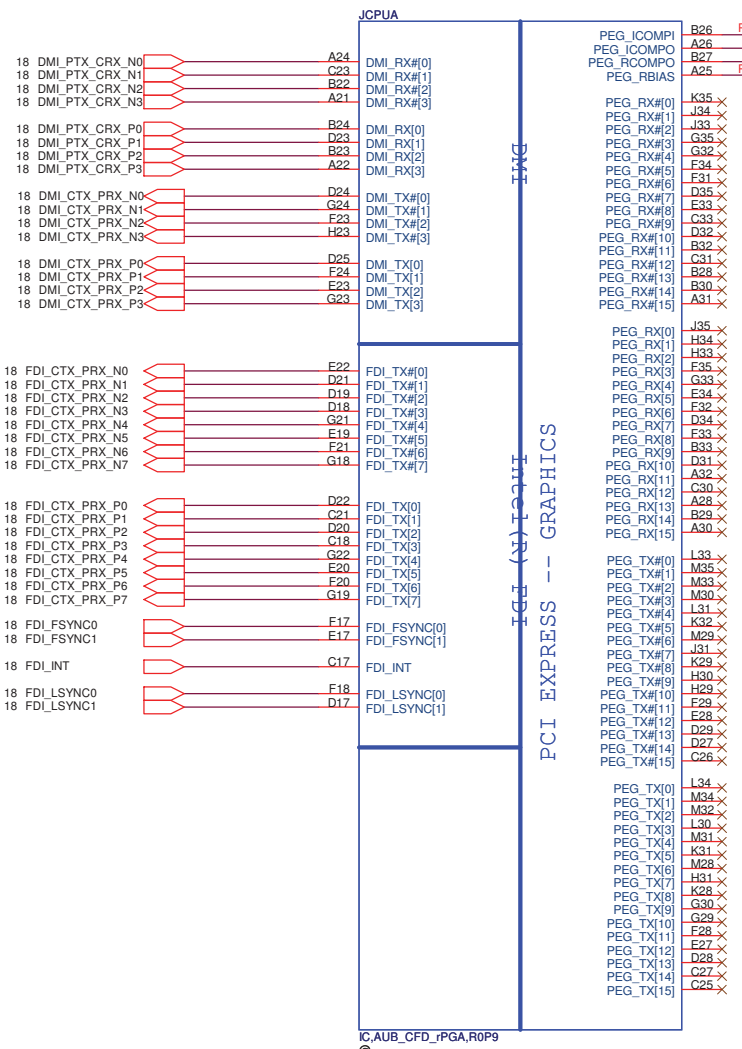
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW



For S3 CPU Power Saving

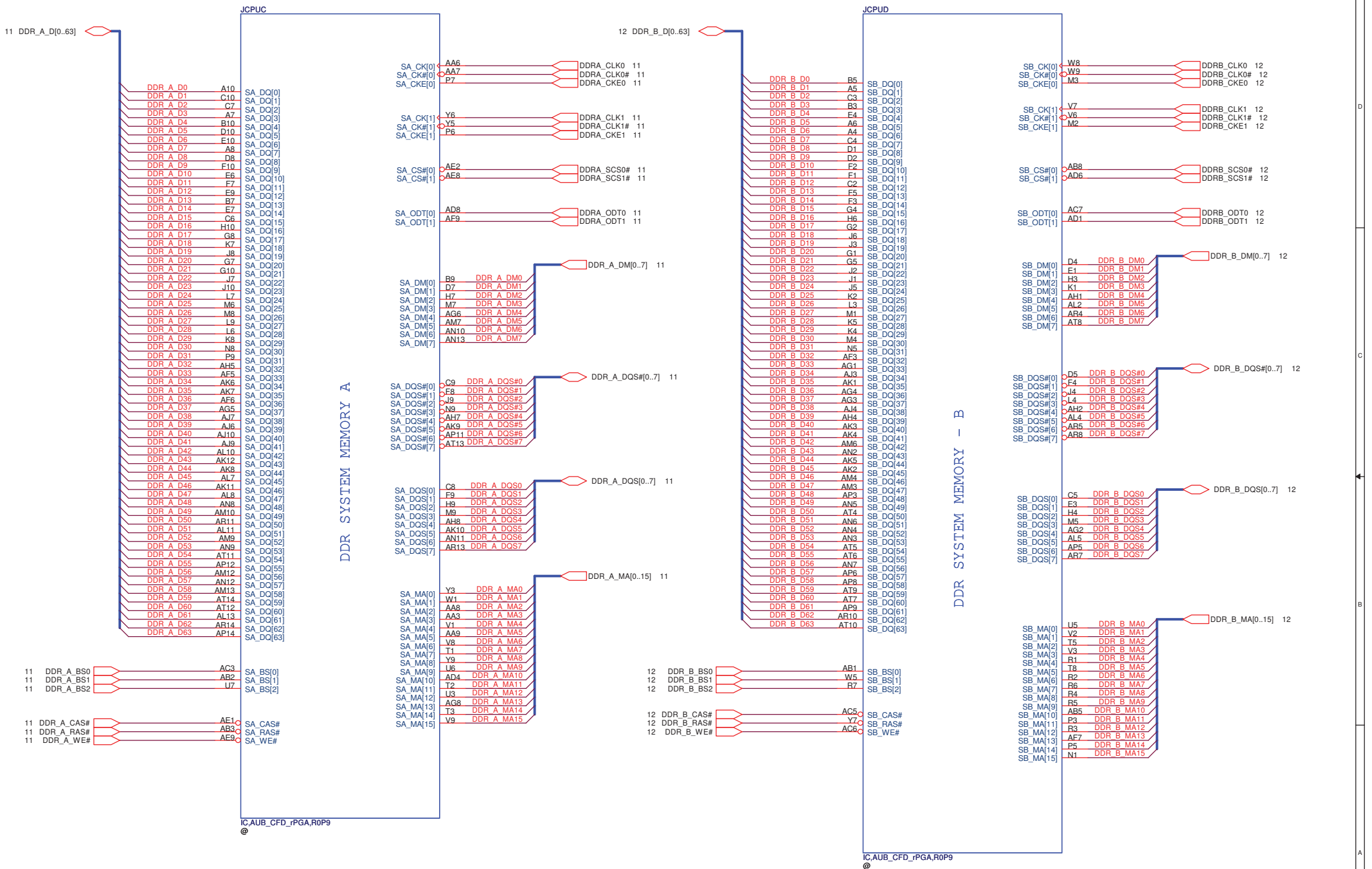


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Size	Document Number	Date		Rev	
Custom	PWWAA LA6842P M/B	Wednesday, July 28, 2010		5 of 45	



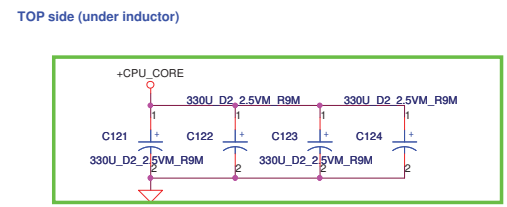
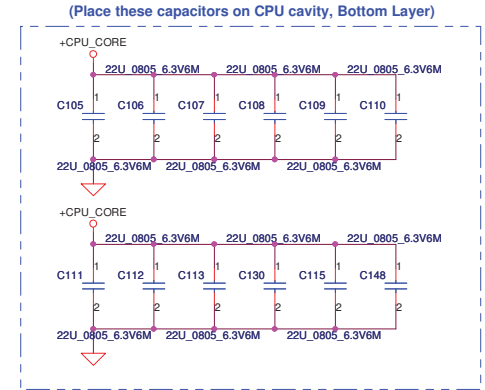
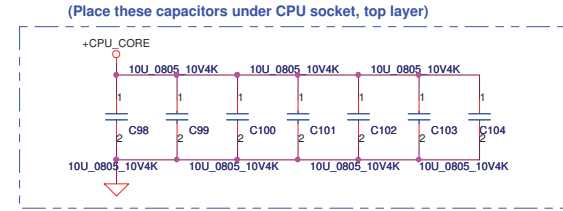
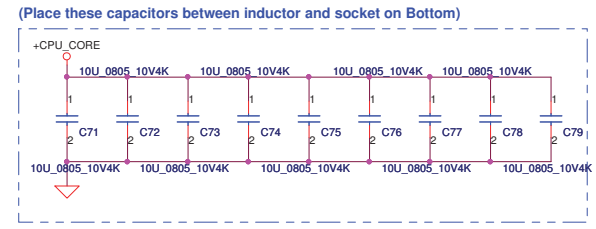
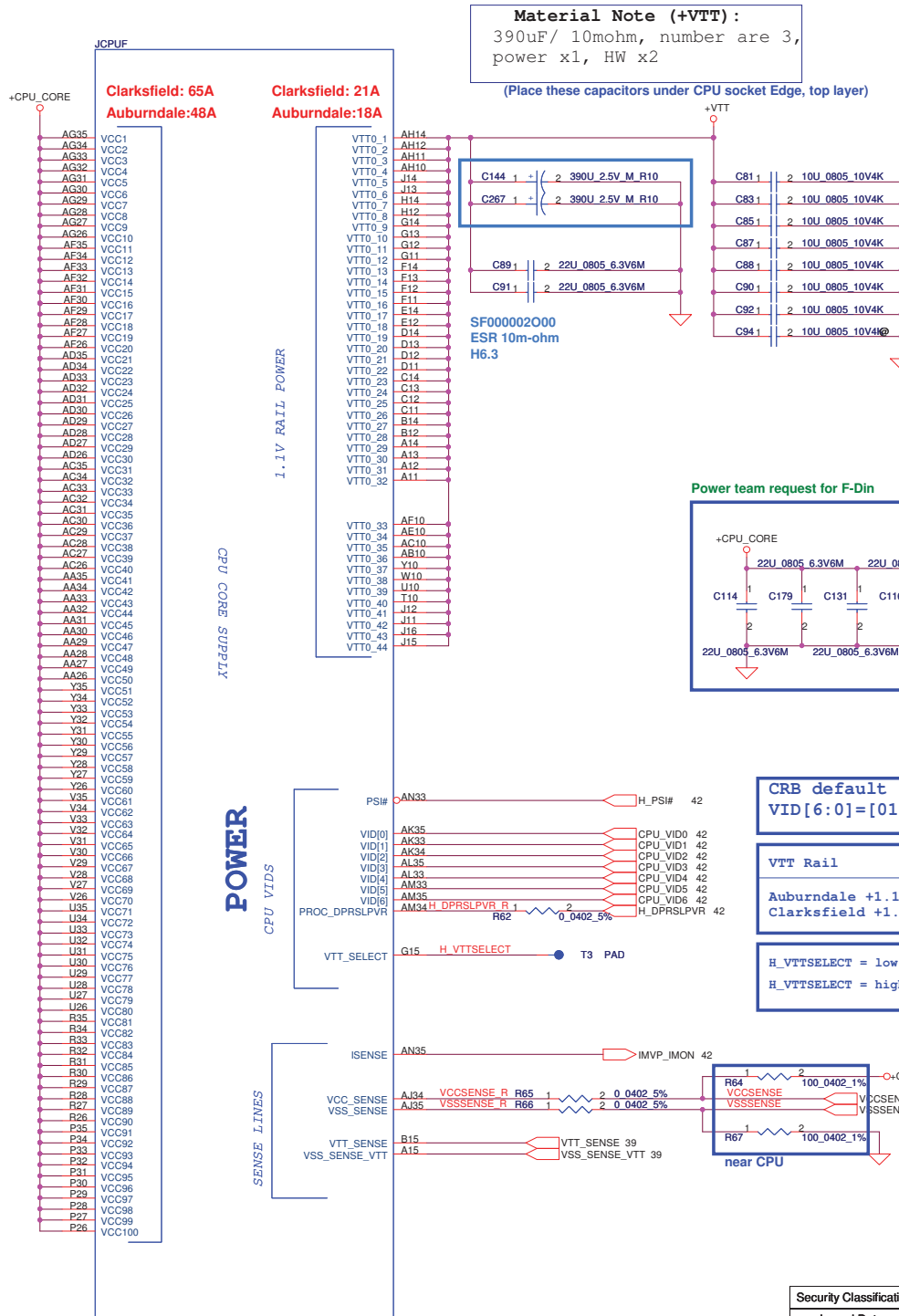
Remove Cap, for EMI

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				PWWAA LA6842P M/B	
				Date	Rev
				Wednesday, July 28, 2010	0.2
				Sheet	6 of 45



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				B	PWWAA LA6842P M/B
				Date	Rev
				Wednesday, July 28, 2010	0.2
				Sheet	7 of 45

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Check list:

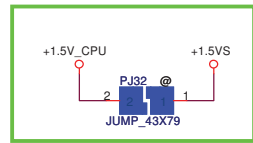
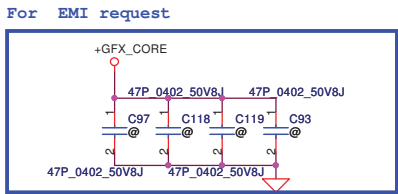
+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF

+VTT: 4x 330uF, 7x 22uF, 8x 10uF

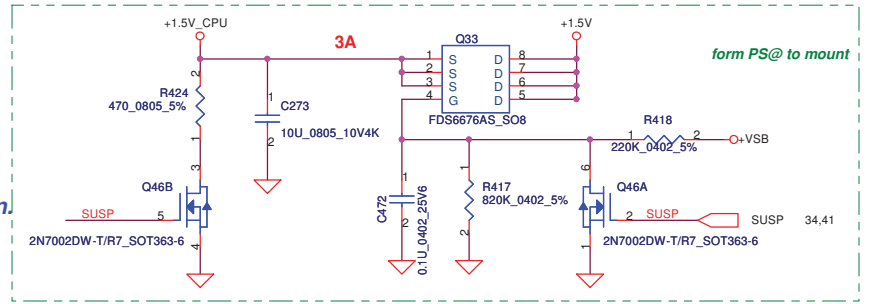
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		Custom	PWWAA LA6842P M/B	0.2	
Date:	Wednesday, July 28, 2010	Sheet	8	of	45

<http://laptop-motherboard-schematic.blogspot.com/>

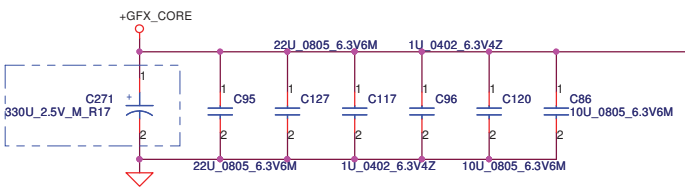


7/22 modified for cost down

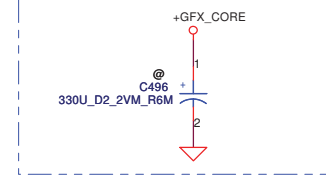


form PS@ to mount

Change C271 to 4.5mm height OS-CON at PVT



Add C496 Co-Layout with C271



For POLY Cap.
0714 --> C271 mount, C496 unmount

- JCPU@
- AT21 VAXG1
 - AT19 VAXG2
 - AT18 VAXG3
 - AT16 VAXG4
 - AR21 VAXG5
 - AR19 VAXG6
 - AR18 VAXG7
 - AR16 VAXG8
 - AP21 VAXG9
 - AP19 VAXG10
 - AP18 VAXG11
 - AN21 VAXG12
 - AN19 VAXG13
 - AN18 VAXG14
 - AM21 VAXG15
 - AM19 VAXG16
 - AM18 VAXG17
 - AM16 VAXG18
 - AL21 VAXG19
 - AL19 VAXG20
 - AL18 VAXG21
 - AK21 VAXG22
 - AK19 VAXG23
 - AK18 VAXG24
 - AK16 VAXG25
 - AJ21 VAXG26
 - AJ19 VAXG27
 - AJ18 VAXG28
 - AH21 VAXG29
 - AH19 VAXG30
 - AH18 VAXG31
 - AH16 VAXG32
 - AH14 VAXG33
 - AH13 VAXG34
 - AH12 VAXG35
 - AH11 VAXG36

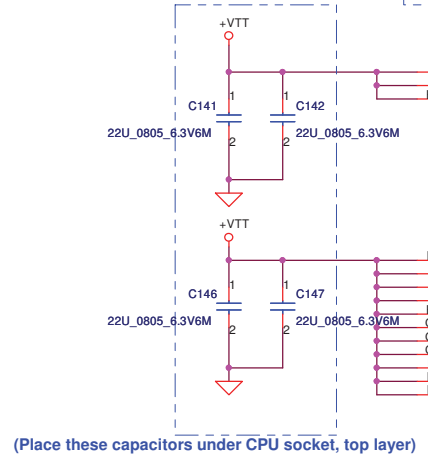
- GRAPHICS
- SENSE LINES
- VAXG SENSE
 - VSSAXG SENSE
 - GFX_VR_EN
 - GFX DPRSLPVR
 - GFX_IMON
- GRAPHICS VIDS
- GFX_VID[0]
 - GFX_VID[1]
 - GFX_VID[2]
 - GFX_VID[3]
 - GFX_VID[4]
 - GFX_VID[5]
 - GFX_VID[6]
- near CPU
- GFXVR_VID_0 43
 - GFXVR_VID_1 43
 - GFXVR_VID_2 43
 - GFXVR_VID_3 43
 - GFXVR_VID_4 43
 - GFXVR_VID_5 43
 - GFXVR_VID_6 43
- POWER
- DDR3 - 1.5V RAILS
- VDD01
 - VDD02
 - VDD03
 - VDD04
 - VDD05
 - VDD06
 - VDD07
 - VDD08
 - VDD09
 - VDD10
 - VDD11
 - VDD12
 - VDD13
 - VDD14
 - VDD15
 - VDD16
 - VDD17
 - VDD18
- 1.1V
- VTT0_59
 - VTT0_60
 - VTT0_61
 - VTT0_62
 - VTT1_63
 - VTT1_64
 - VTT1_65
 - VTT1_66
 - VTT1_67
 - VTT1_68
- 1.8V
- VCCPLL1
 - VCCPLL2
 - VCCPLL3

Clarksfield: 5A
Auburndale: 3A

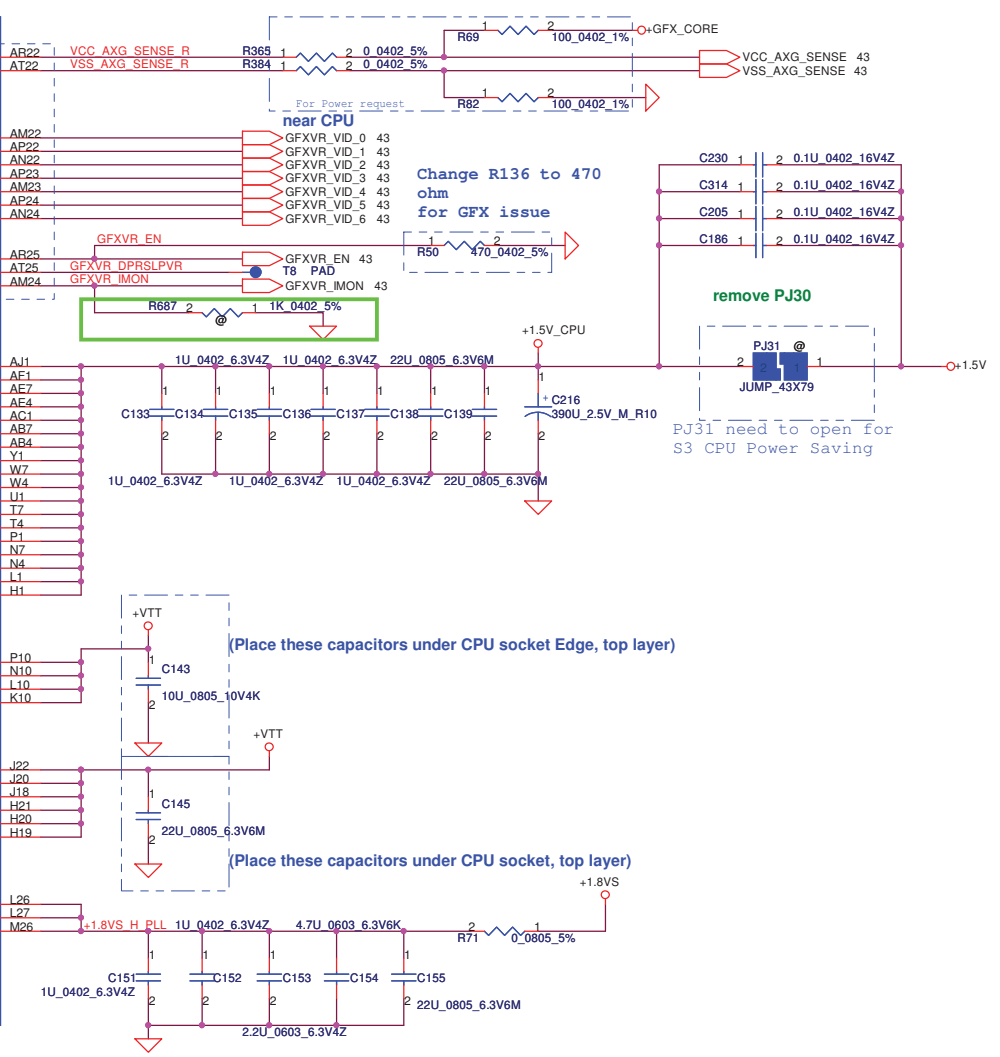
Auburndale: 22A

Clarksfield: 21A
Auburndale: 18A

Clarksfield: 0.6A
Auburndale: 1.35A



(Place these capacitors under CPU socket, top layer)



Change R136 to 470 ohm for GFX issue

remove PJ30

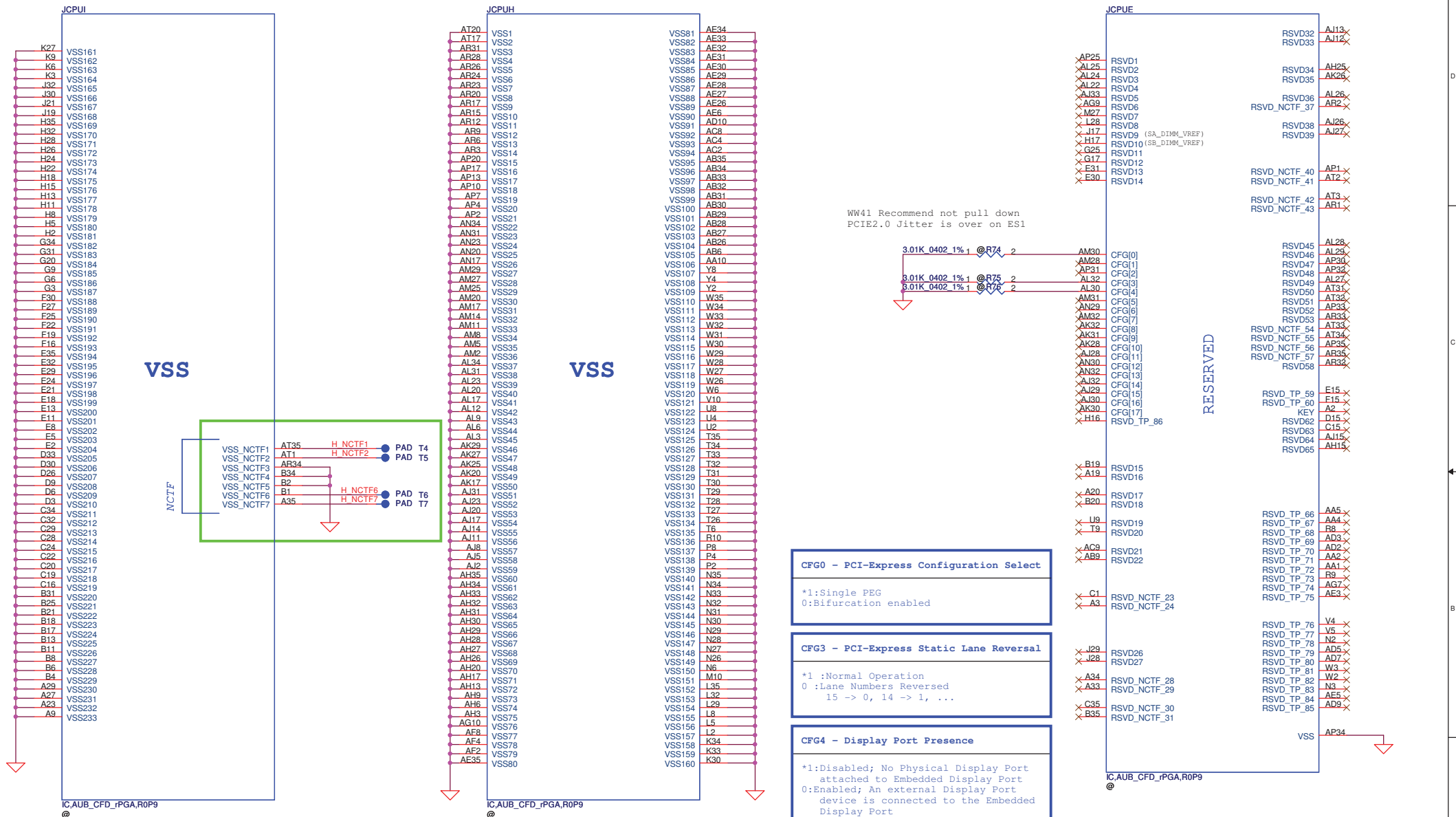
PJ31 need to open for S3 CPU Power Saving

(Place these capacitors under CPU socket Edge, top layer)

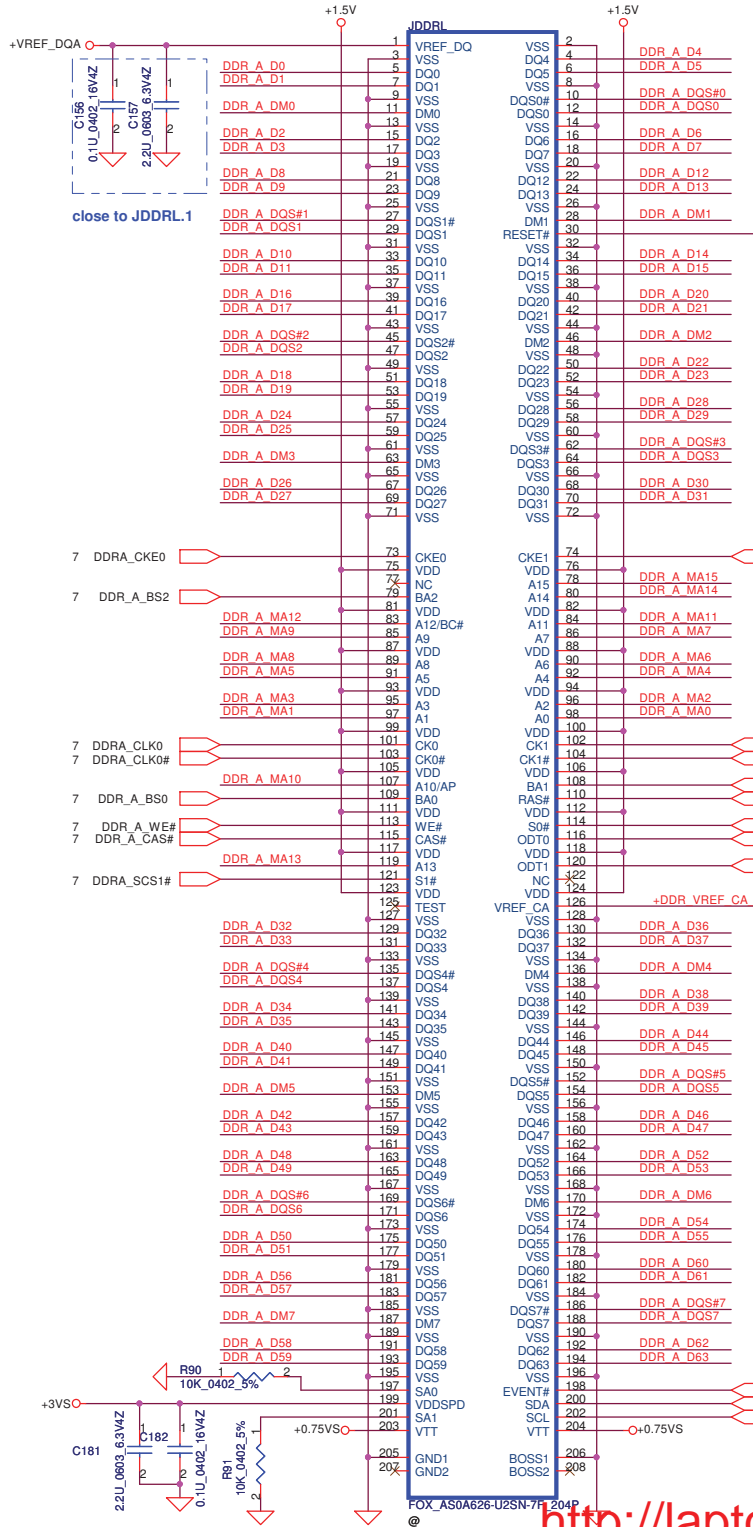
(Place these capacitors under CPU socket, top layer)

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Size B	Document Number	Date		Sheet	Rev
	PWWAA LA6842P M/B	Wednesday, July 28, 2010		9	0.2
				of	45

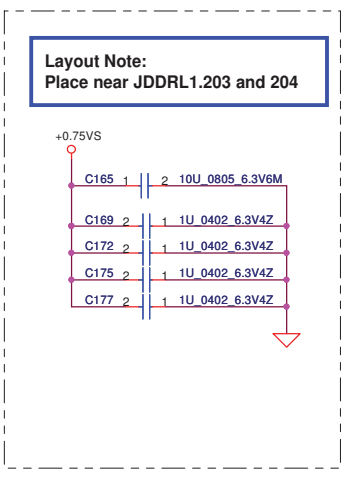
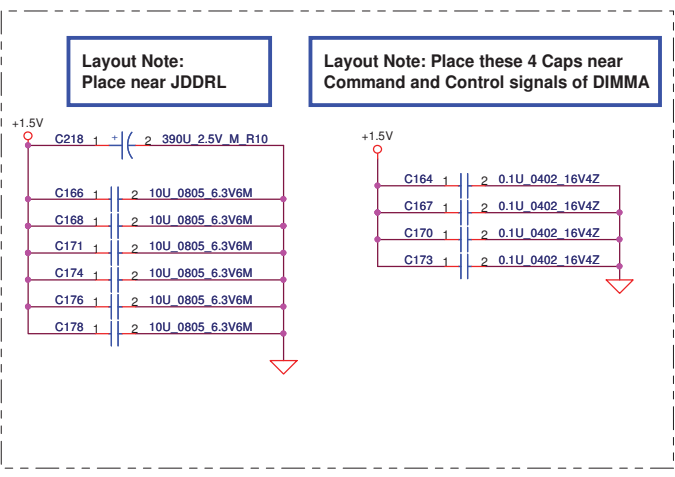
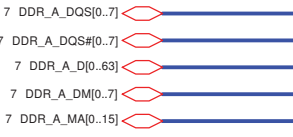
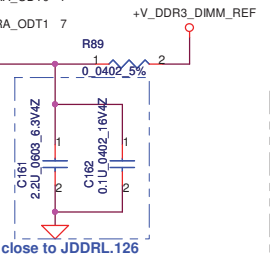
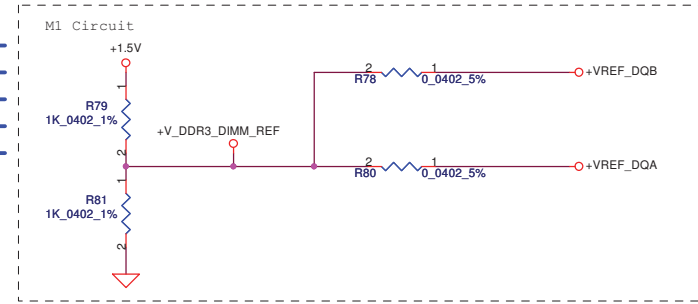
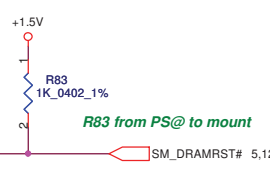
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				Customer	PWWAA LA6842P M/B
				Date	Wednesday, July 28, 2010
				Sheet	10 of 45
				Rev	0.2

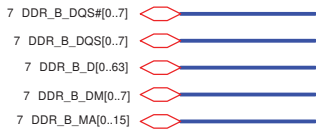
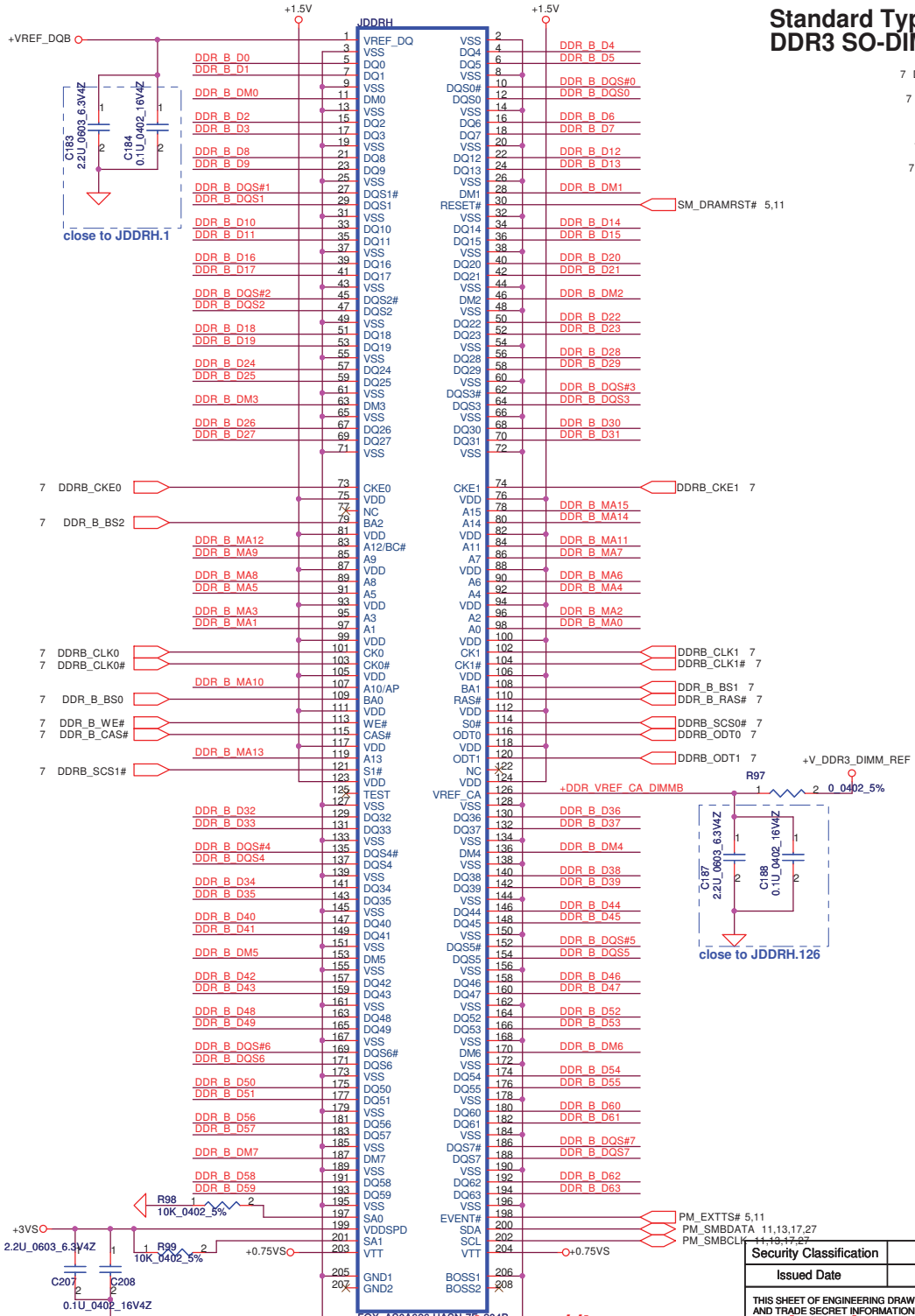


DDR3 SO-DIMM A Standard Type



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				DDRIII-SODIMMO		
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				Date: Wednesday, July 28, 2010	Sheet 11	of 45

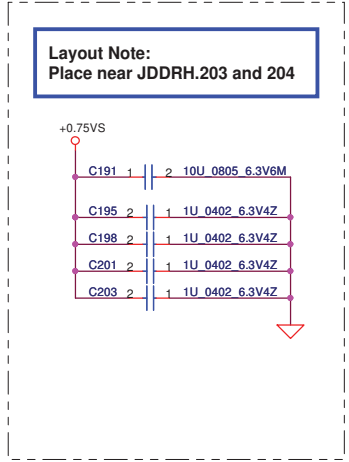
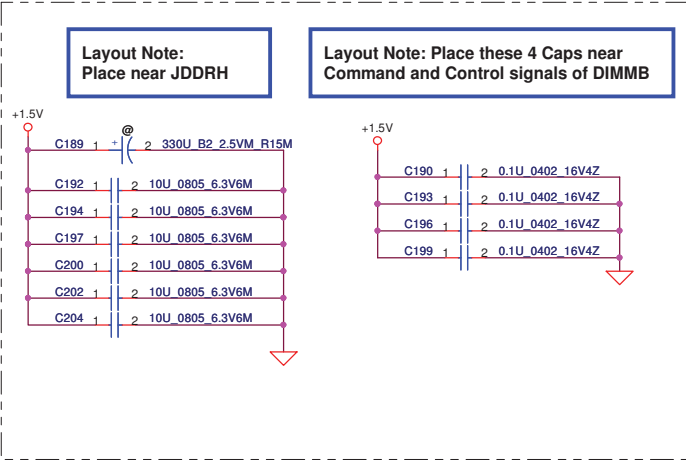
Standard Type DDR3 SO-DIMM B



Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

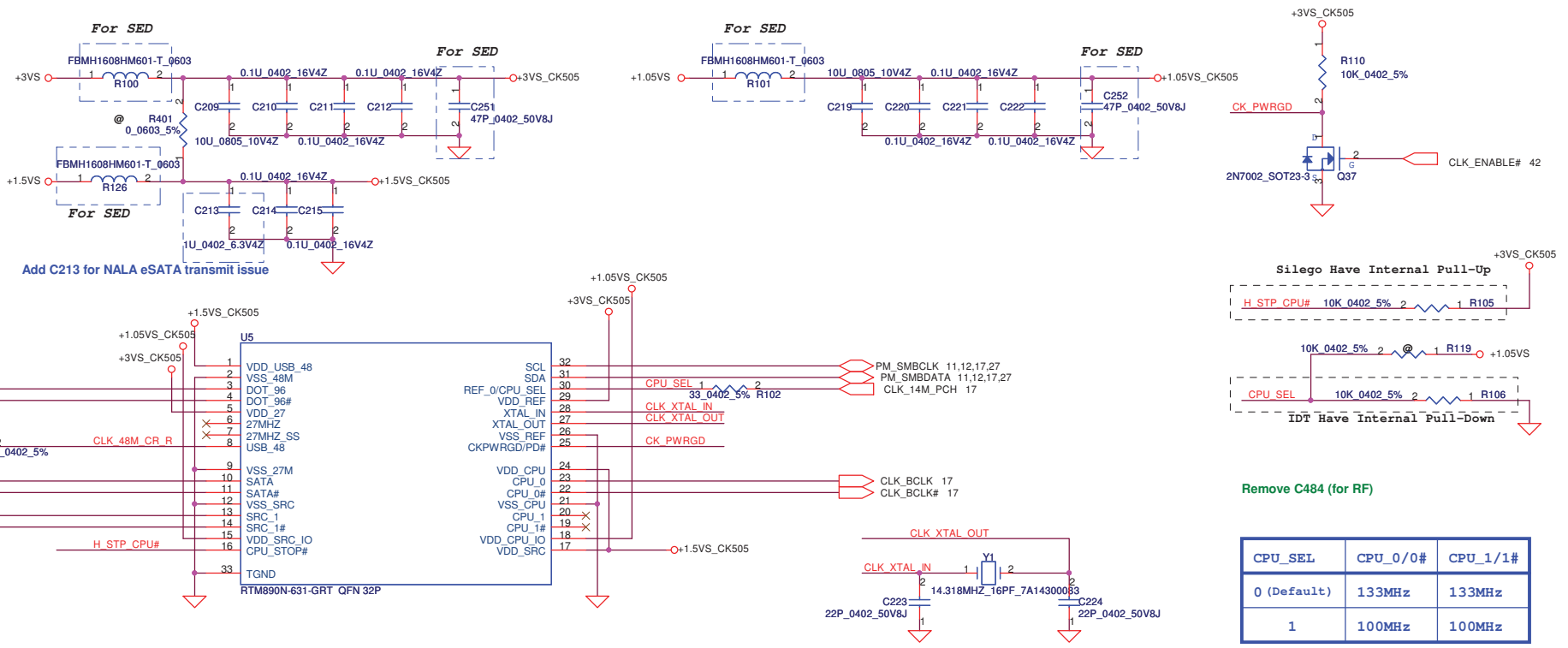
Layout Note: Place near JDDRH.203 and 204



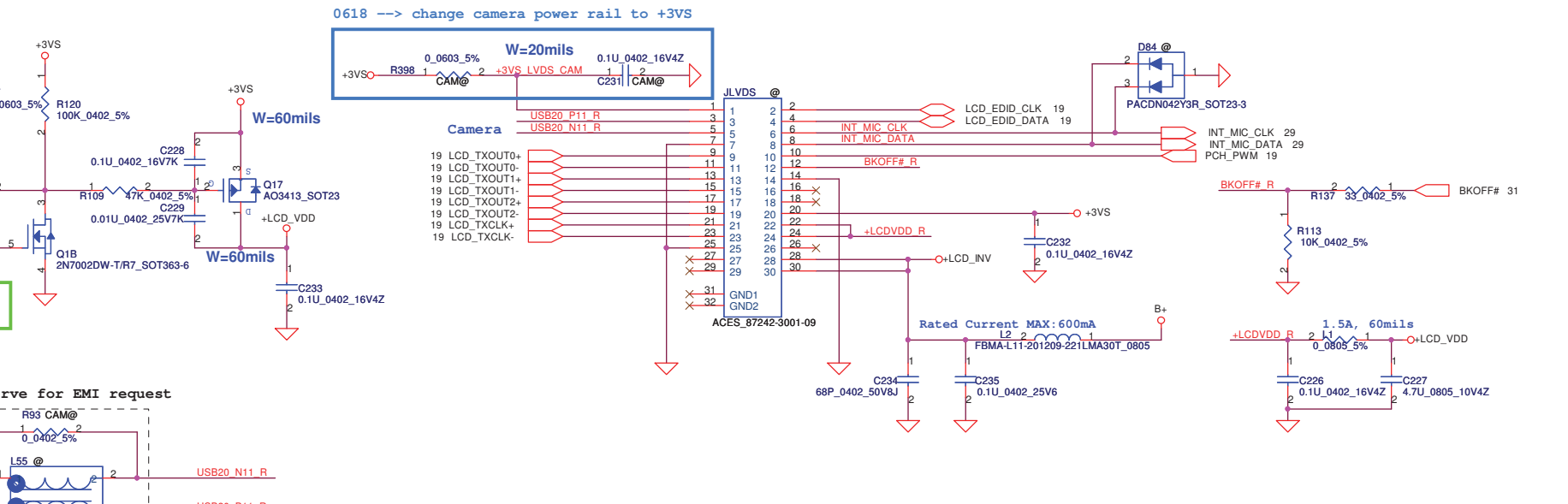
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Title DDRIII-SODIMM1			
Size	Document Number	Rev	
Custom	PWWAA LA6842P M/B	0.2	
Date:	Wednesday, July 28, 2010	Sheet	12 of 45

Clock Generator

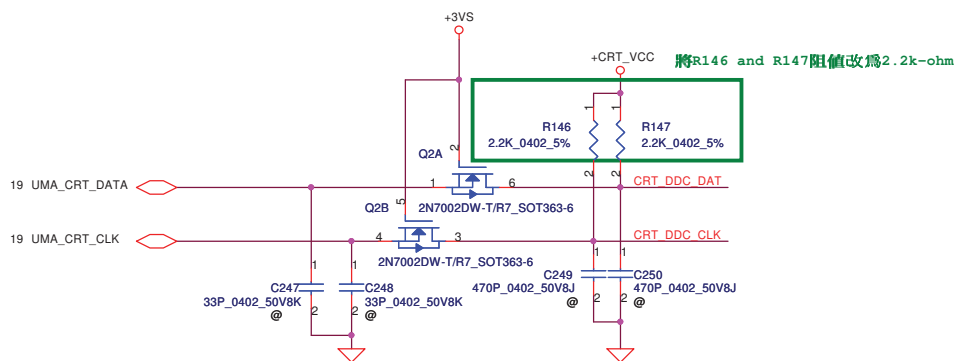
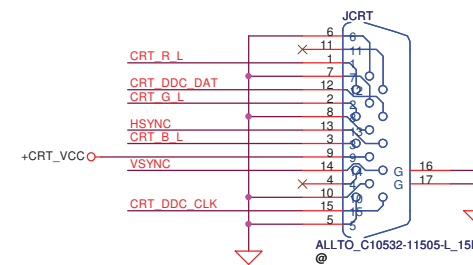
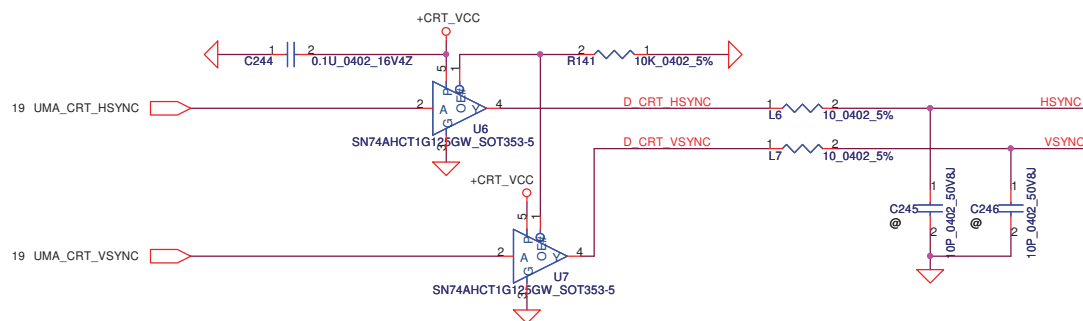
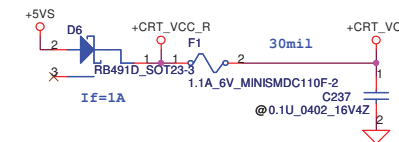
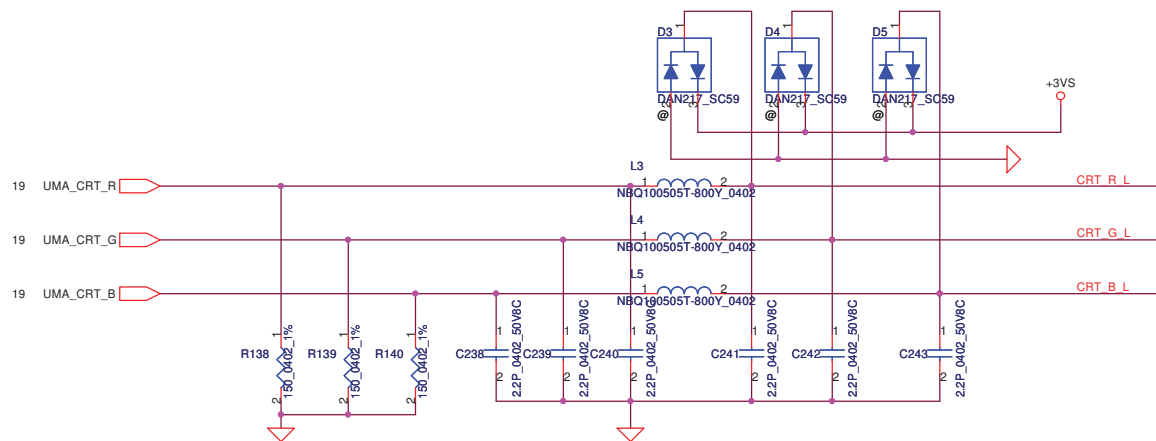


LVDS / Int.Camera / Int.MIC Conn



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				Customer	PWWAA LA6842P M/B
				Date	Wednesday, July 28, 2010
				Sheet	13 of 45

CRT CONNECTOR

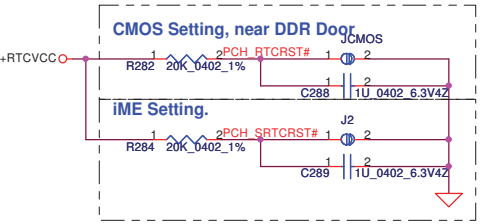


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				CRT/VLVDS	
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			PWWAA LA6842P M/B	0.2	
Date:	Wednesday, July 28, 2010	Sheet	14	of	45

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0624 --> Remove BIOS ROM Debug Circuit

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http://laptop-motherboard-schematic-diagram.com/			Size	Document Number
			PWWAA LA6842P M/B	
			Date:	Wednesday, July 28, 2010
			Sheet	15 of 45
			Rev	0.2



Integrated SUS 1.05V VRM Enable

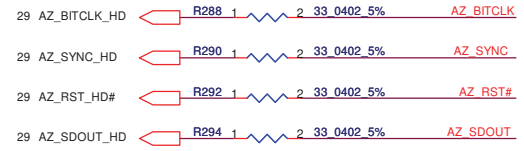
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

HDA_SYNC
 This signal has a weak internal pull down.
 H=>On Die PLL is supplied by 5V
 L=>On Die PLL is supplied by 1.8V

HDA_SDO
 This signal has a weak internal pull down.
 This signal can't PU

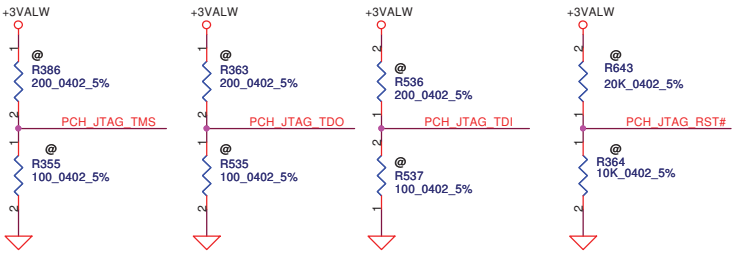
Flash Descriptor Security Override

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------



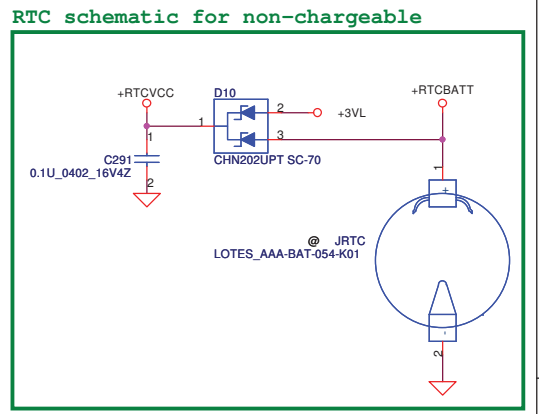
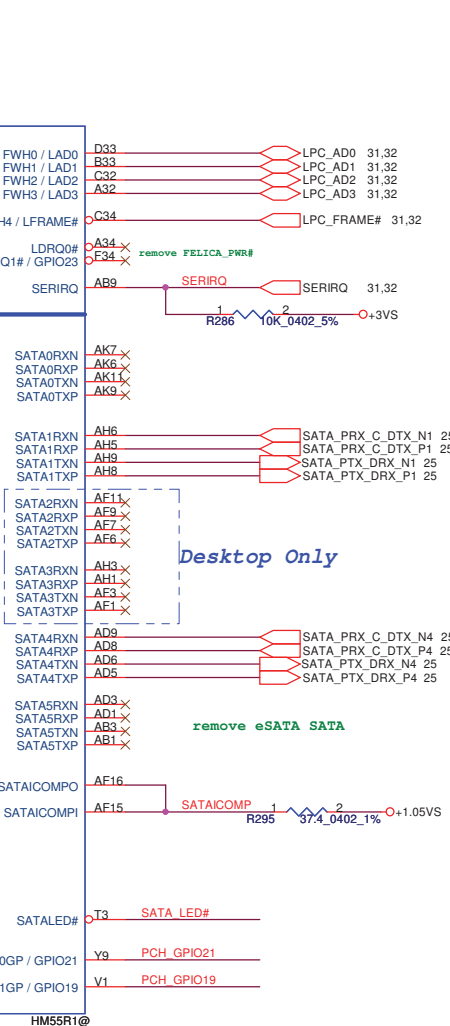
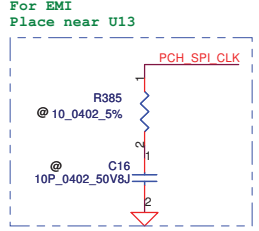
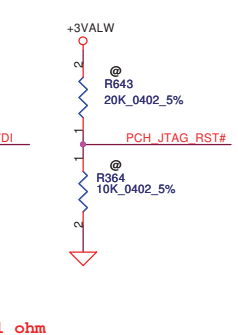
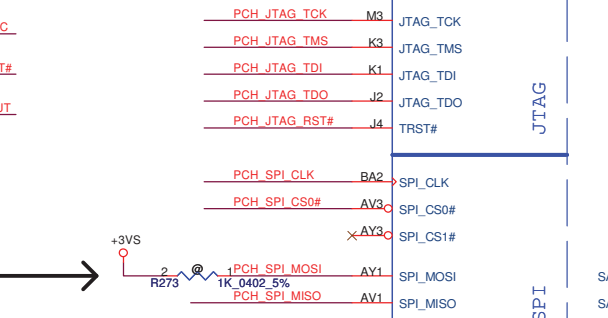
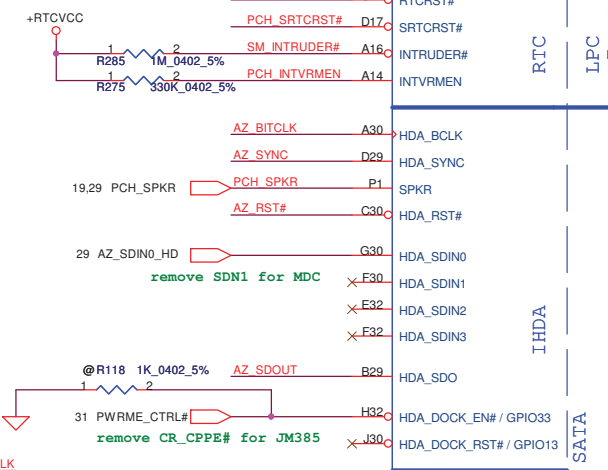
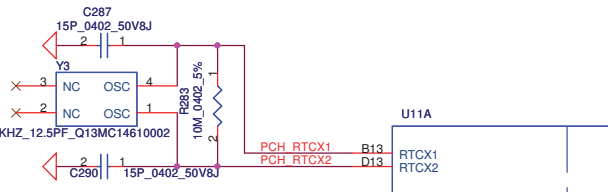
ITPM Enabled Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



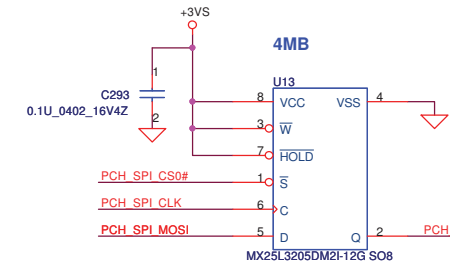
06/01 change R125 from 4.7K to 51 ohm

PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20kohm	No Install
PCH_JTAG_TCK	R537	100ohm	100ohm	10kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
PCH_JTAG_RST#	R353	10kohm	10kohm	No Install	No Install



1ST HDD

SATA ODD

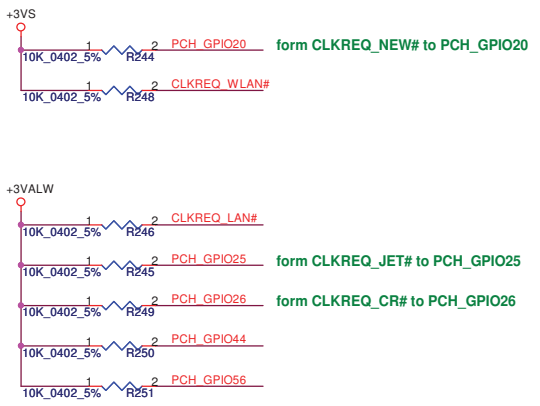


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		PCH-SPI/SATA/LPC/RTC/HDA	
Size	Document Number	Rev	
B	PWWAA LA6842P M/B	0.2	
Date:	Wednesday, July 28, 2010	Sheet	16 of 45

For LAN
For WLAN

- 28 PCIE_PRX_C_LANTX_N1
- 28 PCIE_PRX_C_LANTX_P1
- 28 PCIE_PT_X_C_LANRX_N1
- 28 PCIE_PT_X_C_LANRX_P1
- 27 PCIE_PRX_WLANTX_N2
- 27 PCIE_PRX_WLANTX_P2
- 27 PCIE_PT_X_C_WLANRX_N2
- 27 PCIE_PT_X_C_WLANRX_P2

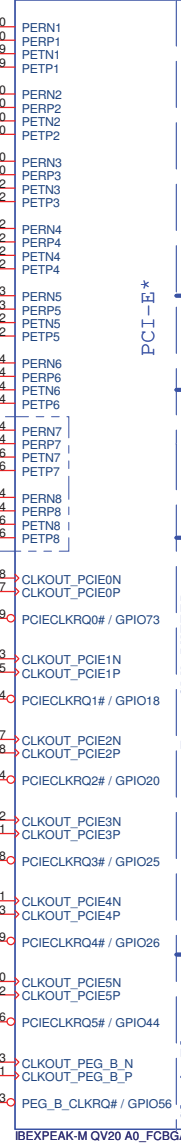
LAN
WLAN



remove NewCard PCIE
remove JET PCIE
remove CardReader PCIE

NC

U11B



PCI-E*

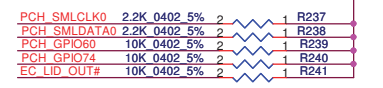
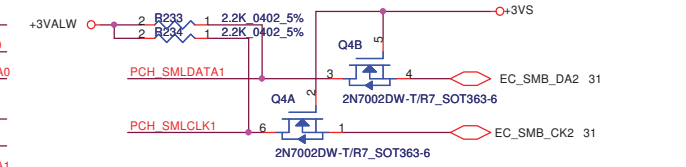
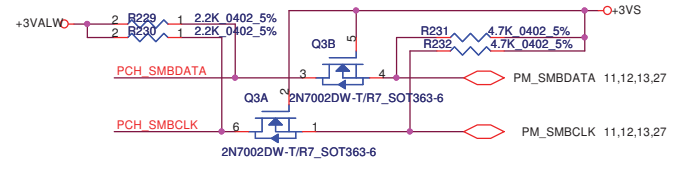
SMBus

Controller Link

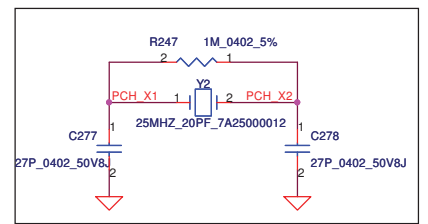
PEG

From CLK BUFFER

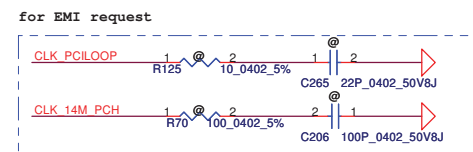
Clock Flex



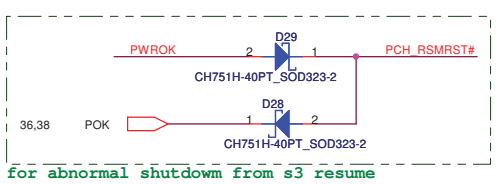
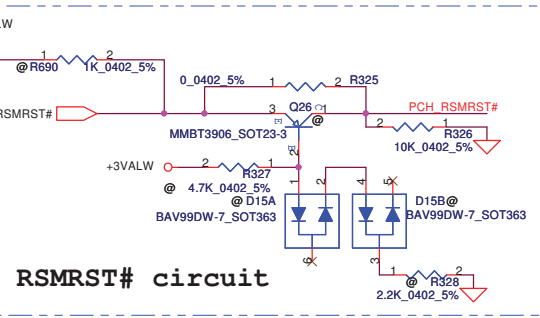
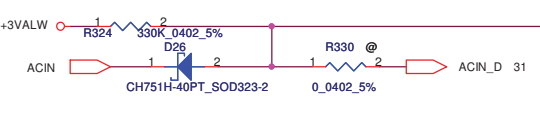
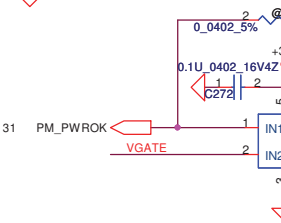
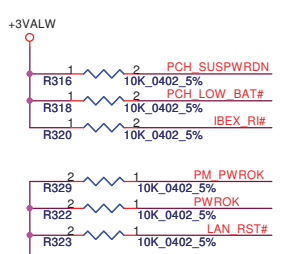
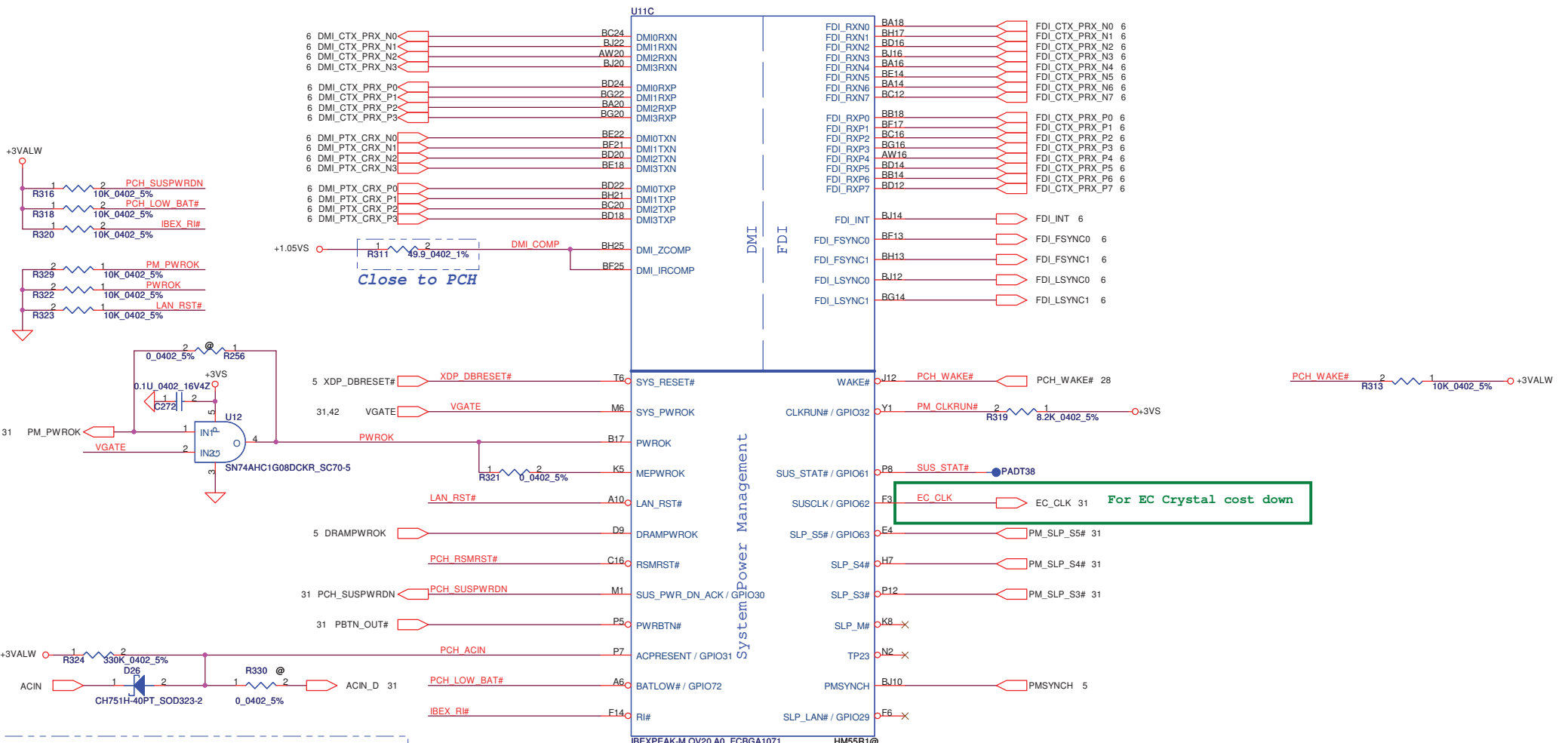
FROM CLK GEN FOR: 133/100/96/14.318 MHZ



Note: Stuff 0 ohm if 25MHz crystal un-stuff



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Date:	Wednesday, July 28, 2010	Sheet	17	of	45



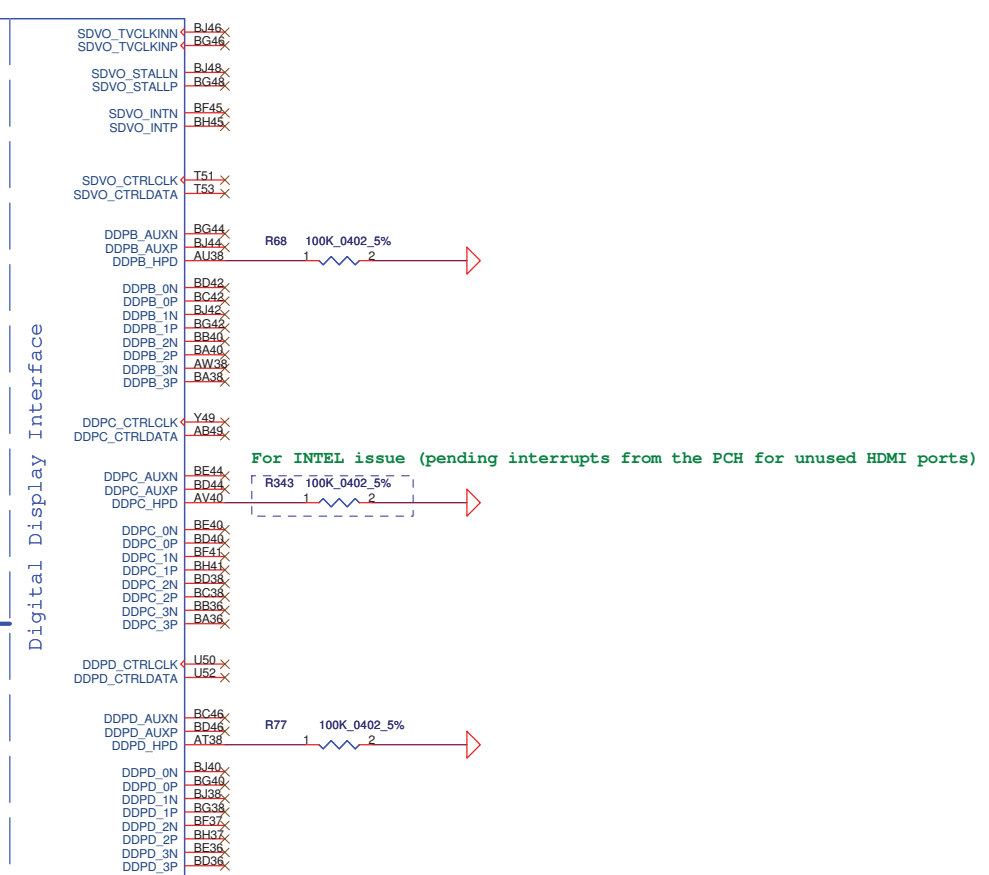
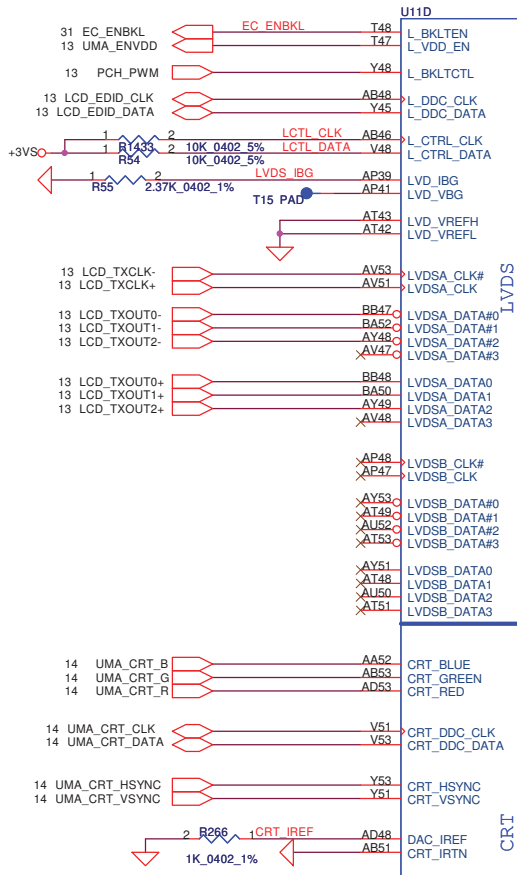
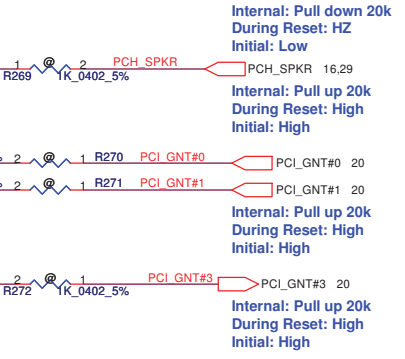
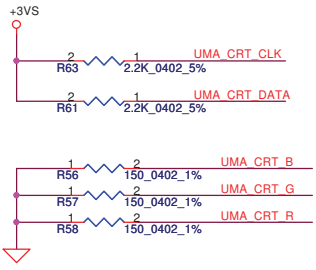
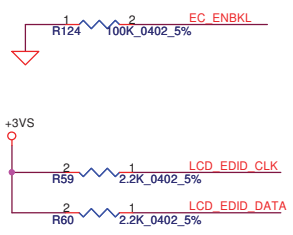
0716 --> Unmount : R327, Q26, D15A, D15B, R328, R690
Mount : R325, D29, D28

Close to PCH

For EC Crystal cost down

for abnormal shutdown from s3 resume

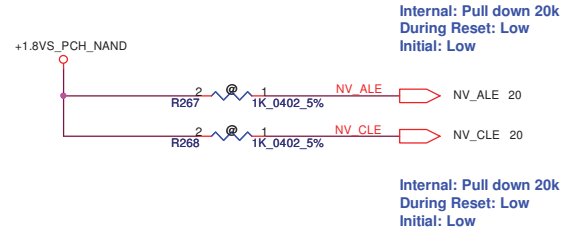
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				PCH-DMI/FDI/PWM	
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				B	0.2
				Date:	Wednesday, July 28, 2010
				Sheet	18 of 45



For INTEL issue (pending interrupts from the PCH for unused HDMI ports)

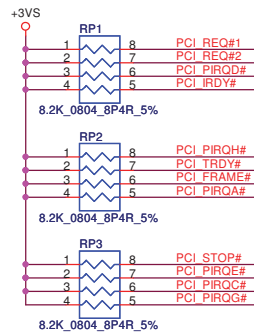
PCH Strap Pin

NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)
A16 Swap Override Strap		
PCI_GNT#3	Low= A16 swap override Enable	High= A16 swap override Disable



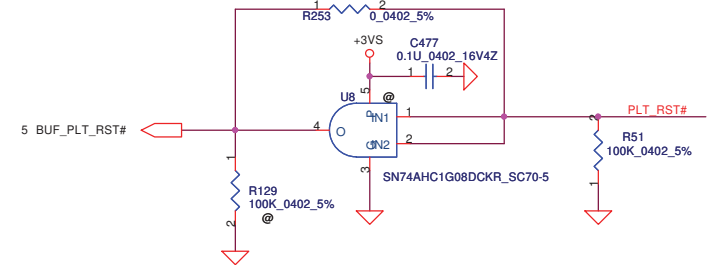
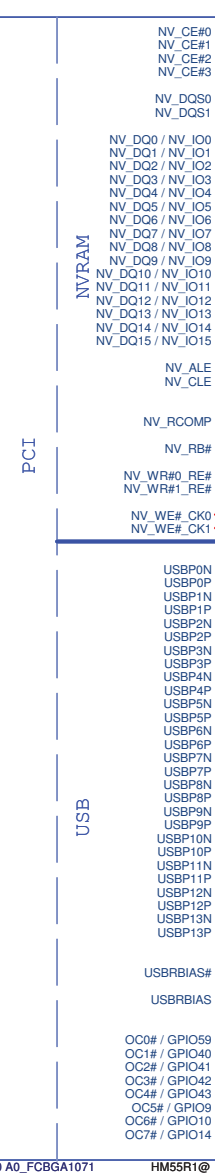
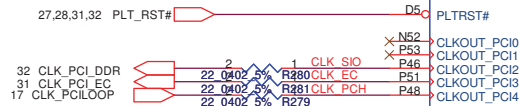
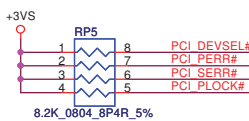
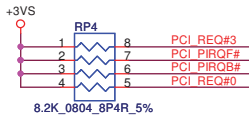
Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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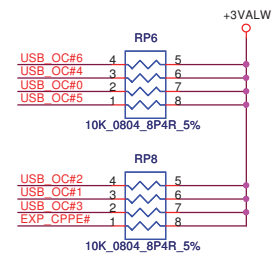


add PCI_REQ#2 for non-ODD_EN#

GNT2#: Not pull low, internal pull up 20K



- USB-LIGHT1
- USB-LIGHT2
- USB-Left1
- remove eSATA
- remove NewCard
- remove BT
- remove FingerPr
- remove FELICA
- Card reader(2 in 1)
- Int. Camera
- remove 3G/TV#1
- WiMax(WLAN)



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				Date:	Wednesday, July 28, 2010	
				Sheet	20 of 45	

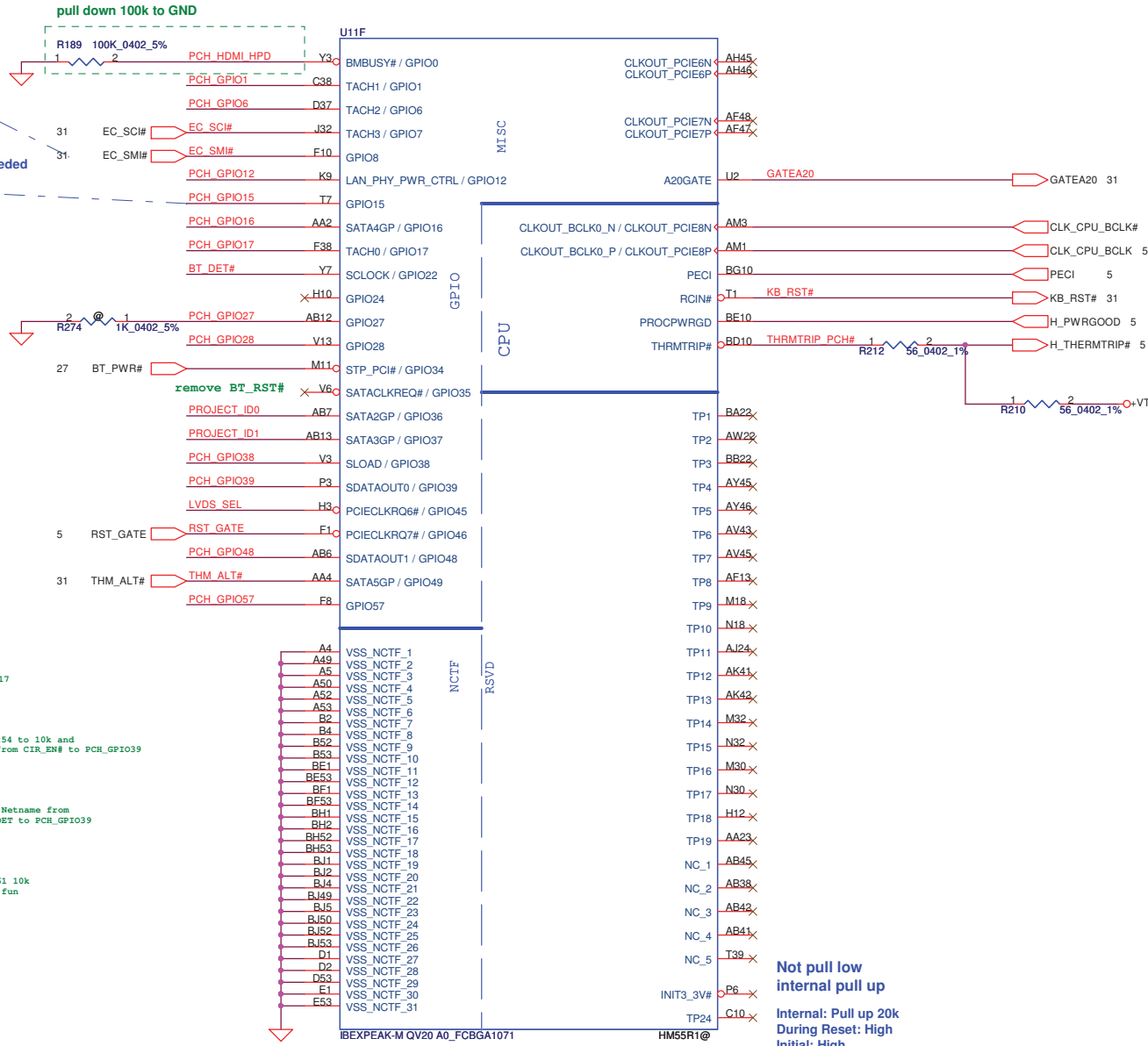
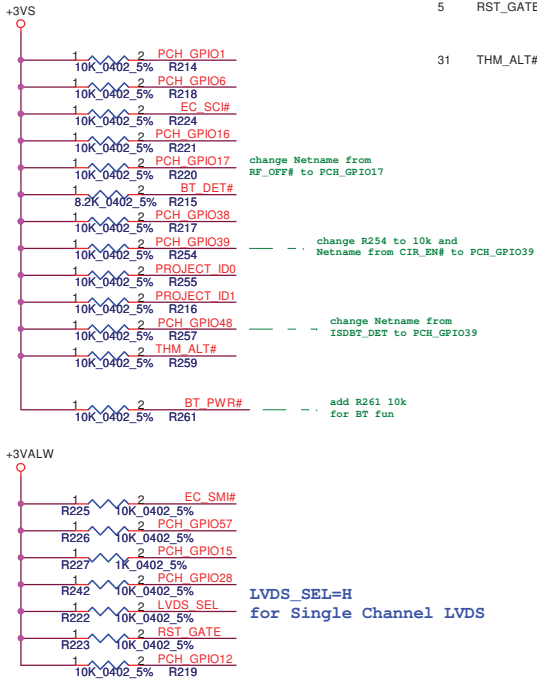
GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR

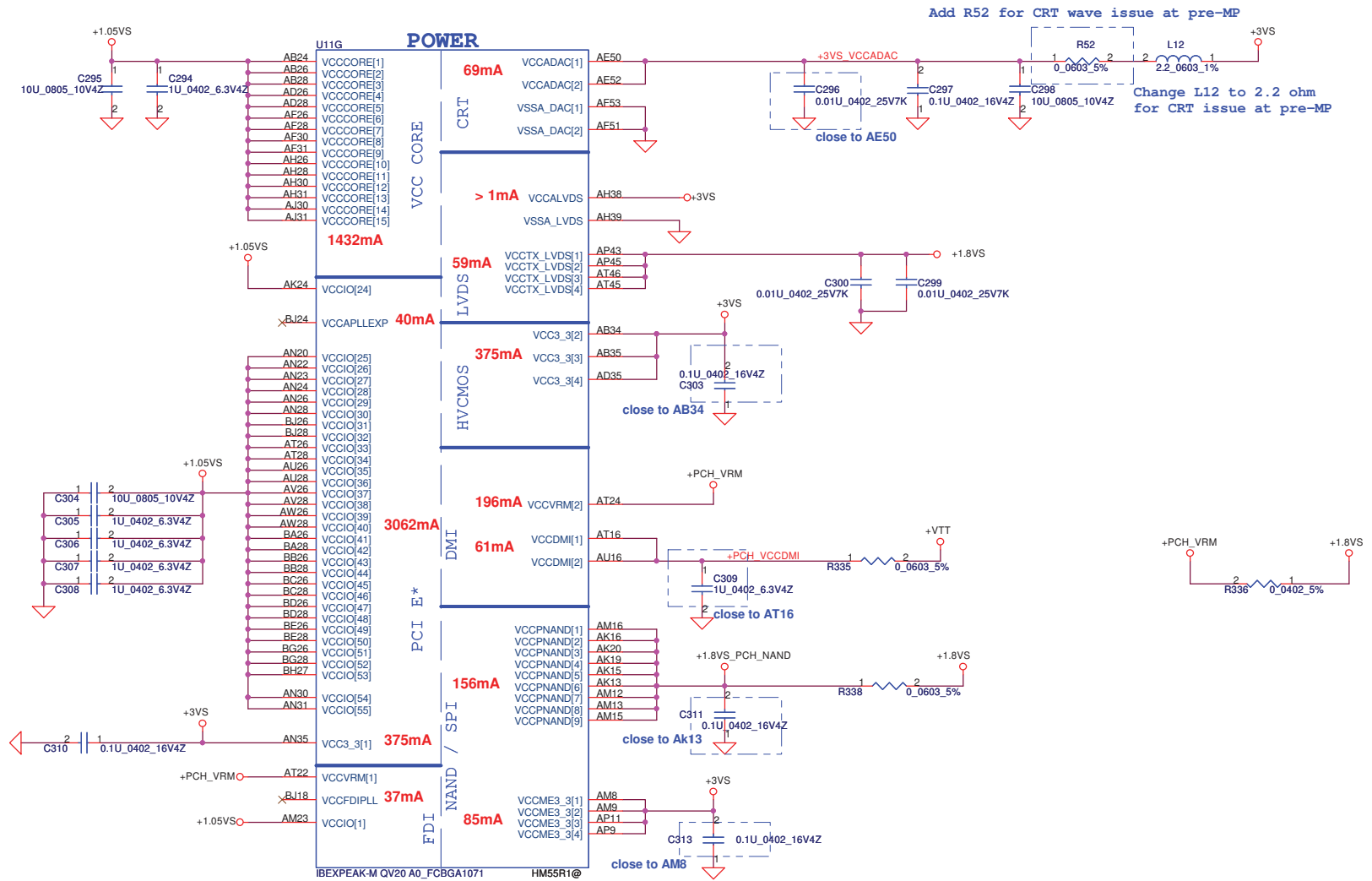
PCH_GPIO27 High = Enabled (Default)
Low = Disabled

PROJECT_ID			
Name	ID0	ID1	
NBQAA 11.6/13.3"	L	L	
NBQAA 14"	L	H	
*NBQAA 16"	H	L	
NALAA 17.3"	H	H	



Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

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				PCH CPU/GPIO	
Size	Document Number			Rev	0.2
B	PWWAA LA6842P M/B				
Date:	Wednesday, July 28, 2010	Sheet	21	of	45



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				Date:	Wednesday, July 28, 2010	Sheet 22 of 45

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VccLAN may be grounded if Intel LAN is disabled

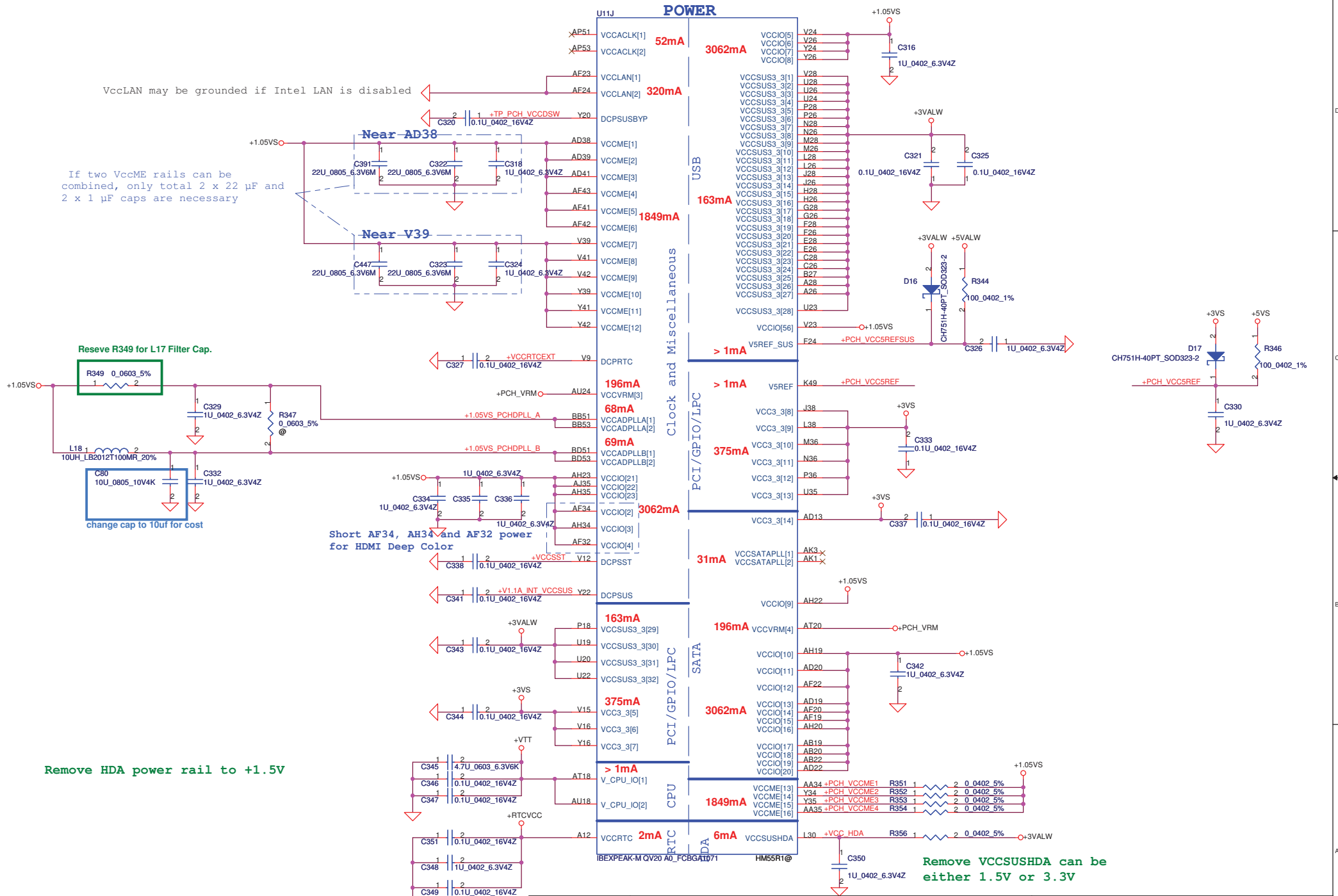
If two VccME rails can be combined, only total 2 x 22 µF and 2 x 1 µF caps are necessary

Reserve R349 for L17 Filter Cap.

change cap to 10uf for cost

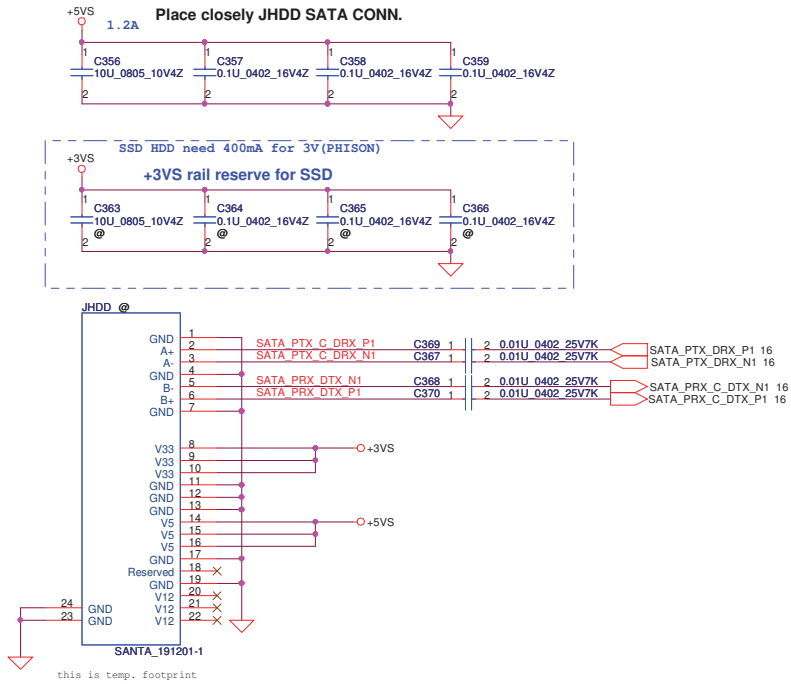
Remove HDA power rail to +1.5V

Remove VCCSUSHDA can be either 1.5V or 3.3V

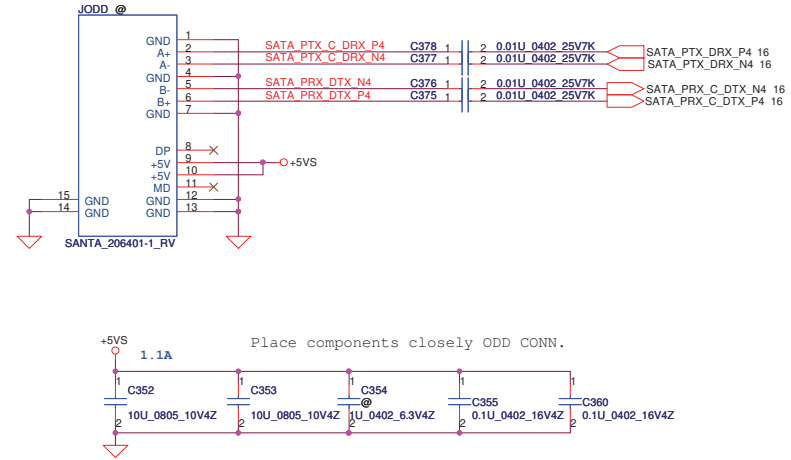


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Customer	PWWAA LA6842P M/B	0.2			
Date:	Wednesday, July 28, 2010	Sheet	23	of	45

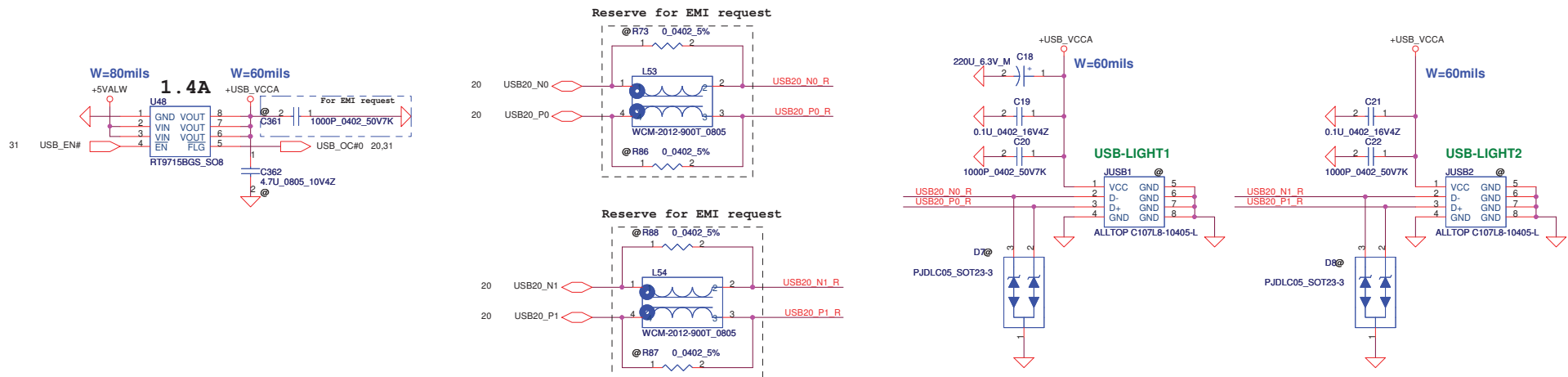
SATA HDD Conn.



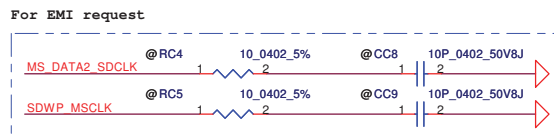
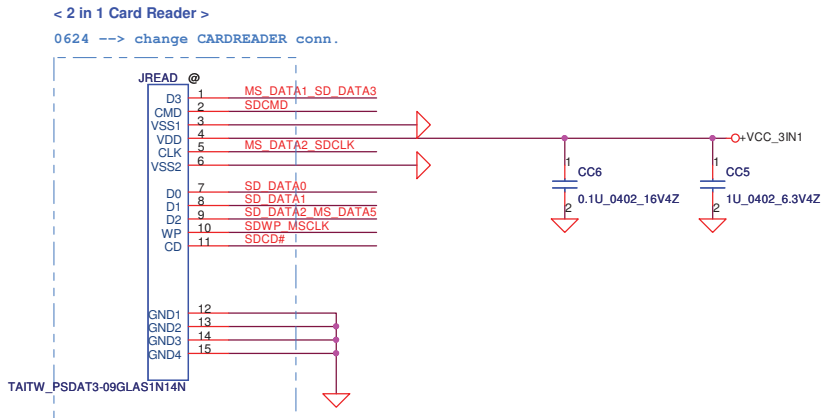
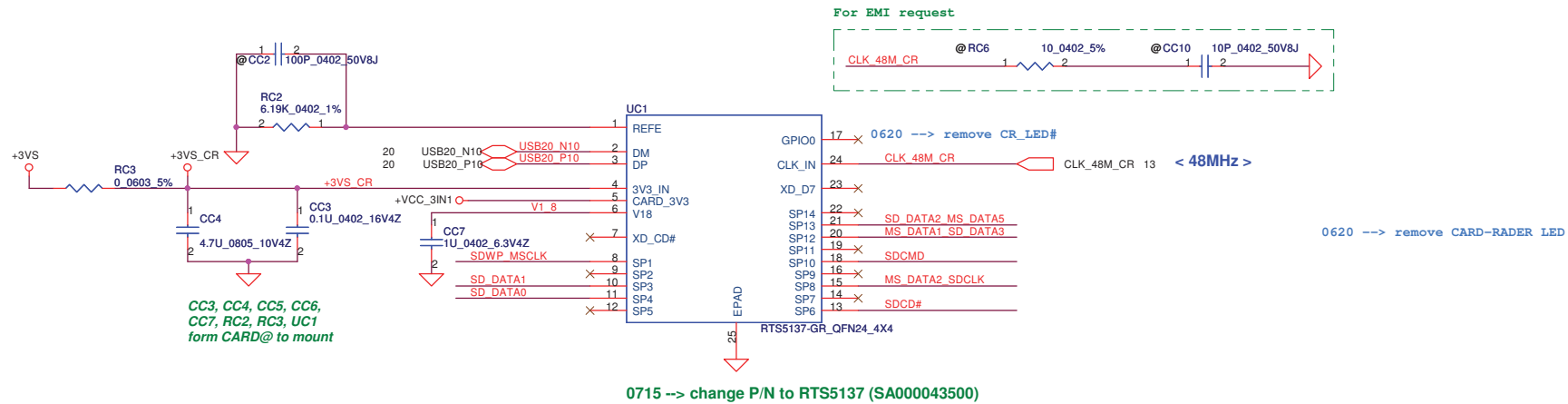
SATA ODD Conn



USB Conn. (2 Port)



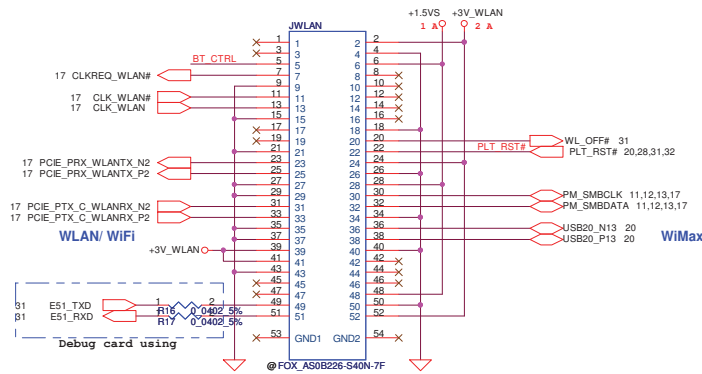
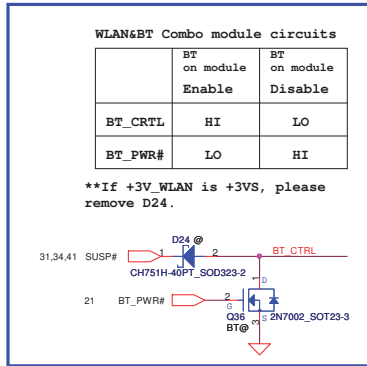
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Date	Wednesday, July 28, 2010	Sheet	25	of	45	



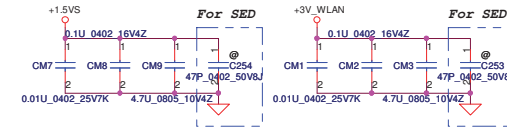
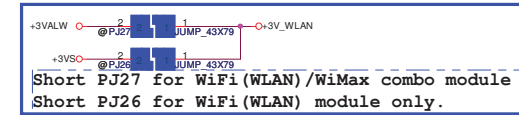
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Date	Wednesday, July 28, 2010	Sheet	26	of	45

<http://laptop-motherboard-schematic.blogspot.com/>

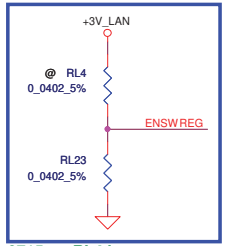
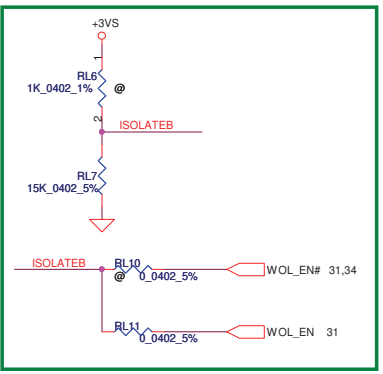
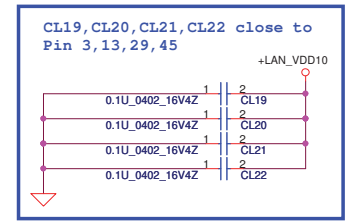
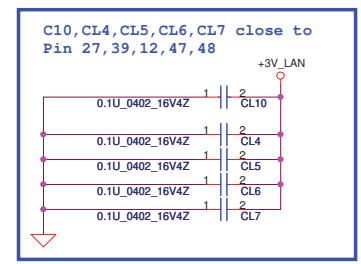
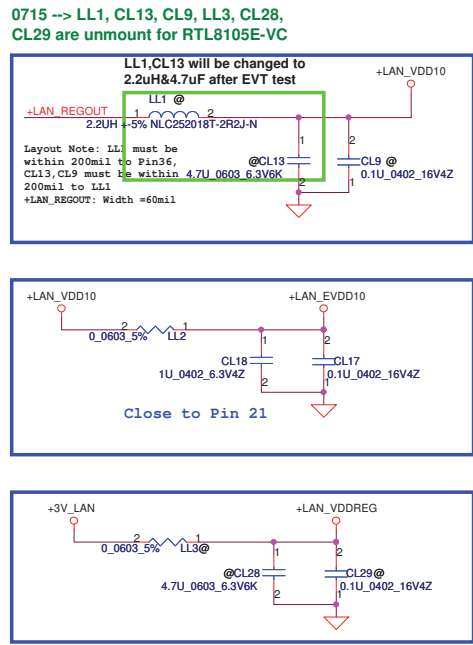
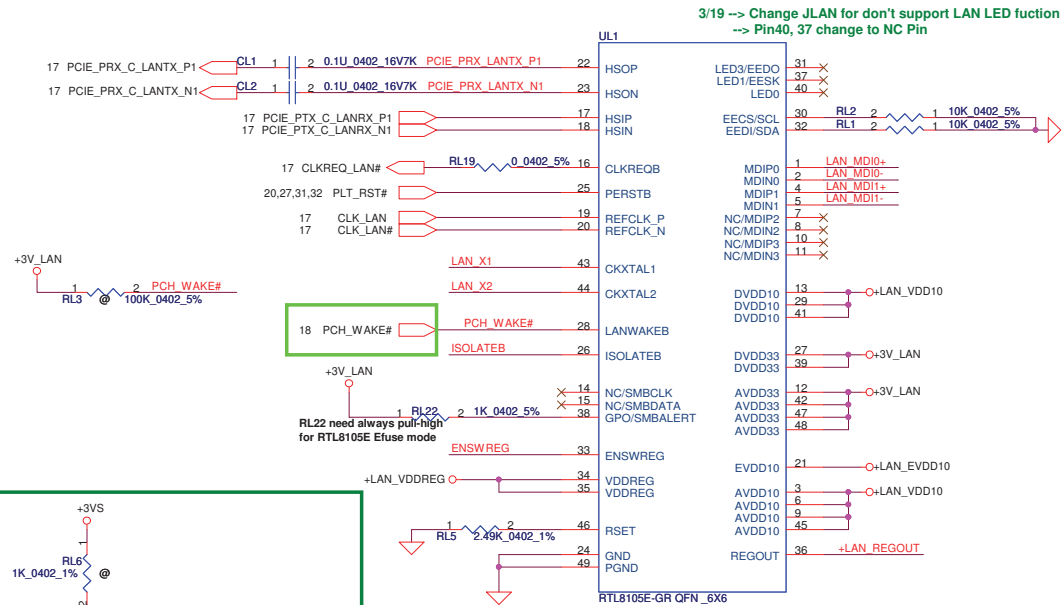
PCIe Mini Card-WLAN/WiMax



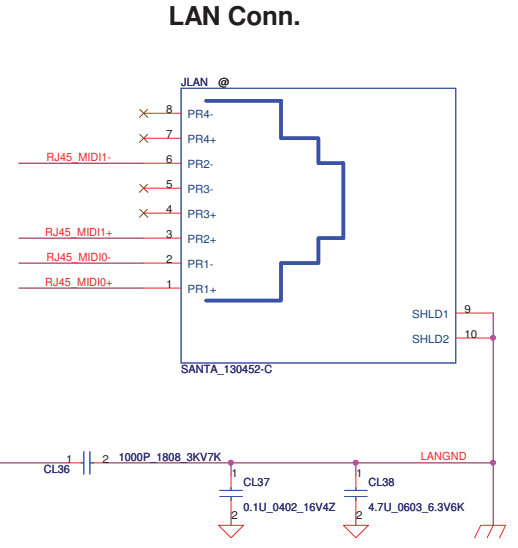
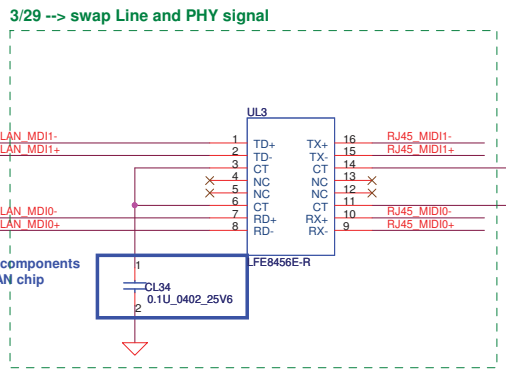
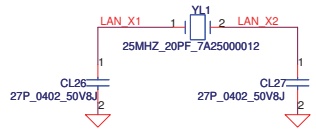
Slot#1 Half PCIe Mini Card-WLAN/WiMax



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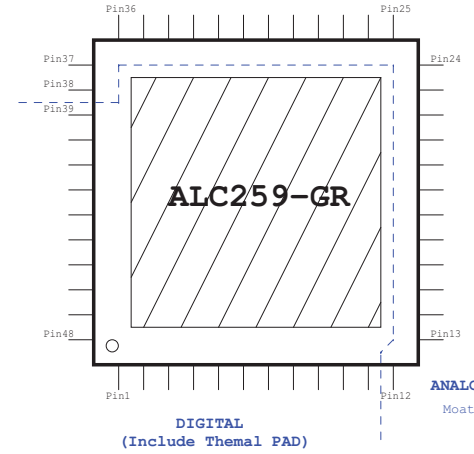
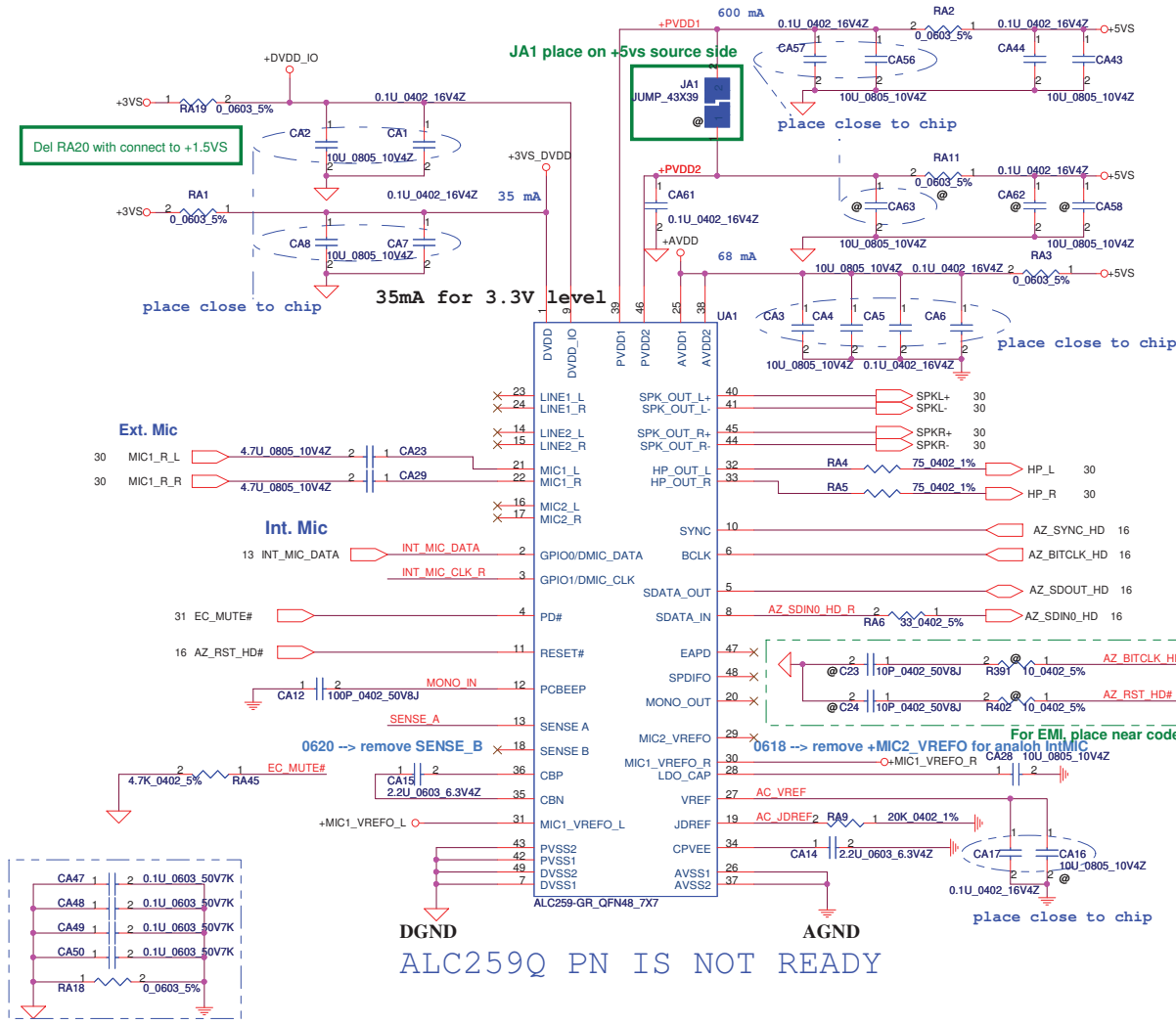


4/2-->remove RL8, RL9, CL11

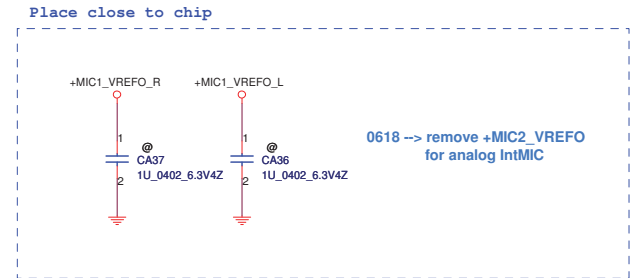
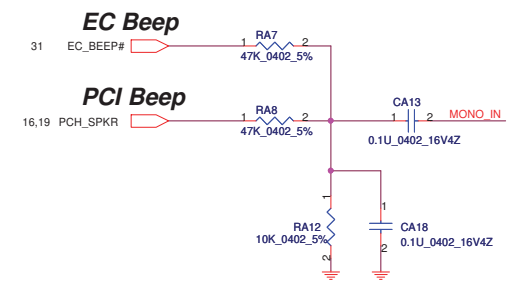


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			Date:	Wednesday, July 28, 2010	Sheet 28 of 45

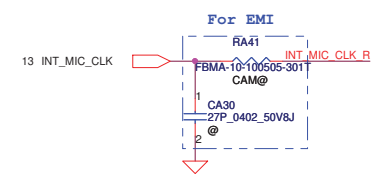
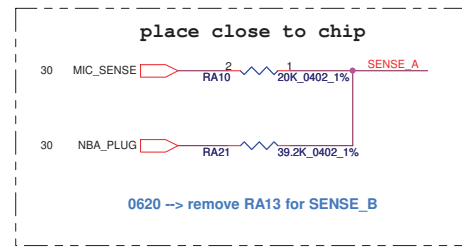
Codec



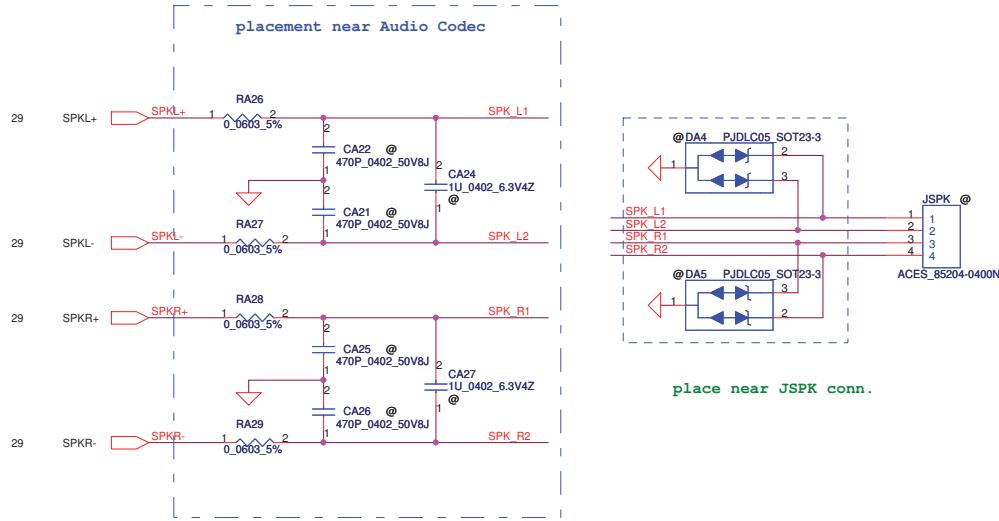
Beep sound



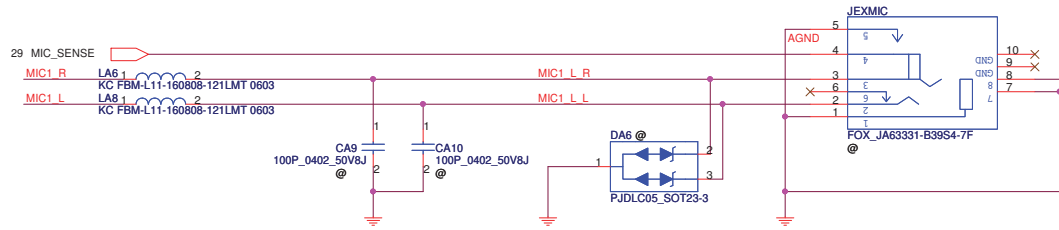
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	



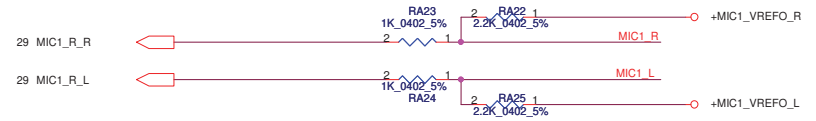
Speaker Connector



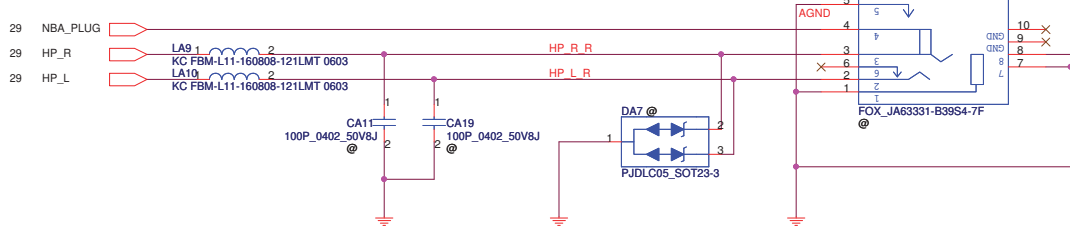
Ex.MIC JACK



Ext.MIC/LINE IN



Head Phone JACK

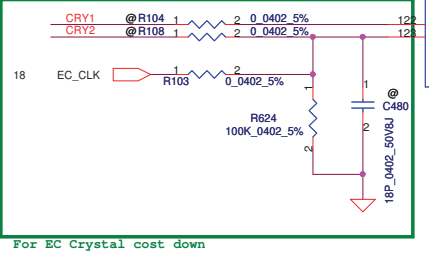
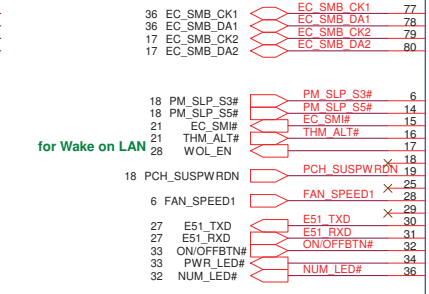
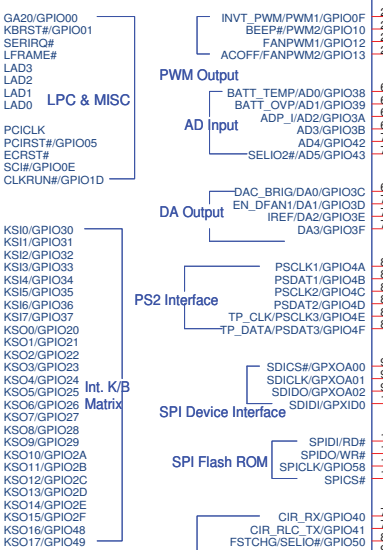
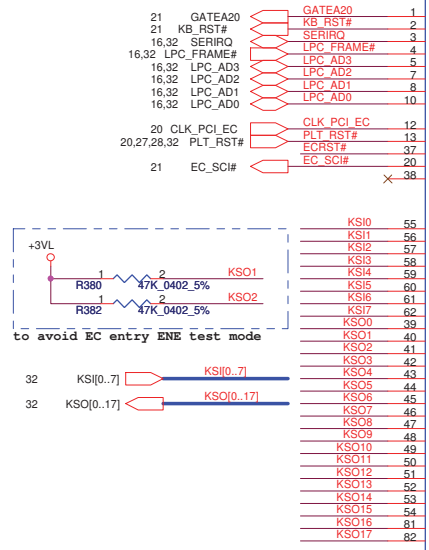
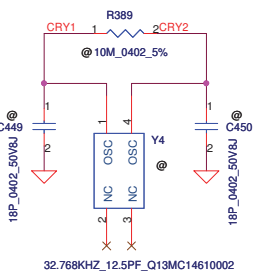
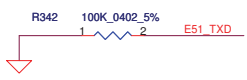
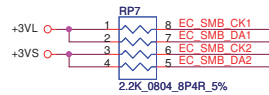
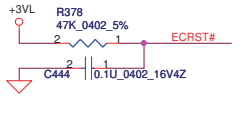
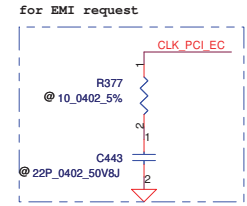
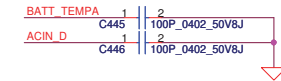
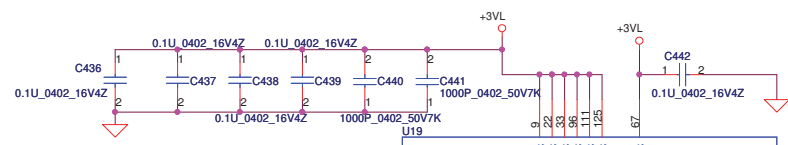


Int. Mic

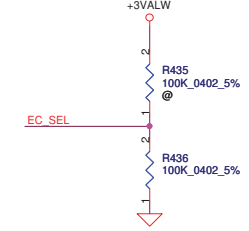
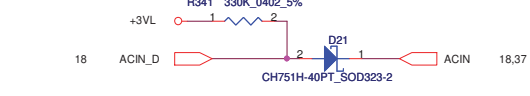
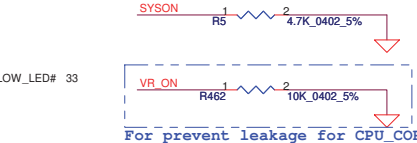
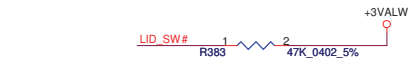
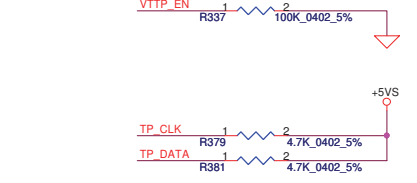
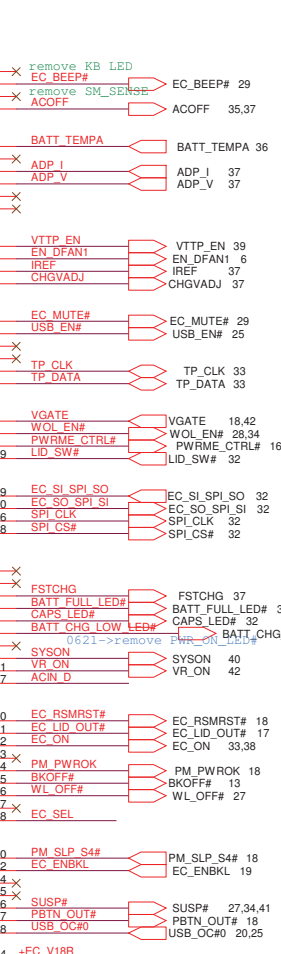
0618 --> remove Analog IntMIC, and change to DIGITAL MIC

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				HDA CODEC ALC259-GR	PWWAA LA6842P M/B	0.2
				Date: Wednesday, July 28, 2010	Sheet	30 of 45

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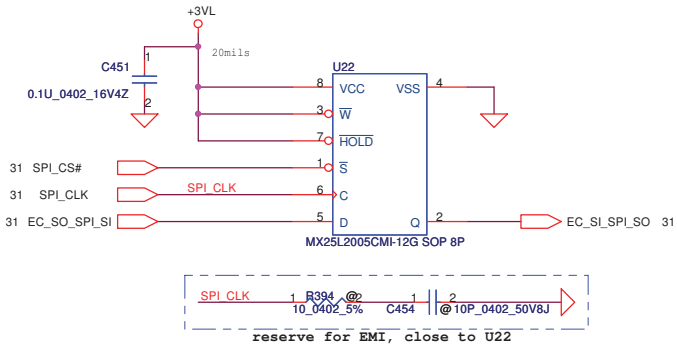
For EC Crystal cost down



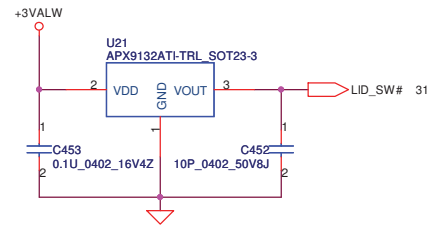
EC SEL		EC Version	
High	KB926D3	Low	KB926E0

Remove PM_SLP_S4#/S5# AND Gate

SPI Flash (256KB)

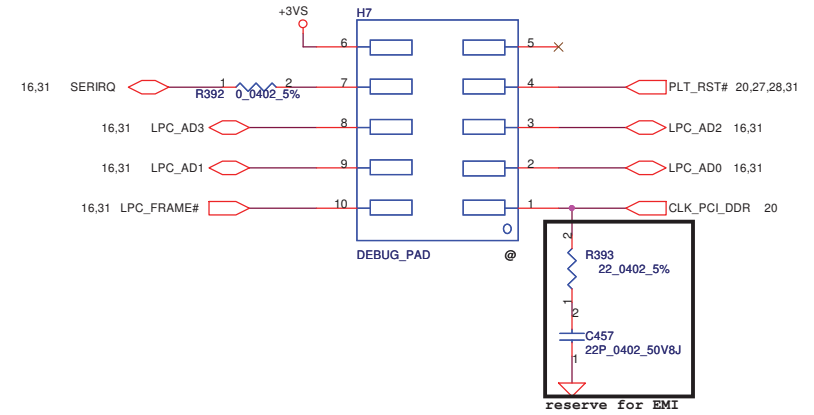


Lid SW



LPC Debug Port

Please place the PAD under DDR DIMM.

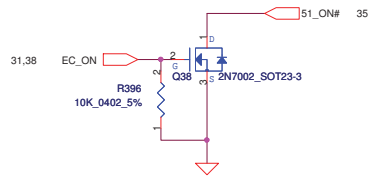
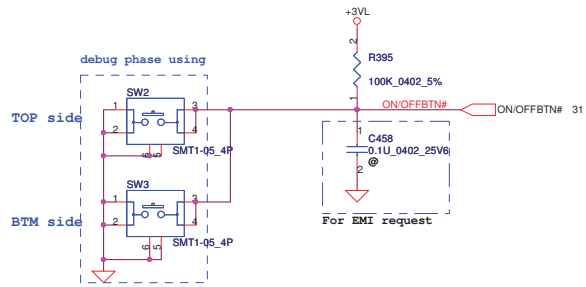


KEYBOARD CONN.

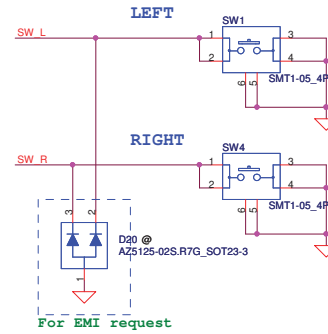


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Size	Document Number	PWWAA LA6842P M/B		Rev
				0.2
Date:	Wednesday, July 28, 2010	Sheet	32	of 45

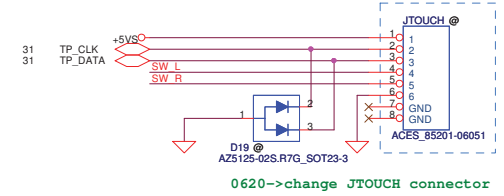
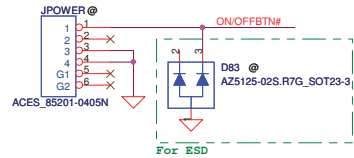
Power Button



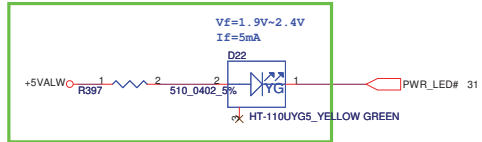
TP Button/Conn.



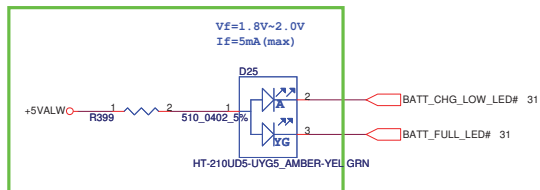
PWR/B to MB Conn.



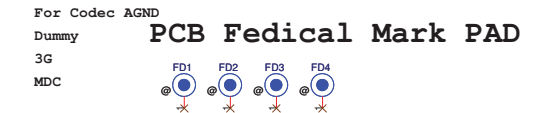
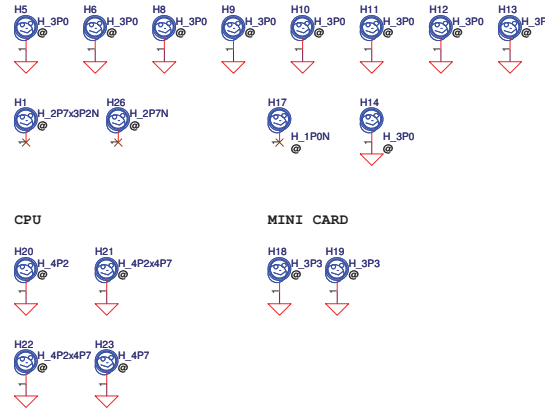
POWER/SUSPEND LED



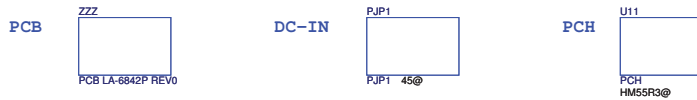
BATT CHARGE/FULL LED



Screw Hole

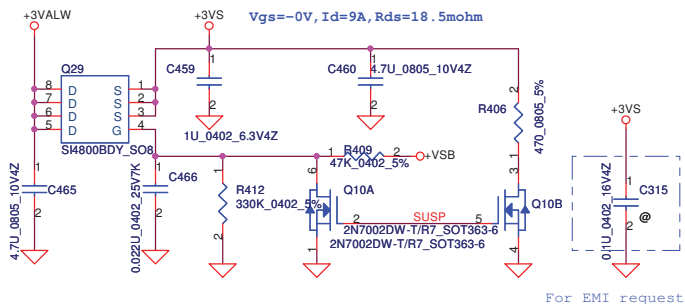


ISPD

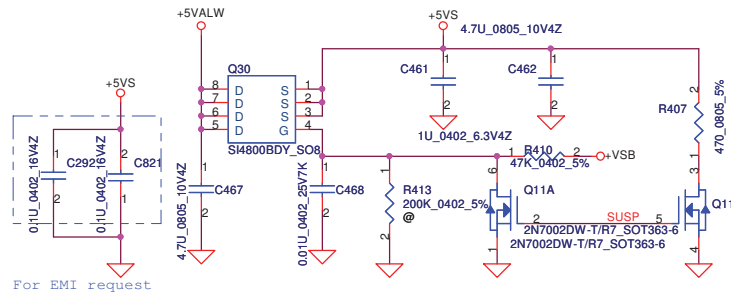


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Size	Document Number	PWWAA LA6842P M/B		0.2
Date	Wednesday, July 28, 2010	Sheet	33	of 45

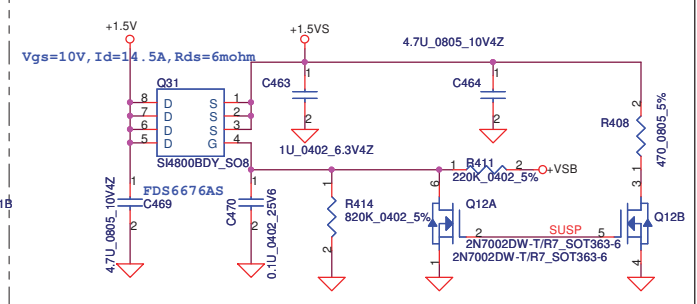
+3VALW TO +3VS



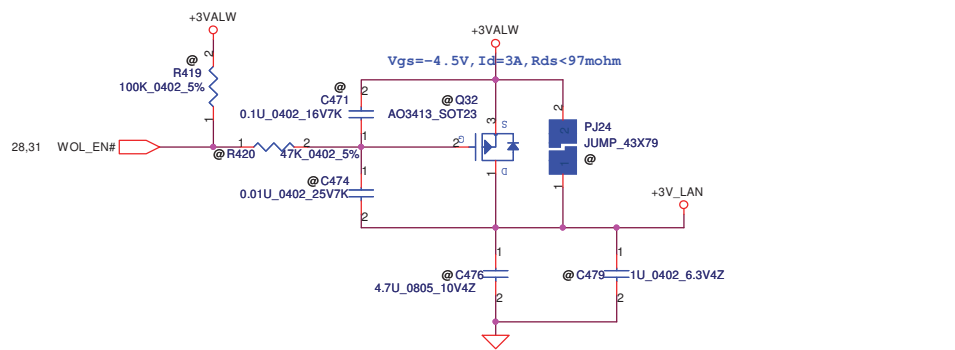
+5VALW TO +5VS



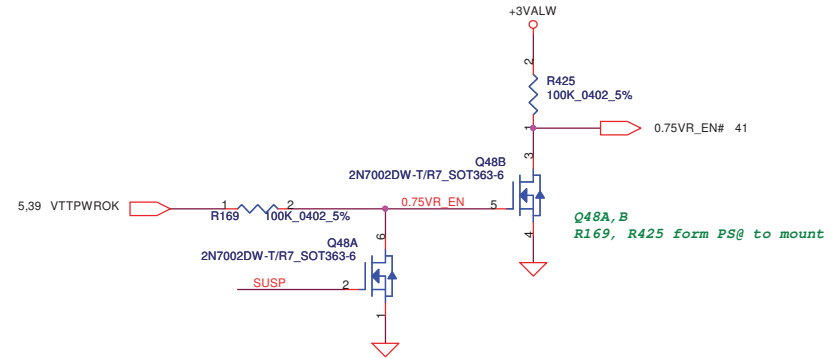
+1.5V to +1.5VS



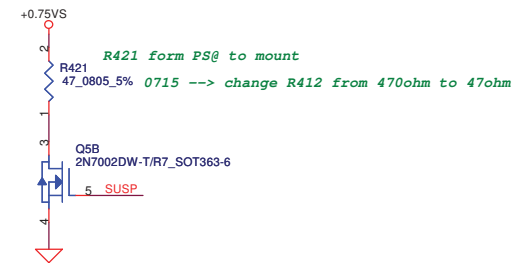
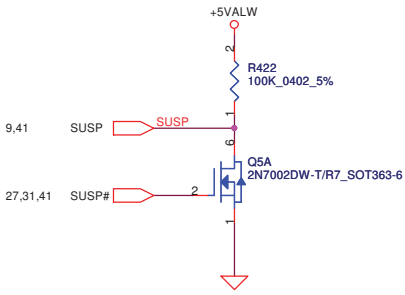
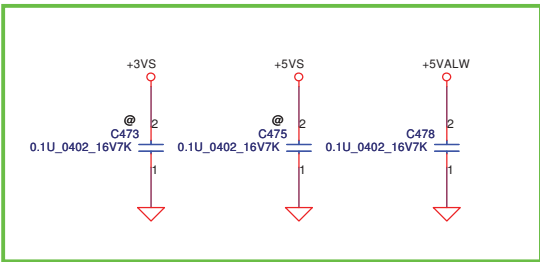
+3VALW TO +3V_LAN



For S3 CPU Power Saving



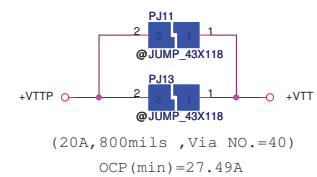
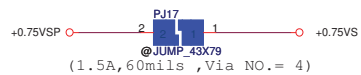
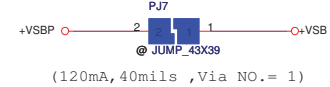
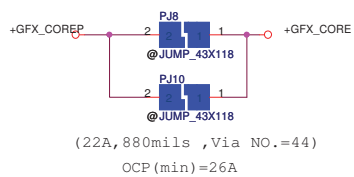
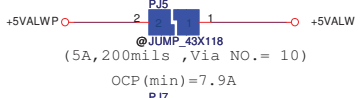
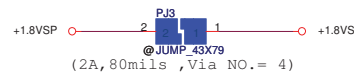
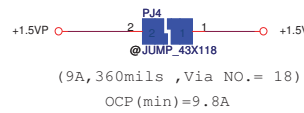
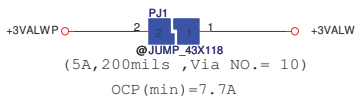
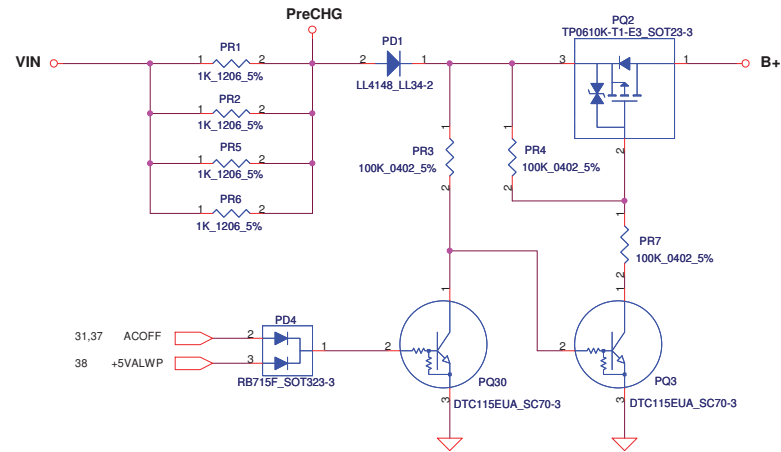
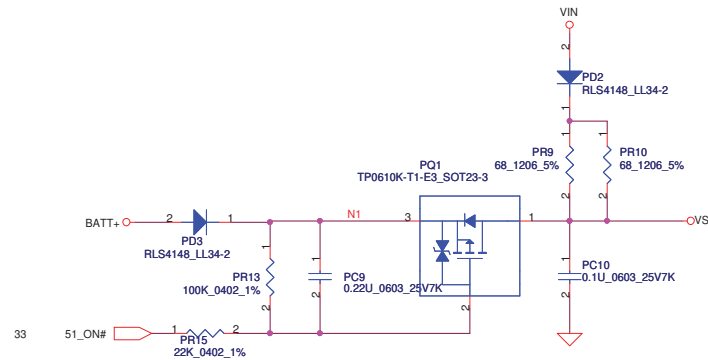
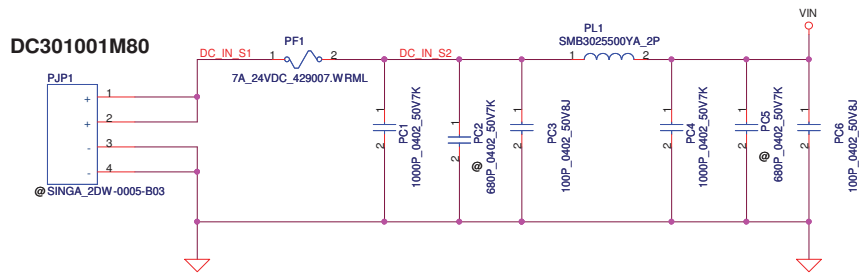
Reserve for EMI test



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Size	Document Number	Date		Sheet	Rev
	PWWAA LA6842P M/B	Wednesday, July 28, 2010		34	0.2
				of	45

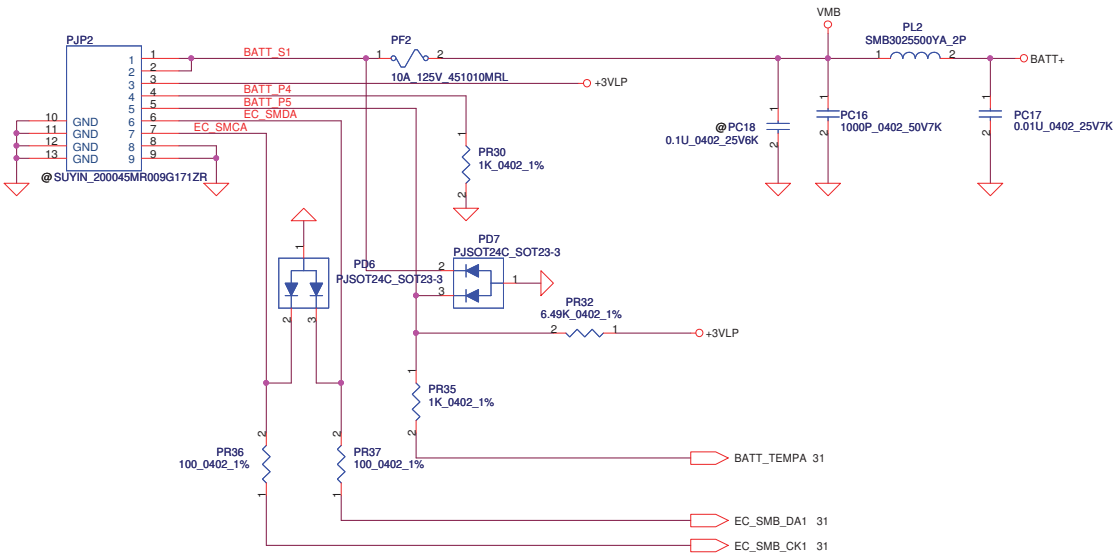
<http://laptop-motherboard-schematic.blogspot.com/>

DC301001M80

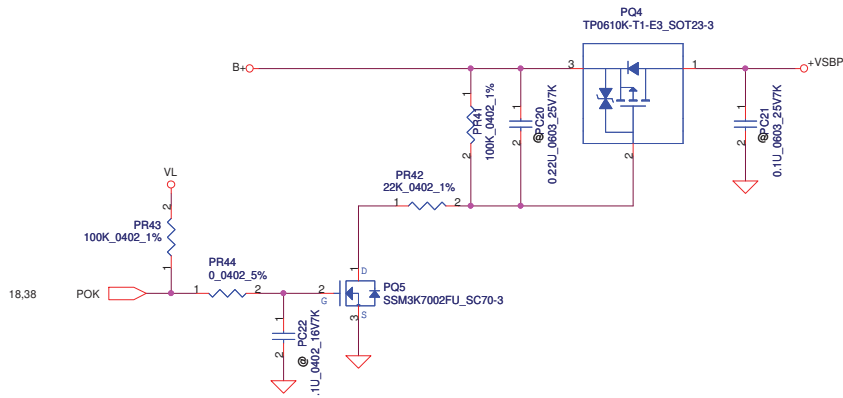
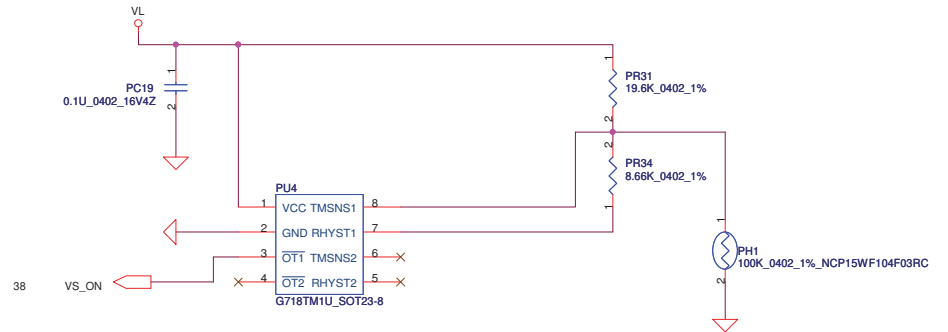


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Date:	Wednesday, July 28, 2010		Sheet		35		of 45	

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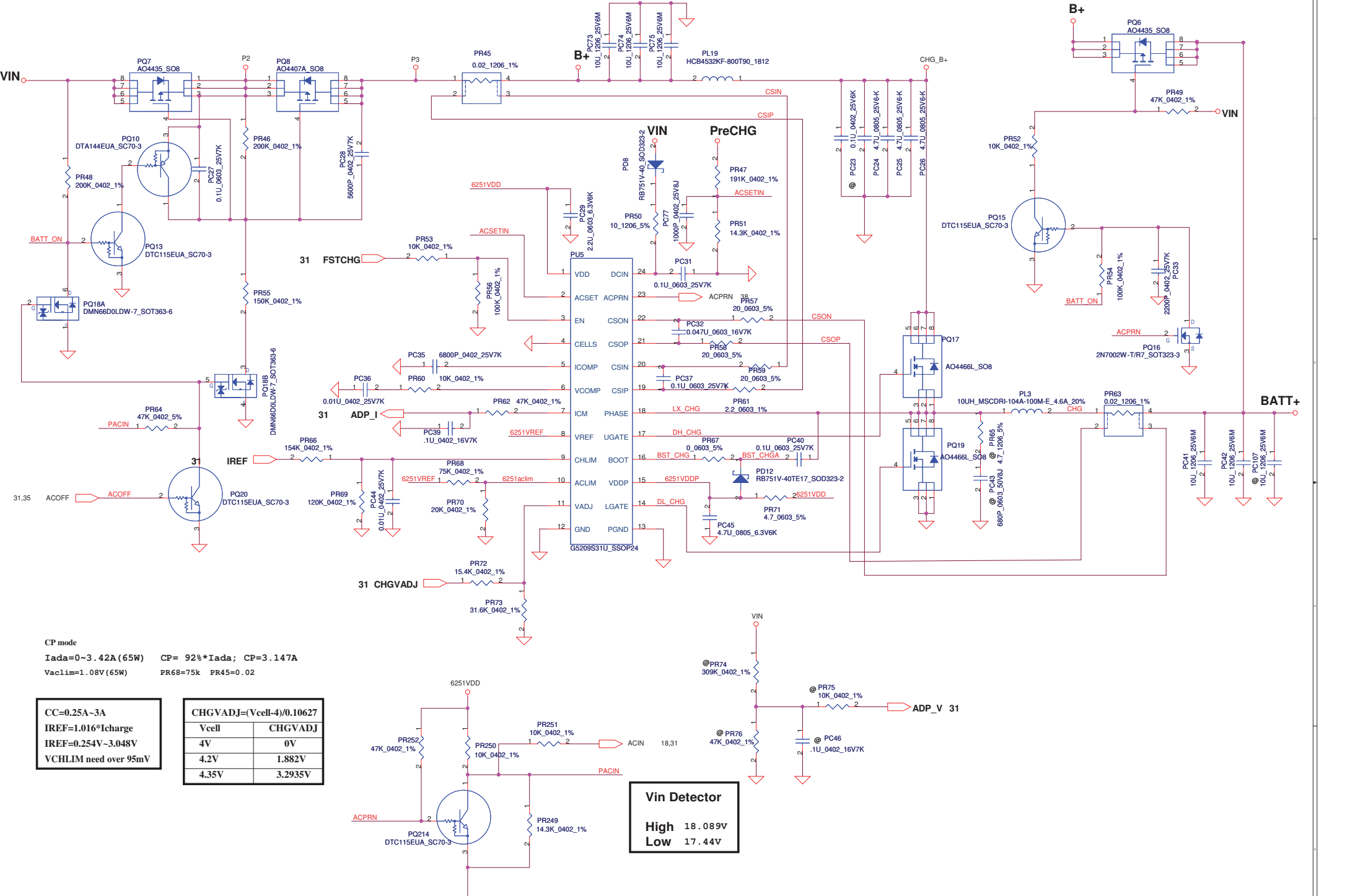


PH1 under CPU botten side :
 CPU thermal protection at 95degree C
 Recovery at 56 degree C



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Date:	Wednesday, July 28, 2010	Sheet	36	of	45

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CP mode
 $I_{ada} = 0 \sim 3.42A (65W)$ $CP = 92\% * I_{ada}$; $CP = 3.147A$
 $V_{aclim} = 1.08V (65W)$ $PR68 = 75k$ $PR45 = 0.02$

$CC = 0.25A \sim 3A$
 $I_{REF} = 1.016 * I_{charge}$
 $I_{REF} = 0.254V \sim 3.048V$
 V_{CHLIM} need over 95mV

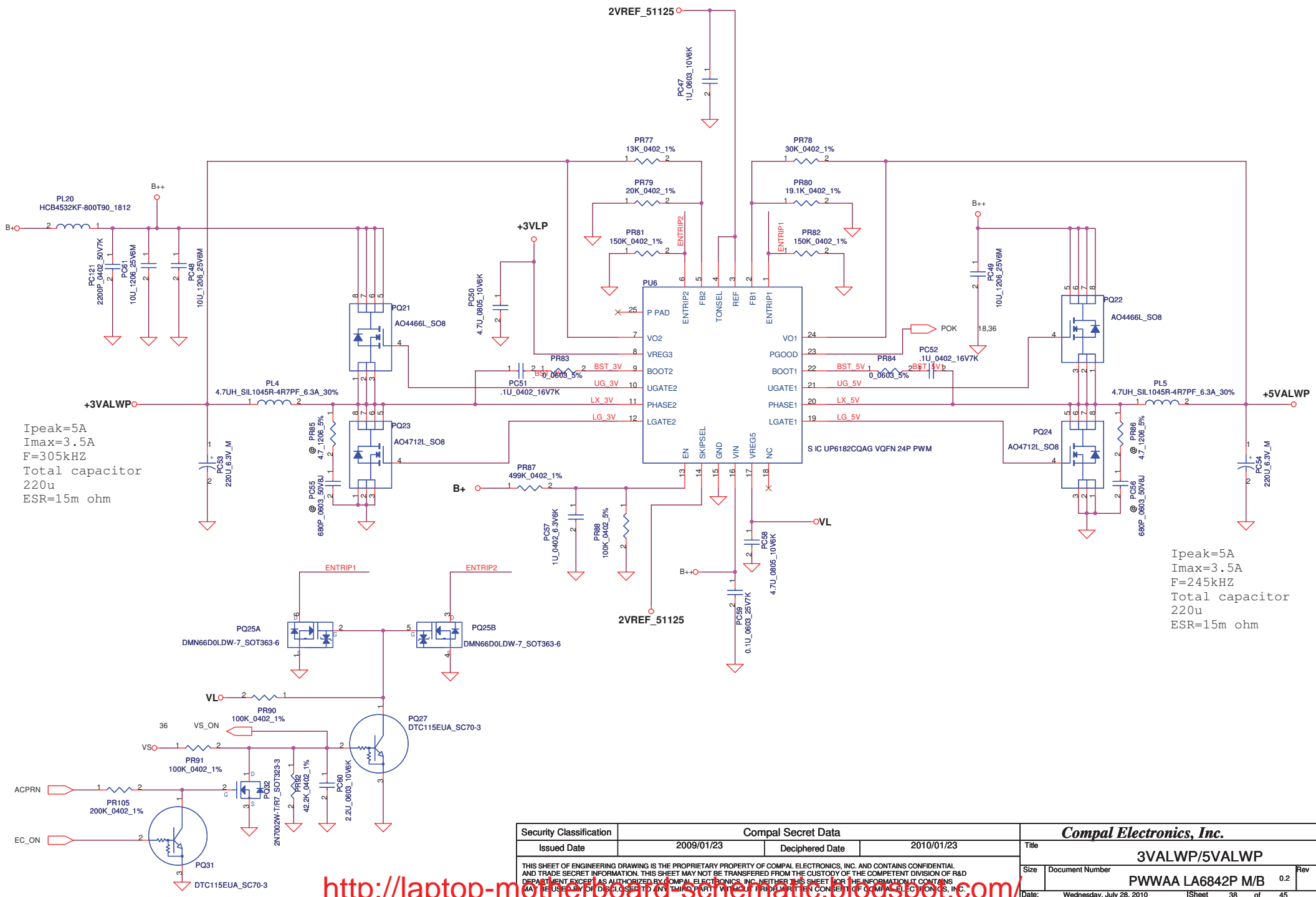
$CHGVADJ = (V_{cell} - 4) / 0.10627$

V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Vin Detector
 High 18.089V
 Low 17.44V

<http://laptop-moth.com> <http://www.cnhw.com> <http://www.hq.com>

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Date:	Wednesday, July 28, 2010	Sheet	37	of 45	

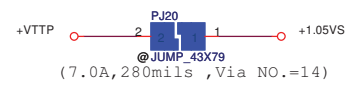
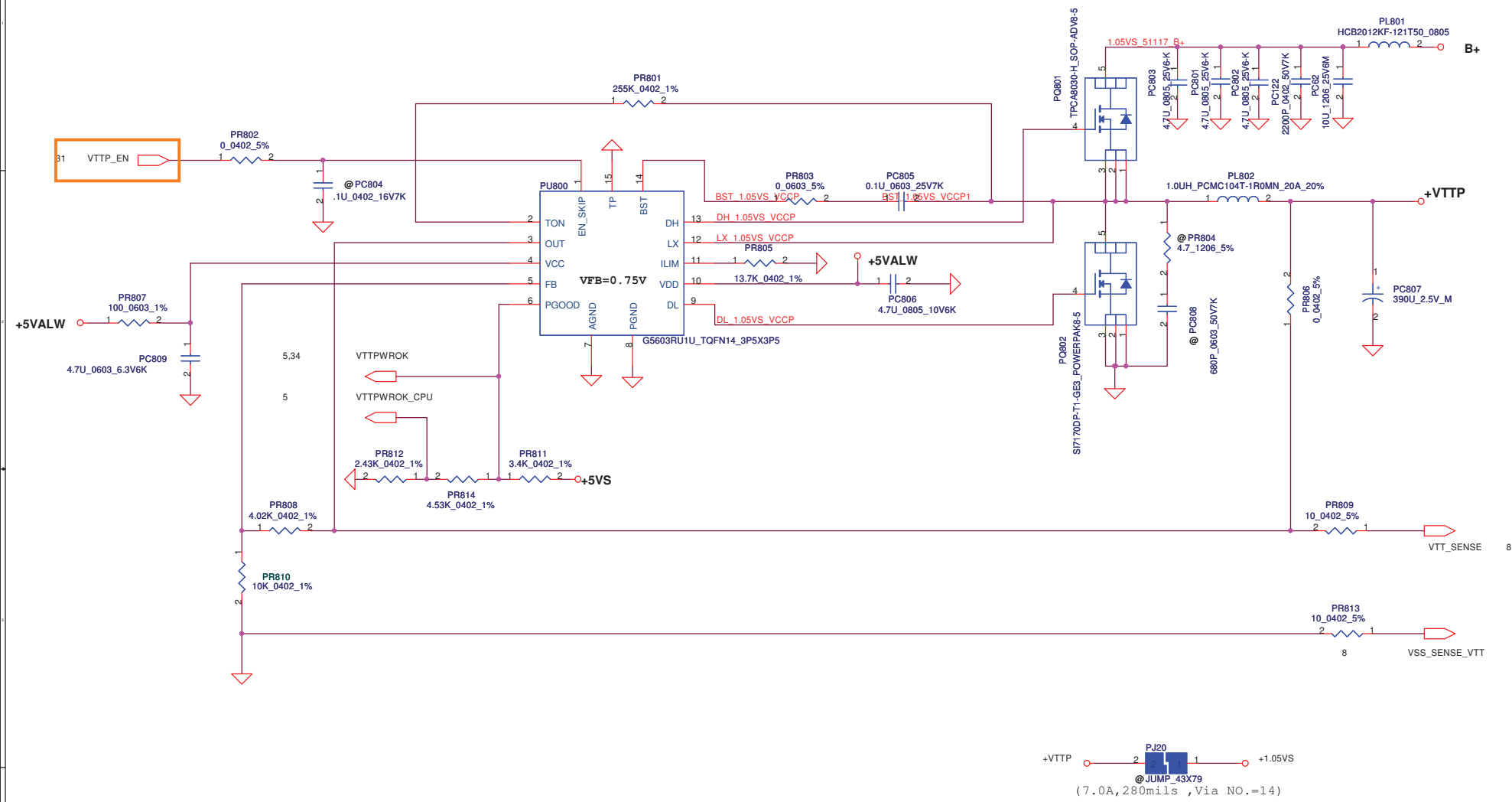


Ipeak=5A
 Imax=3.5A
 F=305kHz
 Total capacitor
 220u
 ESR=15m ohm

Ipeak=5A
 Imax=3.5A
 F=245kHz
 Total capacitor
 220u
 ESR=15m ohm

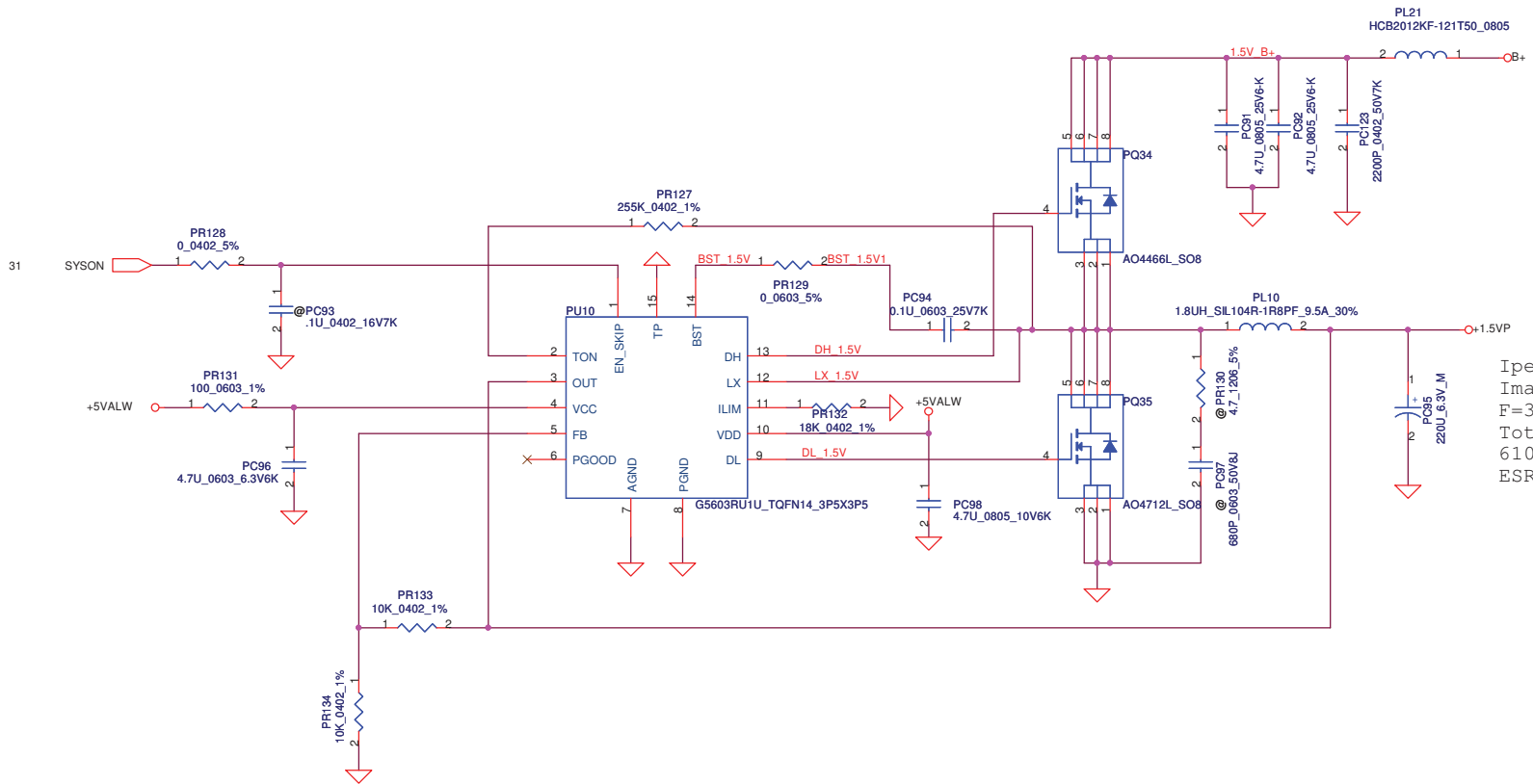
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Date	Wednesday, July 28, 2010	Sheet	38	of 45	

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				Date:	Wednesday, July 28, 2010	Sheet 39 of 45

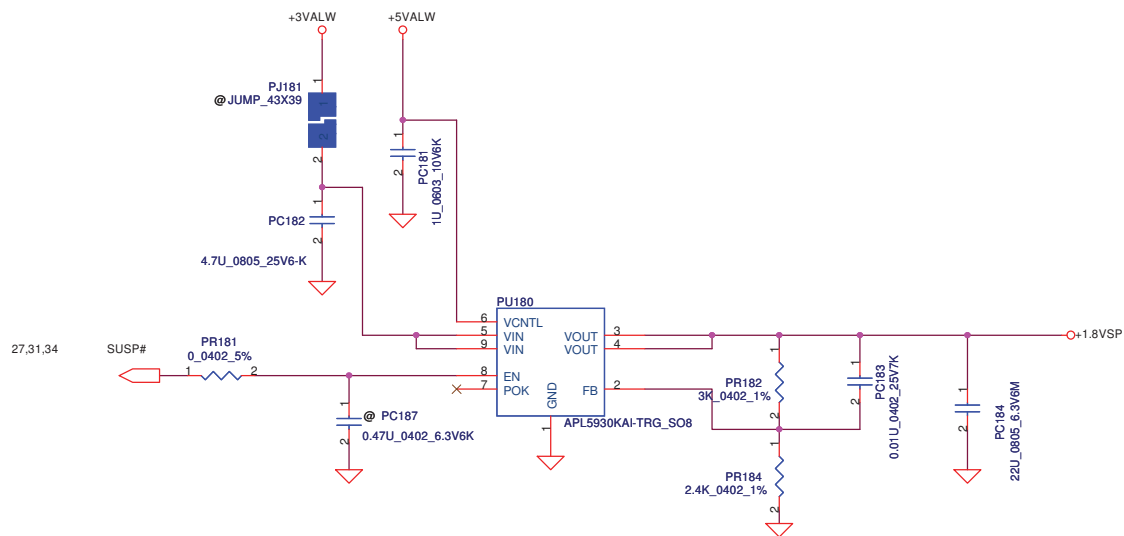
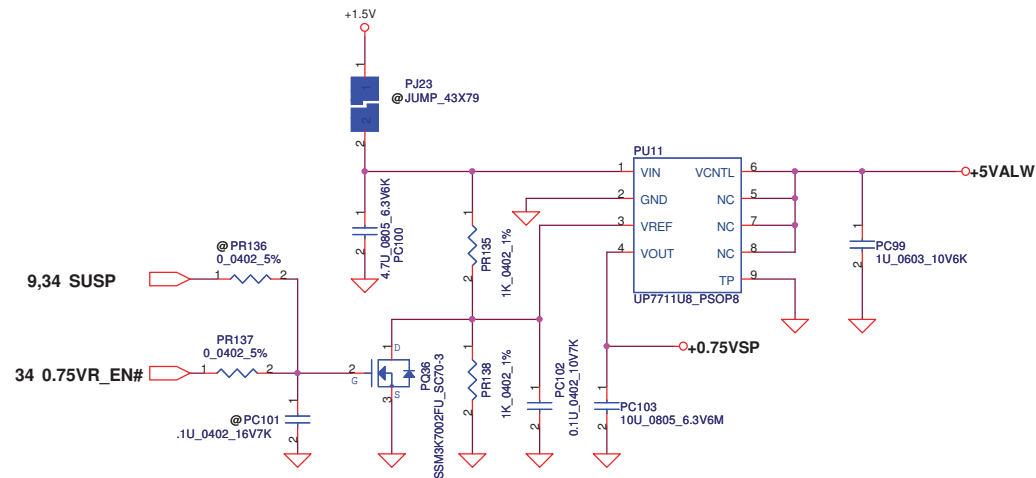
<http://laptop-motherboard-schematic.blogspot.com/>



$I_{peak}=9A$
 $I_{max}=6.3A$
 $F=313kHz$
 Total capacitor
 610u
 $ESR=5m\ ohm$

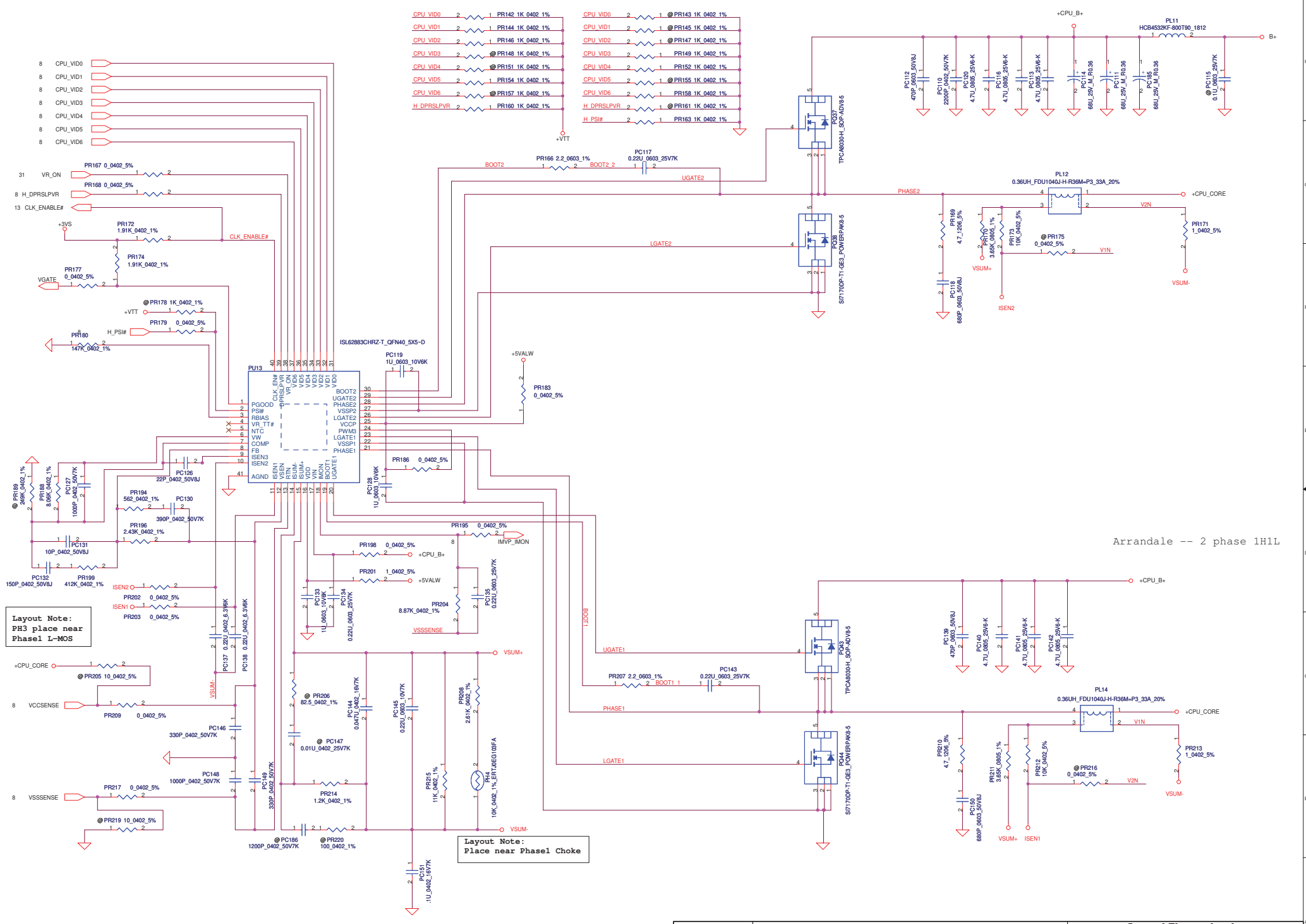
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				Date:	Wednesday, July 28, 2010
				Sheet	40 of 45
				Rev	0.2

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					PWWAA LA6842P M/B
				Date:	Wednesday, July 28, 2010
				Sheet	41 of 45
				Rev	0.2

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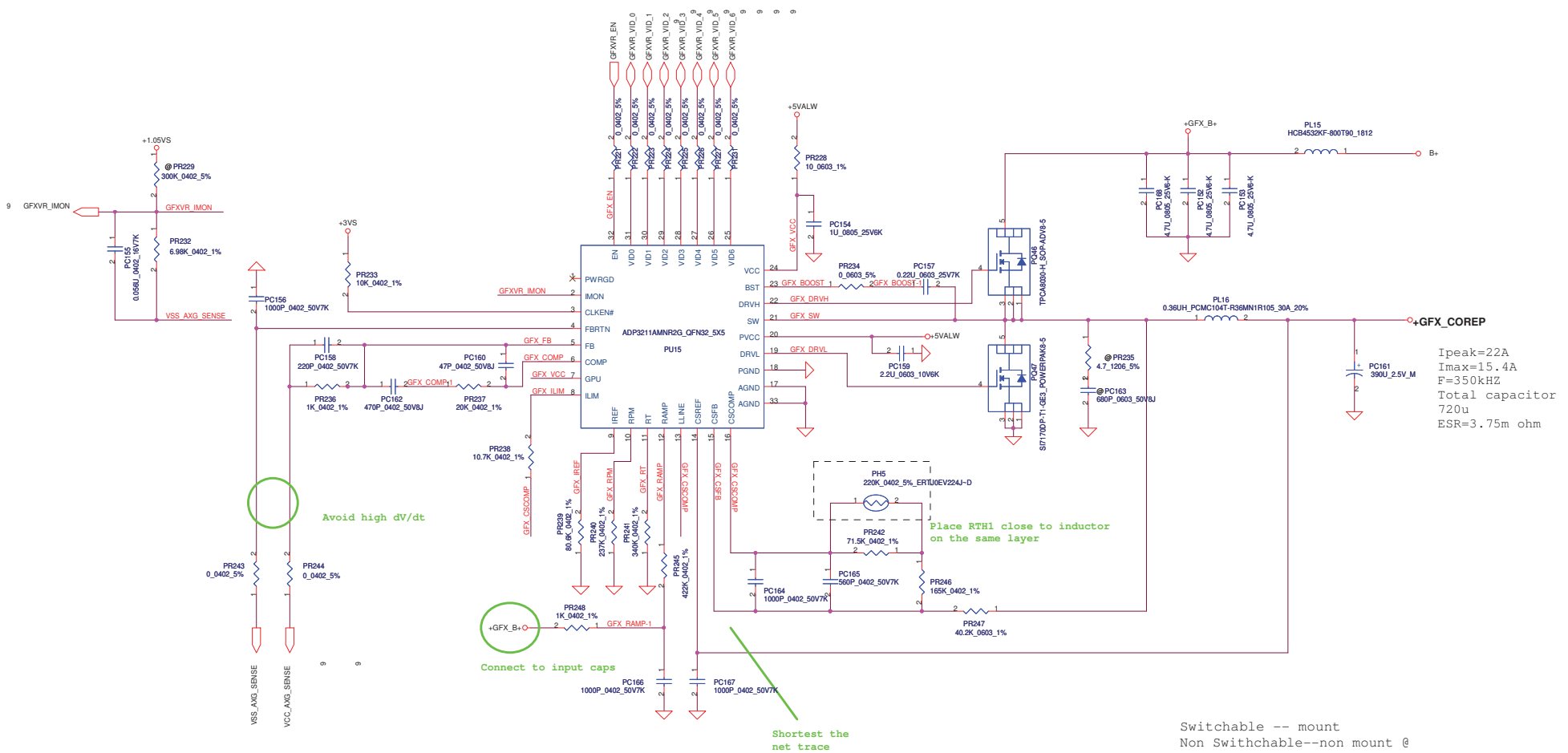


Arrandale -- 2 phase 1H1L

Layout Note:
PH3 place near
Phasel L-MOS

Layout Note:
Place near Phasel Choke

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Size	C	Document Number	PWWAA LA6842P M/B	Rev	0.2
Date:	Wednesday, July 29, 2010	Sheet	42	of	45



Avoid high dV/dt

Connect to input caps

Shortest the net trace

Place RTH1 close to inductor on the same layer

Switchable -- mount
Non Switchable--non mount @

Ipeak=22A
I_{max}=15.4A
F=350kHz
Total capacitor
720u
ESR=3.75m ohm

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				PWWAA LA6842P M/B	Rev 0.2
				Date: Wednesday, July 28, 2010	Sheet 43 of 45

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/07/13		42	Change PL12,PL14 to SH00000IN00	BOM modify
2010/07/13		43	Change PL16 to SH00000IN00	BOM modify
2010/07/23		36	Change PC19 to SE070104Z80	BOM modify
2010/07/26		36	Add PD6,PD7	EMI request
2010/07/26		37	Add PC73,PC74,PC75(10U_1206)	EMI request
2010/07/26		38	Add PC121(2200P_0402),PC61(10U_1206)	EMI request
2010/07/26		39	Add PC122(2200P_0402),PC62(10U_1206)	EMI request
2010/07/26		40	Add PC123(2200P_0402)	EMI request

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				Size	Document Number
				PWWAA LA6842P M/B	
				0.2	
Date:				Wednesday, July 28, 2010	
				Sheet 44 of 45	

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PIR (Product Improve Record)

PWWAA LA-6842P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1 TO 0.2
 GERBER-OUT DATE: 2010/07/31

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

1.	20100714 /	Page13	--> add 10u Cap to +1.5VS_CK505	For eSATA transmit issue ---> not add 10u Cap into schematic yet

NWQAA LA-6061P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 1.0 TO 2.0
 GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue

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Date:	Wednesday, July 28, 2010		Sheet	45 of 45