

COMPAL CONFIDENTIAL

MODEL NAME : *DBL10 -- Sapporo X*

COMPAL P/N : *DA8BL10L010*

PCB NO : *LA-1931*

Revision : *1.0*

DBL10 -- Sapporo X Schematics Document

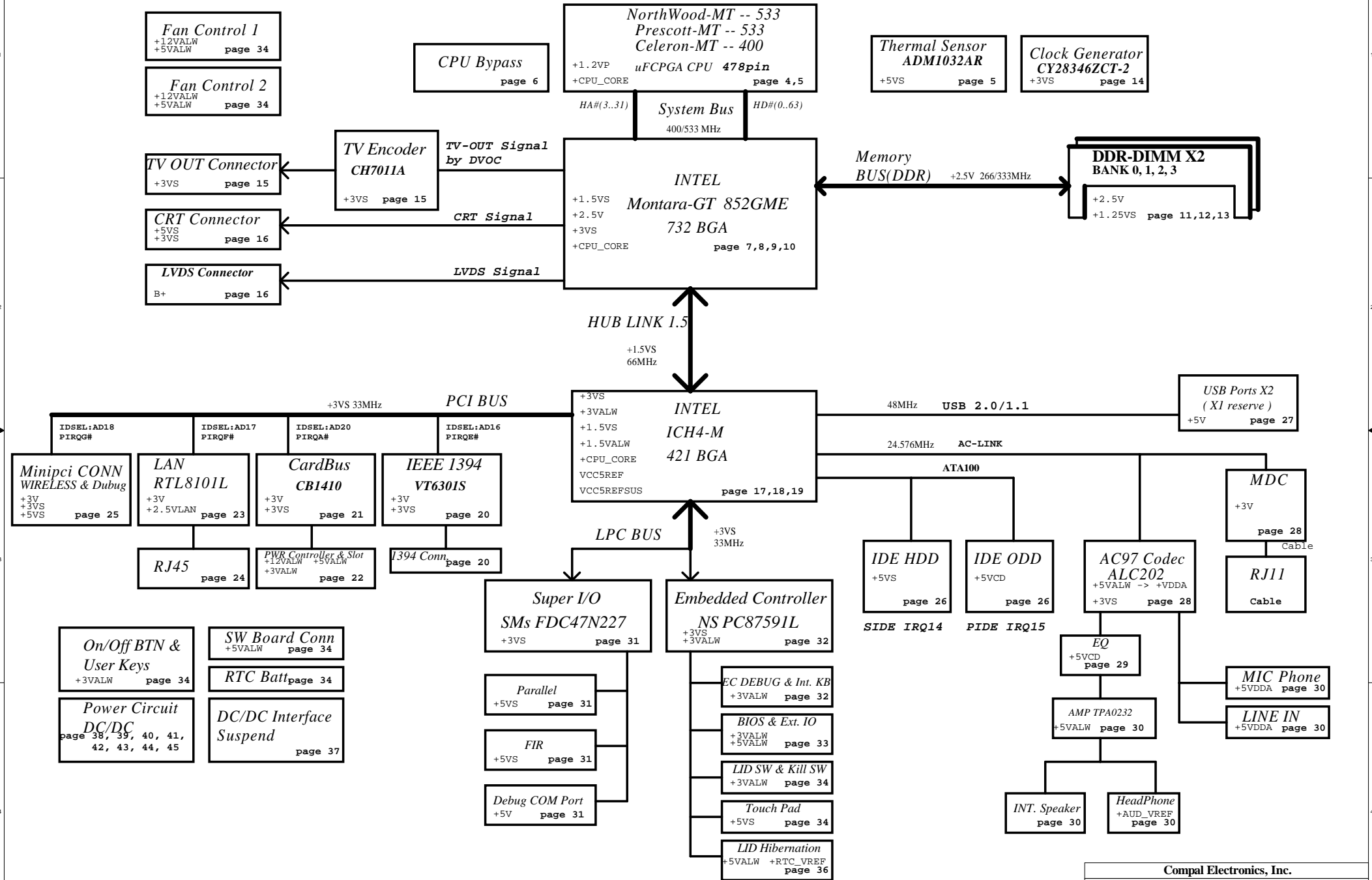
uFCBGA/uFCPGA NorthWood MT

2003-09-19 v1.0

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Model : DBL10 -- Sapporo X



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	1.2V switched power rail for CPU AGTL Bus	ON	ON	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Power Management table

Signal \ State	+1.5VALW +3VALW +5VALW +12VALW	+5V +3V +2.5V +1.2V	+5VS +3VS +1.5VS +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

External PCI Devices (follow PCI IRQ routing plannig ver0.2.04)

Device	IDSEL#	REQ#/GNT#	Interrupts - (ICH4-M)
CardBus (ENE-CB1410)	AD20	2	PIRQA#
IEEE 1394 (VIA-VT6301S)	AD16	0	PIRQE#
LAN (Realtek-RTL8101L)	AD17	3	PIRQF#
Mini-PCI	AD18	1 INTA#/INTB#	PIRQG# / PIRQH#

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16)	1010 000X b		

EC SM Bus2 address

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

ICH4 SM Bus address

Device	Address
CLK GEN (ICS-950810)	1101 001X

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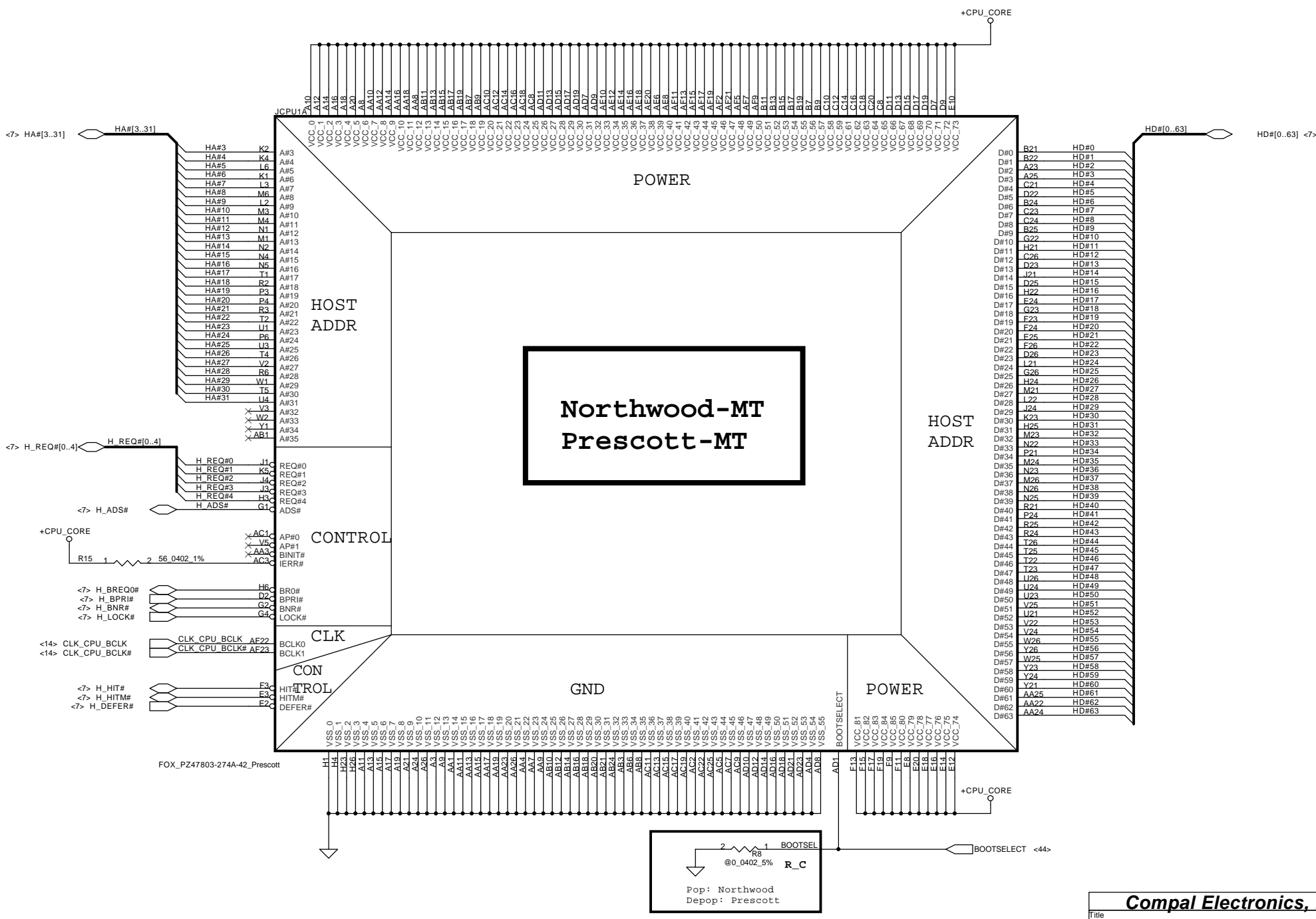
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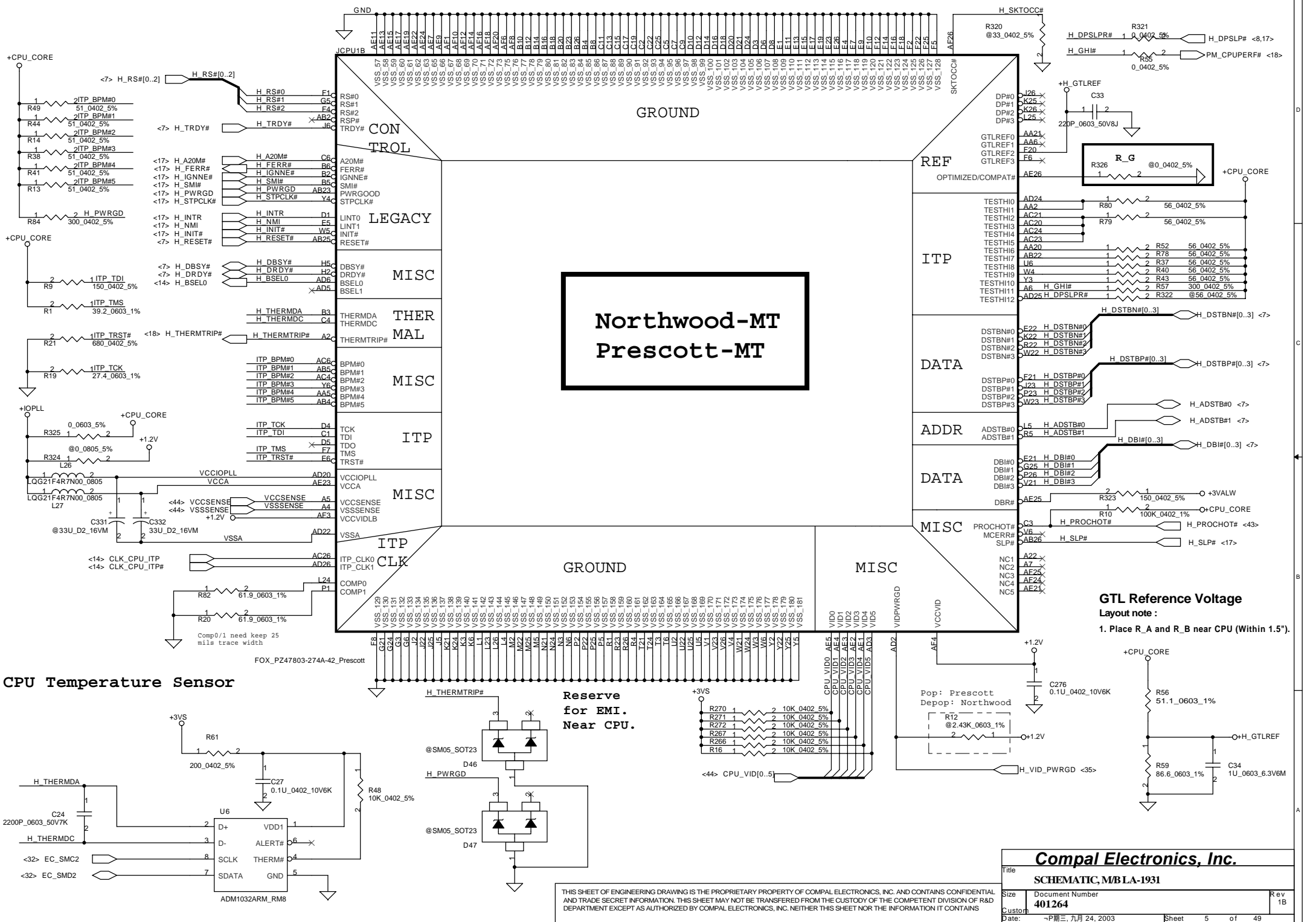
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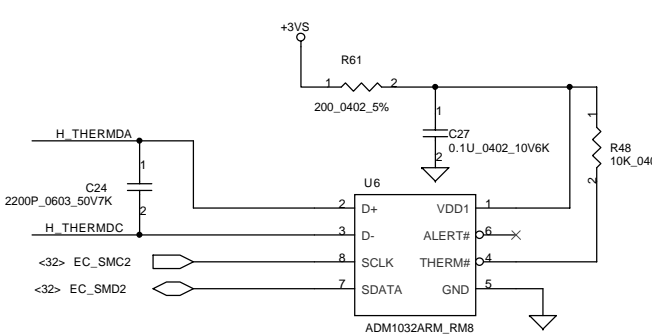
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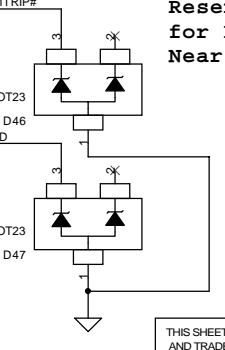
Northwood-MT Prescott-MT

GTL Reference Voltage
Layout note:
1. Place R_A and R_B near CPU (Within 1.5").

CPU Temperature Sensor



Reserve
for EMI.
Near CPU.



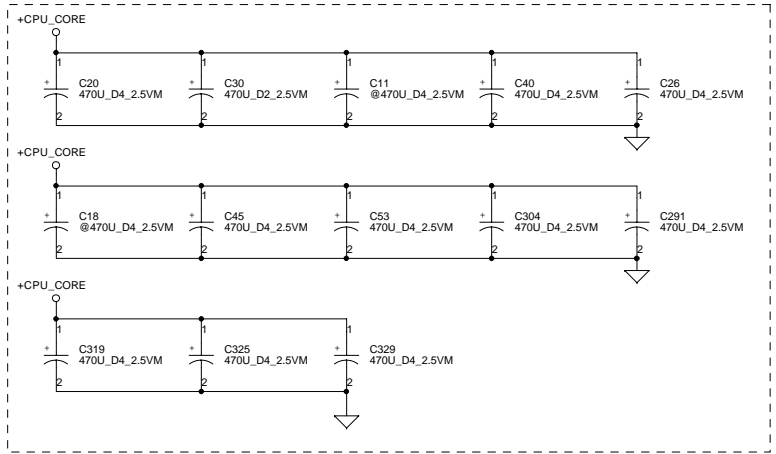
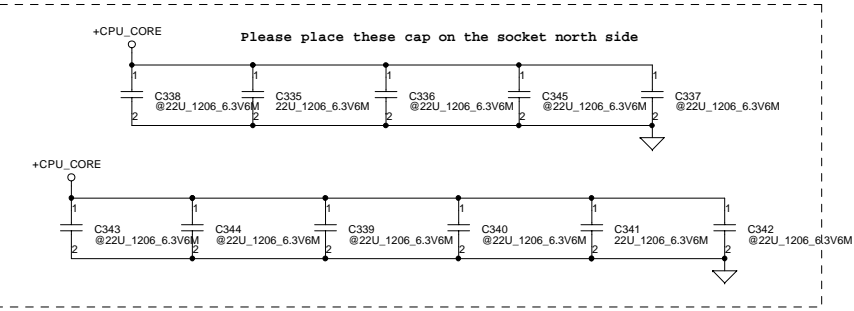
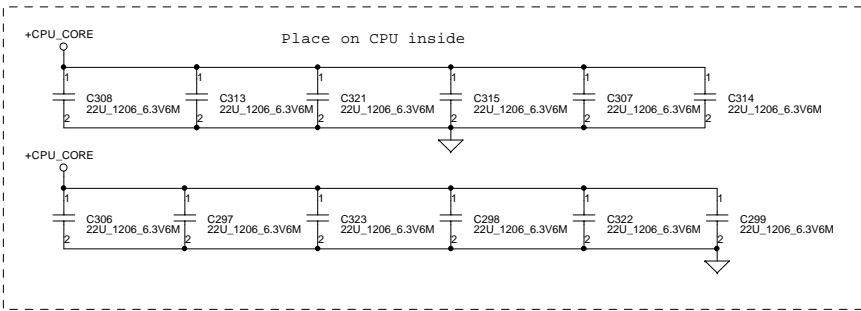
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Layout note :
 Place close to CPU. Use 2-3 vias per PAD.
 Place 22uF caps x31 pcs, populated 14pcs.

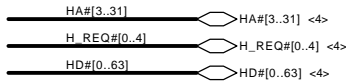
Layout note :
 Place close to CPU power and ground pin as possible (<1inch)

For Desktop's CPU:
 470uFx15/12mOhm H=1.8 each
 Total 0.923m ohm



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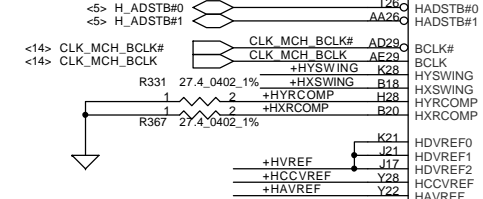
Montara-GT

HA#3	P23C	HA#3	HD#0	HD#0
HA#4	T25C	HA#4	H27	HD#1
HA#5	T28C	HA#5	K25	HD#2
HA#6	R27C	HA#6	L24	HD#3
HA#7	U23C	HA#7	J27	HD#4
HA#8	U24C	HA#8	G28	HD#5
HA#9	R24C	HA#9	L27	HD#6
HA#10	U28C	HA#10	L23	HD#7
HA#11	V28C	HA#11	L25	HD#8
HA#12	U27C	HA#12	J24	HD#9
HA#13	T27C	HA#13	H25	HD#10
HA#14	V27C	HA#14	K23	HD#11
HA#15	U25C	HA#15	G27	HD#12
HA#16	V26C	HA#16	K26	HD#13
HA#17	Y24C	HA#17	J23	HD#14
HA#18	V25C	HA#18	H26	HD#15
HA#19	V23C	HA#19	E25	HD#16
HA#20	W25C	HA#20	E26	HD#17
HA#21	Y25C	HA#21	B27	HD#18
HA#22	AA27C	HA#22	H23	HD#19
HA#23	W24C	HA#23	E27	HD#20
HA#24	W23C	HA#24	G25	HD#21
HA#25	W27C	HA#25	F28	HD#22
HA#26	Y27C	HA#26	D27	HD#23
HA#27	AA28C	HA#27	G24	HD#24
HA#28	W28C	HA#28	G28	HD#25
HA#29	AB27C	HA#29	E26	HD#26
HA#30	Y26C	HA#30	G22	HD#27
HA#31	AB28C	HA#31	C26	HD#28

HD#0	HD#0
HD#1	HD#1
HD#2	HD#2
HD#3	HD#3
HD#4	HD#4
HD#5	HD#5
HD#6	HD#6
HD#7	HD#7
HD#8	HD#8
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HD#13	HD#13
HD#14	HD#14
HD#15	HD#15
HD#16	HD#16
HD#17	HD#17
HD#18	HD#18
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HD#30	HD#30
HD#31	HD#31

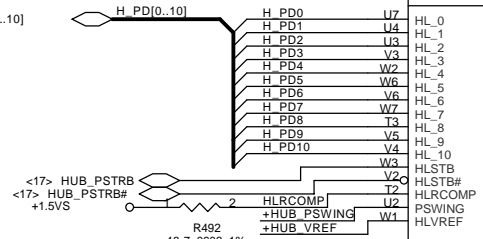
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H_REQ#1	P25C	H_REQ#1
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H_REQ#3	R25C	H_REQ#3
H_REQ#4	T23C	H_REQ#4

HOST



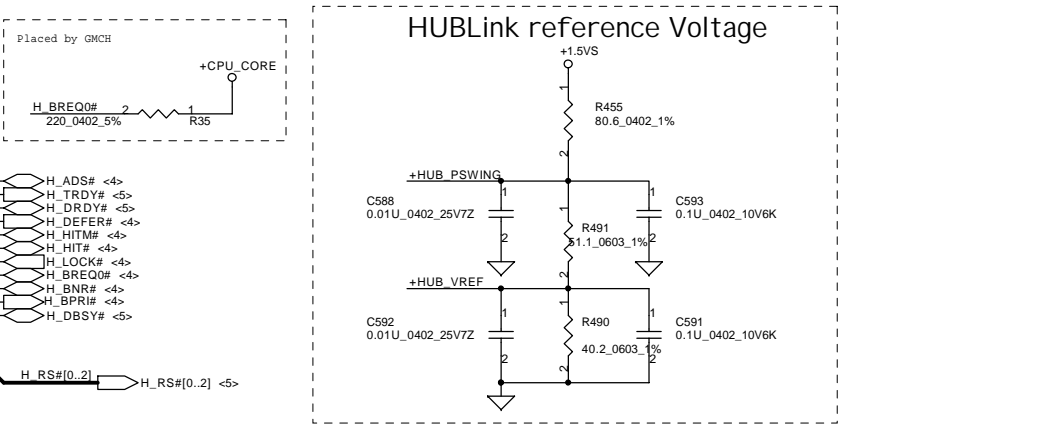
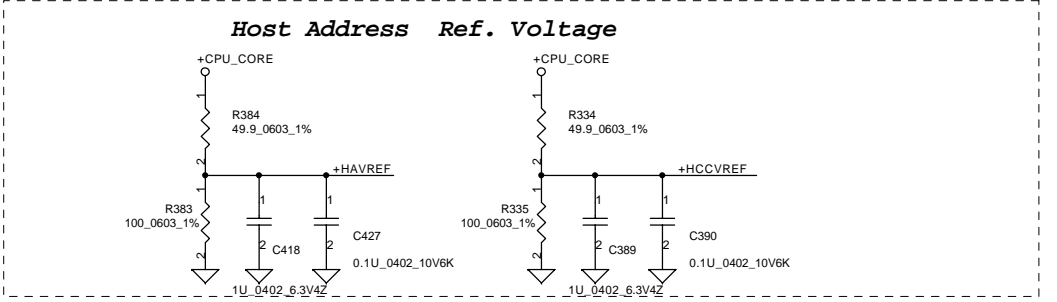
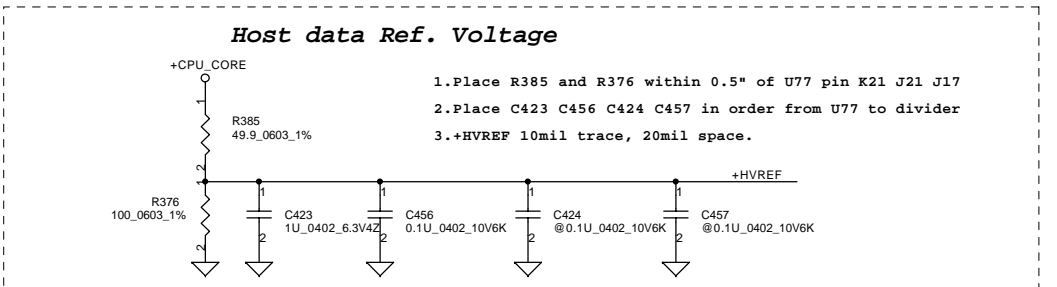
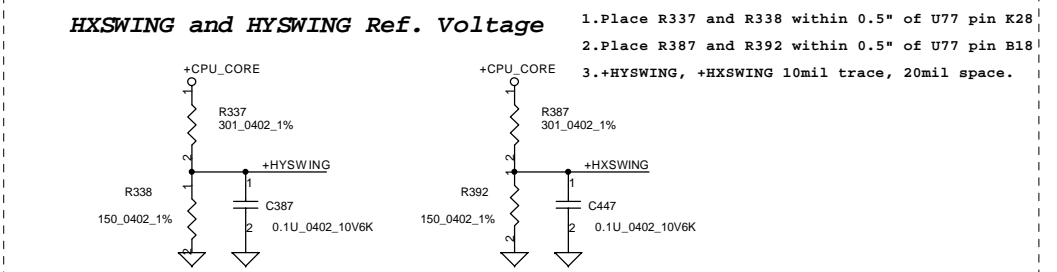
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H_DSTBN#2	E22C	HDSTBN#2
H_DSTBN#3	D18C	HDSTBN#3
H_DSTBP#0	K27C	HDSTBP#0
H_DSTBP#1	D26C	HDSTBP#1
H_DSTBP#2	E21C	HDSTBP#2
H_DSTBP#3	F14C	HDSTBP#3
H_DBI#0	J25C	DIN#0
H_DBI#1	E25C	DIN#1
H_DBI#2	B25C	DIN#2
H_DBI#3	G19C	DIN#3

H_RESET#	F15C	CPURST#
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HUB I / F

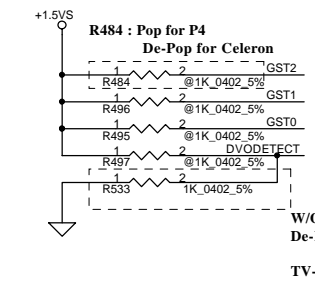
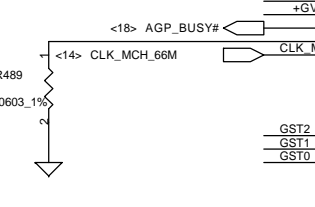
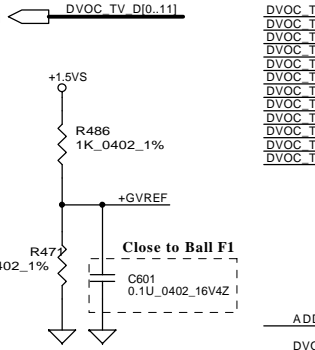
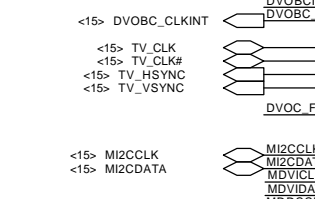
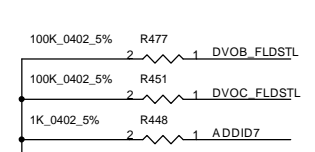
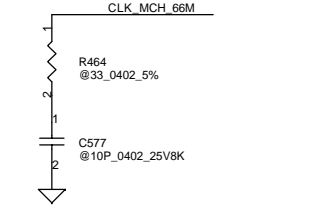
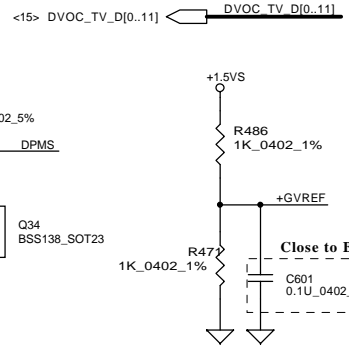
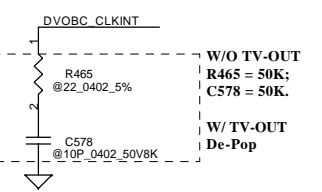
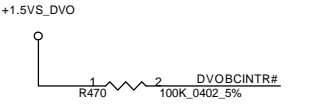
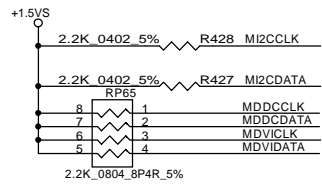
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HL_5	W6	HL_5
HL_6	W6	HL_6
HL_7	W7	HL_7
HL_8	T3	HL_8
HL_9	V5	HL_9
HL_10	V4	HL_10
HLSTB	W3	HLSTB
HLSTB#	V2C	HLSTB#
HLRCOMP	U2	HLRCOMP
PSWING	U1	PSWING
HLVREF	U1	HLVREF



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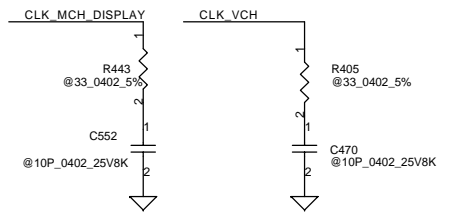
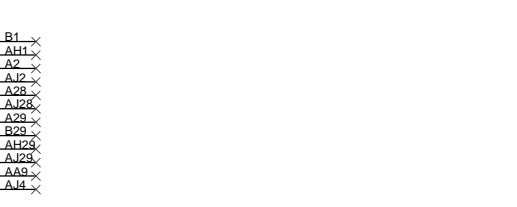
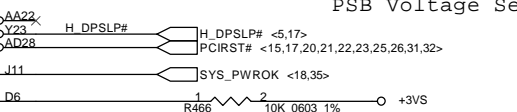
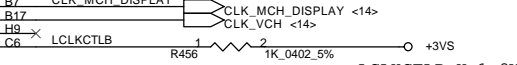
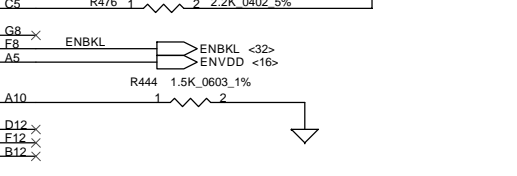
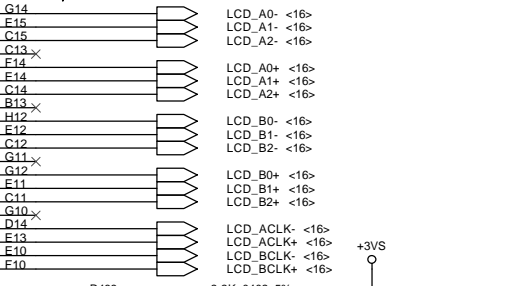
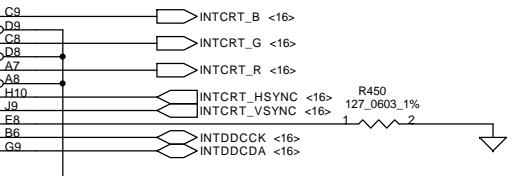
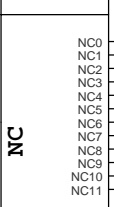
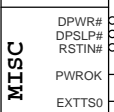
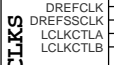
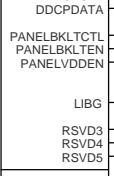
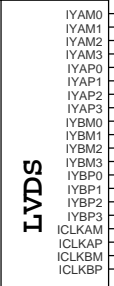
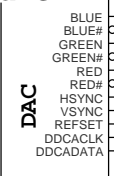
I2C BUS PULL UP



Montara-GT

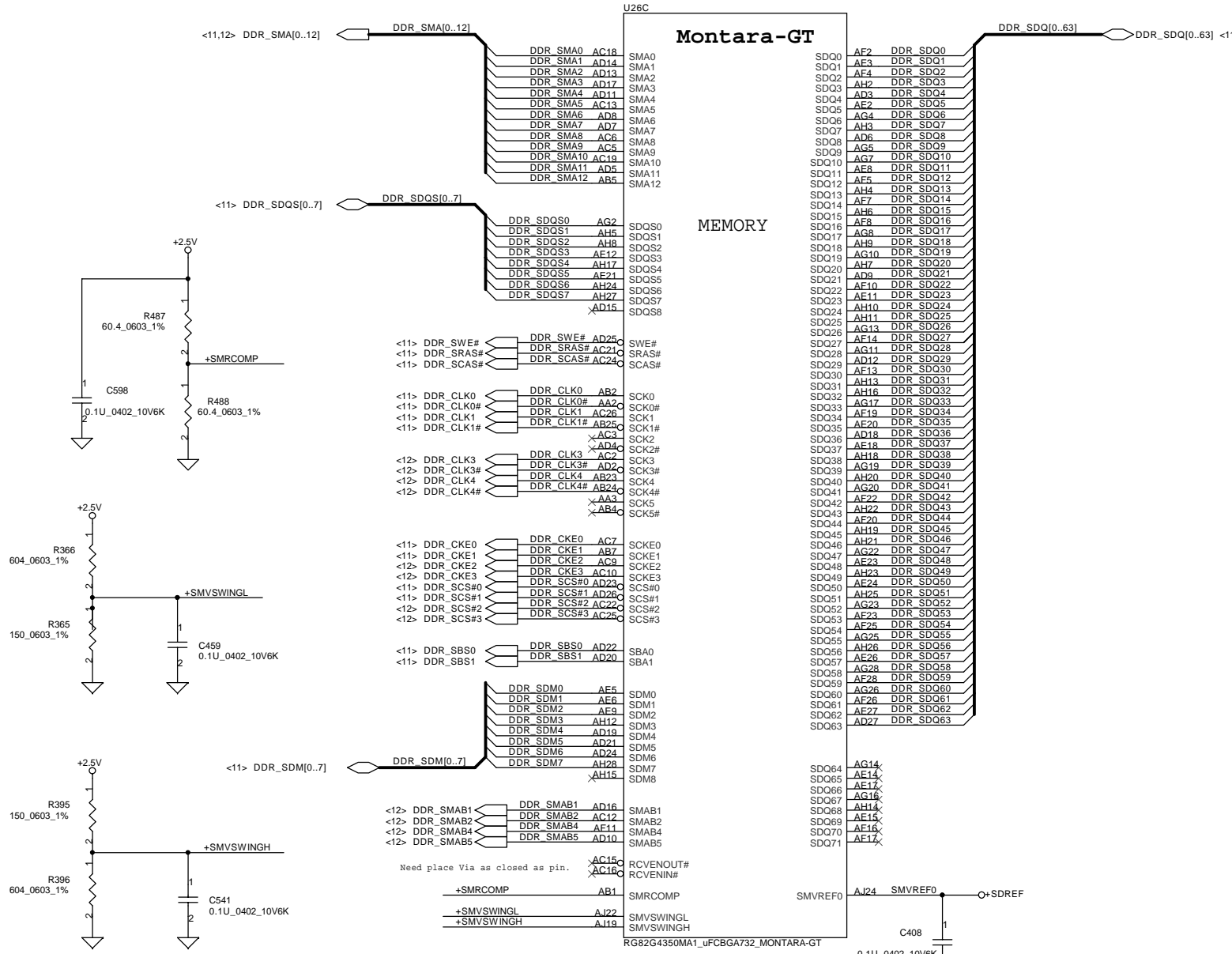
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P4	DVOBCLK#/GADSTB0#	P4	DVOBCLK#/GADSTB0#
T6	DVOBHSYNC/GAD0	T6	DVOBHSYNC/GAD0
T5	DVOBVS/GAD1	T5	DVOBVS/GAD1
L2C	DVOBBLANK#/GCBE1#	L2C	DVOBBLANK#/GCBE1#
M2	DVOBFLDSTL/GAD14	M2	DVOBFLDSTL/GAD14
G2C	DVOBCINTR#	G2C	DVOBCINTR#/GAD30
M3	DVOBC CLKINT	M3	DVOBCCLKINT#/GAD13
J3	DVOCCCLK/GADSTB1	J3	DVOCCCLK/GADSTB1#
J2	DVOCHSYNC/GAD17	J2	DVOCHSYNC/GAD17
K6	DVOCHSYNC/GAD17	K6	DVOCHSYNC/GAD17
L5	DVOCVSYNC/GAD16	L5	DVOCVSYNC/GAD16
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K3	DVOC2/GAD21	K3	DVOC2/GAD21
K2	DVOC3/GAD22	K2	DVOC3/GAD22
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H1	DVOC7/GAD24	H1	DVOC7/GAD24
H4	DVOC8/GAD27	H4	DVOC8/GAD27
H6	DVOC9/GAD26	H6	DVOC9/GAD26
G3	DVOC10/GAD29	G3	DVOC10/GAD29
G2	DVOC11/GAD28	G2	DVOC11/GAD28
E5	ADDID0/GSBA0	E5	ADDID0/GSBA0
F5	ADDID1/GSBA1	F5	ADDID1/GSBA1
E3	ADDID2/GSBA2	E3	ADDID2/GSBA2
E2	ADDID3/GSBA3	E2	ADDID3/GSBA3
G5	ADDID4/GSBA4	G5	ADDID4/GSBA4
F4	ADDID5/GSBA5	F4	ADDID5/GSBA5
G6	ADDID6/GSBA6	G6	ADDID6/GSBA6
F6	ADDID7/GSBA7	F6	ADDID7/GSBA7
L7	DVODETECT/GPAR	L7	DVODETECT/GPAR
D5	DPMS/GPIPE#	D5	DPMS/GPIPE#
F1	GVREF	F1	GVREF
E7C	AGPBUSY#	E7C	AGPBUSY#
D1C	DVO_GRCOMP	D1C	DVO_GRCOMP
Y3	GCLKIN	Y3	GCLKIN
F2	GSBSTB	F2	GSBSTB
E3	GSBSTB#	E3	GSBSTB#
B2C	GGNT#	B2C	GGNT#
B3C	GREQ#	B3C	GREQ#
C2	GST2	C2	GST2
C3	GST1	C3	GST1
C4	GST0	C4	GST0
D2C	GWBF#	D2C	GWBF#
D3C	GRBF#	D3C	GRBF#
L4C	GCBE#2	L4C	GCBE#2
D7	RSVD1	D7	RSVD1
AA5	RSVD2	AA5	RSVD2



LCLKCTLB H:1.2V
PSB Voltage Select

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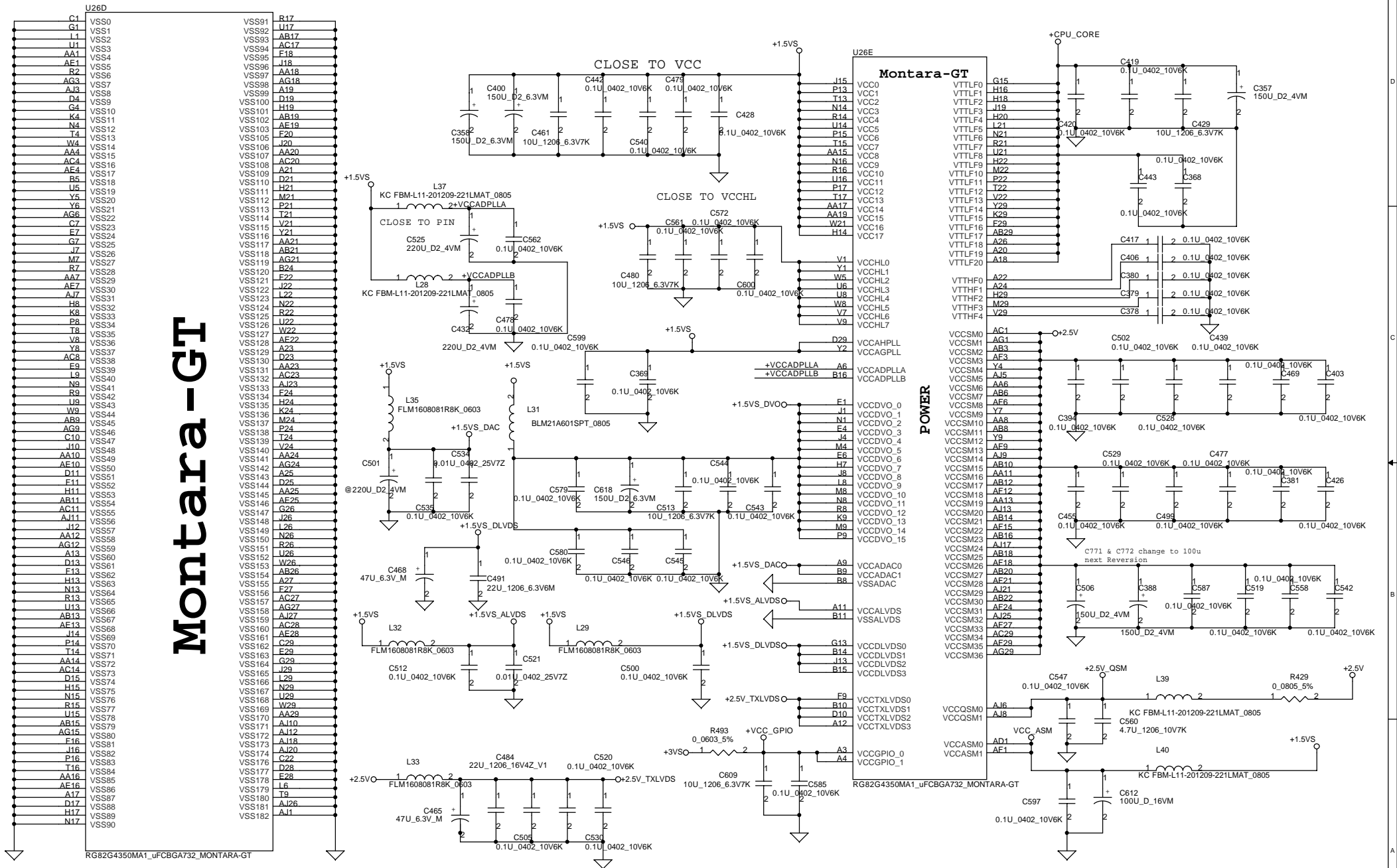


TOPOLOGY 1 FOR DDR
 SMAA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

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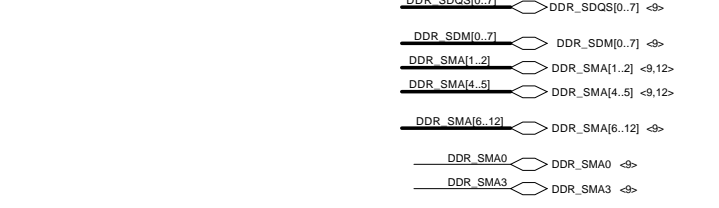
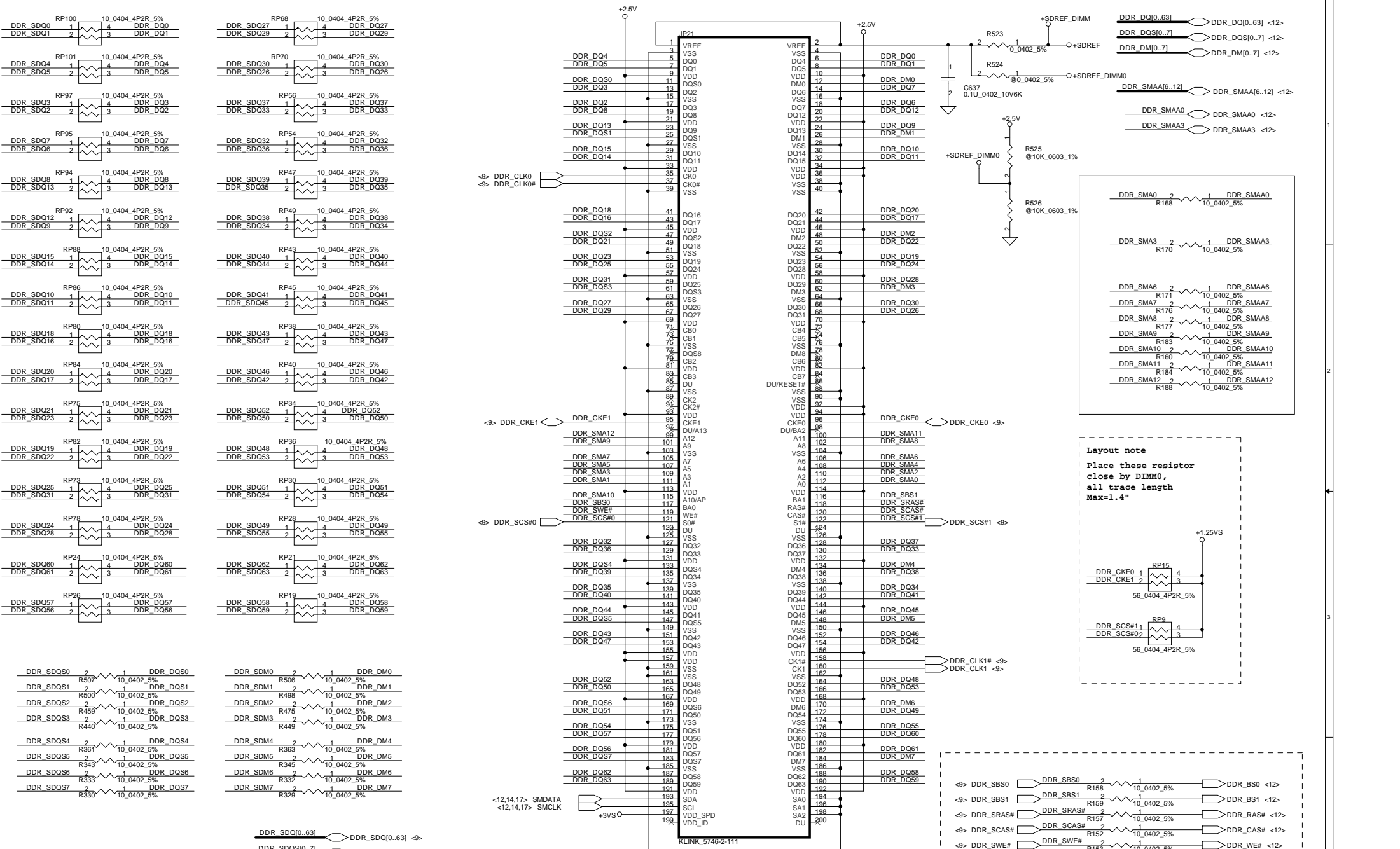
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Montara-GT



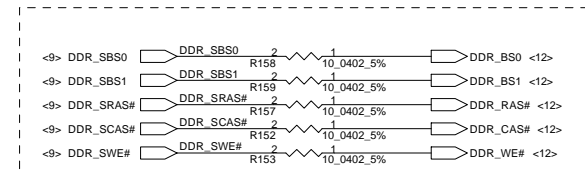
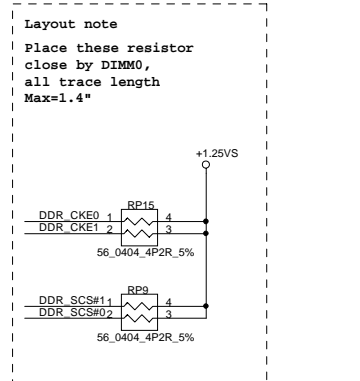
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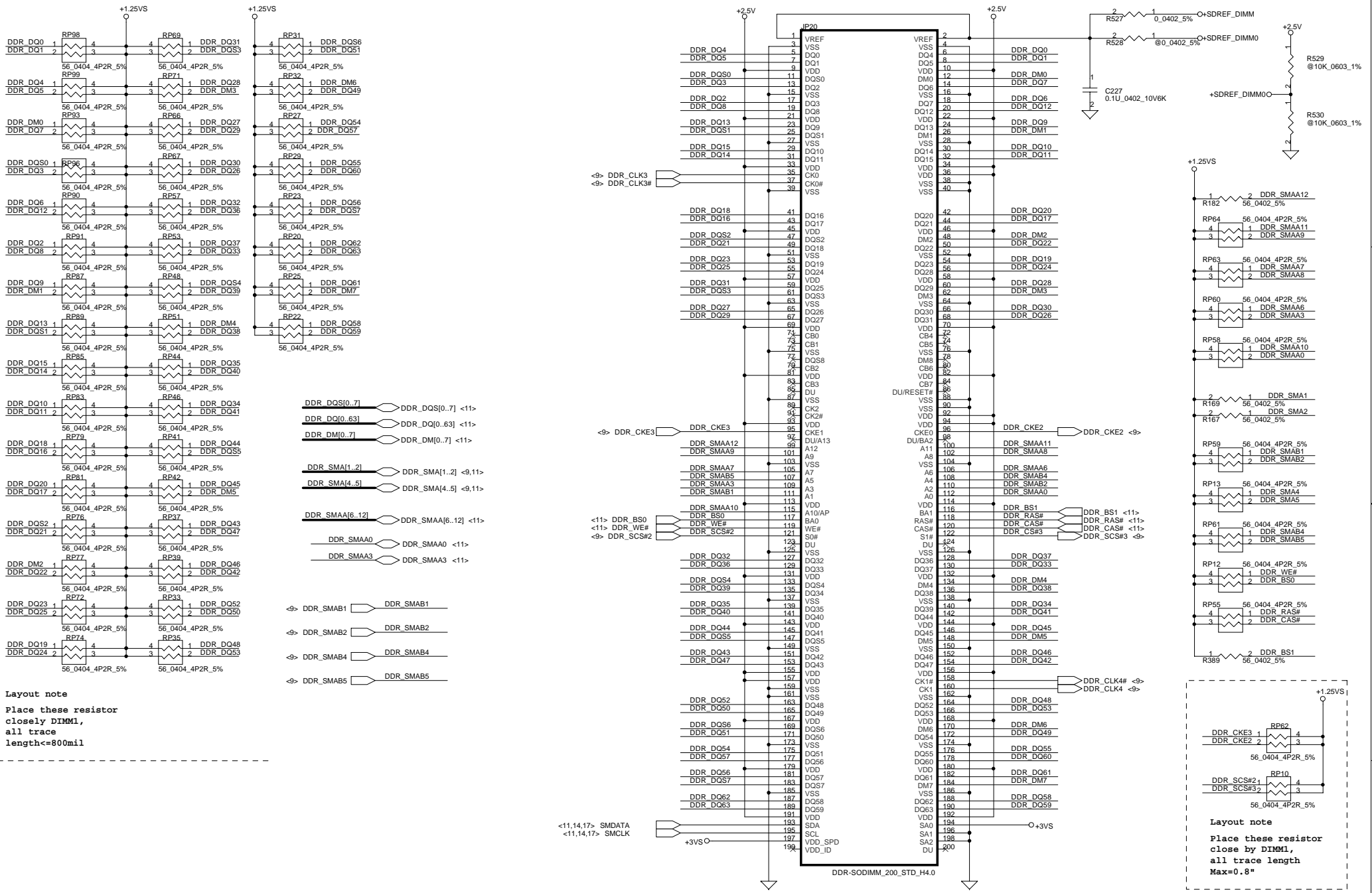
Layout note
 Place these resistors
 close to DIMM0,
 all trace length<500 mil

DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#



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Layout note
Place these resistor closely DIMM1, all trace length=800mil

Layout note
Place these resistor close by DIMM1, all trace length Max=0.8"

DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#

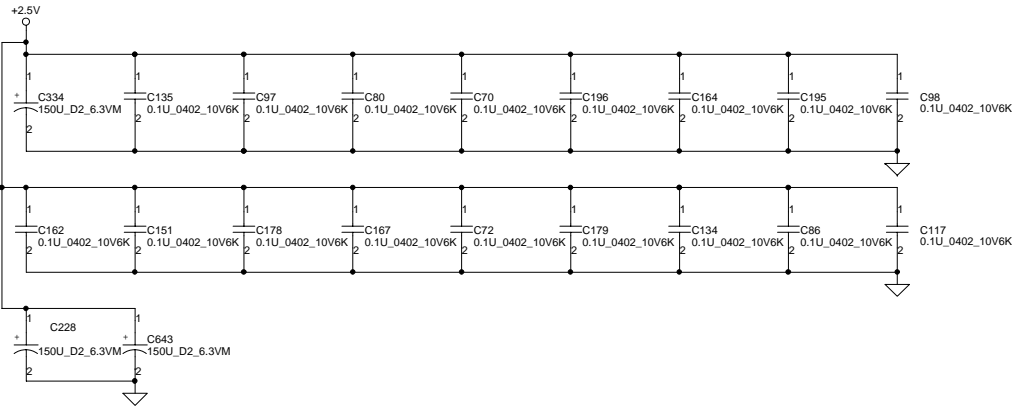
Compal Electronics, Inc.

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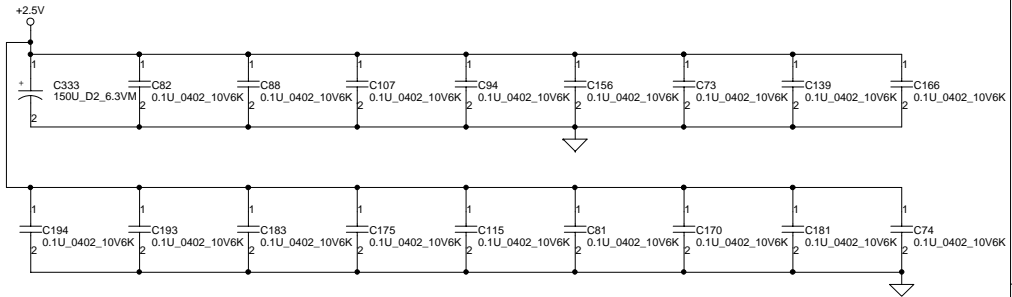
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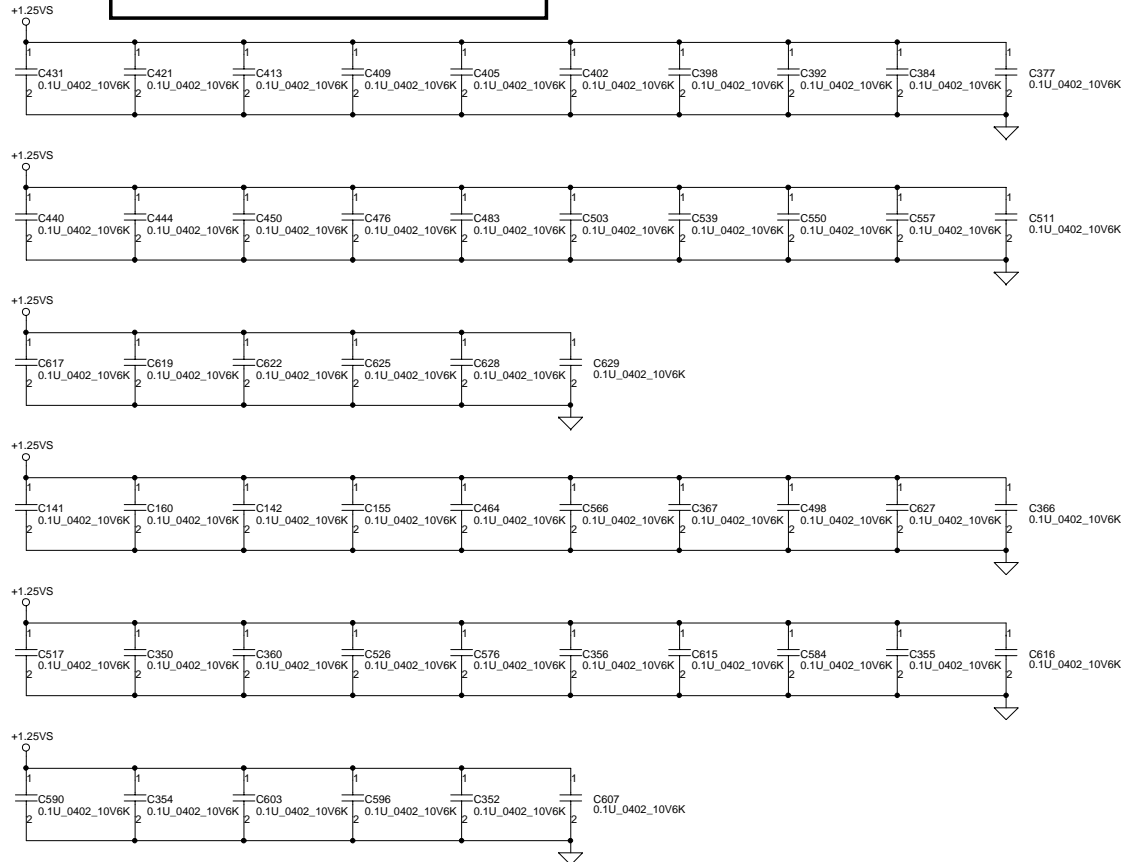
Layout note :
Distribute as close as possible to DDR-SODIMM0.



Layout note :
Distribute as close as possible to DDR-SODIMM1.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS

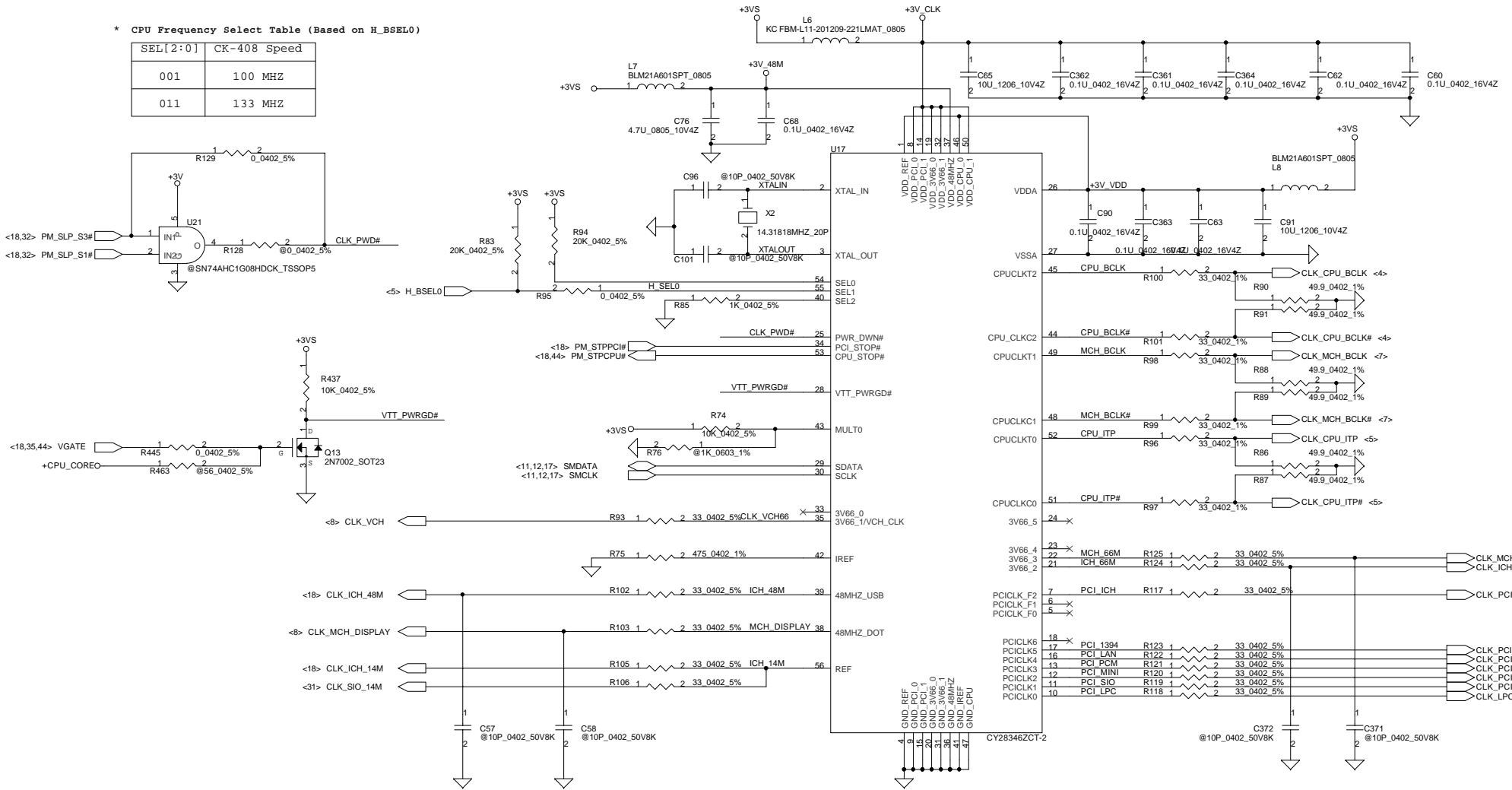


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* CPU Frequency Select Table (Based on H_BSEL0)

SEL[2:0]	CK-408 Speed
001	100 MHZ
011	133 MHZ



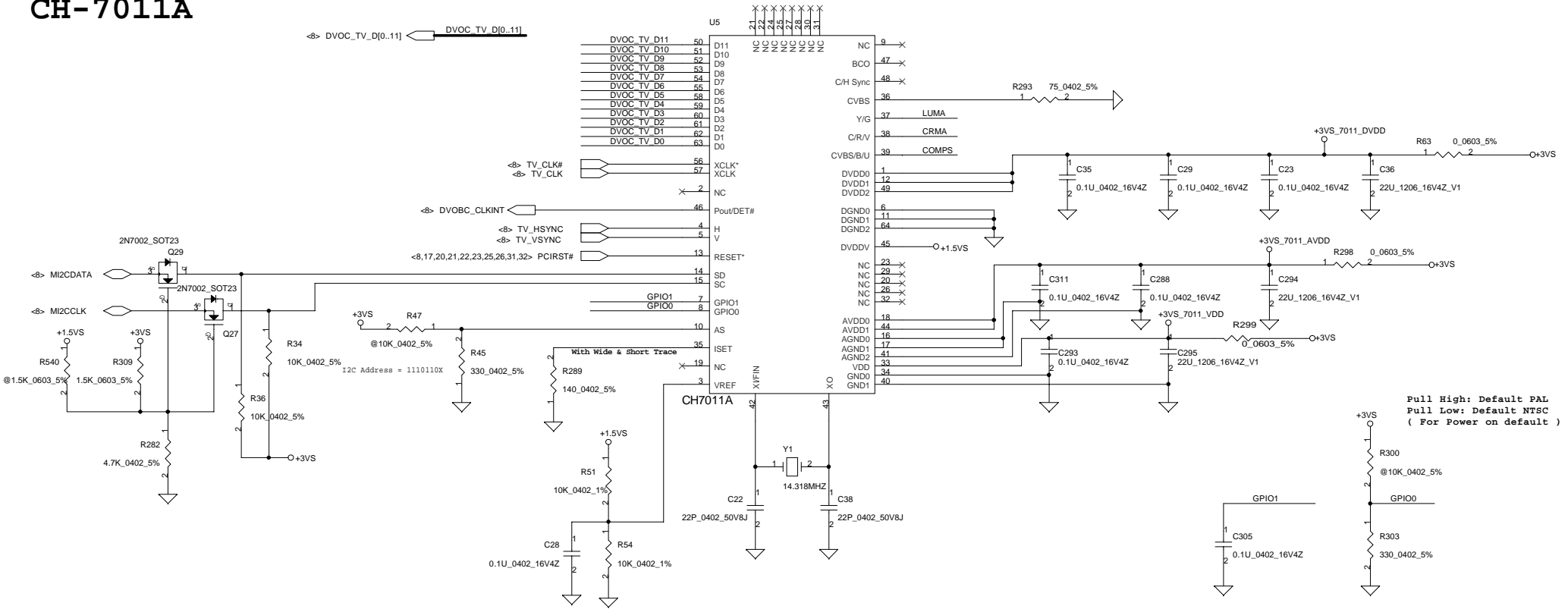
Compal Electronics, Inc.

Title
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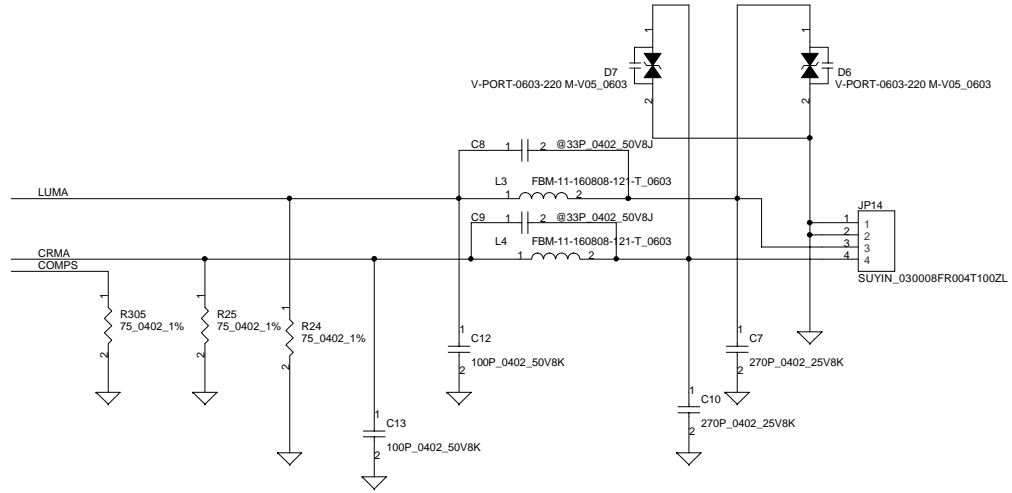
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CH-7011A

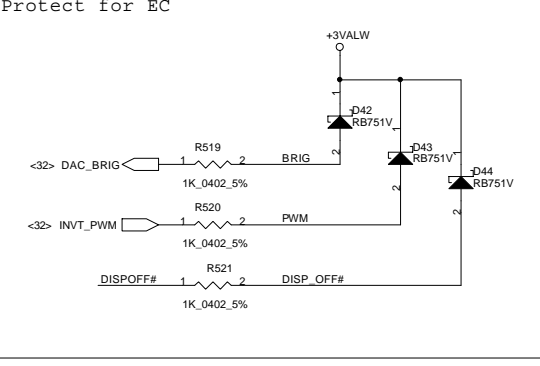
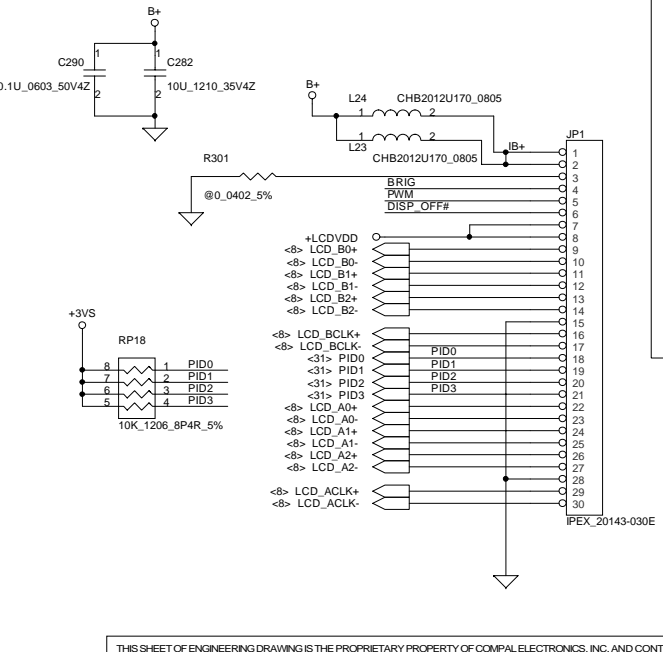
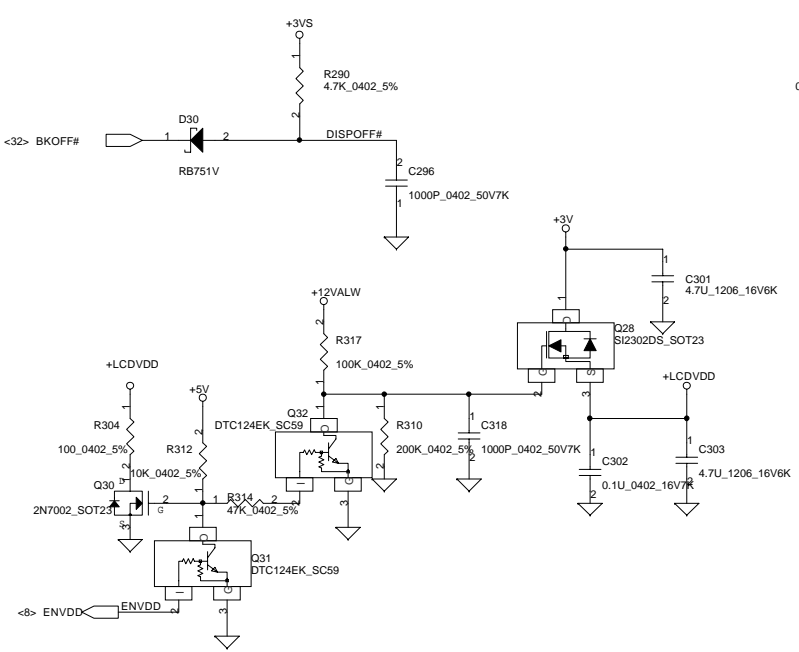
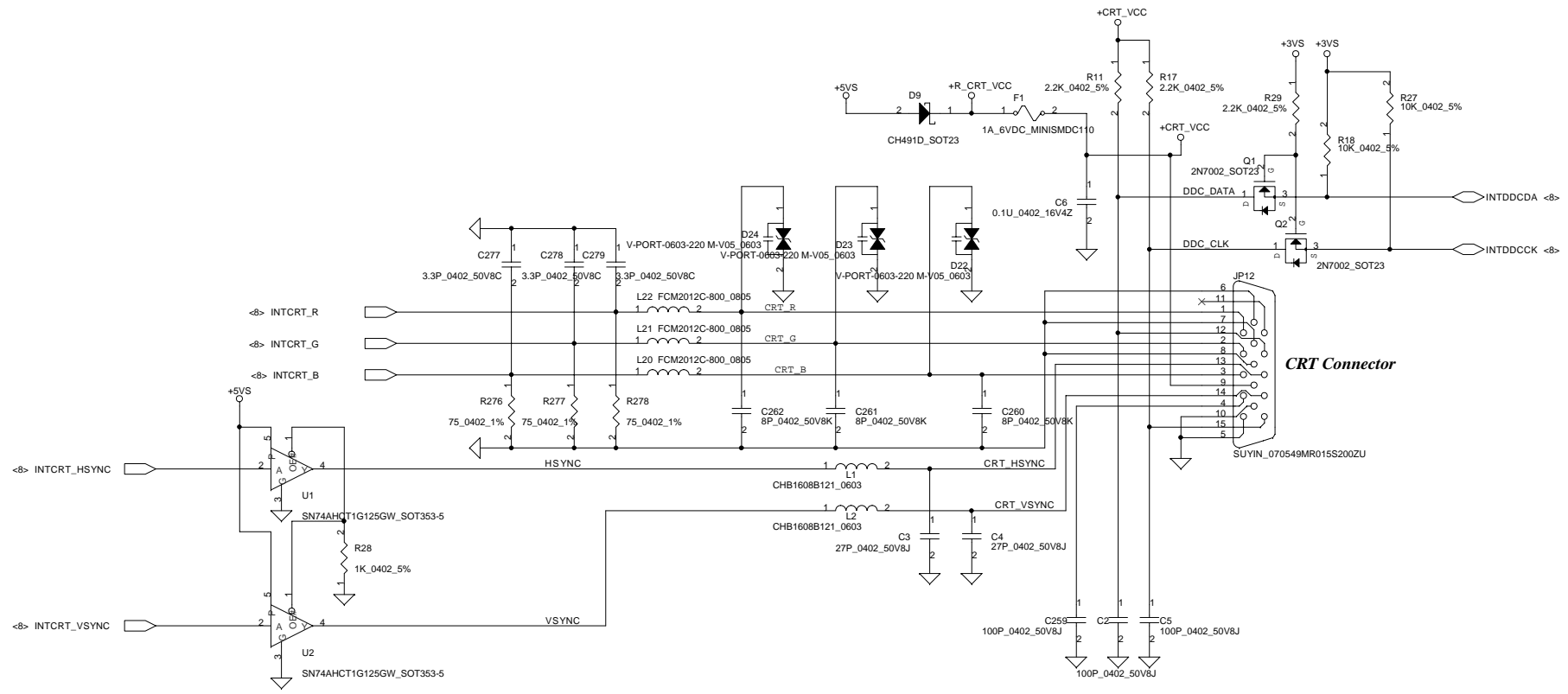


TV-OUT CONN.



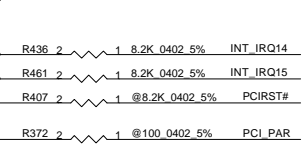
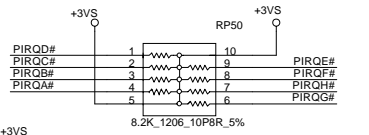
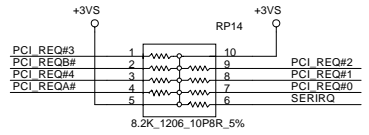
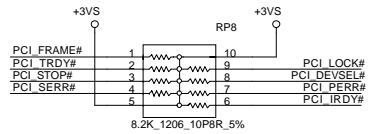
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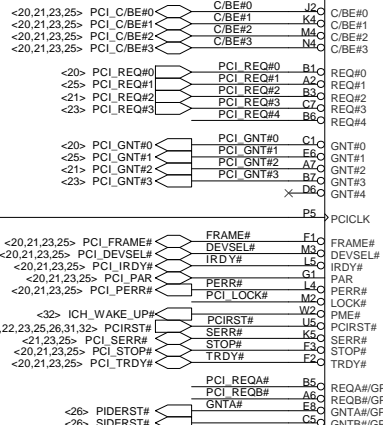
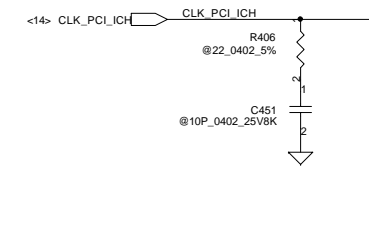


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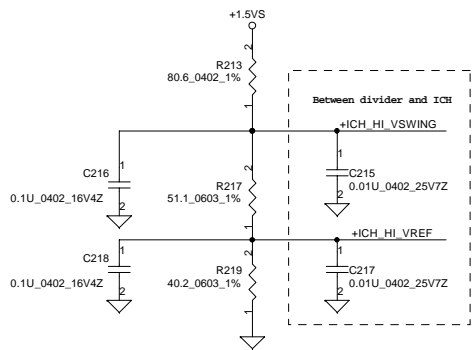
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Note:
In ICH4, PCI_GNT[0..4] don't need external pullup

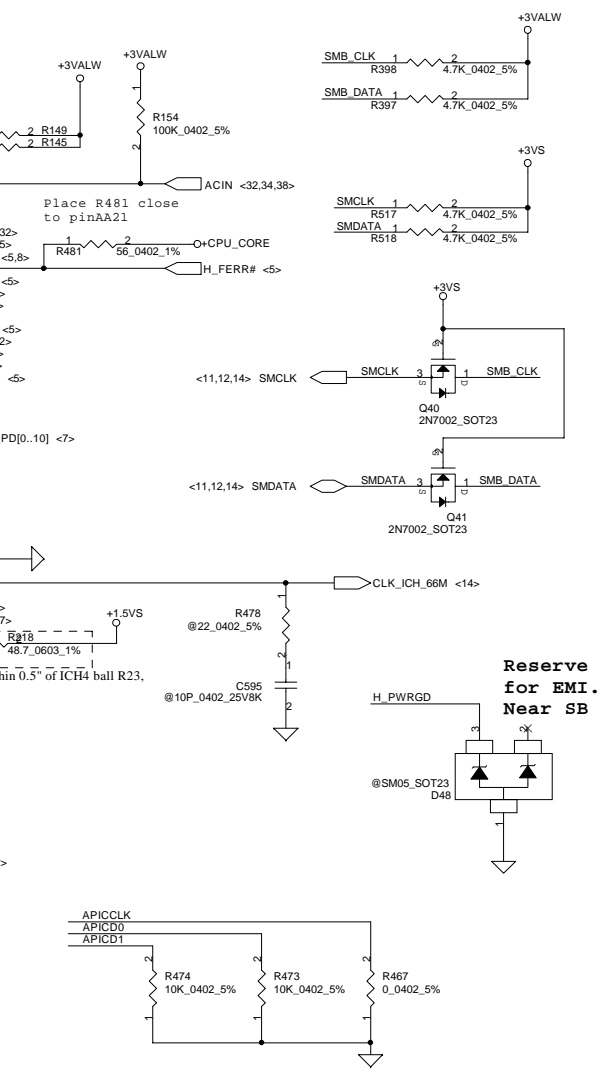
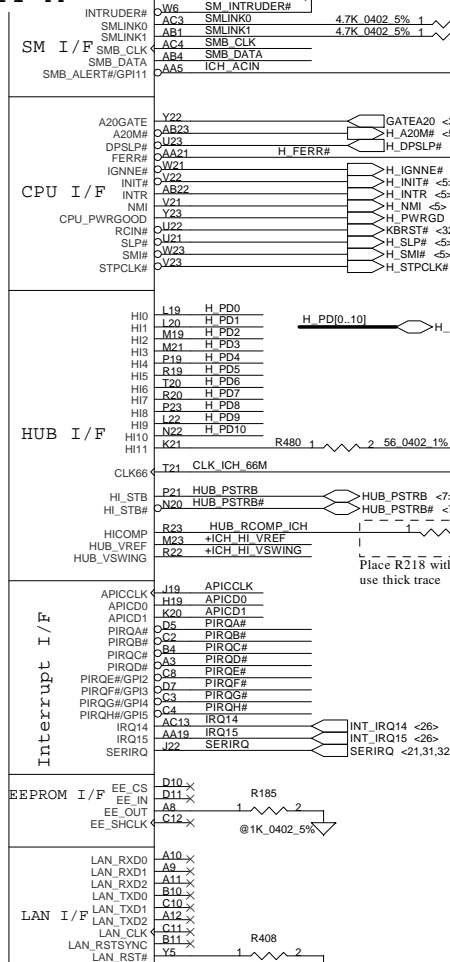


HUB I/F REF VOLTAGE



Place this schematic close to ICH

ICH4-M



Reserve for EMI. Near SB

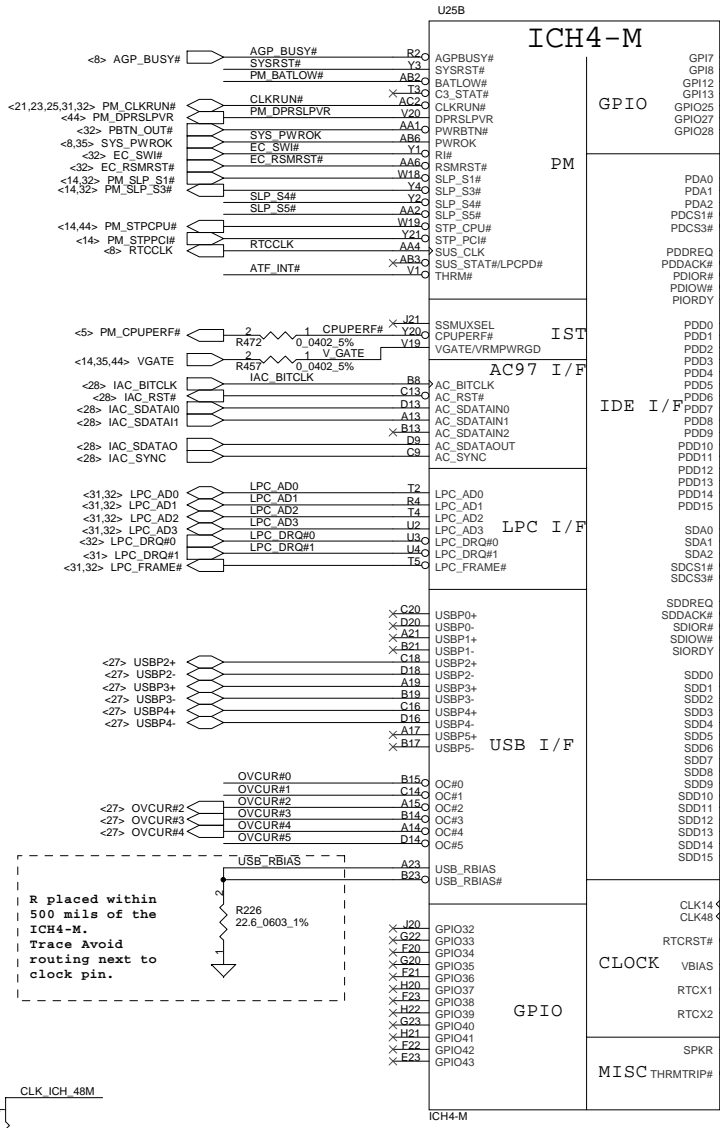
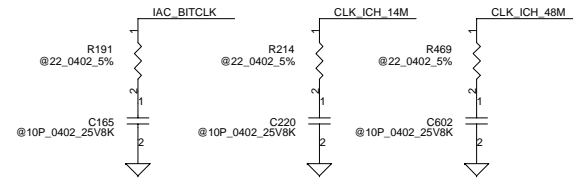
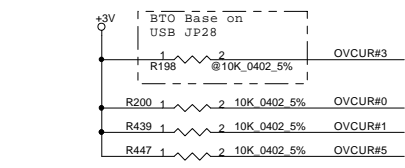
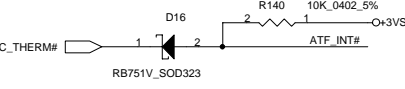
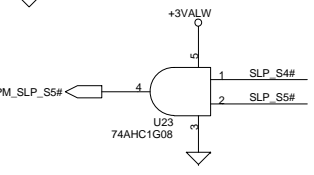
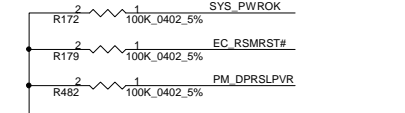
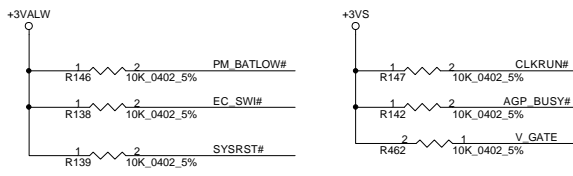
	Topology 1: Pop : RP52 and R393 Depop : RP11
1394	Trace: PIRQE#_1394 Use IRQE
CardBus	Trace: PIRQA# Use IRQA
LAN	Trace: PIRQ#_LAN Use IRQF
MINIPCI	Trace: PIRQG# Use IRQG

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Schematic, M/B LA-1931

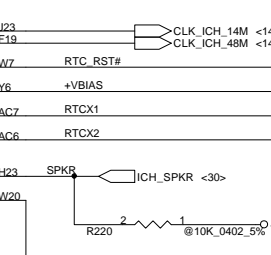
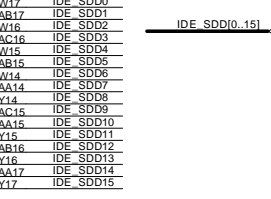
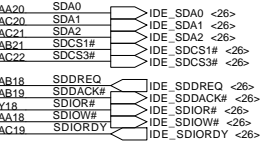
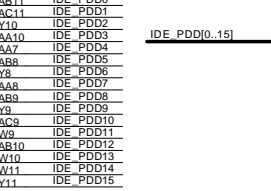
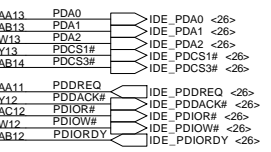
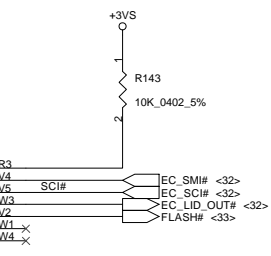
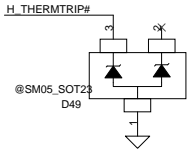
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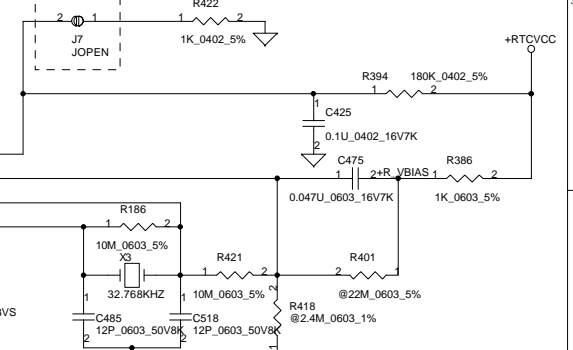


Place within 500 mils of the ICH4-M. Trace Avoid routing next to clock pin.

Reserve for EMI. Near SB.



Place J1 close to DDR-SODIMM

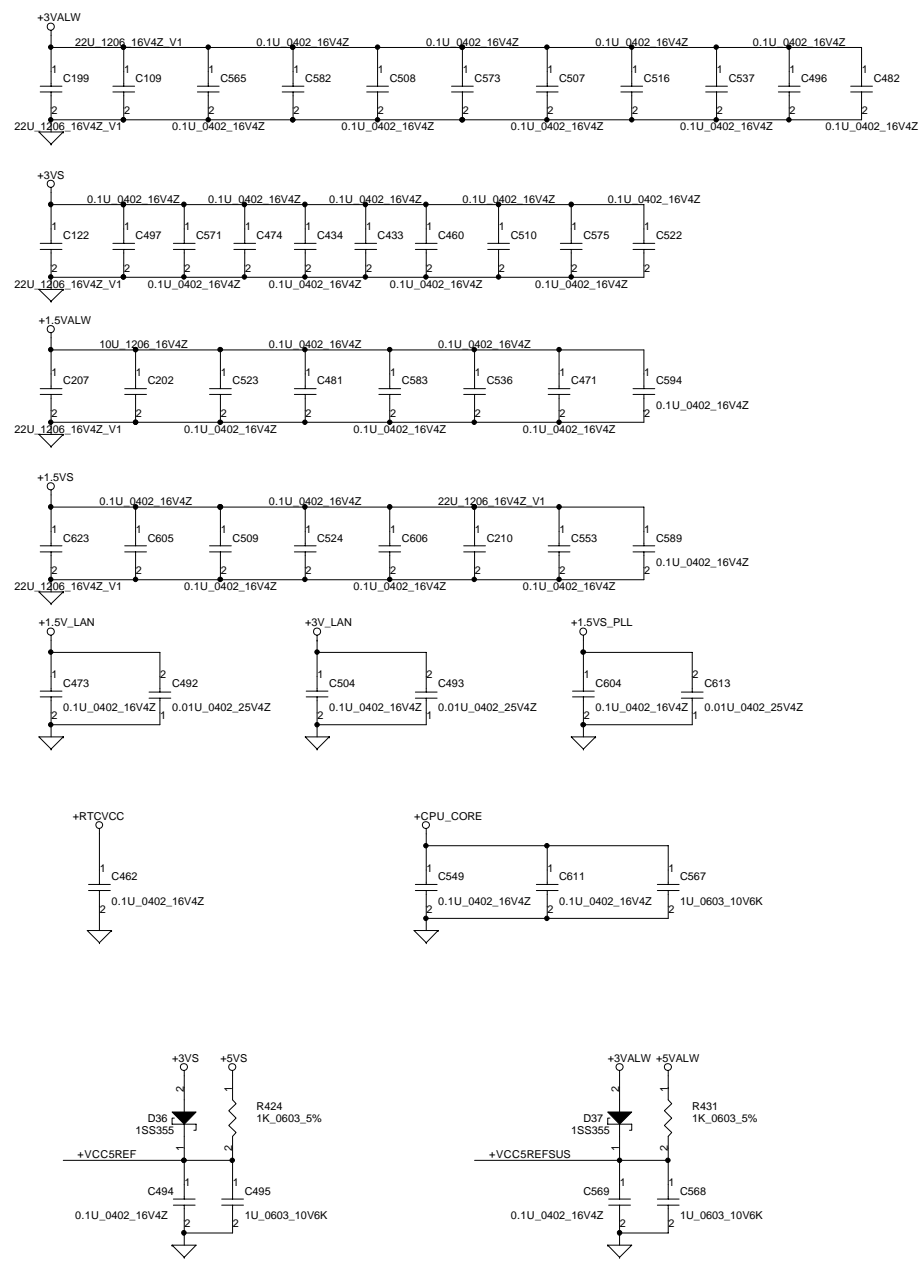
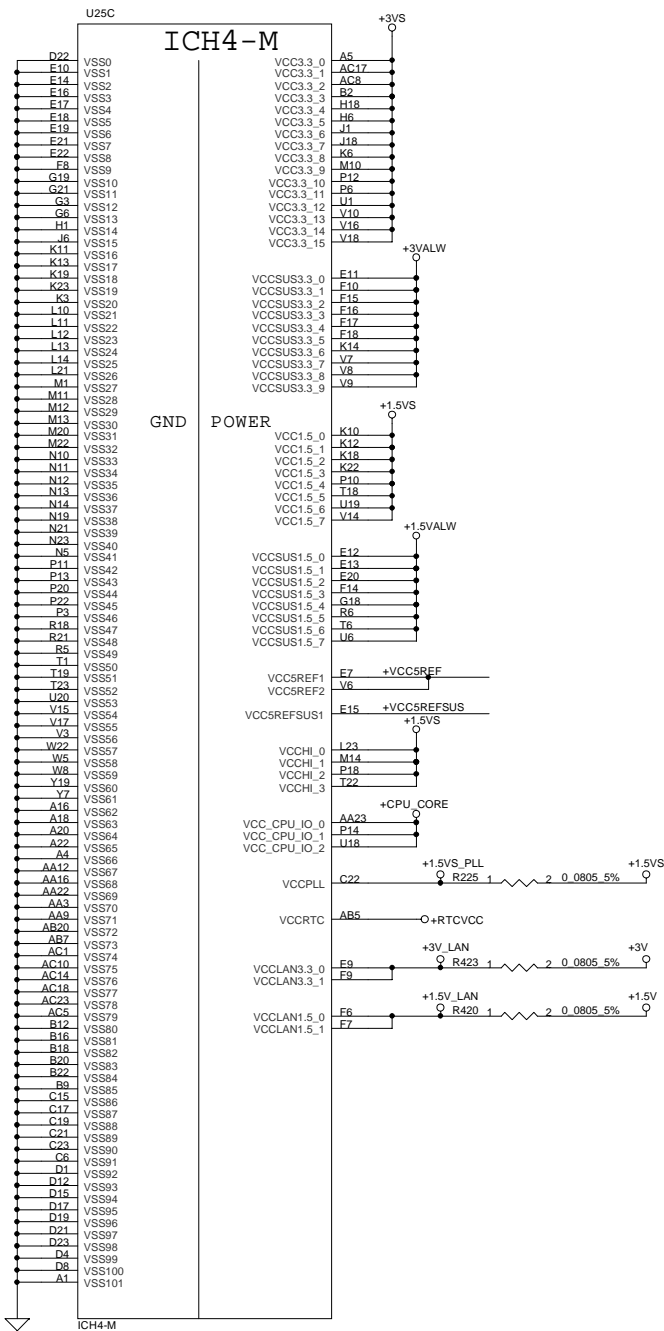


Place R502 near to U12 pinW20



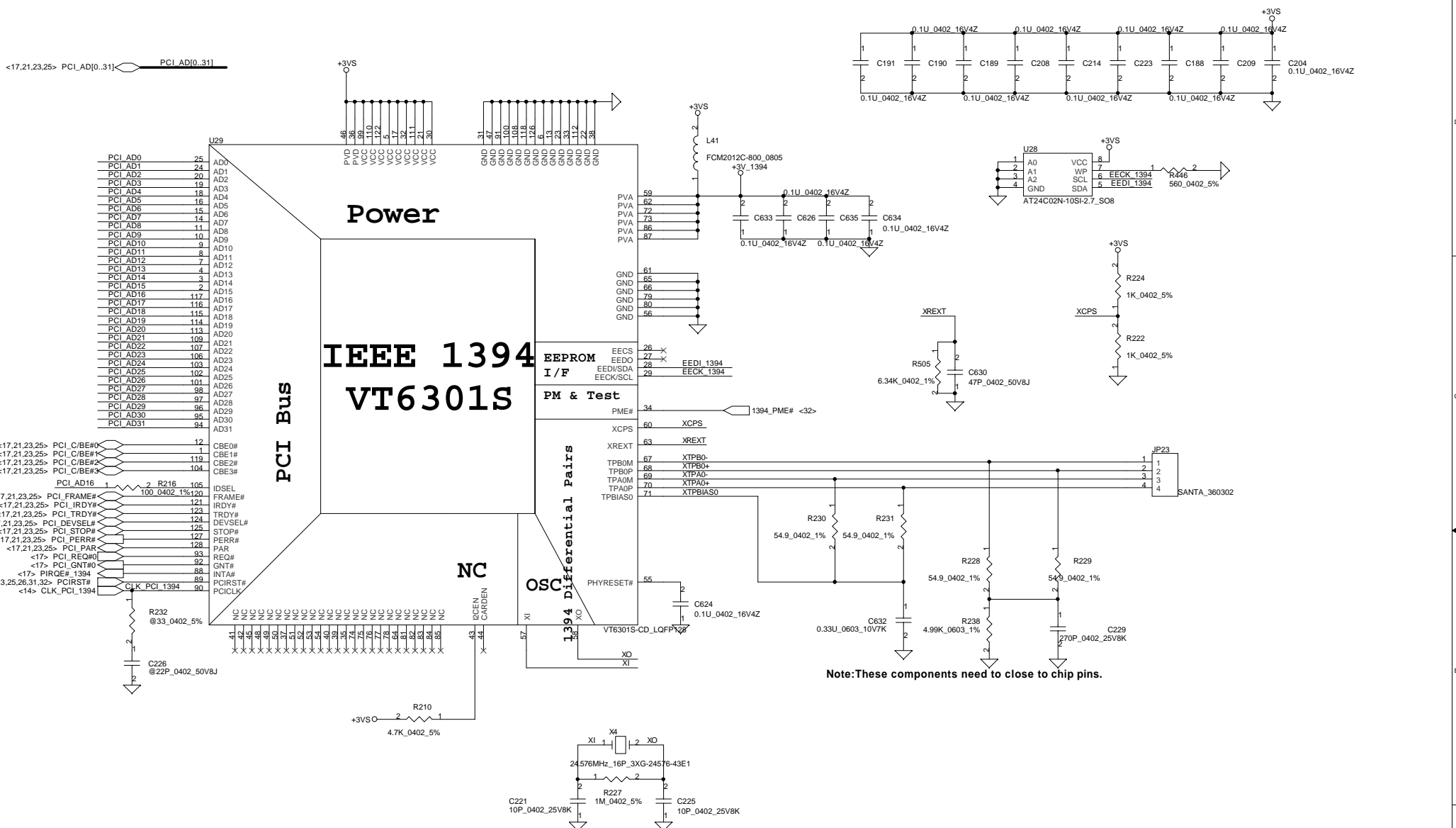
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Power

IEEE 1394

VT6301S

PCI Bus

NC

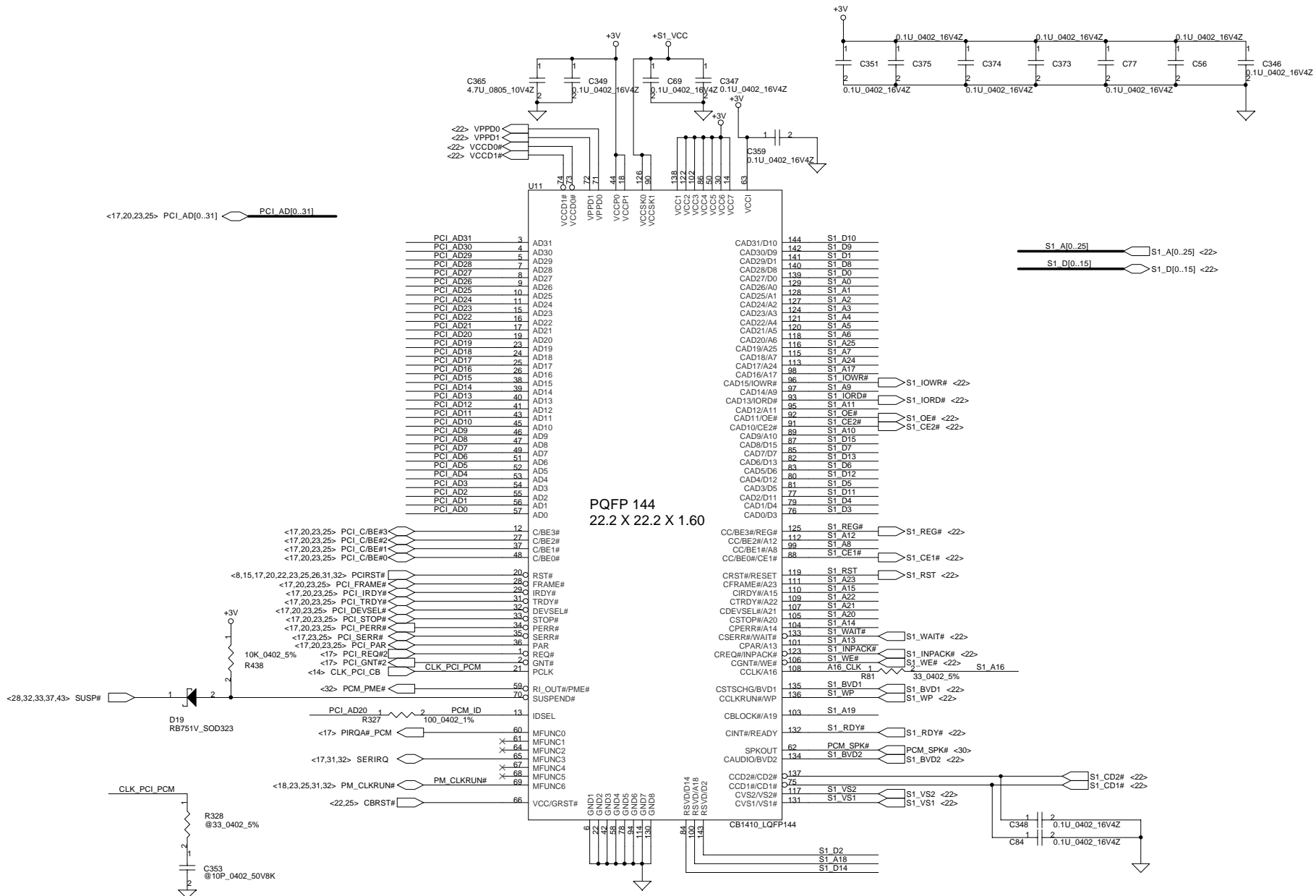
OSC

1394 Differential Pairs

Note: These components need to close to chip pins.

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**PQFP 144
22.2 X 22.2 X 1.60**

PCI AD31	3	AD31	CAD31/D10	144	S1 D10
PCI AD30	4	AD30	CAD30/D9	141	S1 D9
PCI AD29	5	AD29	CAD29/D8	140	S1 D8
PCI AD28	7	AD28	CAD27/D0	139	S1 D0
PCI AD28	8	AD27	CAD26/A0	129	S1 A0
PCI AD25	9	AD26	CAD25/A1	128	S1 A1
PCI AD24	10	AD25	CAD24/A2	127	S1 A2
PCI AD23	11	AD23	CAD23/A3	124	S1 A3
PCI AD22	15	AD23	CAD22/A4	121	S1 A4
PCI AD21	16	AD22	CAD21/A5	120	S1 A5
PCI AD20	17	AD21	CAD20/A6	118	S1 A6
PCI AD19	19	AD19	CAD19/A25	116	S1 A25
PCI AD18	23	AD18	CAD18/A7	115	S1 A7
PCI AD17	24	AD18	CAD17/A24	113	S1 A24
PCI AD16	25	AD17	CAD16/A17	98	S1 A17
PCI AD15	26	AD16	CAD15/IOVR#	96	S1 IOVR# <-22>
PCI AD14	38	AD14	CAD14/A9	97	S1 A9
PCI AD13	39	AD13	CAD13/IOVR#	93	S1 IOVR# <-22>
PCI AD12	40	AD13	CAD13/IOVR#	95	S1 A11
PCI AD11	41	AD12	CAD12/A11	92	S1 OE# <-22>
PCI AD10	43	AD10	CAD11/CE#	91	S1 CE2# <-22>
PCI AD9	45	AD10	CAD10/CE2#	89	S1 CE2# <-22>
PCI AD8	46	AD9	CAD9/A10	87	S1 D15
PCI AD7	47	AD8	CAD8/D15	85	S1 D7
PCI AD6	49	AD7	CAD7/D7	82	S1 D13
PCI AD5	51	AD6	CAD6/D13	83	S1 D6
PCI AD4	52	AD5	CAD5/D6	80	S1 D12
PCI AD3	53	AD4	CAD4/D12	81	S1 D5
PCI AD2	54	AD3	CAD3/D5	77	S1 D11
PCI AD1	55	AD2	CAD2/D11	79	S1 D4
PCI AD0	56	AD1	CAD1/D4	76	S1 D3
PCI AD0	57	AD0	CAD0/D3		
CC/BE3#/REG#	125	S1 REG#			S1_REG# <-22>
CC/BE2#/A12	112	S1 A2			
CC/BE1#/A8	99	S1 A8			
CC/BE0#/CE1#	88	S1 CE1#			S1_CE1# <-22>
CRST#/RESET	119	S1 RST			S1_RST <-22>
CFRAME#/A23	111	S1 A23			
CIIRDY#/A15	110	S1 A15			
CTRDY#/A22	109	S1 A22			
CDEVSEL#/A21	107	S1 A21			
CSTOP#/A20	104	S1 A14			
CPERR#/A14	103	S1 WAIT#			S1_WAIT# <-22>
CSERR#/WAIT#	101	S1 A13			
CPAR/A13	123	S1 INPACK#			S1_INPACK# <-22>
CREQ#/INPACK#	106	S1 WE#			S1_WE# <-22>
CGNT#/WE#	108	A16 CLK			S1_A16
CCLK/A16					
CSTSCHG/BVD1	135	S1 BVD1			S1_BVD1 <-22>
CCLKRUN#/WP	136	S1 WP			S1_WP <-22>
CBLOCK#/A19	103	S1 A19			
CINT#/READY	132	S1 RDY#			S1_RDY# <-22>
CPMSPK#/PCM_SPK#	62	PCM_SPK#			PCM_SPK# <-30>
CAUDIO/BVD2	134	S1 BVD2			S1_BVD2 <-22>
CCD2#/CD#	137	S1 CD2#			S1_CD2# <-22>
CCD1#/CD#	75	S1 VS2			S1_CD1# <-22>
CVS2/VS#	117	S1 VS2			
CVS1/VS#	131	S1 VS1			

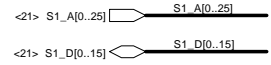
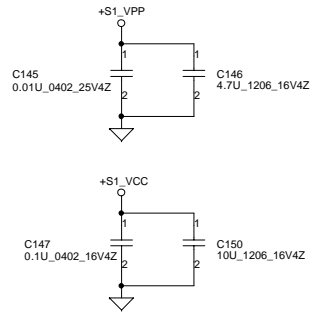
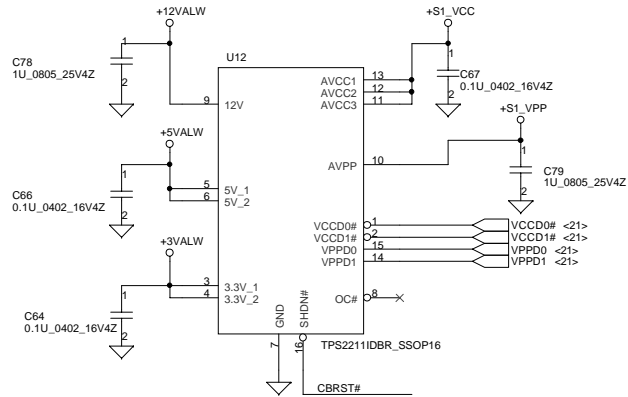
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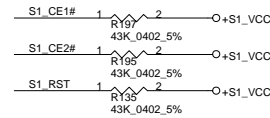
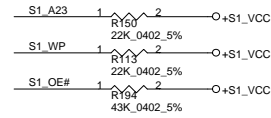
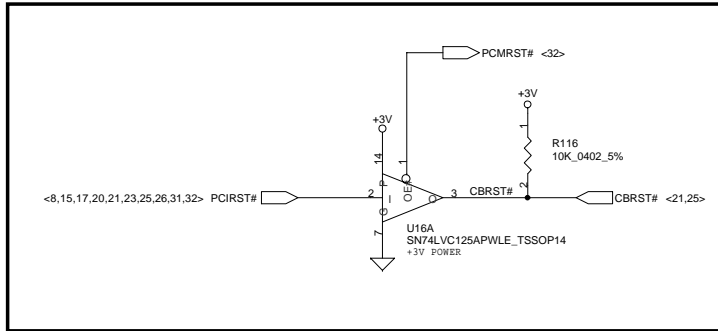
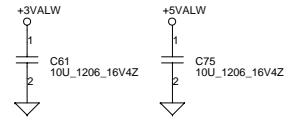
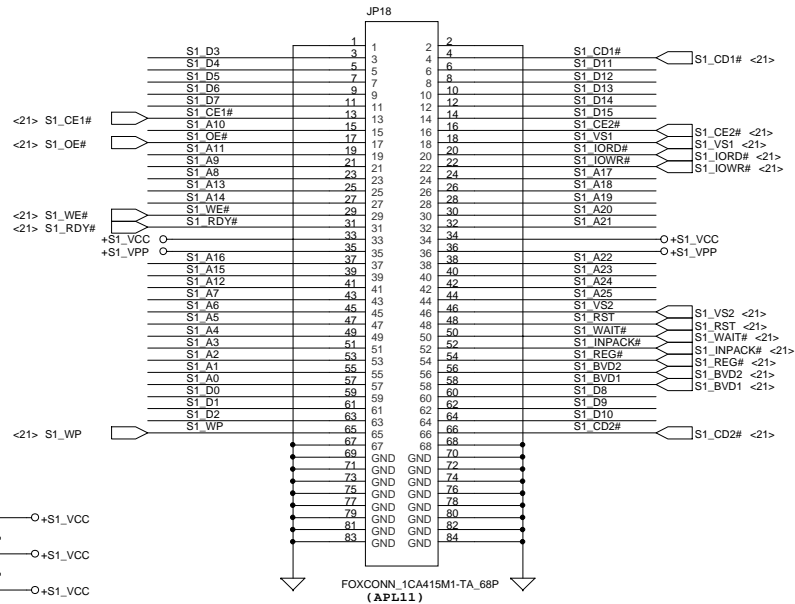
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PCMCIA Power Controller



CardBus Socket



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PCI AD0	47	AD0
PCI AD1	46	AD1
PCI AD2	45	AD2
PCI AD3	43	AD3
PCI AD4	42	AD4
PCI AD5	41	AD5
PCI AD6	40	AD6
PCI AD7	39	AD7
PCI AD8	36	AD8
PCI AD9	35	AD9
PCI AD10	34	AD10
PCI AD11	33	AD11
PCI AD12	32	AD12
PCI AD13	30	AD13
PCI AD14	29	AD14
PCI AD15	28	AD15
PCI AD16	15	AD16
PCI AD17	13	AD17
PCI AD18	14	AD18
PCI AD19	12	AD19
PCI AD20	11	AD20
PCI AD21	10	AD21
PCI AD22	9	AD22
PCI AD23	8	AD23
PCI AD24	93	AD24
PCI AD25	96	AD25
PCI AD26	92	AD26
PCI AD27	91	AD27
PCI AD28	89	AD28
PCI AD29	87	AD29
PCI AD30	86	AD30
PCI AD31	85	AD31

<17,20,21,25> PCI_AD[0..31] PCI_AD[0..31]

<17,20,21,25>	PCI_C/BE#0	38	C/BE#0
<17,20,21,25>	PCI_C/BE#1	27	C/BE#1
<17,20,21,25>	PCI_C/BE#2	17	C/BE#2
<17,20,21,25>	PCI_C/BE#3	84	C/BE#3

PCI_AD17 1 LAN_IDSEL 98 IDSEL

<17,20,21,25>	PCI_PAR	24	PAR
<17,20,21,25>	PCI_FRAME#	18	FRAME#
<17,20,21,25>	PCI_IRDY#	19	IRDY#
<17,20,21,25>	PCI_TRDY#	20	TRDY#
<17,20,21,25>	PCI_DEVSEL#	21	DEVSEL#
<17,20,21,25>	PCI_STOP#	23	STOP#

<17,20,21,25>	PCI_PERR#	25	PERR#
<17,21,25>	PCI_SERR#	26	SERR#

<17>	PCI_REQ#3	83	REQ#
<17>	PCI_GNT#3	82	GNT#

<17>	PIRQF#_LAN	80	INTA#
<17>	PCI_GNT#3	79	INTB#

<32>	LAN_PME#	57	PME#
------	----------	----	------

<8,15,17,20,21,22,25,26,31,32>	PCIRST#	81	RST#
<14>	CLK_PCI_LAN	97	PCICLK
<18,21,25,31,32>	PM_CLKRUN#	50	CLKRUN#

VDD	6	DGND1
VDD	22	DGND2
VDD	37	DGND3
VDD	49	DGND4
VDD	90	DGND5
VDD	95	AGND1
VDD		AGND2
VDD		AGND3

Power

RTL8101L_LQFP100

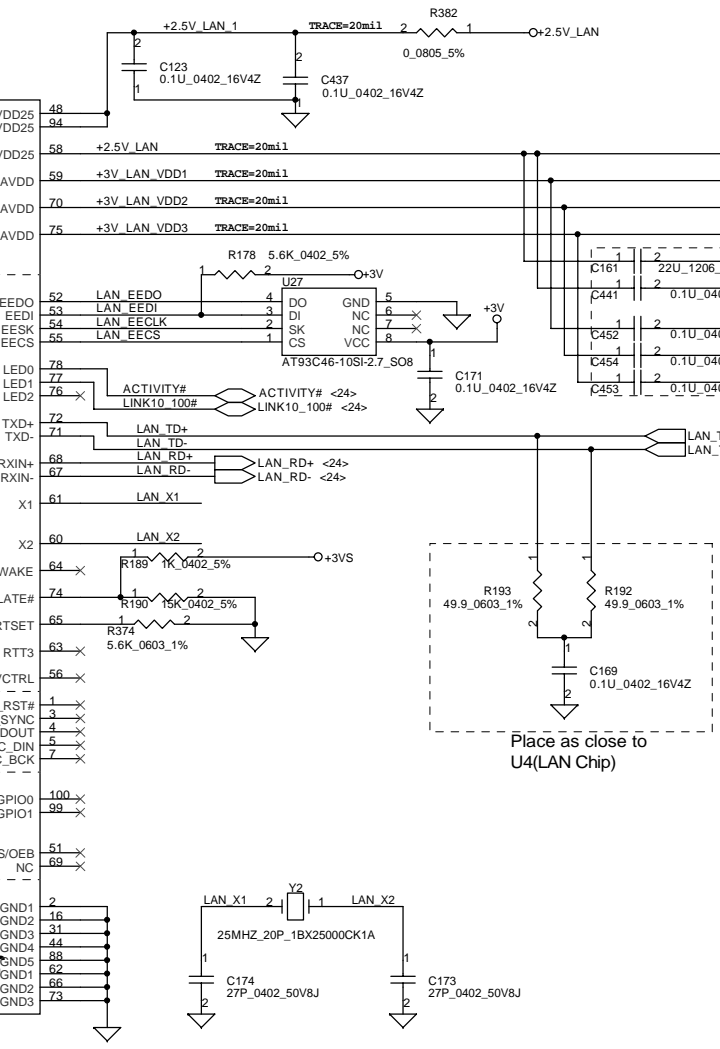
Power

PCI I/F

LAN I/F

Power

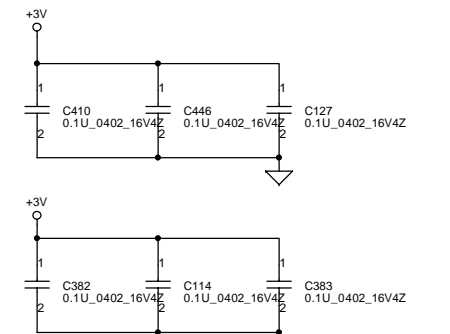
AC-Link



RTL8101L has internal +2.5V generator at pin58

Place closed to RTL8101L pin58

Place as close to U4(LAN Chip)



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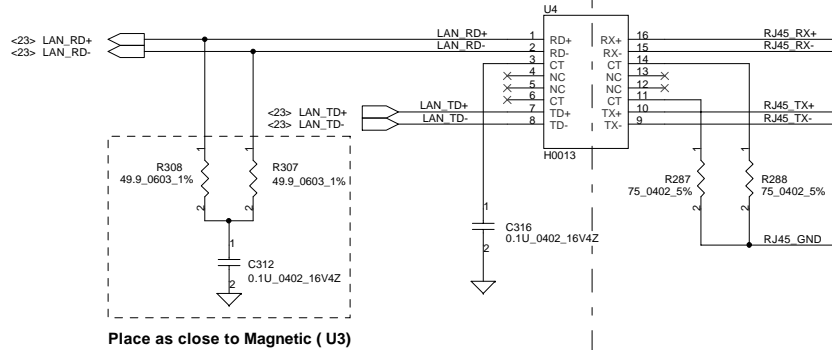
Size: Document Number 401264 Rev: 1B

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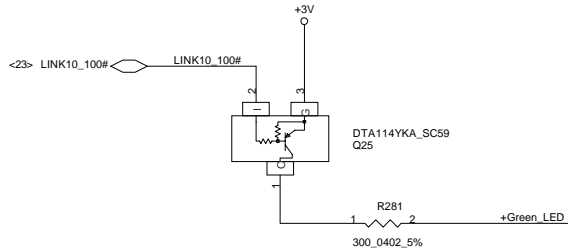
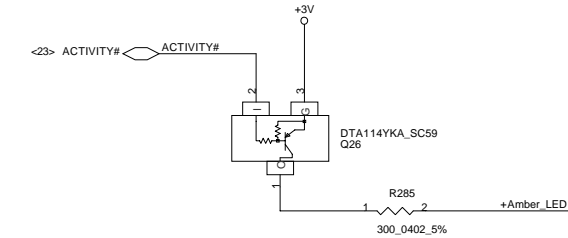
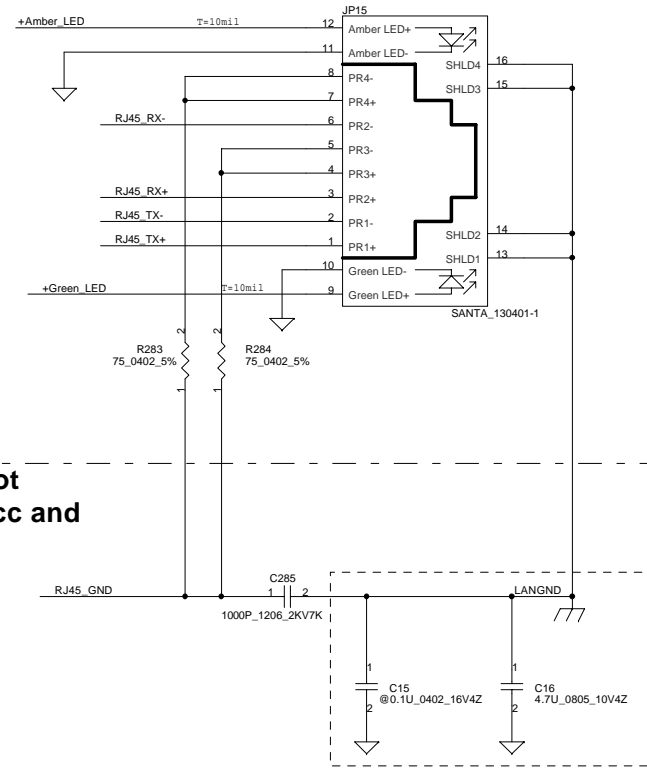
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Keep Out 40mil

Layout Note
H0013 pls close to
conn.

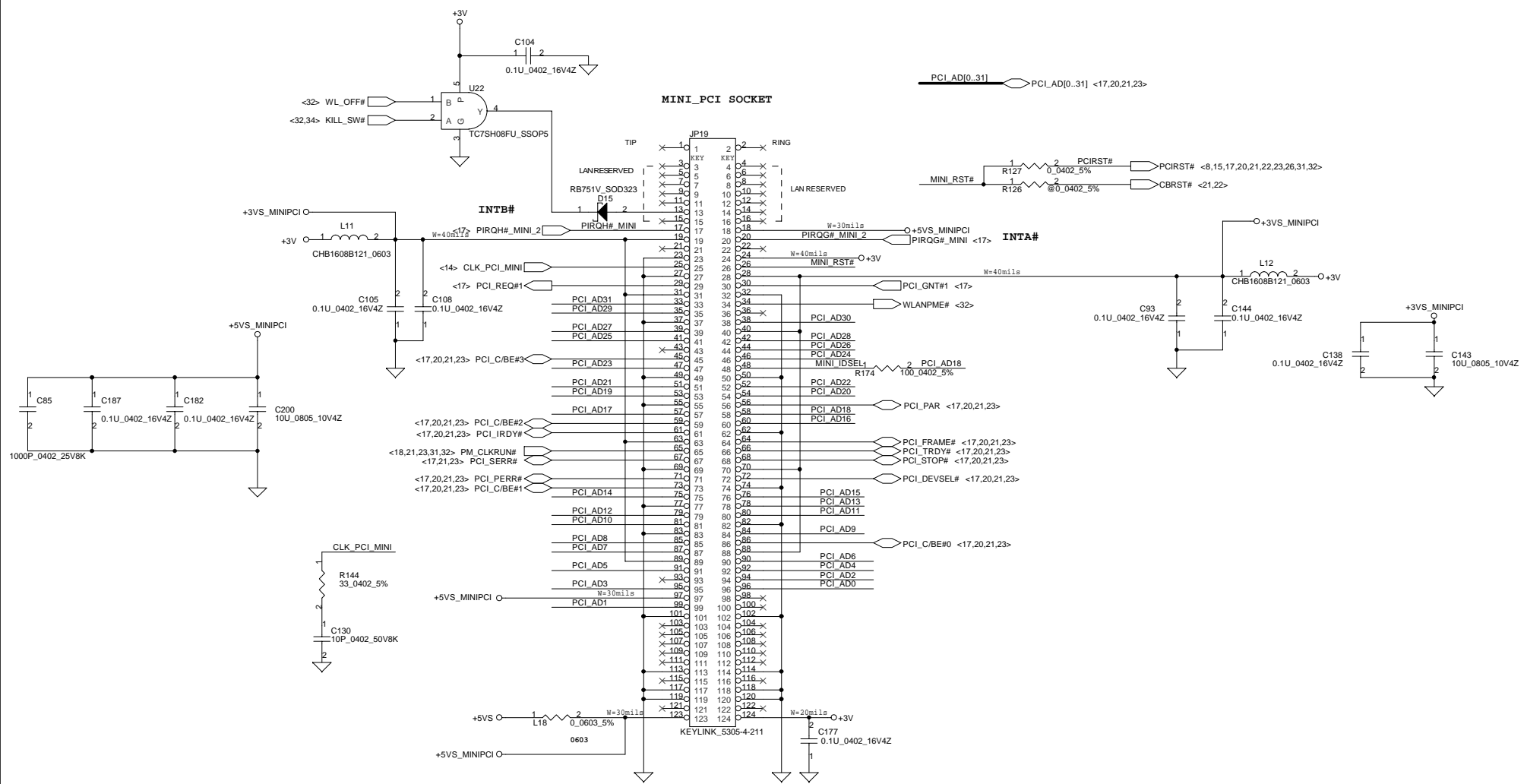


LAYOUT NOTICE: This area do not connect to power plan include Vcc and GND in any layer



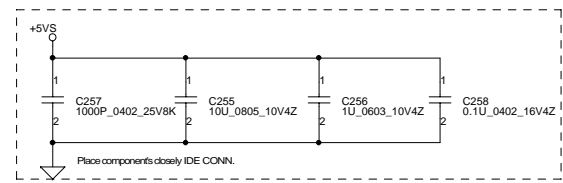
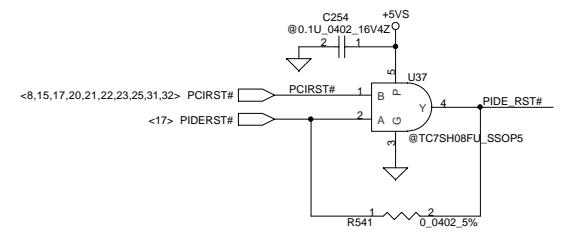
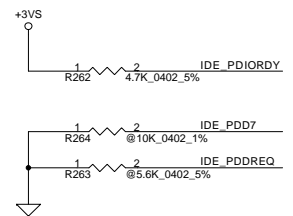
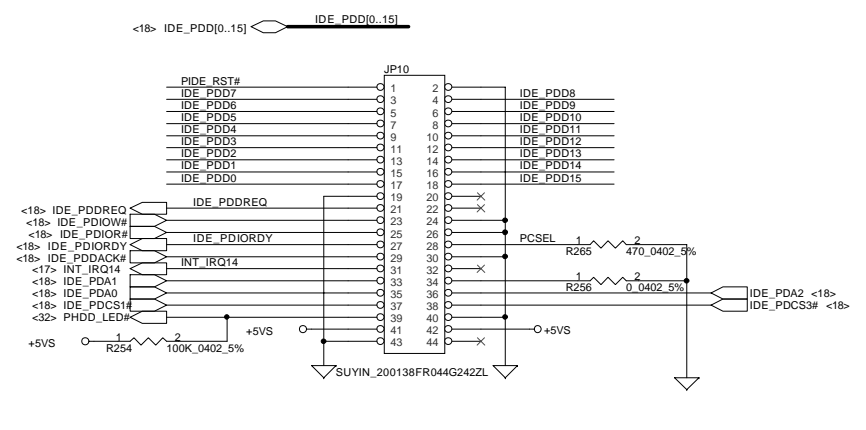
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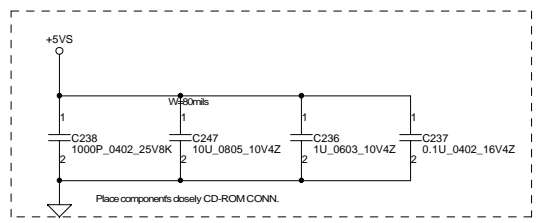
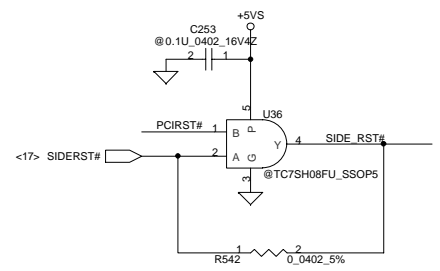
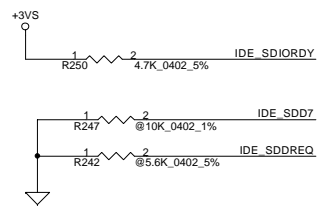
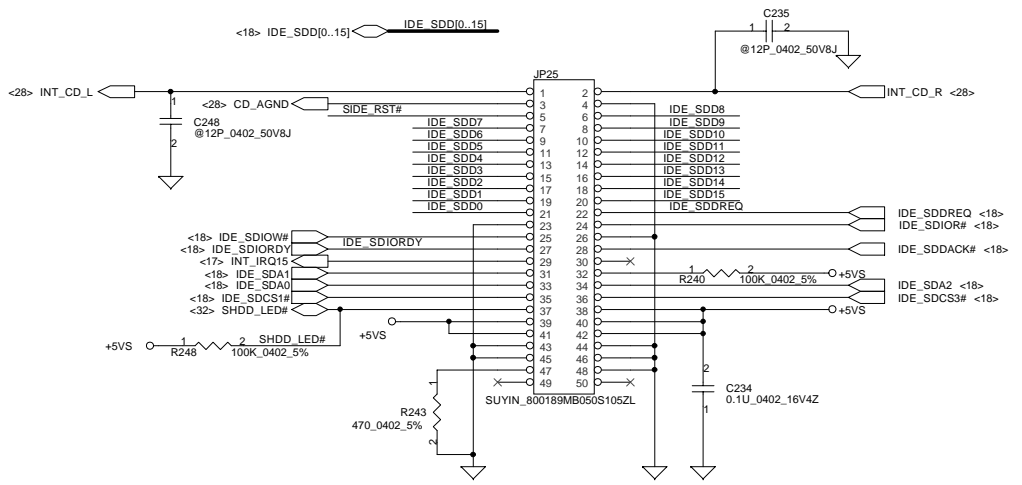


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IDE Module CONN.



CD-ROM Module CONN.

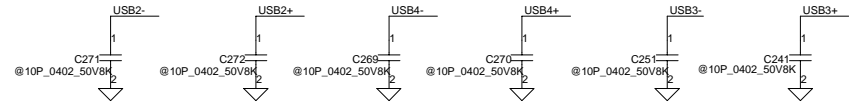
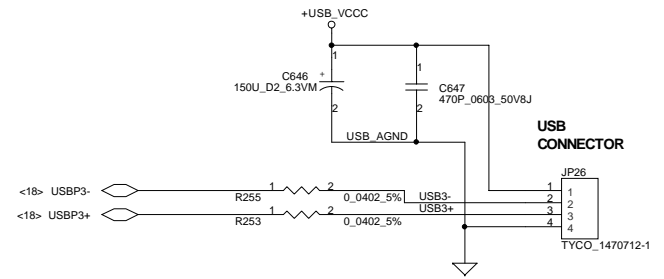
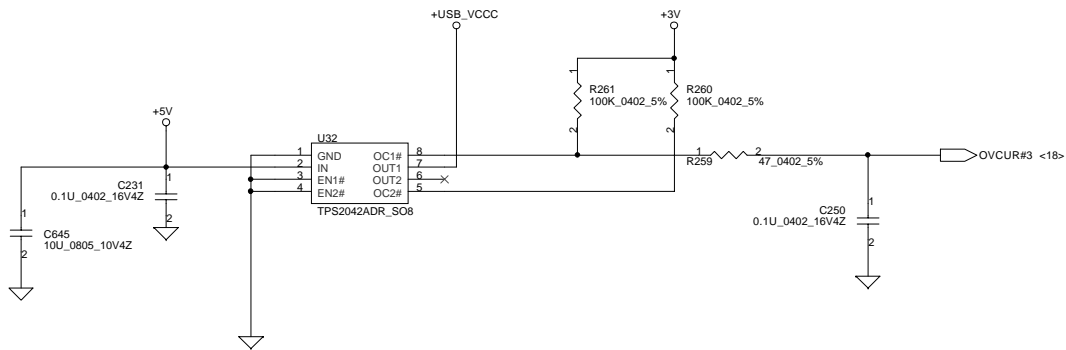
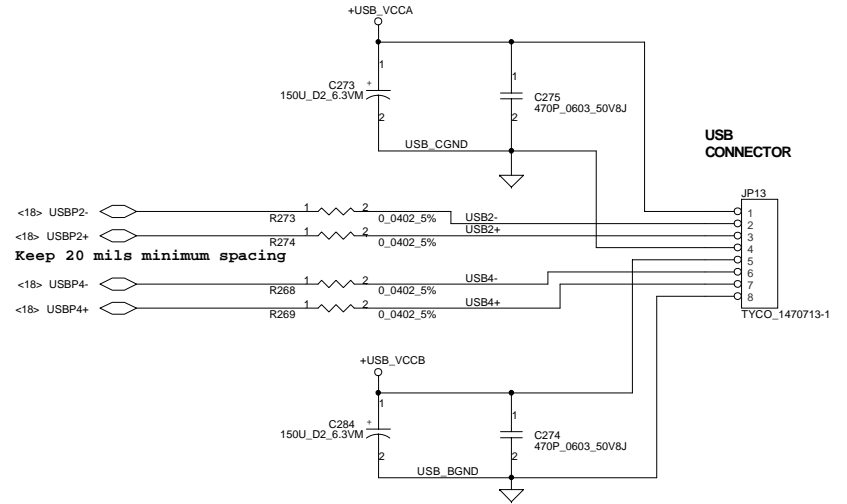
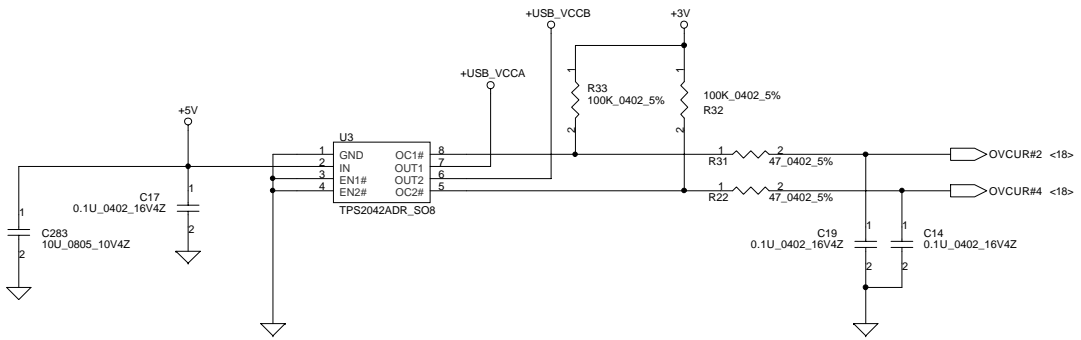


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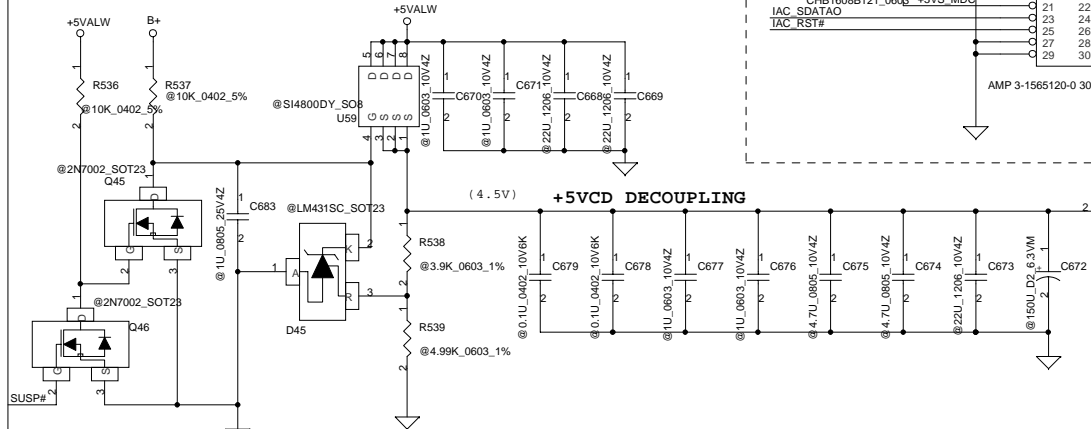
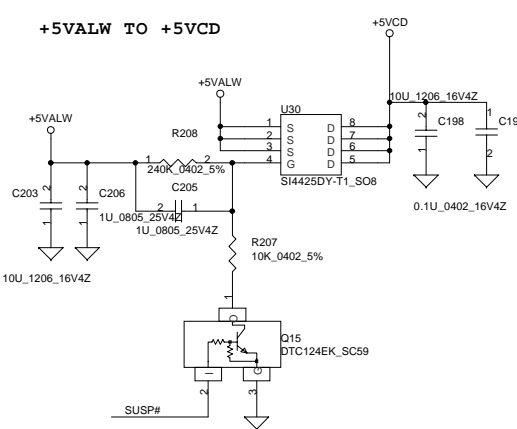
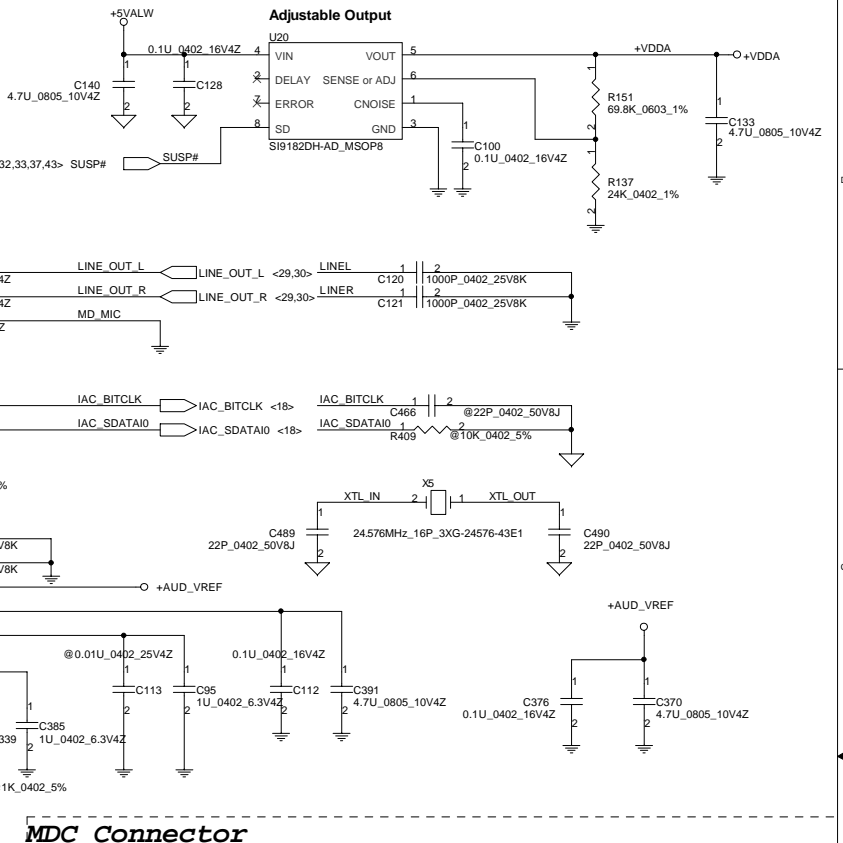
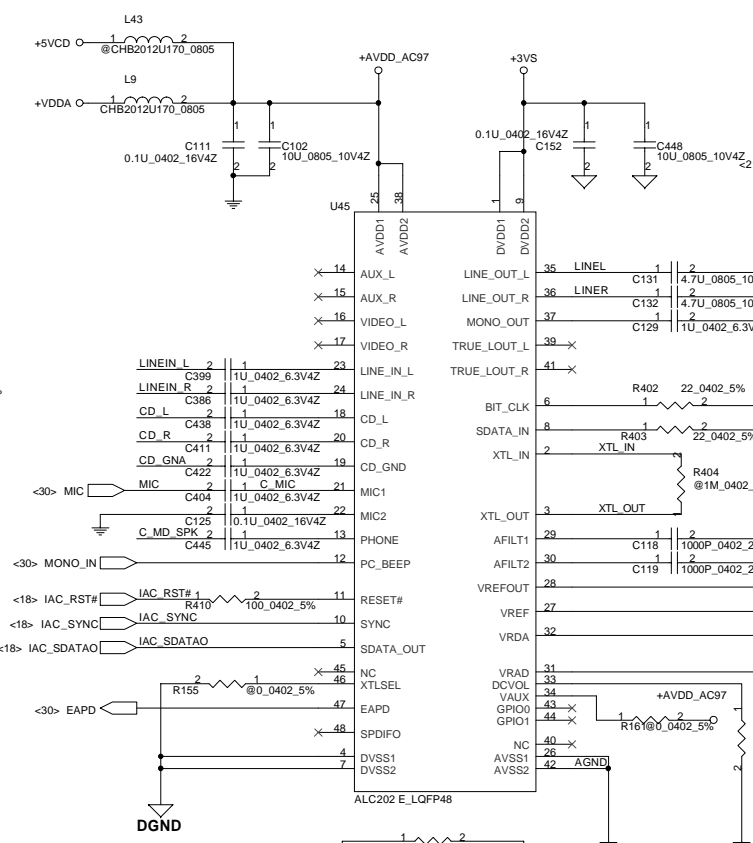
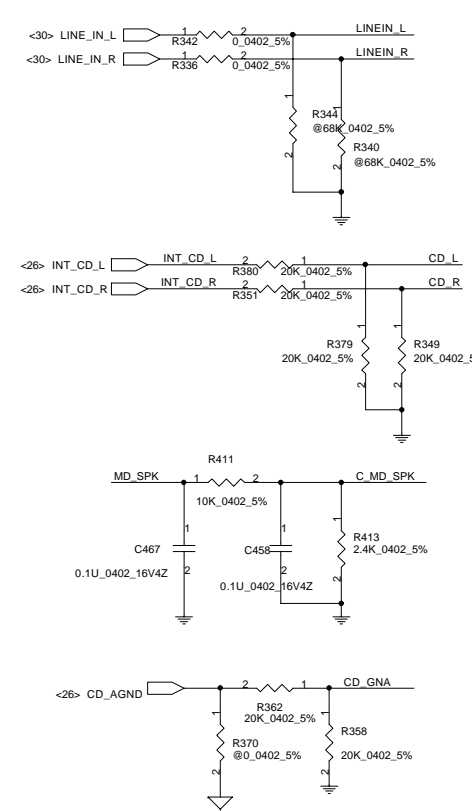
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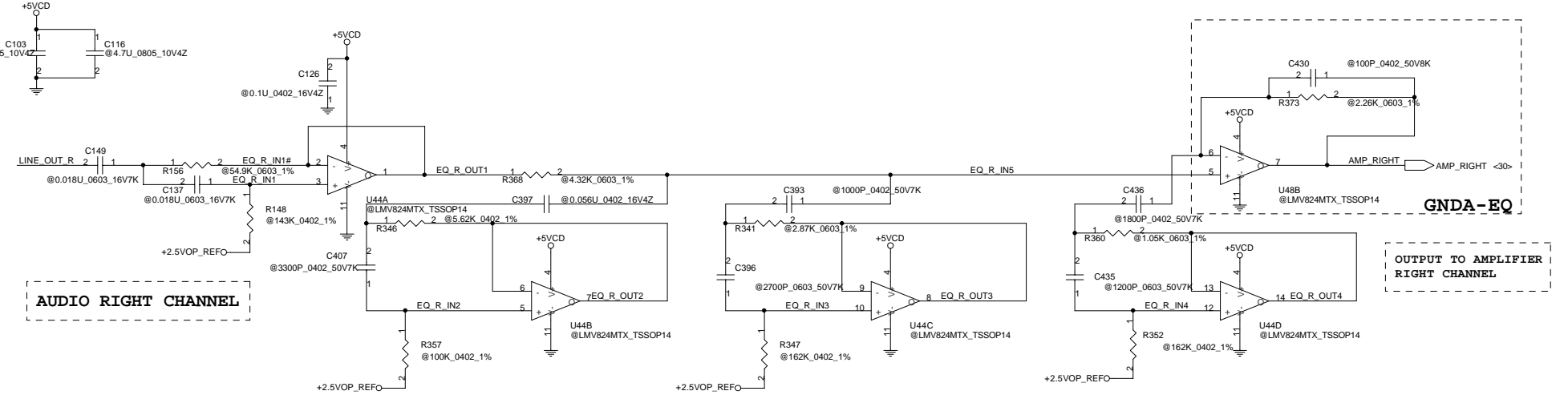
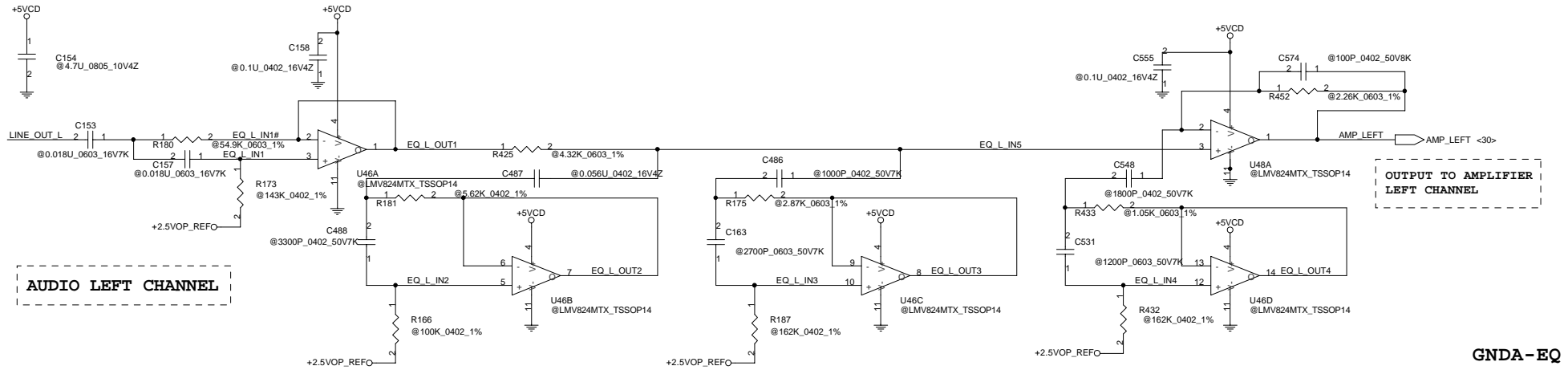
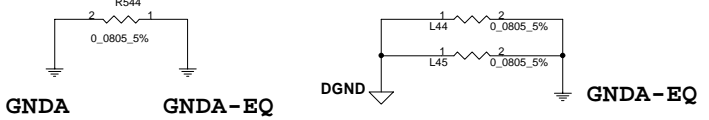
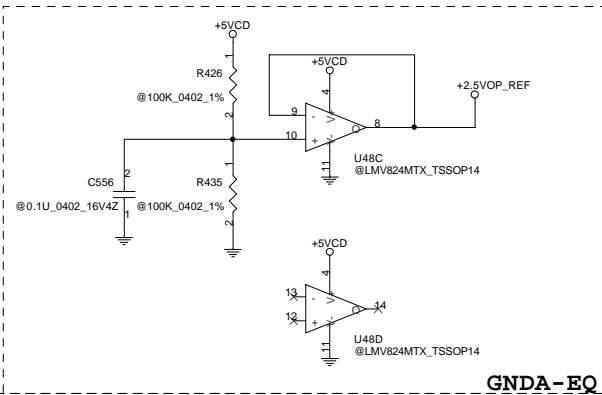
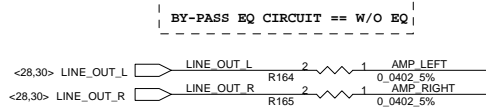
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AC97 Codec



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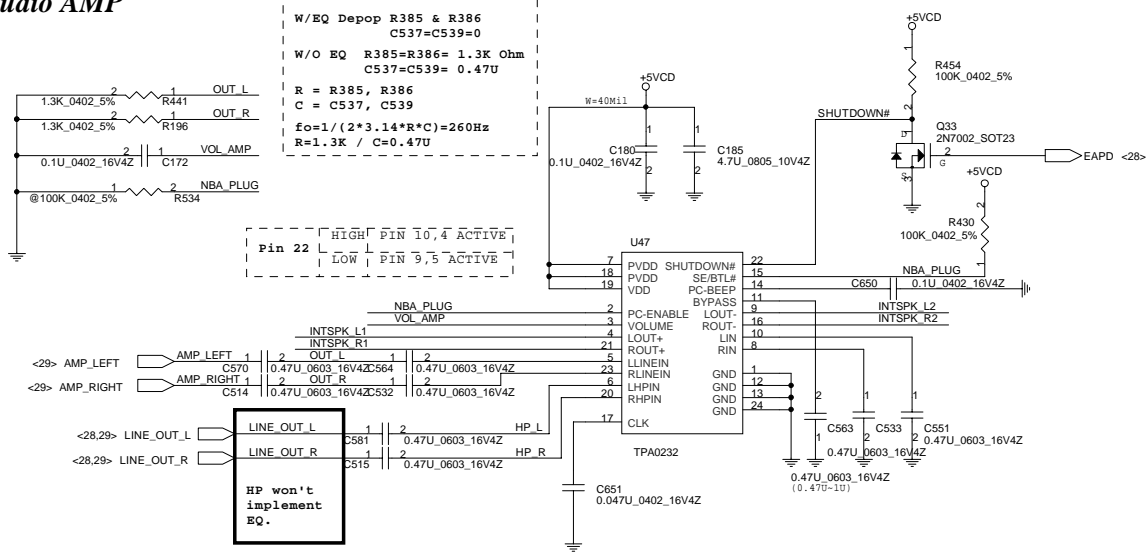
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Audio AMP

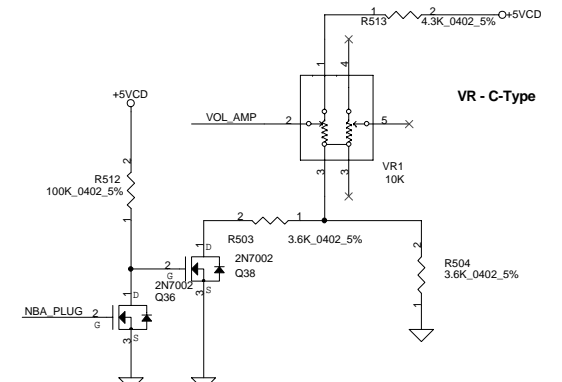
W/EQ Depop R385 & R386
C537=C539=0
W/O EQ R385=R386= 1.3K Ohm
C537=C539= 0.47U

R = R385, R386
C = C537, C539
 $f_o = 1 / (2 * 3.14 * R * C) = 260\text{Hz}$
R=1.3K / C=0.47U

Pin 22 HIGH PIN 10,4 ACTIVE
Pin 19 LOW PIN 9,5 ACTIVE

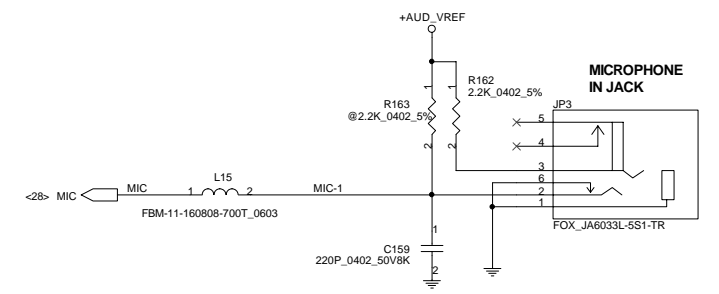
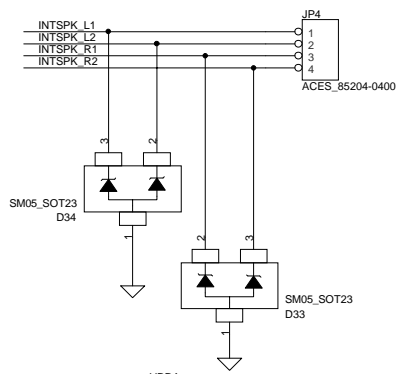


	W/EQ	W/O EQ
R513	4.3K	4.3K
R504	3.6K	3.6K
R503	6.2K	3.6K
Bias (Gain)	SPK 0.687 V 10 dB HP 1.006 V -2 dB	SPK 0.560 V 12 dB HP 1.006 V -2 dB

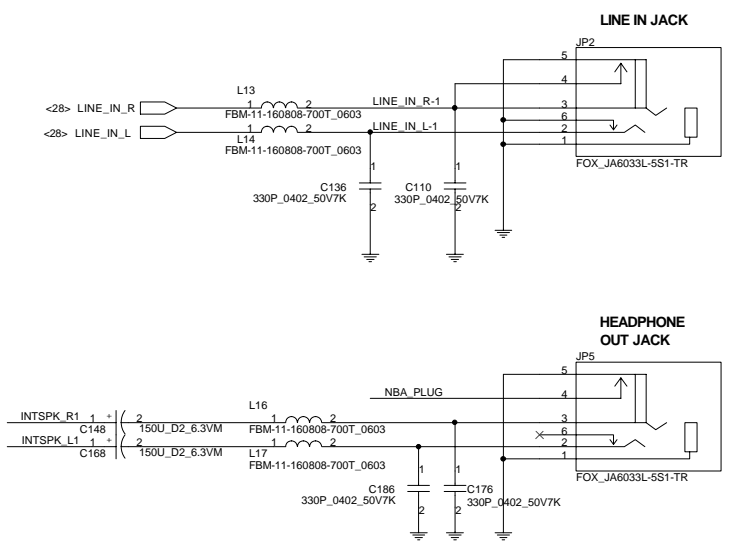
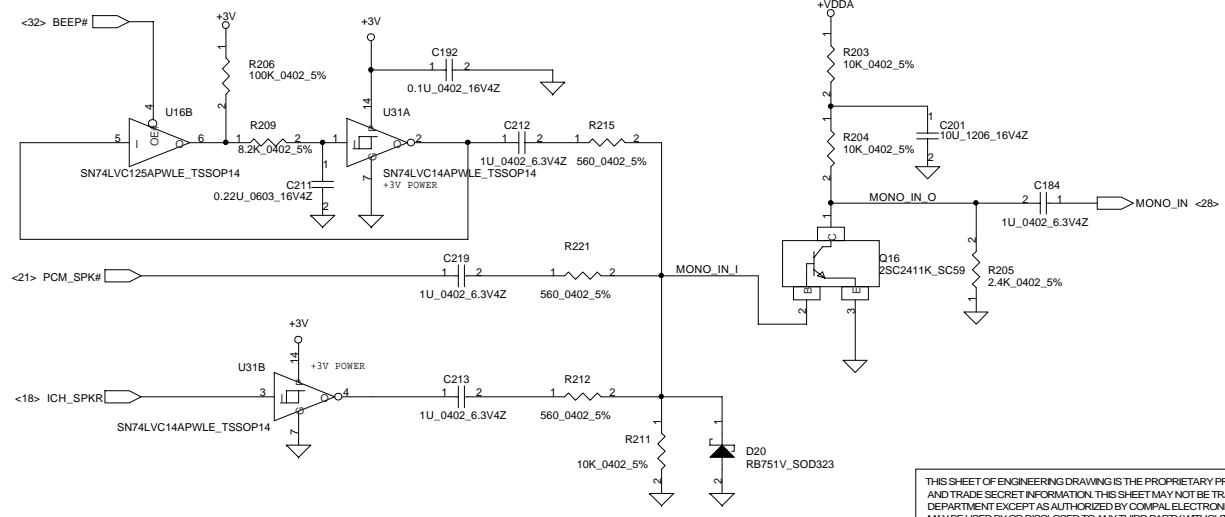


HP won't implement EQ.

Speaker Connector



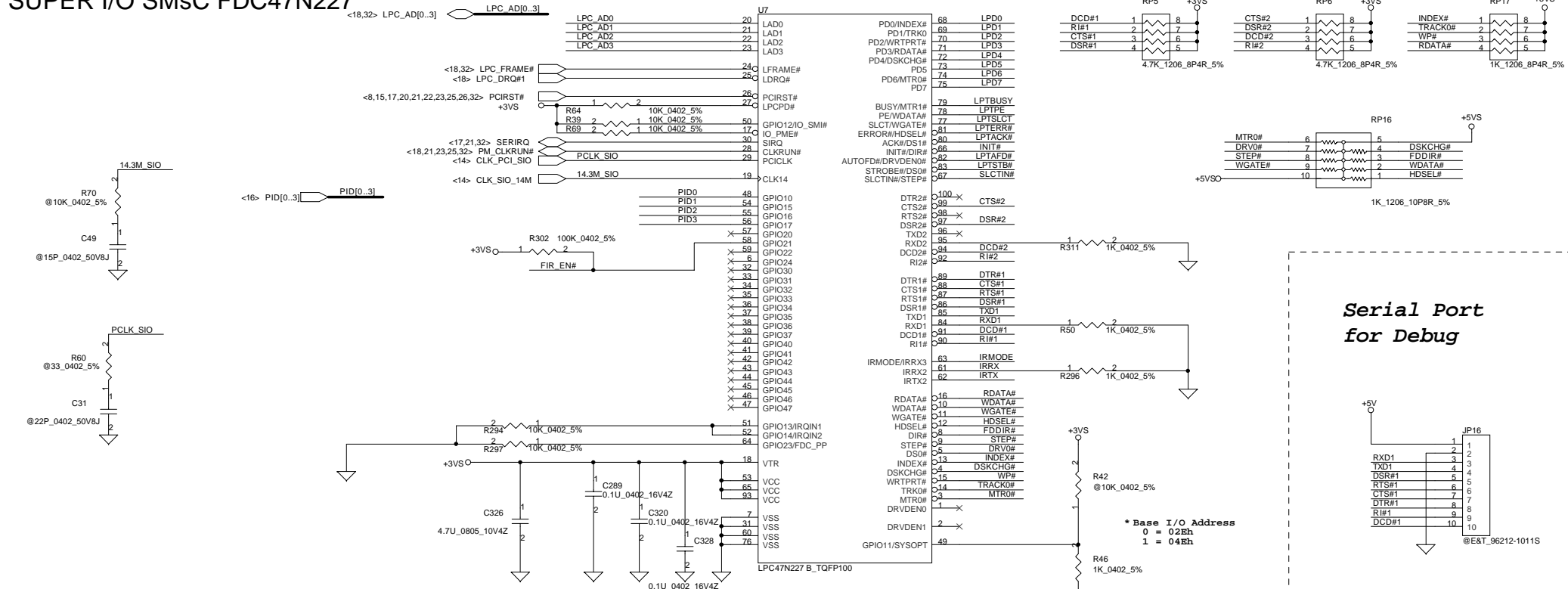
System Sound



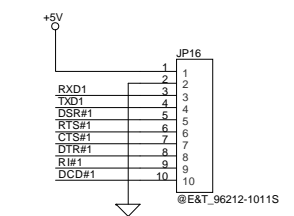
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SUPER I/O SMC FDC47N227

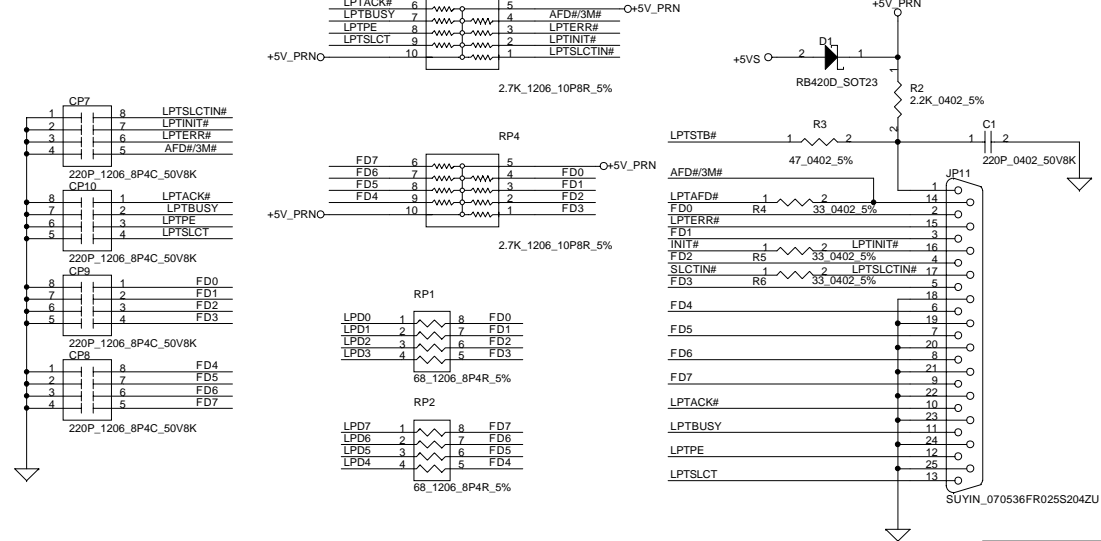


Serial Port for Debug

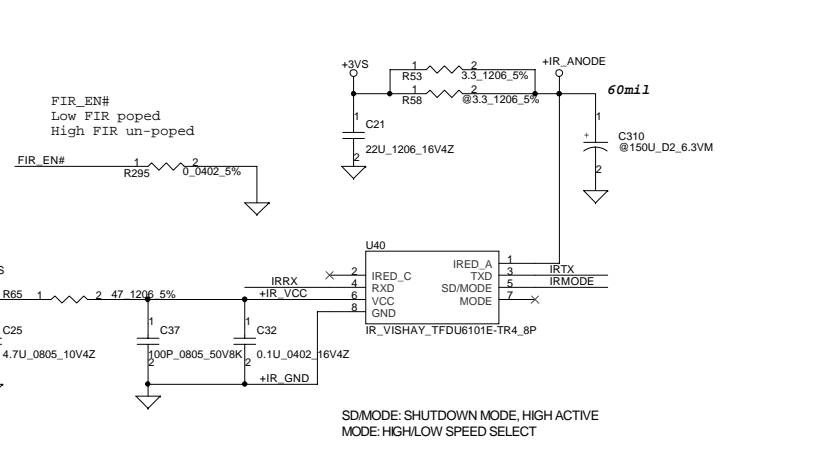


* Base I/O Address
 0 = 02Eh
 1 = 04Eh

Parallel Port

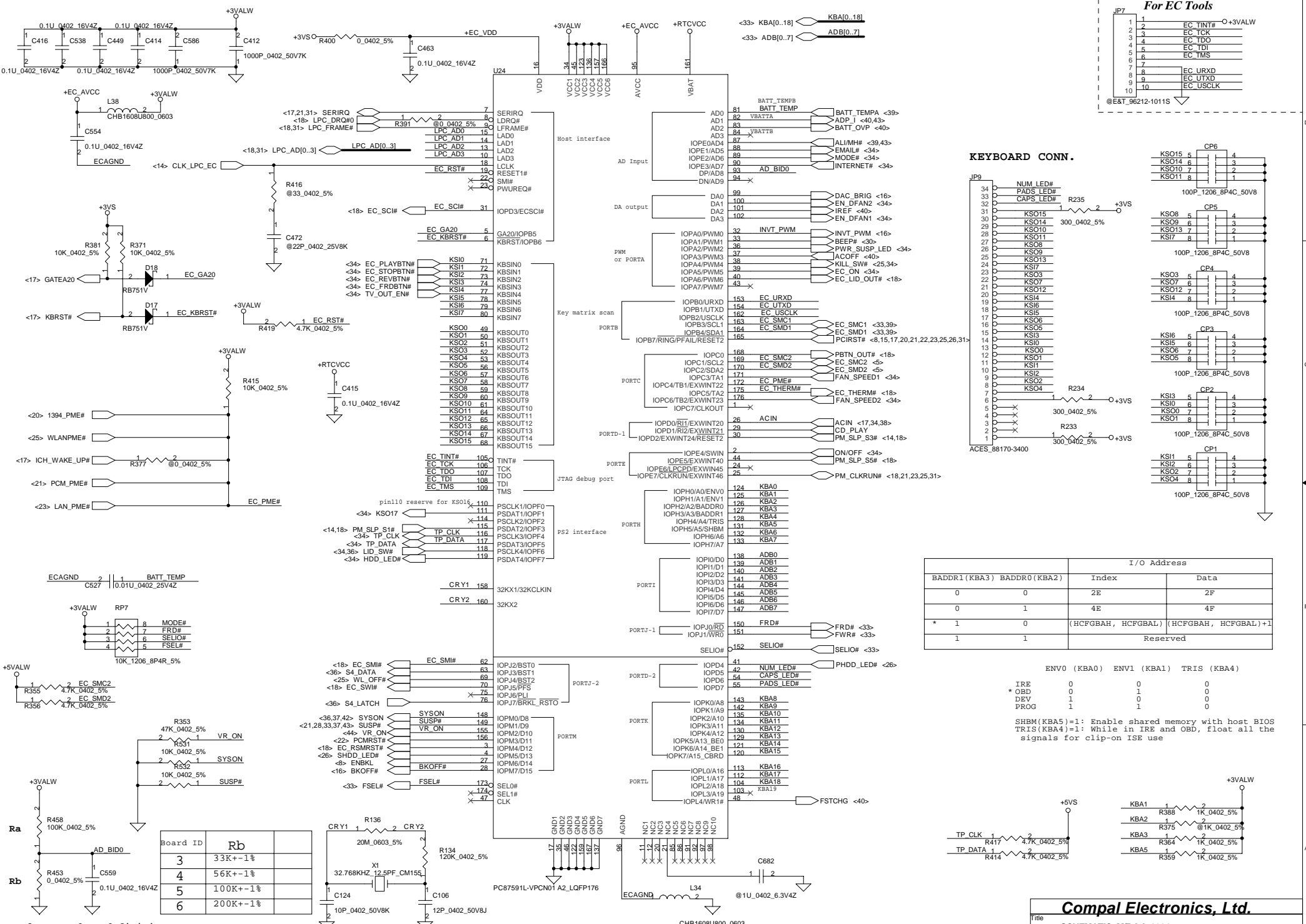


FIR Module

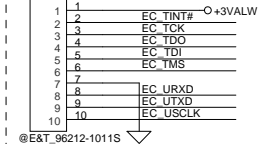


SDMODE: SHUTDOWN MODE, HIGH ACTIVE
 MODE: HIGH/LOW SPEED SELECT

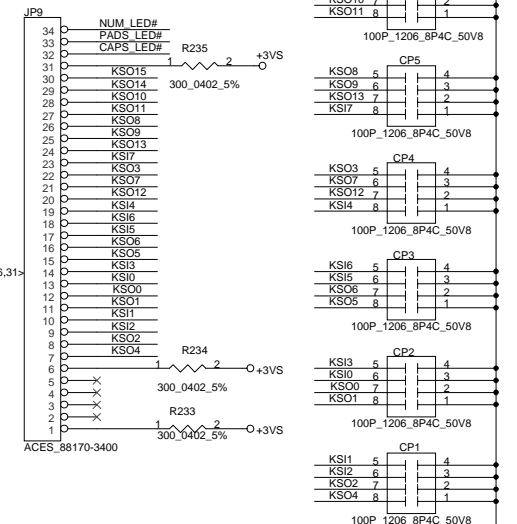
Compal Electronics, Ltd.
 SCHEMATIC, M/B LA-1931



For EC Tools



KEYBOARD CONN.



I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1	Reserved	

	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

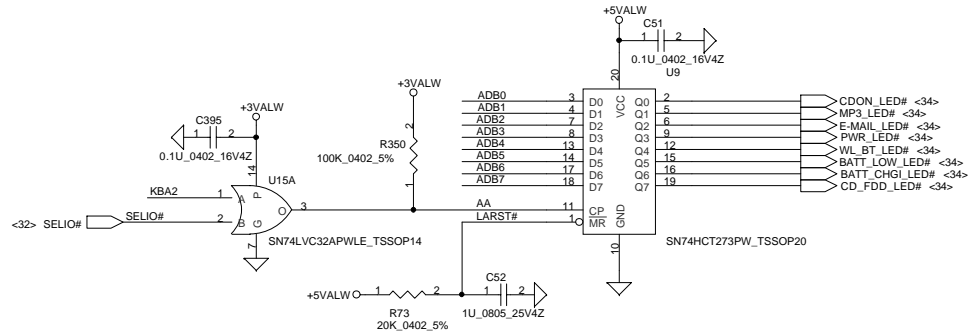
SBM(KBA5)=1: Enable shared memory with host BIOS
 TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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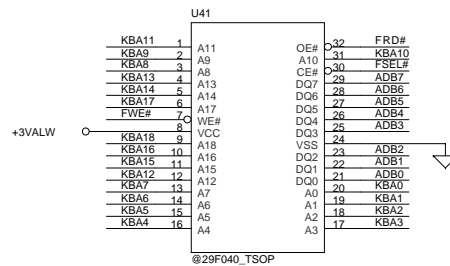
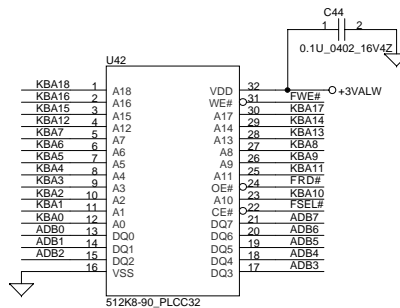
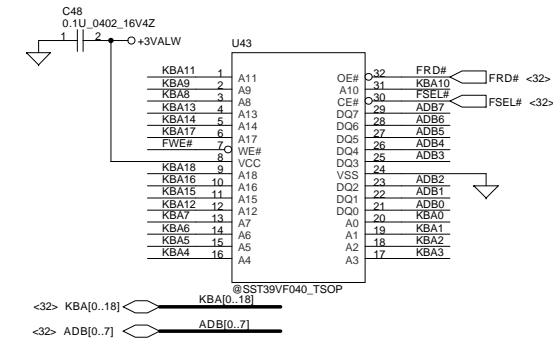
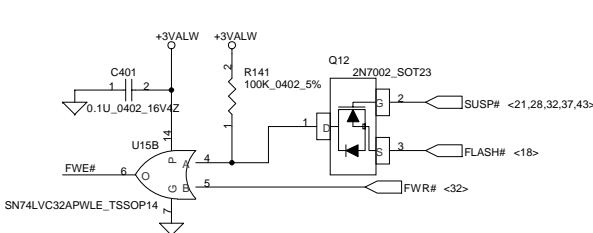
Schematic, M/B LA-1931

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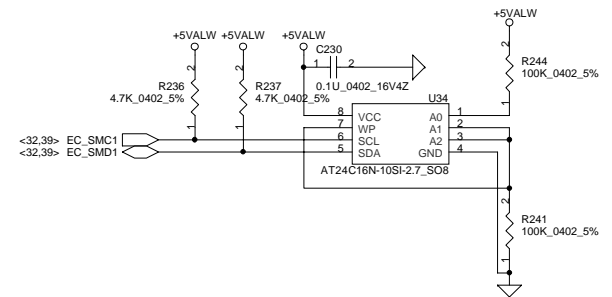
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System BIOS



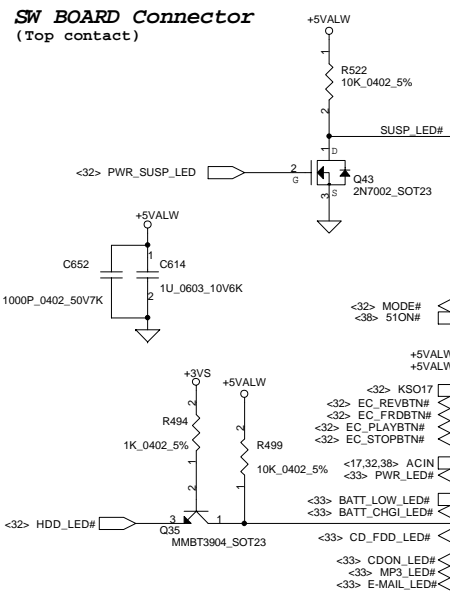
SMBus EEPROM



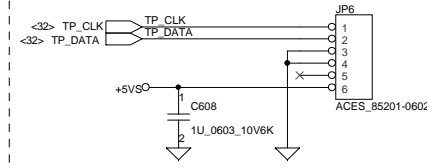
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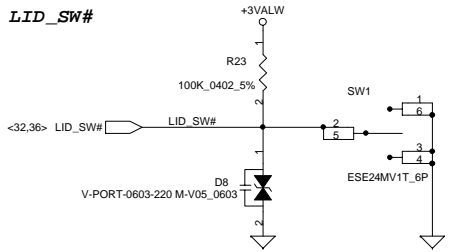
SW BOARD Connector
(Top contact)



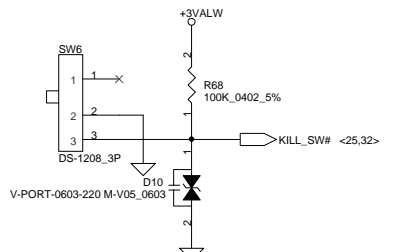
Touch Pad Connector



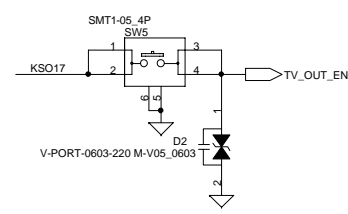
LID_SW#



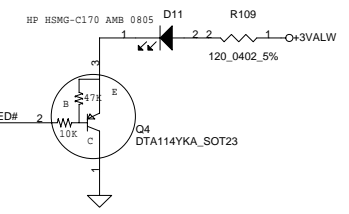
Kill SWITCH



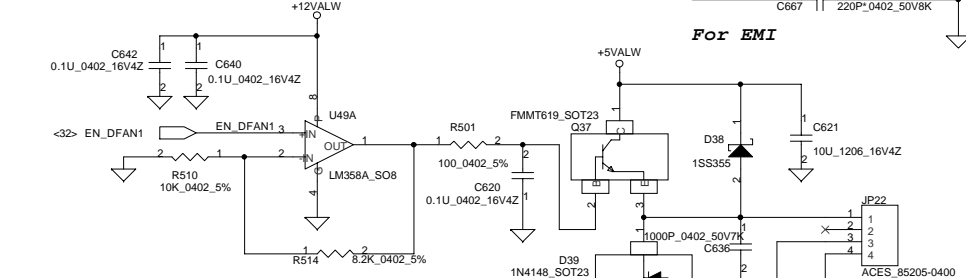
TV-OUT BUTTON



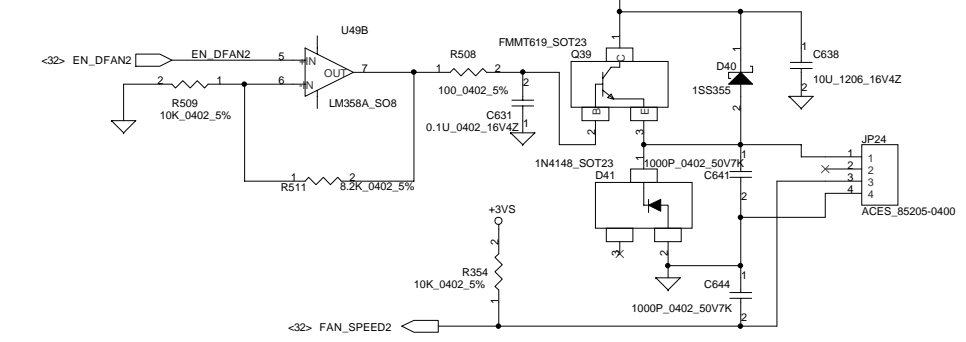
WIRELESS ACTIVE AMB LED



FAN CONN. 1



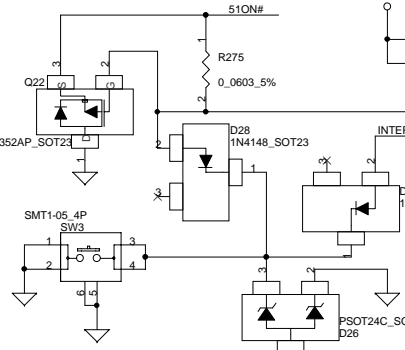
FAN CONN. 2



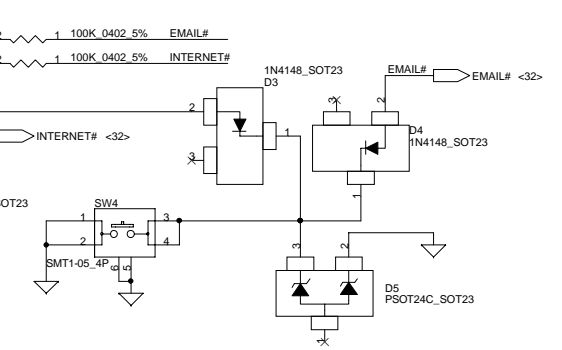
For EMI

51ON#	C653	100P_0402_50V8K
MODE#	C654	100P_0402_50V8K
KSO17	C655	100P_0402_50V8K
EC REVBTN#	C656	100P_0402_50V8K
EC FRDBTN#	C657	100P_0402_50V8K
EC PLAYBTN#	C658	100P_0402_50V8K
EC STOPBTN#	C659	1000P_0402_50V7K
ACIN	C660	100P_0402_50V8K
PWR_LED#	C661	1000P_0402_50V7K
SUSP_LED#	C662	100P_0402_50V8K
BATT_LOW_LED#	C663	1000P_0402_50V7K
BATT_CHGI_LED#	C664	100P_0402_50V8K
HDD_LED#	C665	100P_0402_50V8K
MP3_LED#	C666	100P_0402_50V8K
E-MAIL_LED#	C667	220P_0402_50V8K

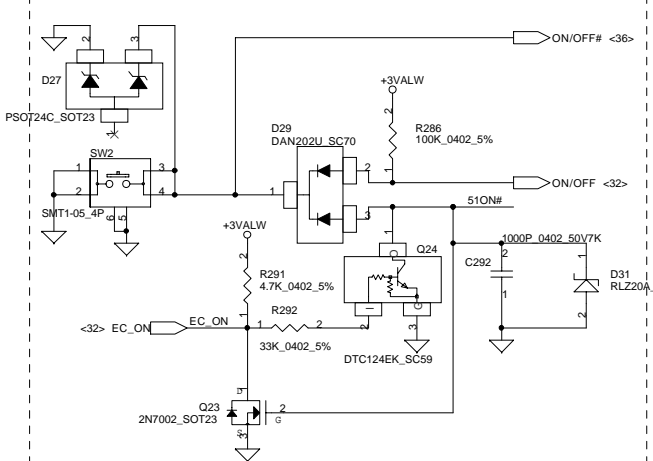
Internet Button



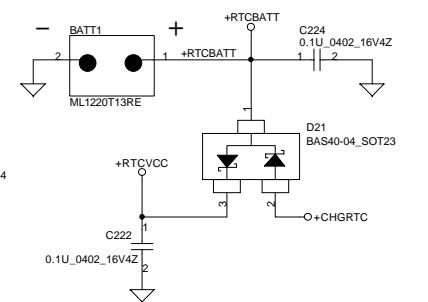
User Button & E-MAIL SW



Power Button



RTC BATT



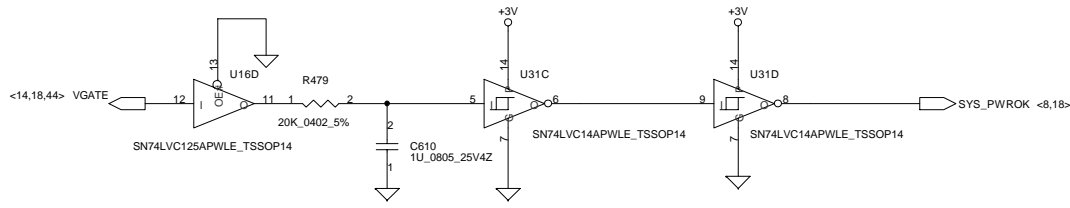
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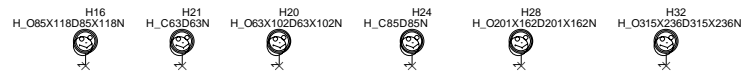
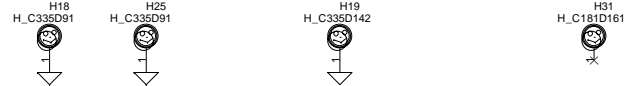
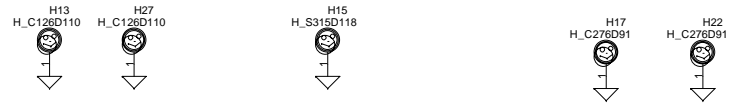
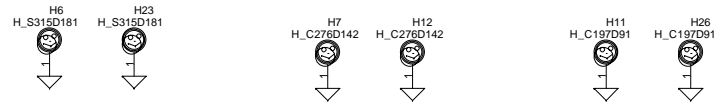
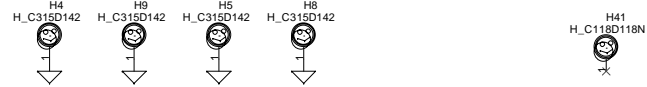
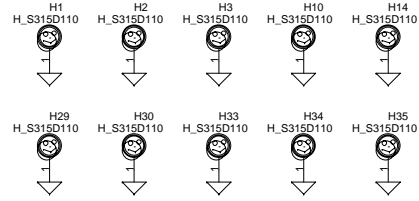
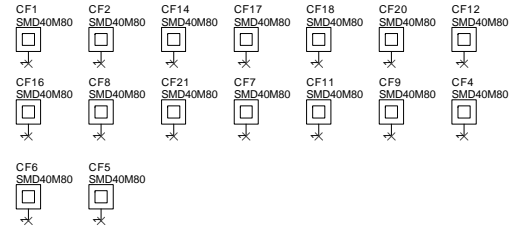
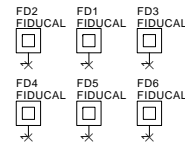
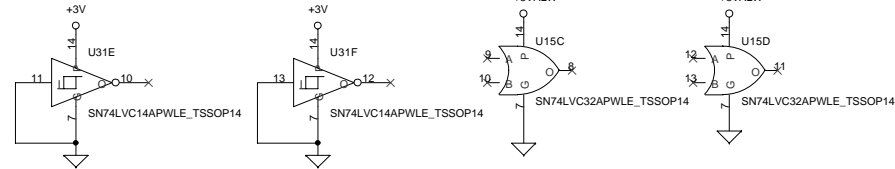
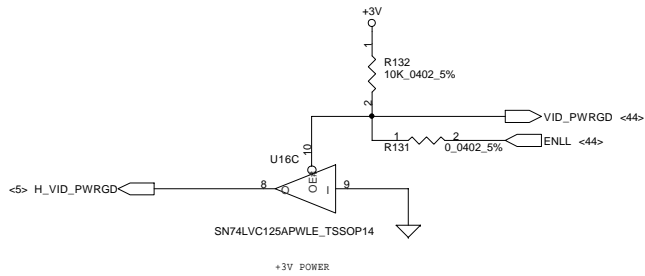
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Power Good Circuit



VID_PWRGD

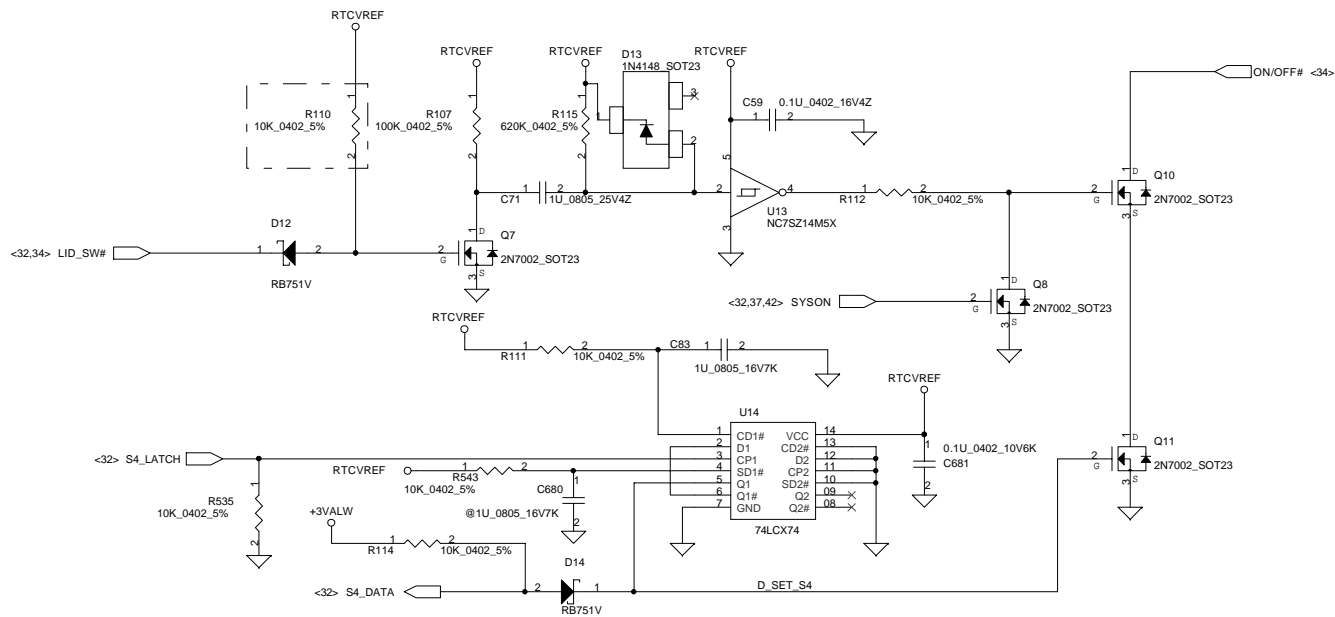


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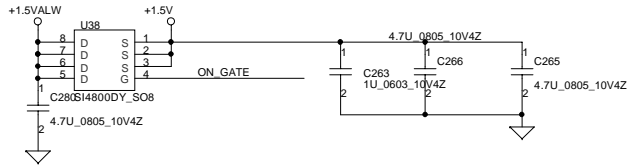
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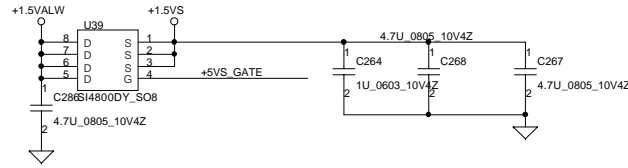
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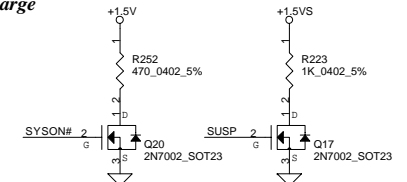
+1.5VALW To +1.5V Transfer



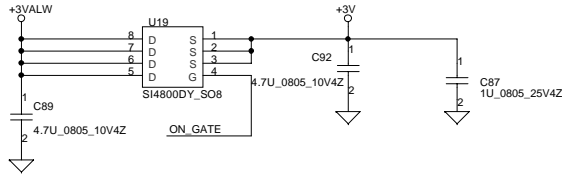
+1.5VALW To +1.5VS Transfer



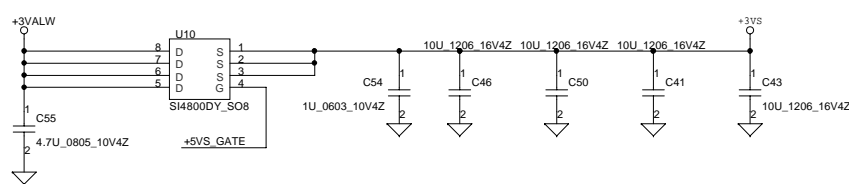
+1.5V & +1.5VS Discharge



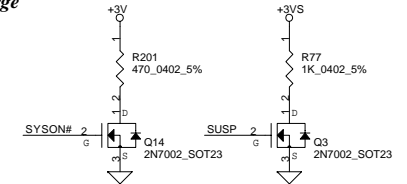
+3VALW To +3V Transfer



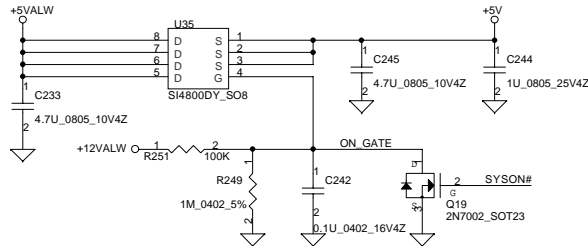
+3VALW To +3VS Transfer



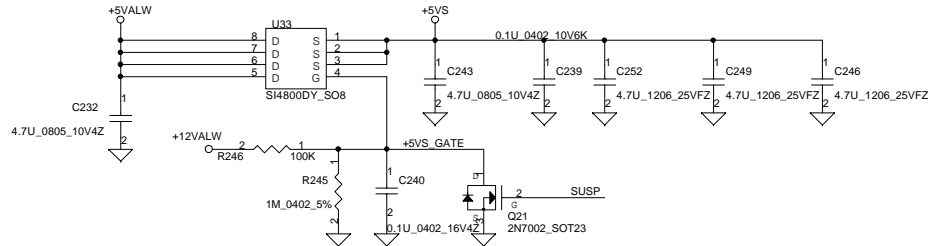
+3V & +3VS Discharge



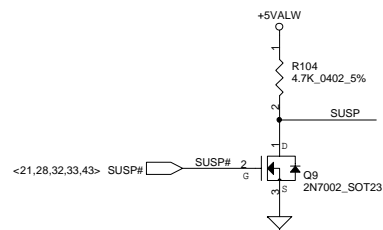
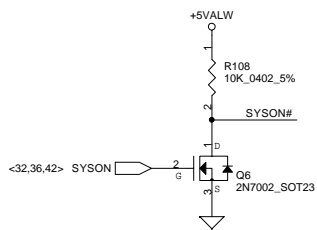
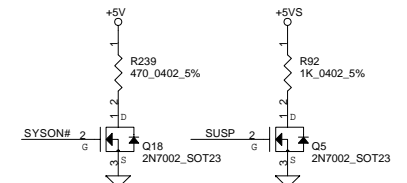
+5VALW To +5V Transfer



+5VALW To +5VS Transfer

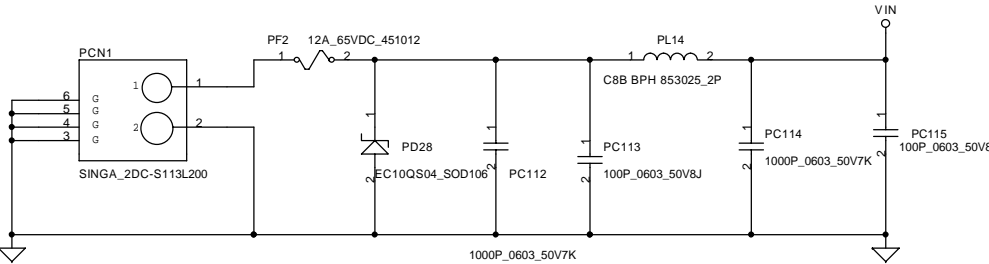


+5V & +5VS Discharge

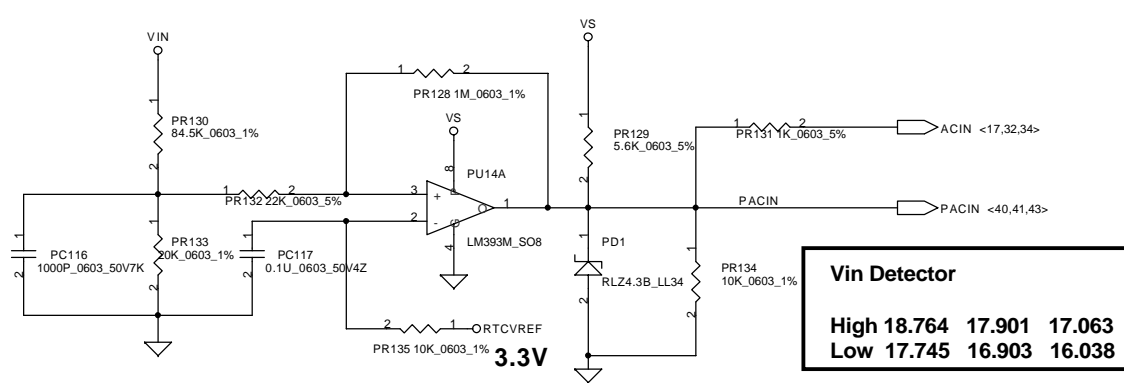


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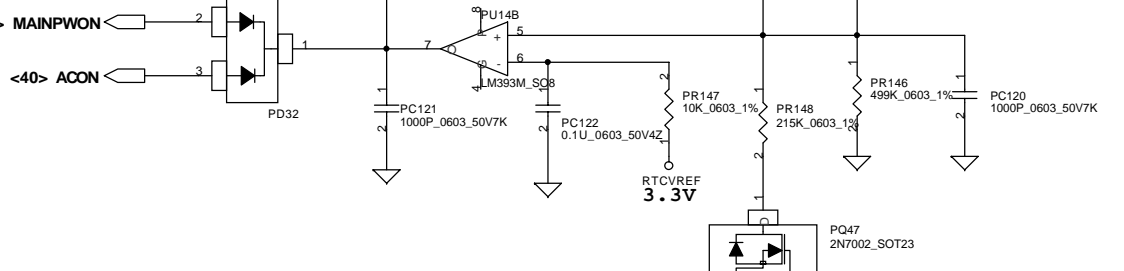
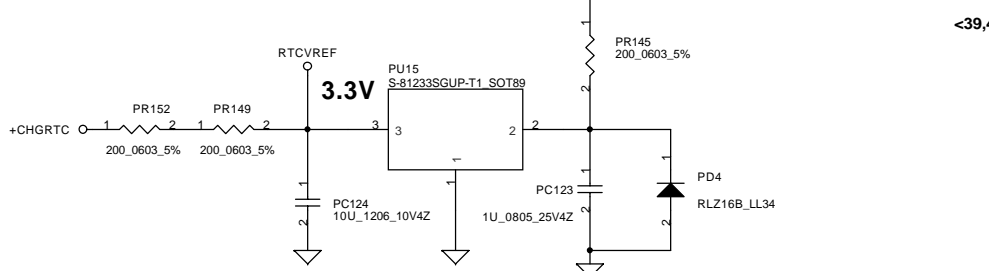
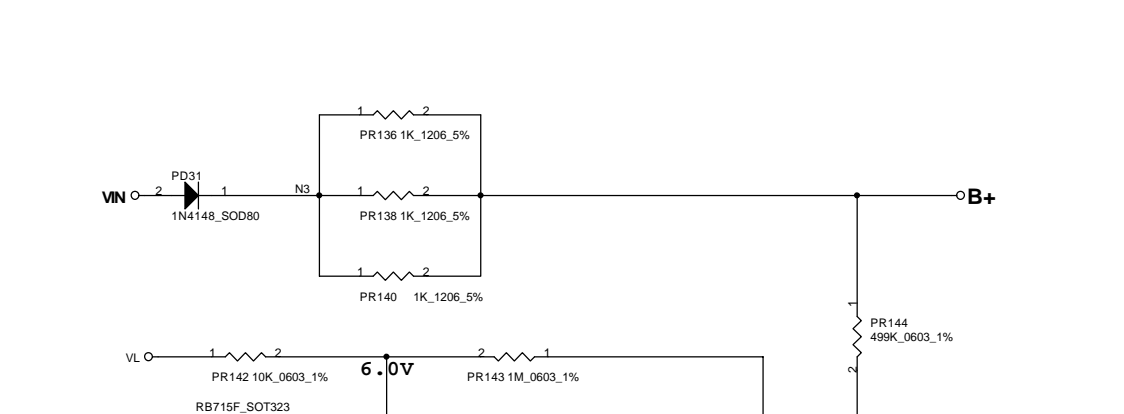
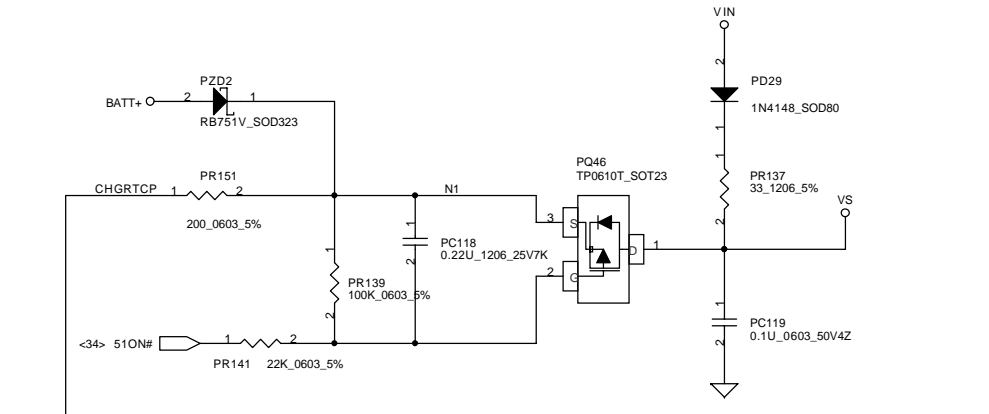
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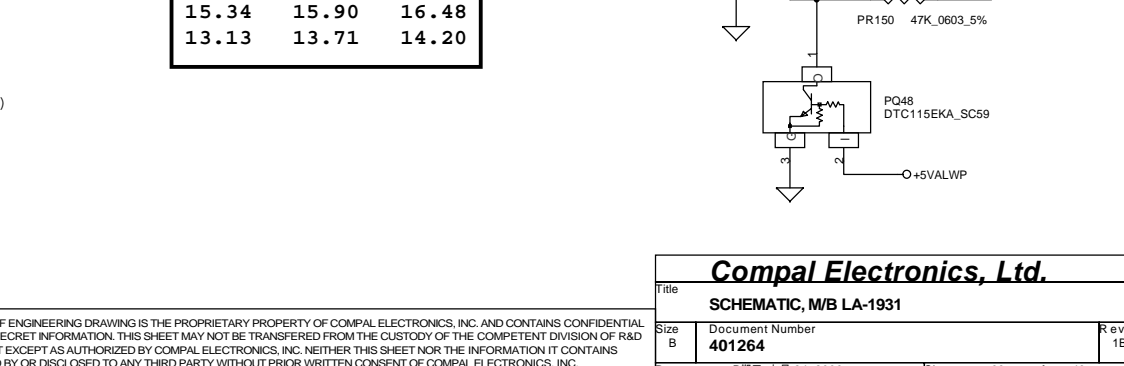
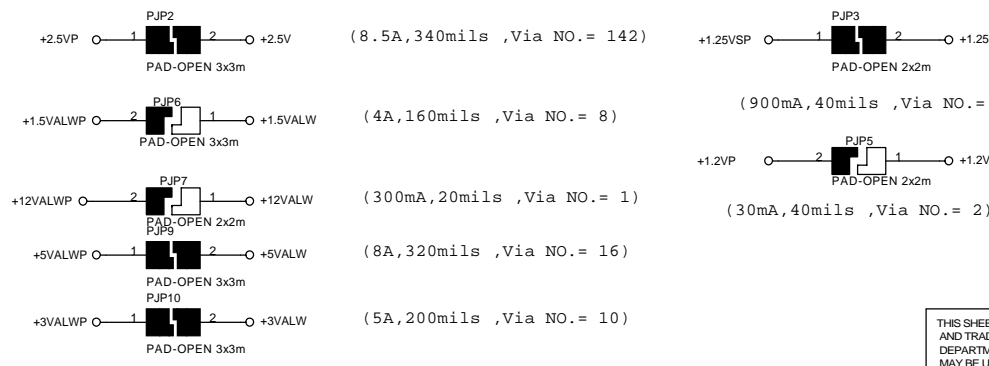
SINGA_2DC-S133L200	120W
SINGA_2DC-S726B201	90W



Vin Detector		
High	18.764	17.901 17.063
Low	17.745	16.903 16.038

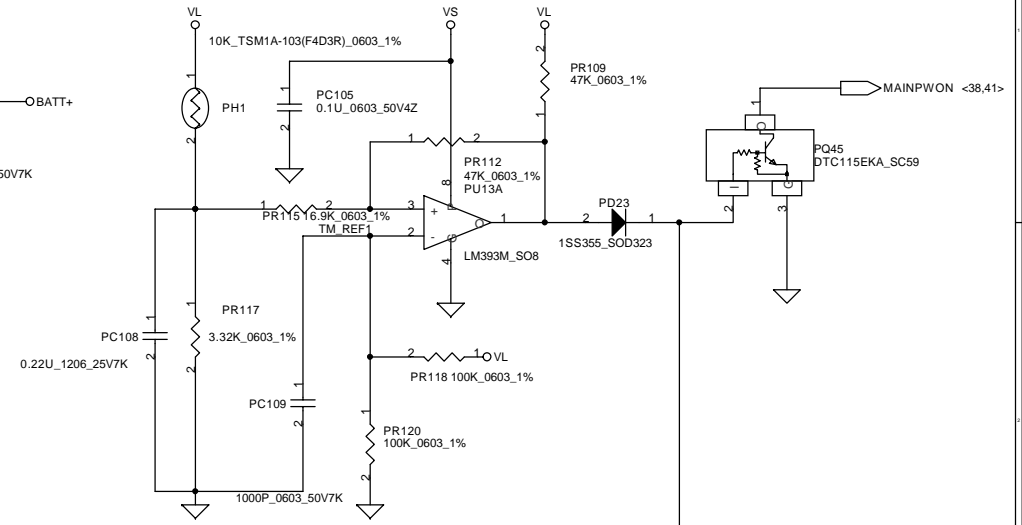


Precharge detector		
<39,41> MAINPWON	15.34	15.90 16.48
<40> ACON	13.13	13.71 14.20

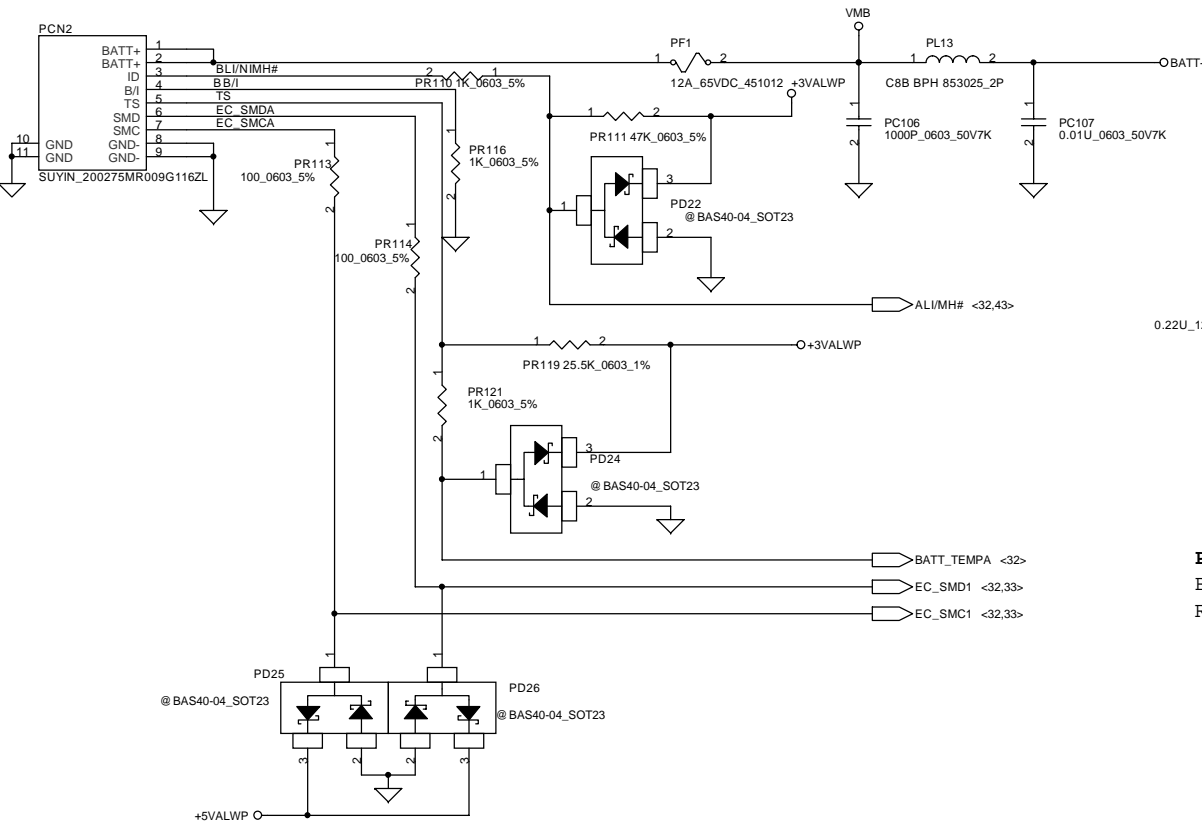
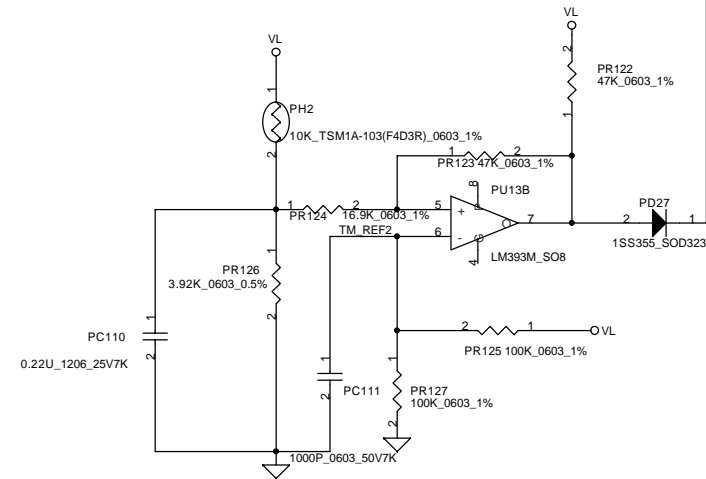


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PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 44(45) degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 78 degree C
 Recovery at 39(40) degree C



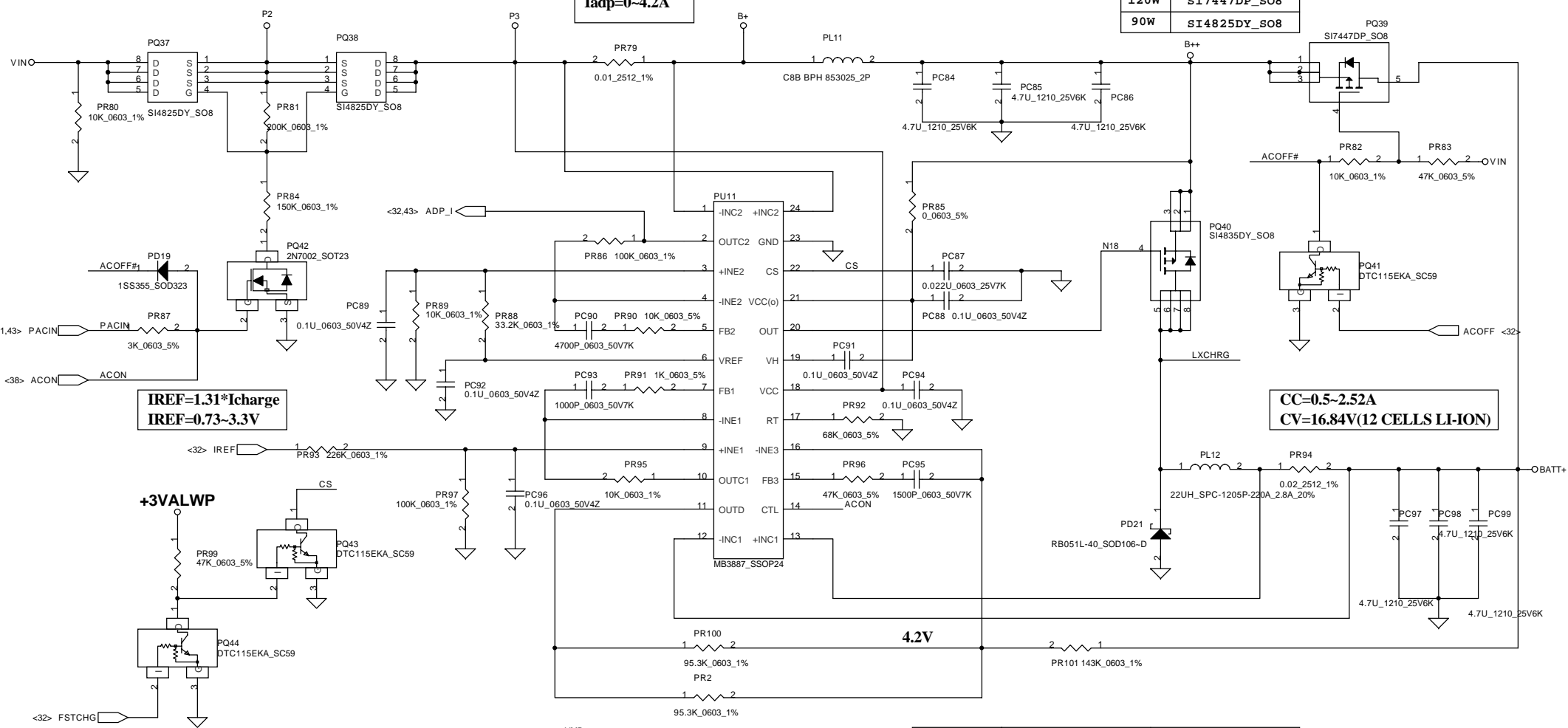
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	PQ39
120W	SI7447DP_SO8
90W	SI4825DY_SO8

Iadp=0-4.2A



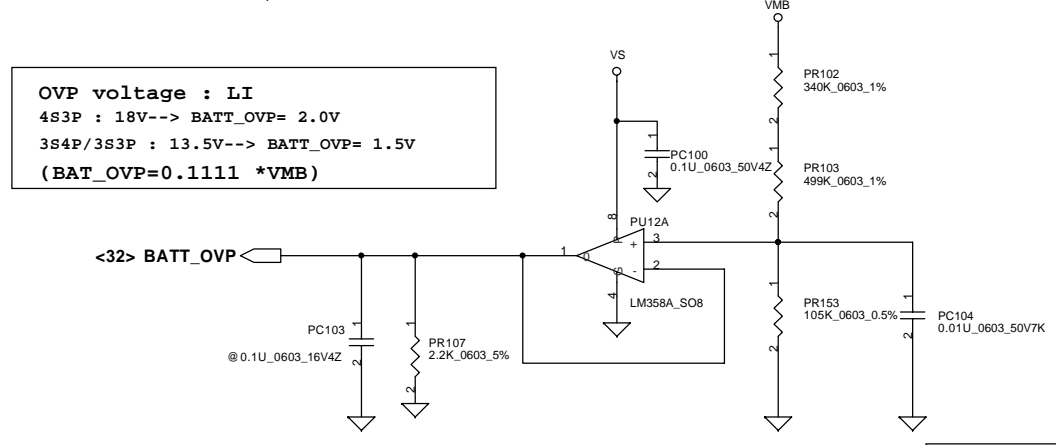
IREF=1.31*Icharge
IREF=0.73-3.3V

CC=0.5-2.52A
CV=16.84V(12 CELLS LI-ION)

+3VALWP

OVP voltage : LI
4S3P : 18V--> BATT_OVP= 2.0V
3S4P/3S3P : 13.5V--> BATT_OVP= 1.5V
(BATT_OVP=0.1111 *VMB)

	120W	90W
PR79	0.01_2512_1%	0.015_2512_1%
PR86	100K_0603_5%	10K_0603_5%
PR88	33.2K_0603_1%	29.4K_0603_1%
PR90	10K_0603_5%	4.7K_0603_5%



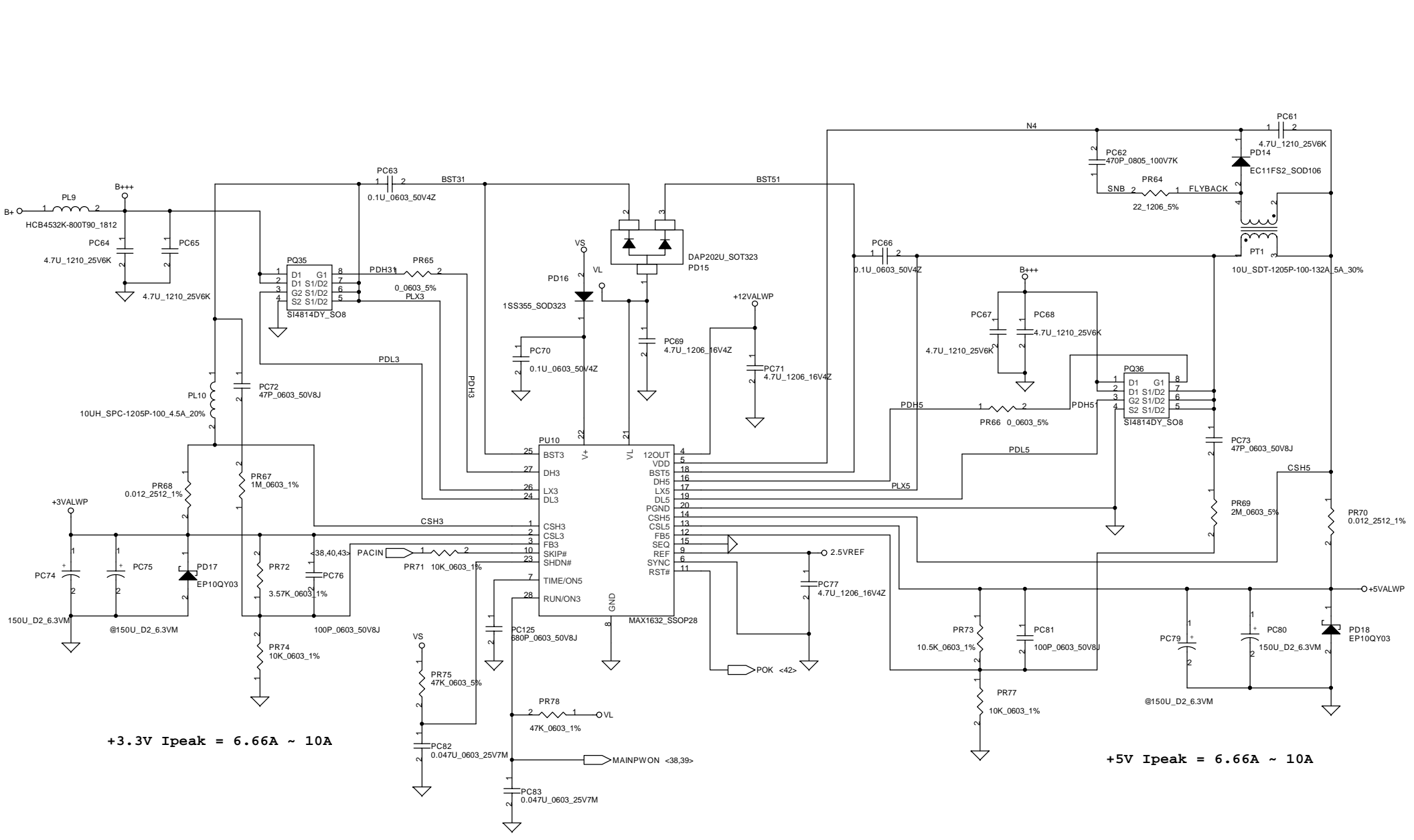
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Size B Document Number **401264** Rev 1B

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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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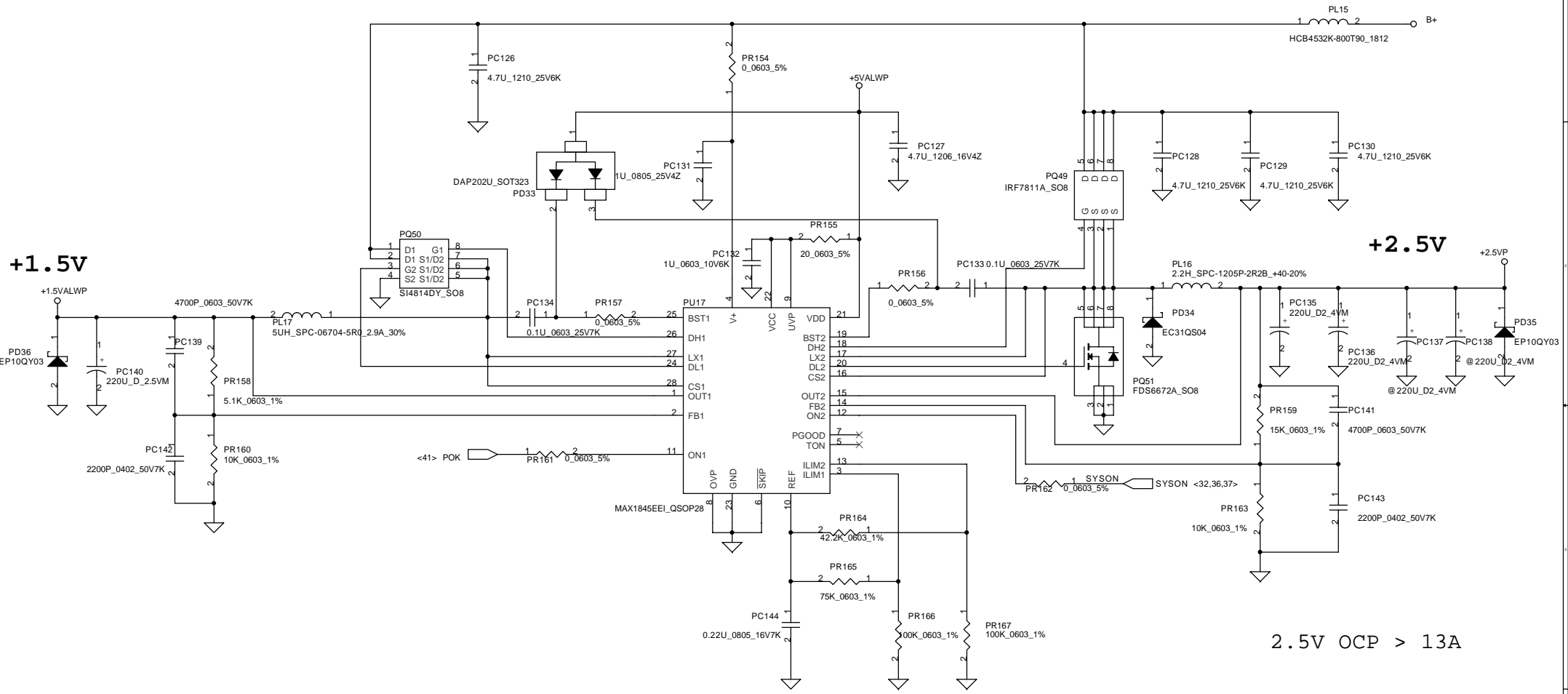
+2.5V/+1.5V

+1.5V

+2.5V

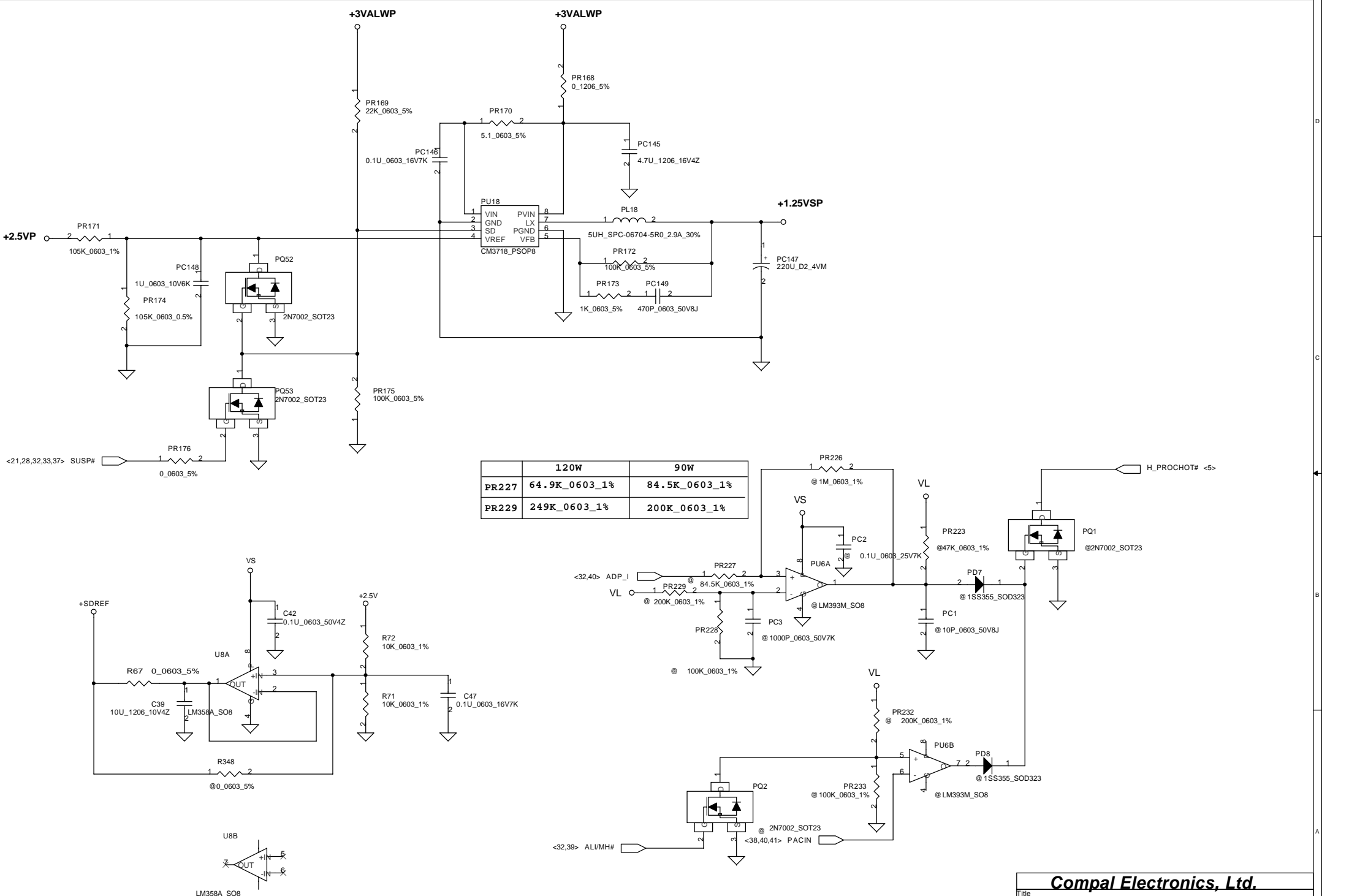
+2.5VP

2.5V OCP > 13A



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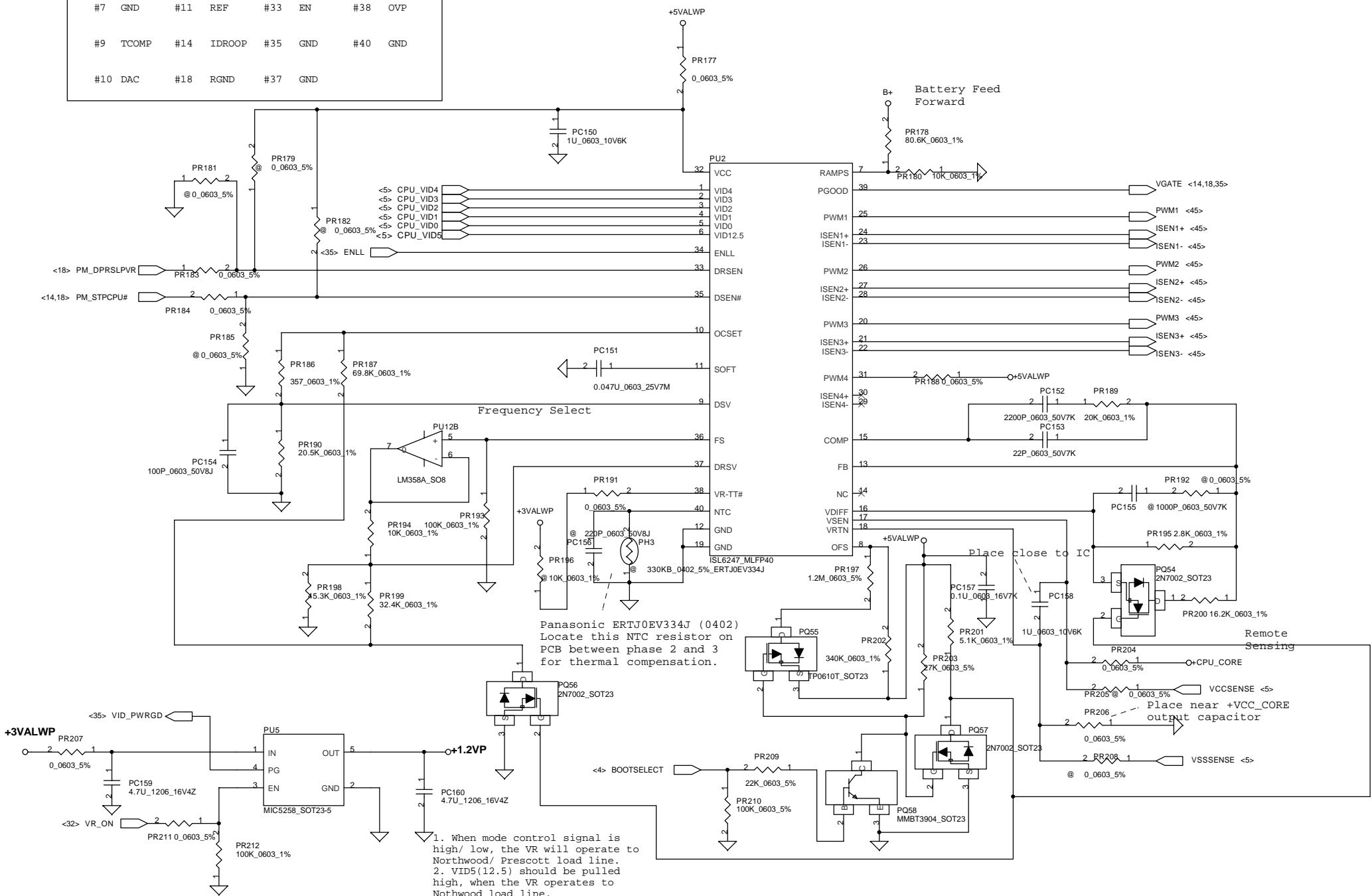
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#7 GND	#11 REF	#33 EN	#38 OVP
#9 TCOMP	#14 IDROOP	#35 GND	#40 GND
#10 DAC	#18 RGND	#37 GND	



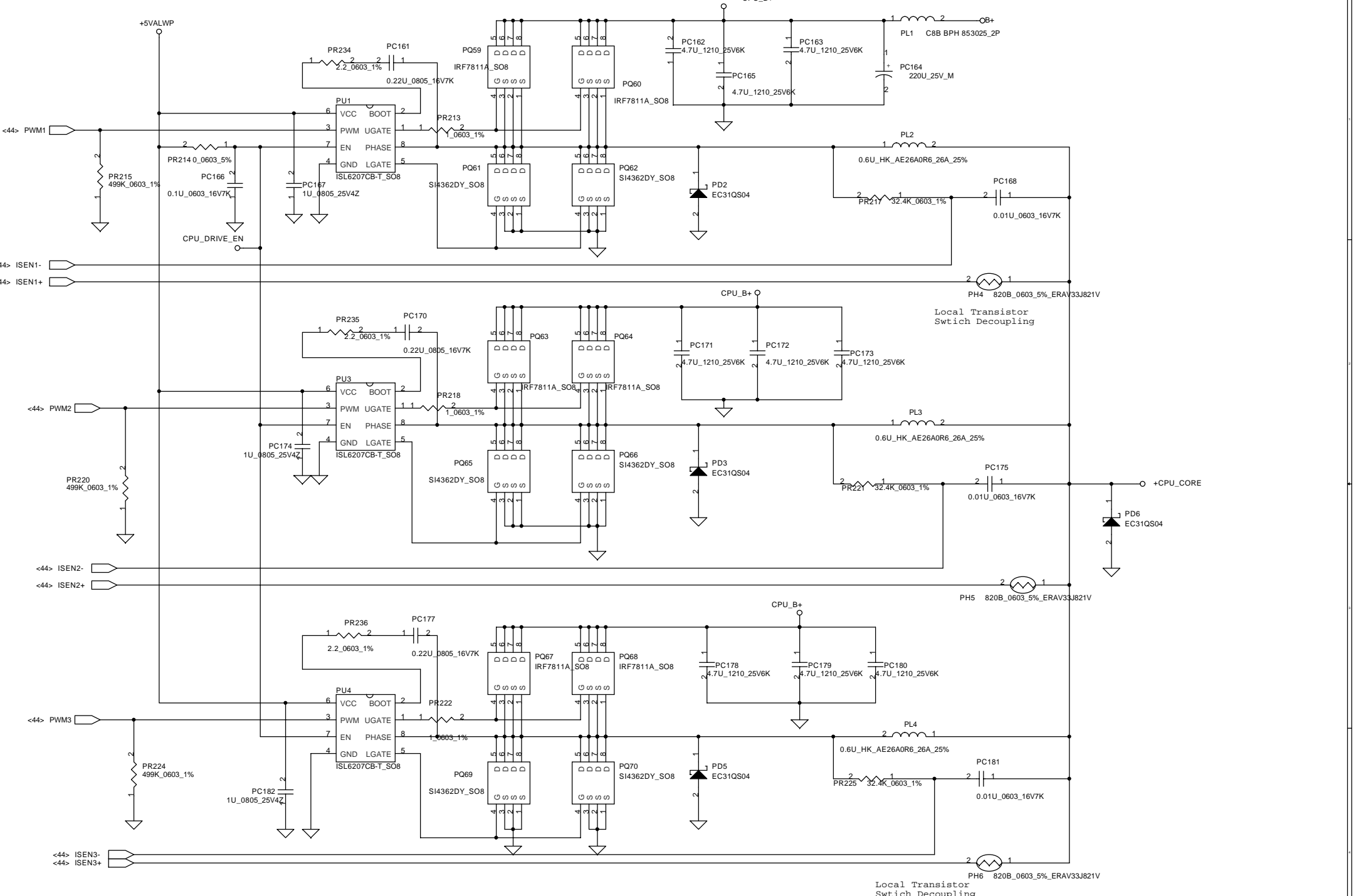
Panasonic ERTJ0EV334J (0402)
Locate this NTC resistor on PCB between phase 2 and 3 for thermal compensation.

1. When mode control signal is high/ low, the VR will operate to Northwood/ Prescott load line.
2. VID5(12.5) should be pulled high, when the VR operates to Northwood load line.

BOOTSELECT=1 PRESCOTT
BOOTSELECT=0 NORTHWOOD

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Local Transistor Switch Decoupling

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REV 0.1

Date	Page	Description
04/10	21	Delete Power interface short line.
04/13	21, 22	Change Card Bus controller as one slote CB1410
	11, 12	Swap RAM data signals.
04/16	29	Add EQ circuit
	43	Add throuloling circuit.
	26, 31	Add FIR and Remove SW DJ cicuit
04/24	17	Add R569 and R570 for Layout Request. Move Signal IRQE#~H# from RP92 to RP91 and del RP92.
	14	CLK-GEN. pin 1(VDD_REF) and pin 46(VDD_CPU_0) change power plan as +3V_VDD. Suggestion from ICS C249 and C251 change power plane as +3VDD
04/25	45	PL4 swap pin1 and pin2.
	6	Change CPU Decoupling CAP. from 22U_1210_6.3V6M to 22U_1206_6.3V6M (H=1.6)
	32	1. EC GPIO signal HDD_LED# move from pin114 to pin119. 2. Add signal PM_SLP_S1# on EC GPIO pin115.
	28	Q44 for +5VCD change part name as U55
04/28	8	Del R73, cause it duplicate pull high.
	27	Change C478 and C488 from 150U to 10U
	36	Change R480 from 560K to 620K Ohm
	4	Add R571 for BOOTSELECT
	5	Add R573 for OPTIMIZED/COMPAT#
	18	Add R572 for signal PM_DPRSLPVR
04/29		Rename from Layout
04/30	33	R73 0402 -> 0603 and C52 0805 -> 0603
	16	C2, C5, C259, C3, C4, C6, C260, C261 and C262 Link CIS.
	5	Thermal Sensor : Del R62, R61 8.2K-->200Ohm and power +5VS -> +3VS, C27 value 0.1U -> 1U, Sensor power rout direction : +3VS -> R61 -> C27.1 -> U6.1
	17	Add Q40 and Q41, R517 and R518 for SMBus isolate solution.
05/01	8	Change CRT_HSYNC -> INTCRT_HSYNC and CRT_VSYNC -> INTCRT_VSYNC on MGCH terminal.
05/02	33	Remove dummy net on SUSP#.
	16	R28, C277, C278 and C279 modify P/N for CIS link
	17	C215 and C217 modify P/N for CIS link
	22	C145 modify P/N for CIS link
	20	Remove dummy net on Xi
	14	R83 and R94 modify P/N for CIS link
05/03	32	CP4 pin2 add connected to GND
05/05	42	PR151 pin1 SYSON signal --> MAINPWON
	8	Swap U26.B6 (INTDDCDA) and U26.G9 (INTDDCCK) --> U26.B6 (INTDDCCK) and U26.G9 (INTDDCDA)
	9	+SDREF circuit move to page 44
	6	Modify Cap.s location same with Layout
	14	Change R129 net from PM_SLP_S3# to PM_SLP_S1#
	16	Add R519 and R520 for EC protect
05/06	20	EEDI_LAN --> EEDI_1394; EECK_LAN --> EECK_1394
	27	Remove R26. Delete USBEN# and U3.3, U3.4, U32.3 and U32.4 connect to GND. Delete R30, R279, R258 and R257. Change C273, C284 and C646 220U -->150U.
	42	PR151 pin1 SYSON signal --> POK; PU10 pin 11 output POK.
	5	R324 size 0603 -> 0805
	32	U24.175 ATF_INT# --> EC_THERM#
05/07	28	Add L42 between GND and AGND by EMI request.
	17	R408, remove @ for Intel comment.
	5	R56 60.4_0603_1% --> 51.1_0603_1%; R59 102_0603_1% -> 86.6_0603_1%
05/08	35	H19 GNDA -> GND; H31 GND -> GNDA
	37	C242 0.01U -> 0.1U.
	11	JP21 DDR-SO-DIMM link with CIS.
	29	De-pop EQ components, add @ symbol on components.

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REV 0.2

Date	Page	Description
05/12	35	Change H31 GND --> AGND and H19 AGND --> GND
	37	R104 and R108 power plane changed, +3VALW --> +5VALW
05/29	40	Change PR100 47.5K-->95.3K PR100 47.5K-->95.3K;PQ37,PQ38,PQ39 SI4835DY-->SI4825DY PR79 0.015-->0.01; PR86 10K-->100K ;PR90 4.7K-->10K; PR88 29.4K-->33.2K Add PR2 95.3K
	38	Change PCN1 90W-->120W
	20	U29 Pin 37 pull up with 4.7K Ohm --> U29 Pin 43 change X4 footprint same as X2
	16	Add Protect circuit for EC (Add D42, D43 ,D44 and R521)
	32	PWR_SUSP_LED# --> PWR_SUSP_LED
	34	Add reverse circuit for PWR_SUSP_LED (Add Q43 and R522).
	23	change Y2 footprint same as X2
	36	change J1 ~ J6 footprint from JUMP_2MM to 2MM
05/30	35	Add H41 and change H13 H27 size.
06/02	38	Change PL14 value
	39	Change PL13 value
	45	Change PL1 value
	40	Change PQ39 and PL11 value
	11	Add R523, R524, R525 and R526, Del R515
	12	Add R527, R528, R529 and R530
06/03	6	Delete C281, C287, C300, C309, C317, C324, C327 and C330.
06/05	34	Add C648 and C649 for EMI request
	32	Add R531 and R532 for EC floating issue
	8	Add R533 for DVO device detect

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REV 0.3

Date	Page	Description
06/12	25	Swap IRQG#_MINI2 and IRQH#_MINI
06/30	30	Change sound resource, cause Headphone without EQ.
07/01	40	Modify PQ38 direction
	28	Add regulator : Add Q44, Q45, Q46, D45 and R536 ~ R539.
		Change C95, C129, C385, C386, C399, C404, C441, C422, C438 and C445 size : 0603 -> 0402.
	29	Change R166, R357, R426, R435, R148, R173, R187, R347, R352, R432, R181 and R346 size : 0603 -> 0402.
	30	Change amplifier from TPA6011A4 to TPA0232.
		Add R534, C651 and C650
		Delete R202, R199, R434 and R442.
		Change C563 1U to 0.47U
		Change VR type from A-Curve to C-Curve.
		Change C184, C212, C213, C219 size 0603 -> 0402.
	14	R129 change net from PM_SLP_S1# to PM_SLP_S3#
		Q13 : 2SC2411K --> 2N7002
		R445 : 10K --> 0 Ohm
	10	Change C491 size : 1210 -> 1206; Change C465 and C468 size : 1210 --> D type
	35	Change SYS_PWROK control signal
	25	SWAP PIRQG#_MINI and PIRQH#_MINI_2
07/09	14	U21 and R128 add '@', and R129 remove '@' CLK_PWD#.
	26	U36, U37, C253 and C254 --> @; Add R541 and 542 --> 0 Ohm
	28	Change Q44 --> U59; Add decoupling CAPs., C668 ~ C679.
	35	Change H13 and H27 size
	30	Change ESD diode type near speaker connector. Change D35 and D33 type, Del D34 and D32.
07/10	36	Change S4 resume function power plane +RTC_VCC -> RTCVREF
		Add R543, C680 and C681
	32	Add C682, reserve for PC97551.
07/16	5	R270 R271 R272 R267 R266 R16 R220 1K_0402_5% --> 10K_0402_5%
	32, 8	Delete R412 R399 R369 R390 R485 R306
	16	R304, R314, R317, R310, C318 1_0603_5% -> 1_0402_5%
	18	R422 1_0603_5% -> 1_0402_5%
07/16	5	Add D46 and D47 for EMI solution
	17	Add D48 for EMI solution
	19	Add D49 for EMI solution
	10	C491 C_1210 -> C_1206
	30	MONO_IN GNDA --> GND
07/18	28	Delete L36, L19, L10 and L42
07/21	30	D33, D34 GND --> GNDA
07/22	35	H31 GNDA --> Non-PDH hole.
	29	EQ-1 and EQ-2 GNDA --> GNDA-EQ
		Add R544 for GNDA <-> GNDA-EQ
		Add L44 L45 for EMI request GND <-> GNDA-EQ
	28	Add L36, L19, L10 and L42 for EMI request GNDA <-> GND

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REV 1.0

Date	Page	Description
08/04	28	Reserve C683, C684 and C685 for Audio noise issue R370 --> @ C467 and C458 change as 0.1U for Audio noise issue
08/18	44	PC151 0.033U -->0.047U; PC152 1000P --> 2200P; Add PC153 22P
09/19	44	PR195 2.26K --> 2.8K
09/22	45	PR217 PR221 PR225 48.4K -->32.4K

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